Integrated Circuit Techniques and Architectures for Beamforming Radio Transmitters

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Abstract

This thesis deals with circuit techniques and architectures for beamforming radio transmitters.

A short introduction to the concept of beamforming is firstly given with the purpose of highlighting it as a technology for reducing the output power specification of the power amplifier in a wireless transmitter, facilitating its integrability and increasing the system capacity. An overview of the 802.11a Wireless LAN standard as a target application is also made.

Various architectures for a beamforming transmitter are studied with the aim of reducing the overall complexity and the hardware overhead. A direct conversion architecture with a frequency offset in the local oscillator path and phase shifting at one third of the carrier frequency is proposed for the subsequent implementation.

Methods and circuit techniques for phase shifting are researched with respect to phase accuracy and resolution, control linearity and overall complexity. A vector modulator is found to be most suitable for the already proposed architecture.

An 802.11a WLAN transmitter with adaptive beamforming capability is designed. An efficient beamforming architecture with a linearly controlled 360° phase shifting range is proposed for linear transmitters. The design of key circuit blocks is discussed. The circuit implemented in 0.25 μm CMOS technology has a -1dB OCP of -7.1 dBm and it consumes 65 mA. It has a phase shifting resolution of 10°.

During the design of the transmitter a resonator loaded LO buffer is found to be potentially common mode unstable, when it is connected to drive a double balanced current steering mixer. The stability margin is shown to be inversely proportional to the quality factor of the resonator load and, therefore, to the power consumed by the LO buffer. A known solution to the problem is compared with two proposed ones. The approaches differ in terms of current consumption, occupied voltage headroom and area.

Some coupling effects in an integrated beamforming transmitter are studied. Analysis shows that with realistic component values the produced beam shape becomes distorted due to coupling. Assuming that the coupling effects are known, predistortion is proposed as a mean to compensate for them.

Acknowledgments

There are many people who inspired me in this work that I am grateful to, I hope I don't forget anyone. First I would like to thank my supervisors Saska Lindfors and Torben Larsen for the guidance and inspiration and all the people in RF Integrated Systems and Circuit Division (RISC) for the help and encouragement. Special thanks to Eva Hansen for the help with the administrative matters, to Ole Kiel Jensen for the fruitful technical discussions and to Peter Boie Jensen for the chip bonding.

I also like to thank my officemates Huseyin Aniktar, Jorge Martires, Per Madsen, Mika Laiho and Ragnar Reynisson for the nice social atmosphere that they have contributed to.

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Contents

Chapter 1

Introduction

The demand for wireless connectivity has increased over the last years. The commercial applications on a vast scale have imposed tight constrains on the mobile terminals with respect to their cost, size and efficiency. As a result a large part of the current electronic research is focused on the single chip integration and on the reduction of power consumption of the wireless transceivers. (Fig. 1.1)

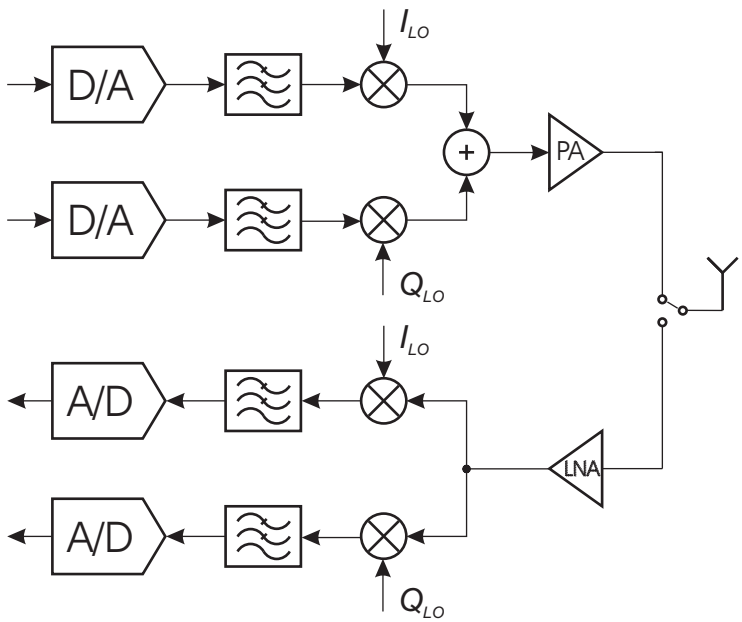


Figure 1.1: A wireless transceiver

The scope of this work is limited to the transmitter side of a mobile terminal because the Power Amplifier (PA) usually dominates the power consumption of the transceiver. In the common case of a single omnidirectional

(isotropic) antenna all the power is transmitted equally in all directions. This is inherently inefficient because the communication in a wireless network is of point to point nature and all the transmitted power that is not directed towards the intended user is wasted. *Introducing directivity to the antenna will ensure that a larger portion of the transmitted power is captured by the target receiver, which will inherently improve the power efficiency.* As a result the power amplifier needs to consume less power in order to produce the same received signal strength at the receiver, which prolongs the battery life of the mobile terminal.

It is highly desirable to be able to control the directivity of the antenna in an electronic way in order to avoid bulky moving mechanical components. According to the antenna theory [1] an antenna can be steered in an electronic way by delaying the signals applied to an antenna array or by changing their relative phasing (Fig. 1.2) so that the propagation delays between the transmitted signals are compensated for a particular direction at which a coherent signal addition takes place. In the other directions at the same

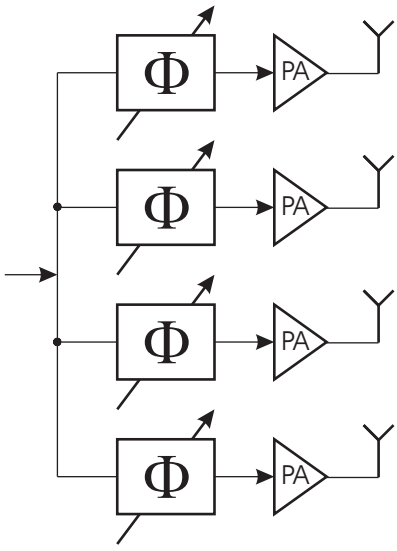
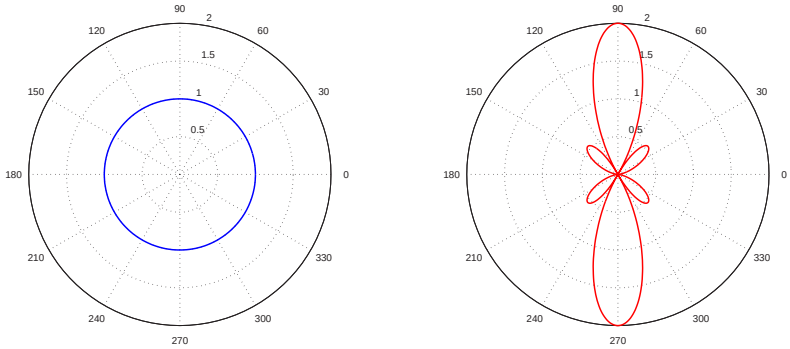


Figure 1.2: A general structure of a beamforming transmitter with four antennas

time there is partial or full signal cancelation leading to forming of a beam. If it is necessary to control the shape of the beam the amplitudes of the antenna signals must be controlled as well. The beam width is proportional to the number of antennas but even a few antennas result in considerable improvement compared to the case of a single antenna (Fig. 1.3). For a narrow band system the delay is usually approximated by a phase shift [2] due to the difficulties in implementing a true delay on chip.



(a) An omnidirectional antenna pattern

(b) A pattern of linear array of four isotropic antennas with 0^0 relative phase shift and half a wave length spacing

Figure 1.3: Patterns of an omnidirectional antenna and an array of four omnidirectional antennas radiating equal total power

Typically the dimensions of an antenna are strongly dependent on the wave length of the transmitted signal. High operating frequency results in a small antenna size. On the other hand, the separation between the elements of a uniform antenna array is also usually a fraction of the wave length as $\lambda/2$ is the most common choice. Subsequently in order to have the size of the antenna array sufficiently small so that it can easily be fitted on a typical mobile terminal a 5 GHz IEEE 802.11a Wireless Local Area Network (WLAN) standard was chosen as a target application [3]. This standard is mainly intended for relatively short range indoor communications, which limits its coverage, but also reduces the cost of building the network backbone structure. WLAN can be considered simply as substitute or an alternative to the conventional fixed computer networks. However, the inexistence of physical cables allows roaming within the network's coverage area as well as between different networks. WLAN access is already being offered at a number of public places such as airports, libraries, universities, shopping malls ...

In order to reduce the cost it is highly desirable that the system is fully integrated on chip. The CMOS technology is a good candidate for the task because of its low cost and due to the fact that it is the process of choice for systems on chip having large digital core. However, with the scaling of the CMOS technology the supply voltage goes down. (Fig. 1.4) This results in reduced voltage dynamic range. It also limits the maximum output power that on chip PA can deliver. The second limitation can be overcome by the beamforming architecture as well. The required total output power can be distributed between several lower power parallel PAs, making the integration of a "combined" high power amplifier possible.

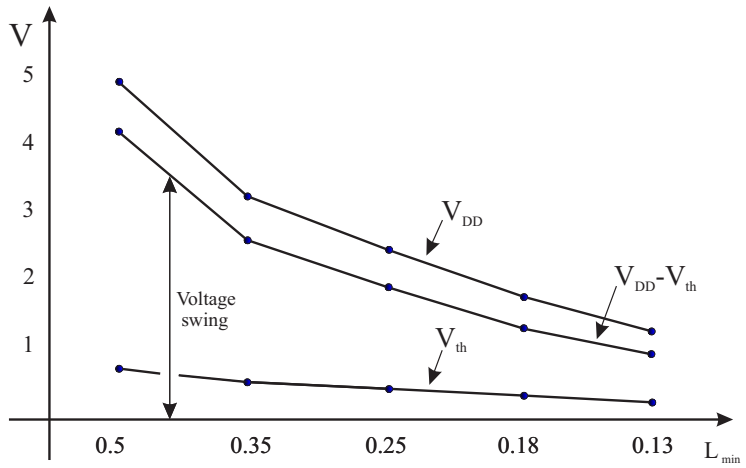


Figure 1.4: Scaling of the CMOS process -V_{DD}, V_{th} and $V_{DD} - V_{th}$ as a function of L_{min}

Apart from reducing the output power requirements of the PA and facilitating its on chip integration the beamforming has the added advantage that it reduces the system capacity by reducing the interference between the communicating devices.

The IEEE 802.11a WLAN standard, which was chosen as target application for this work without limiting the general applicability elsewhere, specifies a radio link in the 5 GHz frequency range. Three frequency bands are allocated depending on the maximum transmitted power as shown in Fig. 1.5. There is a continuous portion from 5.15 GHz to 5.35 GHz, sub-

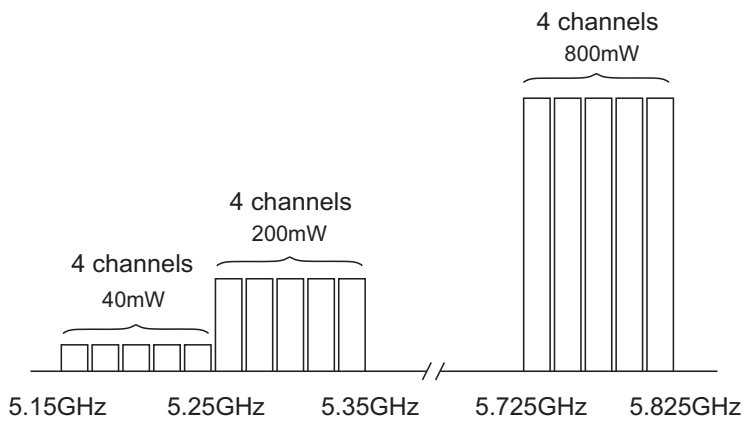


Figure 1.5: Frequency allocation and maximum transmitted output power for IEEE 802.11a (WLAN) standard

divided into two equal 100 MHz parts with maximum output power levels limited to 40 mW and 200 mW correspondingly. The third band occupies a segment from 5.725 GHz till 5.825 GHz and the transmitted power is restricted to 800 mW. It is worth mentioning that only the bandwidth from 5.15 GHz to 5.35 GHz is allocated for this application worldwide. Because the WLAN mobile terminals are quasi-static the formation of the antenna beam does not need to be fast.

In order to make efficient use of the allocated spectrum Orthogonal Frequency Division Multiplexing (OFDM) is specified as a modulation scheme for IEEE 802.11a standard and it has a direct impact on the requirements with respect to the architecture building blocks. OFDM subdivides the carrier into several individually modulated orthogonal sub-carriers all of which are subsequently transmitted in parallel [4]. This transmission scheme offers the following key advantages:

- OFDM is an efficient way to deal with multipath; for a given delay spread, the implementation complexity is significantly lower than that of a single carrier system with an equalizer
- In relatively slow varying channels, it is possible to significantly enhance the capacity by adapting the data rate per subcarrier according to the signal to noise ratio of that particular subcarrier
- OFDM is robust against narrowband interference, because such interference affects only a small percentage of the subcarriers
- OFDM makes single-frequency networks possible, which is especially attractive for broadcasting applications

Nevertheless OFDM has some disadvantages namely:

- Greater sensitivity to frequency offset and phase noise compared to a single carrier system
- Large Peak-to-Average Ratio (PAR), which affects the power efficiency of the RF power amplifier

The IEEE 802.11a WLAN standard employs OFDM with N=52 sub carriers. Forty-eight of them are data sub-carriers and the remaining four with corresponding numbers -21, -7, 7, 21 are pilot sub-carriers used for synchronization. There is no sub-carrier placed at DC in order to make the scheme robust against offset and 1/f noise. The resulting signal occupies 20 MHz of bandwidth and is shown in frequency domain in Fig. 1.6. The sub carriers are offset at 0.3125 MHz from each other and depending on the propagation conditions can have different modulation ranging from binary phase-shift keying (BPSK) till 64-level quadrature amplitude modulation (64-QAM) for the highest data rate (Table A.1). The IEEE 802.11a WLAN transmitter has

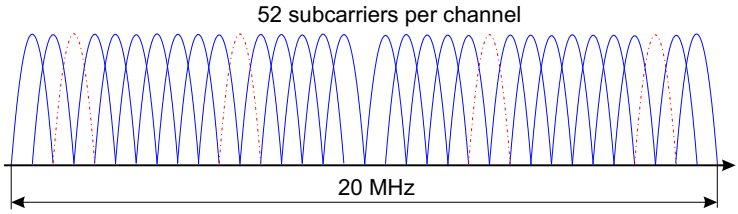


Figure 1.6: Frequency domain representation of an OFDM signal consisting of 52 sub-carriers, occupying 20 MHz of bandwidth

to meet certain modulation accuracy requirement. It is generally specified in terms of Error Vector Magnitude (EVM) error. The modulation accuracy for the given modulation scheme is directly related to the data rate (Table A.2). It is specified in particular by a relative constellation RMS error (Eqn. A.1).

Chapter 2

Transmitter Architectures for Adaptive Beamforming

A real beamforming transmitter is a synergy between system and circuit level techniques. However, for the sake of simplicity the considerations in this chapter are given only from system point of view.

In order to implement a beamforming transmitter, the phase of the transmitted signal at each antenna must be controlled [1]. For the broad validity of the discussion a classical double up conversion transmitter, where the image signals are removed via filtering[1] rather than signal cancellation, is considered from beamforming point of view.

2.1 Baseband phase shifting

The phase of the transmitted signal can be changed before the first up conversion [5, 6]. This can be done in the digital domain prior to the digital to analog conversion, resulting in the architecture shown in Fig. 2.1. The output signal is given by:

$$S(t) = \Re\left\{\left[C(t)\sum_{k=0}^{n-1} e^{jk\varphi}\right] e^{j\omega_{LO_1}t} e^{j\omega_{LO_2}t}\right\} \tag{2.1}$$

Where $C(t)$ is the baseband signal, φ is the relative phase shift and n is the number of antenna elements.

The digital phase shift is very accurate and there is no dedicated hardware phase shifting block. However the solution requires more computing power and the whole transmitter chain from the Digital to Analog (D/A) converter to the antenna has to be multiplied several times with the proper matching between the parallel paths. This inevitably leads to substantial complexity

[1] It is possible to implement a transmitter without any explicit filters if the intermediate frequency and the sampling frequency of the digital to analog converter are high enough

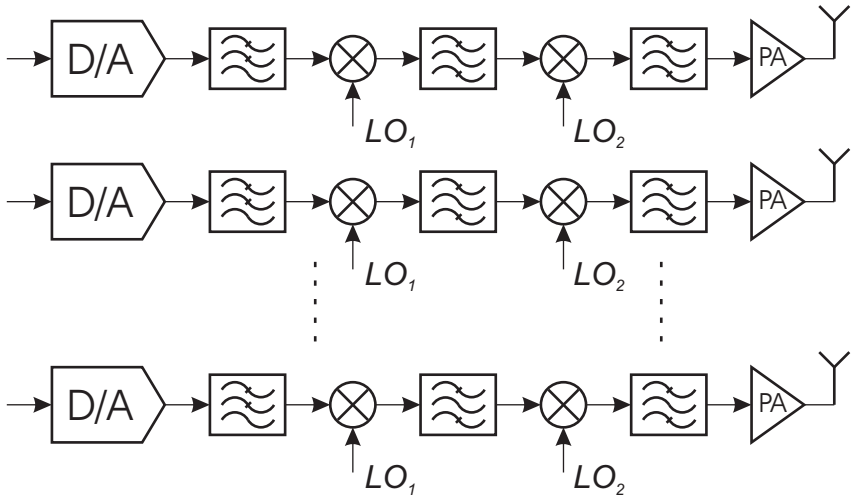


Figure 2.1: A double up conversion beamforming transmitter with phase shifting implemented in the digital domain.

and high power consumption. It is worth mentioning that this structure is suitable for implementing a Multiple Input Multiple Output (MIMO) system, and as such provides more functionality than just beamforming. An implementation of 2×2 integrated (MIMO) system is reported in [5]. Two transmit antennas send two independent data streams simultaneously over the same channel while at the receiver another two antennas receive from both of them. Theoretically if the propagation channel is rich in multipath propagation the data streams can be separated at the receiver in this way doubling the data rate compared to a single antenna system. However, in practice the multiple signal paths are not fully uncorrelated and hence they are not really two separate data streams but something between 1 and 2.

Another possible solution for implementing a beamforming transmitter is to change the phase after the anti aliasing filter. The corresponding architecture is shown in Fig. 2.2. The output signal is given by Eqn. 2.1. The necessary phase shifters usually operate at relatively low frequency of several mega Hertz at maximum facilitating their design. On the other hand, they are at the beginning of the signal path followed by high gain blocks, which makes their noise contribution important. Also depending on the modulation specified by the standard there may be linearity requirements imposed on them. Nevertheless, only the D/A converter and the anti aliasing filter can be shared between the parallel transmitter paths-all other building blocks like the two up conversion mixers and the corresponding band pass image rejection filters plus the power amplifiers need to be multiplied several times.

2.2 Local Oscillator (LO) phase shifting

The phase shifting can take place at the LO path of the first or the second up-conversion [2, 7]. The resulting architectures are shown correspondingly in Fig. 2.3 and Fig. 2.4. The output signal is given by:

$$S(t) = \Re\left\{ C(t) \sum_{k=0}^{n-1} e^{j[(\omega_{LO_1}\omega_{LO_2})t+k\varphi]} \right\} \tag{2.2}$$

Where $C(t)$ is the baseband signal, φ is the relative phase shift and n is the number of antenna elements. Both of them have a major advantage of significantly relaxing the design of the phase shifter. The local oscillator signal is amplitude limited and hence there is no linearity issue. Moreover, if fully switched mixers are used for the up conversion, the amplitude noise originating from the phase shifter and the other circuits in the local oscillator part has a minimal effect on the signal path.

In addition if the system is a Time-Division Duplexing (TDD) one, the phase shifter can be shared between the receive and the transmit paths in a beamforming transceiver. In this case the control values of the phase shifter may be different if the transmit and the receive signals are not at the same frequency, because the radio channel is frequency dependent.

Considering the hardware overhead the second LO phase shifting is more efficient than the first LO one, because only the second up conversion mixers, the RF image reject filters and the PAs have to be multiplied several times. However this advantage is somehow offset by the typically higher frequency of the second LO signal, which makes the design of the phase shifters more difficult.

2.3 Intermediate Frequency (IF) and RF phase shifting

The phase of the transmitted signal can also be changed in the intermediate frequency or in the RF part. Both locations are in the signal path where the noise is not an issue and if the modulation used is not of varying envelope type, the non-linearity of the phase shifters significantly affect the linearity of the whole transmitter. The output signal is given by:

$$S(t) = \Re\left\{ C(t) e^{j\omega_{LO_1}t} e^{j\omega_{LO_2}t} \sum_{k=0}^{n-1} e^{jk\varphi} \right\} \tag{2.3}$$

Where $C(t)$ is the baseband signal, φ is the relative phase shift and n is the number of antenna elements.

The RF phase shifting leads to the most hardware efficient double up conversion transmitter beam-forming architecture. This is evident from Fig. 2.5,

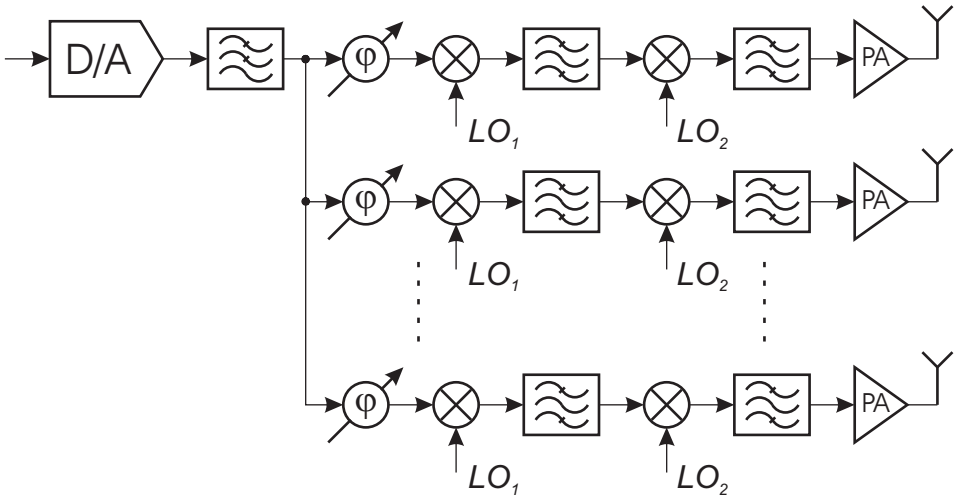


Figure 2.2: A double up conversion beamforming transmitter with phase shifting implemented in the baseband path.

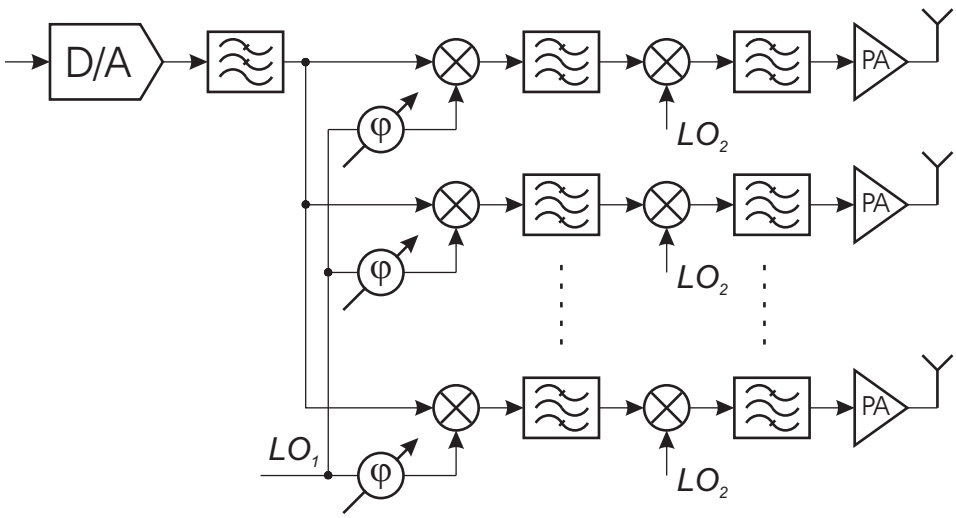


Figure 2.3: A double up conversion beamforming transmitter with phase shifting implemented in the first Local Oscillator path.

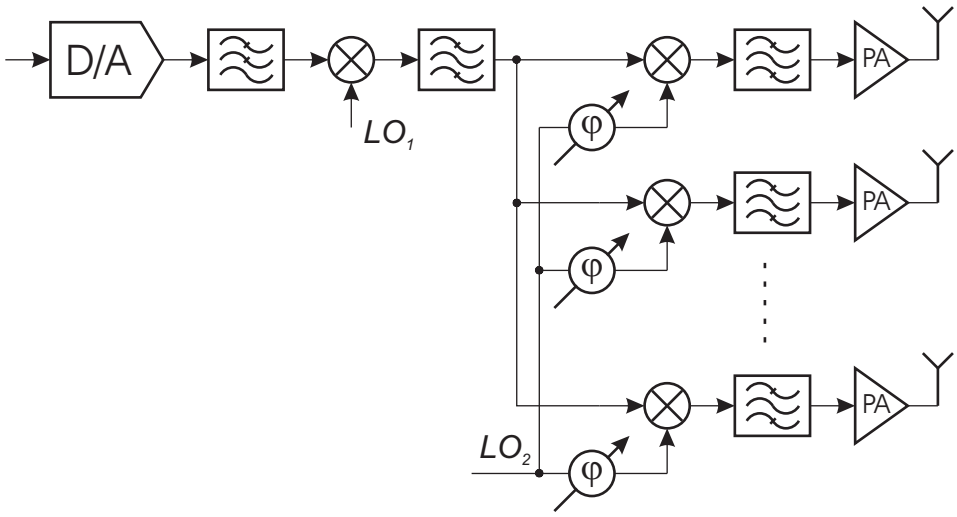


Figure 2.4: A double up conversion beamforming transmitter with phase shifting implemented in the second Local Oscillator path.

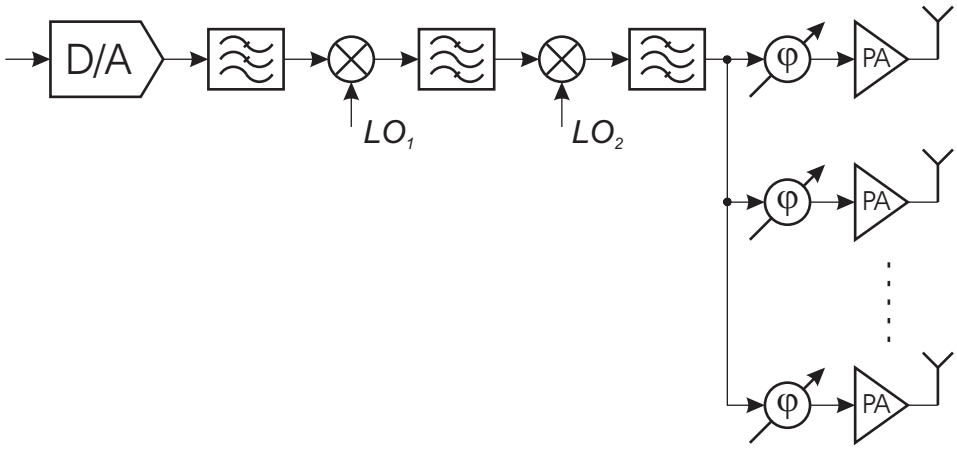


Figure 2.5: A double up conversion beamforming transmitter with phase shifting implemented in the RF path.

where only the power amplifiers need to be multiplied several times. However the phase change takes place at high signal levels and the highest possible frequency. All these make the design of the phase shifters quite challenging.

The phase shifting in the IF path (Fig. 2.6) is less hardware efficient than

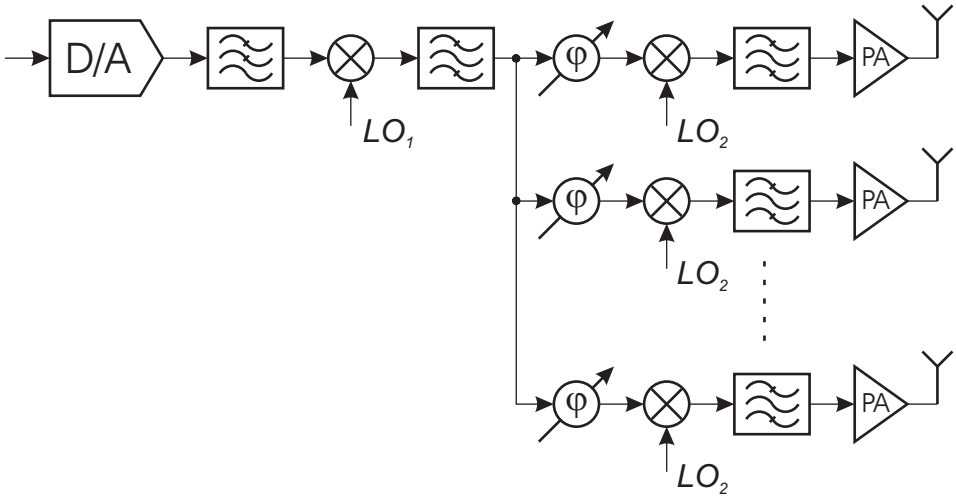


Figure 2.6: A double up conversion beamforming transmitter with phase shifting implemented in the intermediate frequency path.

the RF one as the second up conversion mixers, the RF image reject filters and the PAs have to be multiplied several times. On the other hand the intermediate frequency is typically several times lower than the radio one which facilitates the design of the phase shifters.

2.4 A beamforming offset LO direct conversion architecture

Various transmitter architectures can satisfy the 802.11a WLAN requirements [8–13]. From an integration point of view especially attractive are the direct conversion and the double quadrature up-conversion architecture, because they do not require external filters[2] [8–12]. For this work the direct conversion architecture was chosen because of its inherent simplicity and due to the fact that there is no subcarrier placed at DC in an 802.11a WLAN system. This is an especially convenient feature in the standard, because during up-conversion various offsets in the LO and baseband paths lead to a LO leakage that interferes with a DC subcarrier. The direct conversion architecture directly up-converts the baseband signal to RF (Fig. 2.7). In fact

[2]The image created is removed through signal cancelation.

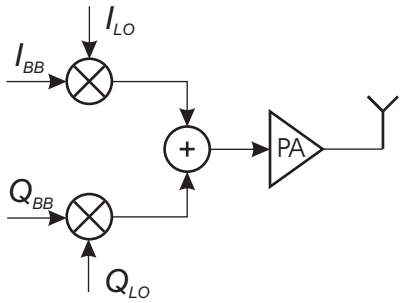


Figure 2.7: A direct conversion architecture.

the architecture is so simple that it can easily be multiplied several times. However, the local oscillator and the PA operate at the same frequency and this leads to interference between them known as injection pulling. Since it is difficult to ensure adequate shielding, the output of the PA still corrupts the oscillator spectrum. To solve this problem the LO can be offset in frequency by adding or subtracting the output frequency of another oscillator [14]. This architecture is shown in Fig. 2.8. The selectivity of the band

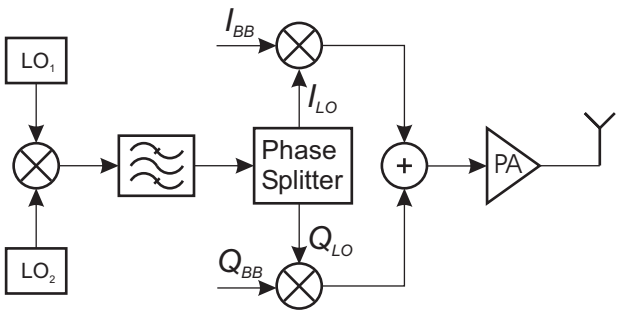


Figure 2.8: A direct conversion architecture with a frequency offset LO.

pass filter directly affects the quality of the transmitted signal, which makes it difficult to implement. An elegant approach to the problem is presented in [15] and shown in Fig. 2.9. The local oscillator signal is divided by two and the resulting quadrature output is mixed with the initial signal itself by a pair of offset mixers, leading to the generation of a carrier that is 1.5 times the LO frequency. The image signal created is f_{LO} far away from the carrier and it is easily filtered out by the frequency band of the mixers. At the output of the divider the frequency is one third of the carrier one, which makes it convenient to change the phase of the LO signal at that location, reducing the sensitivity to the parasitics. A beamforming architecture that incorporates the structure already described is shown in Fig. 2.10. It was

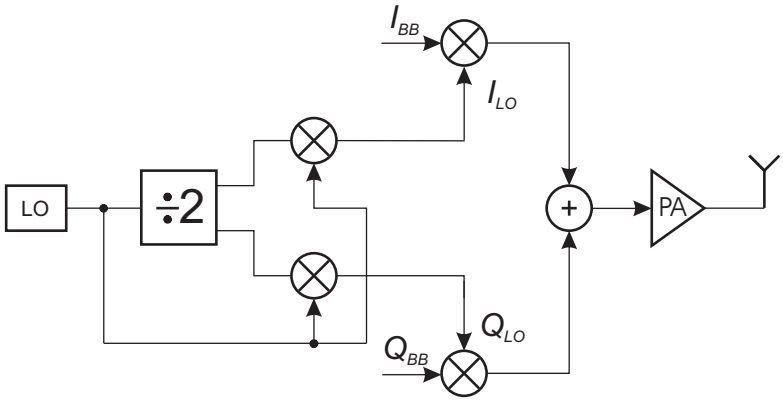


Figure 2.9: A direct conversion architecture with an offset LO.

chosen for the subsequent implementation.

2.4.1 System Level Simulations

The transmitter has to transmit 40 mW (16 dBm) output power for the lowest power class. For the practical case of four antennas each of the four channels has to transmit 10 dBm. The specified EVM by the standard (Table A.2) for the highest data rate of 54 Mbit/s is -25 dB. The EVM for a direct conversion OFDM transmitter depends on the nonlinearity, the noise, the I&Q mismatch and the phase noise. Obviously, there is an unlimited number of combinations between these parameters that will satisfy the EVM specification. One possible system partitioning is shown in Fig. 2.11. The Gain/Phase imbalance of the I&Q upconverter is 0.17 dB/2° and the phase noise of the LO is -120 dBc at 1 MHz offset. The signal levels, the noise and the linearity are presented by a level diagram shown in Table 2.12. The stage NF is given for a source impedance of 50 Ω, while the cumulative NF is calculated according to the impedances in Fig. 2.11. It has to be pointed out that only a third order nonlinearity is considered. At maximum speed the system is limited by the EVM [10]. The simulated constellation in Fig. 2.13 corresponds to an EVM of -26.6 dB at 10 dBm output power.

2.5 Conclusions

In this chapter the optimum location for implementing beamforming in a superheterodyne transmitter architecture is discussed. The pros and cons of phase shifting in the baseband, LO and signal paths are shown. It was highlighted that phase shifting in the LO path is most suitable for beamforming 802.11a transmitter. From integration point of view a direct conversion ar-

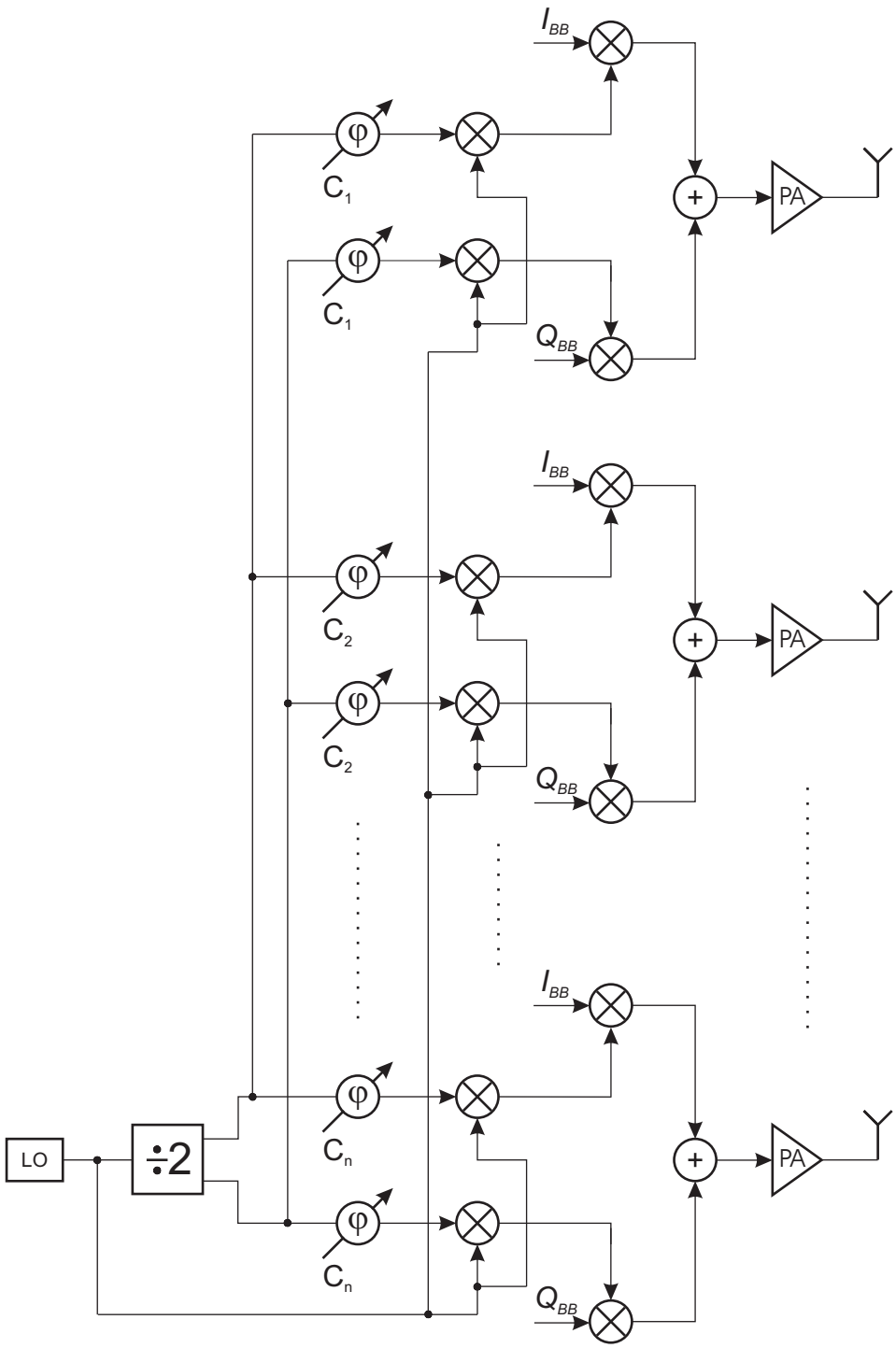


Figure 2.10: A beamforming offset LO direct conversion architecture.

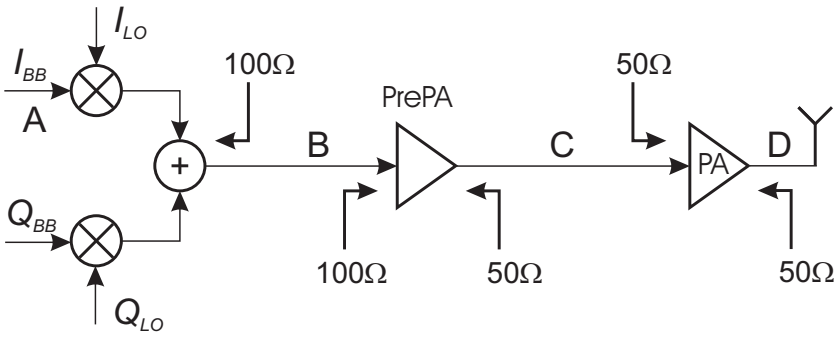


Figure 2.11: A possible system partitioning

	I&Q Modulator	PrePA	PA
	A	B	C	D
Stage gain (dB) Voltage	-10.46	6	15	
Power		3	15	
Cumulative Voltage gain (dB)		-10.46	-4.46	10.54
Voltage (amplitude (V))	0.297	0.089	0.178	1
Stage NF (dB)	10	4	5	
Cumulative NF (dB)	13.86	3.6	5	
Stage OIP_3 (dBm)	15	20	25.6	
Cumulative $IIP_3(V)$	1.67	0.51	1.077	

Figure 2.12: Level diagram corresponding to the cascade of Fig. 2.11

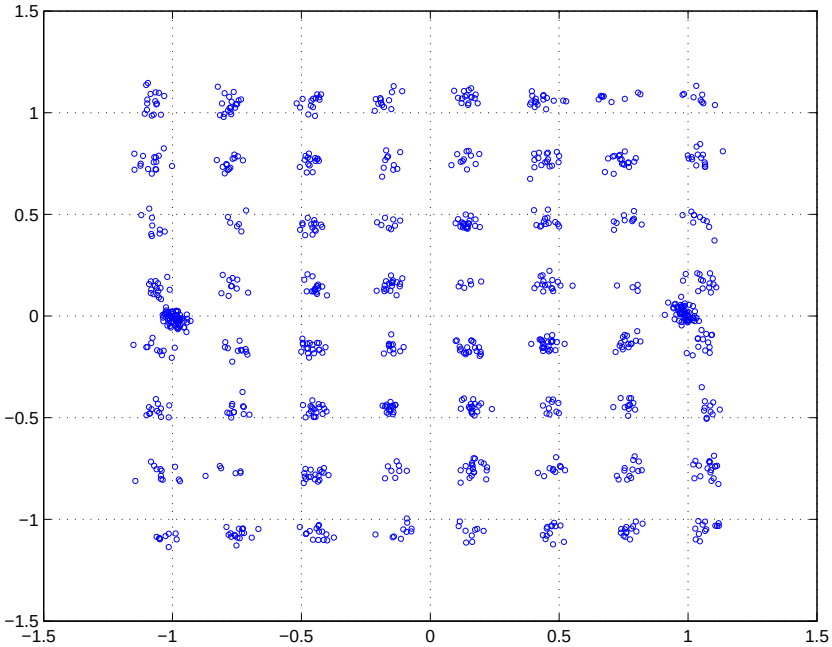


Figure 2.13: A simulated 64-QAM constellation corresponding to the described non idealities

chitecture with frequency offset in the LO path and phase shifting at one third of the of the carrier frequency was proposed for the subsequent implementation.

Chapter 3

Methods and Circuit Techniques for Phase Shifting

The phase shifter is an elementary building block of every beamforming transmitter. Ideally the phase shifter provides up to 360° of phase shift with linear control without affecting the amplitude of the signal. Before discussing various phase shifting techniques suitable for integration it is instructive to consider the amplitude and phase response of a simple RC circuit shown in Fig. 3.1. It is well known that the slope of the amplitude is -20dB/dec

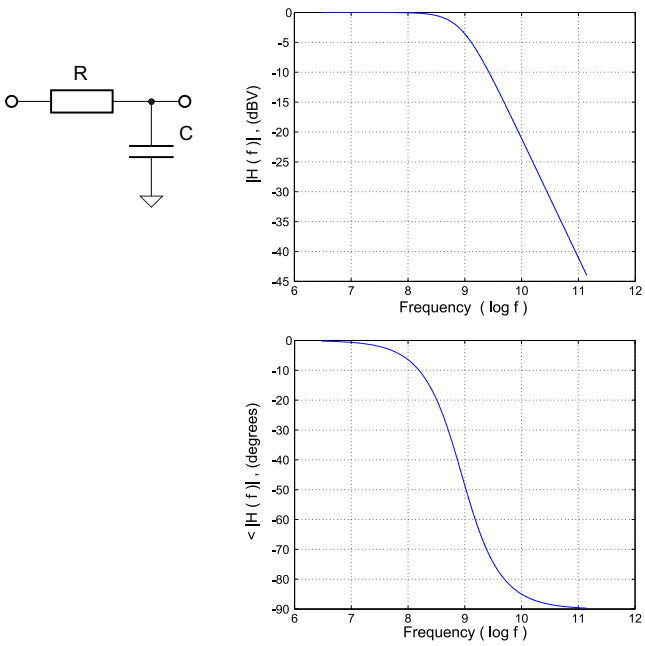


Figure 3.1: Illustration of a simple RC network and the amplitude and phase response of its complex transfer function.

after the pole frequency f_p. On the other hand the phase begins to drop at approximately $0.1f_p$, experiences a change of $-45°$ at f_p and approaches a change of $-90°$ at approximately $10f_p$. It is important to note that the phase is much more significantly affected by the location of the pole than the amplitude. Since the values of the resistors and capacitors on chip are subject to matching and process spread the phase is much harder to control. The most sensitive operating region is the vicinity of the pole itself. In general, every network that has a defined phase response can be considered as phase shifter at a single frequency.

There are two basic approaches towards implementing a programmable phase shift. The first one is to generate all phase states required and to multiplex the ones that are currently needed [2, 16]. This solution is shown in Fig. 3.2. In order to preserve the phase shifting accuracy the multiplexers

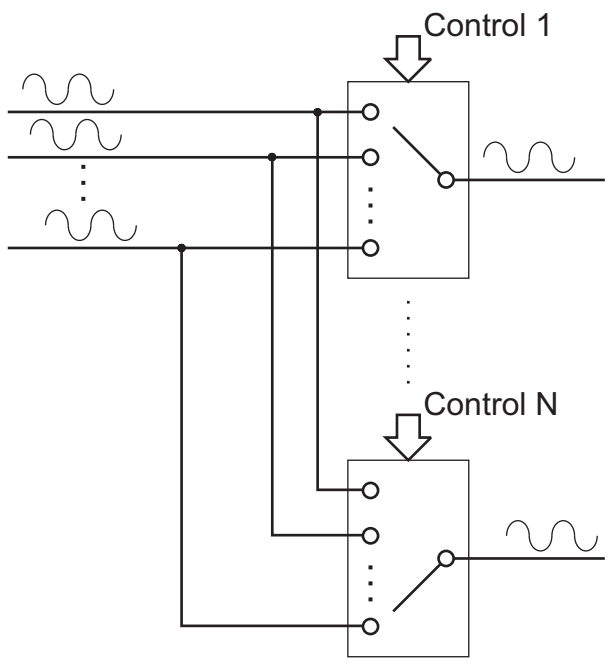


Figure 3.2: Multiplexing the signals with the required phases from a phase sequence.

have to be matched and the signal delays in the interconnects have to be equalized. This significantly complicates the layout especially if several output signals are needed with many phase states. The second method (Fig. 3.3) is to change the phase of a signal directly by using phase shifters, providing lower complexity in most cases. The phase shifters do not need to be with the same topology, however, in practice often they are. The layout of the interconnects is less complex than in the previous case.

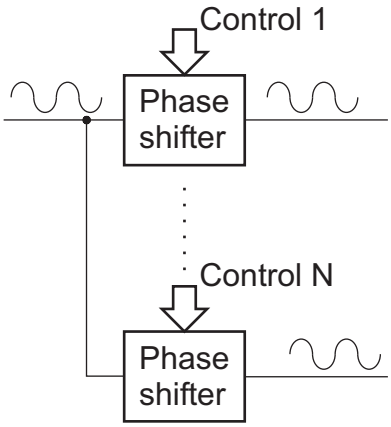


Figure 3.3: Phase shifting from a single source.

3.1 Generating a sequence of phases

3.1.1 DLL based phase shifter

Generating several consecutive phases can be done in a number of ways. Perhaps the most straightforward one is to utilize a Delay Locked Loop (DLL) [17]. The basic structure is shown in Fig. 3.4. When the loop is

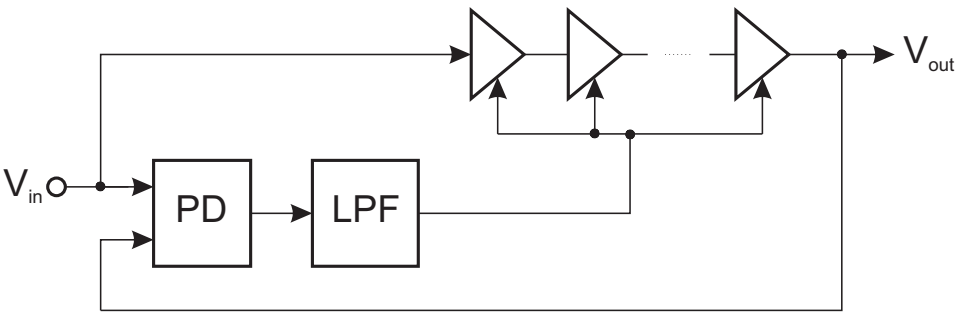


Figure 3.4: Phase sequence generation by means of Delay Locked Loop.

in lock, the Phase Detector (PD) maintains a delay of nT_{in} between V_{in} and V_{out}, where n is an integer and T_{in} is the period of the input voltage. Therefore, the output signals of k consecutive delay stages exhibit a phase difference of nT/k, which is independent of device parameters. The delay accuracy is limited in practice by the matching of the delay elements.

Since the loop can lock with delay nT_{in} some means must be provided to obtain the desired n. Typically some combinatory logic is needed, which may be difficult to run at high frequencies where beamforming becomes interesting. Also the loop gain of the DLL is not infinity meaning that the

signals at the input of the phase detector are not going to be perfectly in phase in this way deteriorating the phase accuracy.

3.1.2 Ring oscillator based phase shifter

Another way to generate the necessary phases is by means of a ring oscillator shown in Fig. 3.5 [17]. Here a cascade of M gain stages with a total phase

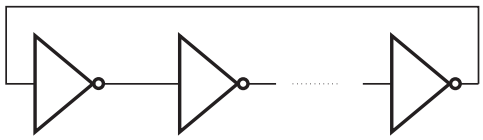


Figure 3.5: Phase sequence generation by means of ring oscillator.

shift of 180° is placed in a feedback loop. The loop oscillates with a period equal to $2MT_d$, where T_d is the delay of each stage. From another point of view the oscillation can be seen as occurring at the frequency for which the total phase shift is zero and the loop gain is unity. The phase sequence generated is with a resolution of $360°/M$. If differential stages are used, the resolution is doubled. In practice the accuracy is limited by the matching between the gain stages. It is important to note that there is a trade off between the frequency of oscillation and the number of phase states. In order to make it run faster the delay T_d has to be reduced by introducing negative delay skewed paths between the stages [18]. However, this in fact creates several coupled loops inside one another and as a result such a system can have several modes of oscillation. Special care has to be taken to guarantee the operation in the desired one [19]. The ring oscillators are also well known for their bad noise performance compared to LC oscillators [20]. In order to solve the problem they must be injection locked or embedded in a wide band PLL [21].

3.1.3 Coupled injection locked oscillator based phase shifter

An interesting solution for generating a controlled sequence of phases was proposed in [22]. An array of identical oscillators are mutually synchronized via a coupling network. Each oscillator is bilaterally[1] injection locked to the neighboring array elements(Fig. 3.6). Two external coherent signals with variable relative phase are injected in the end oscillators. They are generated by splitting the signal of an extra common oscillator and delaying one of the channels. The delay created $\Delta\psi$ is uniformly distributed along the array

[1]In general each oscillator in an array can be unilaterally injection locked as well.

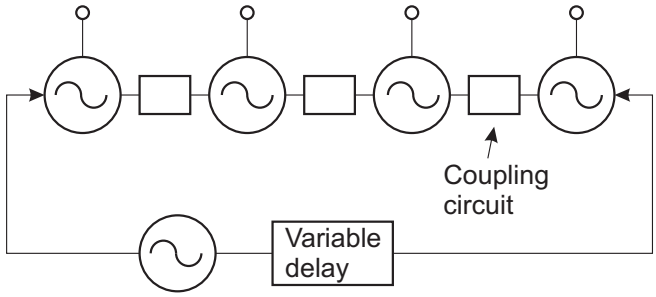


Figure 3.6: Phase sequence generation by means of injection locked oscillators.

producing a constant output phase progression with step of $\Delta\psi/(N+1)$. The maximum phase shift between adjacent oscillators is limited by the stability to $\pm 90°$. Although it is elegant, the technique is actually quite complex. A nonlinear system of simultaneous equations must be solved in order to fully describe the behavior. To complicate the things even further in general a system of N oscillators can have N modes of oscillation, only one of which is the desired one. This requires some extra care or circuitry to ensure that it functions properly [19]. As a further development of the technique it was found that just a slight frequency detuning of the outmost oscillators in an array in opposite directions is sufficient to establish a phase progression at the output without any extra oscillator and delay line [23]. This phase sequence is independent of the number of oscillators. In another work [24] it was shown that the same effect can be obtained by controlling (debalancing) the coupling network of the first and the last oscillators of the array. For completeness it must be mentioned that once a sequence of phases is produced extra phases can be generated by employing an interpolation technique [25].

3.2 Signal phase shift from a single source

3.2.1 A reflective type phase shifter

At microwave frequencies a Reflective Type Phase Shifter (RTPS) is a well known technique for phase shifting [26, 27]. Its basic topology is shown in Fig. 3.7, where the 90° branch line coupler is realized with lumped elements instead of microstrip lines. This is done because at 5 GHz range a quarter wavelength transmission line is too long to be integrated on chip. The phase of the RTPS is controlled by varying the phase angle of the reflection coefficient, which is changed by varying the impedance of the reflective loads Z_r

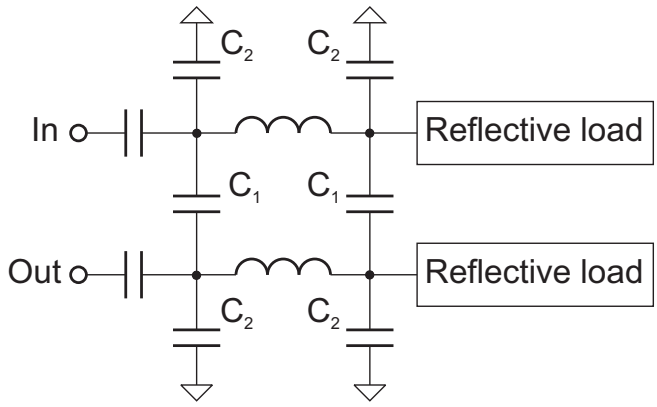


Figure 3.7: A reflective type phase shifter.

using varactors. It is given by

$$\varphi = \arctan\left\{\frac{\Im\left(\frac{Z_r - Z_0}{Z_r + Z_0}\right)}{\Re\left(\frac{Z_r - Z_0}{Z_r + Z_0}\right)}\right\} \tag{3.1}$$

which is a nonlinear function. Z_0 is the characteristic impedance of the transmission line equivalent. The absolute value of the phase shift is:

$$\Delta\varphi = 2\left|\arctan\left(\frac{Z_{max}}{Z_0}\right) - \arctan\left(\frac{Z_{min}}{Z_0}\right)\right| \tag{3.2}$$

where Z_{max} and Z_{min} are the maximum and the minimum values of Z_r. If the reactive load is implemented by a simple on-chip varactor its small tuning range (< 2) limits the maximum phase shift to about 40°. The phase shift range can be increased if an inductor is added in series with the varactor to form a resonance. This is the so called Resonated Load (RL). According to the theory, the maximum phase shift can be extended beyond 360° by connecting two RL with overlapping resonance frequencies in parallel. The resulting large amplitude variation of the reflection coefficient can be mitigated by connecting a simple LC transformation network in series with the load. However, these improved solutions have higher loss and large chip area due to the larger number of inductors and varactors. The loss originating from the series resistance of the inductors can be partially compensated by a negative resistance [27].

In general it is difficult to obtain a linear phase control for the RTPS because firstly Eqn. 3.1 is nonlinear, and secondly the control characteristic of the CMOS varactor is nonlinear as well. The amplitude frequency response versus control signal is also not flat which requires some form of linearisation at system level-for example with look-up table [26]. Getting the values into the table requires some sort of nontrivial self-calibration.

3.2.2 A vector modulator phase shifter

The principle of the phase change by means of a vector modulator originates from the geometry. If two signals represented by vectors have a phase difference Φ between them by changing the magnitude of these signals by means of Variable Gain Amplifiers (VGAs) or Variable Attenuators (VAs) the amplitude and the phase of their vector sum changes. (Fig. 3.8) The amplitude

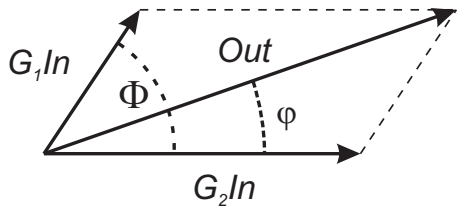


Figure 3.8: A phase shifting vector diagram.

is given by:

$$Out = In\sqrt{G_1^2 + G_2^2 + 2G_1G_2\cos\Phi} \tag{3.3}$$

Where G_1 and G_2 are the control coefficients. The resulting phase shift is:

$$\varphi = \arctan\left\{\frac{G_2\sin\Phi}{G_1 + G_2\cos\Phi}\right\} \tag{3.4}$$

The gain of the VGAs should be controlled linearly and the phase deviation across the used gain range should ideally be equal to zero. Moreover, in order to allow a 360° phase shifting capability the gain of the VGAs has to vary from $-G_{max}$ to $+G_{max}$ (Fig. 3.9). In general the angle Φ can have

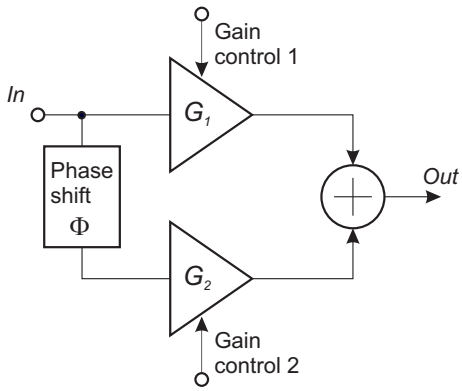


Figure 3.9: A vector modulator.

any value although having the transmitter signals processed in quadrature

makes 90° a natural choice. A VGA that is well suited to be used in a vector modulator is the Gilbert cell shown in Fig. 3.10. The control signal

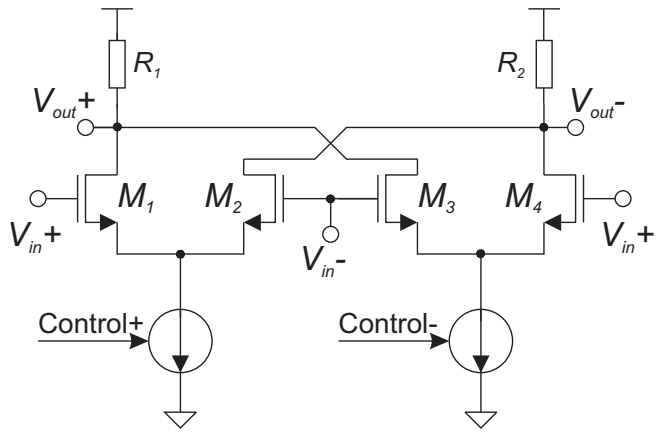


Figure 3.10: A Gilbert variable gain amplifier.

is the linearly regulated tail current. For a LO input signal the transistors can be fully switched, which ensures linear gain control. The phase in this case is not affected when the gain changes. If properly designed the vector modulator can provide power gain, constant amplitude response versus phase shift, linear phase control and area efficiency.

3.2.3 An all pass network based phase shifter

The phase of the signal can be changed by means of all pass network [7, 28]. The poles and zeros of the transmission function of such circuit lie on the real axis of the complex frequency plane. A possible implementation that does not have inductors and it is therefore suitable for integration is shown in Fig. 3.11. It consists of two RC bridge circuits, output buffers and switches. The values of the resistors and the capacitors are chosen in such a way that at the output of the first bridge the signal is with phase shift of $90° + \phi/2$ and at the output of the second one correspondingly with $90° - \phi/2$ at a selected frequency. The amplitude is constant because the bridge has all pass characteristic [7]. The frequency response of the two bridges is shown in Fig. 3.12(a). The phase difference between the two signals is shown in Fig. 3.12(b) and has a flat maximum at the designated frequency indicating a zero element sensitivity at this point. Like all types of passive phase shifters the RC all pass bridge is quite lossy, requiring amplifiers in order to restore the power level. In practice in order to make the parasitics negligible the bridge impedances should be kept low.

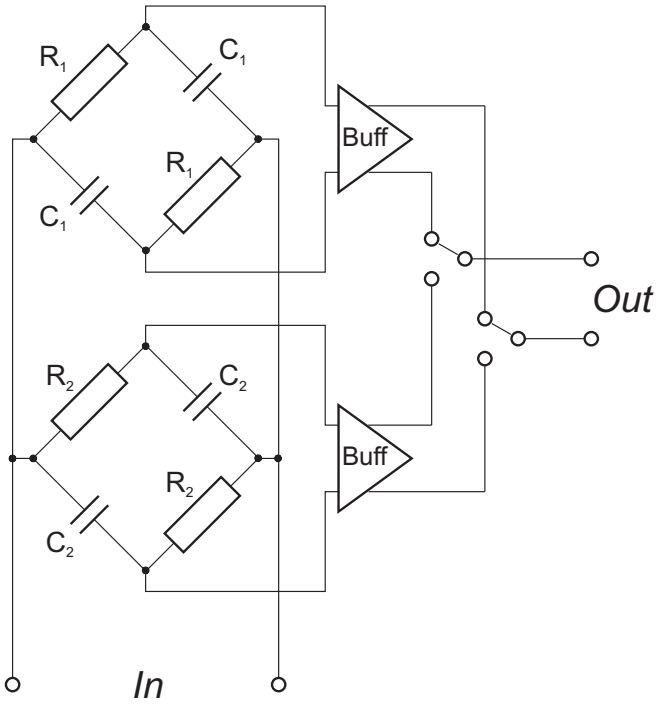
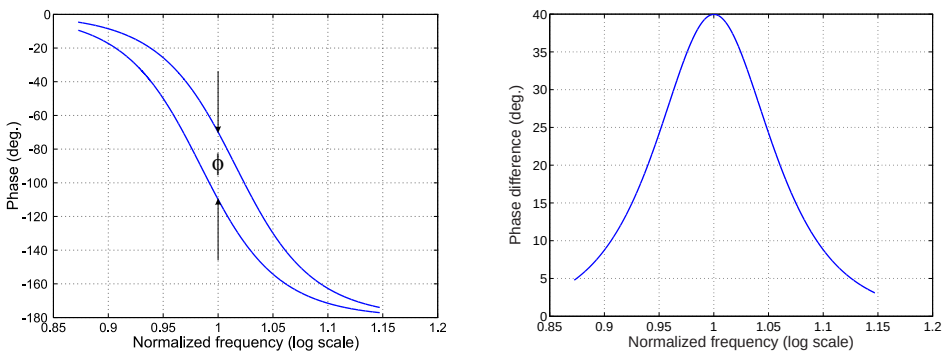


Figure 3.11: An RC all pass bridge based phase shifter.



(a) Phase at the output of each RC bridge.

(b) A differential phase response at the output of an RC all pass bridges.

Figure 3.12: Principle of operation of a double RC all pass bridge phase shifter.

3.2.4 A PLL based phase shifter

The phase of the signal can be changed by directly modulating a Phased Locked Loop (PLL). (Fig. 3.13) In general this can be done anywhere in

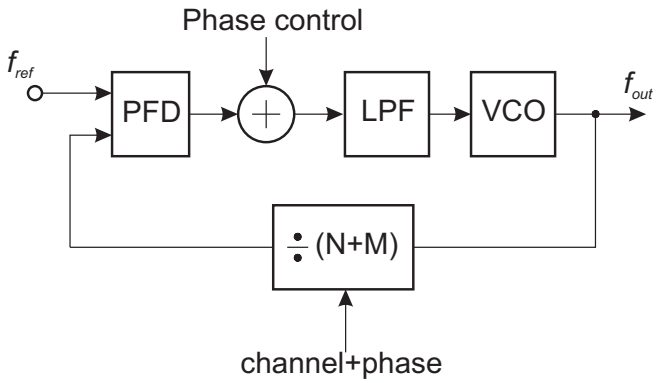


Figure 3.13: A PLL based phase shifter.

the loop, but in practice the most convenient location is between the Phase Frequency Detector (PFD) and the loop filter [29]. The reason is that the output signal of the PFD is usually a current that facilitates the summing operation and the phase shift can be set by a current ratio which is easy to control in an integrated circuit. In order to have a linear control the transfer characteristic of the PFD has to be linear. Another popular way for implementing a constant envelope modulator is to make the divider ratio fractional-leading to concept of the fractional N PLL [30]. Although feasible the PLL based phase shifter is prohibitively complex if several of them are needed.

3.3 Discussion

Various methods and circuits techniques for implementing on ship phase shifting were presented. Their limitations are discussed with respect to important characteristics for beamforming such as phase resolution and accuracy, control linearity and overall complexity. All of them are feasible, however, a vector modulator seems to fit best to the LO phase shifting architecture. Because of its attractive properties like linear phase control, 360° phase shifting range, flat amplitude response versus phase change, area efficiency and power gain it was chosen for the subsequent implementation.

Chapter 4

Phase shifting transmitter IC

This chapter presents the design of an 802.11a WLAN transmitter with adaptive beamforming capability. It is partially based on [31]. An efficient beamforming architecture with a linearly controlled 360° phase shifting range is proposed for linear transmitters. The design of key circuit blocks is discussed. The circuit implemented in 0.25 μm CMOS technology has a -1dB OCP of -7.1 dBm and it consumes 65 mA. It has a phase shifting resolution of 10° with a differential accuracy of 2°.

4.1 Introduction

The Power Amplifier is difficult to integrate with the rest of the transceiver circuitry. The low supply voltage of the digital CMOS processes and the high Peak to Average Ratio (PAR) of the modern modulation technologies make the problem even more pronounced.

Beamforming is a solution to both problems because it allows the design of several lower power PA's and although it does not improve the power efficiency of the PA's *per se*, it increases the power efficiency of the transmission, which means that less power needs to be dissipated at the transmitter for a given power at the receive antenna. A general structure of a beamforming transmitter is shown in Fig. 4.1. The direction at which the transmitted signals from several different antennas in an antenna array combine coherently can be controlled by delaying the signal applied to each antenna or adjusting its phase so that the propagation delays between the transmitted signals are compensated for a particular direction. In the other directions, there is partial or full signal cancelation leading to beam formation. Such a system also has the added advantage of increasing the system capacity because the power is mostly transmitted towards the intended user thus reducing the interference between the communicating devices. If the phase shifting is done electrically, the beam can be steered without mechanical movement.

Recently the integration of beamforming systems has received some at-

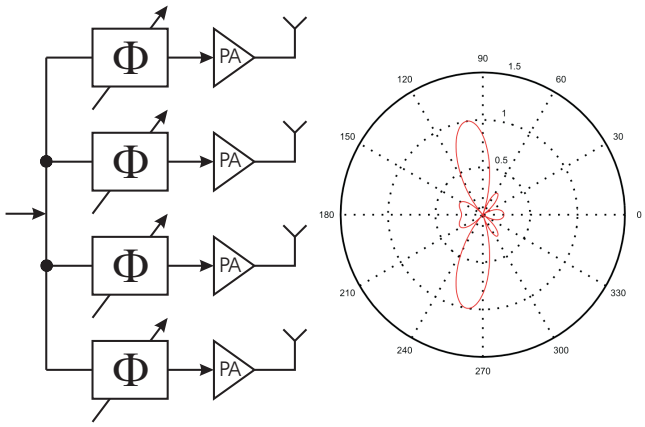


Figure 4.1: A general structure of a beamforming transmitter with 4 isotropic antennas and the corresponding antenna pattern for 30° relative phase shift and half a wave length linear array spacing

tention at the transmitter side [2] as well as at the receiver side [16, 32]. However, the solutions presented either use a large number of inductances per channel [2, 16], which potentially leads to increased die area, or does not provide linear phase control [32], which complicates the beam steering. Phase control can be linearized using external digital calibration [26] that increases the cost of the solution. In this chapter an alternative design is shown, which overcomes the above mentioned limitations.

Typically the dimensions of an antenna are strongly dependent on the wave length of the transmitted signal. High operating frequency results in a small antenna size. On the other hand the separation between the elements of a uniform antenna array is also usually a fraction of the wave length as $\lambda/2$ is the most common choice. Subsequently, in order to have the size of the antenna array sufficiently small so that it can easily be fitted on a typical mobile terminal a 5 GHz IEEE 802.11a Wireless Local Area Network (WLAN) standard was chosen as a target application [3]. According to the specification, two frequency bands are allocated–from 5.15 GHz to 5.35 GHz available worldwide and from 5.725 GHz to 5.825 GHz. In order to make efficient use of the allocated spectrum Orthogonal Frequency Division Multiplexing (OFDM) is specified as modulation scheme for the standard [4]. It subdivides the carrier into 52 individually modulated orthogonal sub-carriers that are transmitted in parallel occupying a bandwidth of 16.6 MHz. The sub-carriers are offset at 0.3125 MHz from each other and depending on the propagation conditions can have different modulations ranging from Binary Phase-Shift Keying (BPSK) to 64-level quadrature amplitude modulation (64-QAM) for the highest data rate of 54 Mbits/s. The specified baseband signal has a theoretical Peak to Average Ratio (PAR) of 17 dB and the

maximum Error Vector Magnitude (EVM) is -25 dB.

The chapter is organized as follows: In section 4.2 the architecture is introduced. In section 4.3 details of the circuit design are described. Experimental results are presented in section 4.4 and the chapter is concluded in section 4.5.

4.2 Beamforming Transmitter architecture

In general, it is possible to implement beamforming at each stage of the transmitter chain-at baseband, at Intermediate Frequency, at Radio Frequency or in the first or second Local Oscillator part (Fig. 4.2). The closer

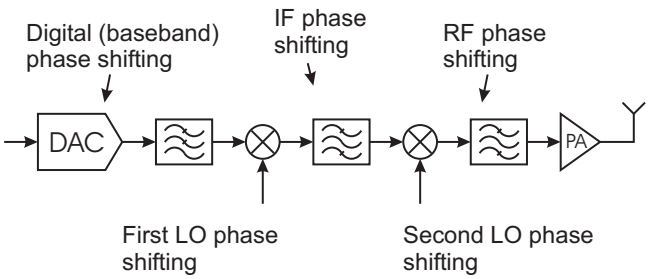


Figure 4.2: A classical superheterodyne architecture with specified possible locations for implementing phase shifting

the phase shifting takes place to the antenna, the shorter are the parallel antenna paths, meaning fewer functional building blocks need to be multiplied. This results in lower power consumption and reduced complexity. On the other hand moving towards the antenna the operating frequency and the power levels become higher, making it increasingly difficult to implement accurate phase control.

The high PAR of 17 dB and maximum EVM specification of -25 dB[1] demand a high linearity in the signal path. In such a case it is particularly suitable to change the phase in the local oscillator path because there the amplitude noise and non-linearity are not an issue. Another important consideration is that 802.11a WLAN system is a Time-Division Duplexing system so that the phase shifter can be shared between the receive and the transmit paths. In addition the fact that the LO signal is amplitude saturated allows the necessary phase change to be generated by multiplexing the outputs of a Delay-Locked Loop or a ring oscillator [2].

Various transmitter architectures can satisfy the 802.11a WLAN requirements [8–13]. From an integration point of view especially attractive are the

[1] In practice the required EVM is achievable with some signal clipping.

direct conversion and the double quadrature up-conversion architecture because they do not require external filters [8–12]. For this work the direct conversion architecture was chosen because of its inherent simplicity and since there is no subcarrier placed at DC in an 802.11a WLAN system. This is an especially convenient feature in the standard, because during up-conversion various offsets in the LO and baseband paths lead to LO leakage that interferes with a DC subcarrier.

In order to avoid the frequency pulling of the Voltage Controlled Oscillator (VCO), a frequency offset was introduced in the local oscillator path by an extra mixer for each of the I and Q parts [15]. This solution is shown in Fig. 4.3. The VCO signal is divided by two and the result is mixed with the initial signal itself, leading to the generation of a carrier that is at 1.5 times the VCO frequency. This solution facilitates the design of the oscillator because of the reduced operation frequency. At the output of the divider the

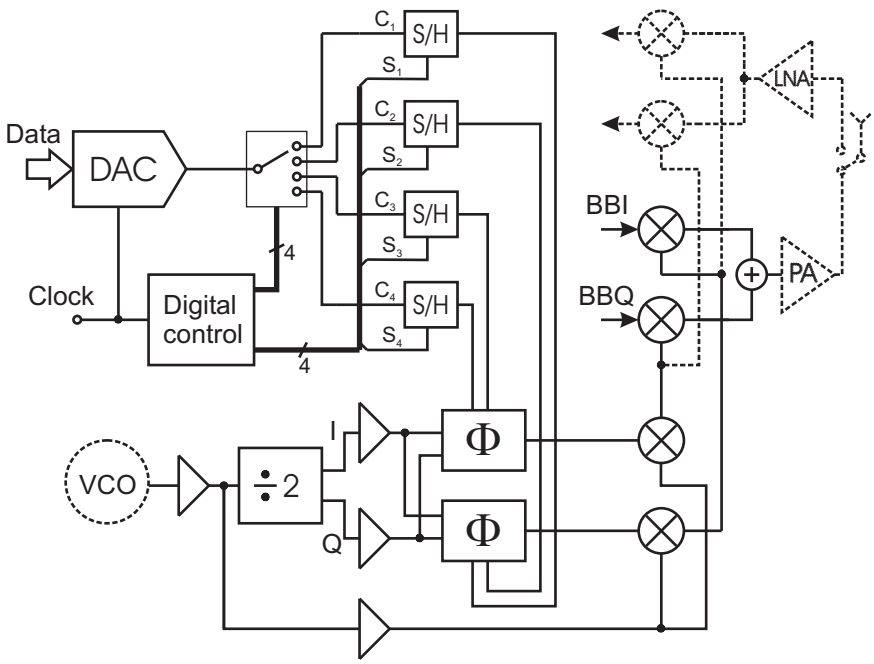


Figure 4.3: Architecture of one signal path of four channel beamforming transmitter. The blocks with dashed lines are not included in this particular chip prototype

frequency is one third of the carrier, which makes it convenient to change the phase of the LO signal at that location, reducing the sensitivity to the parasitics.

4.3 Circuit design

A phase-shifter circuit is needed for implementing the beamforming function. The ideal solution should provide a linear control of the phase over the entire 360° range without affecting the amplitude of the signal. There are several major methods to change the phase of a signal-a reflective type phase shifter utilizing a transmission line with controlled termination [26], high pass low pass cascaded filter elements, an all pass bridge [7] and a vector modulator [33]. In general, it is difficult to provide a proper reactive termination control for a transmission line so that there is linear control of the phase of the reflection coefficient. Moreover, the line equivalent itself implemented on the chip is lossy and the implementation of lumped element equivalent of a 90° hybrid is area consuming. A switchable set of low pass high pass filters is also area consuming and a constant amplitude response is difficult to ensure. An RC all pass bridge [7] can provide very process-insensitive phase shift, but the insertion loss is about 10 dB or more and generally the phase control is nonlinear.

A quadrature vector modulator is chosen for the implementation because it can provide linear control of the phase. Apart from the phase shifting properties it is also area efficient and provides additional gain needed in the LO path. For proper functionality accurately balanced I and Q signals are needed. They are available for free at the outputs of the frequency divider with proper topology (Fig. 4.6), which is primarily used for LO generation.

Beamforming requires several parallel transmitter paths with independent phase control. Since the structure will be multiplied several times it is important that its implementation is efficient both in terms of area and power. The Sample and Hold (S/H) structures allow just one Digital to Analog Converter (DAC), which provide all control signals for the phase shifting in all four parallel signal paths (Fig. 4.1). A tuning resolution of 10° was targeted and a DAC resolution of 6-bits was found to be adequate. The image rejection depends on the matching between the I and Q paths. It is not affected by the DAC inaccuracies since they appear as a common-mode effect. The accuracy of S/H circuits is more important since their errors lead both to reduced image rejection and inaccurate phase control. The precision can be easily achieved because the application is quasi static and the refreshment rate of the sample and hold circuits is just 1.25 MHz. The divider could also be shared between all four parallel paths thus reducing the overall power consumption (Fig. 4.1). The divider output is buffered in order to provide the necessary voltage swing for the phase shifters and to improve the isolation. The buffers themselves employ a differential pair topology. In order to bring the external VCO signal on chip, another differential pair buffer was used with an LC tank at the tail. This provides a better common mode rejection for the differential VCO signal. This is important in order to ensure a 50 per cent duty cycle needed for accurate quadrature generation [section4.3.4].

The inputs of this measurement buffer have a 50 Ω resistive match on chip. In a fully integrated transmitter it is very likely that the VCO will have a differential topology thus providing the accurately balanced signal directly.

4.3.1 Phase shifter

Two differential sample and hold circuits, the vector modulator and the frequency offset mixer can be implemented as shown in Fig. 4.4. The stacked

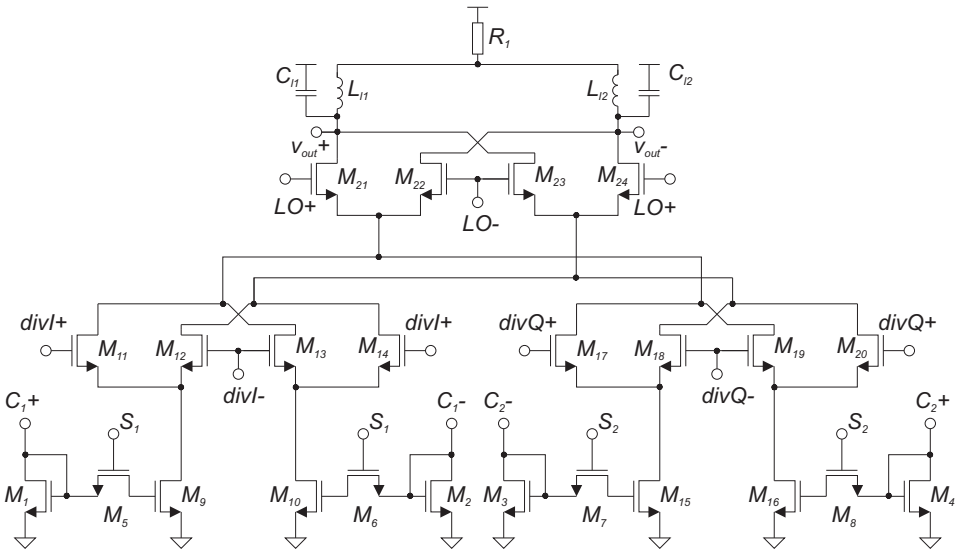


Figure 4.4: Two differential sample and hold circuits, a phase shifter (vector modulator) and a frequency offset mixer

implementation is power efficient because the supply current is reused [10,34]. The vector modulator utilizes two Variable Gain Amplifiers (VGA) with current control implemented like in Gilbert cells. The first one is formed by the transistors $M_9 - M_{14}$ and the second one correspondingly by the transistors $M_{15} - M_{20}$. The control of the Gilbert cell is linear assuming that it is switched fully and that the input transconductors are linear. (In this design the transconductors are actually replaced by current memories that have current input and current output so there is no transconductance in the same sense as usually and therefore they can not contribute to the nonlinearity assuming perfect current coping.) The stacked frequency offset mixer consists the transistors $M_{21} - M_{24}$. The single ended S/H is a current memory cell comprising of M_1, M_5 and M_9 with input signal coming from a PMOS multiplexer. In order to ensure copying accuracy, the current mirror transistors are quite large (W/L=220/3). The error due to the finite output impedance causes phase shifting inaccuracy, but does not affect the image

rejection because the I&Q signals are rotated by the same angle and their amplitudes change by the same amount preserving the relative accuracy. The sampling transistor is a minimum size device, providing very low values for the switching errors. The image signal created by the upper stacked mixers is 3.5 GHz away from the carrier and it is attenuated significantly by the resonator loads. The resistor $R_1 = 37.5\Omega$ is used to prevent potential common mode oscillations [35]. The DC voltage drop of 300 mV across R_1 also biases the switches of the I&Q up-converter.

4.3.2 Digital to Analog converter

The 6-bit digital to analog converter employs a current steering architecture, which is simple to realize and provides a convenient interface for the sample and hold structure. Binary scaled current sources are switched to the differential output depending on the applied digital code. The required 6 bit accuracy can be achieved without calibration. The differential analog multiplexer at the output of the DAC is realized by PMOS transistor switches.

4.3.3 Quadrature up-converter

The baseband signal is directly up-converted to RF by an I&Q modulator based on a Gilbert-type mixer shown in Fig. 4.5. In order to achieve the

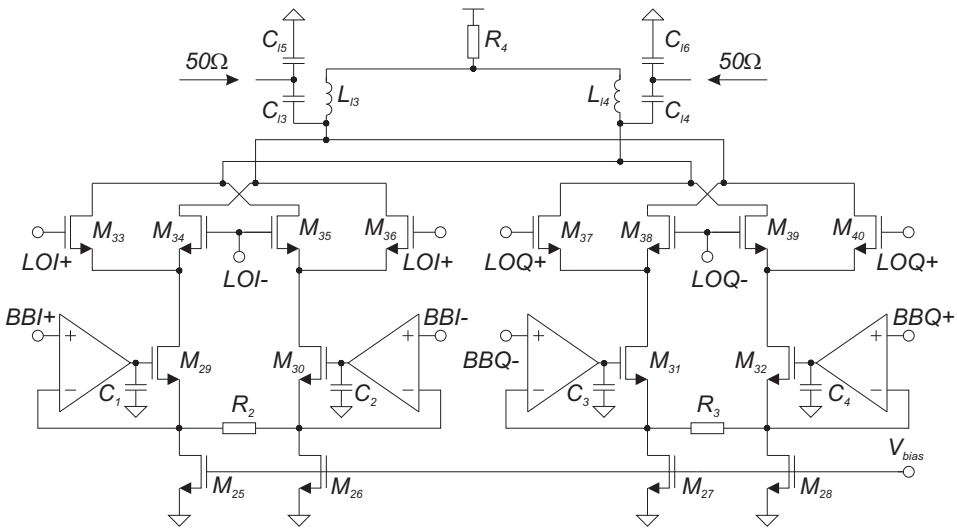


Figure 4.5: Quadrature up-converter

necessary linearity the input voltage is converted into current across a degeneration resistor by a negative feedback that employs an operational amplifier

with a gain of 60 dB. The amplifier itself has a folded cascode topology. The bandwidth of the loop is designed to be 20 MHz, which is adequate to pass the baseband signal of 802.11a system. The capacitors $C_1 - C_4$ are added to the circuit to stabilize the feedback. The outputs of the I and Q mixers are summed by a pair of inductor loads that are impedance matched to 50 Ω. The 3.5-turn inductors used in the design have a quality factor of about 8.5 at 5.25 GHz. The operational amplifiers can be shared between all four parallel paths (Fig. 4.1) providing further reduction of complexity and power consumption on a system level.

4.3.4 Frequency Divider

A frequency divider is used to generate accurate quadrature signals needed for the vector modulator from a 3.5 GHz external VCO. A divide by two circuit can be implemented by using two latches in a feedback configuration. The latches themselves employ a Current Mode Logic (CML) topology (Fig. 4.6). In order to have accurate quadrature generation the VCO signal

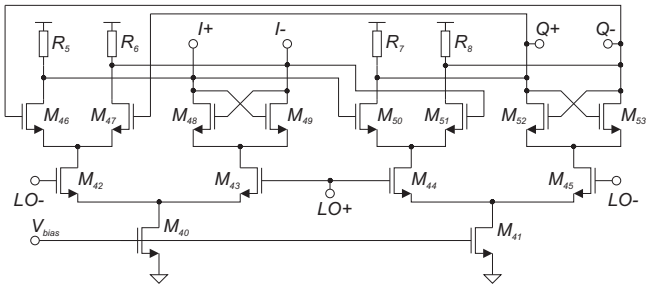


Figure 4.6: Frequency Divider

must have a 50 percent duty cycle. Any deviation from this value or any mismatch between the latches will result in EVM error as well as in inaccuracy of the phase control. It is important to note that in order to achieve the required EVM for the maximum speed assuming that there is no gain imbalance a phase accuracy of about ±1.5° is necessary while for the phase control ±5° is sufficient.

4.4 Experimental results

The transmitter was designed in 0.25 μm CMOS technology with high resistivity substrate, 2 μm thick top Metal5 and MIM capacitor option. No third well was available. Differential inductors were not used because the corresponding models were not available although their presence would result in considerable area saving. In order to facilitate the measurements

the chip was bonded directly on gold plated Printed Circuit Board (PCB). The die microphotograph is shown in Fig. 4.7. The transmitter occupies

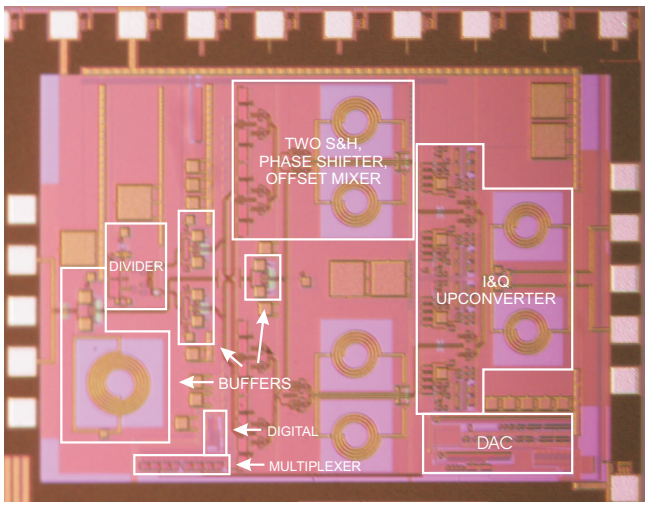


Figure 4.7: A microphotograph of the die

2 mm^2 excluding the bond pads. The silicon area is split between the major building blocks as follows: The phase shifters and the offset mixers occupy 0.23 mm^2, the I&Q modulator has correspondingly 0.35 mm^2, the D/A converter-0.07 mm^2 and the divider-0.034 mm^2. The chip consumes 65 mA at 2.5 V power supply without the input buffer, which is only for measurement purposes. The differential LO signal is provided on chip via a balun and a differential RF probe. The output of the transmitter is taken out in the same way. In order to measure the phase shift of the LO, a balanced DC voltage of 283 mV is applied to both I&Q baseband inputs (Fig. 4.8). In this way the LO signal is made available at the output. The signal generator providing the 3.5 GHz LO signal is phase locked by a network analyzer that is phase locked to a point frequency of 5.25 GHz corresponding to the carrier. The first port of the analyzer is terminated with 50 Ω, while the second one is connected to the output of the chip via a balun. The digitally controlled phase change of the carrier is measured as change of the phase of S_{21}.

The phase shifter has a 360° range. For simplicity the data presented is just for one quadrant. The absolute values of the control currents of the phase shifters in the other quadrants are the same, only the sign is changed by the fully differential current steering D/A converter. The phase change versus the phase control is shown in Fig. 4.9. The accuracy of the measurement is estimated to be better than 0.6°. The measured phase shift error of the carrier for every step of 10° as a function of the phase control is shown in Fig. 4.10. It is well below the limit of ±5° [36]. The measured

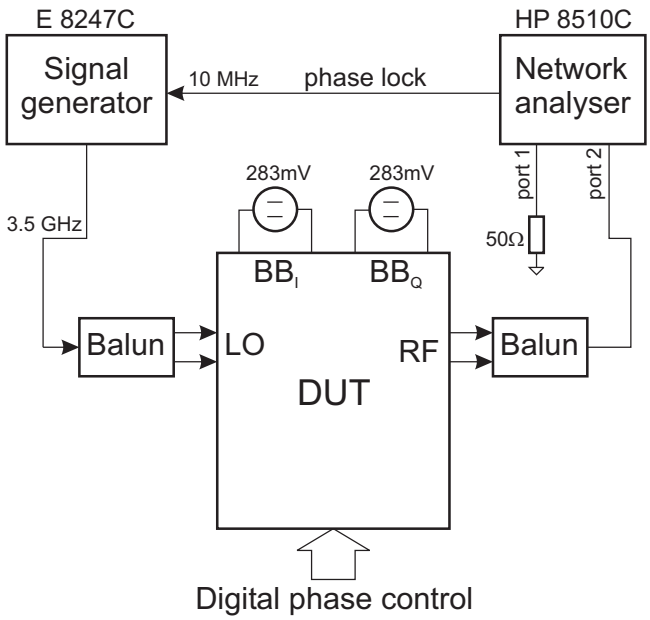


Figure 4.8: A test setup for measuring the carrier phase change

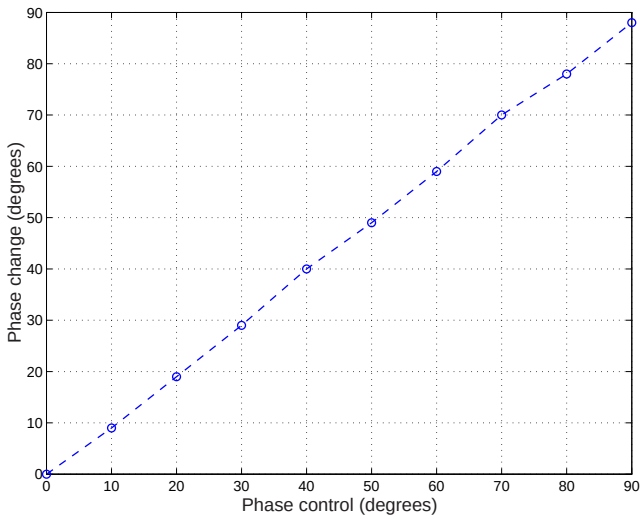


Figure 4.9: Measured phase change versus phase control for one quadrant of the phase shifter

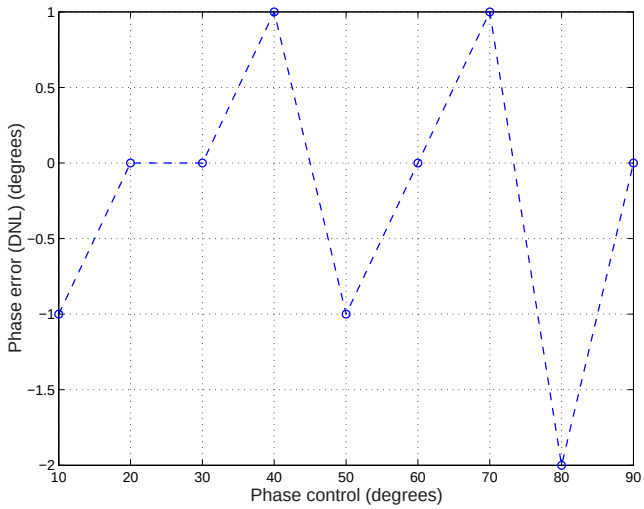


Figure 4.10: Measured phase error versus phase control for one quadrant of the phase shifter

output amplitude variation versus the phase control is shown in Fig. 4.11. It is also within the specification of ±0.5 dB [36]. The measured linearity of the quadrature up-converter is presented in Fig. 4.12. The losses of the balun, the cables and the probe were tuned out. The transmitter reaches its -1dB output compression point of -7.1 dBm when the baseband signal is 1.12 V measured in terms of differential amplitude. The measured output spectrum of the transmitter is shown in Fig. 4.13. The 1 MHz balanced quadrature baseband signals applied to the chip are generated directly with AMIQ I&Q modulation generator. The power out of the chip is -17.1 dBm. The image rejection is 32.1 dB. The LO leakage is 37 dB below the carrier. The third harmonic of the baseband signal is 41.7 dB below the desired signal. The performance of the transmitter is summarized in Table 4.1.

4.5 Conclusion

The design of an 802.11a WLAN transmitter with beamforming capability was presented. Performing the phase shifting in the local oscillator path has several advantages-insensitivity to amplitude noise, no linearity requirement and the possibility to share the phase shifter between the transmit and the receive path. An architecture that further relaxes the design of the phase shifter was proposed, allowing the phase change to take place at one third of the carrier frequency, thus reducing the sensitivity with respect to the parasitics. The phase shifters were implemented as linearly controlled vector modulators in a power efficient way by employing a current reuse technique.

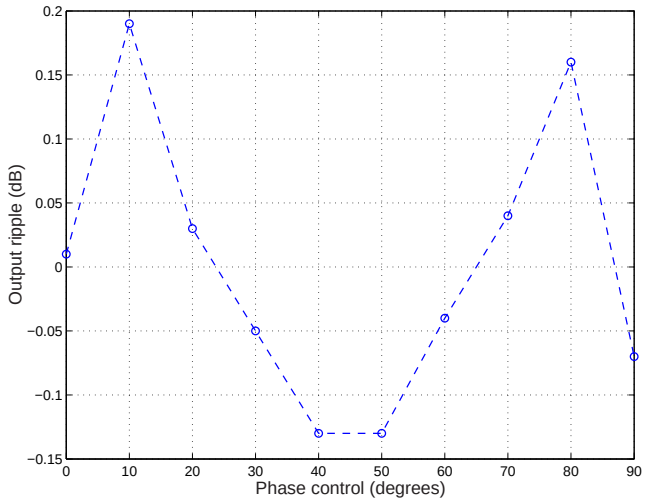


Figure 4.11: Measured output amplitude variation versus phase control for one quadrant of the phase shifter

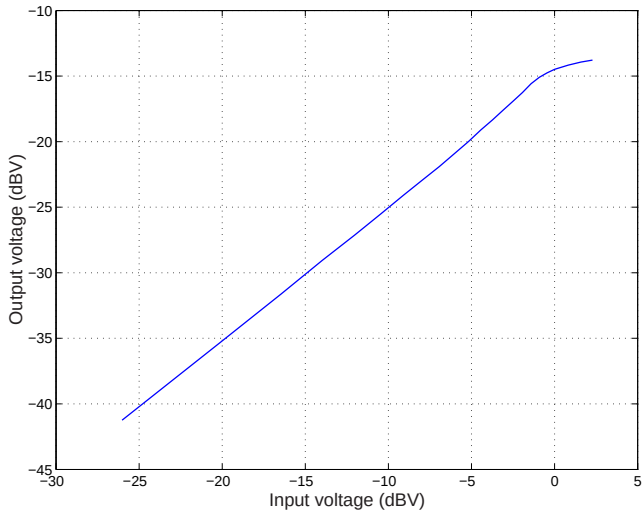


Figure 4.12: Measured AM to AM curve of the I and Q up-converter

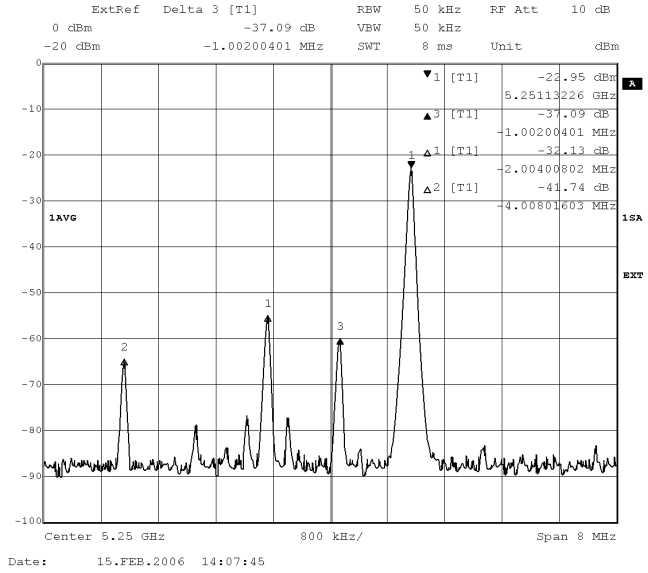


Figure 4.13: The measured output spectrum of the transmitter

Table 4.1: Summary of the transmitter performance

Vdd	2.5	V
P_{sat}	-6.8	dBm
Transmit -3dB Bandwidth	> 200	MHz
P_{out} -1dB	-7.1	dBm
Current Consumption	65	mA
Technology	0.25um 1P5M	CMOS
Die Size	2	mm^2
Divider Silicon Area	0.034	mm^2
D/A Converter Silicon Area	0.07	mm^2
I&Q Modulator Silicon Area	0.35	mm^2
Phase Shifter and Offset Mixer Silicon Area	0.23	mm^2

To further reduce the power consumption the control currents were provided by a single digital to analog converter by means of sample and hold circuits.

Chapter 5

Conclusions and Future work

This work concentrates on developing integrated circuit techniques and architectures for beamforming radio transmitters.

The beamforming as an antenna technology has been known for decades. However, it was too expensive for use in commercial applications, which could not benefit from the advantages that it offers - reduced power consumption and decreased interference between the communicating devices. System integration on a single chip in inexpensive technology like CMOS is one way to reduce the cost. Another way is to look for beamforming architectures with minimum hardware overhead. In order to reduce the cost it is important to integrate the beamforming transmitter on a single chip in low cost technology like CMOS.

An efficient architecture for linear transmitters with accurate phase shifting at one third of the carrier frequency is proposed. The phase shifters are implemented as linearly controlled vector modulators, whose control currents are provided by a single digital to analog converter by means of sample and hold circuits. The chip implemented in 0.25 μm CMOS technology consumes 65 mA from 2.5 V power supply, has a -1dB OCP of -7.1 dBm and phase resolution of 10°.

5.1 Future work

One out of four parallel signal paths was implemented in order to prove the concept of the architecture. What remains to be done is to put all four paths on chip with power amplifiers that are to be designed. The coupling between the parallel high power paths must be taken into account [37].

Appendix A

EVM Specification for the different modulation schemes supported by IEEE 802.11a WLAN Standard

Table A.1: Supported data rate and the corresponding modulation scheme used

Data rate (Mbit/s)	Modulation
6	BPSK
9	BPSK
12	QPSK
18	QPSK
24	16-QAM
36	16-QAM
48	64-QAM
54	64-QAM

Specification for the EVM error

$$Error_{rms} = \frac{\sum_{i=1}^{N_f} \sqrt{\frac{\sum_{j=1}^{L_p} \left[\sum_{k=1}^{52} \{ (I(i,j,k) - I_0(i,j,k))^2 + (Q(i,j,k) - Q_0(i,j,k))^2 \} \right]}{52 L_p \times P_0}}}{N_f} \tag{A.1}$$

Where:
$(I_0(i,j,k) - Q_0(i,j,k))$ is the ideal symbol point
$(I(i,j,k) - Q(i,j,k))$ is the observed signal point
L_p is the length of the packet
N_f is the number of frames for the measurement
P_0 is the average power of the constellation

Table A.2: Relative constellation error versus data rate

Data rate (Mbit/s)	Relative constellation error (dB)
6	-5
9	-8
12	-10
18	-13
24	-16
36	-19
48	-22
54	-25

Common-mode Stability in Low-power LO Drivers

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***Abstract*— A resonator loaded LO buffer is shown to be potentially common mode unstable, when it is connected to drive a double balanced current steering mixer. The stability margin is found to be inversely proportional to the quality factor of the resonator load and, therefore, to the power consumed by the LO buffer. A known solution to the problem is compared with two proposed ones. The approaches differ in terms of current consumption, occupied voltage headroom and area.**

I. Introduction

In wireless communication systems mixers are widely used to perform frequency translation in both reception and transmission. The inputs of a mixer are the signal to be translated and a Local Oscillator (LO) signal, which determines how much in frequency the input signal is translated. In general, the oscillator output cannot be connected directly to the mixer but an intermediate amplifier stage is used to provide isolation and to drive the mixer. Double balanced current steering mixers are a popular topology, because they do not require a very large LO signal and can be designed to provide power gain. In addition, they can be insensitive to amplitude noise in the LO signal and also have good port-to-port isolation (Fig. 1).

Since minimizing power consumption is very important in wireless devices, which are often mobile and, hence, battery operated, a great deal of effort has been invested in finding circuit structures with a low power consumption. One technique for reducing the power consumption of a current steering mixer is to use a resonator load. This is most practical in up-conversion, where the output is at RF and a large output power is highly desirable.

The LO driver of an up-conversion mixer can also consume a significant amount of power. In particular, when the up-conversion is to RF, either from baseband or intermediate frequency (IF), the driver must amplify at radio frequencies. A resonator load can be used in the driver as well to save power (Fig. 2) [1], [2]. However, in the case of current steering mixer, the real part of the LO port common-mode input impedance is in general negative at some high frequencies. When connected in parallel with the resonator load of the driver, it can easily give rise to a common-mode instability, unless some counter measures are taken.

In section II the LO port common-mode impedance of a double balanced current steering mixer and the mechanism causing the potential instability is discussed in more detail. A known circuit technique for stabilization is presented in section III along with two proposed solutions. A comparison is made in section IV and the paper is concluded in section V.

II. Common-mode impedance of a current steering mixer's LO port

The circuit equivalent of the current steering mixer and its driving stage for the common-mode component of the LO signal are shown in Fig. 3. In order to estimate the common-mode load of the driving stage the input impedance Z_{in} at the LO port of the mixer is calculated. For that purpose, the loss of the resonator load is modeled with a parallel resistor. The combined input transistor output impedance is modeled with

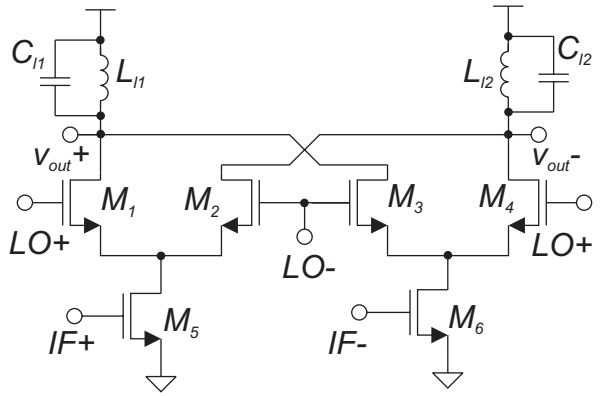

Fig. 1. A CMOS double balanced current steering up-conversion mixer

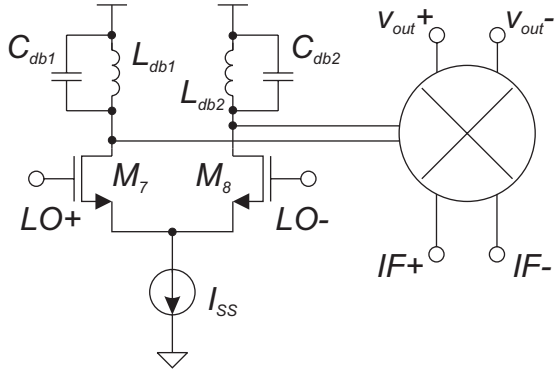

Fig. 2. The double balanced CMOS current steering upconversion mixer from Fig. 1 with its driving circuitry

a resistor and a capacitor, which includes also the parasitics at the sources of $M_1 + M_2 + M_3 + M_4$. Observing the resulting schematic in fig. 4 we note that the transistors M_1, M_2, M_3 and M_4 form a capacitively loaded (C_{out}) source follower with respect to the common-mode signal. It is well known that the input impedance of such a circuit has a negative real part at high frequencies [3]. The impedance Z_1 can easily be derived and its real part is given by:

$$\Re(Z_1) \approx -\frac{g_m}{w^2 C_{gs} C_{out}} \tag{1}$$

Since the drain of the circuit is loaded with a resonator rather than connected to supply, as in a source follower, the impedance Z_2 also affects the real part of the input. Unfortunately, the resulting expression is rather complex and due to the narrow band resonator model, it is not even very accurate over a wider frequency range. For simplicity, the input admittance is simulated with Spice using a more accurate model for the inductor. The simulated real part of Y_{in} is plotted in fig. 5 for different values of R_l. We note that, with the resonator included, the real part of input admittance is still negative over a wide frequency range. Furthermore, the real part of Y_{in} becomes more negative when the loss of the mixer load resonator is reduced. This is very undesirable, because it is in contradiction with the requirement of high mixer gain or low power consumption.

A negative real part in an input admittance is not necessarily a problem. However, when it is connected in parallel with the resonator load of the driver circuit (Fig. 6), it may cancel the loss in the resonator resulting in oscillation much the same way as in LC-oscillators. For proper functioning the condition

$$R_{cm} < \frac{1}{\Re(Y_{in})} \tag{2}$$

must be met. This can be ensured by making the Q-value of the resonator load sufficiently low. However, this will reduce the LO amplitude at the driver output, because the load impedance at resonance frequency is lowered. In order to restore the LO output amplitude more power has to be consumed in the driver circuit. In order to resolve this trade-off the load for the common-mode component of the LO signal has to be decoupled from the load for the differential component. In

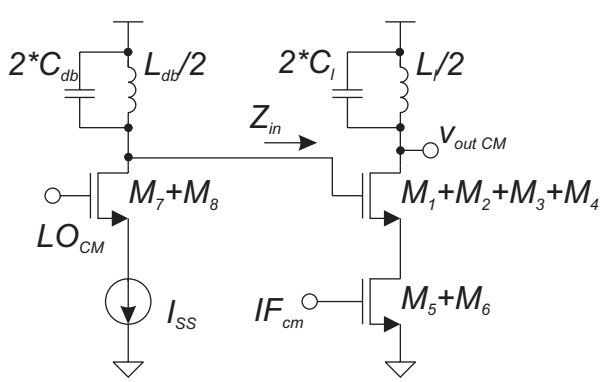

Fig. 3. The structure of Fig. 2 for the common mode signal

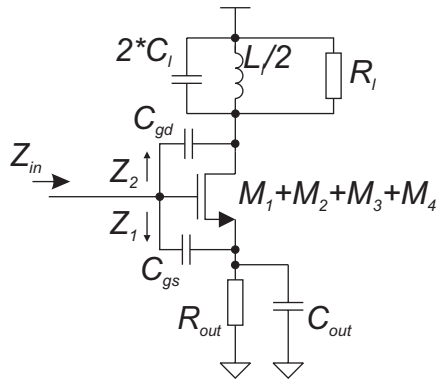

Fig. 4. The model of the mixer for calculating its common mode impedance from the local oscillator port

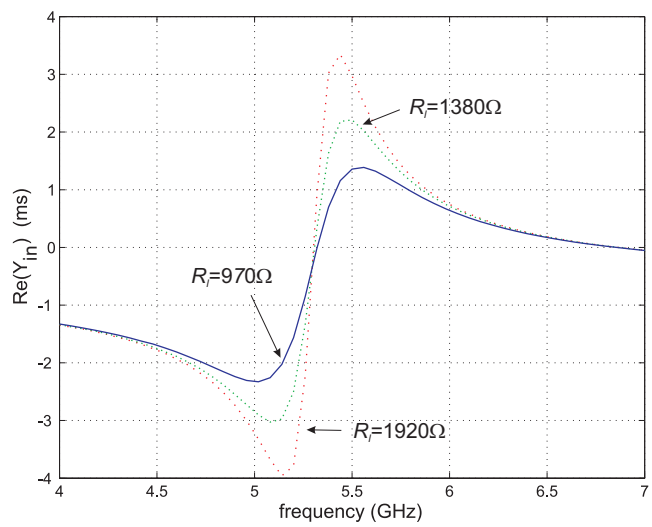

Fig. 5. The real part of Y_{in} versus frequency for different values of R_l;$C_{gd} = 30fF, C_{gs} = 200fF, C_{out} = 600fF, 2C_l = 270fF$,$L_l/2 = 3nH, g_m = 0.005$

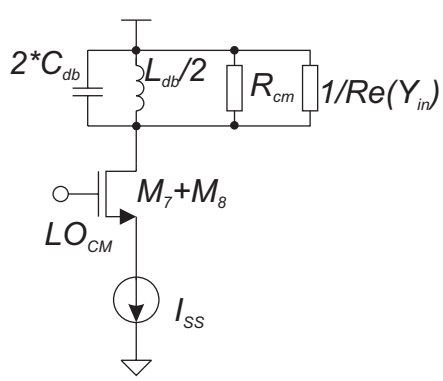

Fig. 6. The buffer with the *oscillating* load

the following section three techniques for achieving this are discussed.

III. Methods for common mode stabilization

A. Common biasing resistor

The first method to decouple the load for the common-mode component from the differential one is well known and is shown in fig. 7 [2]. Point A is a virtual ground and the differential signal does not see the resistor R_b. However, for the common-mode signal the Q of the resonator is reduced. The differential load at the frequency of resonance is:

$$R_{diff} = 2R_{db} \tag{3}$$

and for the common mode is:

$$R_{cm} \approx \frac{R_{db} w^2 L_{db}^2}{2(w^2 L_{db}^2 + 2R_{db}R_b)} \tag{4}$$

The advantage of this solution is that the resistor R_b can be used to bias the switches of the mixer lower than the positive supply. If the LO frequency is high compared to the f_T of the transistors, the bias current in the driver stage needs to be high causing the resistor to occupy substantial voltage headroom. Depending on the particular mixer topology this can be a limitation, when the supply voltage is low.

B. Transformer load

This elegant solution is shown in fig. 8. It exploits the fact that by utilizing a transformer the inductance of the tank is different for the common-mode and for the differential signal. The resistance for differential signal is:

$$R_{diff} = 2R_{db} \tag{5}$$

and for the common mode signal it is:

$$R_{cm} \approx \frac{R_{db}\omega_2^2}{2\omega_1^2} \frac{(L_{db} - M)^2}{(L_{db} + M)^2}, \tag{6}$$

where

$$\omega_1 = \frac{1}{\sqrt{C_{db}(L_{db} + M)}} \tag{7}$$

is the resonance frequency for the differential signal and

$$\omega_2 = \frac{1}{\sqrt{C_{db}(L_{db} - M)}} \tag{8}$$

is the resonance frequency for the common mode signal. Furthermore, the common mode resonance of the driver load is shifted away from the frequency range, where the negative notch of $\Re(Y_{in})$ lies (Fig. 5). This effect of frequency shift can also be achieved by introducing a differential capacitor or inductor in the tank. However in practice the capacitances C_{db} are dominated by the input capacitances of the mixer and introducing a differential capacitor for a given operating frequency would mean a lower L_{db} and subsequently lower R_{db}. Also, a higher resonance frequency for the common mode leads to a higher R_{db} at that frequency, which is something undesired. Introducing a third differential inductor is obviously not a practical solution. The presented solution has all the advantages of using transformer loads and in fact it does not cost any extra hardware compared to a two inductor solution. Nevertheless, the design of transformers is an iterative and time consuming process.

C. Differential negative resistance

The most obvious solution is to connect parallel resistors (R_{c1}, R_{c2}) to the resonators to lower the load's common mode resistance to fulfill the condition of equation 2. Unfortunately, the differential resistance becomes lower as well, which must be compensated by a higher bias current in the driver transconductor. The solution proposed here is to restore the differential resistance by connecting a floating negative resistance to the load (Fig. 9).

The common mode load resistance at resonance is given by:

$$R_{cm} = \frac{R_c R_{db}}{2(R_c + R_{db})} \tag{9}$$

and the differential one:

$$R_{diff} = \frac{-2R_c R_{db} R}{2R_c R_{db} - R(R_c + R_{db})} \tag{10}$$

In order to ensure proper functioning the denominator has to be always negative. The second term of the polynomial expression has to be bigger than the first one taking into account the

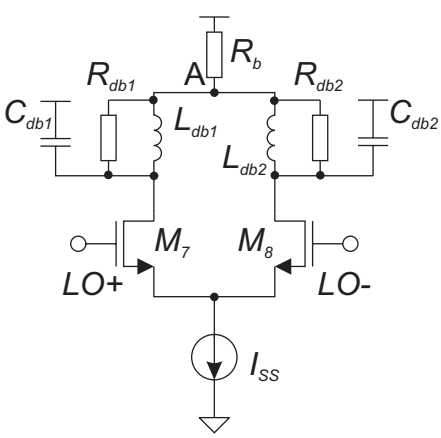

Fig. 7. Decoupling of the differential load from the common mode one by means of biasing resistor R_b

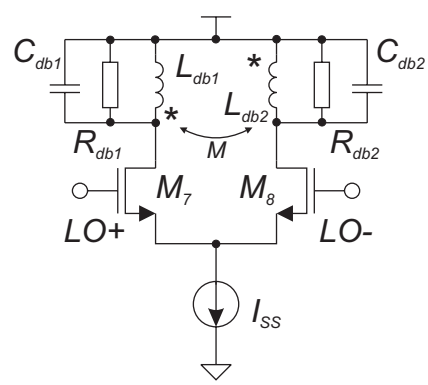

Fig. 8. Decoupling of the differential load from the common mode one by means of electromagnetically coupled inductors

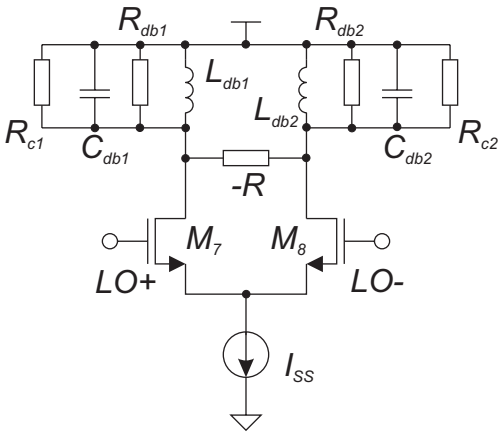

Fig. 9. Decoupling of the differential load from the common mode one by means of differential negative resistance

process spread and the temperature. The differential negative resistance can be implemented by using well known techniques such as a differential cross coupled pair [4].

For completeness it should be noted that combinations between the presented solutions are also possible.

IV. Comparison between the presented methods

In order to facilitate the design choice between the presented solutions a first order comparison between them was made in terms of power consumption. For that purpose three test buffers were designed in 0.25u CMOS process. They were meant for driving an earlier designed 5.2 GHz Wireless LAN (WLAN) I/Q modulator. The comparison is based on the following assumptions:

- A LO frequency equal to the center frequency of the resonator load for the differential signal is fixed ($f = 5.2\ GHz$).
- The inductive part of the load is fixed, meaning that the inductance of the first and the third solution is equal to the sum of the inductance and the mutual inductance of the second one.
- The losses associated with the inductive part are the same.
- The load resistance for the differential signal R_{diff} is equal for all the solutions at the resonance frequency.
- Equal voltage gain of all buffers.

According to the simulations the common biasing resistor and the transformer load solutions consume 4.86 mW, providing common mode resistance of $R_{cmo} = 185\Omega$ (including the output impedances of the transistors) at the corresponding resonance frequencies of 5.2GHz and 12.3GHz. The biasing resistor R_b is found to be 11Ω. The negative differential resistance from Fig. 9 was implemented as a cross coupled differential pair. The total power consumption of the corresponding solution is 9.18mW, but it provides $R_{cmo} = 113\Omega$. If the ratio between the consumed power and the corresponding R_{cmo} provided is calculated it appears that the negative differential resistance solution is slightly less power efficient. The results for R_{cmo} are shown in fig. 10.

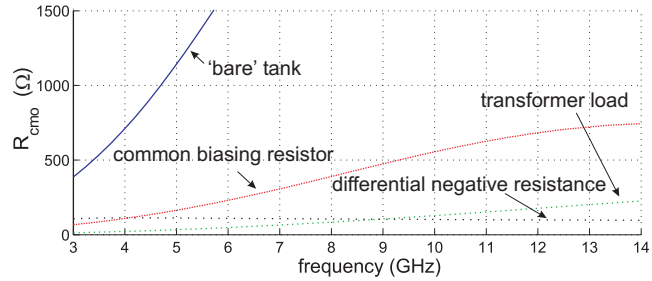

Fig. 10. The real part of the output common mode impedance R_{cmo} versus frequency for the presented solutions

In practice apart from the power consumption other issues play an important role as well. The RF transformers are area efficient and eliminate the problem of the uncertain electromagnetic coupling between two single inductances on a chip. On the other hand their design requires specialized expertise and it is long and labor intensive process. Most design kits available don't provide models for them at all. The common biasing resistor solution provides quite some freedom in adjusting R_{cm}, if there is no voltage headroom limitation. Its use is limited in the advanced CMOS processes, because of the low voltage supply. Also in some applications it is possible to have a large DC current through the resistor R_b making the voltage drop over it excessively high. The differential negative resistor solution has a load that does not have almost any voltage drop over it, but the negative resistor itself consumes power.

V. Conclusion

The power consumption of a mixer LO driver can be reduced substantially by utilizing a resonator load. However, due to the negative real-part in the LO port input impedance of a CMOS double balanced current steering mixer, it has a potentially unstable common-mode level. Three solutions to the problem were presented. A common-mode series resistor is mainly limited by the additional voltage drop, the transformer approach is time-consuming to design and the differential negative resistor circuit consumes additional current, while providing additional stability margin.

Acknowledgment

The authors would like to thank all members of the RISC group for the fruitful discussions, especially Ole Kiel Jensen.

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COUPLING EFFECTS IN AN INTEGRATED BEAM-FORMING TRANSMITTER

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ABSTRACT

In an integrated beam-forming transmitter the proximity and common silicon substrate will inevitably lead to coupling between the different antenna phases. Chain matrix representation of individual stages is used to model the different coupling effects. Analysis shows that with realistic component values the produced beam shape becomes distorted due to the coupling. Predistorting the array control vector is proposed as a means to compensate for the coupling effects. Assuming that the coupling effects are known, it is possible to calculate the predistortion matrix in advance. The actual predistortion then takes only a single matrix multiplication per beam direction.

1. INTRODUCTION

Antenna arrays are used to provide directivity and thus increased gain in wireless communications. The resulting radiation pattern depends of course on the individual antennas but also on their distance and relative phasing. Fixed phase shifting networks may be used in some cases but in mobile communication applications it is often necessary to change the direction and shape of the antenna beam.

The simplest adaptive antenna implementations have a predefined set of beam directions. Such arrangements are used to sectorice cells in mobile telephony [1]. In more sophisticated schemes a base station could, for example, track a mobile user while placing reception nulls to the directions of interferers [1].

Traditionally the phase shifting for adaptive antennas has been done either with pin- diode phase shifters [2] or already in the digital domain. Microwave phase shifters are not easy to integrate with other circuitry and being after power amplification they reduce the efficiency. Implementing the control in DSP is obviously very flexible, but it requires dedicated transmitter hardware for each antenna [3] thus increasing the cost and size considerably.

In order to make adaptive antennas viable for mass consumer applications it is crucial that cheap and physically small implementations are developed. An obvious approach to cost and size reduction is to integrate on a single chip as much of the required circuitry as possible. However, the integration of several high power blocks such as power amplifiers (PA) results in a significant interference between them. In order to be able to preserve the overall performance of the system it is important that the effects of the non-idealities are estimated and subsequently corrected for.

2. SYSTEM OVERVIEW

A general architecture of a transmitter back end utilizing an antenna array for beam-forming is shown in fig.1. The load impedances Z_0 represent the antennas. Ideally the signal paths are independent, and by controlling the relative phases between the antennas, via vector modulators (VM), the antenna beam is steered in the chosen direction. However, if all circuitry is integrated onto a common substrate there will be a number of parasitic coupling paths, which are represented in fig. 1 by mutual impedances $Z_{M,}$ and a ground impedance Zg.

The array gain and the beam width are dependent on the number of antennas. A doubling of array size yields a 3dB increase in the gain. Since one of the aims of integration is size reduction, the most interesting cases are limited to having 2 to 4 antennas. For simplicity of discussion, we will consider an array consisting of four dipole antenna elements placed linearly with λ/2 separation. The ideal system is described by the following matrix equation.

$$\overline{V}_o = \mathbf{G} \times \overline{C} \times \overline{V}_i \qquad (1)$$

Where **G** is the ideal 4×4 transfer matrix and $\overline{C}$ is the beam forming control vector. Eq. 1 can be used to describe the operation of the system in fig. 1. In the idealized case where Z_g, Z_M, Z_L, Z_{out} and Z_{MA} are zero, the transfer matrix **G** is given by

$$\mathbf{G} = K\mathbf{I}, \qquad (2)$$

Where K is the unloaded voltage gain of the power amplifiers in fig. 1 and **I** is a 4×4 unitary matrix.

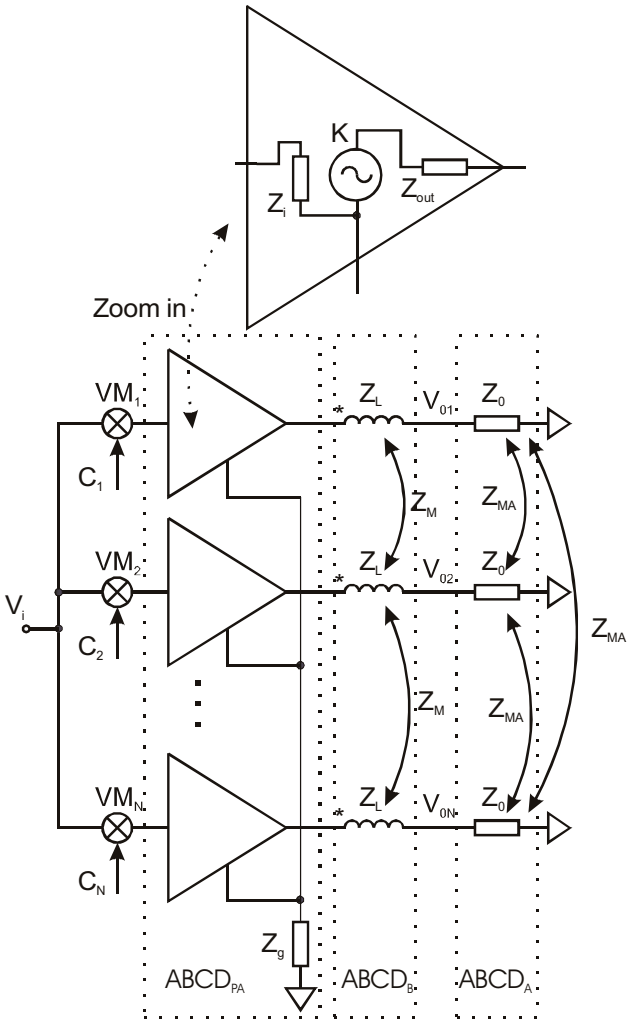

Fig.1 A general structure of a transmitter back end utilizing antenna array. The impedance Z_0 denotes the antennas.

3. COUPLING EFFECTS

For integrating a beam-forming transmitter the coupling between its building blocks has to be considered. It is possible to reduce the on-chip coupling by appropriate layout techniques, but the off-chip connections are more problematic.

The PAs all share the same on-chip ground, which is connected via non-zero impedance Z_g to the external ground. The impedance of the ground connection should be minimized but in practice there is only a limited number of pins available. The return currents of the different outputs all pass through Z_g thus producing an unavoidable coupling between them.

The outputs of the PAs are connected out by bond wires. Because of the small dimensions they are always placed close to each other and at high frequency they will couple reactively. Usually the dominant coupling is between the neighboring bond wires. The antenna array is also going to exhibit coupling between the individual antennas.

In order to estimate the effect of the coupling mechanisms, ABCD matrices are utilized to model the different stages [4]. This approach has the advantage that it can capture port-to-port couplings as well as the effect of source and load impedances. Furthermore, the transfer function of a cascaded system can be obtained by multiplying the corresponding ABCD matrices (Fig.1). The ABCD matrix of an n-port is defined as

$$\begin{bmatrix} \bar{V}_{in} \\ \bar{I}_{in} \end{bmatrix} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix} \begin{bmatrix} \bar{V}_{out} \\ \bar{I}_{out} \end{bmatrix}, \tag{3}$$

Where **A**, **B**, **C** and **D** are all n/2 × n/2-matrices and $\bar{V}_{in}$, $\bar{V}_{out}$, $\bar{I}_{in}$ and $\bar{I}_{out}$ are the input and output voltage and current vectors, respectively.

As an example, the **A**-matrix for the inductive coupling network is found, by opening the output port, to be a unitary matrix **I**. The **B**-matrix is obtained by solving the equation group.

$$\mathbf{B_B} \times \bar{I}_{out} = \bar{V}_{out} - \bar{V}_{in}. \tag{4}$$

$\mathbf{B_B}$ is given by

$$\mathbf{B_B} = -\begin{bmatrix} z_L & z_{M21} & 0 & 0 \\ z_{M12} & z_L & z_{M32} & 0 \\ 0 & z_{M23} & z_L & z_{M43} \\ 0 & 0 & z_{M34} & z_L \end{bmatrix}, \tag{5}$$

Where z_L and z_{Mij} are self- and mutual inductances of the bond wires. As can be seen only the coupling between the neighboring bond wires is taken into account. The input and output currents must in this case be equal but with an opposite sign yielding **D** as -**I** and finally **C** as being zero. Collecting the results, the inductive coupling in the bond wires can be represented by

$$\mathbf{ABCD_B} = \begin{bmatrix} \mathbf{I} & \mathbf{B} \\ 0 & -\mathbf{I} \end{bmatrix}. \tag{6}$$

The ABCD matrix representing the ground coupling between the PAs becomes more complex, but it can be derived in an analogous manner. For realistic antenna geometries it is difficult to find analytical solutions and the corresponding couplings must be either simulated or directly measured. Once ABCD matrices of all blocks are available, the ABCD matrix representing the cascaded system can be found as

$$\mathbf{ABCD_{total}} = \mathbf{ABCD_{PA}} \times \mathbf{ABCD_B} \times \mathbf{ABCD_A}. \tag{7}$$

The output power can be found from eq.3 for $\mathbf{ABCD_{total}}$ by setting $\bar{V}_{out}$ to zero and solving for the output current $\bar{I}_{out}$.

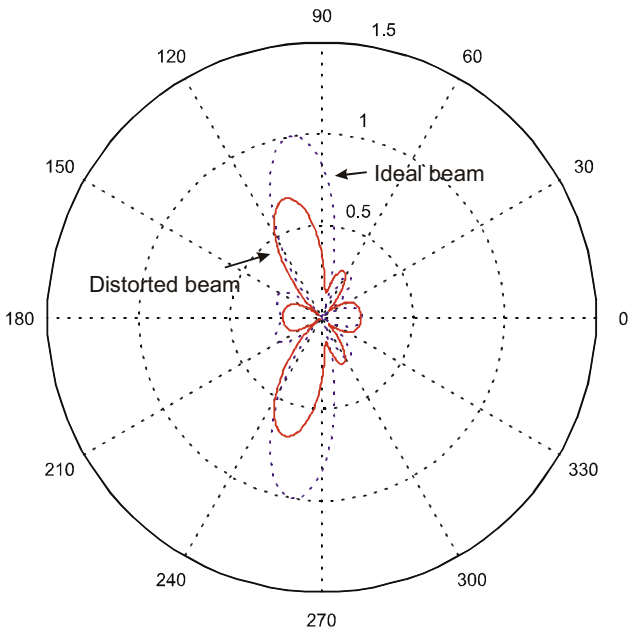

Fig.2 An ideal beam and distorted one due to ground pulling and inductive coupling between the output pins.

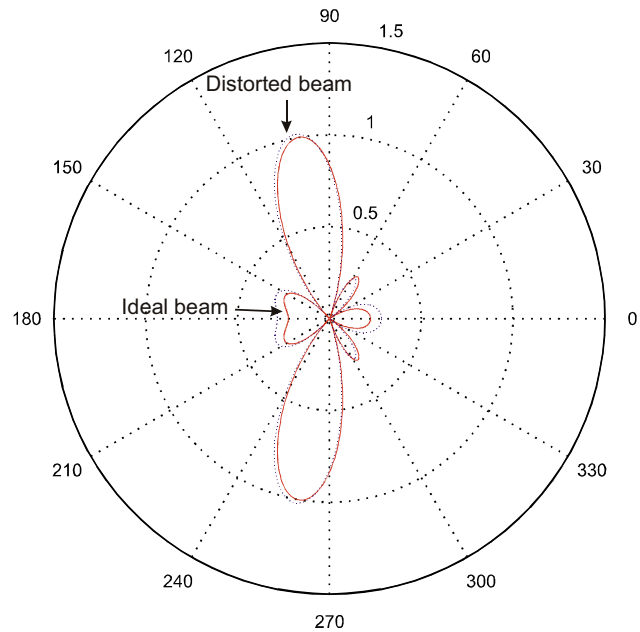

Fig.3 An ideal beam and distorted one due to quantization error in the pre-distortion.

In order to formulate the transfer function as in eq.1, we must write an expression for the antennas' input voltages.

$$\begin{bmatrix} \bar{V}_{in} \\ \bar{I}_{in} \end{bmatrix} = \mathbf{ABCD_{PA}} \times \mathbf{ABCD_{B}} \begin{bmatrix} \bar{V}_{o} \\ \bar{I}_{o} \end{bmatrix}, \qquad (8)$$

Where $\bar{V}_o$ and $\bar{I}_o$ are the antennas' input voltage and current vectors respectively. In order to eliminate $\bar{I}_o$ it must be expressed in terms of $\bar{V}_o$. A relation between them can be found with the aid of the chain matrix of the antennas by setting the output voltage to zero.

$$\begin{bmatrix} \bar{V}_{o} \\ \bar{I}_{o} \end{bmatrix} = \mathbf{ABCD_{A}} \begin{bmatrix} 0 \\ \bar{I}_{out} \end{bmatrix}. \qquad (9)$$

Solving for $\bar{I}_o$ in terms of $\bar{V}_o$ and substituting it in eq.8. leads to the desired form. Assuming that there are no couplings between the antennas, $\bar{I}_o$ equals $\bar{V}_o / Z_o$ and equation 8 becomes:

$$\begin{bmatrix} \bar{V}_{in} \\ \bar{I}_{in} \end{bmatrix} = \underbrace{\begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix}}_{ABCD_{PA+B}} \begin{bmatrix} \bar{V}_{o} \\ \bar{V}_{o} / z_{o} \end{bmatrix}. \qquad (10)$$

Eliminating the currents yields

$$\mathbf{G_d} = \left[\mathbf{A} + \frac{\mathbf{B}}{z_o} \right]^{-1}, \qquad (11)$$

$\mathbf{G_d}$ is the nonideal voltage transfer matrix, which can be used in eq. 1, to find out the voltages at the antenna ports taking the coupling effects in the driving circuitry into account.

Due to the on-chip coupling the signal amplitude and phase at the different antennas is distorted. The calculated effect on the normalized beam [5] is illustrated in fig.2 for Z_g =(2+j*2)Ω, Z_L=j*33Ω, Z_M=j*13Ω, K=40, Z_i =10kΩ, Z_{out} =400Ω, Z_o=50Ω. Clearly, it is necessary to keep the coupling at a very low level to produce an accurate beam.

4. PREDISTORTION

It is clear that the coupling effects may deteriorate the accuracy of the beam significantly. Designing the circuitry so that the couplings are minimized will help but it may be difficult to reduce the effects to a negligible level due to physical limitations. However, since most of the coupling effects are fixed by material properties and the physical geometry of the circuit and its external connections, it is sufficient to estimate or measure the nonideal transfer function $\mathbf{G_d}$ in advance and predistort the beam-forming control vector $\bar{C}$ so that the effect of the couplings is cancelled. This is achieved by multiplying the control vector with a matrix $\mathbf{G_{pd}}$ satisfying the condition

$$\mathbf{G_{pd}} = \mathbf{G} / \mathbf{G_d}. \qquad (12)$$

Then the output voltage is given by

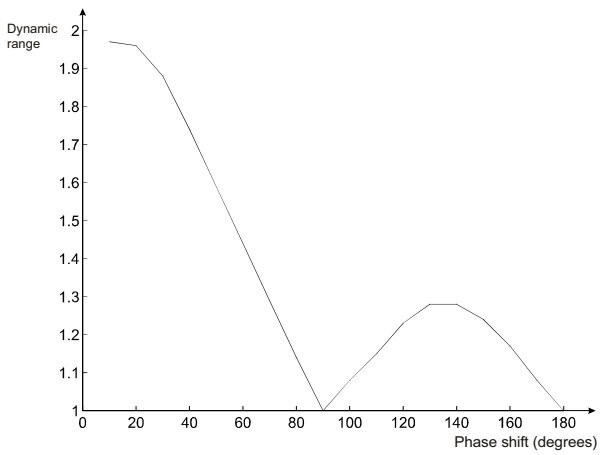

Fig.4 The dynamic range required by the vector modulator for the case Z g =(2+j*2)Ω, Z_L=j*33Ω, Z_M=j*13Ω

$$\overline{V}_o = \mathbf{G_d} \times \mathbf{G_{pd}} \times \overline{C} \times \overline{V}_i, \qquad (13)$$

which is equal to the ideal transfer equation given by eq.1. and the effect of parasitic couplings is cancelled from the output.

The multiplication $\mathbf{G_{pd}} \times \overline{C}$ takes place in digital domain and, assuming static couplings, $\mathbf{G_{pd}}$ may be found in advance. In this case the predistortion will require one matrix multiplication per beam-direction, which is computationally cheap.

The predistortion matrix $\mathbf{G_{pd}}$ was calculated for the same nonidealities as in fig. 2 and a new control vector was calculated. The resulting beam with the predistortion control together with the ideal one is shown in fig. 3. The real and imaginary controls of the vector modulators were quantized to 5 bits [6], which is why there is a small residual error in the beam.

Since the predistortion is applied digitally to the control vector, it is vital that the vector modulators have adequate control dynamic range to accommodate the predistortion. The required dynamic range was simulated for the same nonidealities as in fig. 2 for phase shifts ranging from 0 to 180º. The result in fig. 4 is normalized to the control range required in the ideal case.

The dynamic range appears to be very dependent to the phase shifts. For phase shifts of 90º and 180º there is no error, which is attributed to the balance between the four output PAs. The large increase in the required control range when all antennas are driven with the same phase is mainly due to the degeneration effect of the common ground impedance. In order to account for the gain sensitivity to the antenna phasing it is either necessary to allocate some of the vector modulator resolution for that or to compensate for the gain error earlier in the chain and correct only the direction of the beam with the vector modulators.

5. CONCLUSION

The effects of parasitic coupling between signals paths in an integrated beam-forming transmitter were studied. A methodology based on n-port chain matrices was used to capture both the loading effects between stages as well as the internal couplings between separate signal paths. The method allows breaking the coupling analysis into smaller parts and then evaluating their effect on the whole transmitter chain. Consequently, the accuracy of the antenna beam can be estimated in advance.

Predistorting the beam forming control vector was proposed as a means to eliminate the effect of the parasitic couplings. Since the couplings depend mainly on the technology and device geometries a predistortion matrix can either be estimated or measured in advance and then used to correct the control vector. Only a single matrix multiplication must then be performed in real time per beam direction.

The implications of the predistortion to the circuit implementation were studied and it was found that the predistortion will increase the control dynamic range of the vector modulators. However, most of the dynamic range increase is simple gain control, which can alternatively be placed elsewhere in the transmitter chain.

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