CMOS Power Amplifiers for Wireless Communication Systems

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Publication date:
2011

Document Version
Accepted author manuscript, peer reviewed version

CMOS Power Amplifiers for Wireless Communication Systems

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A dissertation submitted in partial fulfillment
of the requirements for the degree of

Doctor of Philosophy

in Wireless Communications

Aalborg University

Department of Electronic Systems

December 2010

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Published by:

Aalborg University
Faculty of Engineering and Science
Department of Electronic Systems
Technology Platforms
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ISBN: 978-87-92328-49-6

Abstract

This thesis summarizes results obtained during three year research in the field of CMOS RF power amplifiers (PA) at Technology Platforms Section of Aalborg University. In order to increase the data throughput of a wireless link modern communication systems employ both the amplitude and phase modulation of the RF carrier. This requires the use of linear RF power amplifiers. The linear PAs suffer by inherently low efficiency that leads to decreased talk time. To satisfy the demand for high linearity and high efficiency PAs there is need for new approach. A linearized and highly efficient switch-mode PA is one of the feasible alternatives.

Switch-mode PAs offer high efficiency but they are highly non-linear. Using suitable linearization technique they can be utilized in modern wireless transmitters. Nowadays the polar transmitter topology, where the amplitude and phase modulated signals are processed in two separate paths, is one of the major techniques that enables to employ a switch-mode PA in the RF transmitters with varying amplitude signals.

Because the amplitude modulated signal can not be directly applied to the RF input port as in a linear PA, a switch-mode PA has to use different method to combine the amplitude and phase modulated signals. In this thesis a new approach for amplification of modulated varying envelope signals is presented. The concept is called cascode modulated class-E PA.

The main advantages of the cascode modulated class-E PA are high output power dynamic range and no need for an external supply modulator as it is in the conventional power supply modulation method. The major drawback of cascode modulation is higher AM-AM distortion compared to the supply modulation.

Feasibility of the cascode modulated class-E PA concept was verified via its implementation in CMOS technology. The PA was tested with EDGE and WCDMA signals. In order to meet the linearity requirements imposed by GSM/EDGE and 3GPP standards a digital predistortion is used to linearize the PA.

Keywords: Class-E amplifier, CMOS, Envelope modulator, Polar transmitter, Power control, RF power amplifier

CMOS effektforstærkere til trådløse kommunikationssystemer

Resumé

Denne afhandling sammenfatter de resultater, der er opnået gennem tre års forskning i CMOS RF effektforstærkere (PA) ved Technology Platforms sektionen ved Aalborg Universitet. For at efterkomme transmissionskapaciteten bruger moderne kommunikationssystemer både amplitude og fasemodulation af RF bærebølgen. Det kræver brug af lineære RF effektforstærkere. Men en lineær PA har grundlæggende en lav effektivitet, hvilket medfører nedsat taletid. For at opfylde kravet om effektforstærkere med høj effektivitet og høj linearitet er der brug for en ny fremgangsmåde. En højeffektiv og lineariseret switch-mode PA er et af de egnede alternativer.

Switch-mode PA'er har høj effektivitet, men er meget ulineære. Ved brug af en passende lineariseringsteknik kan de anvendes i moderne trådløse sendere. For tiden er den polære sendertopologi , hvor amplitude og faseinformation behandles i to separate grene, en af de vigtigste teknikker som gør det muligt at anvende en switch-mode PA i RF sendere med signaler med varierende amplitude.

Da det amplitudemodulerede signal ikke kan tilføres direkte til RF indgangen som i en lineær effektforstærker, måen switch-mode PA bruge en anden metode til at kombinere amplitude og faseinformation. I denne afhandling er en ny metode til forstærkning af et moduleret signal med varierende amplitude præsenteret. Metoden kaldes kaskodemoduleret klasse E PA.

De vigtigste fordele ved den kaskodemodulerede klasse E PA er et stort dynamikområde for udgangseffekten og intet behov for en ekstern modulation af forsyningsspændingen, i modsætning til den traditionelle metode med ekstern modulation af forsyningsspændingen. Den største ulempe ved kaskodemodulation er højere AM-AM forvrængning i sammenlignet med modulation af forsyningsspændingen.

At princippet i en kaskodemoduleret klasse E PA er egnet, er vist via en implementation i en CMOS teknologi. PA'en er afprøvet med EDGE og WCDMA signaler. For at opfylde de linearitetskrav, der stilles i standarderne fra GSM/EDGE og 3GPP er der brugt digital modforvrængning til at linearisere PA'en.

CMOS Power Amplifiers for Wireless Communication Systems

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Date Approved: December 14, 2010

This work was supported by

Texas Instruments Denmark

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List of Abbreviations

3G	Third generation wireless technology defined by International Mobile Telecommunications-2000
3GPP	3rd generation partnership project
ACLR	Adjacent channel leakage ratio
AM	Amplitude modulated signal
BB	Base-band signal
BPF	Bandpass filter
BW	Bandwidth
CPCT	Cascode power control technique
CW	Continuous wave signal
DE	Drain efficiency
EDGE	Enhanced Data rates for GSM Evolution
EVM	Error vector magnitude
GMSK	Gaussian minimum shift keying
GSM	Global System for Mobile communications
IMD	Intermodulation distortion
LINC	Linear amplification with non-linear components
LUT	Look-up table
P_{in}	The available average input power
P_{out}	The average output power delivered into the $50\,\Omega$ load at the fundamental frequency
PA	Power amplifier
PAE	Power added efficiency
PAPR	Peak to average power ratio
PM	Phase modulated signal
PWM	Pulse width modulation

QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
R_L	Load resistor
RFC	RF choke inductor
SRC	Series resonant circuit
SVPCT	Supply voltage power control technique
UMTS	Universal Mobile Telecommunications System
V_{DD}	The supply voltage
VNA	Vector network analyzer
WCDMA	Wideband Code Division Multiple Access
ZVS	Zero voltage switching

Chapter 1

Introduction

Contents

Contemporary wireless communication technologies use complex digital modulation schemes what require the use of linear RF power amplifiers. The linear PAs suffer by inherently low efficiency what leads to a decreased talk time. Therefore, a new approach is needed to satisfy the demand for high linearity and high efficiency PAs. The linearized and high efficient switch-mode PA is one of the feasible alternatives.

Nowadays, most of the commercially available PAs use GaAs or InGaP devices that exhibit better high-frequency performance and higher quality of the passive on-chip components. On the other hand, high performance digital circuits are usually fabricated in the CMOS technology. There has been a significant effort to develop a fully integrated RF transmitter in the standard CMOS process technology. This will reduce the size and the costs of the RF transceivers.

The research in the wireless transceivers has been focused on the new system topologies that can reduce the power consumption and increase the system integration. Indeed, the number of additional discrete components has been significantly decreased but the ultimate goal of having the digital baseband circuits integrated with the high efficient RF circuits on the same die has not been achieved.

1.1 Modern wireless communication systems

Nowadays, it is very common to share the personal high-resolution photos and videos with friends, connect to life audio and video streams, download emails or just browse the internet. Beside that users expect soon to have available an internet access with very high data rates (at least 100 Mbps) and also the possibility of the on-line gaming (that requires the latency below 10 ms in the wireless network).

Modern communication systems employ both the amplitude and phase modulation of the RF carrier in order to increase the data throughput of a wireless link. The amount of data transferred through the mobile terminals in the wireless network has significantly increased. To satisfy these needs the mobile standards have to evolve rapidly. The frequency spectrum is scarce and therefore spectrally efficient modulations are used. This leads to the use of varying amplitude and phase modulation techniques.

The first widely used standard which employed the phase and amplitude modulation was the Enhanced Data rates for GSM Evolution (EDGE). It offers much higher data rates and has much higher spectral efficiency (bps/Hz) than the Global System for Mobile Communications (GSM). It is using 8PSK modulation which results in 3.4 dB peak to average power ratio (PAR). The maximum data rate is 473.6 kbit/s for both the up-link and down-link.

The most widely used mobile data systems are employing the third generation wireless technology (3G). In Europe it is implemented by the UMTS (Universal Mobile Telecommunications System). This system is using the CDMA (Code Division Multiple Access) technology. The up-link modulation scheme utilizes the QPSK (Quadrature Phase Shift Keying) or in case of HSPA+ (Evolved High Speed Packet Access) 16-QAM (Quadrature Amplitude Modulation). Both modulations require a linear amplification to prevent the power leakage into the neighboring channels.

The emerging standard is called LTE (Long Term Evolution) or sometimes it is referred to as 3.9G. It supports both the FDD (Frequency Division Duplex) and TDD (Time Division Duplex). The down-link utilizes OFDMA (Orthogonal Frequency Division Multiple Access) and the up-link SC-FDMA (Single Carrier FDMA) scheme. The LTE is employing QPSK, 16-QAM or 64-QAM modulation which requires a linear amplification. It allows up to 326 Mbpsk downlink and 86 Mbpsk uplink speeds.

The selected mobile standards are compared in the Table. 1.1. Note that only the highest theoretical performance indicators are specified (max down-link and up-link speeds).

	GSM	EDGE	WCDMA	HSPA	HSPA+	LTE
Max down-link speed [bps]	85.6 k	473.6 k	384 k	14 M	56 M (MIMO)	326 M (4x4 MIMO)
Max up-link speed [bps]	42.8 k	473.6 k	384 k	5.7 M	22 M	86 M (64-QAM)
Latency (round trip) [ms]	600	300	150	100	50	10
Channel bandwidth [Hz]	200 k	200 k	5 M	5 M	5 M	1.5 M - 20 M
Duplex schemes	FDD	FDD	FDD	FDD	FDD	FDD, TDD
Access schemes (up-link)	TDMA FDMA	TDMA FDMA	CDMA	CDMA	CDMA	SC-FDMA
Modulation types supported (up-link)	GMSK	8-PSK	QPSK	BPSK QPSK	16-QAM	QPSK 16-QAM 64-QAM

Table 1.1: Comparison of selected mobile systems.

The linear PA has to operate with a sufficient power back-off in order to amplify signals with a high PAR otherwise the output signal will be distorted. This degrades the

PA efficiency. On the other hand, the phase modulated PA always operates at its peak efficiency. The peak PA efficiency is not an important performance indicator because the output signal only seldom reaches the maximum. More important is the average efficiency that is calculated based on the probability distribution function of the power in the given system (EDGE, WCDMA etc.). The average efficiency is directly related to the mobile device efficiency in the wireless network.

The consequence of the varying amplitude modulation is that the PA has to be linear. Any non-linear effects which disturb the amplitude signal will cause errors in data and a distortion in the adjacent channels. Switch-mode PAs offer a high efficiency but they are highly non-linear. By using a linearization technique they can be utilized in modern wireless transmitters. Because the amplitude modulated signal can not be directly applied to the RF input port as in a linear PA, a switch-mode PA has to use a different method to combine the amplitude and phase modulated signals. Usually it is done using the polar transmitter topology.

In this thesis a new approach for amplifying modulated varying envelope signals is presented. The whole work is focused on switch-mode RF PAs that are attractive due to their high efficiency. The proposed concept of "cascode modulated class-E PA" was practically implemented in CMOS technology and tested with EDGE and WCDMA signals. Digital predistortion is used to linearize the PA in order to meet the linearity requirements imposed by the EDGE and WCDMA standards.

1.2 Organization of the thesis

The thesis is organized as follows. Chapter 2 explains the fundamental aspects of RF power amplifiers. The basic classes of operation are briefly introduced. Then the most important figures of merit of the PAs are discussed. Particular attention is given to the PA efficiency analysis. Linearity aspects of the RF PAs are explained.

In Chapter 3 linear transmitters using switch-mode PAs are discussed. The chapter starts with the description of three different topologies which can be used to accommodate switch-mode PAs to amplify varying amplitude signals. First two methods, which are based on the pulse width modulation (PWM) technique and linear amplification using non-linear components (LINC) technique, are introduced in brief. The third method, polar transmitters, is explained in detail because it was used in the experimental work. State-of-the-art approaches of polar modulate PAs are shown.

Chapter 4 handles the class-E PA analysis and design. The principles of operation of the class-E amplifier are explained and the architectural design issues are discussed. The chapter starts with an analytical section where the operation of the class-E amplifier is mathematically described. Later non-idealities that significantly influence the behavior of the class-E amplifier are introduced. The chapter is concluded with a small section on the impedance transformation.

Chapter 5 discuss various aspects of the cascode modulated class-E PA. The simulated performance of the simplified cascode class-E PA is shown. The main part of the chapter is the analysis of design aspects and trade-offs in the cascode class-E PA.

The focus is on the study of how the sizing of the cascode transistors influences the input and output capacitance, ON resistance, drain efficiency and the PA driving requirements. The reliability issues of CMOS class-E PAs are described with particular focus on the reliability of the proposed cascode modulated class-E PA.

In Chapter 6 various models of the cascode modulated PA are discussed. Firstly, the current RF analysis of the cascode class-E PA is performed. Then two DC models are proposed. The last step in the cascode class-E PA modeling is the analytical model. The goal of the modeling is to analytically describe the transfer function of the PA and to understand the distortion mechanisms in the cascode modulated PA.

Chapter 7 presents the experimental results of the implemented cascode modulated class-E PA in CMOS technology. The suitability of the cascode class-E PA concept for PA power control is firstly demonstrated. In the second part of the chapter the measured results of the cascode modulated class-E PA using EDGE and WCDMA test signals are shown. The simulated and measured results are compared. In addition, the digital predistortion linearization technique is described. The digital predistortion technique is used to linearize the PA. The performance with and without the digital predistortion is compared.

Chapter 8 summarizes the thesis and also provides ideas for possible future research in the area of CMOS polar PAs.

Chapter 2

Fundamentals of RF PAs

Contents

The PAs can be divided into several groups according to linearity, efficiency, frequency, technology and output power. Traditionally, the PAs are divided into two groups: linear and switch-mode PAs. The common characteristic of all the PAs is that the most linear classes are the least efficient.

In the linear class the power transistor operates as a transconductor. One can expect that in the linear PA the output power is a linear function of the input power. This is literally true only for the class-A PAs and as it is shown further, not all linear PAs exhibit a high linearity. Therefore, a better name for this group of PAs would be the transconductance PAs.

In the switch-mode class the power transistor operates as a switch. Sometime these PAs are referred to as saturated or non-linear. The switching PAs are very efficient but they require harmonic filtering at the output in order to obtain the desired output signal.

The first part of this chapter will describe the basic types of RF PAs. The second part will introduce the common figures of merit of the PAs.

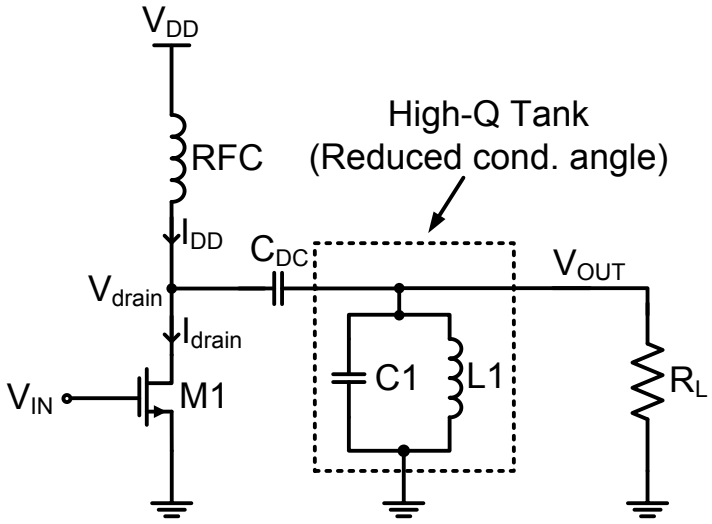


Figure 2.1: Simplified circuit of class-A amplifier (dashed LC tank is used for reduced conduction angle operation).

2.1 Transconductance PAs

In these PAs the active device operates as a transconductor or simply as a voltage controlled current source. The transconductance PAs are divided into classes A, AB, B and C. Class-F is usually assigned as a switch-mode PA, but the active device of class-F PA operates as a transconductor (unless it is driven very hard) and therefore it should belong to the transconductance PAs.

2.1.1 Class-A

The class-A PA is biased in such a way that the active device is always ON and it always conducts a quiescent current. The conduction angle, which represents the time of the RF cycle when the PA is ON, is 360°. The idealized class-A amplifier is shown in Fig. 2.1.

If the active device exhibits a linear transconductance characteristic, the output waveform has no distortion. Therefore, the output power can be expressed as

$$P_{out} = \frac{V_{out}^2}{2R_L} \tag{2.1}$$

where V_{out} is the amplitude of the output RF voltage and R_L is the load. Note that the harmonic filter at the PA output is not needed (in ideal operation) because the output signal contains only the fundamental component (see Fig. 2.2). In order to calculate the drain efficiency the DC power drawn from the supply has to be known. This can be written as

$$P_{DC} = V_{DD} I_{DD} = \frac{V_{DD}^2}{2R_L} \tag{2.2}$$

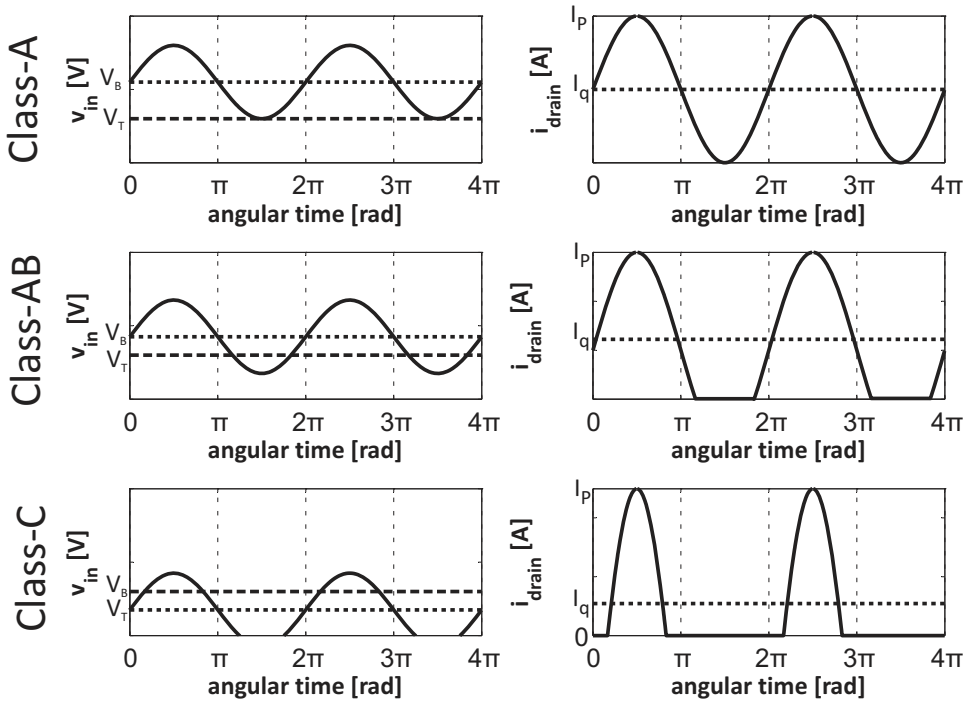


Figure 2.2: Illustration of input and output waveforms of class-A, AB and C amplifiers. V_T is the threshold voltage of the active device and V_B is the bias voltage of the amplifier. I_p is the peak current and I_q is the quiescent drain current through the output device.

where V_{DD} and I_{DD} are the supply voltage and the supply current respectively. It is assumed that the quiescent current is chosen to maximize the output voltage swing and equals to V_{DD}/R_L. Finally the maximum drain efficiency is equal to

$$\eta_{max} = \frac{P_{out,max}}{P_{DC}} = \frac{1}{2}\frac{V_{out,max}^2}{V_{DD}^2} = \frac{1}{2}\left(\frac{V_{DD}}{V_{DD}}\right)^2 = 50\% \tag{2.3}$$

where it is assumed that the maximum amplitude of the output voltage equals to V_{DD}. Practically the drain efficiency will be even lower because the maximum output voltage swing is decreased by the necessary drain-source voltage needed to keep the MOS transistor in the saturated region. The drawback of the high quiescent current is therefore low peak drain efficiency. The DC power (it is constant and independent of the output power) which is not converted into the RF power has to dissipate in the PA (in the form of heat). The heat dissipation is highest when the output power is low.

If the active device exhibits a non-linear transconductance, for example the square law characteristics as in the CMOS transistor, then the drain current through the power

transistor will be distorted. This can be seen from

$$\begin{aligned} i_d &= K\, v_{in}^2 = K\,(V_B + V_{in}\sin(\omega t))^2 \\ &= KV_B^2 + \frac{1}{2}KV_{in}^2 + 2KV_BV_{in}\sin(\omega t) + \frac{1}{2}KV_{in}^2\cos(2\omega t) \end{aligned} \tag{2.4}$$

where V_B is the bias voltage and K is a constant. It can be seen that the drain current has beside the DC and fundamental components also the second harmonic component. Therefore, the harmonic filter at the output of such a class-A PA is needed to select the fundamental component. The linearity of the PA using the square law transconductance active device is deteriorated compared to the linear transconductance active device but the peak drain efficiency increased to 66.7 % [Cripps 2002].

2.1.2 Classes AB, B and C

One possibility to increase the efficiency of the class-A amplifier is to limit the conduction angle. If the transistor doesn't have to conduct during the whole RF period it will be more efficient. The class-AB PA has a conduction angle between 180° and 360°.

The topology of the class-AB amplifier is the same as for class-A amplifier with the exception that the class-AB amplifier requires an output harmonic filter (Fig. 2.1). If the output resonant tank has a high quality factor, the output voltage will be a sine wave.

The conduction angle is adjusted by the bias voltage (Fig. 2.2). As the input voltage drops below the threshold voltage the drain current goes to zero. The conduction angle is directly related to the quiescent current (Fig. 2.2) of the PA. The lower conduction angle is a result of the lower input bias voltage and this will lead to the lower quiescent device current.

By decreasing the conduction angle even further the efficiency is improved but the linearity decreases. Class-B amplifier is defined as an amplifier with conduction angle of 180°.

In the class-B amplifier half of the output signal is clipped every RF cycle compared to the class-A amplifier. This will produce even components in the output signal but no odd harmonics. The main advantage of class-B amplifier is that the output power level of the fundamental tone is the same as in class-A amplifier but the peak drain efficiency is increased to 78.5 % due to the reduced DC current [Albulet 2001].

The DC input power and the drain efficiency of the class-B amplifier can be expressed as [Albulet 2001]

$$P_{DC} = V_{DD}I_{DD} = \frac{2}{\pi}\left(\frac{V_{DD}}{R_L}\right)V_{drain} \tag{2.5}$$

$$\eta_{max} = \frac{P_{out,max}}{P_{DC}} = \frac{\pi}{4}\left(\frac{V_{drain,max}}{V_{DD}}\right) = \frac{\pi}{4} = 78.5\% \tag{2.6}$$

where V_{drain} is the amplitude of the RF voltage across the active device.

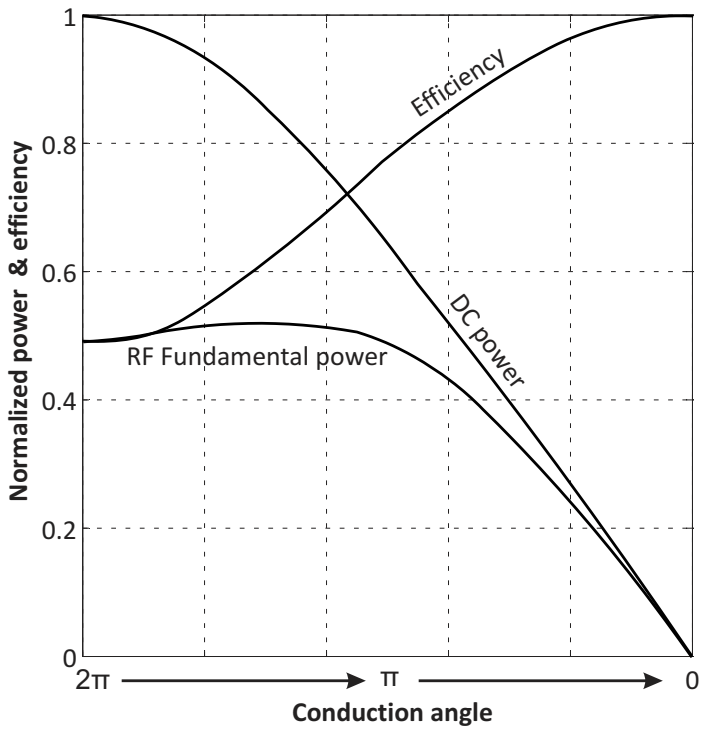


Figure 2.3: The comparison of RF Fundamental output power, drain efficiency and DC power as a function of conduction angle.

It is important to note, that the class-B amplifier exhibits only one half of the gain of a class-A amplifier and therefore it requires a 6 dB higher input drive level in order to deliver the same output power and to keep the same peak transistor current [Cripps 2006].

Further reduction of the bias voltage results in a conduction angle below 180° and this is the area of operation of the class-C amplifier. This amplifier can theoretically achieve 100 % drain efficiency but it will deliver no RF output power (Fig. 2.3). This can be explained by that the reduction of the bias voltage leads to a very high drain current peak (if the output power has to be maintained). The maximum current is limited by the safety operation area of the device. Therefore, for a given maximum drain current the output power and the quiescent current are decreasing with decrease of the conduction angle. The 100 % drain efficiency is achieved but the output power and the DC power goes to zero [Reynaert & Steyaert 2006]. The application of class-C amplifiers in low voltage CMOS technologies is limited due to the low output power. The comparison of RF output power, efficiency and DC power is shown in Fig. 2.3.

The class-AB PA is often used in wireless communication transmitters because it is more efficient than the class-A amplifier and it still maintains a high linearity (compared to the class-B or class-C amplifiers) [Cripps 2002]. The class-C amplifier can be used in such applications that don't require the linear amplification (for example amplifying

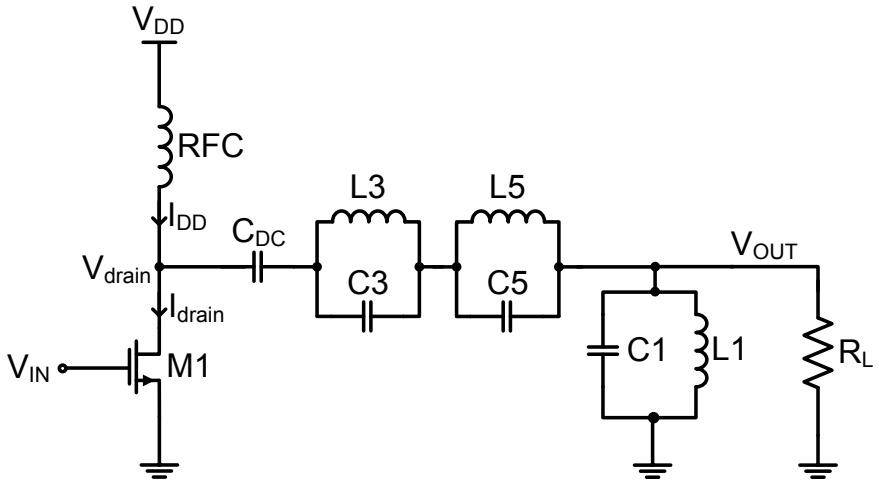


Figure 2.4: Simplified circuit of the class-F amplifier.

CW or FM signals).

2.1.3 Class-F

The main idea used in class-F amplifiers is that by the proper harmonic terminations, the drain voltage and current waveforms have no overlap what will result in minimized power losses in the active device. The schematic of a class-F PA is shown in Fig. 2.4.

If the drain voltage is square wave like then the instantaneous overlap between the drain voltage and current is minimized and there is no power loss in the power transistor. The square waveform contains ideally no even harmonics but an infinite number of the odd harmonics. Therefore, by choosing the output network which filters out all even harmonics and is open for odd harmonics, the square waveforms can be achieved.

Practical implementations are usually using third and fifth harmonics what is sufficient to produce significant improvement in the drain efficiency [Reynaert & Steyaert 2006]. The active device of such amplifier can not be substituted by a switch (switch will produce infinite number of harmonics) and therefore the class-F PA with limited harmonics peaking is as biased as the class-B PA.

The main drawbacks of the class-F PA implementation in the CMOS technology are as follows. In order to shape the harmonics at the output of the active device the harmonics must be present in the active device output current. The problem is that the large output capacitance will provide a low-impedance path for the higher harmonics and the squaring process will be less pronounced. If the third and fifth harmonic peaking is used the theoretical drain efficiency is 88 % and 92 % respectively [Reynaert & Steyaert 2006]. Another drawback is that the implementation of the output network in CMOS is difficult and might not be even feasible (several high quality resonant tanks or a $\lambda/4$ transmission line are needed).

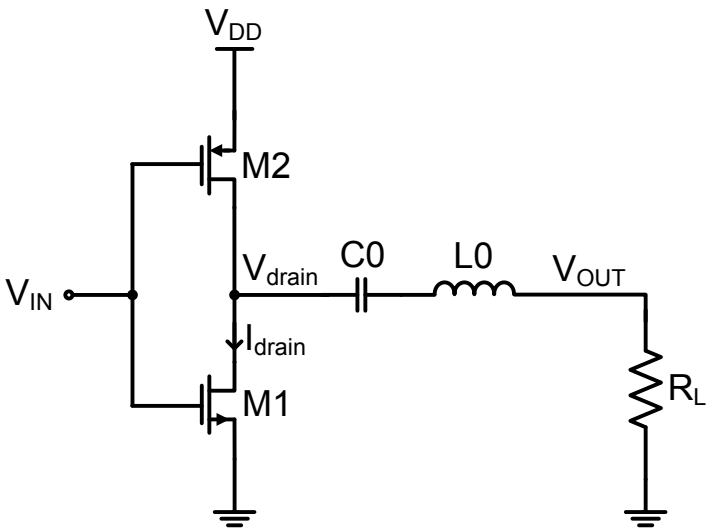


Figure 2.5: Simplified circuit of the class-D amplifier.

2.2 Switch-mode PAs

The switch-mode PAs are divided into two main classes D and E. The common characteristic of the switch-mode amplifiers is that the active device operates as a switch. In the ideal switch there is no overlap of current and voltage waveforms and this leads to the theoretical 100 % drain efficiency. The main drawback of the switching PAs is that the linearity is completely lost. This is a consequence of operating the active device as an ideal switch which has only two (ON/OFF) states. These amplifiers are not-suitable for the amplitude modulated signals. In order to use them to amplify varying envelope signals a linearization technique has to be used.

2.2.1 Class-D

The schematic diagram of a class-D amplifier is shown in Fig. 2.5. The series resonant output network is connected to the push-pull circuit. The active devices are working in anti-phase (one device is ON and the second device is OFF). The output network is alternately connected to the DC supply voltage or to the ground. The waveforms of the class-D amplifier are shown in Fig. 2.6.

It can be seen that the voltage at the drain of the transistors is a square wave. The output current is sinusoidal due to the series resonant output circuit which is tuned to the fundamental frequency. The positive half of the sine wave is conducted by the top switch M2 and the negative by the bottom switch M1.

The output current is sinusoidal at can be written as [Albulet 2001]

$$i_{out}(\phi) = \frac{2}{\pi}\left(\frac{V_{DD}}{R_L}\right)\sin(\phi) \tag{2.7}$$

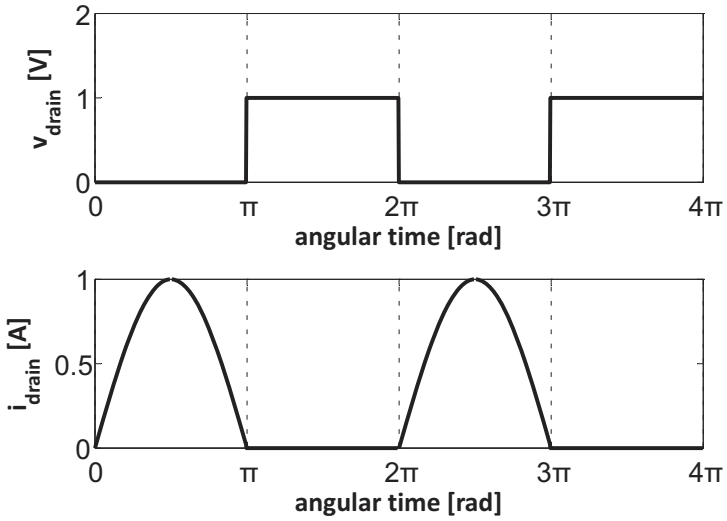


Figure 2.6: Drain voltage and current waveforms of the class-D amplifier.

where ϕ is angular time given as $(\omega t + \varphi)$. The output power is given by

$$P_{out} = I_{DD}(I_{DD}R_L) = \frac{2}{\pi^2}\frac{V_{DD}^2}{R_L} \tag{2.8}$$

The DC power can be calculating according to

$$P_{DC} = V_{DD}I_{DD} = V_{DD}\left(\frac{1}{2\pi}\int_{n=0}^{2\pi} i_1(\phi)d\phi\right) = V_{DD}\left(\frac{2}{\pi^2}\frac{V_{DD}}{R_L}\right) = \frac{2}{\pi^2}\frac{V_{DD}^2}{R_L} \tag{2.9}$$

and the maximum drain efficiency can be expressed as

$$\eta_{max} = \frac{P_{out}}{P_{DC}} = 100\% \tag{2.10}$$

Several circuit modifications of the class-D amplifier are known [Albulet 2001]. These modifications include the transformer coupled voltage or current output circuit.

The main difficulty of implementing class-D RF PA in CMOS technology is decreased efficiency. It is assumed that the active devices in Fig. 2.5 operate as ideal switches. Such large transistors have large parasitic output capacitances that have to be charged and discharged every RF cycle. This energy will be dissipated in the switch. Large output capacitance will also limit the usable operation frequency. Furthermore, the finite turn-on and turn-off time will increase the power losses because the voltage and current waveforms will overlap. Class-D requires a high driving power because of the large input capacitance (two transistors has to be driven).

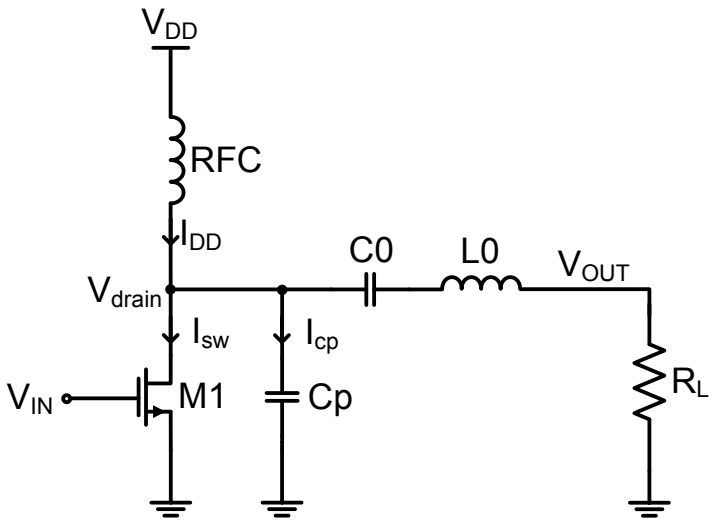


Figure 2.7: Simplified circuit of the class-E amplifier.

2.2.2 Class-E

Another type of the switch-mode amplifier is the class-E amplifier. It can achieve theoretically 100 % drain efficiency as the class-D amplifier, but its concept is based on a completely different approach. The basic topology of the class-E PA is shown in Fig. 2.7.

The basic class-E amplifier utilizes a single transistor which acts as a switch (M1). The output network consists of series resonant circuit (C0 and L0) and shunt capacitor (Cp). The main advantage of the class-E is that the parasitic output capacitance of the active device becomes an element in the output network design. In the previously described classes the parasitic output capacitance of the active device is unwanted and it degrades the performance of the PA. The class-E amplifier requires a small number of passive components (especially compared to the class-F amplifier) what makes it a promising candidate for the CMOS integration.

The role of the output network in class-E amplifier is to shape the drain voltage and device current in such way that there is no instantaneous overlap between them. The basic equations of class-E amplifier are derived in Section 4.1. One of the first detailed mathematical analysis can be found in [Raab 1977]. Very comprehensive analysis of class-E PA can be also found in this book [Albulet 2001]. The class-E PA can be analyzed from various perspectives (duty cycle ratio, finite turn-on and turn-off times, parasitic resistance and inductance of the active device, quality of the output resonant tank, finite RF choke inductance and etc.). Even though the analysis is based on very simplified circuit and assumptions the mathematical derivations are still very complex.

There are three conditions which have to be fulfilled in order to achieve a high efficiency. The first is called the zero voltage switching (ZVS) condition and the second is zero voltage derivative switching (ZVDS) condition. The ZVS condition dictates that the voltage across the switch has to be zero in the instance the switch goes ON. The

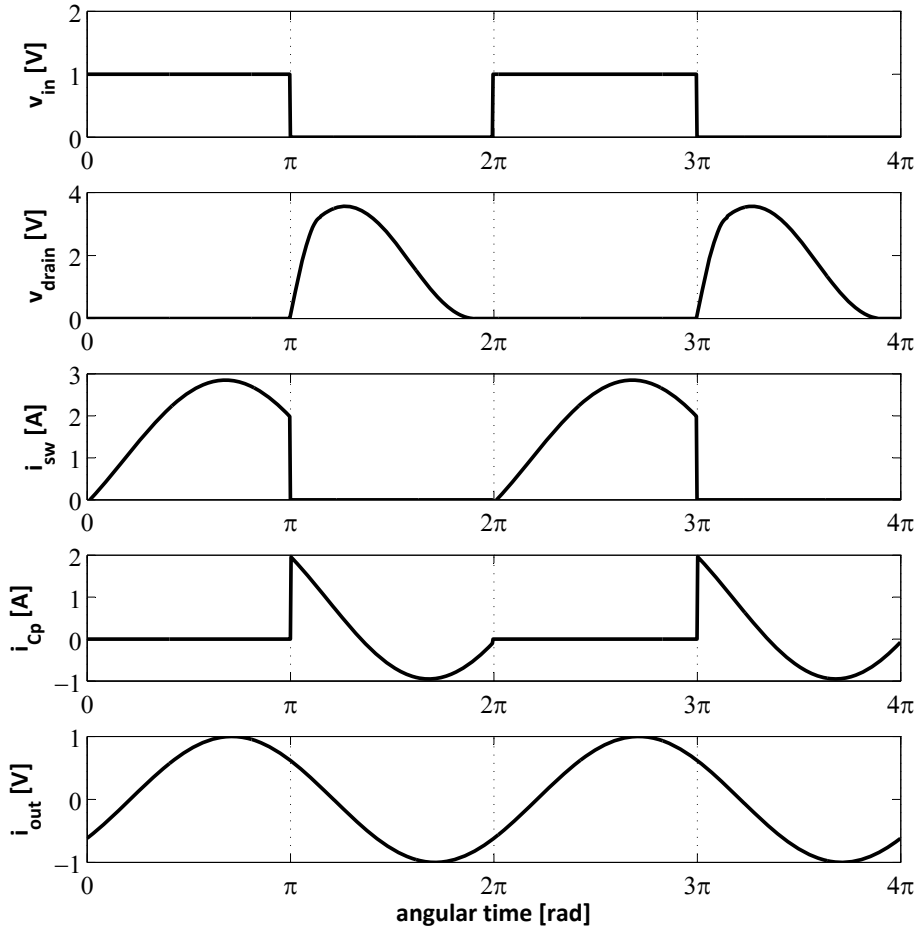


Figure 2.8: The waveforms of the class-E amplifier.

ZVDS condition says that also the derivative of the voltage across the switch has to be zero. These two condition guarantee that the power loss during the switch turn-on is minimized. The third condition is that the rise of the voltage across the switch has to be delayed until the switch is turned OFF to reduce the turn-off transition loss. A more broaden definition of the conditions, provided by the founders of class-E PA, can be found in [Sokal & Sokal 1975]. If the amplifier meets the three conditions it is called an optimum class-E amplifier.

Fig. 2.8 shows the ideal waveforms of the class-E amplifier. It is assumed that the input signal is a square wave with 50 % duty cycle.

It can be seen that there is no instantaneous overlap of V_{drain} and I_{sw} and therefore the switch operates losslessly. When the switch is ON the current flowing through the active device is equal to the DC current (I_{DD}) minus the output current (i_{out}). When the switch is turned OFF the DC current minus the output current will charge the

shunt capacitor C_d. The shape of the drain voltage of the active device in the OFF state, which equals to the voltage across the capacitor C_d, is controlled by the output network. The output network is designed to turn the voltage across C_d back to zero (fully discharge the C_d) before the switch is again turned ON. The output current i_{out} is filtered by the ideal series resonant circuit and therefore it is assumed to be sinusoidal. It can be seen from Fig. 2.7 that the sinusoidal output current is a sum of partial sinusoid currents through the switch (during ON state) and through the shunt capacitor C_d (during OFF state).

It is important to note that the class-E is designed in the time domain because the behavior of the class-E (shapes of device voltage and current waveforms) is described in the time domain (by ZVS and ZVDS conditions).

The main drawback of the class-E amplifier is that the drain voltage peak (during the OFF state) is very high, theoretically $3.6\,V_{DD}$ [Sokal & Sokal 1975]. This represents a serious reliability problem. A transistor with a high break-down voltage is needed or another special technique (like transistors stacking) can be used to relieve the voltage stress of the active device. More on reliability is in Section 5.5.

2.3 Figures of merit

In this section some basic figures of merit of PAs are introduced. Firstly typical parameters of PAs like the output power, power added efficiency (PAE) and peak-to-average power ratio (PAR) are explained. Selected topics on the PA linearity are discussed including AM-AM, AM-PM, harmonic distortion, intermodulation distortion (IMD), adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM).

2.3.1 Output power

The instantaneous output power can be calculated as

$$p_{out}(t) = v_{out}(t) i_{out}(t) \tag{2.11}$$

where $v_{out}(t)$ and $i_{out}(t)$ are instantaneous output voltage and current respectively. The average output power can be written as

$$P_{out} = \overline{p_{out}(t)} = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} p_{out}(t)\, dt \tag{2.12}$$

where $\overline{p_{out}(t)}$ represents the average of the instantaneous output power. If it is not stated otherwise, in this work under the output power we understand the average output power. If the output signal is periodical with the period given by

$$T_0 = \frac{2\pi}{\omega} \tag{2.13}$$

where the angular frequency ω is defined as $\omega = 2\pi f_c$. The average power of a periodic signal can then be calculated using

$$P_{out} = \frac{1}{T_0} \int_{-T_0/2}^{T_0/2} p_{out}(t)\, dt \tag{2.14}$$

The average power delivered to a purely resistive load can also be calculated from the current and the voltage signal according to

$$P_{out} = \frac{V_{out,RMS}^2}{R_L} = I_{out,RMS}^2 R_L \tag{2.15}$$

where $V_{out,RMS}$ and $I_{out,RMS}$ are the RMS values of the output voltage and the current respectively.

2.3.2 Efficiency

In general, the term efficiency signifies how efficiently the PA is converting the DC power from the supply to the RF output power. The DC power drawn from the supply can be simply expressed as

$$P_{DC} = \frac{1}{T} \int_0^T V_{DD}\, i_{dd}\, dt = \frac{V_{DD}}{T} \int_0^T i_{dd}\, dt = V_{DD} I_{DD} \tag{2.16}$$

The more specific DC power calculation can be obtained for each PA class. The drain efficiency is defined as

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.17}$$

where P_{out} is the average output power at the fundamental frequency. Usually every PA consists of the output stage and at least one driver stage. The driver stage consumes also the DC power from the supply and therefore taking this into consideration, the total drain efficiency can be calculated according to

$$\eta_{tot} = \frac{P_{out}}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,DRV_i}} \tag{2.18}$$

where n is the number of driver stages.

The drawback of drain efficiency is that it doesn't depend on the gain of the PA. If two PAs have the same output power and draw the same DC power they still might have different gain and input power. Hence, a different concept is often used to characterize

the efficiency of the PA. It is called PAE (Power Added Efficiency) and it is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC,PA} + \sum_{i=0}^{n} P_{DC,DRV_i}} \tag{2.19}$$

where P_{in} is the available input power. If the power gain is defined as

$$G_P = \frac{P_{out}}{P_{in}} \tag{2.20}$$

then the equation 2.19 can be rewritten as

$$PAE = \eta_{tot}\left(1 - \frac{P_{in}}{P_{out}}\right) = \eta_{tot}\left(1 - \frac{1}{G_P}\right) \tag{2.21}$$

It can be seen that if the two PAs have the same output power and DC power, the PA which has a higher gain will have a higher PAE.

In the previous section the peak drain efficiencies of a different PA classes were given. In some classes this efficiency was 100 %. But the total drain efficiency and PAE of the PA are always below 100 %. The PAs are usually characterized by both PAE and drain efficiency.

2.3.3 Output power and efficiency of amplitude modulated signals

The previous analysis is valid for the constant envelope signals. If an amplitude modulated signal is applied to the PA both the output power and the efficiency are also functions of the varying envelope signal.

The output is varying according to the amplitude modulated signal. This variation can be described by parameters like Crest Factor (CF) in case of voltage signals and by Peak to Average Power Ratio (PAPR) when the power signals are handled. The PAPR is defined as

$$PAPR = \frac{PEP}{P_{out}} \tag{2.22}$$

where PEP stands for Peak Envelope Power and P_{out} is the average output power of the amplitude modulated signal. The peak envelope power is defined as the average power supplied to the antenna transmission line by a transmitter during one RF cycle at the crest of the modulation envelope, under normal operating conditions [ITS 1996]. The PEP of the PA can be expressed as

$$PEP = max\{P_{out}\} = \frac{max\{v_{out}^2(t)\}}{R_L} = \frac{V_{out}^2}{R_L} \tag{2.23}$$

where V_{out} is the amplitude of the output voltage signal v_{out}. The average output

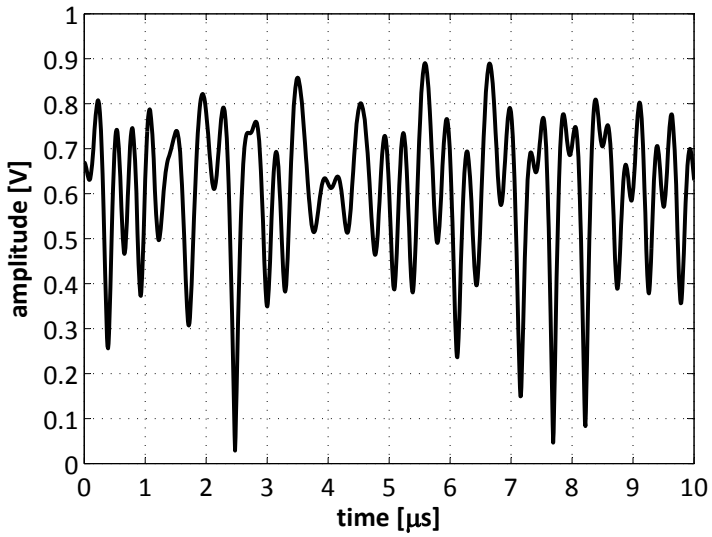


Figure 2.9: The AM component of the WCDMA signal.

power of the PA can be calculated as

$$P_{out} = \frac{V_{out,RMS}^2}{R_L} = \frac{1}{2}\frac{V_{out}^2}{R_L} \tag{2.24}$$

where a sinusoidal output signal is assumed. The Crest Factor (CF) is defined as the peak amplitude divided by the RMS value of the waveform

$$CF = \frac{max\{v_{out}\}}{V_{out,RMS}} = \frac{V_{out}}{V_{out,RMS}} \tag{2.25}$$

Fig. 2.9 shows the example of the time varying amplitude modulated component of the WCDMA signal. The PAPR equals to $PAPR = CF^2$ according to

$$PAPR = \frac{\frac{V_{out}^2}{R_L}}{\frac{V_{out,RMS}^2}{R_L}} = \frac{V_{out}^2}{V_{out,RMS}^2} = (CF)^2 \tag{2.26}$$

If both PAPR and CF are in dBs then $PAPR = CF$ according to

$$PAPR\,[dB] = 10\log\frac{V_{out}^2}{V_{out,RMS}^2} = 20\log\frac{V_{out,max}}{V_{out,RMS}} = CF\,[dB] \tag{2.27}$$

The CF of some selected signals can be find below in the Table. 2.1.

Generally, the efficiency of the PA which has to transmit a signal with a high PAPR will be much lower than the peak efficiency of the PA when it is saturated. The linear PA which has to amplify a modulated signal with high PAPR has to be capable to

	DC	Sine wave	Two-tone	QPSK	16-QAM	64-QAM	OFDM
Crest Factor [dB]	0	3.01	3 - 6	3.5 - 4	6.7	7.7	12

Table 2.1: Crest factor comparison of various waveforms.

transmit the PEP but the average output power will be much lower. The input power of the linear PA has to be decreased according to the PAPR of the modulated signal so that the signal can be transmitted without pushing the PA into saturation. This mode of operation is called power back-off. The power back-off linearization technique significantly decreases the overall efficiency of the PA and it is one of the major reasons why the linear PAs have such a low efficiency when they transmit complex modulated wireless signals with a high PAPR.

The efficiency of a PA is a function of the varying envelope signal($A(t)$). Generally, the efficiency is always a function of the output power. Because the amplitude modulation modulates the output power it will also change the efficiency. To characterize this effect one can define the average drain efficiency as [Reynaert & Steyaert 2006]

$$\eta = \langle \eta(A(t)) \rangle = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \eta(A(t))\, dt \tag{2.28}$$

Notice that the equation obove gives an arithmetic average of drain efficiency and it is different from average efficiency calculated based on Eq. (2.17).

Another effect which directly influences the overall efficiency is the probability distribution function (PDF) of the output power. The average output power level is usually set by the base station which is constantly evaluating the quality and power of the received signal. The active power control can be used to increase the battery life time of a mobile device but it can also be used by the wireless network to maximize its capacity (WCDMA). The period of the power level adjustment is different for each mobile standard. The PDF of the output power is obtained by long term measurements and it is usually specified for the different network environments (urban or rural). An example of the output power PDF in EDGE/WCDMA is shown in Fig. 2.10.

The drain efficiency can be expressed as a function of the PDF according to

$$\eta = \frac{\int_{P_{out,min}}^{P_{out,max}} P_{out}\, PDF(P_{out})\, dP_{out}}{\int_{P_{out,min}}^{P_{out,max}} \frac{P_{out}}{\eta(P_{out})} PDF(P_{out})\, dP_{out}} \tag{2.29}$$

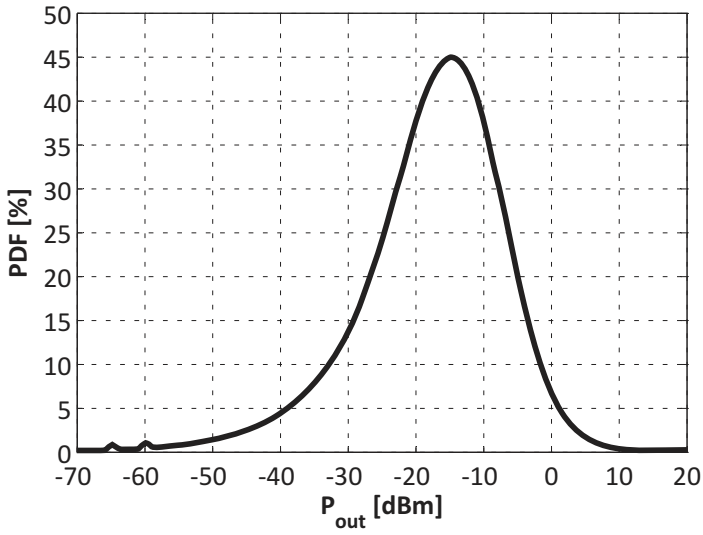


Figure 2.10: PDF versus output power of the WCDMA mobile station transmitter [Hamalainen *et al.* 1999].

2.3.4 Linearity

Linearity is one of the most important figures of merit of PAs. There are several ways to characterize the linearity, such as AM-AM and AM-PM distortion, intermodulation distortion (IMD), adjacent channel leakage ratio (ACLR), error vector magnitude (EVM), total harmonic distortion (THD) and third order intercept point (IP3). The non-linearity of a PA has to be properly classified and evaluated as a figure of merit.

One of the most basic PA metrics is 1 dB compression point (P1dB). It is defined as the output power level $P_{out,-1dB}$ corresponding to 1 dB deviation from the ideal linear behavior. It can be also referred to the input power level $P_{in,-1dB}$. The $P_{out,-1dB}$ usually specifies the maximum linear output power of the PA and $P_{in,-1dB}$ specifies what is the maximum input drive of the PA to operate still in linear region. The disadvantage of this metric is that it is not a very accurate indicator for complex modulated signals because it is based on a single-tone measurement and it can not provide information about the spectral regrowth near the carrier frequency.

Another linearity figure of merit used often in the low frequency amplifiers is the total harmonic distortion (THD). It is defined as the sum of the power of harmonic components to the power in the fundamental. Mathematically it can be written as

$$THD = \frac{\sum_{n\geq 2}^{\infty} P_{out,n}}{P_{out,1}} \tag{2.30}$$

where the n represents the number of harmonics considered in the simulation or measurements and $P_{out,1}$ is the power at the fundamental frequency. The THD is usually expressed in dBc units.

2.3.4.1 Amplitude and phase distortion

The amplitude and phase distortion are the consequence of the PA transfer characteristic nonlinearity. Assume that the transfer function of the PA is approximated by a third-order polynomial

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) \tag{2.31}$$

where $x(t)$ and $y(t)$ are the input and output signals of the PA respectively and $a_1 - a_3$ are constants. Suppose that the input signal is a sinusoid of this form

$$x(t) = A\cos(\omega_c t) = \frac{1}{2}(e^{j\omega_c t} + e^{-j\omega_c t}) \tag{2.32}$$

The resulting output signal is thus

$$y(t) = a_1 A\cos(\omega_c t) + a_2 A^2 \cos^2(\omega_c t) + a_3 A^3 \cos^3(\omega_c t) \tag{2.33}$$

this can be further expanded as

$$\begin{aligned} y(t) =& a_1 A\cos(\omega_c t) + a_2 A^2 \left(\frac{1+\cos(2\omega_c t)}{2}\right) + \\ & a_3 A^3 \left(\frac{3\cos(\omega_c t) + \cos(3\omega_c t)}{4}\right) \end{aligned} \tag{2.34}$$

finally the output can be written as

$$\begin{aligned} y(t) =& \frac{1}{2}a_2 A^2 + (a_1 A + \frac{3}{4}a_3 A^3)\cos(\omega_c t) + \frac{1}{2}a_2 A^2 \cos(2\omega_c t) + \\ & \frac{1}{4}a_3 A^3 \cos(3\omega_c t) \end{aligned} \tag{2.35}$$

where the first term represents the DC offset (as a result of the second-order term in the transfer characteristic), the second term represents the linear amplification at the fundamental frequency, the third and fourth terms represent the second and third harmonic distortion respectively.

The output power at the fundamental frequency can be written as

$$\begin{aligned} P_{out,1} &= \frac{1}{2R_L}V_{out,1}^2 = \frac{1}{2R_L}\left(a_1 A + \frac{3}{4}a_3 A^3\right)^2 \\ &= \frac{1}{R_L}\frac{A^2}{2}\left(a_1 + \frac{3}{2}a_3\left(\frac{A^2}{2}\right)\right)^2 = \frac{1}{R_L}P_{in}a_1^2\left(1 + \frac{3}{2}\frac{a_3}{a_1}(P_{in})\right)^2 \end{aligned} \tag{2.36}$$

and the power gain at the fundamental frequency is

$$G = \frac{1}{R_L}a_1^2\left(1 + \frac{3}{2}\frac{a_3}{a_1}(P_{in})\right)^2 \tag{2.37}$$

where $P_{in} = A^2/2$ is the normalized input power per Ohm. The term a_1^2 is the linear gain coefficient. The term $3a_3/2a_1$ represents a gain compression factor (usually is $a_3/a_1 < 0$ otherwise the PA would have gain expansion) and it is a cause of that the large signal gain G decreases with the input power. It can be seen that the output power and the power gain at the fundamental frequency are no longer linear functions of the input power.

The AM-AM and AM-PM characteristics show the relation of the output signal amplitude and phase on the input signal amplitude. An ideal linear PA has the output signal linearly dependent on the input signal and the output phase is independent of the input signal amplitude. Practically, a PA exhibits always some non-linearity. Therefore, with increasing the input signal level the PA goes into gain compression and the AM-AM will be nonlinear. Similarly the AM-PM response will be changed by increasing the input signal power. This can be mathematically described as

$$y(t) = F(A(t))\cos(\omega_c t + \phi(t) + \Phi(A(t))) \tag{2.38}$$

where $A(t)$ is the amplitude of input signal. The $F(A(t))$ is a nonlinear function of $A(t)$ and $\Phi(A(t))$ is not constant with the input signal level. There is a non-linear relationship between the input and output amplitude (AM-AM) and between the output phase and input amplitude (AM-PM).

There are several ways to measure AM-AM and AM-PM characteristics. The AM-AM and AM-PM response of the PA can be measured using the CW input signal with a swept power level. This is referred to as large signal S-parameters where the input source is a large signal (high power) source.

Another approach is to calculate the AM-AM and the AM-PM characteristics using a real modulated signal. The distorted output signal of the PA can be recorded and demodulated by a vector signal analyzer (VSA). The original baseband (BB) signal is then compared with the measured signal and the AM-AM and the AM-PM functions are obtained.

The AM-PM response is not measured as an absolute value of the phase between the input and output signal but it is the change of the phase as a function of the input signal power.

It is possible to plot the AM-AM and AM-PM characteristics as a function of the DC bias or ambient temperature. When the modeling of the PA is the main objective then the AM-AM and AM-PM response can be measured in a pulse mode in order to minimize the temperature increase caused by the previous input signal power level.

The AM-AM and AM-PM characteristics are not sufficient to fully characterize the non-linearity of the PA. This is especially true if input signals with different bandwidths (BW) are applied to the PA. Modern mobile standards do not specify the requirements on the AM-AM or AM-PM functions (neither on the IMD products) and other indicators like the ACLR or EVM have to be used.

The AM-AM and AM-PM can be expressed from the transfer function only if the coefficients a_k (in Eq. 2.31) are complex values (otherwise there is no AM-PM). The main problem of using AM-AM and AM-PM curves as a non-linearity figure of merit is

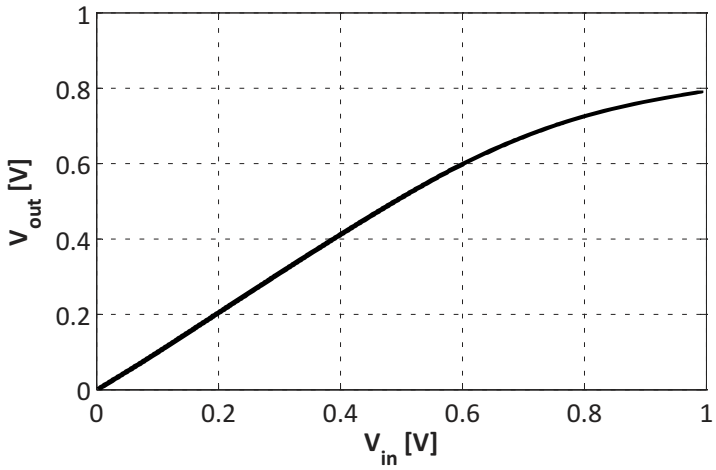


Figure 2.11: Example of AM-AM characteristic.

that they quantify the nonlinearity effect on the fundamental signal. The fundamental signal has a strong linear component and it might be difficult to precisely characterize the non-linear terms of the transfer function. The AM-AM and AM-PM curves are often used to linearize the PA.

2.3.4.2 IMD

In this subsection the intermodulation distortion (IMD) as a basic non-linearity figure of merit will be introduced. Single-tone tests are not sufficient to characterize the non-linearity of PAs because they don't provide any information about the PA behavior over the whole modulation band. Therefore, a two-tone test was introduced in order to investigate the PA non-linearity in the narrowband around the RF carrier. It can be used to investigate the amplitude and phase distortion of the PA.

By performing a two-tone test one can describe the intermodulation distortion (IMD) products and the spectral regrowth. The two test signals are individual single-tone signals. If the PA would have no distortion the output spectrum will contain only those two tones. The two-tone signal has a varying envelope in the time domain.

The PAPR parameter as a basic tool of characterizing varying envelope signals was described in Section 2.3.3. If the two-tone signal is defined as

$$s(t) = A\cos[(\omega_c - \omega_m)t] + B\cos[(\omega_c + \omega_m)t] \tag{2.39}$$

then the PAPR of the two tone signal can be calculated according to [Rouphael 2009]

$$PAPR\,[dB] = 10\log\left(\frac{PEP}{P_{out}}\right) = 10\log\left(\frac{(A+B)^2}{\frac{1}{2}(A^2+B^2)}\right) \tag{2.40}$$

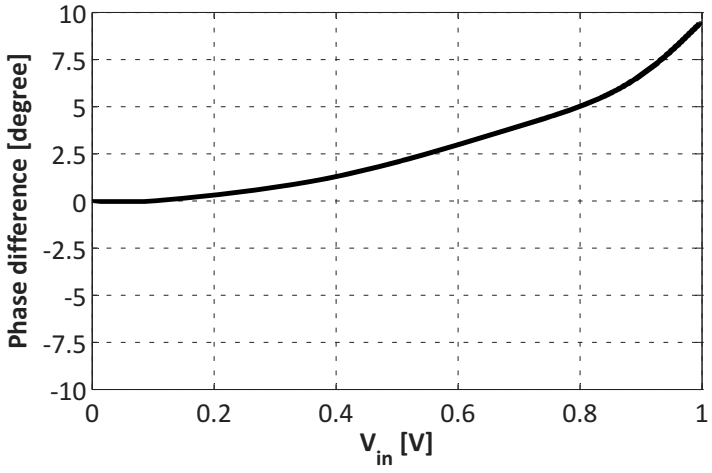


Figure 2.12: Example of AM-PM characteristic.

and if the two tones have equal power ($A = B$) then

$$PAPR\,[dB] = 10\log(4) \cong 6\,dB \tag{2.41}$$

The result is that the two tone signal can represented the signals with PAPR lower than 6 dB (PAPR can be decreased by using a two tones unequal of unequal powers).

When the two-tone input signal is applied to the PA with second-order non-linearity the result is

$$\begin{aligned} x(t) =& A\cos(\omega_1 t) + B\cos(\omega_2 t) && (2.42)\\ y(t) =& K_1 x(t) + K_2 x^2(t) && (2.43)\\ y(t) =& K_1[A\cos(\omega_1 t) + B\cos(\omega_2 t)] + \\ & K_2[A\cos(\omega_1 t) + B\cos(\omega_2 t)]^2 && (2.44) \end{aligned}$$

the second (quadratic) term can be expanded to

$$\begin{aligned} y(t) =& K_2\left[A^2\cos^2(\omega_1 t) + 2AB\cos(\omega_1 t)\cos(\omega_2 t) + B^2\cos^2(\omega_2 t)\right] \\ =& K_2\Bigg[A^2\left(\frac{1}{2} + \frac{\cos(2\omega_1 t)}{2}\right) + B^2\left(\frac{1}{2} + \frac{\cos(2\omega_2 t)}{2}\right) + \\ & ABcos(\omega_1 t \pm \omega_2 t)\Bigg] \end{aligned} \tag{2.45}$$

It can be seen that the output contains the two original tones, second harmonics and two additional tones at frequencies $f_1 \pm f_2$. These two additional tones are called second-order intermodulation products. These two tones are quite far away from the band of interest and therefore can be easily filtered.

The PA with third-order non-linearity will produce at the output these six additional

tones compared to the previous case

$$\begin{aligned} f_{IM3a} &= 3f_1 \\ f_{IM3b} &= 3f_2 \\ f_{IM3c} &= 2f_1 + f_2 \\ f_{IM3d} &= f_1 + 2f_2 \\ f_{IM3e} &= 2f_1 - f_2 \\ f_{IM3f} &= f_1 - 2f_2 \end{aligned} \tag{2.46}$$

where the tones at frequencies $2f_1 \pm f_2$ and $f_1 \pm 2f_2$ will fall usually very close to the signal band of the PA and it is difficult to filter them out. They are called third-order intermodulation products (IMD3).

In general, the n-th order intermodulation components can be calculated according to

$$f_{IM} = \sum_{a=0}^{n} af_1 \pm (n-a)f_2 \tag{2.47}$$

The outcome of the two-tone excitation is that additional tones are generated in addition to the DC and harmonics generated by an single-tone excitation. The odd-order intermodulation distortion products (especially third-order and fifth-order) fall very close to the signal band (adjacent and alternate bands) and can not be easy filtered out and they cause a distortion which leads to noncompliance with the non-linearity requirements imposed by a specific telecommunication standard.

The second-order and third-order distortion products are produced by the second-order and third-order terms in the PA transfer characteristic. Notice that the power of these terms is quadratically and cubically increasing with the input power (the fundamental term increases linearly). With increasing the input power, there would be a point where the power in the fundamental component is equal to the power in the harmonic distortion product. This point is called the intercept point. As mentioned above, the third-order distortion is usually the most significant distortion in the PA and the third-order intercept point (IP3) is an important non-linearity indicator of the PA. The IP3 refers either to the input power (IIP3) or the output power (OIP3).

The concept of the IP3 is shown in Fig. 2.13. The power of the IMD3 components increases by 3 dB per each 1 dB increase in the input power. The point where the fundamental and IMD3 power plots meet is called IP3 (this point is based on extrapolation of both IMD3 and fundamental power curves and can not be practically reached and measured).

It can be shown that [Sechi & Bujatti 2009]

$$P_{IIP3}\,[dBm] = P_{out,-1dB} + 9.6 \tag{2.48}$$

$$P_{OIP3}\,[dBm] = P_{out,-1dB} + 10.6 \tag{2.49}$$

where $P_{out,-1dB}$ is the single-tone output power at 1 dB compression point.

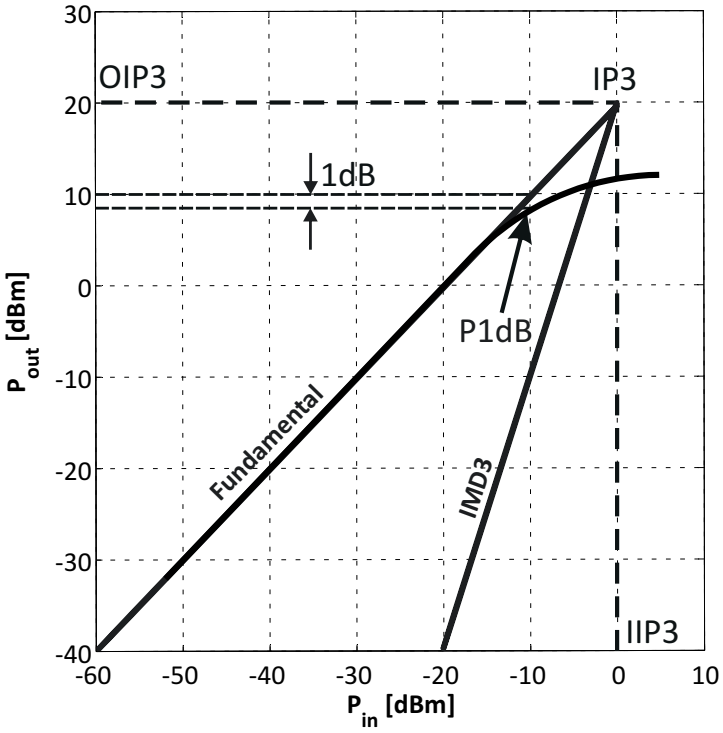


Figure 2.13: Third-order intercept point and 1 dB compression point definition.

The IP3 can be calculated as [Rogers & Plett 2003]

$$OIP3\,[dBm] = P_{in} + \frac{1}{2}(P_{out,fund} - P_{out,IM3}) \tag{2.50}$$

$$IIP3\,[dBm] = OIP3 - G \tag{2.51}$$

It can be seen from Fig. 2.13 that for each 1 dB power drop the IM3 drops by 2 dB. Note that the IM3 at the compression point is -20 dBc.

The carrier to intermodulation ratio (C/I) is defined as the ratio between the useful power and IMD products. This can be written mathematically as

$$C/I\,[dBc] = 10\log\frac{P_{f_{n(m)}}}{P_{2f_{n(m)}-f_{m(n)}}} \qquad n,m = 1,2 \tag{2.52}$$

$$C/I\,[dBc] = 2(OIP3 - P_{out}) = 2(IIP3 - P_{in}) \tag{2.53}$$

where P_{out} and P_{in} are the output and input power of each single tone in a two-tone signal.

The drawback of the IP3 as a non-linearity indicator is that it will not predict the non-linearity of amplitude modulated signals which are using a complex modulation. The two-tone measurement is very convenient but such a simple signal does not model

the actual operation of the PA using typical modulated signals (QPSK, OFDM etc.) accurately because it has different signal statistics.

Note that the IP3 concept can not be used in switch mode PAs. As it is shown in the next chapter (Section 3.3) the power of the switch-mode PAs is adjusted by the supply voltage and not by the input power as it is in transconductance PAs. The switch-mode PA should be always driven with a high enough input power so that the power transistor operates as a switch. Therefore, the IP3 characterization which is based on the sweeping of the input power of the two-tone signal is not valid for switching PAs.

2.3.4.3 ACLR

The adjacent channel power leakage ratio (ACLR) is defined as a ratio of the power that is contained in the adjacent channel to the power in the channel band. The signal band, the adjacent band and allowed ACLR limit has to be specified by the standard. Some standards (GSM/EDGE) do not specify ACLR but uses the spectrum mask where the transmitted output power spectrum has to be confined below certain limit.

The single-tone or two-tone measurement techniques can be used to investigate the PA non-linearity in a narrowband system. They can be used to emulate selected properties of the multicarrier input signals (PAPR) but the commonly used modulated signals in mobile networks might highly deviate from them. Therefore, ACLR was introduced for band-limited input signals. The main advantage of the ACLR method is that it uses real modulated signals and hence it provides the useful information about the signal distortion and the spectral regrowth. The ACLR can be calculated as

$$ACLR\,[dBc] = 10\log\frac{\int\limits_{LB\ or\ HB} P_{out}(f)\,df}{\int\limits_{band} P_{out}(f)\,df} \tag{2.54}$$

where LB and HB are lower adjacent band and higher adjacent band respectively. The ACLR can be calculated separately for the upper or lower adjacent bands but it can be also expresses as total ACLR where the power in both adjacent bands is considered. The alternate channel power leakage ration (ACLR2), is defined for the alternate channels.

The ACLR can be combined with previous non-linearity characterization methods. For example the ACLR is directly related to the third-order IMD products.

2.3.4.4 EVM

The error vector magnitude (EVM) characterizes the deviation of the received (demodulated) signal due to the non-linearity of the PA. It is defined as the magnitude of the error vector between the ideal constellation points and the received symbols constellation points. The EVM characterizes the in-band distortion (modulation fidelity) of the PA.

Chapter 3

Linear transmitters using switch-mode PAs

Contents

In this chapter transmitter topologies capable of transmitting varying envelope signal using switch-mode PAs are discussed. The focus on the switch-mode PAs is mainly due to their potential for high efficiency and integration in the CMOS technology. These PAs are naturally suitable to amplify constant envelope signals, as explained in the previous chapter. To employ switch-mode PAs in the RF transmitters using varying amplitude signals requires a linearization. There are three main approaches to accomplish that: Linear amplification with Non-linear Components (LINC), Pulse Width and Pulse Position Modulation (PWPPM), and polar transmitters. The first two techniques are introduced in this work only briefly as a background for the polar transmitter.

The polar transmitters are described and analyzed in more detail. The requirements on the PA are discussed. The chapter is concluded with two state-of-the-art examples of polar PAs.

3.1 LINC

LINC technique was originally introduced by Chireix in the 30's [Chireix 1935] and therefore it is sometimes referred to as Chireix amplifier. The concept of LINC amplifier is illustrated in Fig. 3.1

The basic idea of this concept is that a generic RF band pass signal, which can be defined as

$$RF_{in} = A(t)\cos(\omega_c t + \varphi(t)) = A\cos(\phi(t))\cos(\omega_c t + \varphi(t)) \tag{3.1}$$

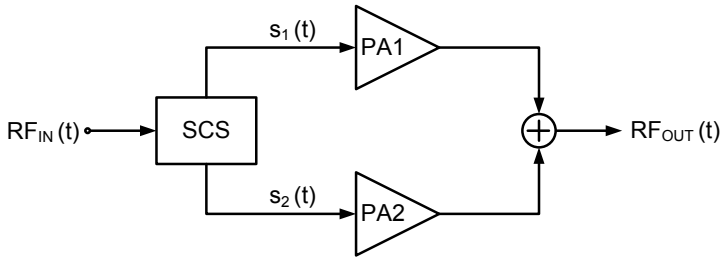


Figure 3.1: Block diagram of the LINC transmitter.

is applied to the input of the signal component separator (SCS) block. A is the maximum amplitude of the amplitude modulated signal $A(t)$. The SCS block performs the amplitude to phase modulation. The varying amplitude and phase RF input signal is converted into the two constant envelope and phase modulated signals. This process can be described as

$$\begin{aligned} RF_{in} &= s_1(t) + s_2(t) \\ &= \frac{1}{2}A\cos(\omega_c t + \varphi(t) + \phi(t)) + \frac{1}{2}A\cos(\omega_c t + \varphi(t) - \phi(t)) \end{aligned} \tag{3.2}$$

where

$$\phi(t) = \cos^{-1}\left(\frac{A(t)}{A}\right) \tag{3.3}$$

The two signals $s_1(t)$ and $s_2(t)$ can be then amplified by a highly efficient but nonlinear switch-mode PAs (PA1 and PA2 in Fig. 3.1). The output signal can be simply written as

$$RF_{out} = G(s_1(t) + s_2(t)) = 2GA(t)\cos(\omega_c t + \varphi(t)) \tag{3.4}$$

where G is the power gain of each power amplifier.

This concept is indeed very appealing and the LINC transmitter would exhibit both a high efficiency and a high linearity. Unfortunately, there are several important difficulties (practical challenges) which prevent the implementation of such transmitters without a severe deterioration of the performance (especially efficiency).

The first issue arises with $s_1(t)$ and $s_2(t)$ signals generation. The SCS block performs the signal separation according to the equation (3.2). This operation is quite complex because the phase of the original signal RF_{in} has to be modulated by $\phi(t)$ which is a non-linear function of the amplitude modulated signal $A(t)$ (3.3). The first SCS circuits were implemented on the circuit level but the circuits are very complex and not suitable for RF integrated transmitters [Cox & Leck 1975].

Another approach is to use the power of today's DSP chips. The schematic of a modern LINC transmitter is shown in Fig. 3.2.

The SCS function is performed in the baseband by the DSP and then each IQ signals

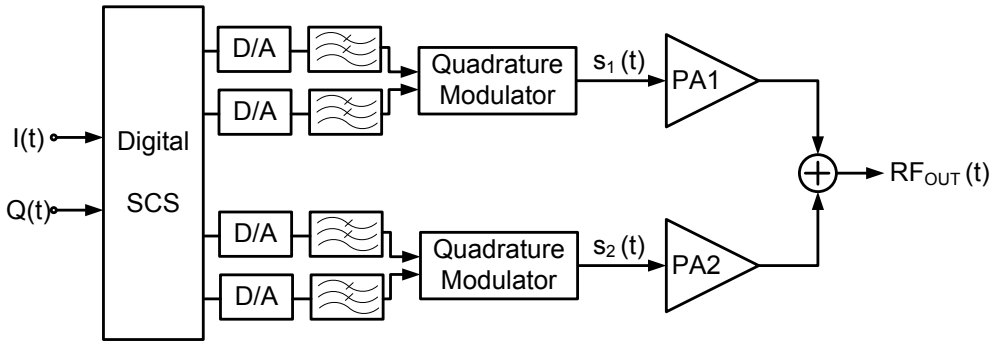


Figure 3.2: Block diagram of the LINC transmitter with SCS function implemented in baseband by the DSP.

are up converted to the RF and applied to the switch-mode PAs [Hakala *et al.* 2005]. The DSP and D/A converters have to operate at a high sampling rate and that will significantly increase the power consumption. The main problem of this approach is that the signal separation is a non-linear operation (3.3) which will create a bandwidth regrowth. The bandwidth of the two BB signals is much larger that the bandwidth of the original amplitude and phase modulated BB signal. Depending on the BB BW of the original signal the required BW might be at the edge of the capabilities of the best today DSPs. This approach (without a BW reduction technique) will not be feasible to implement in the mobile station transmitters.

Another difficulty is to maintain the mismatch between the two signal paths low. The amplifiers and quadrature modulators in the two channels need to have a precisely matched gain and phase response. Several complex methods have been proposed to correct either the gain or the phase errors or both. A summary of the linearization techniques can be found in [Vankka 2005]. A fully digital predistortion technique can be also used to compensate the gain and phase impairments [Garcia *et al.* 2005].

And the last but very significant issue of the LINC transmitter is the efficient power combining [Cripps 2006]. The requirements on the power combiner are that it should have low loss and high isolation between the two PAs. A conventional hybrid combiner can be used to combine the two signals. It provides a high isolation but the major disadvantage is a high loss if the two signals are not equal (uncorrelated signals have loss of 3 dB). A more efficient combining technique suitable for the LINC transmitters is required.

All of the above mentioned issues will lead to significant efficiency degradation. This is the main reason why the LINC transmitters are so popular among researchers. LINC offers an interesting research challenges, but it has not been implemented in the commercial mobile RF transmitters.

3.2 Pulse width and pulse position modulation

Pulse width modulation (PWM) is a recently re-discovered approach which encodes the envelope modulated signal into the pulse width so that it can be processed by a switch-

mode PA. The RF PWM was firstly demonstrated by Raab [Raab 1973]. A modern RF transmitter using the PWM concept is shown in Fig. 3.3.

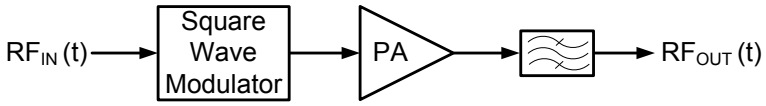


Figure 3.3: Simplified block diagram of the RF transmitter using PWM.

In the pulse width and pulse position modulation (PWPPM) one pulse is transmitted during each RF period. The RF input signal can be described by equation (3.1) where $A(t)$ and $\Phi(t)$ are the amplitude and phase varying signals respectively. The pulse width of the PWPM signal is related to the $A(t)$ signal and pulse position depends the $\Phi(t)$ signal. In this way the amplitude and phase modulated signal is transformed into constant envelope PWPPM signal.

The pulse modulated signals allow to use high efficient switch-mode amplifiers to amplify varying envelope signals. There are several techniques to create the pulse modulated signals. The first approach is using the sigma delta ($\Sigma\Delta$) modulation [Hung *et al.* 2007]. Hung et al. proposed a technique where the bandpass $\Sigma\Delta$ is fully implemented in the DSP. The transmitter is using a CMOS class-D PA operating at 800 MHz. This approach increases the flexibility of the system, avoids the problems associated with many analog circuits and can be easily implemented in a mobile handset RF transceiver. The modulated IQ BB signals are up-converted (in DSP) and processed by the bandpass sigma delta modulator. The main problem of this approach is the quantization noise which is a common issue for all the pulse modulation concepts which are using $\Sigma\Delta$ modulator. Even though the quantization noise is spectrally shaped into out of the band frequencies it is still difficult to meet the spectral emission mask. The bandpass filter at the output of the PA is required but the feasibility of its implementation was not investigated in [Hung *et al.* 2007].

A different approach was presented in [Nielsen & Larsen 2008]. The proposed pulse width modulator is operating at 2 GHz and is implemented in GaAs HBT process. It uses a low-frequency feedback together with the predistortion to linearize the output signal. This concept has three main drawbacks: a potential in-stability due to the feedback, the DSP need to have a high sampling rate and high signal BW (the amplitude and phase signals have much wider BW than the complex IQ signal) and the predistortion is needed.

Another technique was published by Walling et al. in [Walling *et al.* 2009]. Here the authors proposed to combine the PWPPM concept with the LINC technique. The transmitter is using a CMOS class-E PA operating at the frequency of 2.2 GHz. Firstly the signal is processed by the LINC modulator. Instead of a hybrid power combiner as in the conventional LINC transmitter the proposed technique is employing a PWM power combiner. The measured peak PAE is only 28.5 % and therefore it is not obvious if the PWM combining technique will lead to a higher PAE than using a hybrid power combiner. This technique has several major weak points. Specifically a high complexity of the transmitter, bandwidth regrowth and high sampling rate of the signal component

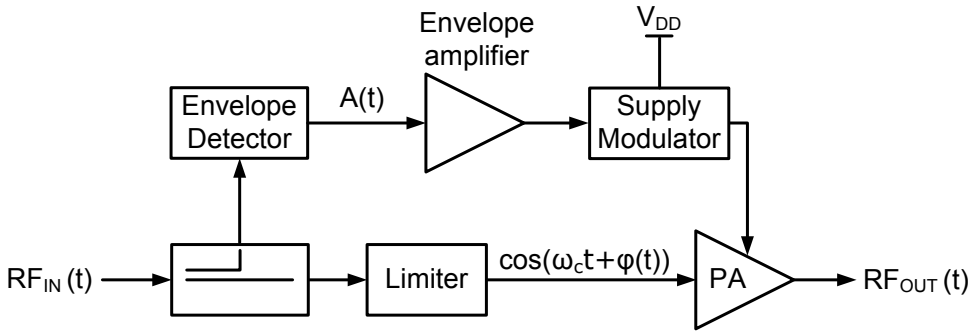


Figure 3.4: EER RF transmitter.

separator block in the LINC modulator and that PWPPM requires a linearization.

Generally, the pulse width and pulse position modulators seems attractive because the efficiency of such a transmitter can theoretically reach 100 %. The main drawbacks are a high quantization noise of $\Sigma\Delta$ topologies, high sampling rate and high signal BW requirements of the DSP implementations.

There is one more thing which should be addressed in the PWPPM transmitters and that is the selection of the PA topology. Usually the PWPPM transmitters are not using a class-E PAs and there is a good reason for this. The output signal of the pulse width and pulse position modulator is a non-periodic signal. The concept of the class-E PA is based on the zero voltage switching and zero voltage derivative switching conditions (Section 2.2.2). These condition can be fulfilled for a periodic input stimuli and hence the class-E PA would not achieve a high efficiency when it is driven by a PWPPM signal [Hung *et al.* 2007]. The work published in [Walling *et al.* 2009] is using a class-E PA and the authors justify this by a simple analysis of the class-E operation under the different duty cycle ratios. Indeed the AM modulation will cause the variation of the duty cycle but what is not investigated is that the phase modulation leads to a different timing of the pulses and this cause the non-periodicity of the signal. The behavior of the class-E PA should be investigated under both of these conditions.

3.3 Polar transmitters

The polar transmitters are based on the Envelope Elimination and Restoration (EER) technique or sometimes it is also referred to as Kahn technique [Kahn 1952]. In generally, the EER technique allows to combine both high efficiency and linearity assuming a highly efficient PA and amplitude modulator is used. Originally, this technique was intended for the amplification of the single sideband (SSB) modulated signals. The basic concept of the EER technique is showed in Fig. 3.4.

The EER technique is exploiting the principle that the amplitude and phase modulated band limited input signal (in Cartesian form)

$$RF_{in} = A(t)\cos(\omega_c t + \varphi(t)) = I(t)\cos(\omega_c t) + Q(t)\sin(\omega_c t) \tag{3.5}$$

can be decomposed to varying envelope signal and constant envelope phase modulated signal (polar form) according to

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{3.6}$$

$$\varphi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right) \tag{3.7}$$

where $A(t)$ and $\varphi(t)$ are the amplitude modulated signal and phase modulated signal respectively. Note that the mathematical operations described in 3.6 and 3.7 are non-linear. This is the reason for the bandwidth expansion of both amplitude and phase modulated signals compared to the bandwidth of the complex input signal RF_{in}.

The input signal in the EER transmitter is a RF phase and envelope modulated signal. Firstly, the envelope of the signal is separated using a directional coupler and an envelope detector. The constant envelope phase modulated signal is obtained from the input signal using the limiter circuit. This signal can be directly applied to the input of the switch-mode PA. The envelope path is bit more complex. After the varying envelope signal is extracted from the RF input signal, it has to be amplified and its level has to be adjusted. This signal is then applied to the power controller which will modulate the supply voltage of the PA (in some literate it is referred as a drain modulation). The output from the envelope amplifier can not be used directly to control the supply voltage of the PA simply because the PA has high current driving requirements which can not be easily met using an arbitrary voltage amplifier. The power controller can be implemented as a DC/DC converter, low voltage drop-out regulator (LDO), sigma delta converter or for example a generic high power switched amplifier (class-S).

The EER transmitter is exploiting that the output power of the saturated PA is directly related to the supply according to

$$P_{out} = \frac{1}{2}\frac{V_{out}^2}{R_L} = K\frac{V_{dd}^2}{R_L} \tag{3.8}$$

where K is a constant which value depends on the PA class of operation ($K = 2/\pi^2$ in class-D amplifier and $K = 8/(\pi^2 + 4)$ in class-E amplifier). It can be seen that the relation of the V_{out} on V_{dd} is linear and can be expressed as

$$V_{out} = \sqrt{2K}V_{dd} \tag{3.9}$$

Therefore, the EER transmitter can be used to linearize the switch-mode PAs so they can efficiently and linearly amplify the amplitude and phase modulated signals. It is important to note that the efficiency remains constant when the supply voltage is reduced. Hence, the EER transmitter can theoretically achieve 100 % efficiency for the whole AM dynamic range and the output power level range.

The present EER transmitters differ significantly from the original concept. The advancement in the DSP technologies allowed to implement a large part of the concept directly in the digital domain. Modern EER transmitters are usually referred to as the

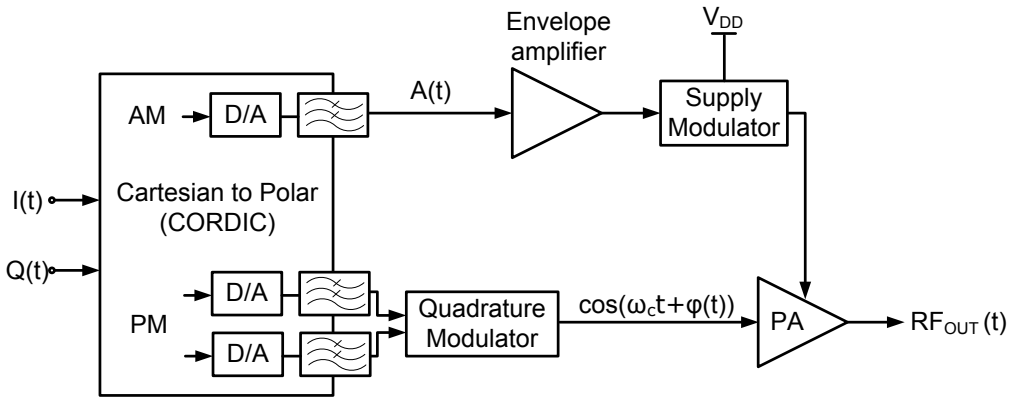


Figure 3.5: The basic architecture of the polar RF transmitter.

Polar Transmitters (Polar TX). The basic topology of the polar RF transmitter is shown in Fig. 3.5.

It can be seen that the input signal is a modulated BB signal (not the RF signal as in the original concept) which is fully processed in the digital domain. The envelope and phase separation is usually done in the DSP by the COordinate Rotation DIgital Computer (CORDIC) algorithm. Hence, the envelope detector in the original topology can be omitted. There is no need for the amplitude limiter in the phase path neither because the phase modulated signal is be directly outputted from the DSP as a constant envelope signal. The phase modulated signal is then up converted by the quadrature modulator to the desired RF carrier frequency and applied to the switch-mode PA. The envelope path contains the envelope amplifier and a supply modulator (DC/DC converter).

One of the most critical blocks in the polar transmitter is the supply power modulator. There are various suitable topologies (among others LDO regulator, DC/DC converter and PWM modulator). In general, there is a trade-off between a high efficiency (of switching DC/DC converters) and high linearity (LDO regulator). The overall efficiency of the polar TX can be calculated according to

$$\eta_{(total)} = \eta_{(PA)} \cdot \eta_{(power\ modulator)} \tag{3.10}$$

where it is assumed that the output power is so high that the consumption of the other polar TX blocks is negligible. It can be seen that if for example PA has the peak efficiency of 60 % and the power supply modulator 90 % the total efficiency is 54 %. If it is assumed that the PA is operated always in the saturation then the overall efficiency as a function of the input power depends mostly on the efficiency of the power supply modulator. Usually the efficiency of the switching modulators drops drastically when the modulator is delivering a low output power [Kitchen *et al.* 2007].

There are several main challenges in the polar transmitters and mostly all of them are related to the linearity. The first is the delay between the amplitude and phase paths. The polar transmitter requires a very precise timing and ideally the both, amplitude

and phase signals, are synchronized at the inputs of the PA. This is difficult to achieve without an additional delay adjustment because usually the delay in the phase path (mainly due to up-conversion) and the amplitude path (caused by the envelope amplifier and the power controller) are different. Therefore, the delay has to be adjusted either in digital domain after the amplitude and the phase separation or manually either in phase or amplitude path. The allowable differential delay depends on the bandwidth of the complex input signal (the larger the BW of the input signal is, the smaller delay is allowed). For example the single carrier WCDMA signal requires the differential delay between the amplitude and phase paths below 15 ns. The rule of thumb is that the differential delay has to be lower than

$$delay \leq \frac{1}{20}\frac{1}{BW_{RF}} \tag{3.11}$$

where the BW_{RF} is the signal BW of the modulated complex output signal. In the paper [Talonen & Lindfors 2005] the authors came to the conclusion the maximum acceptable delay mismatch between the amplitude and phase paths for IEEE 802.11a OFDM modulated signal is 3 ns (the BW of the complex input signal is 16.6 MHz).

The differential delay deteriorates the linearity of the RF transmitter. The effect of the differential delay on the IMD was studied in [Raab 1996] using a two-tone test. It is shown that for the small delays the magnitude of the IMD products can be calculated according to

$$IMD = \frac{2}{\pi}\tau^2 \tag{3.12}$$

where τ is the differential delay in radians. Note that the amplitude of the intermodulation distortion products specified by the equation 3.12 is a voltage related parameter. The τ can be written as

$$\tau = \pi \Delta t BW_{RF} \tag{3.13}$$

where Δt is the differential delay in seconds. The C/I ratio can be therefore expressed as [Raab 1996]

$$\begin{aligned} C/I[dB] &= 20\log\left(\frac{2}{IMD}\right) = 20\log\left(\frac{\pi}{\tau^2}\right) = 20\log\left[\frac{\pi}{(\pi\Delta t BW_{RF})^2}\right] = \\ &= 20\log\left[\frac{1}{\pi(\Delta t BW_{RF})^2}\right] \end{aligned} \tag{3.14}$$

where the C/I ratio is defined with respect to an un-modulated carrier (amplitude of unity). The modulated carrier signal have two spectral components of 1/2 amplitude. The equation 3.14 is plotted in Fig. 3.6. The simulated C/I ratio versus the differential delay using the EDGE and WCDMA signals is shown in Fig. 3.7(a) and Fig. 3.7(b) respectively. The EDGE has modulation bandwidth of 200 kHz and the WCDMA has modulation bandwidth of 3.84 MHz. It can be seen that the 50 dBc C/I ratio would

require the differential delay below 150 ns and 8 ns for the EDGE and WCDMA input signals respectively. As it was discussed in the previous chapter, the carrier to intermodulation ratio can not fully characterize the linearity of a modern complex modulated signals but it can provide a useful guide in a first approximation.

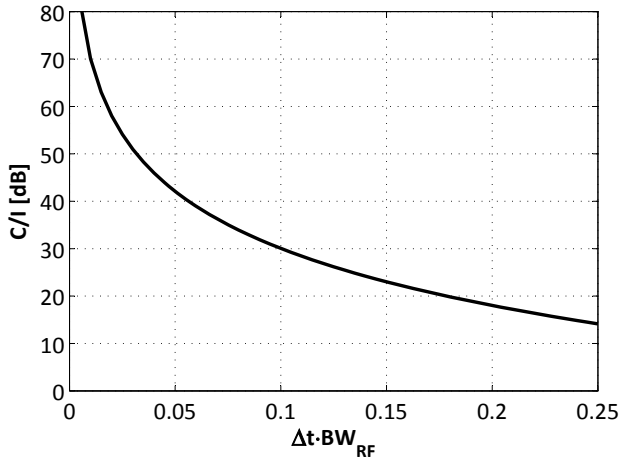
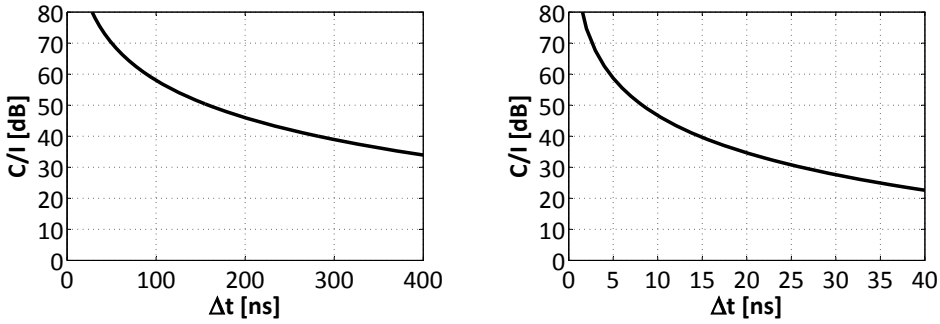


Figure 3.6: The carrier to intermodulation ration (C/I) of a two-tone signal as a function of the differential delay constant.



(a) EDGE (b) WCDMA

Figure 3.7: Simulated C/I ratio versus differential time delay of (a) EDGE and (b) WCDMA signals.

Another drawback of the polar transmitter is the bandwidth regrowth of both, the amplitude and phase signals. This is a common problem of all transmitters which are using Cartesian to polar conversion (for example LINC). As was mentioned before the amplitude and phase separation is a nonlinear operation (see equations 3.6 and 3.7) and this will cause the bandwidth regrowth in the frequency domain. Usually, it is difficult to estimate the BW of amplitude and phase signals because the roll-off is quite slow (Fig. 3.9). The required BW is usually calculated (or simulated) in order to meet a given ACLR or EVM. If the BW in the amplitude or phase path is below required limit than the linearity of the polar transmitter is deteriorated and the transmitted signal

might not meet the specification. Various studies provide a different numbers of the BW regrowth [Talonen & Lindfors 2005, Vankka 2005] but usually the rule of thumb is that the BW of the AM and PM signals is 3-6 times larger than the BW of the complex input signal. The study of envelope BW on the C/I ratio using a two-tone test can be found in [Raab 1996]. The fully analytical solution is not available but the author provided there a table with C/I ratio as a function of the envelope BW (BW_E). This data from the table is shown in the graphical form in Fig. 3.8. It can be seen that the 50 dBc C/I ration requires that the envelope bandwidth BW_E is 6 times larger than the RF bandwidth (BW_{RF}).

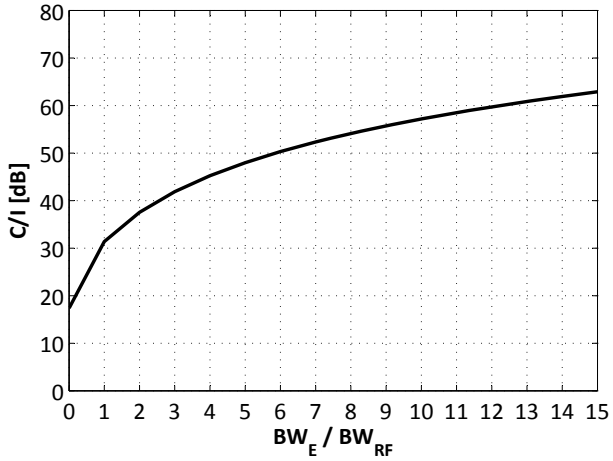


Figure 3.8: The carrier to intermodulation ratio (C/I) of a two-tone signal as a function of the envelope (BW_E) to RF signal BW_{RF} bandwidth [Raab 1996].

In [Talonen & Lindfors 2005] it is concluded that the amplitude and phase BW has to be at least 35 MHz and 50 MHz respectively to meet the 2 % EVM and transmit mask requirements of the IEEE 802.11a standard. Note that the phase signal requires a higher BW than the amplitude one. This imposes strong requirements on both the envelope and phase paths circuits. For example if the complex input signal has BW of 3.84 MHz (WCDMA signal) than the phase and amplitude BW is 12 MHz - 23 MHz. It is very challenging if not impossible with nowadays technology to design a switching power converter which can process signals with such a high BW [Kitchen *et al.* 2007]. This will limit the polar transmitter application only to a certain modulation standards with a low signal BW.

Another issue of the polar topology is the amplitude and phase distortion (AM-AM and AM-PM). The drain modulation of the PA is not ideally linear as it may look from the basic and simple equations. If the supply voltage drops very low, the switching transistor can be pushed from triode to saturation region and the AM-AM characteristic will become more nonlinear. It is very difficult to obtain a sufficiently linear transfer characteristic of the PA in the full amplitude variation range and output power control range [Sowlati *et al.* 2004]. Furthermore, the parasitic capacitances of the active device are voltage dependent and therefore varying the supply voltage causes

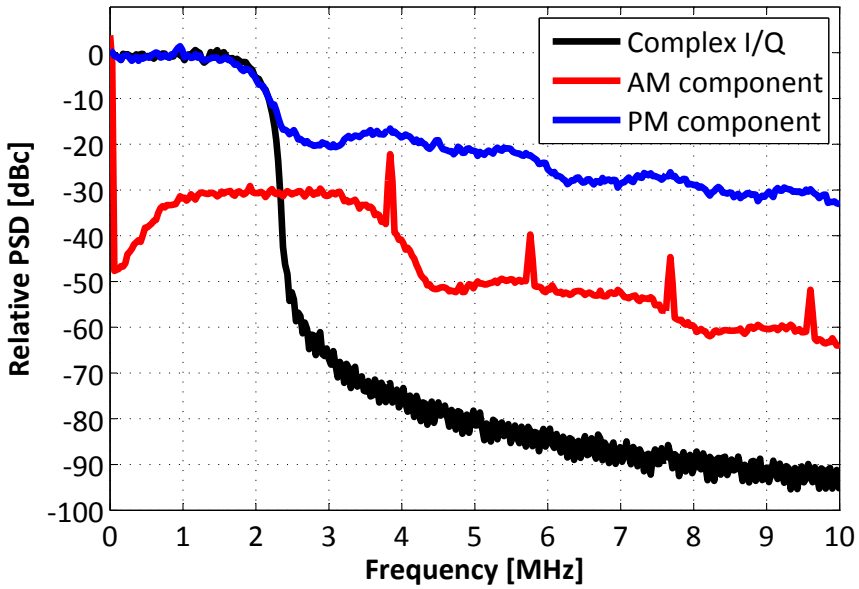


Figure 3.9: The spectrum of the WCDMA signal. The spectrum of the complex signal (black), the spectrum of the amplitude (red) and phase (blue) components.

the AM-PM distortion. Hence, the linearization of the polar transmitter is usually required (very common is the digital predistortion linearization). The AM-AM and AM-PM predistortion is usually using thousands of data points in the look-up tables for the digital predistortion (for different output power level, bias level, temperature or technological variation) [Cripps 2006].

Even though the polar transmitter can achieve ideally 100 % efficiency the overall efficiency will be much lower mainly because the finite efficiency of the power modulator and the power loss in the PA driver. The latter one is the main cause why the switch-mode PAs don't exhibit 100 % efficiency nor practically neither in theory. The efficiency would be significantly increased if the supply voltage (DC power consumption) of the driver is decreased with the decreasing output power. This will cause an amplitude variation of the RF phase modulated signal. The drive supply voltage level shouldn't decrease too low otherwise the active device in the output stage will not act as a switch (because it will be not driven hard enough) and hence the efficiency will drop. The driver stage power adjustment can lead to a significant increase of the efficiency at the low output power levels what was demonstrated in [Raab 1999].

The polar transmitter can be also configured as a close-loop system. This architecture is called Polar Loop Transmitter and its topology is shown in Fig. 3.10.

This system is using a close-loop feedback in order to control both the phase and amplitude of the transmitted signal. The input signal of the polar loop TX is a complex modulated IF signal. The transmitter consists of a two loops: the amplitude and the phase loop. In each loop the input signal is compared with down converted output signal. In the phase loop, the output signal is compared with the input IF signal. The

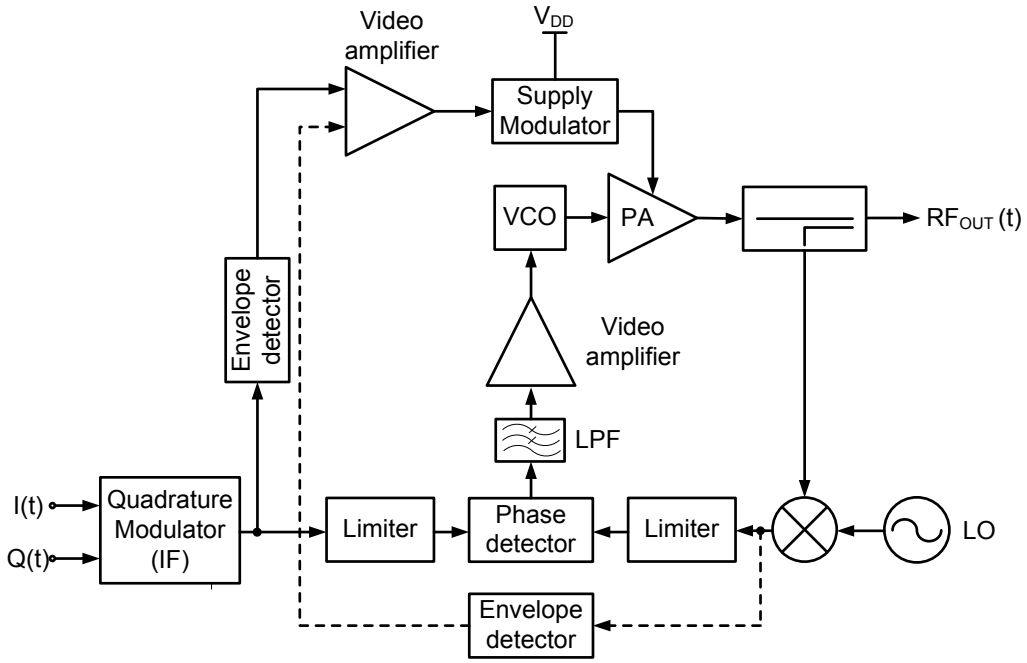


Figure 3.10: The topology of the polar loop transmitter.

output signal of the phase locked loop (PLL) corresponds to the error signal between the output and input phase modulated signal. This signal controls a VCO which feeds directly the PA. Note that the VCO is part of the feedback loop. The amplitude loop works in similar way. The amplitude of output and input signals are compared and the error signal from the output of the comparator controls the gain of the PA by varying the PA supply voltage.

The main advantage of this topology is that the problems with AM-AM and AM-PM distortion are eliminated. By using the feedback topology the AM-AM and AM-PM nonlinearities can be corrected on-the-fly and no digital predistortion (or other linearization) technique is needed. The feedback linearization will work for all temperatures, bias voltages, supply voltages and will fully cover the technology process variations. Hence, the extensive and rather cumbersome individual calibration and characterization which is used in the digital predistortion is avoided. Generally, the polar loop feedback system is capable to fully correct the non-linearity of the RF transmitter. Great advantage is also that the polar loop TX does not need a pre-PA or post-PA filtering to meet TX noise in RX band [Sowlati *et al.* 2004]. Generally, the output power dynamic range would be significantly limited by the linear range of the envelope detectors. But it was shown that using a variable gain amplifiers in the envelope loop the output power control range can be much higher compared to the open-loop polar TX (65 dB linear power control range including amplitude modulation was reported in [Sowlati *et al.* 2004]).

The polar loop TX has also several associated issues. The amplitude and phase paths have the same bandwidth regrowth as the above mentioned open-loop polar TX. Therefore, the video amplifiers (Fig. 3.10) in both loops need to have a sufficient BW

which is rather large in the recent mobile standards (for example 20 MHz channel RF BW in WiMAX or LTE). Furthermore, the stability of the video amplifiers and generally of the both loops proposes a serious design issue and limitation. The polar loop TX is also very sensitive to a noise, because there is no external filter at the output of the PA.

3.3.1 Polar PAs

In this subsection selected novel and innovative approaches in the polar PAs are briefly described. The term polar PA refers in this work to a PA that is intended for the polar transmitters.

There have been published several RF polar PAs. A polar PA using the class-D switching PA was published in [Cijvat & Sjoland 2008] but majority of the polar PAs is using a class-E PA [Reynaert & Steyaert 2005, Kitchen *et al.* 2007, Park *et al.* 2007]. Many works are implemented in the specialized RF technologies [Bakalski *et al.* 2008, Choi *et al.* 2009] technologies but there are also full CMOS polar PAs [Reynaert & Steyaert 2005, Park *et al.* 2007, Aoki *et al.* 2008]. The advantage of the specialized RF technologies like SiGe, GaAs, AlGaAs, InP and GaN over the CMOS is that they exhibit higher quality of the passive components, have higher power capability (current densities), have higher reliability (high voltage operation) and have generally better RF performance [Raab *et al.* 2003]. Their main disadvantages are the high costs and low integrability with the rest of transmitter front-end. The PA that is made using a specialized technology (for example GaAs) consists of several dies packaged into one module. Only the core of the PA is implemented in a specialized technology and the control circuitry is made in CMOS. Beside the IC dies the PA module contains also number of passive components.

From mobile standard perspective most of the polar PAs are targeting the EDGE or WCDMA standards. These standards have relatively low signal bandwidth what makes them a very suitable for the polar TX, though there were also published several WiMAX polar PAs [Shameli *et al.* 2008] but the maximum signal BW is usually only around 5 MHz.

Very often the polar PAs are designed together with a supply modulator. In some cases the supply modulator and PA are implemented in a different IC technologies [Hietala 2006, Choi *et al.* 2009].

An example of a typical conventional polar PA was published in [Reynaert & Steyaert 2005]. The PA is a three stage fully differential PA where the output stage operates as a class-E amplifier and the driver stages are class-D amplifiers. The amplitude modulator is implemented as low dropout (LDO) voltage regulator. The regulator is using PMOS transistor as the pass element. The class-E PA is using a single transistor output stage topology. This limits the reliability of the class-E PA (the reliability issues in class-E PAs are discussed in Chapter 5, Section 5.5.) In order to improve the reliability authors used a thick gate-oxide transistor in the class-E PA stage. The supply voltage of the amplitude modulator is 3.3 V and the average and peak values of the PA supply voltages are 1.9 V and 2.9 V respectively.

Though authors didn't discuss how they obtained the drain voltage peak reduction (the peak drain voltage is up to $3.56\,V_{DD}$ [Sokal & Sokal 1975]). It is also obvious that the supplied current has to be quite large in order to deliver the 23.8 dBm average output power to the load. The overall PAE (PA plus amplitude modulator) using the EDGE signal is 22 %.

The paper [Reynaert & Steyaert 2005] is to my knowledge the first published GSM/EDGE RF polar PA employing the class-E PA together with the amplitude modulator in the CMOS technology. The main drawbacks of the proposed solution are limited amplitude dynamic range and power control, distortion at low output power levels and rather low efficiency. Authors also claim they meet the EDGE E3 specification but the lowest average output power in the figures is approximately 10 mW and not 1 mW (0 dBm) as required by the standard. Furthermore, there is a high distortion at low output power levels (below 40 mW) and this is not discussed neither.

Nowadays the main challenges in the polar PAs are: the BW regrowth related issues (a supply modulator with a high BW), high dynamic range of the amplitude modulated signal and high output power control range, linearization, high efficiency at power back-off and reliability.

There have been published several polar PAs but only a few of them are indeed innovative, practical and feasible for the real applications. Two examples of the recent pioneering work are presented in the following two subsections. Both topologies utilize a special amplitude modulation technique of the polar PA (not the conventional supply modulation) and neither of them operates as a typical PA (class-E or class-D etc.).

3.3.2 Two point modulation

The topology of the polar PA proposed by Shameli et al. in [Shameli *et al.* 2008] is shown in Fig. 3.11. The authors of this paper refer to the method as "Two-Point Modulation".

As it can be seen from Fig. 3.11 the PA consists of a three segments where each segment is eight times larger (the transistors width is eight times larger) than the previous one. The amplitude modulated signal is applied to the common source transistors and the phase modulated signal (LO) is applied to the common gate transistors. The whole topology look similar to a single balanced mixer.

The amplitude modulated signal (AM) controls the tail current of the common source transistors which act as the current sources. The power control is employed by the binary weighted digital to analog converter which is controlled by the digital word $[B_6...B_0]$. The amplitude modulation and power control are separated. The authors claim that the amplitude modulation employed by the tail current modulation is fast and suitable for wideband applications. The 3 dB bandwidth is 17.1 MHz at the maximum output power level.

The digital control word which sets the output power level is applied to the sigma-delta supply modulator. This is done in order to improve the PAE of the polar PA. Because this signal contains only the power control the switching frequency of the $\Sigma\Delta$ can be low. The output power control capabilities are demonstrated in Fig. 3.12.

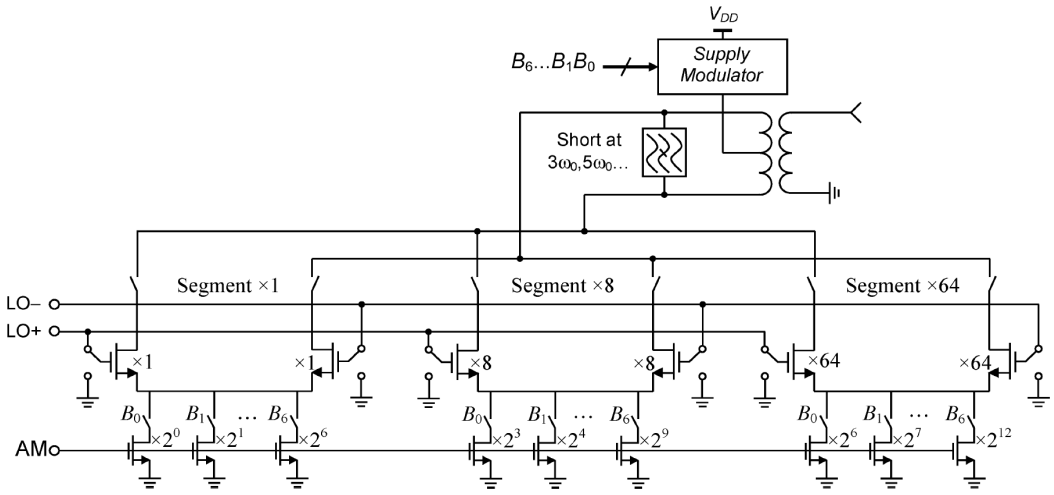


Figure 3.11: Switch-mode PA using the two-point modulation technique proposed in [Shameli *et al.* 2008].

The overall power control range is 62 dB, Both, the DC-DC converter and the PA are fabricated in CMOS technology. The PA is not operating in any class and the output transformer is used as impedance convertor and as a balun.

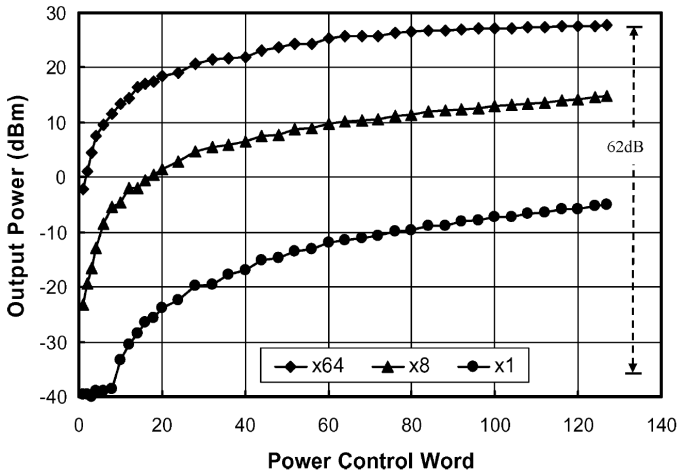


Figure 3.12: Measured output power as a function of the power control word for different PA segments [Shameli *et al.* 2008].

The proposed topology is rather complex (multiple control signals and multiple segments) where the power control signal is used to control both the power and the supply voltage. Furthermore, the output power range is controlled by alternatively switching the three PA segments ON and OFF. It was not explained in the paper how to implement this switching on the fly when for example EDGE or WCDMA signal is transmitted. The PA is also using several off-chip components including the output balun and the supply modulator. The amplitude bandwidth is definitely not sufficient for

the modern wideband standards (20 MHz LTE or WiMAX) even without considering the unavoidable bandwidth regrowth due to the Cartesian to polar conversion. The linearity was not investigated thoroughly (beside the two-tone test and 1 dB compression point measurement), especially ACLR and EVM measurements are missing. A high spectrum regrowth was observed at high output power levels even using the digital predistortion. The authors suggest to use another technique (for instance the polar loop feedback topology) to linearize the PA.

3.3.3 Digitally modulated polar PA

Another excellent work in the field of the polar PAs was published by Presti et al. in [Presti *et al.* 2009]. The topology of the PA is shown in Fig. 3.13

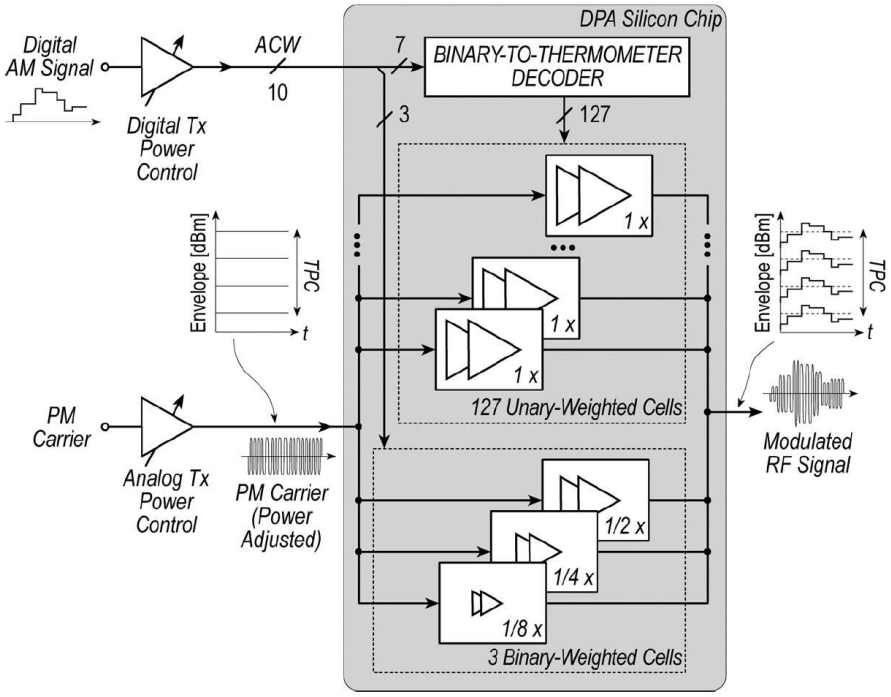


Figure 3.13: The topology of the digital modulated polar PA [Presti *et al.* 2009].

The digitally modulated power amplifier was presented as an alternative to the conventional power supply modulation technique. The AM signal is applied to the PA in the digital form as an amplitude code word (ACW). The PA consists of 127 unary weighted cells and 3 binary weighted cells. The cells are turned ON according to the ACW signal. The resolution of the ACW is 10 bits and it was chosen high enough to keep the quantization noise low. If the whole PA is made of the unary weighted cell it would require $2^{10} = 1024$ cells. That's too high and not feasible to implement. Only the 7 most significant bits are applied to the unary weighted cell. The rest 3 least significant bits are implemented by 3 binary weighted cells. This approach is a trade-off between the simplicity of the full binary approach and the superior matching performance of the

fully unary weighted cells design. Advantage of the digitally modulated polar PA is that there is no need for a wide bandwidth supply modulator as in is the conventional polar PA.

The power control is employed by both the amplitude code word and by the input power variation. The ACW can be decreased until only 6 bits are left when the ACLR limit is reached due to the quantization error. The output power can be further decreased by lowering the input power. The input power can be changed from -95 dBm up to 13 dBm. The input power variation is used solely for the power control and not the AM modulation.

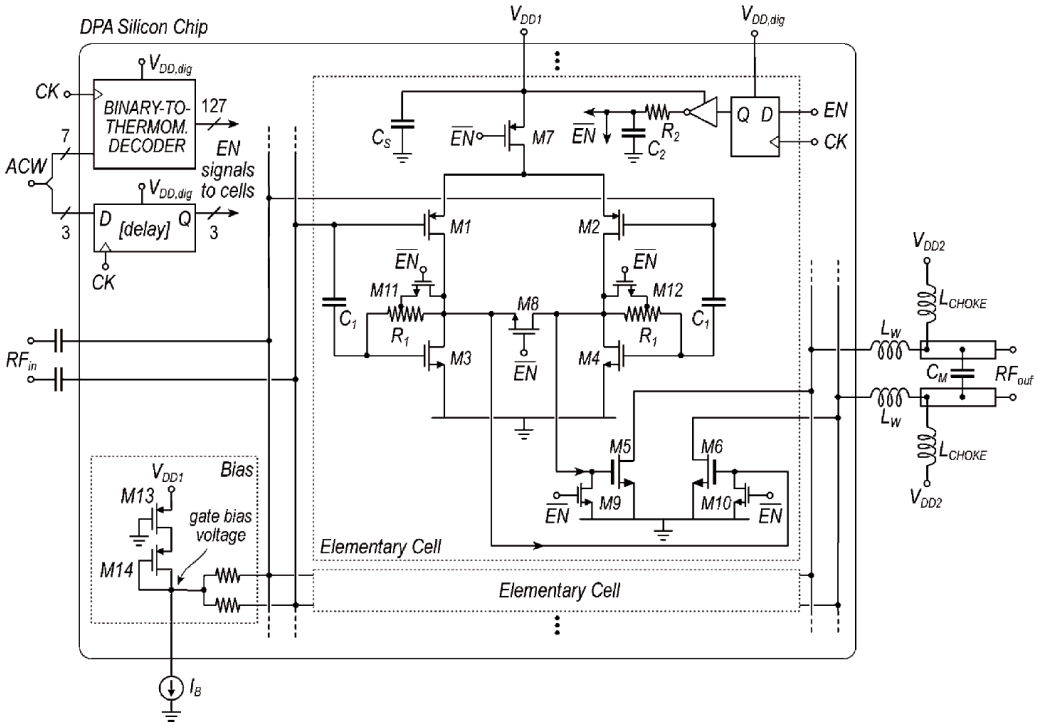


Figure 3.14: The schematic of the elementary gain cell of the digital modulated polar PA [Presti *et al.* 2009].

The digital PA itself is using a rather unique design approach and the PA doesn't fall into any conventional class of operation. The elementary cell is designed as a differential gain cell (see Fig. 3.14). The gain cell consists of a two stage amplifier. The first stage is a complementary common-emitter amplifier. The gain cell topology was optimized for a wideband operation (no interstage matching). The PA was fabricated in SOI CMOS process.

The output signal from the gain cell is a current and therefore the outputs of the individual gain cells can be directly sum together and no special power combining technique is needed. The output network is designed to operate the PA in the class-E like mode.

The main novelty of the work of Presti et al. is that it combines a fully digital AM signal modulation with adaptive input power control of the polar PA. The PA

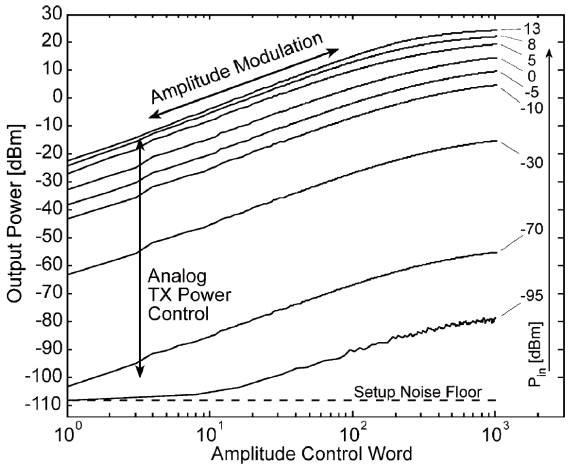


Figure 3.15: Output power versus amplitude code word at different input power values [Presti *et al.* 2009].

exhibits extremely high output power dynamic range of more than 110 dB. The power control range is more than 70 dB and the amplitude modulation dynamic range is more than 40 dB. The output power dynamic range is shown in Fig. 3.15. The PA exhibits a significant non-linear behavior and measured results were obtained using a digital predistortion. The digital predistortion was implemented by an adaptive feedback loop.

One of the main advantages of the digitally modulated polar PA [Presti *et al.* 2009] is a high average PAE. Usually the WCDMA PAs have very low average efficiency when the probability distribution of the output power is multiplied by the actual PAE. The digitally modulated PA concept exhibit much higher average efficiency than the conventional PAs because by decreasing the output power the unused gain cells in the PA are OFF and the overall quiescent current is decreased. Generally, the higher number of the cells is in the PA (that requires a higher resolution of the ACW) the better the overall efficiency will be. In [Presti *et al.* 2009] it is reported an average efficiency of 16.4 % for WCDMA modulated signal (PAPR = 3.4 dB). The PA was tested using EDGE, WCDMA and WiMAX signals.

The proposed PA in not fully integrated on-chip and several off-chip components are needed. The main drawback is the non-linearity of the PA. Furthermore, the input power control as it was presented can not be applied directly to a switch-mode PA. The switching PA requires a high driving signal to operate the active device as a switch and this was not considered in that work. The minimum required power level of the driving signal depends on various circuit parameters and it is a function of the supply voltage.

Chapter 4

Class-E PA

Contents

In this section the basic design procedure of the cascode class-E PA is described. The section starts with a detailed design description of a class-E PA. The cascode class-E PA performance is analyzed using simulations. A particular focus is put on the reliability analysis of the PA. Finally, the model of the cascode PA is proposed.

4.1 Class-E PA design

The simplified class-E circuit analysis that is given in this section will provide the insight on the circuit operation. The results of the analysis are the design equations that can be used to calculate the values of the class-E PA circuit elements.

The class-E PA was briefly introduced in Section 2.2.2. It was mentioned that the class-E PA should be designed in the time domain because the ideal performance is obtained by shaping the drain voltage and current of the active device. This has to be investigated by a time domain analysis. The basic circuit of a class-E amplifier is shown in Fig. 4.1.

Note that the series resonant circuit (SRC) is not tuned to the carrier frequency, but it has at this frequency a series reactance jX. This reactance can be simply expressed as

$$X = 2\pi f L_0 - \frac{1}{2\pi f C_0} \tag{4.1}$$

Usually the SRC is considered to be tuned to the carrier frequency with an additional reactance element in series.

The description of the circuit operation is based on these assumptions:

1. The transistor operates as an ideal switch. There is no series resistance and input/output capacitance associated with the active device.

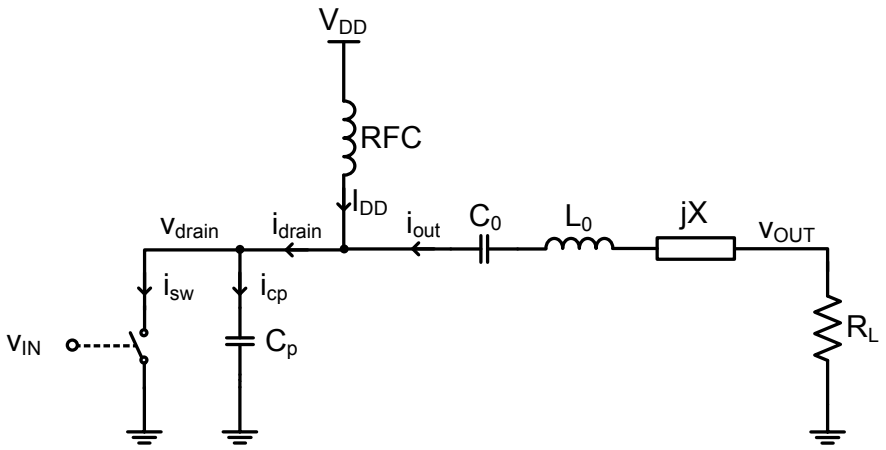


Figure 4.1: Simplified circuit of the class-E power amplifier.

2. The RF choke inductor (RFC) is ideal.

3. The passive components are ideal with no voltage or current dependence. Neither are there any parasitic components associated with them.

4. The duty cycle is 50 %.

The voltage and current waveforms of the idealized class-E power amplifier are shown in Fig. 4.2. Note that the class-E circuit behavior is analyzed over one RF period.

An optimum class-E PA has to fulfill the ZVS and ZDVS conditions (Section 2.2.2) what can be mathematically described as

$$v_{drain}(\theta)|_{\theta=2\pi} = 0 \tag{4.2}$$

$$\left.\frac{dv_{drain}(\theta)}{d\theta}\right|_{\theta=2\pi} = 0 \tag{4.3}$$

where θ is the angular time ($\theta = \omega t$). The output current is assumed to be sinusoidal (an ideal SRC is part of the output network) and it can be written as

$$i_{out}(\theta) = I_{out}\sin(\theta + \varphi) \tag{4.4}$$

The parameter φ represents the phase shift due to the reactive element jX. The drain current i_{drain} is a sum of the switch current and the capacitor C_p current and it can be expressed as

$$i_{drain}(\theta) = I_{DD} + i_{out}(\theta) = I_{DD} + I_{out}\sin(\theta + \varphi) \tag{4.5}$$

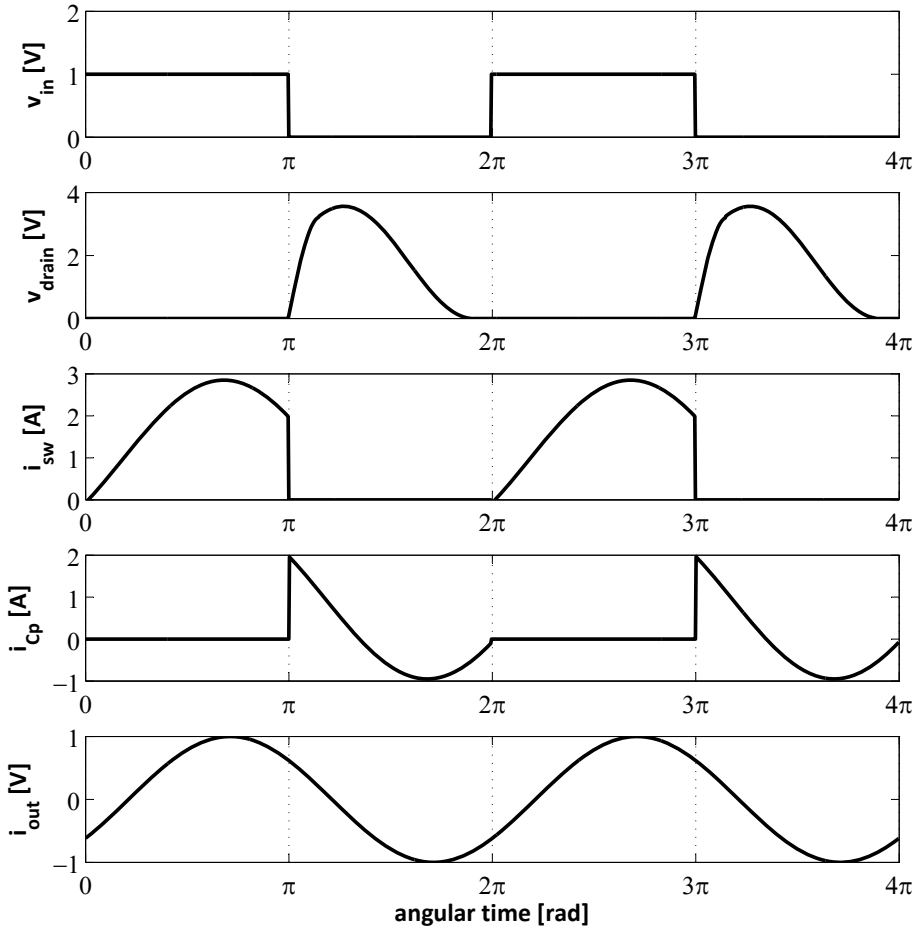


Figure 4.2: The waveforms of a class-E power amplifier.

The switch current is defined as

$$i_{sw}(\theta) = \begin{cases} I_{DD} + I_{out}\sin(\theta + \varphi) & \text{if } 0 \leq \theta \leq \pi \\ 0 & \text{if } \pi \leq \theta \leq 2\pi \end{cases} \tag{4.6}$$

When the switch is ON ($0 \leq \theta \leq \pi$) the capacitor C_p current $i_{C_p}(\theta) = 0$. Applying the Kirchoff's current law to the drain node results in

$$i_{sw}(\theta) = I_{DD} + I_{out}\sin(\theta + \varphi) \tag{4.7}$$

By using the initial condition $i_{sw}(0) = 0$ in Eq. (4.7) the DC current can be expressed as

$$I_{DD} = -I_{out}\sin(\varphi) \tag{4.8}$$

The output current and switch current can be rewritten as

$$i_{out}(\theta) = -\frac{I_{DD}}{\sin(\varphi)}\sin(\theta+\varphi) \tag{4.9}$$

$$\begin{aligned} i_{sw}(\theta) &= -I_{out}\sin(\varphi) + I_{out}\sin(\theta+\varphi) = I_{out}\left[\sin(\theta+\varphi) - \sin(\varphi)\right] \\ &= I_{DD} - \frac{I_{DD}}{\sin(\varphi)}\sin(\theta+\varphi) = I_{DD}\left[1 - \frac{1}{\sin(\varphi)}\sin(\theta+\varphi)\right] \end{aligned} \tag{4.10}$$

When the switch is OFF ($\pi \leq \theta \leq 2\pi$) the switch current $i_{sw}(\theta) = 0$. The current through the capacitor C_p can be written as

$$i_{C_p}(\theta) = I_{DD} + I_{out}\sin(\theta+\varphi) \tag{4.11}$$

By using the initial condition $i_{C_p}(2\pi) = 0$ in Eq. (4.11) the DC current can be rewritten as

$$I_{DD} = -I_{out}\sin(\varphi) \tag{4.12}$$

that is the same as in Eq. (4.8). Therefore Eq. (4.12) is valid in the whole RF period. The capacitor current i_{C_p} can be rewritten as

$$i_{C_p}(\theta) = -I_{out}\left[\sin(\varphi) - \sin(\theta+\varphi)\right] \tag{4.13}$$

The voltage across the capacitor C_p is identical to the drain voltage v_{drain}. It can be described by

$$\begin{aligned} v_{C_p}(\theta) &= \frac{1}{\omega C_p}\int_{\pi}^{\theta} i_{C_p}(\theta)\,d\theta = -\frac{I_{out}}{\omega C_p}\int_{\pi}^{\theta}\left[\sin(\varphi) - \sin(\theta+\varphi)\right]d\theta \\ &= -\frac{I_{out}}{\omega C_p}\left[\cos(\theta+\varphi) + \cos(\varphi) + (\theta-\pi)\sin(\varphi)\right] \end{aligned} \tag{4.14}$$

Applying the ZVS condition from Eq. (4.2) to Eq. (4.14) results in

$$\cos(\theta+\varphi) + \cos(\varphi) + (\theta-\pi)\sin(\varphi) \stackrel{!}{=} 0 \quad \text{for } \theta = 2\pi \tag{4.15}$$

$$2\cos(\varphi) + \pi\sin(\varphi) = 0 \tag{4.16}$$

The initial phase shift can be calculated as

$$\varphi \doteq -32.48^{\circ} \tag{4.17}$$

The φ has to be chosen exactly -32.48° otherwise v_{drain} voltage will be not zero when the switch turns ON. The relation described in Eq. (4.17) is important for further calculations because most of the class-E circuit equations are a function of φ. The

$\sin(\varphi)$ can be expressed as

$$\sin(\varphi) = \frac{-2}{\sqrt{\pi^2+4}} \doteq -0.537 \tag{4.18}$$

The equation 4.12 becomes

$$I_{DD} = -I_{out}\frac{-2}{\sqrt{\pi^2+4}} \doteq 0.537 I_{out} \tag{4.19}$$

Assuming that the SRC is ideal then the DC power is directly transformed to the load with no power dissipated in the active device, on the parasitic components or at harmonic frequencies. The average fundamental output power can be expressed as

$$P_{out} = I_{DD}V_{DD} = \frac{I_{out}^2}{2}R_L \tag{4.20}$$

By using Eq. (4.12) and Eq. (4.18) the DC supply current is calculated as

$$\begin{aligned} I_{DD}V_{DD} = \frac{I_{out}^2}{2}R_L &= \frac{R_L}{2}\left(-\frac{I_{DD}}{\sin(\varphi)}\right)^2 \\ \frac{2V_{DD}}{R_L} &= \frac{I_{DD}}{\sin^2(\varphi)} \\ I_{DD} = \frac{2V_{DD}}{R_L}\sin^2(\varphi) &= \frac{V_{DD}}{R_L}\frac{8}{\pi^2+4} \doteq 0.577\frac{V_{DD}}{R_L} \end{aligned} \tag{4.21}$$

The equivalent resistance seen from the power supply terminal is given as

$$R_{DD} = \frac{V_{DD}}{I_{DD}} = R_L\frac{\pi^2+4}{8} \doteq 1.734 R_L \tag{4.22}$$

The amplitude of the output voltage is obtained using Eq. (4.21)

$$V_{out} = I_{out}R_L = -\frac{I_{DD}}{\sin(\varphi)}R_L = -2V_{DD}\sin(\varphi) = \frac{4V_{DD}}{\sqrt{\pi^2+4}} \doteq 1.074 V_{DD} \tag{4.23}$$

The class-E PA design usually starts by choosing a proper transistor. The selection of the active device depends on the peak voltage and current requirements. The peak current flowing through the switch is

$$I_{sw,max} = I_{DD} + I_{out} = I_{DD}\left[1 - \frac{1}{\sin(\varphi)}\right] \qquad \doteq 2.862 I_{DD} \tag{4.24}$$

$$= I_{out}\left[1 - \sin(\varphi)\right] \qquad \doteq 1.537 I_{out} \tag{4.25}$$

The bias point of the class-E PA has to be selected according to Eq. (4.24). This equation can be rearranged to $I_{DD} = 0.349 I_{sw,max}$. The maximum drain voltage can be obtained by differentiating Eq. (4.14) and setting the result to zero, what results in

[Grebennikov & Sokal 2007]

$$v_{drain,max} = -2\pi\varphi V_{DD} \doteq 3.562 V_{DD} \tag{4.26}$$

where $\varphi = -0.5669\ rad$. Notice that the drain voltage peak is 3.5 times larger than the supply voltage. This imposes a serious reliability issue especially if the transistor is realized in CMOS technology. Eq. (4.26) limits the maximum allowable supply voltage. The peak supply voltage of the class-E PA has to be lower than the break-down voltage of the switching transistor. Therefore, the supply voltage can be calculated according to

$$V_{DD} \leq \frac{v_{drain,max}}{3.562} = \frac{V_{BR}}{3.562} \tag{4.27}$$

where V_{BR} is the break-down voltage of the active device.

Assuming the output power is given and the supply voltage is chosen according to Eq. (4.27), then the load impedance can be calculated from

$$R_L = V_{out}^2 \frac{1}{2P_{out}} = \frac{16V_{DD}^2}{\pi^2+4}\frac{1}{2P_{out}} = \frac{8}{\pi^2+4}\frac{V_{DD}^2}{P_{out}} \doteq 0.577\frac{V_{DD}^2}{P_{out}} \tag{4.28}$$

and

$$P_{out} = \frac{8}{\pi^2+4}\frac{V_{DD}^2}{R_L} \doteq 0.577\frac{V_{DD}^2}{R_L} \tag{4.29}$$

The calculated output impedance can have a very low value (less than $5\,\Omega$) if the supply voltage is limited and a high output power is required. An impedance transformer is required to match the output impedance to $50\,\Omega$.

The next step is to derive the equations for the circuit elements in the output network. The drain voltage that is given by Eq. (4.14) can be rewritten using Eq. (4.8) and Eq. (4.18) as

$$\begin{aligned} v_{C_p}(\theta) &= \frac{I_{DD}}{\omega C_p \sin(\varphi)}\left[\cos(\theta+\varphi)+\cos(\varphi)+(\theta-\pi)\sin(\varphi)\right] \\ &= \frac{I_{DD}}{\omega C_p}\left[\theta - \frac{3\pi}{2} - \frac{\pi}{2}\cos(\theta) - \sin(\theta)\right] \end{aligned} \tag{4.30}$$

what shows that the drain voltage consists of two quadrature components. If the SRC is ideal and it is tuned to the fundamental frequency, then there is no voltage drop across it in resonance. Therefore, the voltage across the capacitor C_p is divided between the excess inductance jX and the output resistance R_L. For easier manipulation the jX component is substituted by inductor L_x. The real part of the drain voltage represents the voltage across the load resistor and the imaginary part is the induced voltage on the L_x inductor. The fundamental component of these voltages can be identified by

applying the Fourier transform to Eq. (4.30). This results in

$$V_{R_L} = -\frac{1}{\pi}\int_0^{2\pi} v_{C_p}(\theta)\sin(\theta+\varphi)\,d\theta = \frac{I_{out}}{\pi\omega C_p}\left[\frac{\pi}{2}\sin(2\varphi)+2\cos(2\varphi)\right]$$

$$\doteq (-0.58)\frac{I_{out}}{\pi\omega C_p} \tag{4.31}$$

$$V_{L_x} = -\frac{1}{\pi}\int_0^{2\pi} v_{C_p}(\theta)\cos(\theta+\varphi)\,d\theta = \frac{I_{out}}{\pi\omega C_p}\left[\frac{\pi}{2}+\pi\sin^2(2\varphi)+2\sin(2\varphi)\right]$$

$$\doteq (-0.67)\frac{I_{out}}{\pi\omega C_p} \tag{4.32}$$

From these two equations the values of C_p and L_x can be calculated as

$$\frac{V_{L_x}}{V_{R_L}} = 1.1525 = \frac{\omega L_x}{R_L} \Rightarrow L_x = \frac{1.152R_L}{\omega} \tag{4.33}$$

$$R_L = \frac{V_{R_L}}{I_{out}} = \frac{0.58}{\pi\omega C_p} \Rightarrow C_p = \frac{0.184}{\omega R_L} \tag{4.34}$$

The L_0 and C_0 of the SRC are simply given as

$$L_0 = \frac{Q_L R_L}{\omega} - L_x \tag{4.35}$$

and

$$C_0 = \frac{1}{\omega^2 L_0} \tag{4.36}$$

where Q_L is the loaded quality of the resonant tank. It is assumed to be high to suppress the harmonics at the output.

The maximum frequency can be expressed as [Grebennikov & Sokal 2007]

$$f_{max} = \frac{1}{\pi^2}\frac{1}{\sqrt{\pi^2+4}+2}\frac{I_{sw,max}}{C_p VDD} \doteq \frac{I_{sw,max}}{56.5C_p VDD} \doteq \frac{I_{sw,max}}{15.86C_p V_{BR}} \tag{4.37}$$

it can be seen that the maximum frequency is proportional to the maximum switch current. It is inversely proportional to the total shunt capacitance (C_p) and the supply voltage. High frequency operation would require a high peak switch current and a low output capacitance and low supply voltage.

This was a simplified analysis of the optimum class-E power amplifier. In the next subsection the effects of non-idealities on the performance of the class-E PA are discussed.

4.2 Practical design aspects

A real class-E RF PA exhibits several non-idealities that affect the circuit performance (the ON resistance of the switch, the finite RFC and low quality inductors, finite switching time, non 50 % duty cycle, non-linear shunt capacitance and a load variation etc.).

A simplified circuit schematic of a real class-E power amplifier is shown in Fig. 4.3.

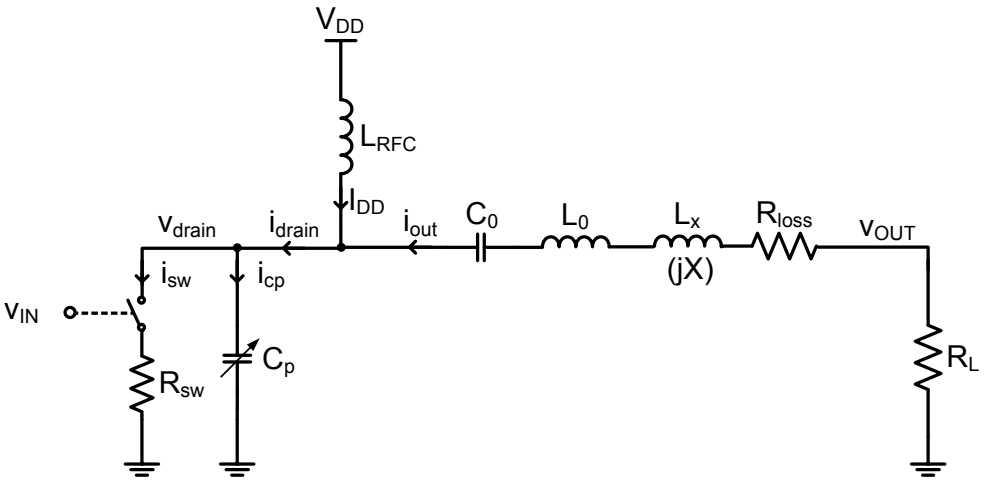


Figure 4.3: Circuit schema of the class-E power amplifier including non-idealities.

Most of the non-ideal effects are well described in textbooks [Albulet 2001, Grebennikov & Sokal 2007, Colantonio *et al.* 2009]. The next subsections are focused on brief description of the effect of R_{SW} resistance of the switch, the quality of inductors and the finite RFC technique on the class-E performance.

4.2.1 ON resistance of the switch

The transistor switch exhibits a non-zero ON resistance R_{SW}. It is assumed that this resistance is constant during the ON period. The effect of the R_{SW} on the class-E PA is that the active device dissipates power and the efficiency decreases. Usually, the size of the transistor is chosen as a trade-off between the capacitance and the drain-source (R_{SW}) resistance. Following analysis is based on [Raab & Sokal 1978].

The power dissipated in the transistor switch is given as

$$P_{diss} = \frac{R_{SW}}{2\pi} \int_0^{\pi} i_{sw}^2(\theta)\, d\theta \tag{4.38}$$

Using Eq. (4.10) it can be rewritten as

$$P_{diss} = \frac{R_{SW}}{2\pi} I_{DD}^2 \frac{8}{\pi}(\pi^2+28) = \frac{\pi^2+28}{2(\pi^2+4)} \frac{R_{SW}}{R_L} P_{out} \doteq 1.365 \frac{R_{SW}}{R_L} P_{out} \tag{4.39}$$

The drain efficiency can be expressed as

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{DC} - P_{diss}}{P_{DC}} = 1 - \frac{P_{diss}}{P_{DC}} \doteq \frac{1}{1 + 1.365\dfrac{R_{SW}}{R_L}} \tag{4.40}$$

Another expression of the drain efficiency that specifically accounts for the losses of a FET transistor was published in [Mader *et al.* 1998]

$$\eta = \frac{1 + \left(\dfrac{\pi}{2} + \omega C_p R_{SW}\right)^2}{\left(1 + \dfrac{\pi^2}{4}\right)(1 + \pi\omega C_p R_{SW})^2} \tag{4.41}$$

The voltage drop on R_{SW} resistor reduces the drain voltage to the effective value that can be calculated as

$$V_{eff} = V_{DD} - V_{Rsw} \tag{4.42}$$

$$V_{eff} = \frac{R_L}{R_L + 1.365 R_{SW}} V_{DD} \tag{4.43}$$

The V_{DD} voltage in all the class-E equations should replaced by V_{eff}. Note that the finite value of the R_{SW} resistance causes that the optimum design equations based on ZVS and ZDVS conditions will not lead to a highest efficiency [Grebennikov & Sokal 2007]. The values of L_x and C_p have to be modified in order to minimize the dissipated power losses. Therefore, the ideal switching conditions represent the optimum only for the idealized class-E amplifier.

4.2.2 Non-ideal LC tank

There are two main practical considerations regarding the LC tank that should be discussed. First is the quality factor of the SRC and second is the quality factor of the inductor L_0. The class-E performance study as a function of the quality factor of the LC tank is summarized in [Huijsing *et al.* 2002]. The loaded quality factor Q_L of the output resonant tank is defined as

$$Q_L = \frac{\omega(L_0 + L_x)}{R_L} = \frac{\omega L}{R_L} \tag{4.44}$$

where L is equal to $(L_0 + L_x)$. The resonant tank LC_0 does not resonate at the carrier frequency. Note that the loaded quality factor calculated by

$$Q_C = \frac{1}{\omega C_0 R_L} \tag{4.45}$$

is not the same as Q_L. They are related to each other by the reactance jX (represented by inductor L_x in Fig. 4.3). If one of the values of L_0 or C_0 is known the other one

can be calculated using $\omega = 1/\sqrt{L_0 C_0}$.

The total parasitic equivalent series resistance of the LC tank is equivalent to

$$R_{LC_0} = R_L + R_{C_0} = \frac{\omega L}{Q'_L} + \frac{1}{\omega C_0 Q'_{C_0}} \tag{4.46}$$

where Q'_L and Q'_{C_0} are the quality factors of L and C_0 respectively. The quality factor of an inductor is much lower than the quality factor of a capacitor. Hence, the parasitic resistance of the inductor that represents the losses in the LC tank is placed in series with the load resistor. The parasitic resistor will dissipate power. The output power from Eq. (4.29) can be rewritten as

$$P_{out} = \frac{8}{\pi^2 + 4} \frac{V_{DD}^2}{R_{LC_0} + R_L} \doteq 0.577 \frac{V_{DD}^2}{R_{LC_0} + R_L} \tag{4.47}$$

Finally, the drain efficiency is

$$\eta = \frac{R_L}{R_{LC_0} + R_L} = \frac{1}{1 + \frac{R_{LC_0}}{R_L}} \doteq \frac{1}{1 + \frac{Q_L + 1.1525}{Q'_L}} \tag{4.48}$$

The loaded quality factor Q_L of the class-E PA output network is an input design parameter. There is a trade-off between BW, output harmonics and power loss in SRC. Practical values of Q can be quite low (below 10) what results in poor harmonics suppression and an additional filter at the output of the PA is required.

4.2.3 Finite RFC technique

In the class-E PA analysis in Section 4.1 it is assumed that the RF choke inductor is ideal. To avoid that RFC will affect the behavior of a class-E PA the RF choke inductor should fulfill the following criteria. The reactance of the RFC should be large enough in comparison with C_p (RFC is in parallel with C_p) to avoid the influence of the RFC on the output network. Usually, the rule of thumb is

$$\omega RFC > 30 R_L \tag{4.49}$$

This value is usually too high for a practical implementation on a silicon chip. The behavior of a class-E amplifier changes when the inductance of the RFC decreases. Nevertheless it is possible to achieve the class-E behavior even with finite RF choke. The RFC inductor becomes a design element of the PA because it directly influences the response of the output network. The finite RFC inductor is denoted in Fig. 4.3 as L_{RFC}. The summary of the class-E PA circuit analysis using the finite RFC technique is provided in this subsection.

A major advantage of using the finite RFC technique is that the drain voltage peak is reduced to as low as $2.5 V_{DD}$ [Yoo *et al.* 2001]. Beside that, for the same output power and supply voltage a higher efficiency can be achieved. The output network

is a function of one more design parameter L_{RFC}. This allows to increase the load resistance compared to the conventional class-E amplifier.

The analysis of the class-E PA behavior with finite dc-feed inductance is quite complex. The fully analytical solution of the differential equations can not be obtained. The result is usually a numerical table or a set of polynomial functions describing the values of the class-E PA circuit elements. The analysis is further complicated by increasing the number of considered non-idealities (finite dc-feed inductance, finite Q of the LC tank, switch ON resistance or varying duty cycle). Examples of a class-E PA analysis using a finite RFC can be found in [Grebennikov & Sokal 2007, Zulinski & Steadman 1987]. The design equations provided in this subsection are based on [Acar *et al.* 2007].

There are four parameters that relate the circuit component values and input parameters. These parameters are defined as

$$K_L = \frac{\omega L_{RFC}}{R_L} \tag{4.50}$$

$$K_C = \omega C_p R_L \tag{4.51}$$

$$K_P = P_{out} \frac{R_L}{V_{DD}^2} \tag{4.52}$$

$$K_X = \frac{X}{R_L} \tag{4.53}$$

where X is the excess reactance of the output network. For example the idealized simple class-E amplifier can be described by

$$\begin{aligned} K_L &= \infty \\ K_C &= 0.184 \\ K_P &= 0.577 \\ K_X &= 1.152 \end{aligned} \tag{4.54}$$

The class-E PA behavior (including the effect of finite RFC) can described by these

set of equations

$$K_L(q,d) = \frac{1}{\frac{d^2\pi}{2p} - 2\cos(d\pi+\varphi) + 2d\pi\sin(\varphi) + 4\cos(\varphi)} \tag{4.55}$$

$$K_C(q,d) = \frac{1}{q^2 K_L(q,d)} \tag{4.56}$$

$$K_P(q,d) = \frac{1}{2}\frac{p^2}{K_L(q,d)^2} \tag{4.57}$$

$$K_X(q,d) = \frac{V_{L_x}}{V_{R_L}} \tag{4.58}$$

where the parameters q, p, φ, d are defined as

$$q = \frac{1}{\omega\sqrt{L_{RFC}C_p}} \tag{4.59}$$

$$p = \frac{\omega L_{RFC} I_{out}}{V_{DD}} \tag{4.60}$$

and φ is the phase shift introduced by the jX element in the output network and d is a duty cycle parameter ($d = 1$ corresponds to 50 % duty cycle). It is shown in [Acar *et al.* 2007] that the equations of parameters φ and p can be solved analytically using q and d as variables. Therefore, Eq. (4.55) - Eq. (4.58) are functions of q and d only. The example of the design set based on these equations for maximum output power is

$$\begin{aligned} K_L &= 0.732 \\ K_C &= 0.685 \\ K_P &= 1.365 \\ K_X &= 0 \end{aligned} \tag{4.61}$$

where $q = 1.412$ and $d = 1$. The tables of different design sets can be found in [Acar *et al.* 2007]. Note that X might be inductive or capacitive depending on the sign of $K_X(q,d)$.

4.3 Impedance transformation

Usually the output impedance R_L of the PA is low (several ohms) and for practical reasons the output impedance of the PA should be matched to 50 Ω. There are numerous

options how the impedance matching circuit can be implemented. One of the simplest and very often used is a low-pass LC circuit (L-match). This type of circuit can be used for the impedance up-conversion and can be easily integrated on-chip. The class-E PA with LC output matching circuit is shown in Fig. 4.4.

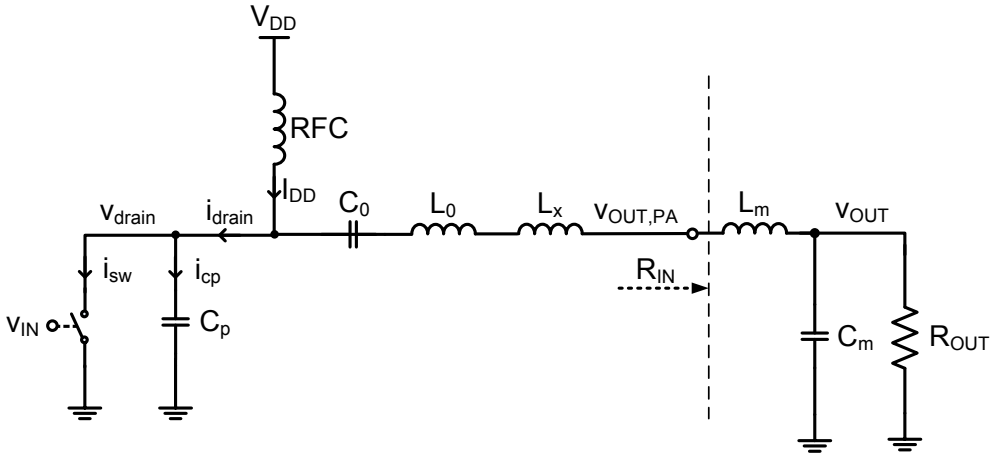


Figure 4.4: Class-E power amplifier with impedance matching circuit.

The main parameter of an impedance matching circuit is its efficiency. A high efficient matching circuit does not have power losses and all the PA output power is delivered to the 50 Ω load. The impedance matching circuit should have a sufficient bandwidth. The signal applied to the input of the matching circuit should be properly filtered.

The advantage of the low-pass LC circuit is that the matching inductor L_m can be integrated into one inductor with L_0 and L_x. The parallel combination of R_{OUT} and C_m can be converted into the equivalent series combination as

$$R_s = \frac{R_{OUT}}{1 + Q_{C_m}^2} \tag{4.62}$$

$$C_s = C_m \left(1 + \frac{1}{Q_{C_m}^2}\right) \tag{4.63}$$

$$Q_{C_m} = \omega C_m R_{OUT} \tag{4.64}$$

The LC circuit L_m and C_s resonates at the carrier frequency. Therefore, the output impedance seen by the PA at fundamental frequency is R_s which is equal to R_{IN}. The impedance transformation ratio r is

$$r = \frac{R_{OUT}}{R_{IN}} = \frac{R_{OUT}}{R_s} \tag{4.65}$$

Using the impedance transformation ratio the quality of the impedance transformation

network can be written as

$$Q_m = \sqrt{r-1} \tag{4.66}$$

The L-match network can be seen as a combination of the series (L_m and R_{IN}) and parallel (C_m and R_{OUT}) circuits. The L_m and C_m values can be calculated from

$$L_m = \frac{Q_m R_{IN}}{\omega} \tag{4.67}$$

$$C_m = \frac{Q_m}{\omega R_{OUT}} \tag{4.68}$$

The quality of the L-match is mainly given by the quality of the L_m inductor. The loss resistance R_{Lm} of the L_m inductor is added in series with the output load R_s. The output power of the PA can be calculated as

$$P_{out,PA} = \frac{V_{R_s}^2}{R_s} = \left(V_{out,PA} \frac{R_s}{R_s + R_{Lm}} \right)^2 \frac{1}{R_s} \tag{4.69}$$

where

$$V_{out,PA} = V_{R_s} + V_{R_{Lm}} \tag{4.70}$$

It is assumed that the $P_{out,PA}$ is losslessly delivered to the output impedance R_{OUT}. The total input power to the L-match network is

$$P_{in,m} = \frac{V_{out,PA}^2}{R_s + R_{Lm}} \tag{4.71}$$

and therefore, the efficiency of the impedance matching circuit can be written as

$$\eta_m = \frac{P_{out,PA}}{P_{in,m}} = \frac{R_s}{R_s + R_{Lm}} \tag{4.72}$$

Chapter 5

Cascode modulated Class-E PA

Contents

In this chapter various design aspects of the cascode class-E PA are discussed. The first section briefly shows simulated performance of an ideal class-E PA. The simulation results of the cascode class-E PA are described in the second section. The various aspects of the design are discussed in the third section. An adaptive supply voltage concept is briefly introduced in the fourth section. The reliability analysis is added in the fifth section.

The simulations in this section use CMOS UMC 0.13 μm technology. The standard NMOS transistor in this technology has gate length of 0.12 μm and its nominal voltage is 1.2 V. The thick gate-oxide NMOS transistor has gate length of 0.34 μm and its nominal voltage is 3.3 V. Unless otherwise stated, the term *output power* (P_{out}) refers to the average output power delivered into the 50 Ω load at the fundamental frequency. The input power (P_{in}) represents the *available average input power*.

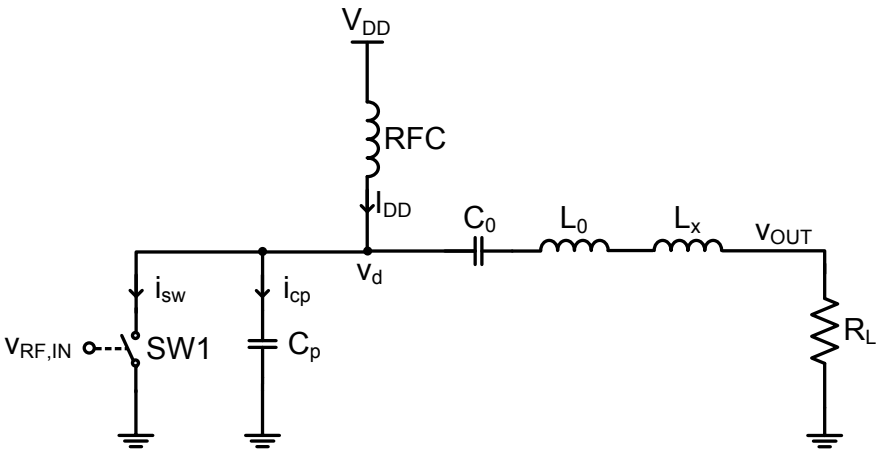


Figure 5.1: Simplified circuit of the ideal class-E power amplifier.

5.1 Ideal Class-E PA

In this section the simulation results of the ideal class-E PA are presented. The design equations of the class-E PA were introduced in the previous chapter.

In order to validate the theory from the Section 4.1 firstly a simple class-E amplifier is designed. Its performance is then confirmed via simulations. Let's assume that the task is to design a class-E PA that should operate at the frequency of 2 GHz. The PA should deliver the output power of 0.5 W to the load resistor with the supply voltage V_{dd} of 1.8 V. The schematic of the class-E PA is shown in Fig. 5.1. It's assumed that the input signal is an ideal square wave that swings from zero to V_{dd}. The RFC is considered to be an ideal inductor (infinitely large lossless inductor).

The design process starts by determining the load resistor (R_L) value that is calculated using Eq. (4.28)

$$R_L = 0.5768\frac{V_{DD}^2}{P_{out}} = 3.74\,\Omega \tag{5.1}$$

Then from Eq. (4.33) the value of excess inductance L_x can be calculated as

$$L_x = \frac{1.152R_L}{\omega} = 0.343\,nH \tag{5.2}$$

Using Eq. (4.34) the value of the shunt capacitor C_p is obtained as

$$C_p = \frac{0.184}{\omega R_L} = 3.91\,pF \tag{5.3}$$

In order to calculate the component values of the LC tank the designer has to choose the quality factor of the resonant tank. In practice, the quality factor of the resonant tank is limited by the quality of the inductor (that can be rather low especially in the CMOS technology). To achieve a performance very close to the ideal class-E PA relatively high loaded quality of 20 is selected. Then L_0 and C_0 is calculated according to Eq. (4.35)

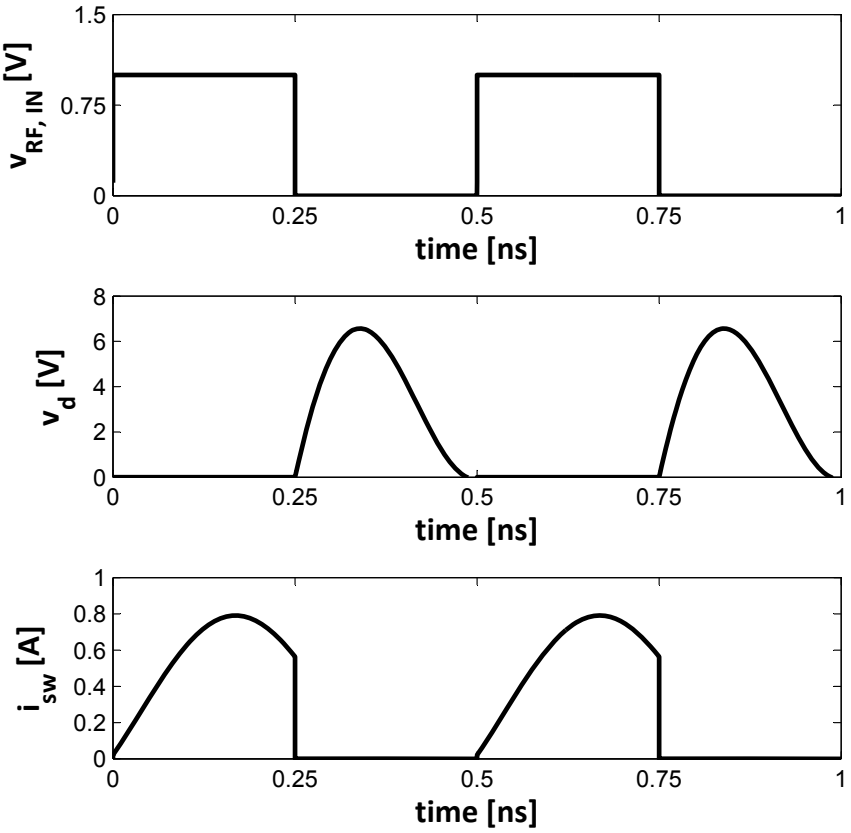


Figure 5.2: RF input voltage ($V_{RF,IN}$), drain voltage (V_d) and current through the switch (i_{sw}) versus time.

and (4.36)

$$L_0 = \frac{Q_L R_L}{\omega} - L_x = 5.6\,nH \tag{5.4}$$

$$C_0 = \frac{1}{\omega^2 L_0} = 1.13\,pF \tag{5.5}$$

The simulated performance is shown in Fig. 5.2. One can see that both the drain voltage and the current through the switch correlate well with the ideal class-E PA waveforms. When the RF input voltage is high, the switch is ON and the current flows through the switch SW1. When the switch is OFF, the drain voltage raises up to 6.4 V predicted by Eq. (4.26). The drain efficiency of the simulated PA is 99.9 % assuming the SW1 is an ideal switch.

The equation (5.1) assumes 100 % drain efficiency. The actual implemented PA has a limited efficiency due to the losses in the system. Therefore, the load resistance cal-

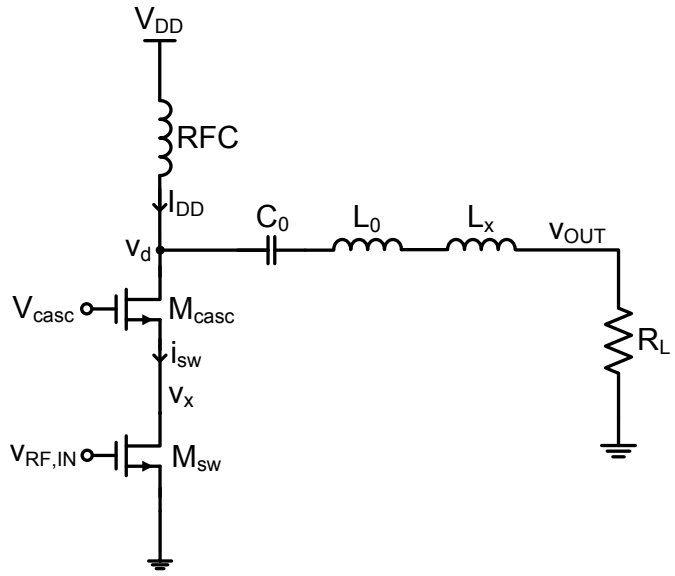


Figure 5.3: Simplified circuit of the cascode class-E power amplifier.

culated by Eq. 5.1 has to be decreased accordingly to the expected efficiency otherwise the required output power will not be met.

5.2 Cascode modulated Class-E PA

The class-E PA from the previous section utilized an ideal switch. In this section the switch is replaced with the real NMOS transistor M_{sw} and the cascode device M_{casc} is added into the topology. The schematic of the cascode modulated class-E PA is shown in Fig. 5.3.

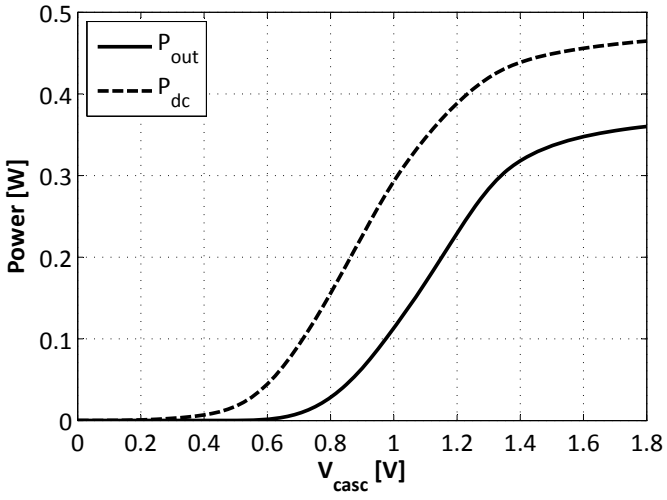


Figure 5.4: Output power and DC input power versus the V_{casc} voltage.

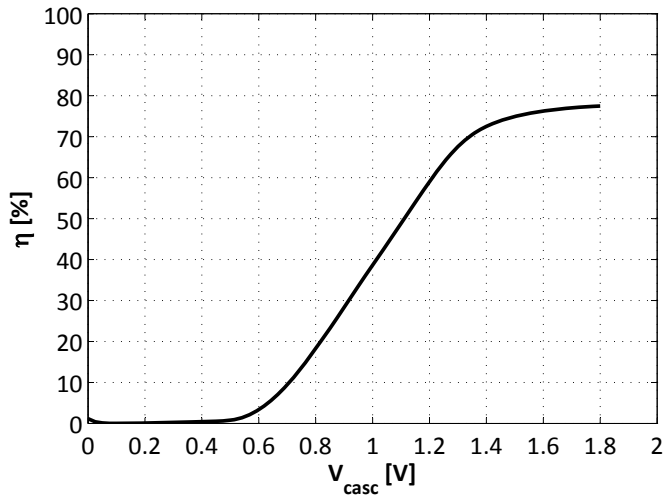


Figure 5.5: Drain efficiency versus the V_{casc} voltage.

The bottom transistor (M_{sw}) is connected as a common-source transistor. The cascode transistor (M_{casc}) operates as a common-gate transistor. The terms *switch transistor* and M_{SW}, and similarly the *cascode transistor* and M_{CAS}, are used interchangeably throughout this thesis.

The sizes of the M_{sw} and M_{casc} transistors are $3040\,\mu m/0.12\,\mu m$ and $6080\,\mu m/0.32\,\mu m$ respectively. In this chapter the M_{sw} transistor is also referred to as 1.2 V NMOS (thin gate-oxide device). The M_{casc} transistor is implemented as 3.3 V NMOS (thick gate-oxide device).

The size of the M_{casc} is chosen so that the shunt capacitor C_p is fully absorbed by the output capacitance of the NMOS transistor. The size of the M_{sw} transistor is selected as a trade-off between the ON resistance and input capacitance. The detailed analysis on device sizing is provided in Subsection 5.3.

The most important feature of the cascode modulated class-E PA is the ability to control the output power by changing the cascode voltage V_{casc}. This relation can be used to control the average power level [Sira *et al.* 2010] or amplitude modulated signal can be directly applied in the case of a polar transmitter [Sira *et al.* 2011]. The relation between the output power and DC input power on the V_{casc} voltage is shown in Fig. 5.47.

The M_{sw} transistor is operated as a switch. That means it is either OFF or in the deep triode region. The M_{casc} transistor operates either in saturation or in the triode region. The mode of the operation of the M_{casc} transistor depends on the V_{casc} voltage.

The drain efficiency (DE) as a function of the V_{casc} voltage is plotted in Fig. 5.5. The maximum drain efficiency is 78 %. One can see that the drain efficiency drops to zero for the V_{casc} below approximately 0.5 V. The decreased DE indicates that the PA is no longer operating as an ideal class-E PA. The effective non zero ON resistance of the transistors is the main cause of the efficiency degradation at high V_{casc} levels. The practical DE will be further reduced due to the losses especially in the inductors. Also

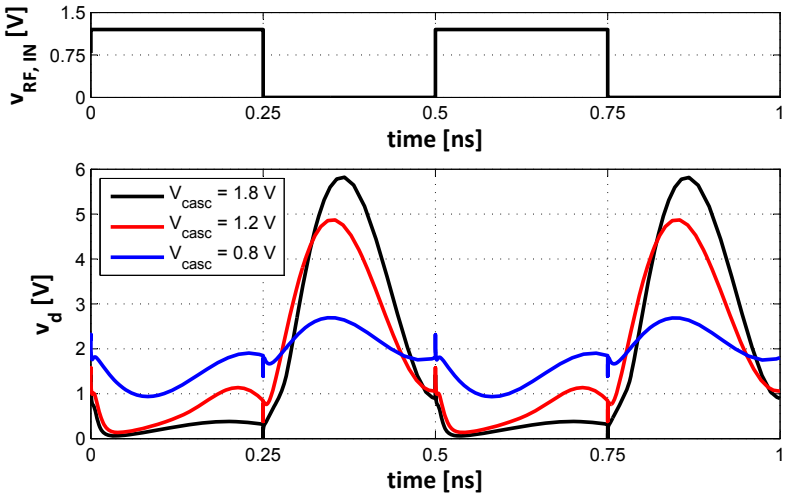


Figure 5.6: RF input voltage ($v_{RF,IN}$) and drain voltage (v_d) versus time. The parameter is V_{casc} voltage.

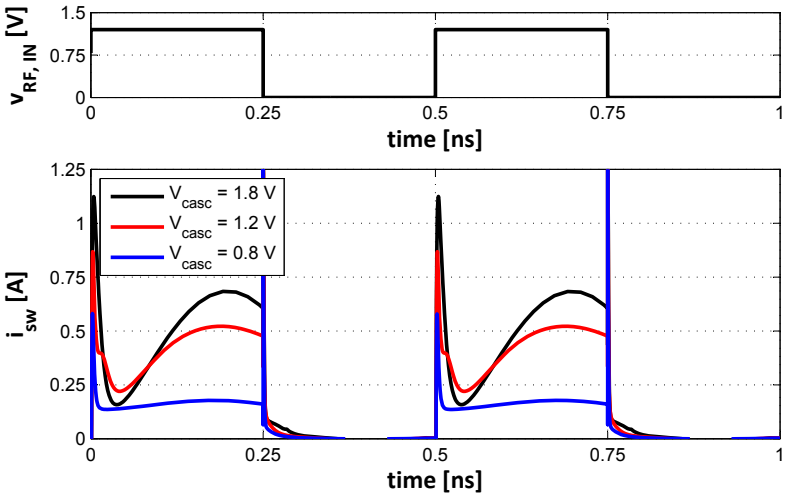


Figure 5.7: RF input voltage ($v_{RF,IN}$) and current through the switch (i_{sw}) versus time. The parameter is V_{casc} voltage.

the variation of the cascode transistor output capacitance causes that the amplifier will diverge from the class-E operation and this will cause additional power loss. If the parasitic capacitance of the transistors deviates even slightly (10 %) from the model the behavior of the circuit changes significantly. The same is valid for the on-chip interconnect capacitances.

The plot of the drain voltage and switch current is shown in Fig. 5.6 and Fig. 5.7 respectively. In each of the figures the parameter is the V_{casc} voltage. From the efficiency perspective the most interesting is Fig. 5.6. One can observe that the drain voltage (v_d is taken from the drain of the cascode transistor M_{casc}) during the ON

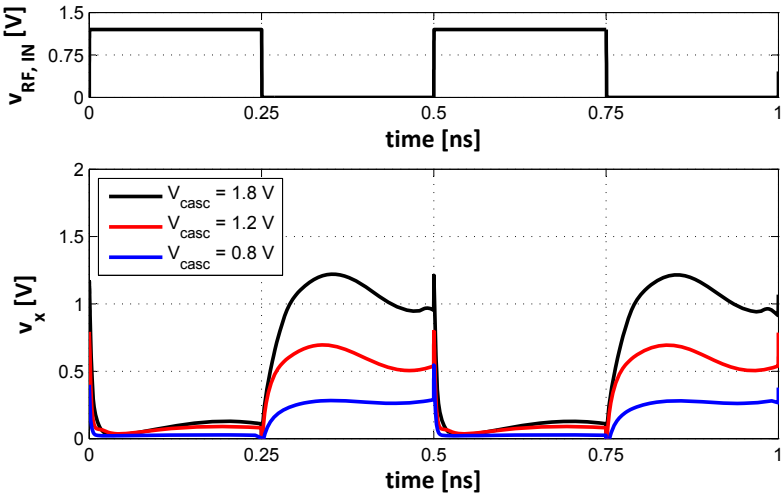


Figure 5.8: RF input voltage ($v_{RF,IN}$) and v_x voltage versus time. The parameter is V_{casc} voltage.

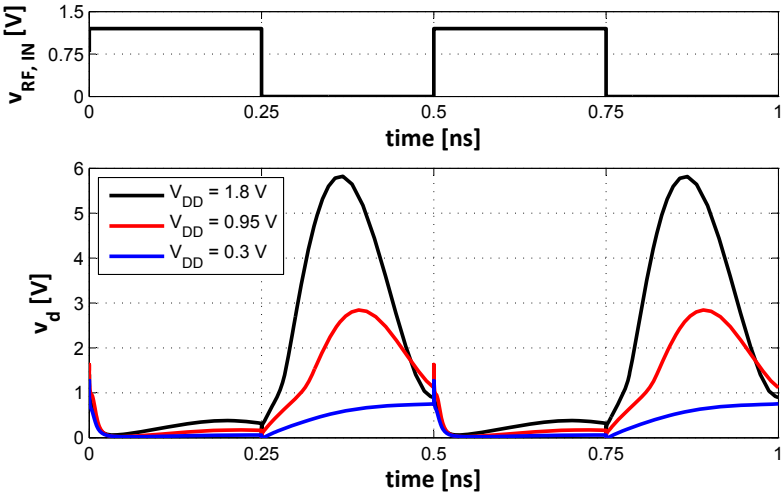


Figure 5.9: RF input voltage ($v_{RF,IN}$) and drain voltage (v_d) versus time. The parameter is V_{dd} voltage.

period (high $v_{RF,IN}$) is increasing with V_{casc} decreasing.

A different view on the behavior of the V_d would be to see the V_d node as a part of the output tuned circuit. When the energy added at each switching action is low (V_{casc} is low) the output tuned circuit (composed of the passive components only) will have shape close to a sine wave with average DC value at V_{DD} supply rail. As the switching action during the ON-phase becomes stronger (larger V_{casc}), the shape becomes more asymmetrical and eventually stays at very low level close to the ground.

From Fig. 5.8 it can be seen that the common node voltage V_x decreases with the decreasing V_{casc}. During the OFF phase the net V_x becomes floating from the DC point

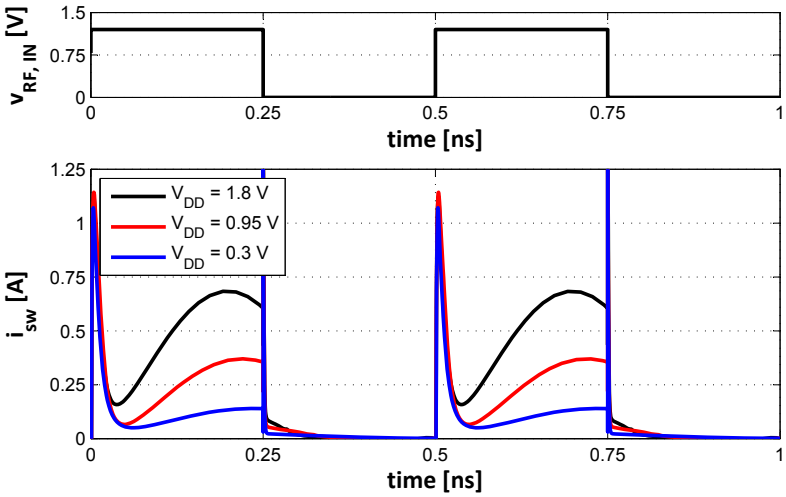


Figure 5.10: RF input voltage ($v_{RF,IN}$) and current through the switch (i_{sw}) versus time. The parameter is V_{dd} voltage.

of view and the cascode transistor will have tendency to enter the moderate-to-week inversion state depending on the amount of parasitic capacitance related to the net V_x.

The consequence of high v_d during the ON period is that the efficiency will be low (there is an instantaneous overlap of the voltage and current in the transistors causing the power being dissipated by the NMOS devices rather than transferred towards the PA output). The DE can be improved by the means of adaptive supply voltage. This technique is discussed later in Section 5.4.

The important conclusion from these observations is that the behavior of the cascode modulated class-E PA deviates significantly from the ideal class-E conditions.

For comparison purposes the drain voltage and switch current using the supply modulation are shown in Fig. 5.9 and Fig. 5.10 respectively.

The peak drain voltages of the transistors during the OFF period are shown in Fig. 5.11. It can be seen that the drain voltage v_d equals to V_{dd} for low V_{casc} and it increases up to 5.8 V for high V_{casc}. The drain-source voltage of the switch transistor v_x is directly limited by the V_{casc}. The drain-gate and drain-source voltages of the cascode transistor exhibit very high voltage swing and this is the cause of the reliability issue of the class-E PAs. The reliability is discussed in the Section 5.5.

As it was mentioned before, the cascode transistor during the ON RF period can operate either in saturation or triode region. The voltages between the cascode transistor terminals are plotted in Fig. 5.12. The black curve that represents the drain-source voltage minus the saturation voltage shows when the cascode transistor is in saturation. If the voltage is positive the M_{casc} transistor is in saturation and if negative it is in triode region. It can be seen that the switching point is approximately at $V_{casc} = 1.2\,V$.

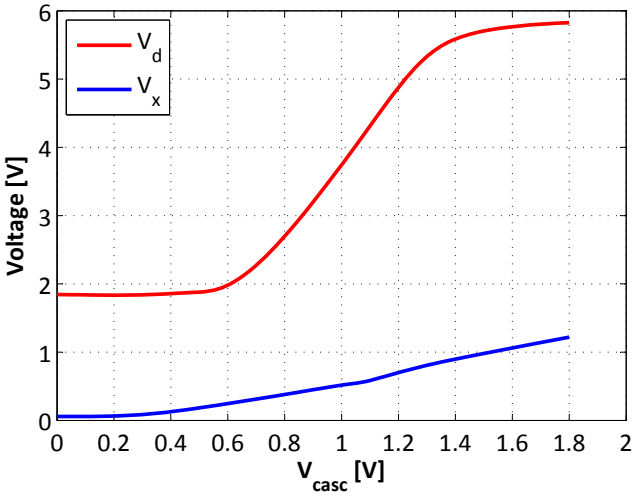


Figure 5.11: Simulated peak drain voltages of M_{sw} and M_{casc} transistors in the OFF period of the RF cycle versus the cascode control voltage V_{casc} ($V_{DD} = 1.8\,V$).

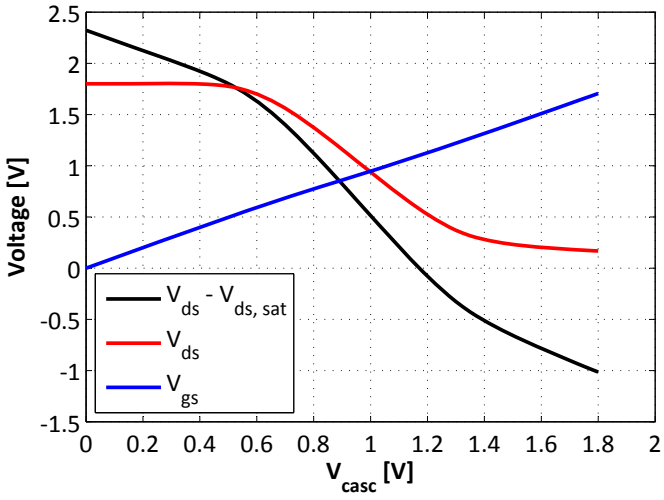


Figure 5.12: Simulated peak voltages of cascode transistor during the ON period of the RF cycle versus the cascode control voltage V_{casc} ($V_{DD} = 1.8\,V$).

5.3 Design

In this section the most important transistor design aspects of the cascode class-E PA are discussed. The cascode class-E PA is a very specific type of circuit. The size of transistors has to be carefully chosen in order to balance the different design trade-offs.

This section is divided into three main parts. First part is focused on the transistor device itself, second part describes the behavior of the cascode topology and in the third part the driving requirements of the cascode class-E PA are analyzed.

5.3.1 Transistors

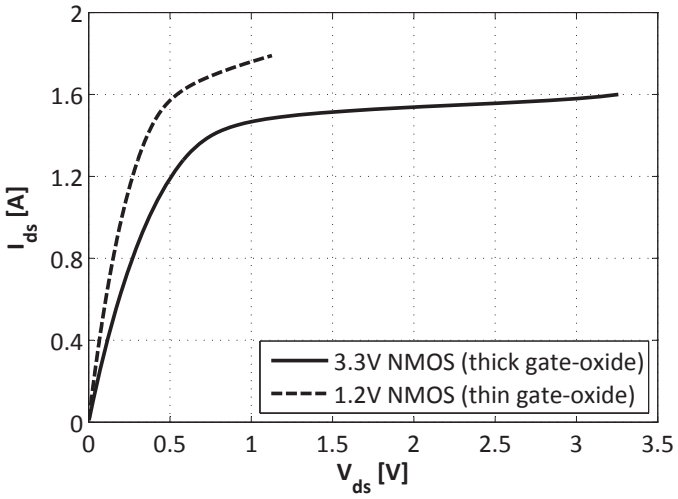


Figure 5.13: Drain current (I_{ds}) versus drain-source voltage (V_{ds}) of a standard (1.2 V NMOS) and thick gate-oxide (3.3 V NMOS) device. The V_{gs} voltage is the maximum nominal voltage of each device. Both transistors have the nominal size.

Various design parameters of the power transistors are compared in this section. The overal goal is to provide a design guideline for the cascode transistors sizing.

If not stated otherwise the simulations are performed using the maximum nominal voltages and nominal transistor sizes. The standard 1.2 V NMOS thin gate-oxide transistor has the maximum nominal terminal voltage of 1.2 V and its nominal size is 3040 μm/0.12 μm. The 3.3 V NMOS thick gate-oxide transistor has the maximum nominal terminal voltage of 3.3 V and its nominal size 6080 μm/0.32 μm.

The output characteristics of both devices are plotted in Fig. 5.13. The primary requirement with regard to the device sizing is that the transistors have to be able to handle the peak current of the cascode class-E PA (Fig. 5.7). The peak drain current is approximately 0.7 A.

5.3.1.1 ON resistance and efficiency

The most important parameter that directly influences the efficiency of the PA is the ON resistance (drain-source channel resistance) of the switch transistor M_{SW}. The channel resistance of the transistor in the saturation region can be calculated as

$$r_{ds} \approx \frac{1}{\lambda I_{ds}} \tag{5.6}$$

and in the triode region as

$$r_{ds} = \frac{1}{\mu_0 C_{OX} W/L (V_{GS} - V_T)} \tag{5.7}$$

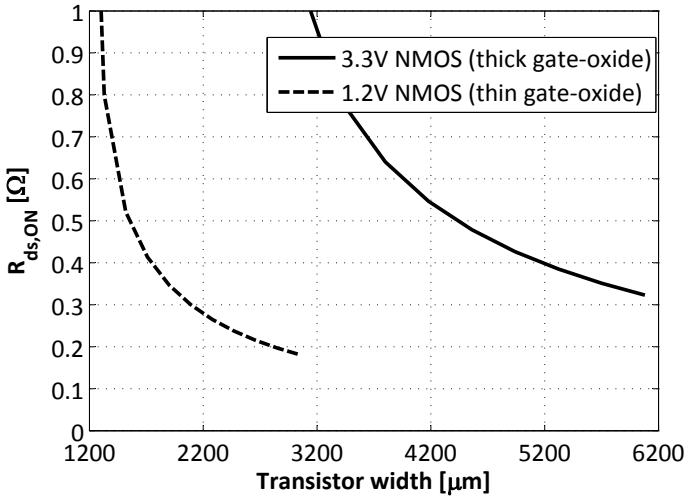


Figure 5.14: Transistor ON resistance versus the channel width of a standard (1.2 V NMOS) and thick gate-oxide (3.3 V NMOS) device. The V_{gs} voltage is the maximum nominal voltage of each device. Both transistors have the nominal size. The drain current is 0.7 A.

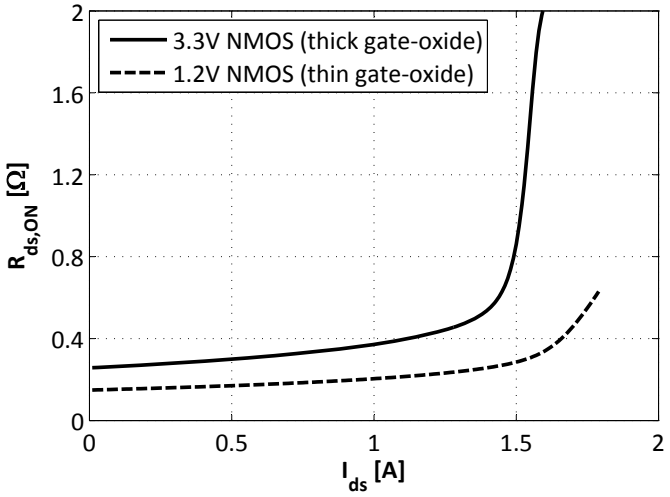


Figure 5.15: Transistor ON resistance versus the drain current of a standard (1.2 V NMOS) and thick gate-oxide (3.3 V NMOS) device. The V_{gs} voltage is the maximum nominal voltage of each device. Both transistors have the nominal size.

where λ is the output impedance constant, μ_0 and C_{OX} are the mobility of the carriers and the gate oxide capacitance respectively. W is the channel width and L is the channel length. It can be seen that the ON resistance in the triode region is inversely proportional to the W/L ratio. The plot of the ON resistance versus the transistor width is shown in Fig. 5.14. In the analyzed PA design the value of the ON resistance has to be well below $1\,\Omega$ in order to maintain a decent PA efficiency.

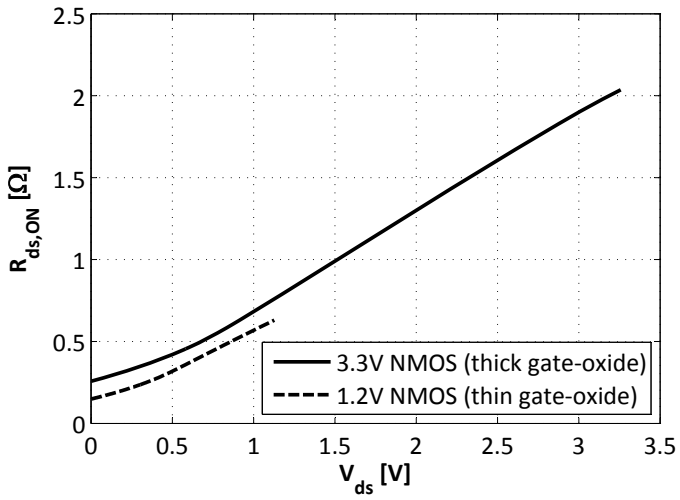


Figure 5.16: Transistor ON resistance versus the drain-source voltage of a standard (1.2 V NMOS) and thick gate-oxide (3.3 V NMOS) device. The V_{gs} voltage is the maximum nominal voltage of each device. Both transistors have the nominal size.

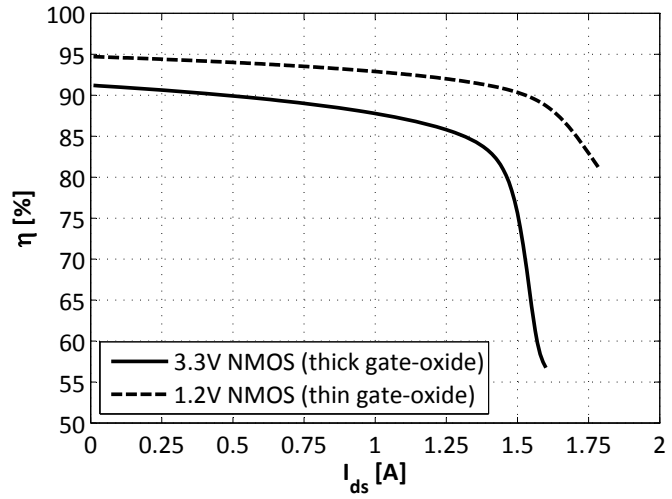


Figure 5.17: The drain efficiency versus the drain current (I_{ds}) of a standard (1.2 V NMOS) and thick gate-oxide (3.3 V NMOS) device. The V_{gs} voltage is the maximum nominal voltage of each device. Both transistors have the nominal size.

The thick gate-oxide transistor has to be approximately 3-times wider to have the same ON resistance as the thin gate-oxide transistor. The ON resistance as a function of the drain current is shown in Fig. 5.15. The ON resistance increases only very slowly with the drain current if the transistors operate in the triode region. Once the transistors enter the saturation region the ON resistance increases rapidly. Another consequence of high ON resistance is that the voltage drop across the power transistor is high. The simulated relationship between the ON resistance and drain-source voltage

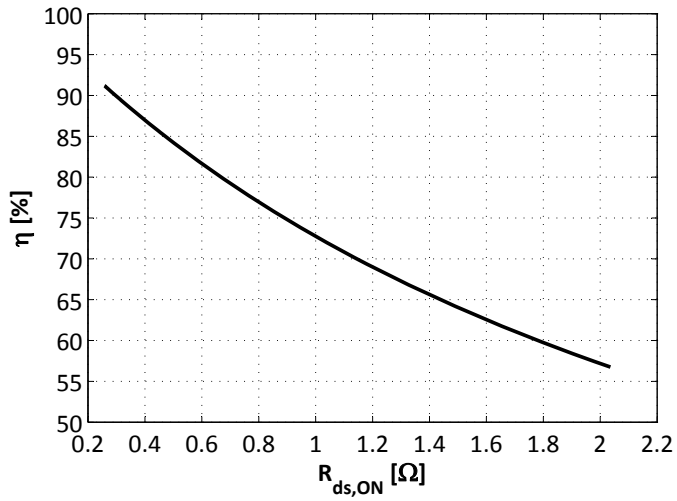


Figure 5.18: The drain efficiency versus the ON resistance.

of the transistor is shown in Fig. 5.16.

Fig. 5.17 and Fig. 5.18 show the simulated drain efficiency of the simple class-E PA (single transistor stage) as a function of the drain current and ON resistance respectively. Assuming the class-E PA is loaded with the resistance of $3.74\,\Omega$, as was calculated in Section 5.1, the drain efficiency of the class-E PA as a function of the ON resistance is given by Eq. (4.40) as

$$\eta \doteq \frac{1}{1 + 1.365\dfrac{R_{ds,ON}}{R_L}}$$

This equation is directly plotted in Fig. 5.18. The drain efficiency drops fast with the increasing ON resistance. If the transistor exhibits $1\,\Omega$ ON resistance the efficiency of the class-E PA would drop below 75 % (other device losses are not considered). If an additional cascode transistor is added the drain efficiency drops even lower.

5.3.1.2 Input capacitance

The input capacitance is an important design parameter because it directly influences the design of the PA driver and cascode transistor driver. The input capacitance of the transistor can be simply approximated as

$$C_{in} = C_{GS} + C_{GD} + C_{GB} \tag{5.8}$$

The input capacitance has to be charged to the threshold voltage before the power transistor starts to turn ON and it has to be discharged before the device turns OFF. The assumption in the following simulations is that the ideal class-E PA complies with the ZVS condition. This means that in the instance when the switch turns ON there

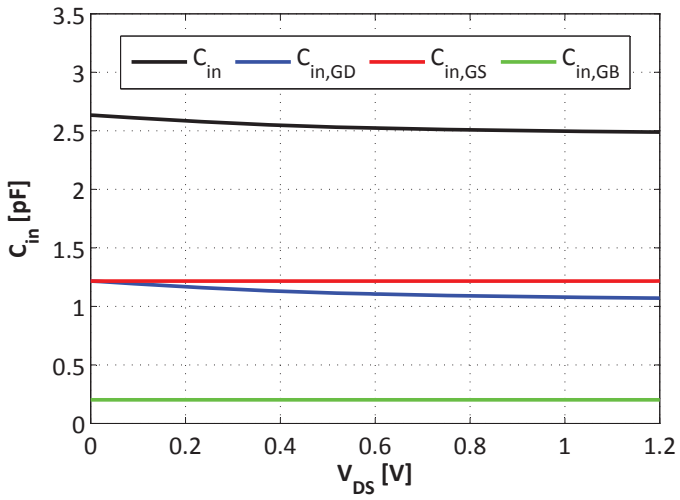


Figure 5.19: Input capacitance as a function of the drain-source voltage (1.2 V NMOS transistor, $V_{GS} = 0\,V$).

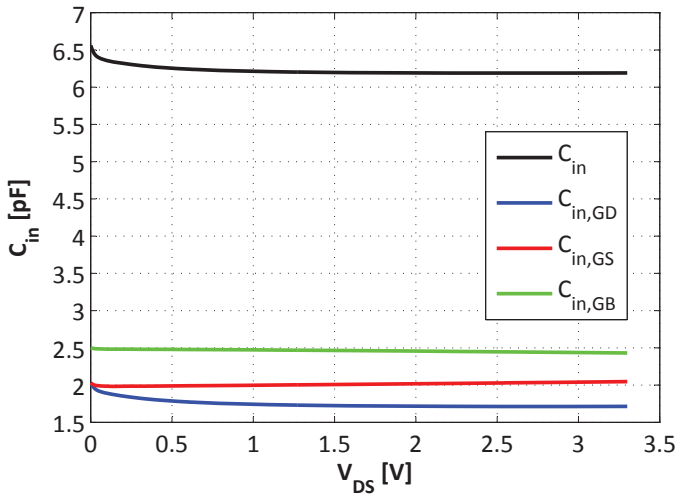


Figure 5.20: Input capacitance as a function of the drain-source voltage (3.3 V NMOS transistor, $V_{GS} = 0\,V$).

is no voltage across it and therefore the Miller effect is not present. The drain voltage change will have impact on the effective gate capacitance via the feedback through C_{DG}. This is known as Miller effect. The input capacitance analysis is performed using the transistor in OFF state ($V_{GS} = 0\,V$).

The simulations of the input capacitance as a function of the drain-source DC voltage is shown in Fig. 5.19 and Fig. 5.20 for 1.2 V NMOS and 3.3 V NMOS transistor respectively. It can be seen that the input capacitance is almost constant with respect to the V_{DS} voltage. The main difference between the two transistors is that the intrinsic capacitance of the thick gate-oxide transistor is much larger than of the thin gate-oxide

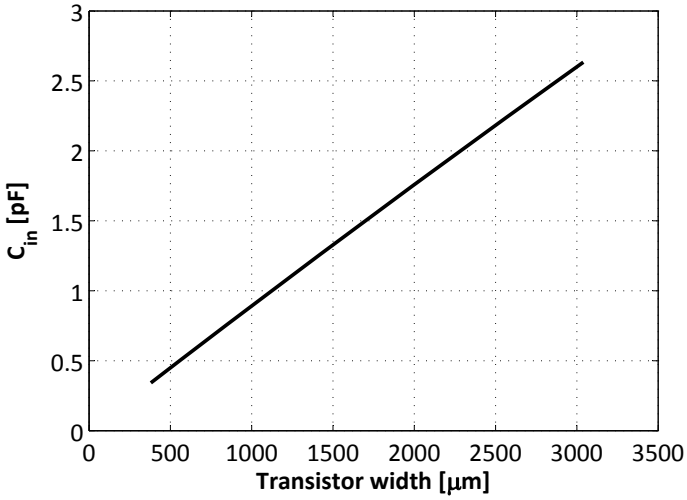


Figure 5.21: Input capacitance as a function of the transistor width (1.2 V NMOS transistor, $V_{GS} = 0\,V$).

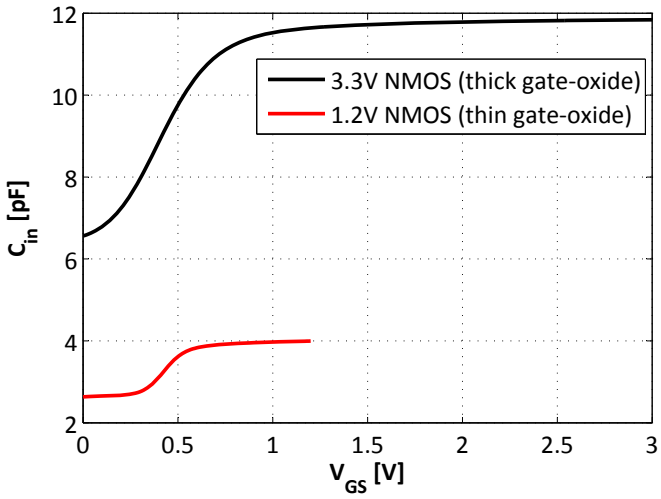


Figure 5.22: Input capacitance as a function of the gate-source voltage (1.2 V NMOS transistor, $V_{DS} = 0\,V$).

transistor.

The input capacitance is proportional to the transistor gate area. The relation between the input capacitance and transistor width is shown in Fig. 5.21.

The input capacitance versus the V_{GS} voltage is shown in Fig. 5.22. It can be seen that the C_{in} increases sharply at the transition between the weak and strong inversion. This is because by increasing the V_{GS} voltage the channel charge increases rapidly and it dominates over the depletion charge.

It can be seen that the input capacitance is changing significantly with the input voltage V_{GS}. The non-ideal class-E PA will also exhibit the Miller effect. Furthermore,

from the driver design perspective it is important to know how much current in given time is needed to be delivered to the gate (to charge it) in order to turn the power transistor ON. Because of highly non-linear nature of the gate capacitance the concept that uses gate charge rather that gate capacitance is adopted for the switch device specification. This approach is described in Subsection 5.3.2.

5.3.1.3 Output capacitance

The total drain capacitance is very important design parameter because it directly influences operation of the class-E PA. Common practice is to set the width of the power transistor so that the calculated shunt capacitance C_p of the class-E PA is fully absorbed by the output capacitance of the NMOS transistor.

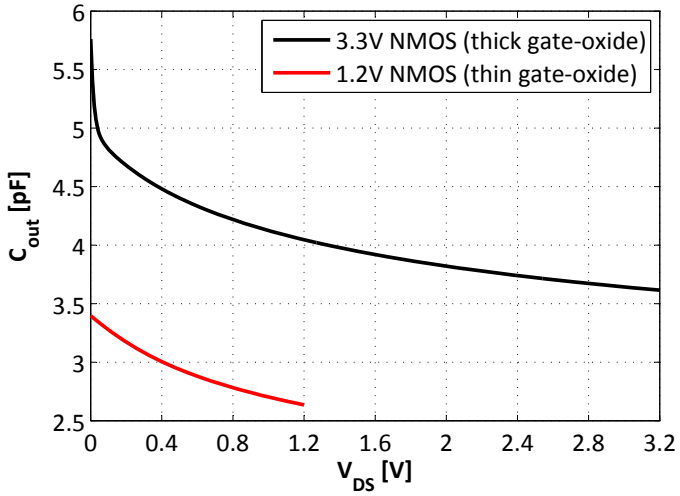


Figure 5.23: Output capacitance versus the drain-source voltage of a standard (1.2 V NMOS) and thick gate-oxide (3.3 V NMOS) device ($V_{GS} = 0\,V$).

The output capacitance of the transistor consists of

$$C_{out} = C_{DG} + C_{DB} + C_{DS} \approx C_{DG} + C_{DB} \tag{5.9}$$

The output capacitance depends strongly on the drain-source voltage because C_{DB} represents the drain-bulk PN junction capacitance. C_{DB} is highest at low V_{ds} voltages.

The total output capacitance versus the drain-source voltage for each thin and thick gate-oxide transistors is shown in Fig. 5.23. In the class-E PA the output capacitance in the OFF state is the most important. Therefore the simulations are performed using $V_{GS} = 0\,V$. This simulation can be used only as a guidance to get an insight on the size of the output capacitance. The output capacitance of the cascode topology in the OFF state depends on the V_{casc} and this is not considered in the simulations in this subsection.

The figures 5.24 and 5.25 show the capacitance values of each component described by Eq. (5.9) for 1.2 V NMOS and 3.3 V NMOS transistor respectively. It can be seen

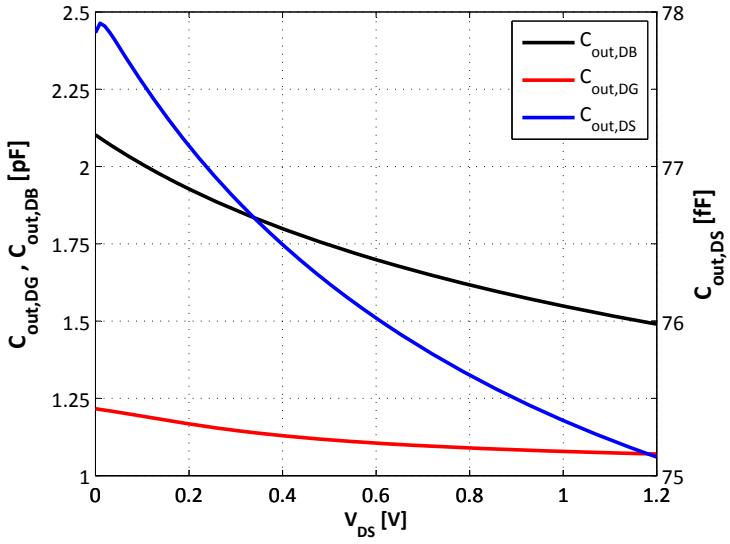


Figure 5.24: Output capacitance components versus the drain-source voltage of a standard (1.2 V NMOS) transistor ($V_{GS} = 0\,V$).

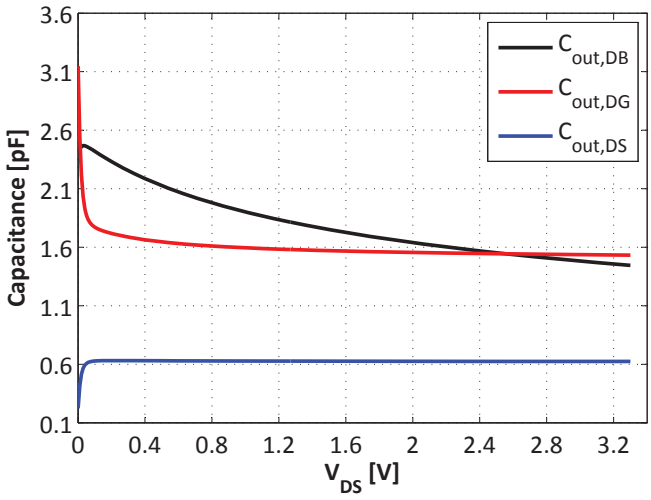


Figure 5.25: Output capacitance components versus the drain-source voltage of a thick gate-oxide (3.3 V NMOS) transistor ($V_{GS} = 0\,V$).

that the dominant capacitance in both cases is $C_{out,DB}$ capacitance. This PN junction capacitance decreases when V_{ds} is increasing as it was predicted. The second largest capacitance is $C_{out,DG}$ that is basically voltage independent capacitance. The smallest of all is the drain-source capacitance $C_{out,DS}$ (it is non-zero when the transistor is in the OFF state). Note that $C_{out,DS}$ in Fig. 5.24 is plotted versus the right y-axis.

The output capacitance is directly proportional to the transistor area. The simulated output capacitance as function of the transistor width for both transistors types in the

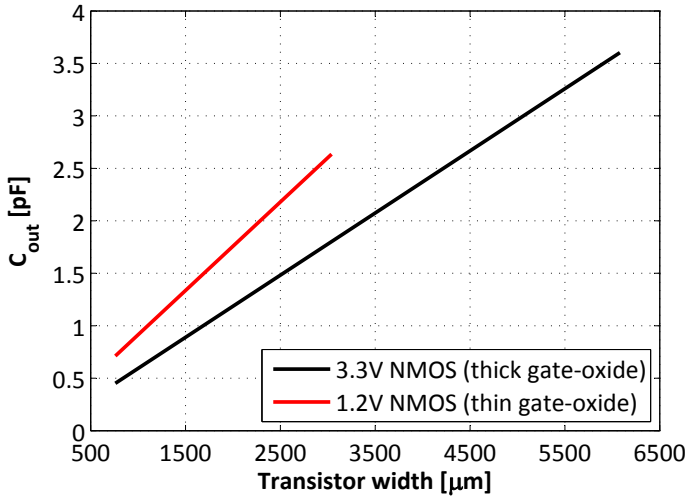


Figure 5.26: Output capacitance as a function of the transistor width of a standard (1.2 V NMOS, $V_{DS} = 1.2\,V$) and thick gate-oxide (3.3 V NMOS, $V_{DS} = 3.3\,V$) device ($V_{GS} = 0\,V$)

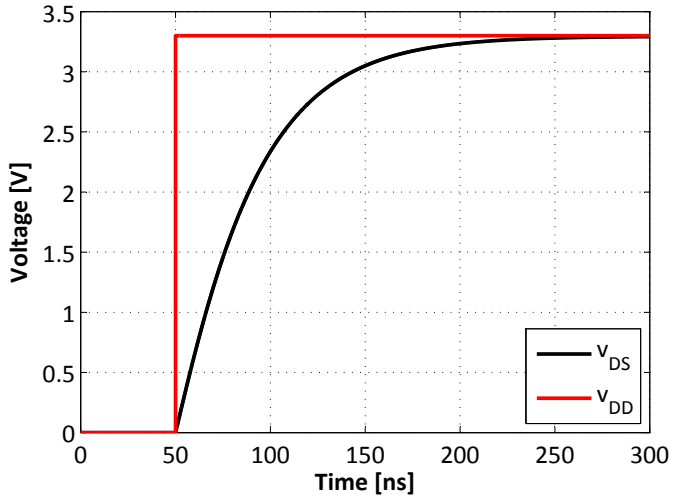


Figure 5.27: Drain voltage of the transistor as a response to the supply voltage step. Thick gate-oxide (3.3 V NMOS) device ($V_{GS} = 0\,V$), $R_{DD} = 10\,k\Omega$.

OFF state is shown in Fig. 5.26.

Another way to characterize the output capacitance of the power transistor is to derive it from the transistor step response. This technique is usually referred to as *effective output capacitance* calculation ($Coss$). As it shown in Fig. 5.23 the output capacitance is highly voltage dependent. Therefore, the effective output capacitance concept is introduced for switch devices (designers also work with an average capacitance over the whole drain-source voltage range, take only the highest value ($V_{DS} = 0\,V$) or the capacitance value at the selected V_{DS} point). $Coss$ is defined as a capacitance that will

have identical charging time as the output capacitance of a MOSFET at V_{DS} equal 80 % of V_{DD} ($V_{GS} = 0\,V$). Based on practical experience the 80 % V_{DD} is usually selected when the output capacitance is used as the part of the output resonant circuit (like in class-E PA).

In this method the output capacitance of the NMOS is charged from the power supply through the resistor R_{DD} to V_{DD}. $Coss$ is calculated from the time (t_c) it takes the drain voltage v_{DS} to reach 80 % of the V_{DD}. The drain voltage can be calculated using the equation for RC charging as

$$v_{DS}(t) = V_{DD}\left(1 - e^{\left[\frac{-t_c}{R_{DD}Coss}\right]}\right) \tag{5.10}$$

and $Coss$ can be expressed as

$$Coss = -\frac{t_c}{R_{DD}\ln\left(1 - \frac{V_{DS,80}}{V_{DD}}\right)} \tag{5.11}$$

where $V_{DS,80}$ is the v_{DS} voltage at 80 % of the V_{DD}.

Fig. 5.27 shows the simulated transistor drain voltage as a response to the supply voltage step from zero to the maximum $V_{DD} = 3.3\,V$ (3.3 V NMOS transistor). It also shows RC charging case. The supply voltage step occurs at time 50 ns. Using Eq. 5.11 $Coss$ is calculated as follows

$$\begin{aligned} V_{DS,80} &= 2.64\,V \\ t_c &= 64.2\,ns \\ Coss &= 3.989\,pF \end{aligned} \tag{5.12}$$

The effective output capacitance can be used to calculate more accurate output network circuit parameters of the class-E amplifier. It is used in the resonant network calculations instead of the static output capacitance.

5.3.2 Driving requirements

Due to the feedback path between the gate and drain of the transistor the effective dynamic input admittance is larger than the sum of the static gate capacitances due to Miller effect. The standard AC simulation setup of the input capacitance does not include the Miller effect and therefore the input capacitance is smaller than the input capacitance with Miller effect. The Miller effect takes place only within certain range of V_{gs}. In order to estimate the input capacitance with Miller effect the gate charge concept has to be used.

The gate charge is defined as the total charge that has to be supplied to the transistor gate either to swing the gate voltage by a given amount or to achieve full switching.

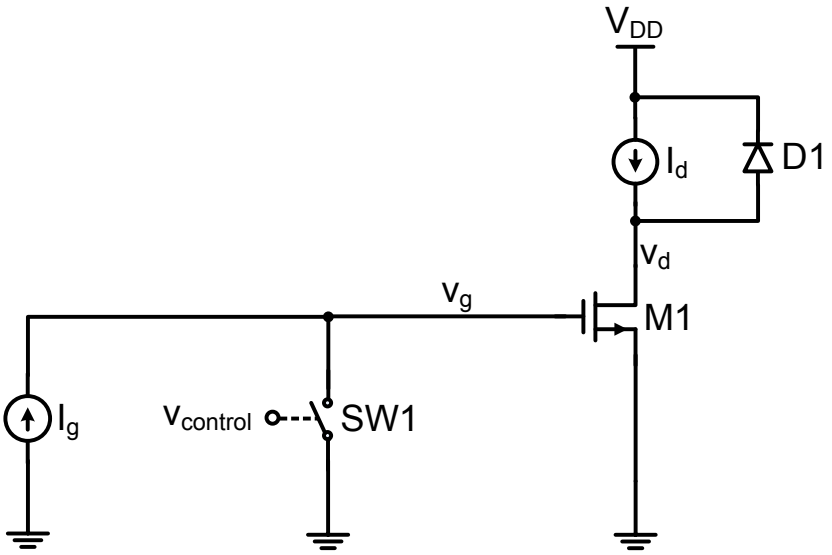


Figure 5.28: Basic gate charge test circuit.

In this work the latter definition is used. The basic gate charge test circuit is shown in Fig. 5.28. The gate of the NMOS transistor is charged from the current source with chosen current (I_g). The current source starts to charge the gate at the instance the switch turns OFF ($t = 0\,\text{ns}$).

The gate charge waveform of the 1.2 V NMOS transistor for two different drain-source voltages is shown in Fig. 5.29. Because the I_g is constant the gate charge (Q_g) can be calculated as

$$Q_g = I_g t_4 \tag{5.13}$$

where t_4 corresponds to the time when the gate-source voltage reaches the maximum allowed value. The total equivalent gate capacitance C_g calculated from the gate charge waveform for selected maximum gate voltage can be calculated as

$$C_g = \frac{Q_g}{V_g} \tag{5.14}$$

where $Q_g = C_g V_g$.

Note that the instantaneous gate capacitance changes in time according to the gate charge curve and its instantaneous deviation from the average capacitance C_g might be high. The gate charge and the total equivalent gate capacitance of the thin gate-oxide transistor can be calculated from Fig. 5.29 (for $V_{DS} = 1.0\,\text{V}$) using

$$\begin{aligned} t_4 &= 5.08\,ns \\ I_g &= 1\,mA \\ V_g &= 1.2\,V \end{aligned} \tag{5.15}$$

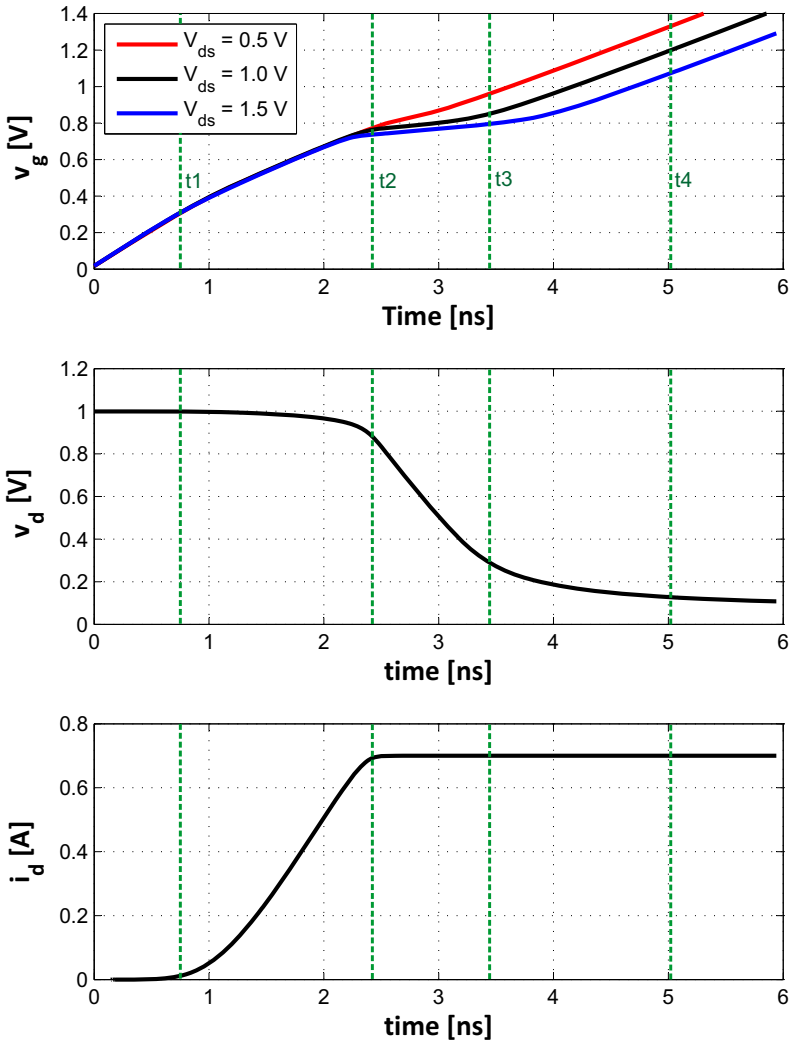


Figure 5.29: Gate charge gate and drain waveforms (1.2 V NMOS). The waveforms v_d and i_d and markers t1-t4 are at $V_{ds} = 1.0\,V$.

and finally we obtain

$$\begin{aligned} Q_g &= 5.08\,pC \\ C_g &= 4.25\,pF \end{aligned} \tag{5.16}$$

The calculated equivalent gate capacitance is significantly higher than the input capacitance simulated in Fig. 5.19 ($C_{in} = 2.6\,pF$).

When the switch SW1 is open ($t = 0$ ns) the gate voltage V_g increases and the gate

current drive is only charging the input capacitance of the transistor in its OFF state. No current flows in the drain until the gate voltage reaches the threshold voltage at $t1$. The time $t1$ can be approximately calculated as

$$t1 = \frac{CinV_T}{I_g} \tag{5.17}$$

where $C_{in} = C_{GS} + C_{GD}$ in the OFF state (see Subsection 5.3.1.2), V_T is the transistor threshold voltage and I_g is the gate charging current. All the current of the bias current source I_d is taken by the diode D1. The effect of the parasitic gate resistance R_g for this concept is negligible.

After $t1$ C_{GS} continues to charge (and C_{DG} discharge) and the drain current begins to increase. This process continues until the i_d reaches the maximum available drain current I_d. At the time $t2$ the drain voltage begins to decrease. The drain current remains constant. At this point the V_{GS} is large enough to support the drain current and the gate current I_g is diverted to discharge the C_{GD} capacitance. If the driver is not capable to supply enough current required to discharge C_{DG}, v_d voltage fall will be slowed down and this will increase the total turn-ON time.

In the time period between $t2$ to $t3$ v_g stays relatively constant but v_d falls to a value given by $V_{ds,sat}$. The high drain-gate voltage swing results in high capacitive current according to

$$i_{C_{GD}} = C_{GD}\frac{d\,v_{DS}}{d\,t} \tag{5.18}$$

This increases the requirements on the PA driver that has to deliver extra current in relatively short time.

After the time $t3$ the gate voltage is no longer constrained by the transfer characteristic of the device and v_g starts to increase until in reaches the maximum allowable switching voltage (in Fig. 5.29 it is 1.2 V). The Miller effect diminishes because of the voltage gain of the transistor is reduced due to the divice entering the linear region.

It is important to note that the gate charge is temperature insensitive but it changes with the drain current and drain-source voltage. The plateau voltage increases slightly with increasing drain current due to the necessity of higher g_m (V_{gs} has to increase). The plateau voltage is directly proportional to the threshold voltage.

The main advantage of using the gate charge (besides that it includes the large signal Miller effect) is that it can be used to calculate the current required from the PA driver to turn ON the switch transistor within a given time. These calculations would not be possible with simple input capacitance value. The gate charge can be used to calculate the required gate charging current as

$$I_g = Q_g t_{charge} \tag{5.19}$$

Another method can use the gate charge to calculate required output impedance of the driver. Assuming the PA driver has a finite output impedance ($R_{drv,ON}$) and the gate

has non-zero series resistance (R_g) then we can write

$$t_{charge} = (R_{drv,ON} + R_g)C_g TC \tag{5.20}$$

$$R_{drv,ON} = \frac{t_{charge}}{(C_g TC)} - R_g \tag{5.21}$$

where TC is the number of time constants.

An important question has to be answered: Is the Miller effect really a problem in the class-E PA? In the ideal class-E PA that fulfills the ZVS condition there is no voltage present at the drain of the power switch at the instance the switch turns ON. Therefore, ideal class-E PA does not suffer from Miller effect. The simulated drain voltage curves of the switching transistor in the cascode class-E PA were shown in Fig. 5.8. It can be seen that the drain voltage of the switch can be as high as 1 V when the switch turns ON. Therefore, the cascode class-E PA can be affected by Miller effect. This is in detail investigated in the next subsection.

Practical implementation of the class-E PA usually does not fully satisfy the ZVS condition because a more optimal circuit performance can be obtained [Grebennikov & Sokal 2007]. The Miller effect will cause switching loss because there is an instantaneous voltage and current present between $t1$ to $t3$ in Fig. 5.29.

The input capacitance, calculated from the gate charge, can be used to better estimate the power loss in the PA driver stage. The power loss analysis due to the gate capacitance charging is straightforward. The power loss in the driver circuit associated with the gate capacitance charging process during the turn-ON period is $P_{diss,ON}$. The power loss when the power transistor goes OFF and the energy of the gate capacitor has to be discharged is $P_{diss,OFF}$. This can be mathematically written as

$$P_{diss} = P_{diss,ON} + P_{diss,OFF} = 2\,(\frac{1}{2}C_g V_g^2 f_s) \tag{5.22}$$

$$P_{diss} = Q_g V_g f_s \tag{5.23}$$

where f_s is the switching frequency. The simulated power dissipation associated with the charging and discharging of the gate capacitance of the power transistor using the C_{in} and C_g versus the power transistor width is shown in Fig. 5.30.

5.3.3 Cascode circuit

In this subsection the behavior of the cascode connected power transistors is investigated. The cascode connected power transistor schematic that is used for the simulations in this subsection is shown in Fig. 5.31.

The nominal size of the transistors is the same as in the previous subsection. The standard 1.2 V NMOS thin gate-oxide transistor has the maximum nominal terminal voltage of 1.2 V and its nominal size is 3040 μm/0.12 μm. The 3.3 V NMOS thick gate-oxide transistor has the maximum nominal terminal voltage of 3.3 V and its nominal size 6080 μm/0.32 μm.

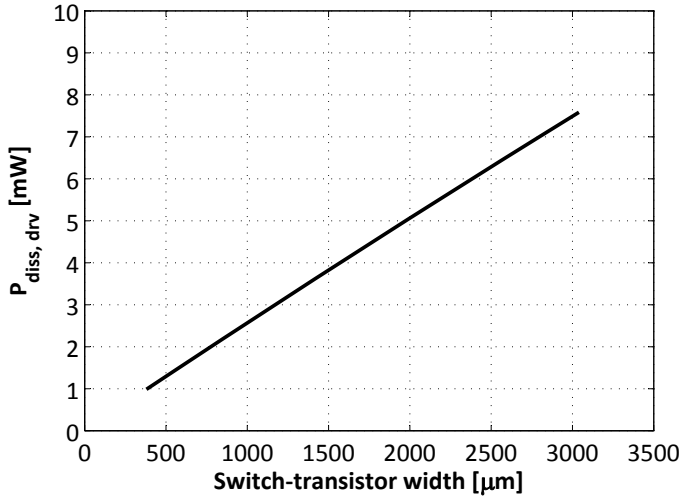


Figure 5.30: Power dissipation due to the gate charging and discharging versus the width of the power transistor (1.2 V NMOS). C_g represent the equivalent input capacitance calculated from the gate charge waveform (at $V_g = 1.2\,V$) and C_{in} is the input capacitance when the transistor is OFF.

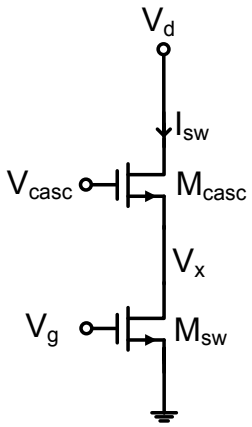


Figure 5.31: Schematic of the cascode topology.

5.3.3.1 DC behavior

The current through the cascode versus the cascode drain voltage is shown in Fig. 5.32. Both transistors in the cascode are ON and have maximum gate voltages with the voltage drop at the peak current (0.7 A) of approximately 0.4 V. The target is to have the drain voltage as close to zero as possible in order to minimize the power loss in the ON RF cycle.

Fig. 5.33 shows the DC current and gate-source voltage of M_{casc} transistor versus V_{casc}. It can be seen that the current through the cascode is linearized. This is because of the negative feedback that is created by the ON resistance of the switch transistor connected to the source of the M_{casc} transistor. The M_{sw} transistor is in the linear

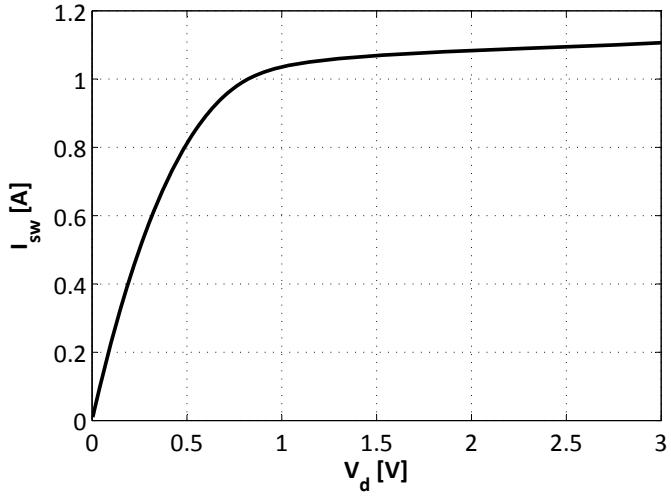


Figure 5.32: Current through the cascode (I_{sw}) versus drain voltage (V_d), $V_g = 1.2\,V$ and $V_{casc} = 1.8\,V$.

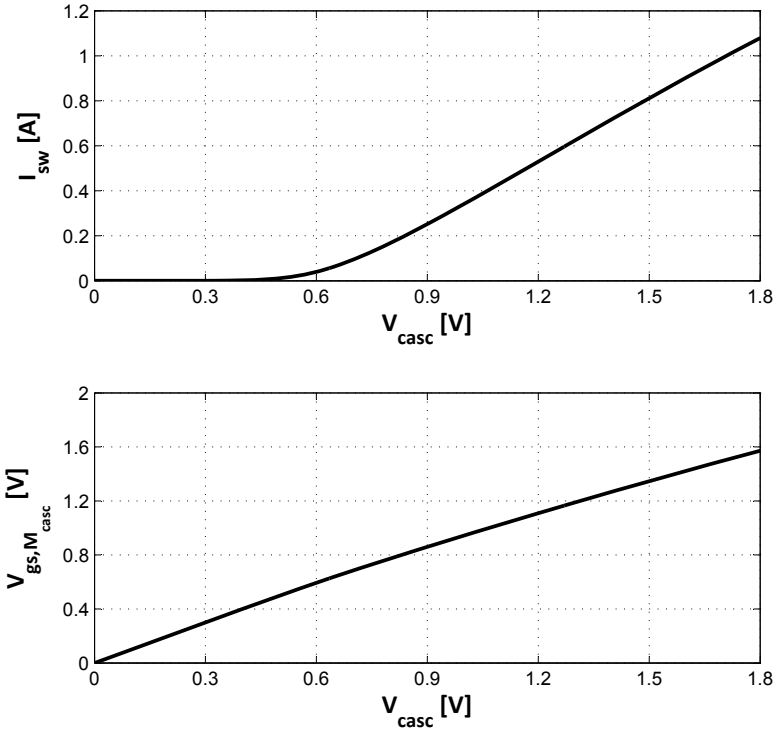


Figure 5.33: Current through the cascode (I_{sw}) and gate-source voltage of the cascode transistor ($V_{gs,M_{\mathrm{casc}}}$) versus V_{casc} voltage, $V_g = 1.2\,V$ and $V_d = 1.8\,V$.

region for the entire range of V_{casc}.

The peak cascode current during the RF operation of the class-E PA is limited to 0.7 A (this is result of the chosen supply voltage and output load impedance). Therefore,

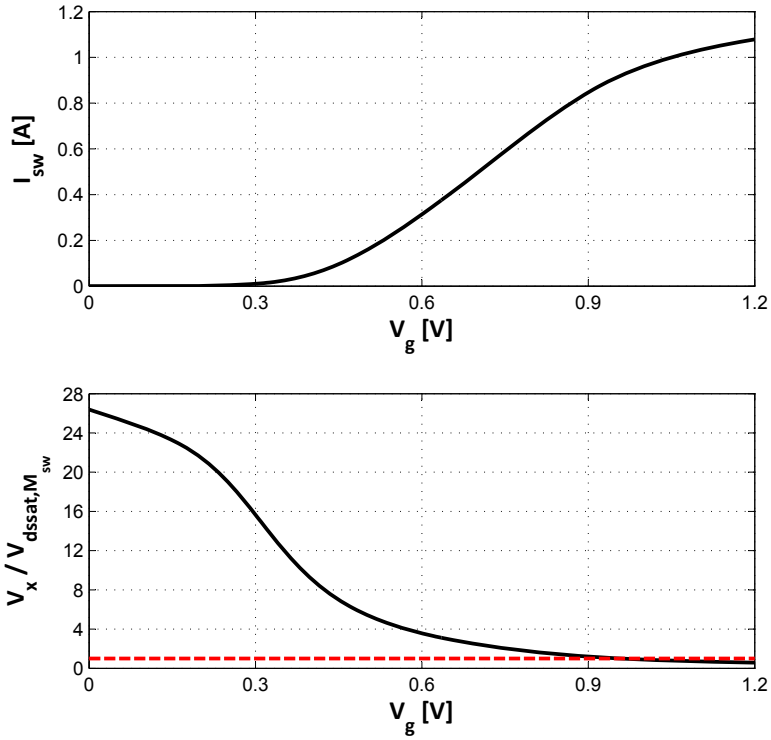


Figure 5.34: Current through the cascode (I_{sw}) and saturation parameter versus V_g voltage of the M_{sw} transistor, $V_{casc} = 1.8\,V$ and $V_{d,max} = 1.8\,V$. The red line indicates the border between the linear and saturation regions.

once the M_{casc} drain current reaches this value the cascode transistor operates in the linear region. This behavior of the cascode class-E PA can be observed from the RF based simulations (Section 5.2).

Fig. 5.34 shows the DC current and saturation parameter of M_{sw} transistor versus V_g voltage. The current through M_{sw} as a function of V_g voltage reveals that the M_{sw} transistor will operate in the saturation for the low gate voltage levels ($V_g < 0.95\,V$). M_{sw} enters the linear region ($V_x \,/\, V_{dssat,M_{sw}} < 1$ in Fig. 5.34) if the V_g is higher than 0.95 V.

5.3.3.2 Gate charge

A very important parameter of the transistors sizing is the equivalent total input capacitance. This can be calculated from the gate charge curves. First we will examine the gate charge curve of the M_{casc} transistor. The cascode connected transistors are biased with current $I_{sw} = 0.7\,A$. The gate voltage of the M_{sw} transistor is 1.2 V, The simulated gate charge plot is shown in Fig. 5.35. The parameter is the drain voltage V_d. The test circuit is the same as in Fig. 5.28 but the single transistor is replaced by the cascode connected transistors. The simulated conditions (V_d voltage) are based on Fig. 5.6. It can be seen that the drain voltage V_d is a function of V_{casc} and V_{casc} controls the current.

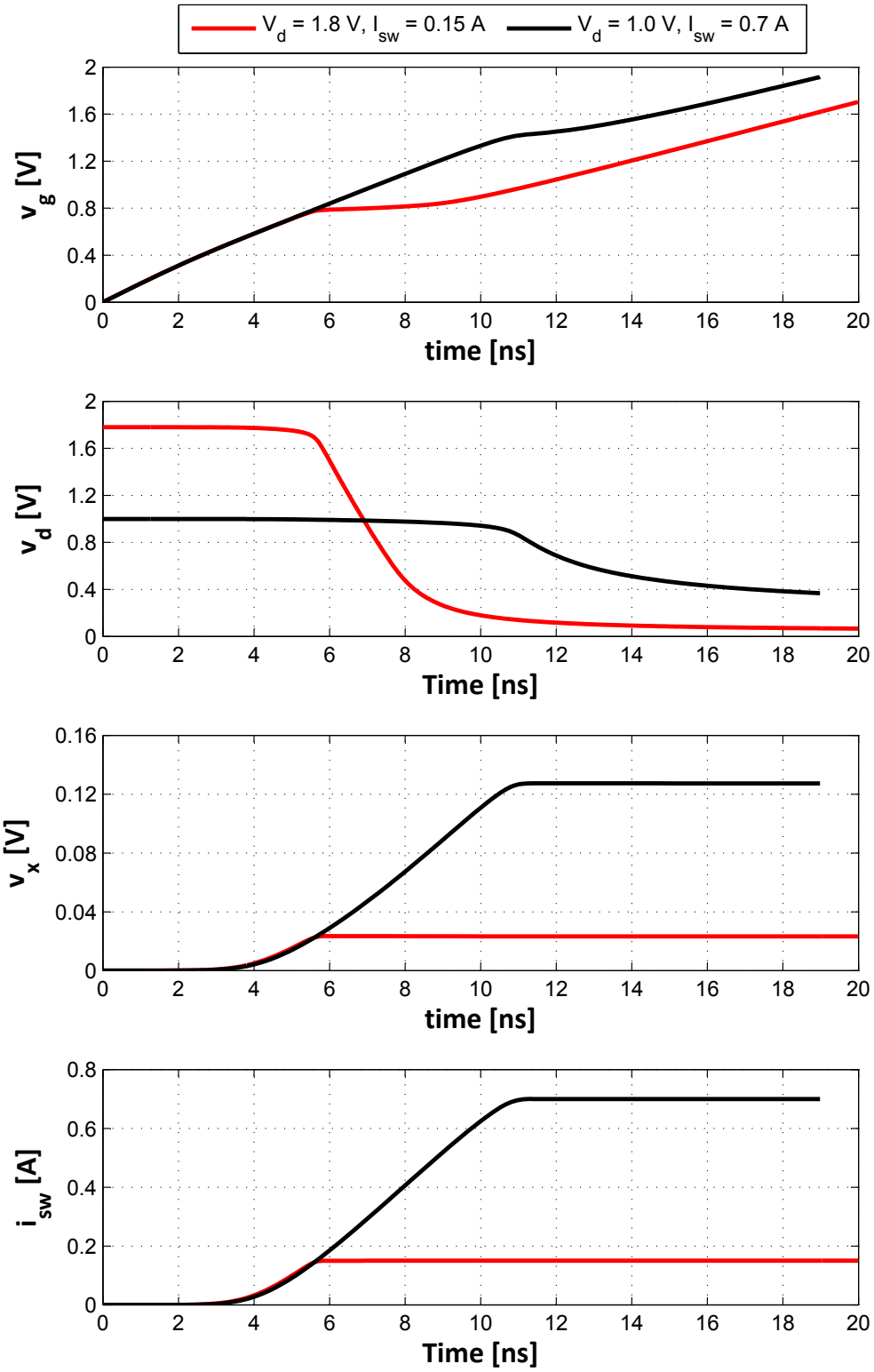


Figure 5.35: Gate charge waveform (v_g) of the M_{casc} transistor connected in the cascode topology and the drain voltage of the M_{casc} (v_d) and M_{sw} (v_x) transistors. The parameter is V_d voltage ($V_g = 1.2\,V$).

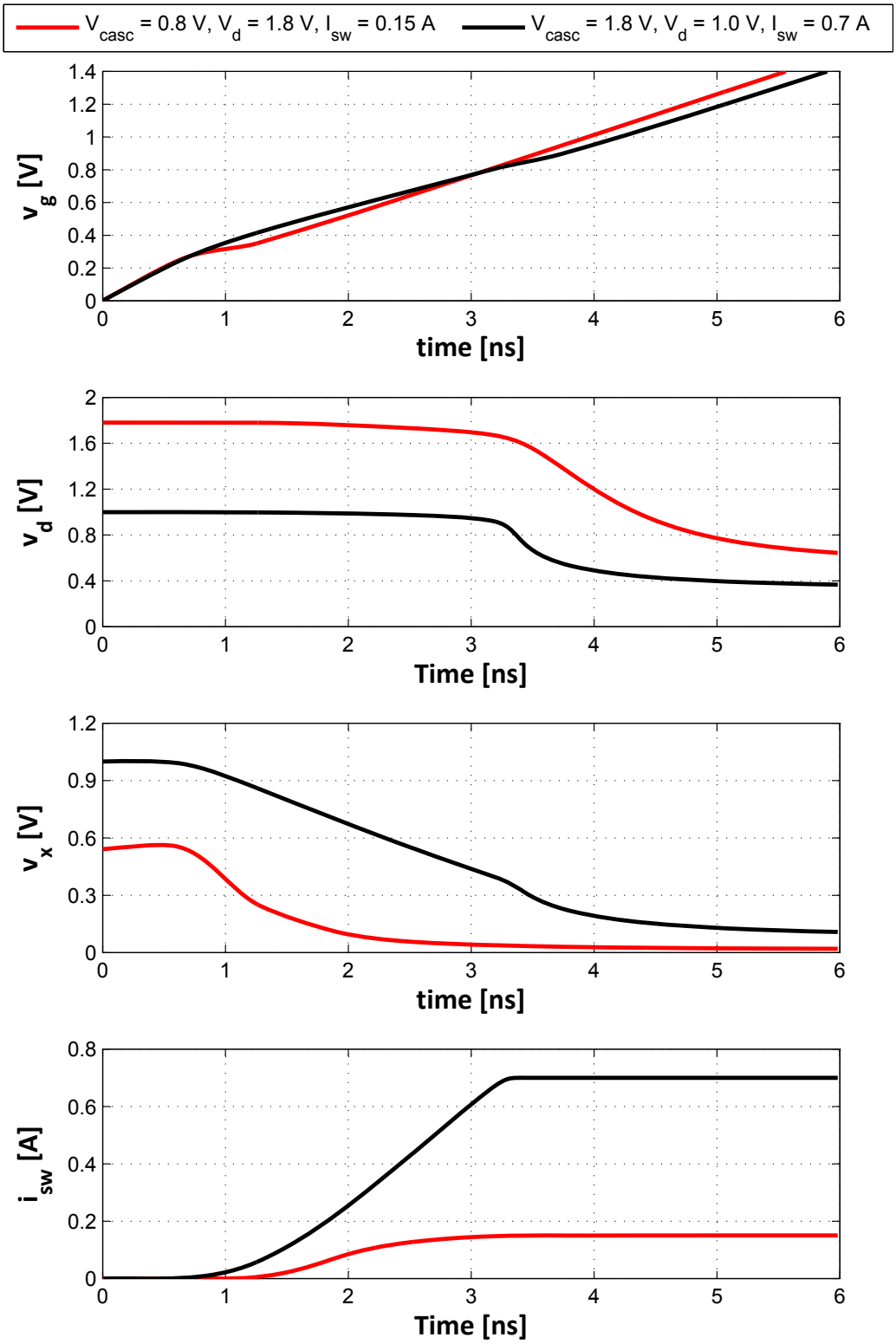


Figure 5.36: Gate charge waveform (v_g) of the M_{sw} transistor connected in the cascode topology and the drain voltage of the M_{casc} (v_d) and M_{sw} (v_x) transistors. The parameter is V_{casc} voltage (with associated I_{sw} and V_d).

The characterization of the input capacitance is rather complex process (because the parameters of the cascode topology are cross-dependent). For simplicity two states are examined $V_{casc} = 1.8\,V$ and $V_{casc} = 0.8\,V$. In the first case $V_d = 1\,V$ and $I_{sw} = 0.7\,A$ and in the second case $V_d = 1.8\,V$ and $I_{sw} = 0.18\,A$ (for reference see Fig. 5.6 and Fig. 5.7). From Fig. 5.35 it can be seen that the Miller effect is present in both curves. For the black curve the target v_g is 1.8 V and for the red one it is 0.8 V. In the black curve v_g (what represents V_{casc}) increases from zero, crosses threshold voltage, reaches the gate voltage needed to draw 0.7 A drain current, goes through the Miller plateau and finally it reaches 1.8 V in 18 ns. In the red curve the M_{casc} transistor stays in the Miller plateau (transistor is in the saturation) and the target v_g of 0.8 V is reached in approximately 8 ns. The gate charge should not be calculated from 0 ns but from the time that corresponds to the lowest V_{casc} utilized during the cascode class-E PA operation ($V_{casc} = 0.4\,V$ corresponds to 2.5 ns). The worst case driving requirement represents the case of highest V_{casc}.

The same simulation is performed for the M_{sw} transistor. From the simulated curves in Fig. 5.36 it can be seen that the Miller effect in the M_{sw} transistor is negligible. This is because of the cascode transistor that shields the M_{sw} transistor. The rapid change of V_d voltage is not reflected on the V_x node. The Miller effect is active only if the drain-source voltage of the transistor is high after the drain current reached the peak value. In case of M_{sw} transistor v_x voltage falls down simultaneously with the increase of the drain current i_{sw}. At the point where i_{sw} reaches the target value, v_x is already low. This minimizes the Miller effect. The target V_g value of 1.2 V is reached in both cases approximately in 5 ns.

5.3.3.3 Capacitance

The input capacitance calculation can be performed based on the gate charge waveforms. In this subsection we will summarize the effect of the V_{casc} on the input and output capacitance. From Fig. 5.37 it can be seen that the input capacitance seen at the input of the M_{sw} transistor is approximately constant. The cascode transistors are OFF and $V_d = 0\,V$, what represents the state when the class-E PA turns ON.

The output capacitance of the cascode connected transistors seen at the drain of the M_{casc} transistor is plotted in Fig. 5.38. The figure shows the output capacitance as a function of both V_{casc} and V_d voltage. The output capacitance changes significantly with V_{casc} if the V_d is below 1 V.

The explanation for this behavior is straightforward. The voltage in the common node V_x is floating and the drain voltage V_d is fixed. Therefore, the source and drain terminals of the M_{casc} transistor exchange their functions. The channel in the M_{casc} transistor is formed when the gate-drain voltage is larger than the threshold voltage. When the M_{casc} transistor is OFF (no channel is formed) the output capacitance seen from the drain terminal is simply the sum of the overlap capacitance $C_{DG,ov}$ and PN junction drain-bulk capacitance C_{DB}. The dominant is the junction capacitance and it is independent of the V_{casc} voltage.

Once the drain-gate voltage is larger than the threshold voltage the transistor is in

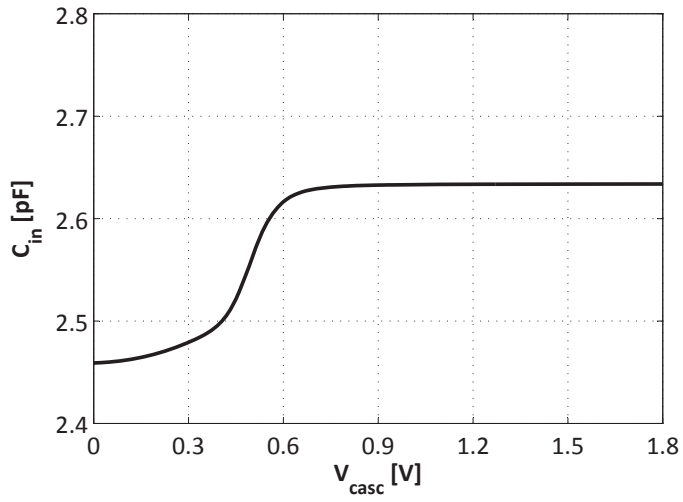


Figure 5.37: Input capacitance seen at the gate of the M_{sw} transistor versus the V_{casc} voltage. The cascode is OFF, $V_g = 0\,V$ and $V_d = 0\,V$.

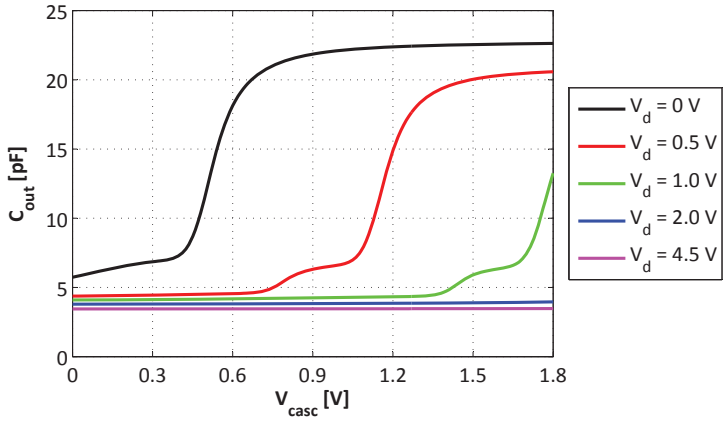


Figure 5.38: Cascode output capacitance seen at the drain of the M_{casc} transistor versus the V_{casc} voltage. The parameter is V_d voltage. The cascode is OFF ($V_g = 0\,V$).

strong inversion and the channel below the gate is formed. This significantly changes the circuit operation. The drain and source diffusions are conductively connected. The drain-bulk capacitance is now much higher than in was in the M_{casc} transistor OFF state. The effective area of the PN junction includes now drain, channel and source regions. The drain-gate capacitance also increases because the intrinsic capacitance of the gate has to be accounted for (compared with only overlap capacitance before). The last mentioned effect that occurs when M_{casc} transistor is in the strong inversion causes that the output capacitance of the switch will contribute to the output capacitance of the cascode. This is because the conductive channel connects the drain and source of the M_{casc} transistor and this reveals the output capacitance of the M_{sw} transistor

(when M_{casc} is OFF, the output capacitance of the switch transistor was not seen from V_d terminal because the drain and source of the M_{casc} transistor are isolated).

To summarize the behavior of the output capacitance of the cascode, the output capacitance significantly increases when the channel is formed in the M_{casc} transistor. This occurs when the drain-gate voltage is larger than the threshold voltage. In practical operation the output capacitance should not be considered constant because in the OFF period of the RF cycle the drain voltage changes from a minimal value ($v_{d,sat}$) to the peak value ($3.6V_{DD}$).

5.3.3.4 ON resistance and Drain efficiency

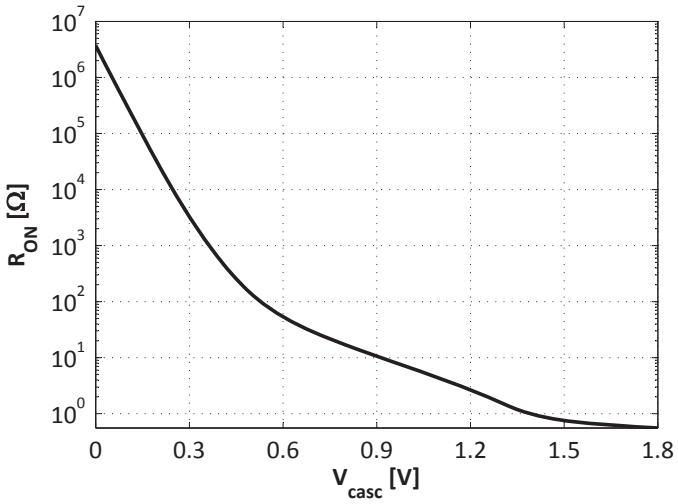


Figure 5.39: ON resistance of the cascode versus the V_{casc} voltage ($V_g = 1.2\,V$). The cascode is biased by voltage source with $V_{DD} = 4.5\,V$ and $R_{DD} = 6\,\Omega$.

The ON resistance of the cascode topology determines the overall efficiency of the class-E PA. The ON resistance as a function of the V_{casc} voltage is plotted in Fig. 5.39. The cascode is biased by a voltage source with $V_{DD} = 4.5\,V$ and $R_{DD} = 6\,\Omega$. The resistor R_{DD} represents the load of the cascode and this setup provides a highest drain current (I_{sw}) of 0.7 A. It can be seen that the cascode ON resistance has three distinguished regions. For approximately $V_{casc} < 0.5\,V$ the transistor is OFF, $0.5\,V < V_{casc} < 1.4\,V$ the M_{casc} transistor is in saturation and for $V_{casc} > 1.4\,V$ the M_{casc} transistor enters the triode region. This is the reason the ON resistance has three different slopes.

The ON resistance as a function of the cascode current (both transistors are ON and highest gate voltage is applied) is shown in Fig. 5.40. The ON resistance of the cascode increases rapidly when $I_{sw} > 0.8\,A$ because the cascode enters the saturation region. This is in agreement with simulation in Fig. 5.32.

Fig. 5.41 and Fig. 5.42 show the ON resistance as a function of the M_{casc}/M_{sw} and M_{sw}/M_{casc} ratio respectively. It can be seen that in order to keep the combined ON

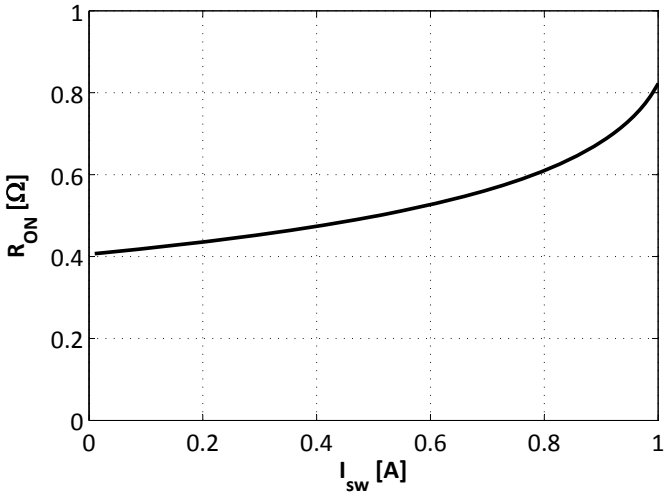


Figure 5.40: ON resistance of the cascode versus the cascode current I_{sw} ($V_{casc} = 1.8\,V$ and $V_g = 1.2\,V$).

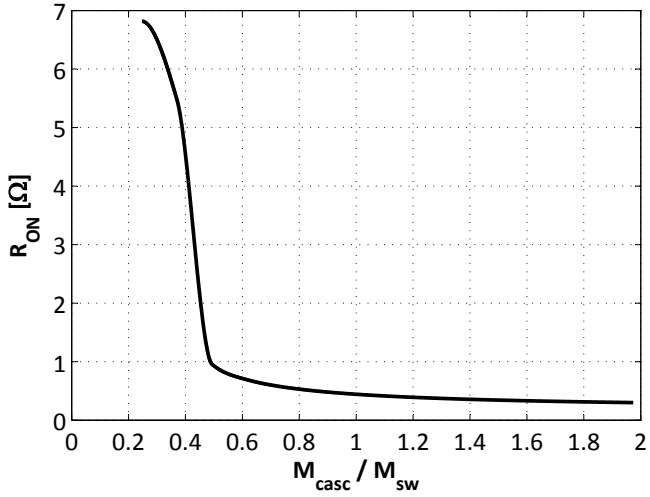


Figure 5.41: ON resistance of the cascode versus M_{casc} to M_{sw} transistors W/L ratio. The W/L of the M_{sw} transistor is fixed (W = 3040 μm, L = 0.12 μm). The length of the M_{casc} transistor is 0.32 μm. The gate voltages are $V_{casc} = 1.8\,V$, $V_g = 1.2\,V$ and the cascode current is $I_{sw} = 0.7\,A$.

resistance below 1 Ω the W/L ratio of the M_{casc} transistor has to be at least half of the W/L ratio of the M_{sw} transistor. Or if the M_{casc} transistor dimensions are fixed, then the W/L ratio of the M_{sw} transistor has to be at least 0.7 times of the W/L ratio of the M_{casc} transistor. Too high M_{casc}/M_{sw} or M_{sw}/M_{casc} W/L ratio does not decrease the ON resistance but the driving requirements are high due to the increased equivalent input capacitance.

The sizing of the cascode transistors can start from selecting the W/L of the M_{casc}

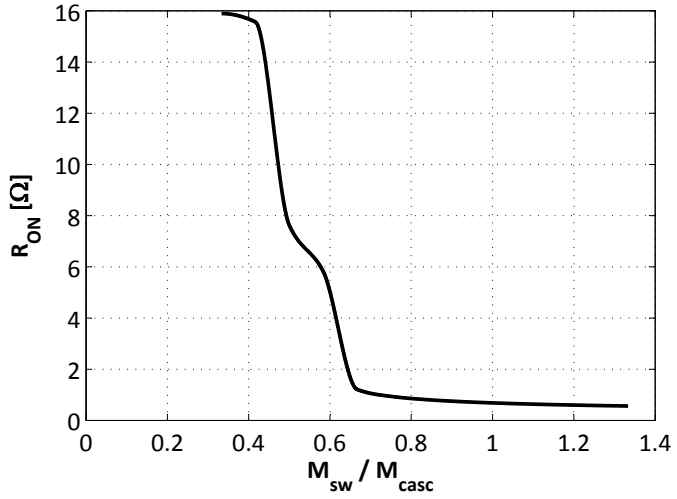


Figure 5.42: ON resistance of the cascode versus M_{sw} to M_{casc} transistors W/L ratio. The W/L of the M_{casc} transistor is fixed (W = 6080 μm, L = 0.32 μm). The length of the M_{sw} transistor is 0.12 μm. The gate voltages are $V_{casc} = 1.8\,V$, $V_g = 1.2\,V$ and the cascode current is $I_{sw} = 0.7\,A$.

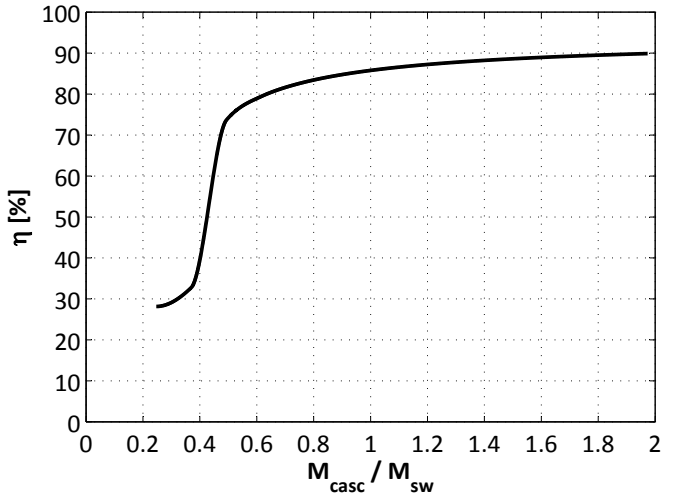


Figure 5.43: Calculated drain efficiency of the cascode class-E PA as a function of the M_{casc} to M_{sw} transistors W/L ratio. The W/L of the M_{sw} transistor is fixed (W = 3040 μm, L = 0.12 μm). The length of the M_{casc} transistor is 0.32 μm. The gate voltages are $V_{casc} = 1.8\,V$, $V_g = 1.2\,V$ and the cascode current is $I_{sw} = 0.7\,A$.

transistor so that the class-E shunt capacitance is fully implemented by the output capacitance of the M_{casc} transistor. The size of the M_{sw} transistor can be selected with respect to the ON resistance of the cascode.

The ON resistance directly influences the drain efficiency as was shown before. The calculated drain efficiency of the cascode class-E PA based only on the finite ON

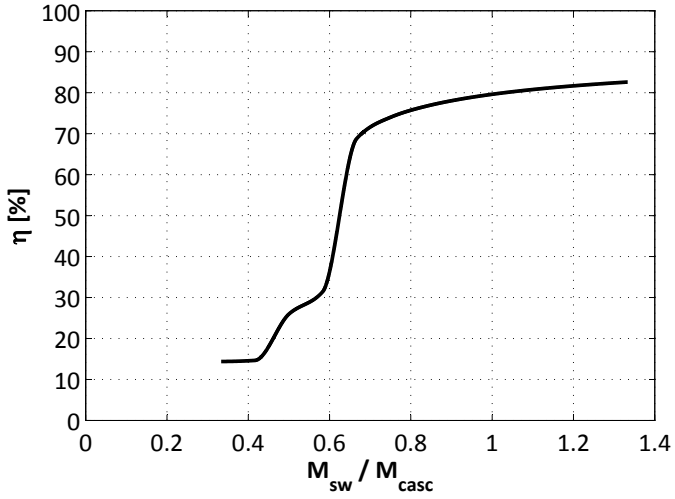


Figure 5.44: Calculated drain efficiency of the cascode class-E PA as a function of the M_{sw} to M_{casc} transistors W/L ratio. The W/L of the M_{casc} transistor is fixed (W $= 6080\,\mu$m, L $= 0.32\,\mu$m). The length of the M_{sw} transistor is $0.12\,\mu$m. The gate voltages are $V_{casc} = 1.8\,V$, $V_g = 1.2\,V$ and the cascode current is $I_{sw} = 0.7\,A$.

resistance as a function of the M_{casc}/M_{sw} and M_{sw}/M_{casc} ratios respectively is shown in Fig. 5.43 and Fig. 5.44. The drain efficiency calculated from the ON resistance can better illustrate the influence of the size of the cascode transistors on the class-E PA. It is obvious that there is a trade-off between the drain efficiency increase and input capacitance increase as a function of the transistor sizes.

Note that the nominal sizes of the cascode transistors used in this chapter give $M_{casc}/M_{sw} = 0.75$ or $M_{sw}/M_{casc} = 1.33$ ratios. The size of the M_{casc} transistor was designed with respect to the class-E shunt capacitance as was described above. An interesting observation is that M_{sw} transistor could be 30 % smaller and the absolut drain efficiency would drop only by 5 % points. The larger M_{casc} would increase the drain efficiency but that would lead to deviation from the ideal class-E operation. This will overall consequently leads to decreased efficiency due to the instantaneous cascode voltage and current overlap.

5.3.4 Modulation BW

One of the main advantages of the cascode modulation technique is that the envelope signal has no BW limitation due to the supply modulator. It is therefore interesting to examine the modulation BW of the proposed PA. For this simulation a circuit envelope analysis is used. The envelope signal applied to the cascode gate terminal can be expressed as $v_{casc} = 1.6\,V + 0.1\cos(\omega_m t)$. The small signal AC tone has a swept frequency (ω_m) and it is superimposed on the DC signal. RF, in signal is a single tone signal with amplitude of 1.2 V. The simulation schematic is shown in Fig. 5.45.

In Fig. 5.46 can be seen that the 3dB BW is approximately 30 MHz. That is much larger than the BW of state-of-the-art switch-mode DC-DC supply modulators. On the

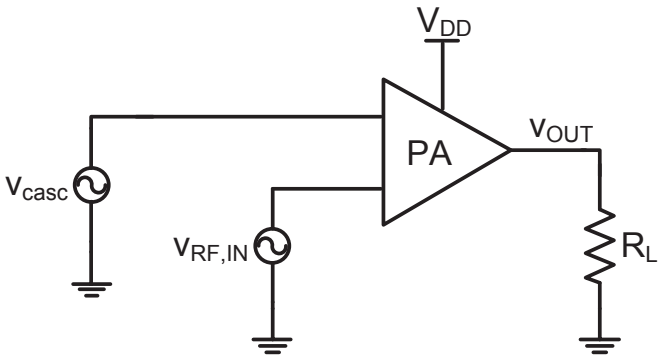


Figure 5.45: Schematic of BW simulation. The PA is single stage cascode modulated class-E PA. Load resistor $R_L = 3.74\,\Omega$.

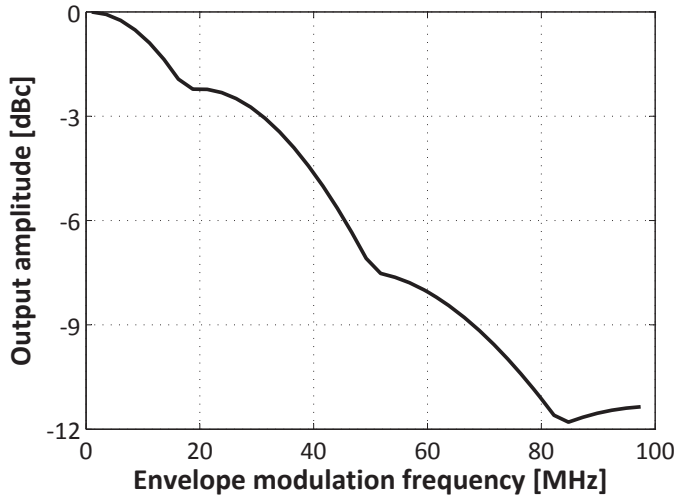


Figure 5.46: Simulated frequency response of the cascode modulated class-E PA (modulation BW is normalized to 1 MHz response).

other hand LTE polar PA needs to have a modulation BW of at least 60 MHz in order to amplify 20 MHz LTE signal (taking into account the amplitude BW regrowth of a polar TX). The conclusion is that the cascode modulation concept is suitable for amplifying signals that have complex IQ BW up to 10 MHz.

5.3.5 Process and temperature variation

The effect of temperature variation on the cascode modulated class-E PA performance is shown in Fig. 5.47 and Fig. 5.48.

One can see that the influence of the temperature on the output power is significant. For practical implementation of the cascode modulated class-E PA suitable type of temperature compensation needs to be developed.

The output power versus the V_{casc} voltage is shown in Fig. 5.49 and Fig. 5.50. The

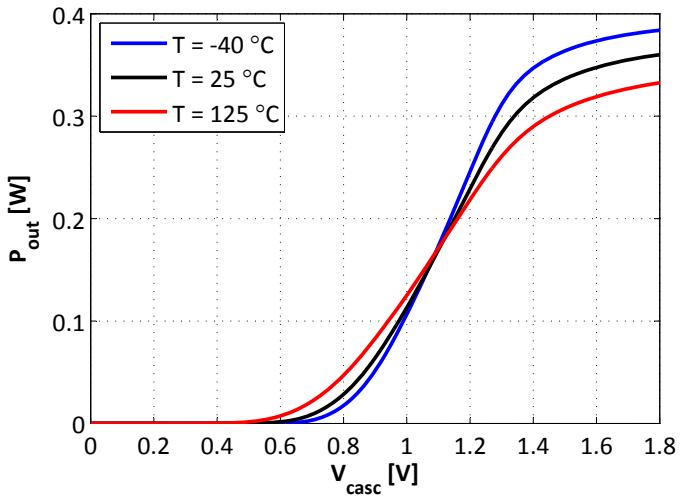


Figure 5.47: Simulated available fundamental output power delivered to the 50 Ω load versus the cascode voltage V_{casc} and temperature.

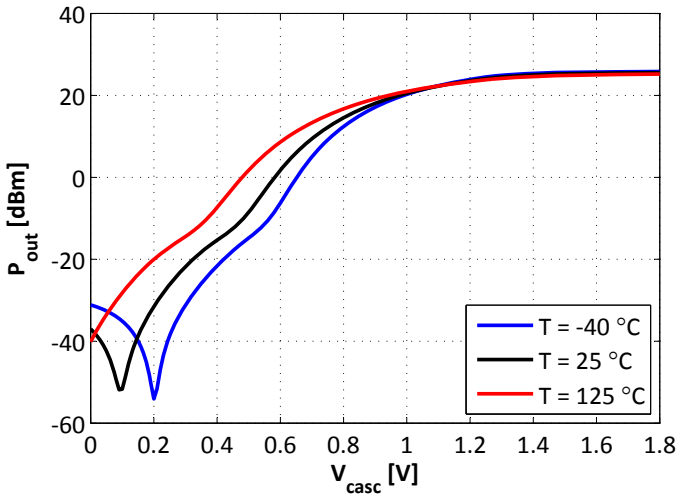


Figure 5.48: Simulated available fundamental output power in dBm delivered to the 50 Ω load versus the cascode voltage V_{casc} and temperature.

parameter is the CMOS process variation. It can be seen that the there is a noticeable variation of the output power with the CMOS process corners. The worst case can be obtained as a combination of both temperature and process variations.

5.4 Cascode modulation and adaptive supply voltage

One of the main problems of the cascode modulated class-E PA is decreased drain efficiency at low power levels compared to the supply modulated class-E PA. The mech-

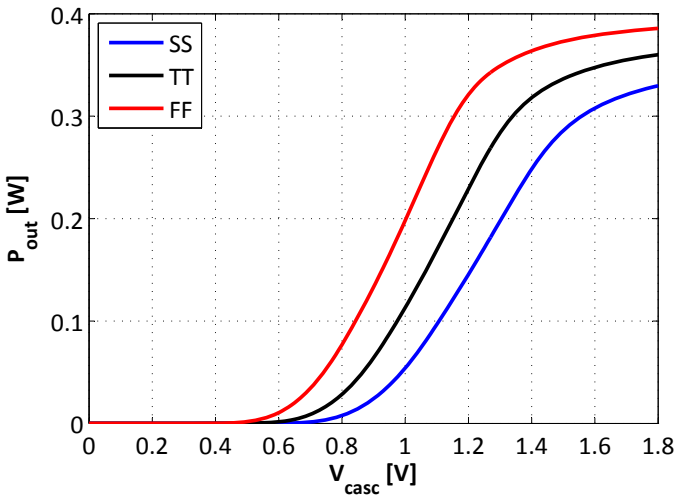


Figure 5.49: Simulated available fundamental output power delivered to the 50 Ω load versus the cascode voltage V_{casc} and and CMOS proces variation. Process options: SS = Slow, TT = Typical, FF = Fast.

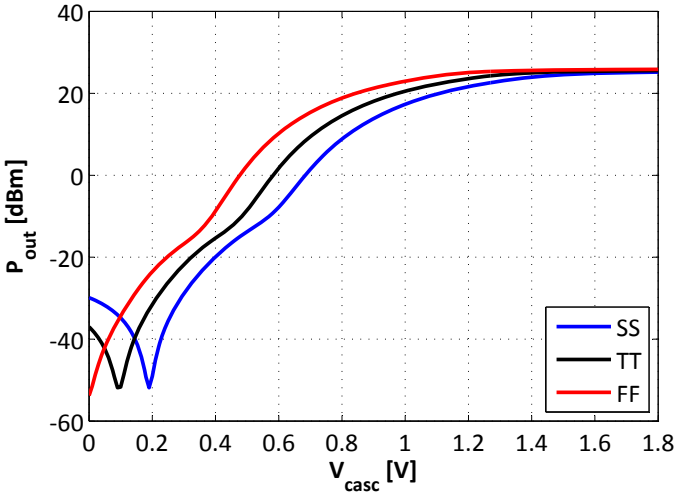


Figure 5.50: Simulated available fundamental output power in dBm delivered to the 50 Ω load versus the cascode voltage V_{casc} and CMOS proces variation. Process options: SS = Slow, TT = Typical, FF = Fast.

anism behind this was discussed before. Simply said, the drain voltage of the cascode modulated class-E PA increases up to the V_{DD} at low V_{casc} voltages (Fig. 5.6). On the contrary, the drain voltage of the supply modulated class-E PA remains low when the supply voltage is low (Fig. 5.9).

One possible way to improve the efficiency of the cascode modulated class-E PA is to also vary the supply voltage according to V_{casc} voltage. The idea behind is that when the V_{casc} is low, the output power is also low and the supply voltage can be decreased.

Therefore, the efficiency at low V_{casc} levels would significantly increase.

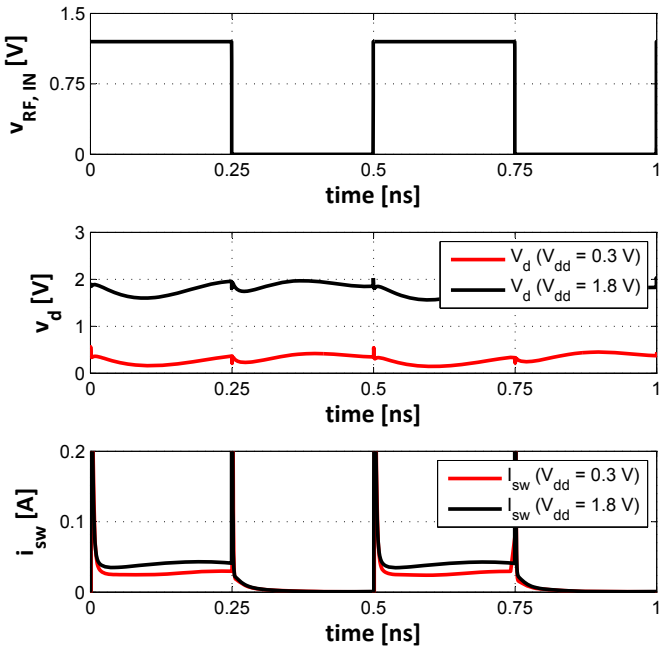


Figure 5.51: RF input voltage ($V_{RF,IN}$), drain voltage (V_d) and cascode drain current (i_{sw}) versus time ($V_{casc} = 0.6\,V$, $V_g = 1.2\,V$). The parameter is power supply V_{dd} voltage.

To verify this concept simulations of the cascode class-E PA with adaptive supply voltage were performed. The cascode class-E PA waveforms are shown in the figure Fig. 5.51. The black set of curves represent the cascode class-E PA without adaptive supply voltage ($V_{casc} = 0.6\,V$ and $V_{DD} = 1.8\,V$). The red curves belong to the decreased supply voltage ($V_{DD} = 0.3\,V$). It can be seen that the drain voltage v_d during the ON period is significantly decreased and therefore the power dissipation also significantly decreases.

The direct effect of the adaptive supply voltage on the drain efficiency of the cascode class-E PA is shown in Fig. 5.52. The drain efficiency at low V_{casc} level ($V_{casc} = 0.6\,V$) is only 3.8 % at nominal supply voltage. It can be increased up to 18.4 % if the supply voltage is decreased to 0.15 V.

The variation of the supply voltage has undesired effect on the output power because the output power is directly related to the supply voltage. The output power in the cascode class-E PA is primarily controlled by the V_{casc} voltage. By decreasing the supply voltage the output power will also decrease. This effect is plotted in Fig. 5.53. If the supply voltage is controlled by the power control signal that is much slower than the amplitude modulated signal then the undesired influence of the adaptive supply voltage on the output power can be cancelled by linearization (digital predistortion).

The simultaneous modulation of both supply voltage and the cascode voltage of

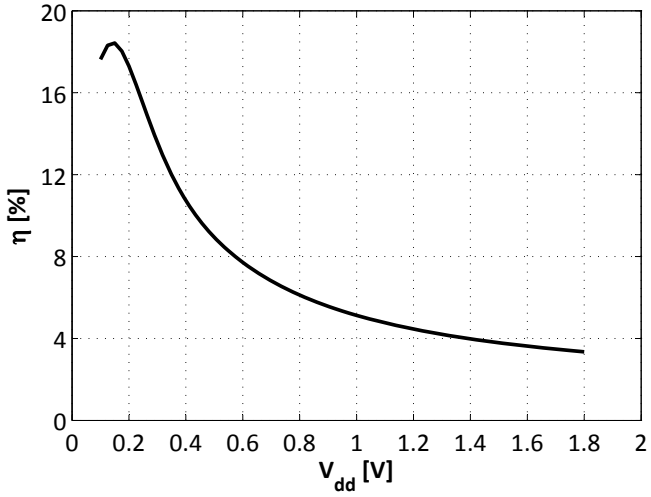


Figure 5.52: Drain efficiency versus the DC supply voltage ($V_{casc} = 0.6\,V$, $V_g = 1.2\,V$).

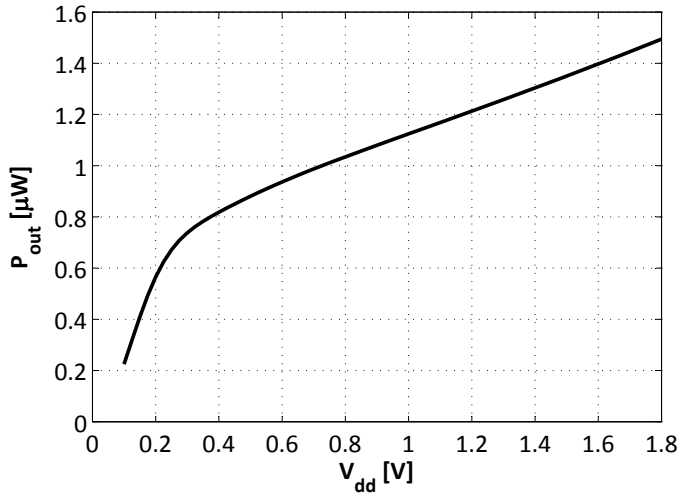


Figure 5.53: Output power versus the DC supply voltage ($V_{casc} = 0.6\,V$, $V_g = 1.2\,V$).

the cascode modulated PA would lose the major advantage of the cascode class-E amplifier what is no need of an additional supply modulator. If the adaptive supply voltage is controlled by a slow power control signal then the requirements on the supply modulation are relaxed and a high efficiency cascode class-E operation can be achieved.

The cascode modulated class-E PA can be used in the polar transmitter where the amplitude modulated signal is applied to the V_{casc} and the power control signal (much slower) to the V_{DD}.

5.5 Reliability

The term reliability refers to the capability of the PA to maintain the output power and efficiency over an extensive period of time (several years). The reliability degradation has several causes.

The reliability of the CMOS PA is mainly limited by the gate oxide breakdown [Mazzanti *et al.* 2006] and the hot-carrier instability (HCI). If the voltage across the gate oxide exceeds certain limit (for given technology) the oxide rapture occurs. Oxide rapture causes a catastrophic and permanent damage [Yang *et al.* 2003].

HCI is a reliability issue that leads to threshold voltage and drain current shifts over time [Hu 1992]. The performance degradation at DC is caused by the channel hot-carrier effect when both the gate voltage and drain voltage are simultaneously high [Yuan & Ma 2008]. The dominant degradation at RF is due to Fowler-Nordheim or direct tunneling [Yuan & Ma 2008]. The main reliability issue for a properly designed class-E PA is the gate oxide breakdown [Mazzanti *et al.* 2006]. This can be explained as that in the ideal class-E operation there is no simultaneous overlap of high voltage and high current and therefore HCI can be neglected.

Usually, the recommended voltage is 10 % above the maximum allowed supply voltage to guarantee a product lifetime of ten years (given by the technology design rules). As the technology scales down the breakdown voltage is reduced as well.

In [Reynaert & Steyaert 2005] authors proposed a single transistor class-E output stage using a thick gate-oxide power transistor operated as a switch. The authors claimed improved reliability but they don't discuss the change in the RF performance of the switch. The conventional cascode topology using a regular gate-oxide transistors is limited by the breakdown of the cascode transistor [Sowlati *et al.* 2004].

The reliability challenge for a class-E RF PA comes from its inherently high drain voltage peaks (theoretically $3.6\,V_{DD}$ [Sokal & Sokal 1975]). The single transistor class-E PA with 1.8 V supply voltage exhibits 6.5 V drain voltage peaks.

In the cascode topology the drain voltage is divided between both transistors (M_{sw} and M_{casc} in Fig. 5.3). The drain voltage of the switch transistor M_{sw} is directly controlled by the V_{casc} voltage and it has to be kept below the recommended voltage. The supply voltage is limited by the gate-oxide breakdown of the transistor M_{casc}. Assuming that $V_{casc} = 1.8\,\text{V}$ and $V_{DD} = 1.8\,V$ then drain-gate voltage of M_{casc} is given by

$$V_{DG,M_{casc}} = V_d - V_{casc} \cong 3.5 \cdot 1.8\,V - 1.8\,V = 4.7\,V \tag{5.24}$$

The simulated voltages of the cascode transistors in the cascode class-E PA are shown in Fig. 5.54. The drain voltage (V_x) of the switch transistor is always below the nominal 1.2 V.

Note that there is a significant difference between the cascode controlled PA and a single transistor solution. In the cascode controlled PA the highest drain voltage peak occurs when the cascode voltage is highest ($V_{casc} = 1.8\,V$). The single transistor class-E PA drain voltage peak occurs when the gate voltage is low ($V_g = 0\,V$). Therefore, the drain-gate voltage stress in the cascode controlled PA is one supply voltage lower than

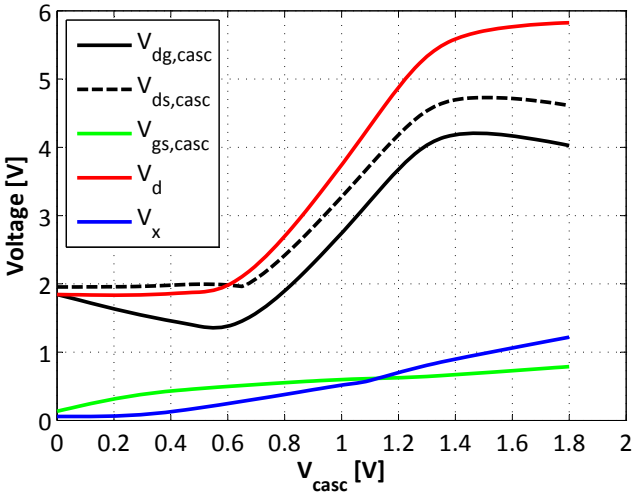


Figure 5.54: Simulated peak voltages of M_{sw} and M_{casc} transistors in the OFF period of the RF cycle versus the cascode control voltage V_{casc} ($V_{DD} = 1.8\,V$).

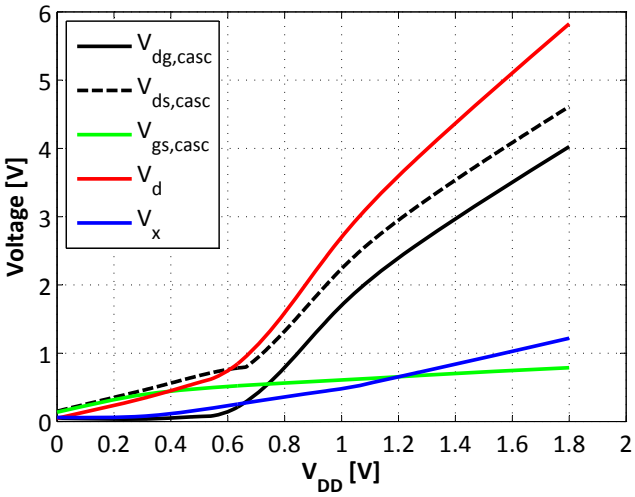


Figure 5.55: Simulated peak voltages of M_{sw} and M_{casc} transistors in the OFF period of the RF cycle versus the DC supply voltage V_{DD} ($V_{casc} = V_{DD}$).

in the single transistor class-E PA case.

The influence of the supply voltage variation on the cascode voltages is shown in Fig. 5.55. The voltages across the cascode transistor and the drain peak voltage are directly proportional to the V_{DD}.

Therefore, using the conventional cascode topology with the gate of the cascode tied to the DC supply voltage ($V_{casc} = V_{DD}$) will not solve the reliability problem.

One possibility to decrease the drain voltage peak is to use the finite RF choke technique. It was demonstrated that by using the finite RFC technique the peak drain voltage is reduced to $2.5\,V_{DD}$ [Yoo *et al.* 2001]. Therefore, if the supply voltage is

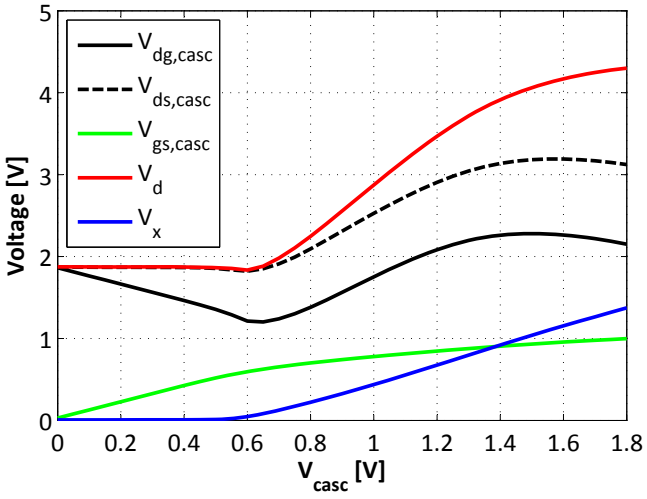


Figure 5.56: Simulated peak voltages of M_{sw} and M_{casc} transistors in the OFF period of the RF cycle versus the cascode control voltage V_{casc} ($V_{DD} = 1.8\,V$). The finite RFC technique is used.

1.8 V then the peak drain voltage is only 4.5 V. It is important to note that the finite RFC choke technique causes a deviation from the ideal class-E amplifier. The RFC becomes a design element of the class-E PA output network and the simple class-E design equations are no longer valid.

The simulated waveforms of the cascode class-E PA using the finite RFC technique are shown in Fig. 5.56. This simulation was performed using the two stage cascode class-E PA that was fabricated in 0.18 μm CMOS process. The measured results are discussed in the next chapter.

The drain-gate voltage of the cascode transistor is still higher than the recommended voltage of the regular gate-oxide transistor (1.2 V in 0.13 μm CMOS or 1.8 V in 0.18 μm CMOS technology). Therefore, the cascode transistor is made of the thick gate-oxide device (3.3 V NMOS device in both technologies). The reliability for low V_{casc} voltages is automatically satisfied, because with decreasing V_{casc} the drain voltage peak decreases as well (see Fig. 5.6). The thick gate-oxide cascode transistor is used to withstand the drain-gate voltage of 2.4 V.

This guarantees that the RF performance of the switch is maintained and the reliability is improved. By implementing the cascode transistor as a thick gate-oxide device the RF performance is not deteriorated as it would be in a case of thin gate-oxide transistor. In order to improve the reliability of class-E PAs the proposed cascode modulated class-E PA combines the cascode topology together with the finite RFC technique.

In the technology used for experimental work (0.18 μm CMOS) the nominal supply voltage is 1.8 V and the gate-oxide breakdown voltage is 3.5 V. The 0.34 μm thick gate-oxide transistors allow for a higher supply voltage of 3.3 V and the device gate-oxide breakdown voltage is increased to 6 V.

An additional benefit of the proposed topology is that the presence of the cascode

device reduces the stress on the switch transistor and this way allows for about 0.5 V higher power supply voltage. This results in increased maximum PA output power or increased efficiency resulting from higher load impedance. The maximum V_{casc} voltage is given by the switch transistor maximum drain-gate what is in this case

$$V_{casc} = V_x + V_{GS,M_{\mathrm{casc}}} \cong 1.8 + 0.5\,V = 2.3\,V \tag{5.25}$$

The switch transistor gate-oxide breakdown occurs when the switch is OFF (Vg is low) and V_x is high (limited by V_{casc} that is changing slowly and can be considered constant for several RF cycles). Increasing V_{casc} voltage allows to increase the supply voltage as well. This allows to deliver higher output power to the same output load or allows to increase the load impedance and improve the efficiency. The upper limit on the V_{casc} voltage depends on the particular technology.

Chapter 6

The model of the cascode modulated class-E PA

Contents

This chapter discusses the modeling of the cascode modulated class-E PA. The model is not intended for precise and quantitative description of the cascode class-E PA but rather to describe the basic dependencies in the PA. The outcome of the modeling is qualitative description of the fundamental output power as function of the DC cascode voltage V_{casc}.

Modeling of the cascode amplifier is divided into three parts. Shown in the first step is that the fundamental output power is directly related to the peak drain current and to the DC current through the cascode. Two models that relate the drain current and cascode voltage, are proposed and analyzed by simulations in the next step. The last step is dedicated to finding analytical description of the model in order to quantitatively describe the V_{casc} and output power relation.

6.1 Drain current analysis

The model equations are based on the ideal class-E PA calculations that are derived in Chapter 4. The schematic of the cascode class-E PA is shown in Fig. 6.1. This topology is used in the RF simulations in this section. It is the same circuit (with the same circuit element values) as the one introduced in Section 5.2. The nominal conditions are $V_{DD} = 1.8\,V$ and $R_L = 3.74\,\Omega$.

An important assumption used in this section is that in order to analyze the relation between the output power and cascode voltage only the ON period of the RF cycle is considered. This is based on that in the OFF period the cascode is OFF and the output power is independent of the cascode voltage V_{casc}.

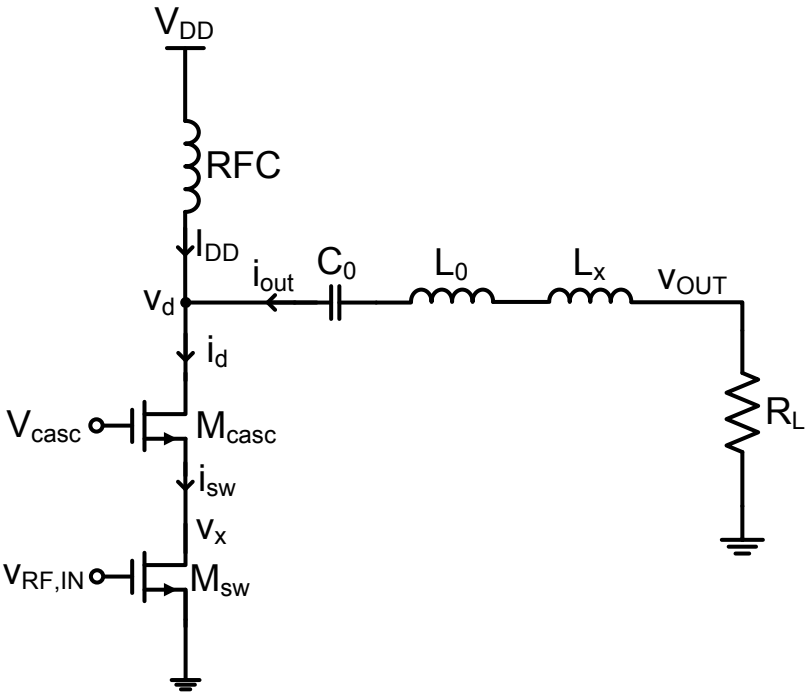


Figure 6.1: Schematic of the cascode class-E PA.

The steady state analysis of the cascode class-E PA starts with the study of harmonic content of the currents in the cascode topology. The drain I_d current as a function of V_{casc} voltage is plotted in Fig. 6.2. The drain current has a DC and fundamental components. The sum of these two components equals to the peak drain current obtained from the transient simulation. The small discrepancy is due to the non-zero (but practically negligible) second harmonic current component. The transient waveforms of the i_d current as a function of V_{casc} are shown in Fig. 6.3. Note that the current peaks don't occur at the same time but are slightly shifted. It can be also observed that the DC component of i_d current is a function of V_{casc} voltage.

The current through the switch transistor $\mathrm{M_{sw}}$ has different harmonic content compared to the I_d. From Fig. 6.4 it can be seen that the switch transistor current has significant 2nd and 3rd harmonic components (and even higher harmonics are still not negligible). The main reason for this is that the transistor operates as a switch. The cascode current I_d has only DC and fundamental harmonic components because the output capacitor of the cascode transistor ($\mathrm{M_{casc}}$) is a part of the tuned output resonant network. This current is a sum of two currents (through the switch and through the output capacitor). The magnitude of the fundamental component of I_d equals to the magnitude of the fundamental output current I_{out}.

The first step in the cascode class-E PA model development is to show that the output power of the PA can be calculated from the drain current through the cascode. The magnitude of the fundamental output current can be calculated from the peak

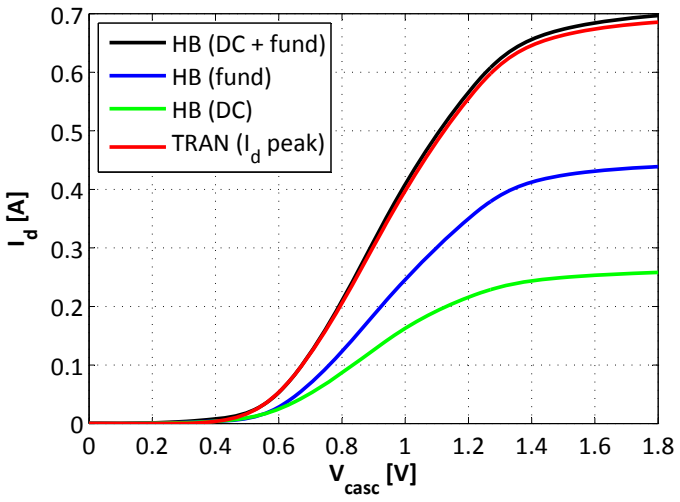


Figure 6.2: Harmonic content of the drain current I_d and transient drain current peak versus V_{casc} voltage.

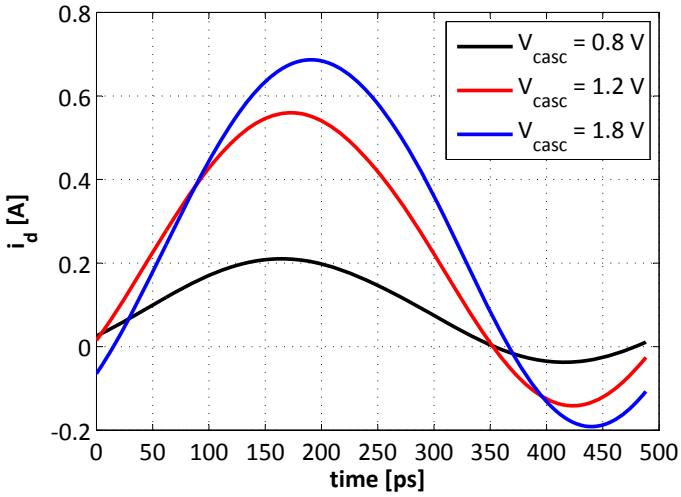


Figure 6.3: Drain current waveforms in the transient domain. The parameter is cascode voltage V_{casc}.

drain cascode current as (see Eq. (4.25))

$$I_{out} \doteq \frac{I_{d,peak}}{1.537} \doteq \frac{I_{d,DC} + I_{d,fund}}{1.537} \tag{6.1}$$

and the output power is simply calculated as

$$P_{out} = \frac{I_{out}^2}{2} R_L \tag{6.2}$$

The result of these calculations is shown in Fig. 6.5. The blue curve represents the

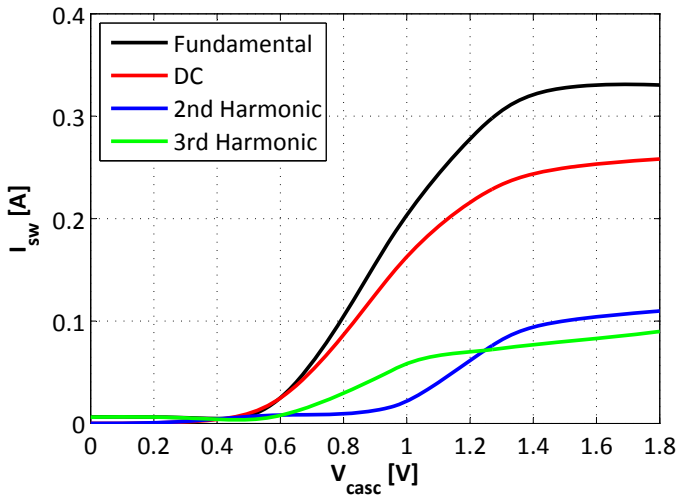


Figure 6.4: Harmonic content of the switch transistor current I_{sw} versus V_{casc} voltage.

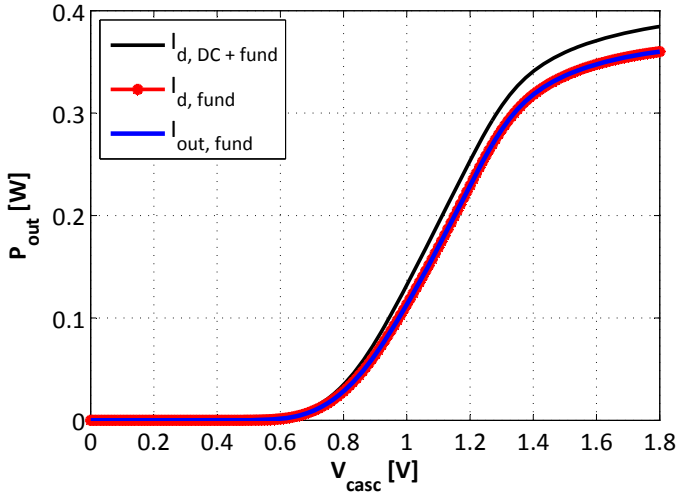


Figure 6.5: Available output power delivered to the load resistor versus the cascode voltage V_{casc}.

output power calculated directly from the output current. It can be seen that it is identical with the output power calculated from the fundamental component of the cascode drain current (red curve). The black curve shows the calculated output power based on Eq. (6.1). The calculated output power fits well simulated output power using I_{out}. The small discrepancy can be caused by various factors. The main reason is that Eq. (6.1) is only valid for an ideal class-E PA (lossless and no cascode topology). The peak discrepancy is for high values of V_{casc} and it is 7 %.

In order to investigate how the basic theoretical equations can predict the behavior of the cascode class-E PA the peak drain current and fundamental output current are

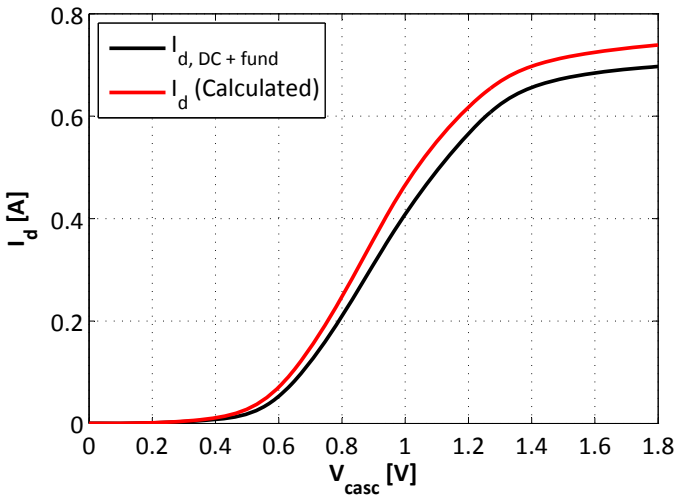


Figure 6.6: Comparison of simulated peak drain cascode current (black curve) and calculated peak drain cascode current based on the DC component of the drain current.

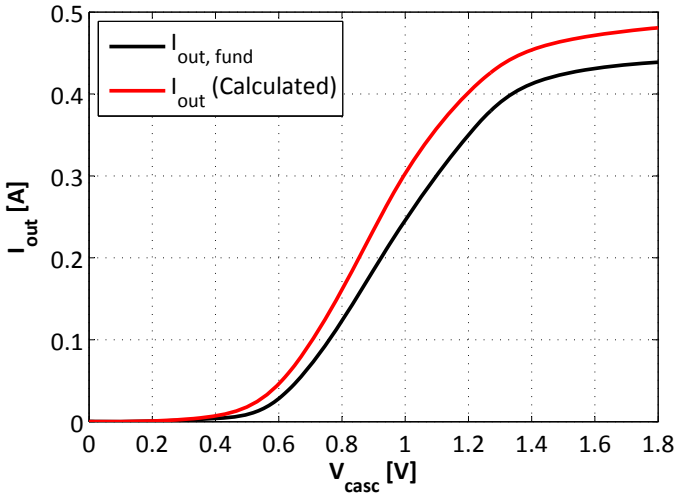


Figure 6.7: Comparison of simulated fundamental output current (black curve) and calculated fundamental output current based on the DC component of the drain current.

calculated based on the DC component of the drain current. The calculated waveforms are then compared with simulated ones. The peak drain cascode current can be expressed as (see Eq. (4.24))

$$I_{d,peak} \doteq 2.862 I_{DD} = 2.862 I_{d,DC} \tag{6.3}$$

The comparison of simulated and calculated peak drain currents is shown in Fig. 6.6.

The fundamental output current can be calculated using the DC component of the

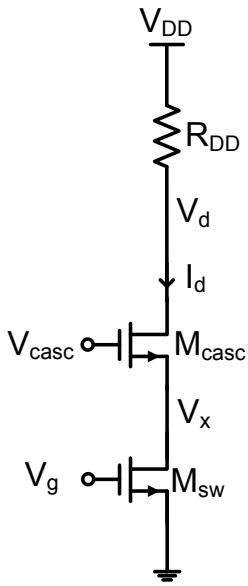


Figure 6.8: Schematic of the DC model of the cascode class-E PA using the equivalent DC supply resistance ($R_{DD} = 6.5\,\Omega$, $V_{DD} = 1.8\,V$, $V_g = 1.2\,V$).

drain cascode current as (see Eq. (4.19))

$$I_{out} \doteq \frac{I_{DD}}{0.537} = \frac{I_{d,DC}}{0.537} \tag{6.4}$$

This characteristic is plotted in Fig. 6.7 as a function of V_{casc} and compared with the simulated fundamental output current.

It can be seen that in both cases there is discrepancy between the calculated curves and the simulated ones. This indicates that the equations developed for ideal class-E PA do not provide perfect fit for a non-ideal cascode class-E PA. Despite that the results obtained by using them are reasonably close to the ideal case and therefore these calculations can still be used for simplified PA modeling.

6.2 Equivalent DC model

The next step after it was shown that the output power can be calculated directly from the drain cascode current is to obtain a DC model of the cascode class-E PA that reveals what is the relation between V_{casc} voltage and I_d.

The first approach presented in this subsection is based on the equivalent supply resistance seen from the supply terminal. The model should match the DC drain cascode current from the RF simulation with the DC simulated function. The schematic of the DC model is shown in Fig. 6.8. The only circuit element needed to be calculated is the

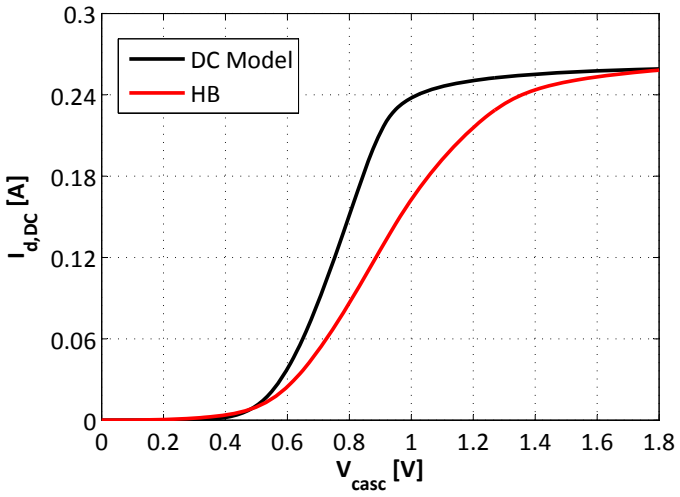


Figure 6.9: DC drain cascode current versus V_{casc} voltage. The parameter is the DC model and Harmonic Balance based simulation.

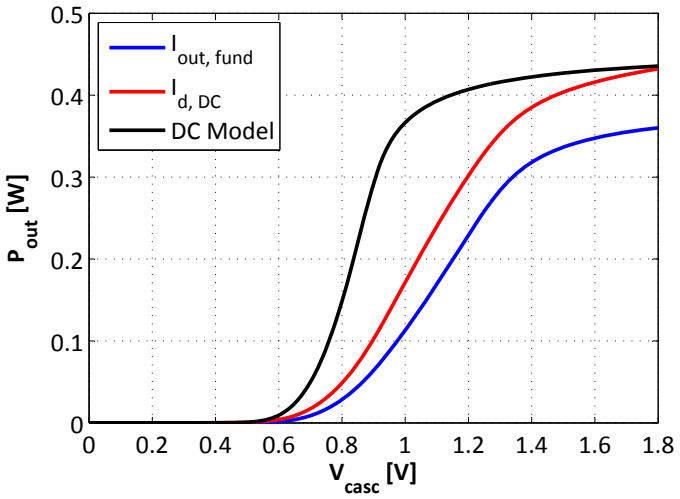


Figure 6.10: Available fundamental output power delivered to the load resistor versus the cascode voltage V_{casc}. The parameter is the current that is used to calculate the output power (DC model, output current or the DC component of the drain current).

equivalent supply resistor. This can be done using

$$R_{DD,eq} = \frac{V_{DD}}{I_{DD}} = \frac{V_{DD}}{I_{d,DC}} = \frac{1.8\,V}{0.258\,A} = 6.97\,\Omega \tag{6.5}$$

The equivalent supply resistor $R_{DD,eq}$ can be seen as the equivalent DC load of the whole cascode class-E PA from the power supply. The Equivalent DC model is build on the assumption that the equivalent DC resistance seen from the power supply terminal

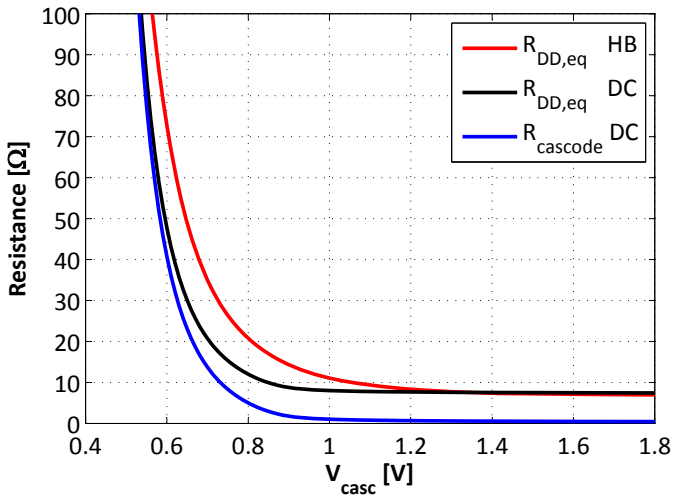


Figure 6.11: Simulated DC resistance from Harmonic Balance simulation of the class-E cascode PA (red curve), DC resistance of the cascode circuit (blue curve) and resistance of the Equivalent DC model versus the cascode voltage V_{casc} ($R_{DD} = 6.5\,\Omega$ in Equivalent DC model).

($R_{DD,eq}$) can be divided into two parts, according to:

$$R_{DD,eq} = R_{DD} + R_{cascode} \tag{6.6}$$

where $R_{cascode}$ is the DC resistance of the cascode circuit in ON state and R_{DD} is an additional external resistor.

Fig. 6.9 shows the comparison of simulated DC drain cascode current versus V_{casc} of the DC model and the Harmonic Balance (HB) RF simulation. For the highest V_{casc} there is a good match between both curves. But the major part of the V_{casc} range exhibits high discrepancy.

Fig. 6.10 shows the fundamental output power versus V_{casc} voltage. The output power calculated directly from the DC component of the RF drain current $I_{d,DC}$ (red curve) shows a significant discrepancy from the ideal curve (blue curve). The DC model output power curve (black) is even worse and the discrepancy is really high. The DC drain current is converted in both cases to the output current using Eq. (6.4).

The reason of the high discrepancy between the two drain current curves is that the DC supply resistance R_{DD} is assumed to be independent of the V_{casc} voltage. The R_{DD} sets the equivalent DC resistance for highest V_{casc} to the desired value and the further increase of $R_{DD,eq}$ is performed solely by cascode resistance R_{casc}. This is illustrated in Fig. 6.11. The assumption expressed in Eq. 6.6 is not valid. This model does not represent the large signal behavior of the cascode modulated class-E PA.

A better DC model needs to implement the DC supply resistance by V_{casc} dependent resistor R_{DD}. The main challenge is to model the DC component of the RF current using the DC model of the cascode circuit. The model should be physically and electrically directly related to the RF cascode class-E circuit.

6.3 Empirical model

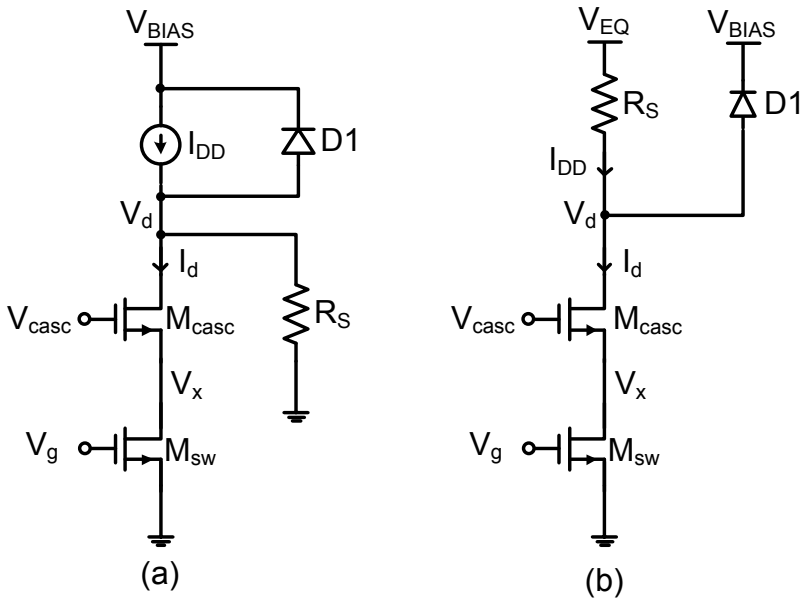


Figure 6.12: Schematic of the empirical DC model of the cascode class-E PA, (a) using the DC bias current and equivalent impedance of the output network (b) using the DC voltage source ($I_{DD} = 0.75\,A$, $V_{EQ} = 5.3\,V$, $R_S = 7\,\Omega$, $V_{BIAS} = 1\,V$, $V_g = 1\,V$).

Another DC model is proposed in order to get better agreement between the modeled and RF simulated drain currents. This model represents a quasi-DC model where not the DC drain current but the peak drain current is modeled. The assumption is that the DC voltage V_{casc} controls the total drain cascode current in RF operation and therefore it is possible to create a DC model that can predict the peak drain cascode current as a function of V_{casc}. The schematic of this model is shown in Fig. 6.12(a).

In Empirical model the cascode transistors are biased from the constant current source I_{DD}. In order to model the conditions the cascode transistors experience during the RF simulation, the drain voltage V_d has to be limited to 1.8 V. This is because in RF simulation when the $V_{casc} = 0\,V$ the drain voltage $V_d = V_{DD} = 1.8\,V$. The diode D1 is implemented in the simulation environment as an ideal PN junction diode (the voltage across the diode when it is ON is 0.8 V). Hence, the bias voltage V_{BIAS} is set to 1 V ($V_{BIAS} + V_{D1} = 1.8\,V$).

The function of R_S is to smooth the transition of the cascode transistor drain current I_d from the saturation to the linear region. Without the load resistor R_S the current I_d would be suddenly limited by the maximum I_{DD} and the transition where the cascode transistor M_{casc} goes from the saturation to the linear region will be very sharp. The value of the R_S resistor is empirically obtained as

$$R_S \approx 10 \cdot R_{cascode} \tag{6.7}$$

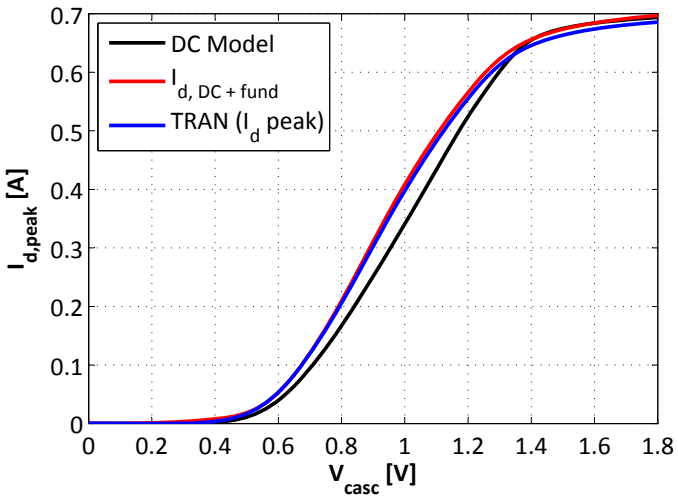


Figure 6.13: Peak drain cascode current versus V_{casc} voltage. The parameter is the empirical DC model, RF simulation peak current and transient simulation peak current.

where $R_{cascode}$ is the resistance of the cascode circuit at the point the drain current I_d saturates. In the simulated circuit $R_{cascode} = 0.64\,\Omega$ and the corresponding V_{casc} is 1.4 V (refer to Fig. 6.13). The load resistor is then calculated as $R_S = 7\,\Omega$.

The summary of assumptions:

- The model is valid in the ON RF period
- The switch transistor can be replaced by its ON resistance
- The V_{casc} voltage controls the total I_d current
- The total I_d current in Empirical model represents the peak value of $I_{d,\,DC}+I_{d,\,RF}$ in the RF domain

The circuit behavior can be described as follows. When V_{casc} is zero there is no current flowing through the cascode circuit. The V_d voltage is 1.8 V; one part of I_{DD} current flows to R_S and the second part returns back to the supply terminal through the diode D1. When the V_{casc} voltage is higher than the threshold voltage of $\mathrm{M_{casc}}$ then the cascode circuit starts to draw the current. The amount of drawn current is directly controlled by the V_{casc} voltage. The cascode transistor $\mathrm{M_{casc}}$ is in saturation and the drain current I_d is increasing with V_{casc}. The cascode circuit resistance $R_{cascode}$ is decreasing. The cascode current I_d will not saturate abruptly because a part of the I_{DD} current is flowing through R_S. If the I_{DD} is set to $I_{d,max}$ obtained from RF simulation (0.7 A) then the cascode current I_d would not reach this value because a small portion of the I_{DD} current flows to R_S. Due to this effect the value of I_{DD} has to be slightly increased to compensate for the loss in R_S ($I_{DD} = 0.75\,A$). The ratio of R_S to $R_{cascode}$ controls the maximum I_d and also sets the slope of I_d when $\mathrm{M_{casc}}$ enters the linear region.

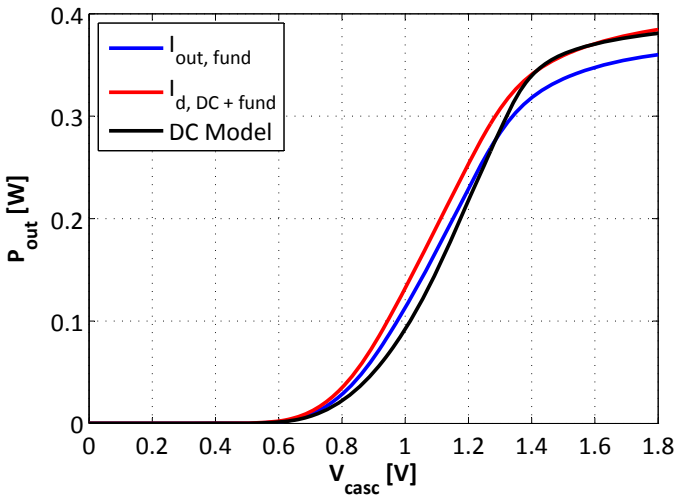


Figure 6.14: Available fundamental output power delivered to the load resistor versus V_{casc} voltage. The parameter is the empirical DC model, RF simulation peak current and transient simulation peak current.

The DC model from Fig. 6.12(a) can be re-arranged using Thevenin theorem into a form that is more suitable for simplified calculations and intuitive analysis. This equivalent circuit is shown in Fig. 6.12(b). The current source I_{DD} and R_S resistor are substituted by an equivalent voltage source V_{EQ} and R_S resistor in series with it. The value of the equivalent voltage source is calculated as

$$V_{EQ} = I_{DD} R_S = 5.3\,V \tag{6.8}$$

Empirical DC model provides good match with the RF simulated curves. The peak drain current versus V_{casc} voltage and output power versus V_{casc} voltage are shown in Fig. 6.13 and Fig. 6.14 respectively. For the high V_{casc} levels both the peak drain current and output power are identical with peak drain current simulated by the harmonic balance simulation. There is a small discrepancy in the region where the cascode transistor M_{casc} operates in saturation.

6.4 Analytical model

A simplified analytical model of the cascode circuit is proposed in this section. The main goal is to obtain a simplified analytical expression of the drain current I_d as a function of V_{casc}. The analytical model is a general model of the cascode amplifier and it is not directly related to the previously described Equivalent and Empirical DC models.

It is assumed that the cascode current is zero during the OFF state (independent of the V_{casc} voltage). Therefore only the current during the ON state is investigated. It is also assumed that the switch transistor operates as an ideal switch with the ON-

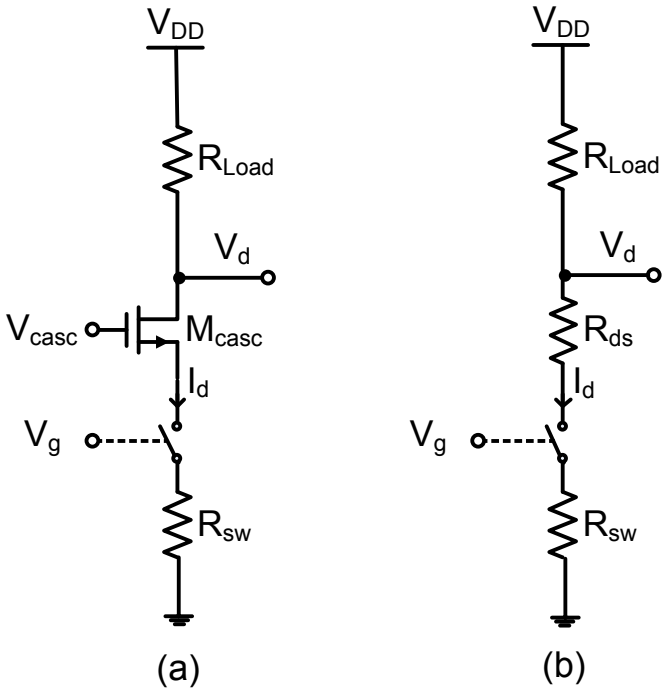


Figure 6.15: Schematic of the analytical model that is based on the empirical model (a) in saturation region (b) in triode region.

resistance R_{sw} (Fig. 6.15). R_{Load} and V_{DD} represent generic load resistance and supply voltage seen by the cascode circuit respectively.

The cascode transistor M_{casc} operates in two states. M_{casc} is in saturation for low V_{casc} voltage. The cascode transistor enters and remains in the linear region when

$$V_d \leq V_{casc} - V_T \tag{6.9}$$

where V_T is the cascode transistor threshold voltage. The equivalent circuits for the saturation and linear regions are shown in Fig. 6.15(a) and 6.15(b) respectively. The following equations are based on a simplified model of the MOSFET transistor.

6.4.1 Saturation region

The drain current of the cascode device in saturation is given by

$$I_d = \frac{1}{2}\mu_0 C_{OX} W/L(V_{GS} - V_T)^2 \tag{6.10}$$

where μ_0 and C_{OX} are the mobility of the carriers and the gate oxide capacity respectively. W is the channel width and L is the channel length. Note that only the channel length modulation is considered. The gate-source voltage V_{gs} of the M_{casc} transistor can be written as

$$V_{GS} = V_{casc} - I_d R_{sw} \tag{6.11}$$

The surface mobility of the carriers in the transistor channel depends on various process parameters and also on the gate and bulk voltages. The effective mobility can be expressed using an empirical relation [Cheng & Hu 2002]

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff}/E_0)^{\nu}} \tag{6.12}$$

where the E_0 and ν are technological constants. Note that this model is not suitable for SPICE simulations because of the power function in the denominator (time consuming calculation). The average electrical field E_{eff} experienced by the carriers in the inversion layer is approximated as [Cheng & Hu 2002]

$$E_{eff} \cong \frac{V_{GS} + V_T}{6T_{OX}} \tag{6.13}$$

where $V_{GS} = V_{casc} - V_x$ but for simplicity $V_{GS} = V_{casc}$ is assumed in further calculations that use Eq. (6.13).

By substituting of Eq. (6.11) – Eq. (6.13) into Eq. (6.10) and solving for I_d the following result is obtained

$$I_d = \frac{L + C_{OX}R_{sw}V'_{eff}W\mu_{eff} - \sqrt{L(L + 2C_{OX}R_{sw}V'_{eff}W\mu_{eff})}}{C_{OX}R_{sw}^2W\mu_{eff}} \tag{6.14}$$

where

$$V'_{eff} = V_{casc} - V_T \tag{6.15}$$

Eq. (6.14) represents analytical form of the drain current as a function of V_{casc} voltage of the cascode class-E PA in the ON RF period when the cascode transistor operates in the saturation region.

6.4.2 Linear region

In the linear region the cascode transistor can be substituted by the equivalent drain-source resistor R_{ds} (Fig. 6.15(b)). The drain current is given by the Sah equation as

$$I_d = \mu_0 C_{OX}\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{6.16}$$

The drain-source voltage can be found using

$$V_{DS} = V_{DD} - I_d R_{Load} - I_d R_{sw} \tag{6.17}$$

By substituting of (6.17) into (6.16) and solving for I_d gives

$$I_d = \frac{\sqrt{\alpha(2V'_{eff} - V_{DD})V_{DD}\beta^2 + (1 + V'_{eff}(R_{Load} + R_{sw})\beta - R_{Load}V_{DD}\beta)^2}}{\alpha\beta} + \frac{R_{Load}V_{DD}\beta - V'_{eff}\beta(R_{sw} + R_{Load}) - 1}{\alpha\beta} \tag{6.18}$$

The coefficient α and β are defined as

$$\alpha = R_{Load}^2 - R_{sw}^2$$
$$\beta = \mu_{eff}C_{OX}\frac{W}{L} \tag{6.19}$$

The drain current as a function of V_{casc} voltage in the cascode class-E PA in the ON RF period when the cascode transistor is in linear region can be analytically expressed by Eq. (6.18).

6.4.3 Analytical model verification

Utilizing equations (6.14) and (6.18) the drain current can be calculated as a function of V_{casc}. The analytical model is verified using Empirical DC model. The supply voltage and load resistance in the analytical model are replaced by the values calculated in the empirical model subsection (V_{EQ} and R_S).

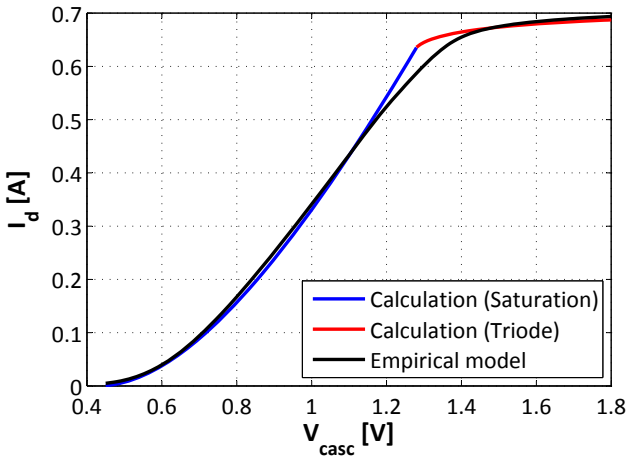


Figure 6.16: Cascode drain current versus the V_{casc} voltage. Simulation result is obtained using the Empirical DC model. Saturation and triode models are calculated based on analytical model.

Fig. 6.16 shows the comparison of the calculated model and the simulation result. The correlation between the model and the simulation is reasonable considering that the equations are very simplified. The roll-off of the transfer characteristic in Fig. 6.16

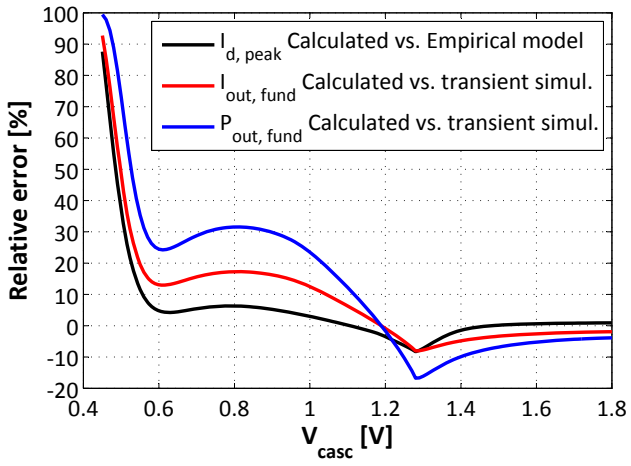


Figure 6.17: Error between the calculated and simulated peak cascode drain current (black) of Empirical model. Error between the calculated fundamental output current and simulated fundamental output current from transient simulations. Error between the calculated on simulated output power based.

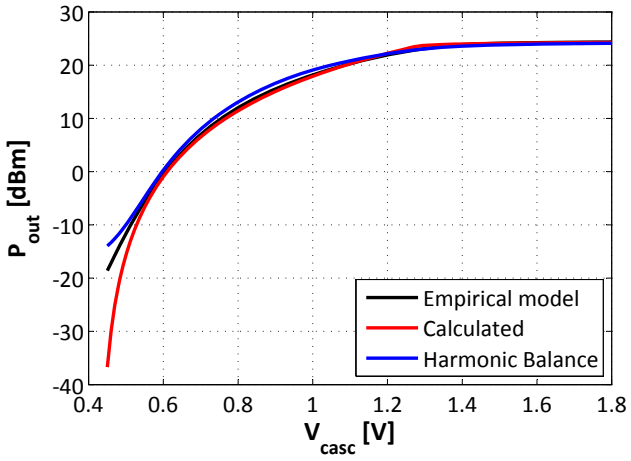


Figure 6.18: Comparison of the simulated fundamental output power versus the V_{casc} voltage. The output power is simulated using Empirical model, calculated using Analytical model and simulated using Harmonic Balance analysis of the cascode modulated class-E PA.

at high drain current is caused by the cascode device entering the linear region where $V_{DS.M_{\text{casc}}} < V_{DS.M_{\text{casc}},sat}$. The significance of this effect depends on the current level through the cascode device, on the device physical dimension (W/L) and on the magnitude of the modulation voltage V_{casc}. The supply voltage level has direct impact on the headroom of the cascode device and therefore significantly influences the shape of the transfer characteristic. For some applications it might be beneficial to limit the V_{casc} voltage so that the cascode transistor doesn't enter the deeper triode region.

	Description	Value	Units
W	Channel width	6.08 $\cdot 10^{-3}$	m
L	Channel length	0.34 $\cdot 10^{-6}$	m
T_{OX}	Gate oxide thickness	7.2 $\cdot 10^{-9}$	m
C_{OX}	Gate oxide capacitance	4.8 $\cdot 10^{-3}$	F/m
μ_0	mobility	0.0391	$m^2/V/s$
E_0	mobility model related parameter	67 $\cdot 10^6$	V/m
ν	mobility model related parameter	1.6	-
V_T	Threshold voltage	0.4294	V
R_{sw}	ON resistance of the switch transistor	0.18	Ω
V_{EQ}	Equivalent supply voltage	5.3	V
R_{Load}	Equivalent load resistance	7.08	Ω

Table 6.1: Technological constants and model variables values used in the analytical model calculations.

The errors between the calculated curves and the simulated ones are shown in Fig. 6.17. The figure shows three plots. First plot (red) shows the comparison of the calculated (Analytical model) and simulated (Empirical model) peak drain current $I_{d,peak}$. Second waveform (red) represents the error between the fundamental output current calculated using Eq. (6.4) and the fundamental output current simulated in transient analysis. The last curve (black) shows the error between the calculated output power based on the calculated output current and the simulated output power in transient analysis.

The discrepancy is highest in the low V_{casc} region where the cascode transistor turns ON. The best fit is achieved when the cascode transistor operates in linear region. The error is calculated as

$$Relative\ error\,[\%] = \frac{(Ideal\,value) - (Calculated\,value)}{(Ideal\,value)} \cdot 100 \tag{6.20}$$

where the ideal and calculated value is the peak cascode drain current $I_{d,peak}$ or the fundamental output power P_{out} in mW. The main source of the error is from the simplified assumptions used in the analytical model calculations. The analytical model is valid from $V_{casc} = V_T \cong 0.43\,V$ up to $V_{casc} = 1.8\,V$.

The comparison of the simulated and calculated output power (in dBm) is shown in Fig. 6.18.

The technological constants used in the drain current calculations are summarized in Table 6.1.

The potential of the before mentioned models is in the linearization of the PA and implementation of power sensing circuits.

Chapter 7

Experimental Results

Contents

In this chapter are summarized the measured results of the produced CMOS cascode class-E PAs. Most of the results were already published in journal papers. The reprint of the publications can be found in Appendix B.

The first section focuses on the usage of the cascode class-E PA to control the output power. The PA is tested with CW and GMSK signals. The second section describes the cascode modulated class-E PA. Two types of test signals are used: EDGE and WCDMA.

7.1 Cascode power control

Power control techniques for a constant envelope modulation schemes can be used to improve the efficiency of the PA. For a switch mode PA, the input power is expected to be constant, and therefore a supply voltage power control technique (SVPCT) is traditionally employed.

7.1.1 Supply voltage power control technique

The supply voltage power control technique is depicted in Fig. 7.1(a). The output power is controlled by a power controller.

The output power control range is the maximum range over which the PA output power can be controlled. The GSM900 standard (GMSK modulation) for a mobile station specified by European Telecommunications Standards Institute (ETSI) requires the power control range of 24 dB (class 5) to 34 dB (class 2). In the DCS1800 and

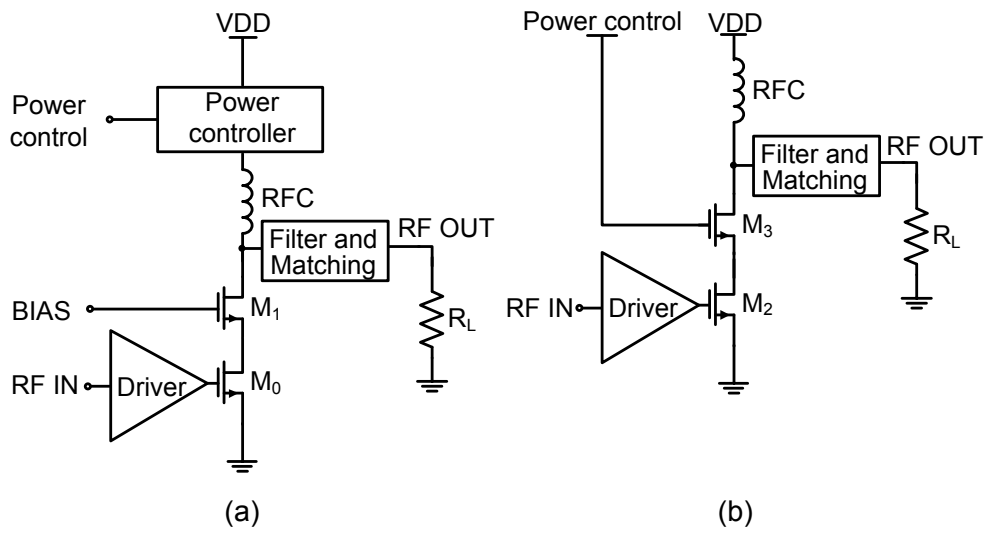


Figure 7.1: (a) Conventional power control technique. (b) Proposed power control technique.

PCS1900 frequency bands, the standard requires 24 dB to 36 dB power control range. The power control range can be written as

$$PCR[\text{dB}] = P_{\text{out,max}} - P_{\text{out,min}} = 20\log_{10}\frac{V_{\text{dd, max}}}{V_{\text{dd, min}}} \tag{7.1}$$

where $P_{\text{out,max}}$ and $P_{\text{out,min}}$ are maximum and minimum average output power in dBm. It is assumed the load impedance is constant. A low voltage class-E PA with a constant input power has a very limited power control range. For a supply voltage range of 0.2 V to 1.8 V the power control range is 19.1 dB.

The main drawbacks of SVPCT are limited output power control range, high sensitivity to load variations, and that the switch mode power controller is placed in the high power path [Kitchen *et al.* 2007]. Since the supply voltage power controller pulls a high current to the PA, the placement in the high power path (in series with the RF choke) makes the efficiency the most important parameter. The efficiency of state-of-the-art power converters is up to 90 % at the maximum output power [Kwak *et al.* 2007].

It is important to note that if the supply voltage drops to zero, there is still some output voltage. This is due to feed-through from the input to the output. In order to maximize the output power control range, the supply voltage controller must be able to reach the positive battery supply rail and also to provide close to zero output voltage. The maximum supply voltage is limited by the reliability of the CMOS PA [Reynaert & Steyaert 2005].

7.1.2 Cascode power control technique

The proposed alternative power control technique is shown in Fig. 7.1(b). The power control signal is applied to the gate of the cascode transistor M3.

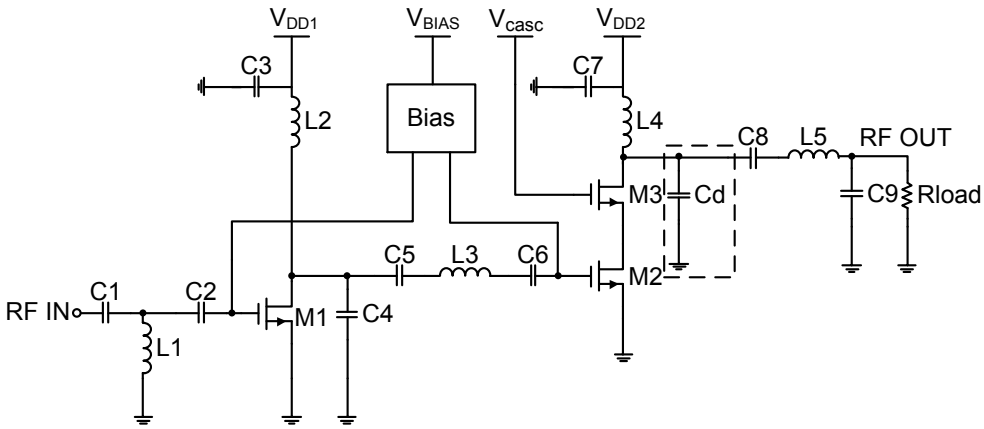


Figure 7.2: Class-E power amplifier schematic.

In the cascode power control technique (CPCT) the input voltage on the gate of the cascode transistor M3 is divided between $V_{gs,M3}$ and $V_{ds,M2}$ (see Fig. 7.2). By decreasing the input voltage, $V_{ds,M2}$ also decreases until $V_{CASC} \approx V_{th,M3}$ when $V_{ds,M2}$ drops close to zero ($V_{th,M3}$ is the threshold voltage of the transistor M3). For the SVPCT, the supply voltage can be decreased almost to zero. Therefore, the input dynamic range of the CPCT is approximately one threshold voltage lower than in the SVPCT. In the technology used for the experimental work in Subsection 7.1.3, the threshold voltage is $0.55\,\mathrm{V}$. By taking into consideration the subthreshold region of the transistor, V_{casc} can be decreased approximately to $0.3\,\mathrm{V}$.

The CPCT also provides higher output power control range than the SVPCT. This is because the capacitive coupling between the input (gate of M2) and the output (drain M3) is reduced, provided the cascode transistor M3 is in saturation. In the CPCT this is fulfilled for the whole V_{casc} range.

The PAE of the CPCT is higher than of the SVPCT due to the lower power losses associated with parasitic capacitances charging/discharging. The voltage across M2 is limited by the cascode M3. By decreasing the supply voltage in the SVPCT, the transistor M3 goes into the linear region. This increases the voltage swing across M3. Therefore, the dissipated power due to the charging/discharging of parasitic capacitances at the common node of M2 and M3 is also increased. On the other hand, by decreasing the V_{casc} voltage in the CPCT M3 stays in saturation and M2 stays in the linear region. The voltage swing across M3 is limited and the CPCT has lower power loss than SVPCT.

In the proposed design, the finite RF choke (RFC) technique was used and the maximum drain voltage peak is reduced to $2.5\,V_{dd}$ [Yoo *et al.* 2001].

7.1.3 Measurements

Fig. 7.2 shows the proposed two-stage PA where the class-E output stage (M2 & M3) is driven by a class-E driver stage (M1). A microphotograph of the implemented power amplifier is shown in Fig. 7.3. The area of the PA is $1.2 \times 1.0\,\mathrm{mm}^2$. Supply voltages

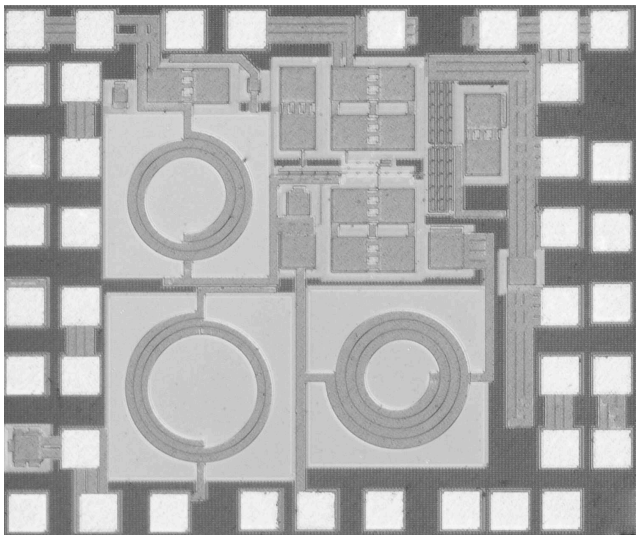


Figure 7.3: Microphotograph of the PA.

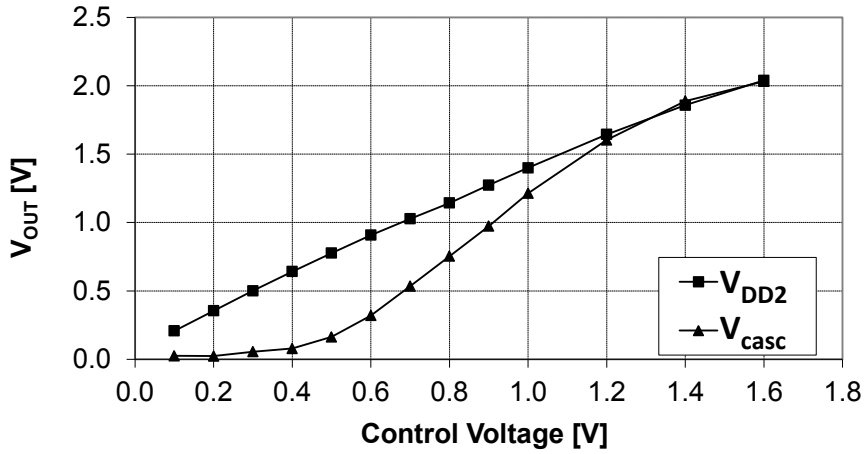


Figure 7.4: Measured effective RF voltage (V_{OUT}) across a 50 Ω load versus V_{DD2} (V_{casc} = 1.6 V) and V_{casc} (V_{DD2} = 1.6 V). The available input power was 3.5 dBm at a frequency of 2.2 GHz.

are filtered on the PCB (capacitors C3 and C7 in Fig. 7.2). Inductors L4 and L5 are realized by bond-wires. The adaptive power control circuit was not implemented in the prototype, and therefore the performance is evaluated for specific values of V_{casc} and V_{DD2} voltages.

The measured AM-AM characteristic is depicted in Fig. 7.4. The input dynamic range of the CPCT is 14.5 dB (from 0.3 V to 1.6 V) whereas SVPCT offers 24 dB (from 0.1 V to 1.6 V). The AM-AM curve of CPCT is non-linear but that is of no major concern in the power control of the constant envelope modulated PA. The available power from the source is chosen as 3.5 dBm to ensure that the switching power transistor works as a switch as intended.

Although the prototype was not designed to meet any particular standard, it was

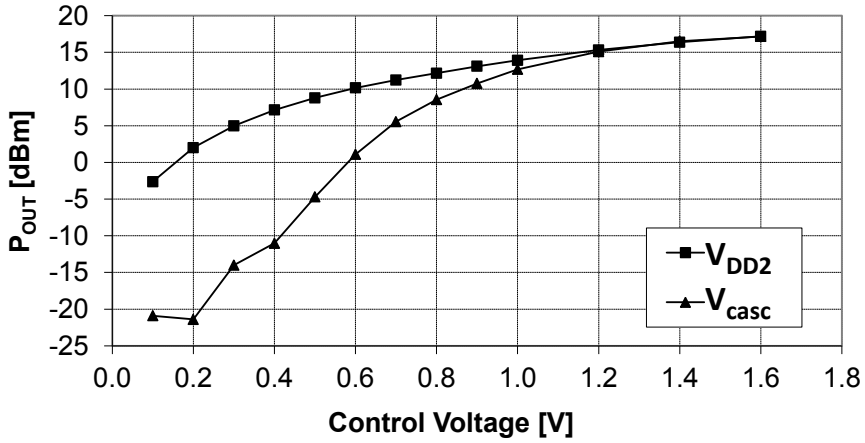


Figure 7.5: Measured average in-band output power of the PA (P_{OUT}) delivered to a 50 Ω load versus V_{DD2} ($V_{casc} = 1.6$ V) and V_{casc} ($V_{DD2} = 1.6$ V). The input signal is a GMSK modulated signal (BT=0.3) at a carrier frequency of 2.2 GHz with 3.5 dBm available average input power. The measurement bandwidth is 200 kHz around the carrier.

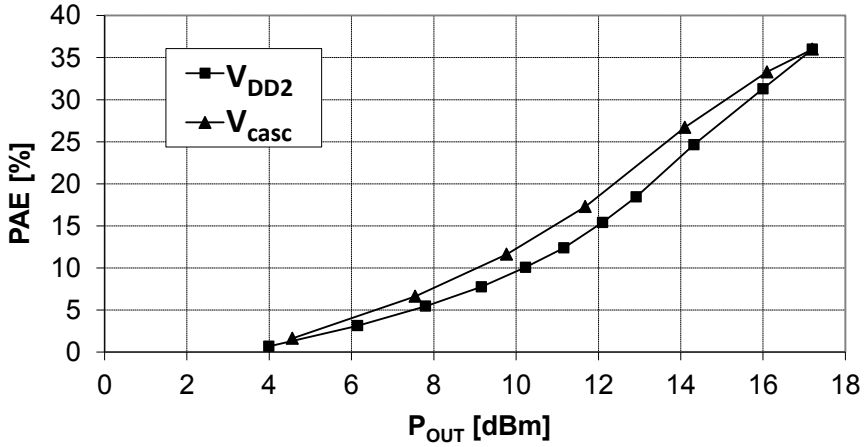


Figure 7.6: Measured power added efficiency (PAE) versus output power (P_{OUT}) delivered to a 50 Ω load. The input signal is a GMSK modulated signal (BT=0.3) at carrier frequency of 2.2 GHz with 3.5 dBm available average input power. The parameter is V_{DD2} ($V_{casc} = 1.6$ V) and V_{casc} ($V_{DD2} = 1.6$ V).

tested with a GMSK signal. Fig. 7.5 shows the measured average in-band output power. It can be seen that the SVPCT provides approximately 20 dB output power control range (from -2 dBm to 18 dBm), roughly the same as refs. [Park *et al.* 2007] and [Shirvani *et al.* 2002]. The CPCT exhibits a much higher output power control range of 36 dB. This is a 16 dB larger control range than of the SVPCT.

The measured results in Fig. 7.6 show that the cascode modulated class-E PA is more power efficient than the power supply modulated cascode class-E PA. The PAE of the cascode modulated PA is up to 3 % higher compared to the power supply modulated

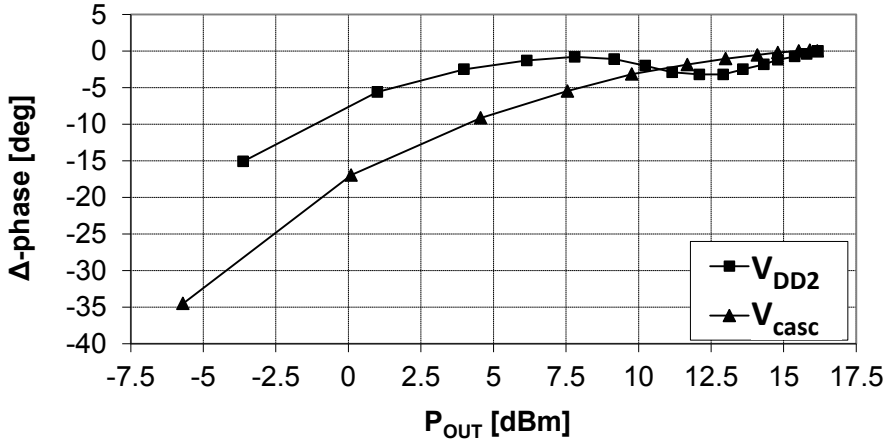


Figure 7.7: Measured phase advance across the PA versus power (P_{OUT}) delivered to a 50 Ω load. The parameter is V_{DD2} ($V_{casc} = 1.6$ V) and V_{casc} sweep ($V_{DD2} = 1.6$ V). The available input power was 3.5 dBm at a frequency of 2.2 GHz.

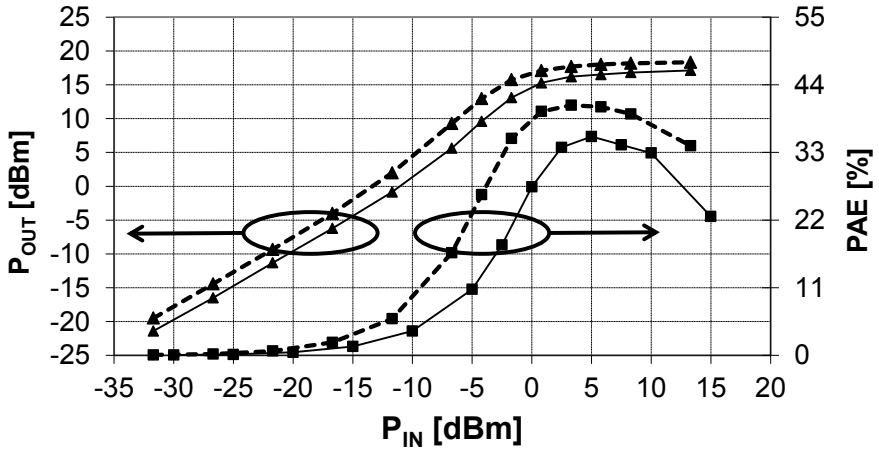


Figure 7.8: Measured (solid line) and simulated (dashed line) output power (P_{out}) delivered to a 50 Ω load and power added efficiency (PAE) versus available input power (P_{in}) at a frequency of 2.2 GHz.

PA. This is valid only for the maximum output power region. At low power levels PAE of the cascode modulated PA is lower than in the power supply modulated PA.

Fig. 7.7 shows the AM-PM distortion for a fixed input power. The phase distortion of the CPCT is larger than that of the SVPCT. This is due to the parasitic drain capacitance variation of the cascode transistor (M3) on the V_{casc} voltage, and due to the Miller drain-gate capacitance of the switching power transistor (M2). The high AM-PM doesn't deteriorate the phase error (or EVM) in the transmitting signal because the power control signal has a very low frequency (for GSM/EDGE it is approximately 16.6 Hz) and its value can be considered constant during the frame period.

Fig. 7.8 shows measured and simulated PAE and P_{out} versus available input power

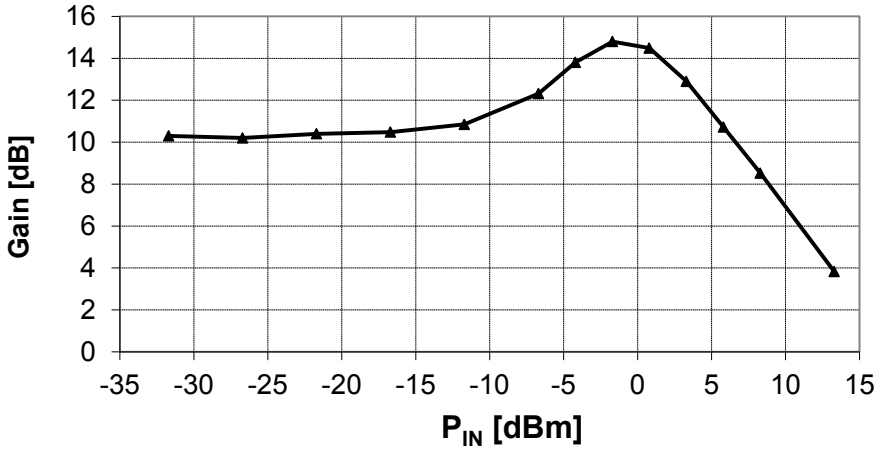


Figure 7.9: Transducer gain versus versus available average input power ($V_{DD2} = 1.6\,\text{V}$, $V_{casc} = 1.6\,\text{V}$). The input signal is a single tone at a frequency of 2.2 GHz.

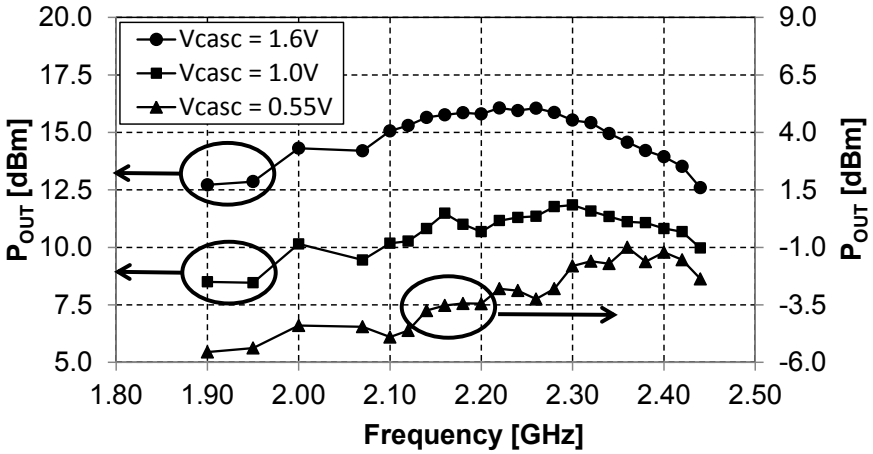


Figure 7.10: Measured average output power of the PA (P_{OUT}) delivered to a 50 Ω load versus carrier frequency ($V_{DD2} = 1.6\,\text{V}$, $P_{IN} = 3.5\,dBm$). The paramter is V_{casc} voltage.

(in Fig. 7.2 V_{DD1} is 0.6 V, V_{DD2} and V_{casc} are both 1.6 V). A sine wave signal was used as stimulus. There is a good agreement between the simulated and measured data. The difficult modeling of the bond wire inductors is a major source of discrepancy. The gain plot versus P_{IN} is shown in Fig. 7.9. The maximum transducer power gain is 14.8 dB.

The output power versus frequency for a different V_{casc} voltages is plotted in Fig. 7.10. The 3 dB bandwidth of the power amplifier is 380 MHz (from 2.00 GHz to 2.38 GHz). As the V_{casc} voltage is decreasing the resonant frequency of the output network is increasing. This is due to strong variation of the cascode transistor (M3) drain capacitance on the V_{casc} voltage.

The power control circuit was not implemented in the prototype and therefore, the performance is evaluated for a three V_{casc} voltages. The maximum output power is obtained with $V_{casc} = 1.6\,\text{V}$. Fig. 7.11 shows the average in-band output power (in

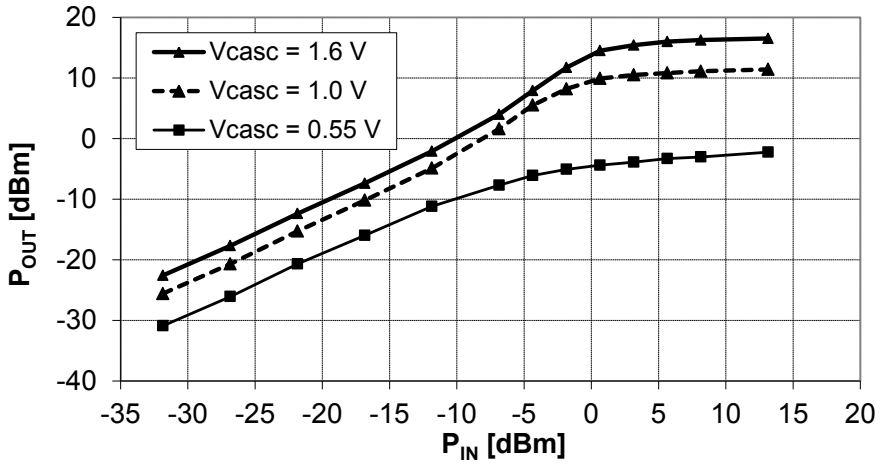


Figure 7.11: Measured average in-band output power of the PA (P_{out}) versus available average input power (P_{in}). The input signal is a GMSK modulated signal (BT=0.3) at carrier frequency of 2.2 GHz. The measurement band-width is 200kHz around the carrier. The parameter is V_{casc} voltage.

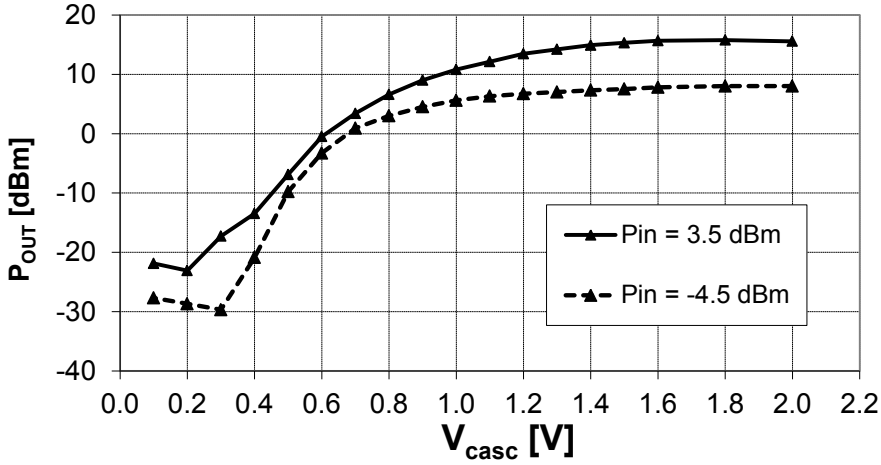


Figure 7.12: Measured average in-band output power of the PA (P_{out}) versus the V_{casc} voltage. The input signal is a GMSK modulated signal (BT=0.3) at carrier frequency of 2.2 GHz. The measurement band-width is 200kHz around the carrier. The parameter is average input power (P_{in}).

200 kHz band width) versus available average input power and the parameter is V_{casc} voltage.

Fig. 7.12 shows average in-band output power (P_{out}) versus V_{casc} voltage as a parameter of average input power (P_{in}). The output power can be further decreased by simultaneous adjusting of Pin and V_{casc}. Too low input power might cause that PA is not operating in the switch-mode and therefore the efficiency will drops. This might be still acceptable for an application where the high output dynamic range is required.

The power added efficiency versus V_{casc} voltage is plotted in Fig. 7.13. The param-

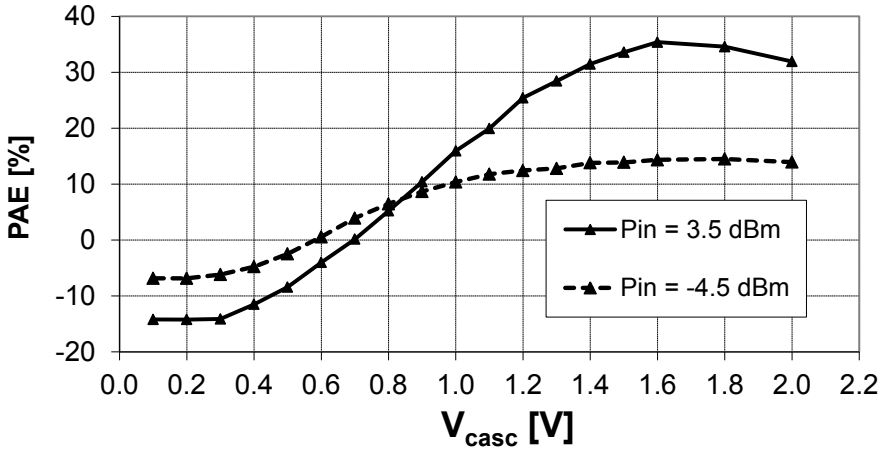


Figure 7.13: Measured power added efficiency of the PA (PAE) versus versus the V_{casc} voltage. The paramter is available average input power (P_{in}). The input signal is a GMSK modulated signal (BT=0.3) at carrier frequency of 2.2 GHz. The measurement band-width is 200kHz around the carrier.

eter is available average input power. It can be seen that by decreasing of the V_{casc} voltage the PAE drops significantly. The PAE exhibit negative values when the output power falls below P_{IN}.

The measured output spectrum mask was lying below the GSM specification mask with a large margin over the whole V_{casc} voltage range. The measured RMS phase error is 0.2 degrees.

7.2 Varying envelope modulation

It this section the measured results of the cascode modulated class-E PA are presented. The PA was tested using WCDMA and EDGE modulated signals. The circuit was fabricated in 0.18 μm CMOS technology. The process offers two gate-oxide thickness options (4.2 nm for 1.8 V and 7 nm for 3.3 V operation). The channel length of all transistors is 0.18 μm except of the two cascode transistors (M1 and M3) with 0.34 μm. The process has 5 metal layers plus thick top layer.

The schematic of the cascode modulated class-E PA is shown in Fig. 7.14. The microphotograph of the realized power amplifier is shown in Fig. 7.15. The chip dimensions are 1.5 x 3 mm.

The width of transistors M2 and M3 is 5000 μm and 8000 μm respectively. The input matching network consists of spiral on-chip inductor L1 (2.1 nH) and capacitor C1 (8 pF). The output matching network consists of inductor L6 (2.7 nH) and capacitor C8 (4 pF). The inductor L6 is a part of the series resonant output tank (with C7) and also a part of the matching network (with C8). L6 is realized by an on-chip bondwire. The driver and output stage RF choke inductors L2 and L5 respectively are realized via bondwires. The interstage inductors L3 (5 nH) and L4 (3.1 nH) are realized as spiral on-chip inductors. Capacitors C3 (2 pF), C4 (2 pF) and C5 (4.9 pF) are also part of

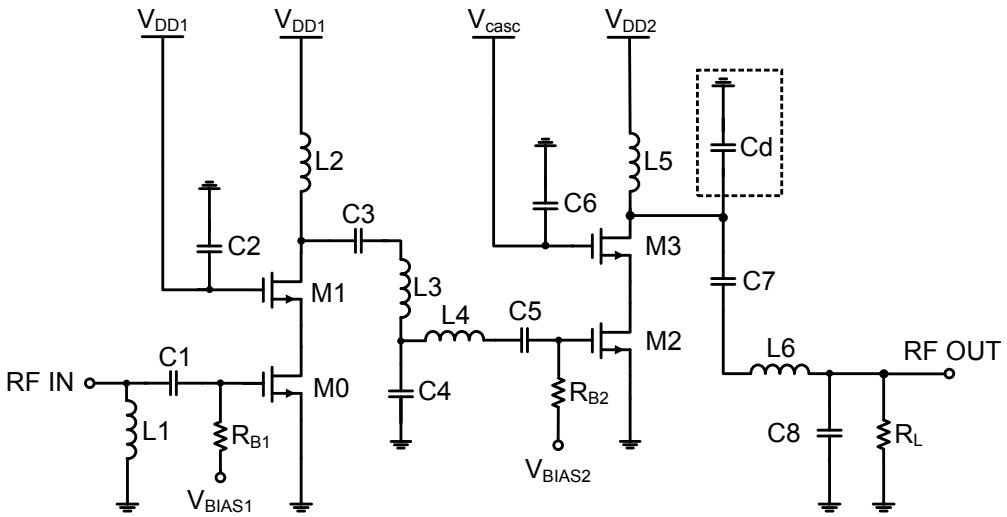


Figure 7.14: Schematic of the cascode class-E CMOS PA.

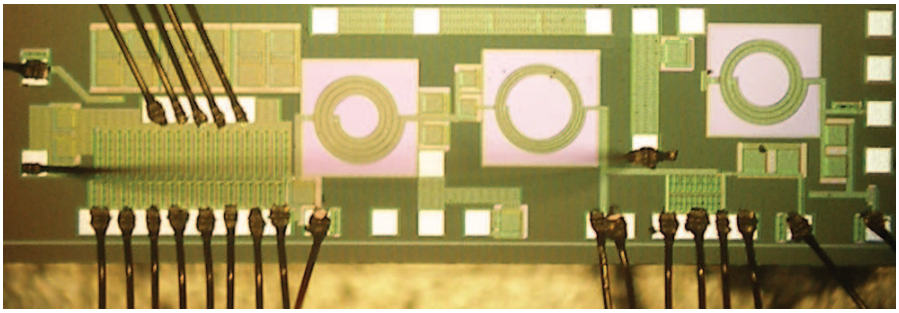


Figure 7.15: Microphotograph of the chip.

the interstage matching. The interstage matching topology is more complex because the driver and output stage were tested separately and have to be impedance matched. The capacitors C2 (10 pF) and C6 (60 pF) should provide RF ground at the gates of cascode transistors.

The envelope adjustment circuit is implemented off-chip. The main function of this circuit is to provide a voltage shift and amplification. This is implemented by the differential receiver amplifier AD8130 by Analog Devices (Fig. 7.17). It has a 200 MHz bandwidth and it can be connected as a voltage level shifter. The gain can be set by the feedback resistors. The signal applied to the cascode transistor M3 contains both amplitude modulated signal and power control signal (Fig. 7.16).

The nominal operation conditions are as follows: available input power 3.5 dBm, frequency 1.75 GHz, output stage power supply 1.8 V, driver stage power supply and cascode voltage 1 V, bias voltage (for each stage) 0.675 V. The maximum cascode voltage in output stage equals to the supply voltage (1.8 V). The PA is designed to have 25 dBm peak output power.

The measured output power versus V_{casc} voltage is shown in Fig. 7.18. The DC

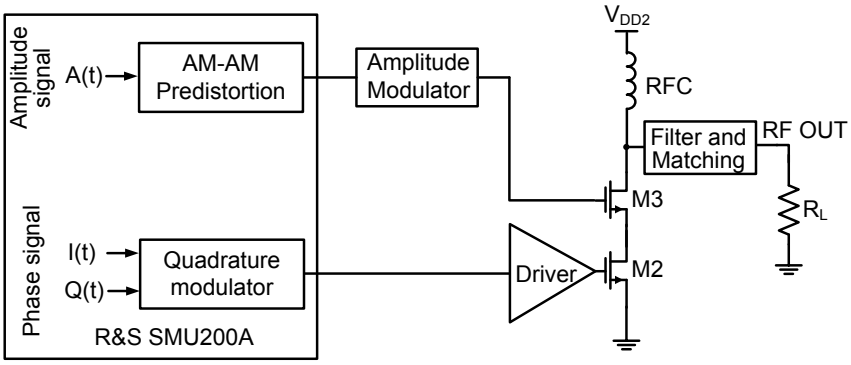


Figure 7.16: Block diagram of a polar modulated PA

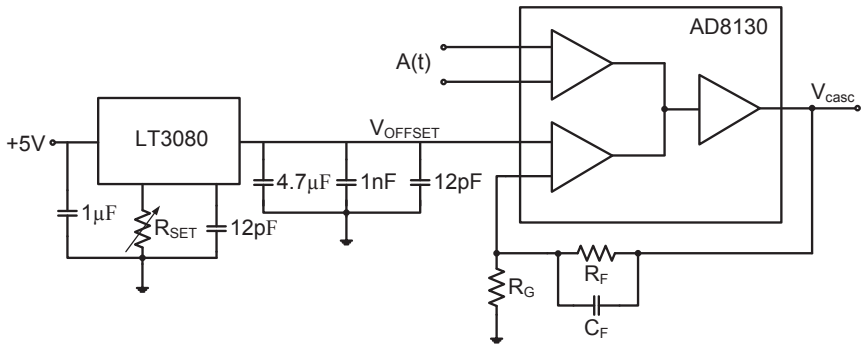


Figure 7.17: Amplitude modulator schematic

V_{casc} voltage (which is close to the effective voltage of the amplitude modulated signal using EDGE or WCDMA modulation) is swept from 0.6 V to 1.8 V. The output power control range is 42 dB. The output power DR of the amplitude modulated cascode PA is limited by the linearity requirements of the particular wireless standard. The lowest output power levels are significantly distorted (that can be observed for example in Fig. 7.30) because the peak-to-peak output power dynamic range using a varying amplitude signal is limited when the cascode transistor operates in the "knee" region. Furthermore, using only single LUT based PA predistortion the linearization of this region of the AM-AM characteristic is difficult (refer to Subsection 7.2.1).

The target of this work is not to meet every aspect of a particular wireless standard. The measured results using varying envelope signals (EDGE and WCDMA) demonstrate the feasibility of the cascode modulation concept.

7.2.1 Linearization

The predistorter linearizes the PA by generating an inverse nonlinear transfer function to the PA so that the overall transfer function is linear. This can be mathematically written as

$$F_{PD}(v_{in}) \cdot F_{PA}(v_{pd}) = C \tag{7.2}$$

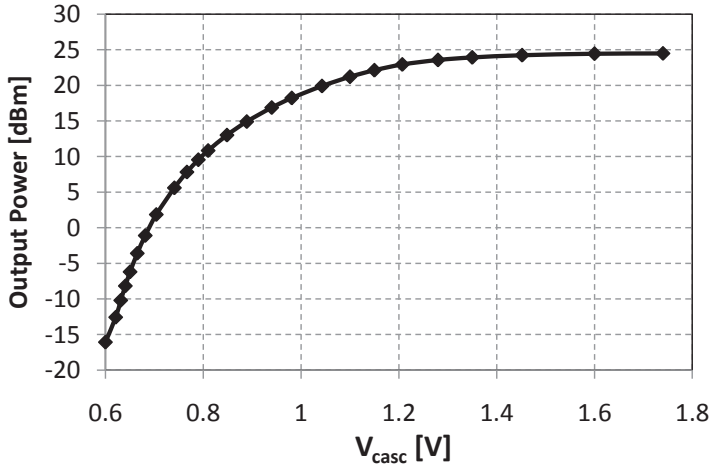


Figure 7.18: Measured average RF output power delivered to a 50 Ω load versus DC cascode voltage V_{casc}. The RF input is a single-tone with available input power of 3.5 dBm at a frequency of 1.75GHz.

where F_{PD} and F_{PA} are the predistorter and PA transfer functions, v_{in} is the amplitude input signal which is in the range where the linearization function is valid, v_{pd} is the amplitude signal at the output of the predistorter and C is a constant.

The predistorter output voltage can be expressed as

$$v_{pd} = F_{PD}(v_{in}) \tag{7.3}$$

In this work, the look-up table (LUT) based memoryless predistortion of the PA is implemented. The LUT coefficient calculation using a linear interpolation can be written as

$$\begin{aligned} y_2 &= F_{PA}(x_2) = F_{PA}(x_1 + c_{x1}) \\ &= F_{PA}(F_{PD}(x_1)) = g(x_1) \end{aligned} \tag{7.4}$$

where $g(x)$ is the target linear transfer function and c_{xi} is the coefficient stored in LUT for x_i in order to correct the AM-AM transfer function. The phase predistortion is given by

$$c_{\Phi(x1)} = \Phi_{constant} - \Phi(x_2) \tag{7.5}$$

where $c_{\Phi(x1)}$ is the phase correction coefficient for x_1 and $\Phi_{constant}$ is a constant target phase.

The AM-AM characteristic (Fig. 7.19) and the AM-PM characteristic (Fig. 7.20) are measured dynamically using the EDGE and WCDMA input signals as PA stimuli. Since the linearization model is memoryless, the LUT coefficients are calculated directly in MATLAB. The AM-AM characteristic is modeled by a 9-th order polynomial and the AM-PM characteristic by the polynomial of 8-th order. The order of the polynomial model was chosen as a trade-off between the correlation of the model and measured

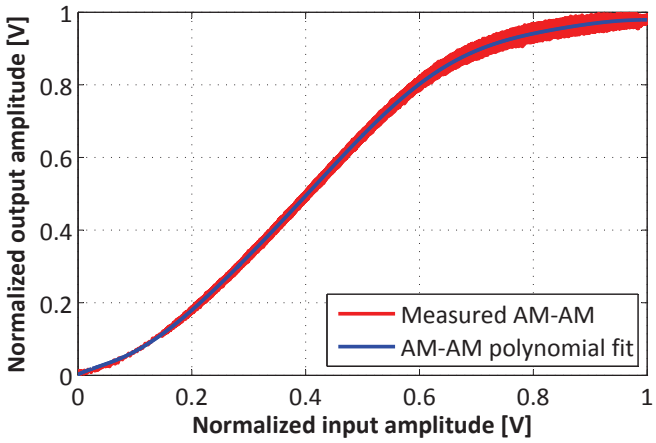


Figure 7.19: Measured AM-AM characteristic and its polynomial fit.

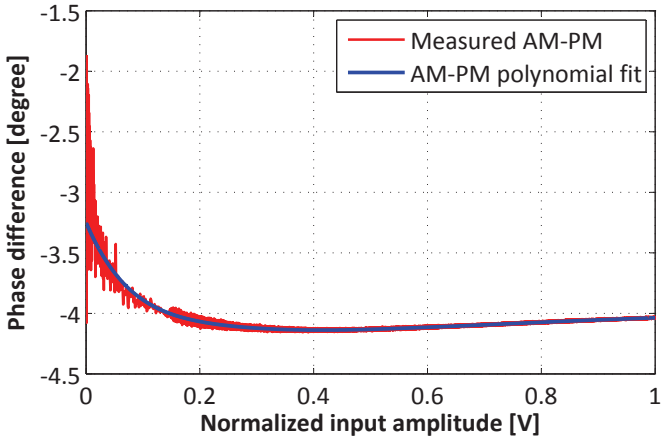


Figure 7.20: Measured AM-PM characteristic and its polynomial fit.

data (especially at the extremes of the input signal) and still keeping the order of the polynomial model as low as possible. The polynomial model is valid within the input parameter range. The LUT coefficients are calculated from 20 ms long data signals, which corresponds approximately to 4 frames long EDGE signal or to 2 frames long WCDMA signal. The predistortion is applied in MATLAB after the modulated input signal is generated.

The predistortion is based on a single behavioral model of the PA which is used for all power levels. Therefore only a single LUT is used, which makes the digital predistortion easier to implement.

The main difference between the EDGE and WCDMA signals is that WCDMA has higher BW, dynamic range and power control range. WCDMA signal using quadrature phase-shift keying (QPSK) modulation has approximately the same 3.4 dB PAR as the EDGE signal. It is very challenging to model the AM-AM response of the WCDMA modulated PA by a single polynomial curve. From the shape of the curves in Fig. 7.19

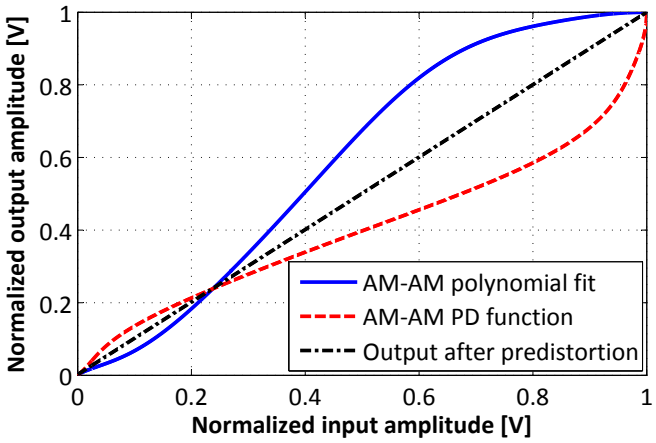


Figure 7.21: Simulated AM-AM characteristic after the predistortion, predistorted transfer function and the polynomial fit of the measured AM-AM of the PA.

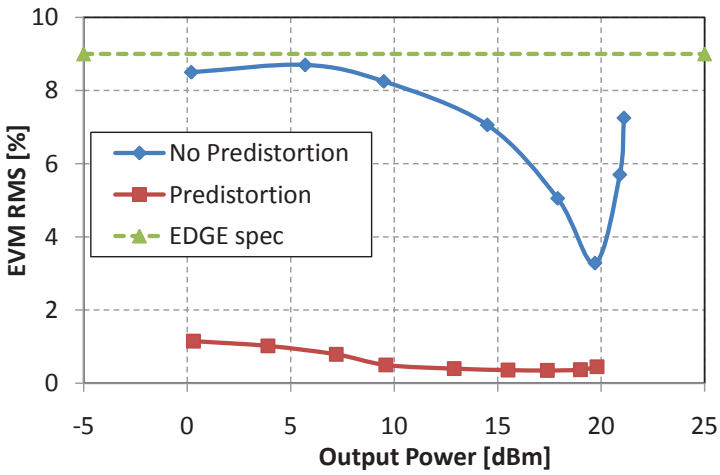


Figure 7.22: Measured EVM rms (EDGE) with and without the digital predistortion versus the average output power delivered to a 50 Ω load.

and Fig. 7.20 is obvious that it is problematic to model the very low input signal amplitudes. The modeled AM-AM and AM-PM characteristics of EDGE and WCDMA are practically identical, which means that the implemented cascode PA has no significant memory effects in the frequency band from 200 kHz to 3.84 MHz.

Fig. 7.21 shows the measured AM-AM characteristic of the cascode PA, the predistortion function and the simulated transfer characteristic of the PA after the predistortion.

7.2.2 EDGE signal experimental results

The measured results show the performance comparison using no digital predistortion or using the static predistortion based on the dynamic AM-AM characteristic, which was

described in Section 7.2.1. The measured error vector magnitude (EVM) versus output power is shown in Fig. 7.22. Even though, the EVM without predistortion is below the required 9 % imposed by the standard, it is much higher than that of state-of-the-art PAs. When the predistortion is employed the EVM is kept below 1.2 %.

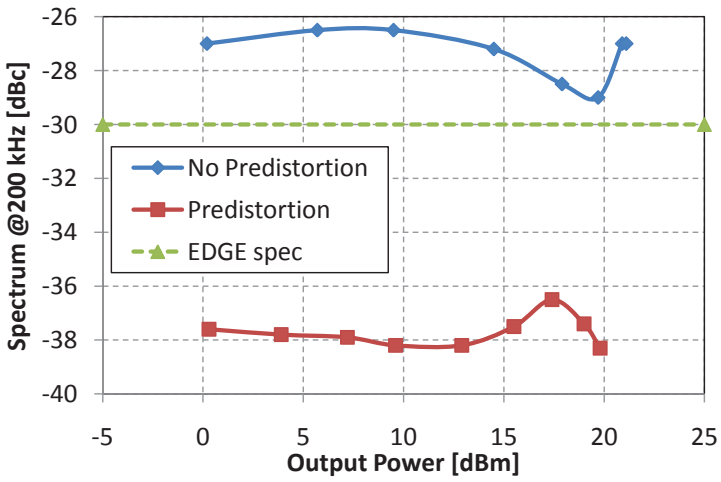


Figure 7.23: Measured relative output power spectrum (EDGE) at 200 kHz frequency offset with and without the predistortion versus the average output power delivered to a 50 Ω load. The resolution bandwidth (RBW) is 30 kHz.

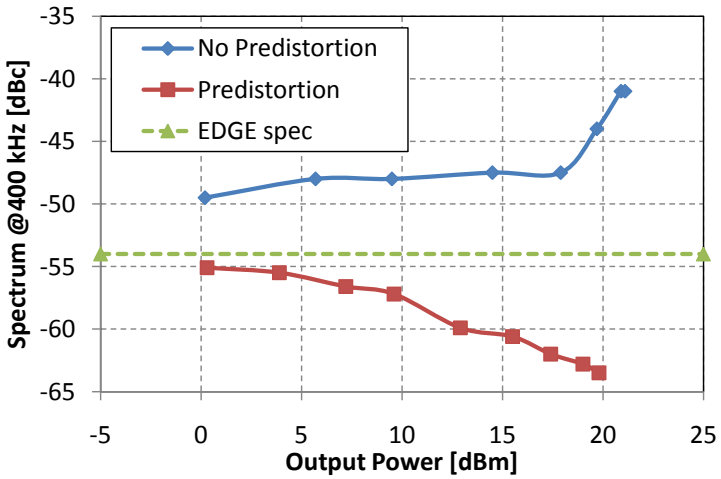


Figure 7.24: Measured relative output power spectrum (EDGE) at 400 kHz frequency offset with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

The next three figures show the spectrum mask measurement versus output power. In Fig. 7.23 the spectrum mask at 200 kHz frequency offset is shown. The non-predistorted PA exhibits a very high out of band non-linearity and therefore the EDGE standard is not met. By applying predistortion the spectrum is well confined below the required limit. The measured output spectrum in Fig. 7.24 shows very similar behavior.

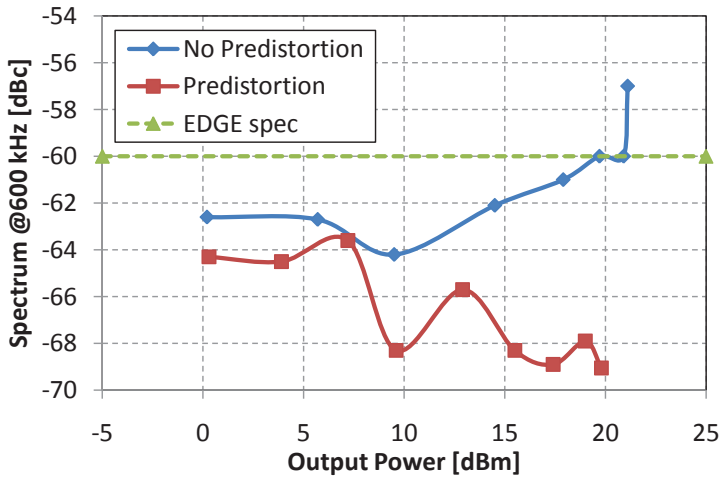


Figure 7.25: Measured relative output power spectrum (EDGE) at 600 kHz frequency offset with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

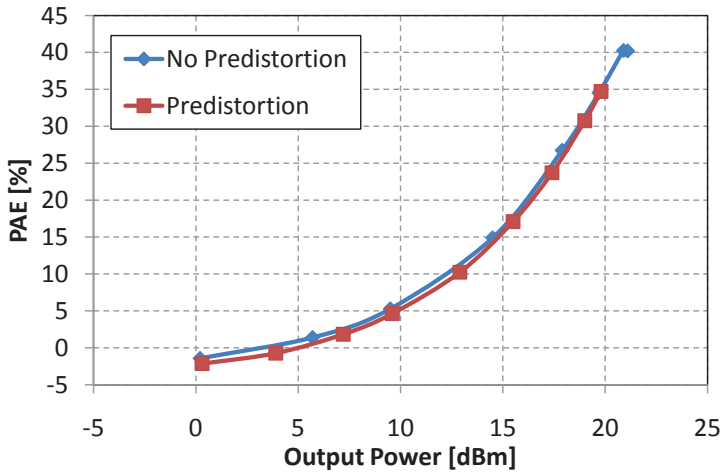


Figure 7.26: Measured power added efficiency (EDGE) with and without the predistortion as a function of the average output power delivered to a 50 Ω load.

It can be observed that the required limit is met very tightly even using the digital predistortion (with almost no headroom at lowest output power). The low output power can be difficult to linearize by a single polynomial based AM-AM and AM-PM predistortion. The output spectrum at 600 kHz frequency offset in Fig. 7.25 violates the standard only for the highest output power. This is corrected by the digital predistortion.

The PAE versus output power is shown in Fig. 7.26. The peak PAE is 40 % without pre-distortion and 35 % using predistortion. The decrease is due to that the predistorted PA provides lower peak output power than the non-predistorted. The PAE in the 0 dBm to 20 dBm range is approximately identical for both pre-distorted and not predistorted case. The PAE exhibits negative numbers when the output power drops below the input

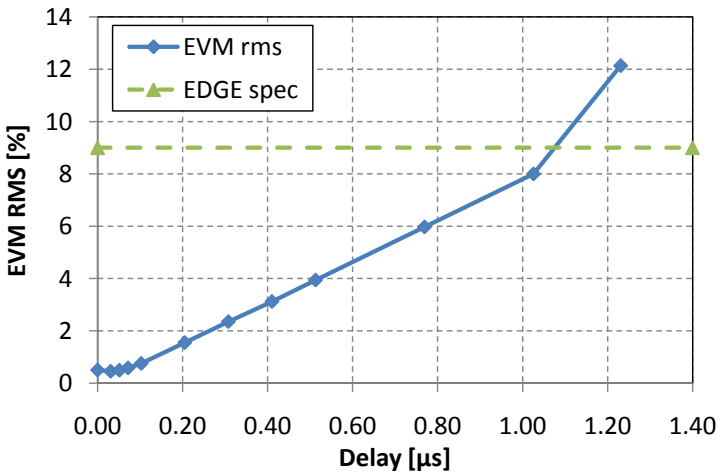


Figure 7.27: Measured EVM RMS (Root Mean Square) as a function of the delay between the amplitude and phase path (EDGE).

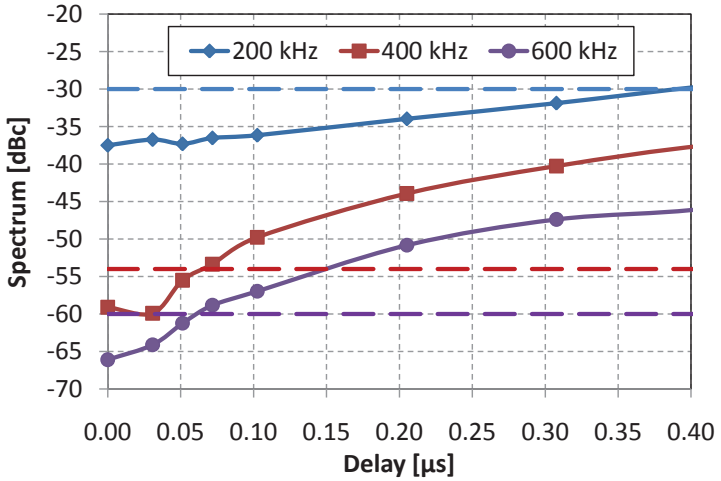


Figure 7.28: Measured relative output power spectrum (EDGE) at 200/400/600 kHz frequency offset versus the delay between the amplitude and phase path. The dashed lines are the corresponding specs. The RBW is 30 kHz

power.

The effect of delay between amplitude and phase paths is shown in Fig. 7.27 and Fig. 7.28. The EVM is not as sensitive to the time delay as is the output spectrum [Reynaert & Steyaert 2005]. The EDGE standard is met even the time delay of 1 μs is introduced between the amplitude and phase paths. The spectrum mask requirement is much more stringent and allows only 50 ns delay. The limit on the maximum allowable delay between the phase and amplitude in the cascode modulated PA is set by the spectrum mask at 400 kHz and 600 kHz frequency offset.

7.2.3 WCDMA signal experimental results

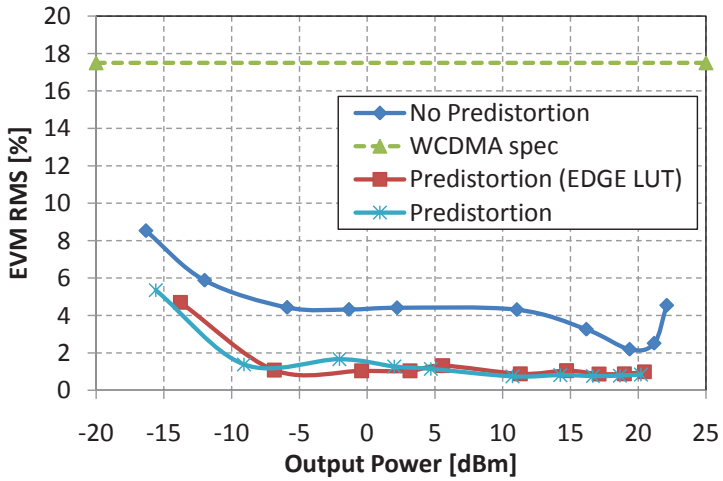


Figure 7.29: Measured EVM RMS (Root Mean Square) with and without the digital predistortion versus the average output power delivered to a 50 Ω load (WCDMA).

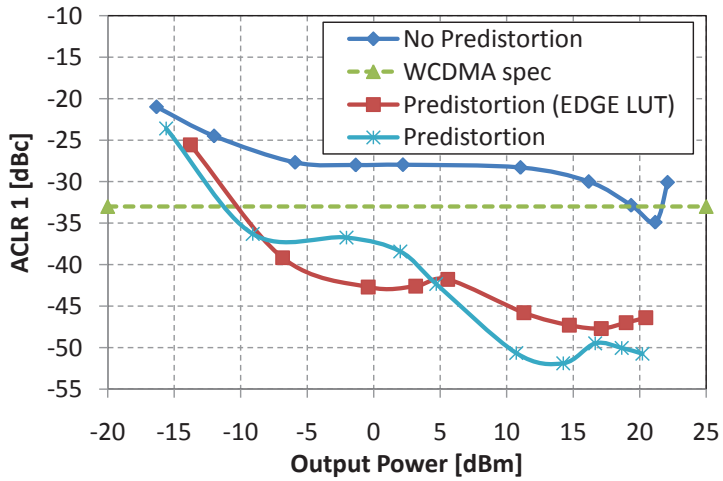


Figure 7.30: Measured adjacent channel leakage power ratio (WCDMA) with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

The measured EVM versus output power of WCDMA modulated cascode PA is shown in Fig. 7.29. The figure shows the results without predistortion, with predistortion using EDGE LUT and with predistortion LUT based on the WCDMA signal. The main differences between the EDGE and WCDMA look-up tables are that the EDGE LUT is based on the input signal with narrower modulation bandwidth and higher minimum output power than the WCDMA one. Both modulations have the same 3.4 dB PAR. Generally, a better performance using WCDMA LUT can be expected (for output power below 0 dBm the EDGE LUT coefficients are constant). Both predistortion coefficients

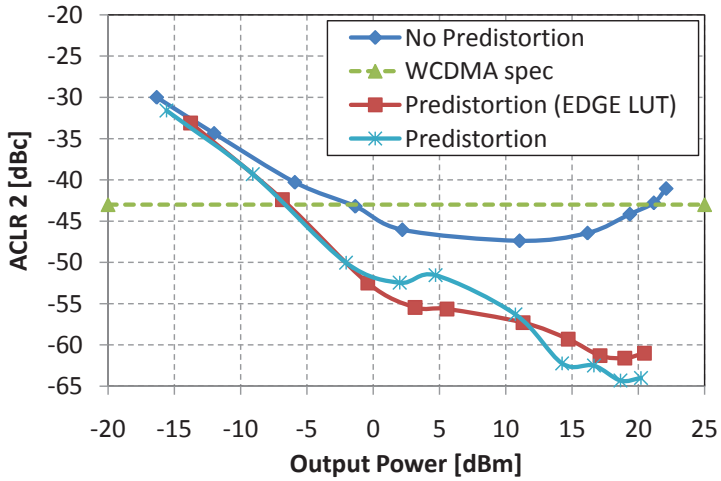


Figure 7.31: Measured alternate channel leakage power ratio (WCDMA) with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

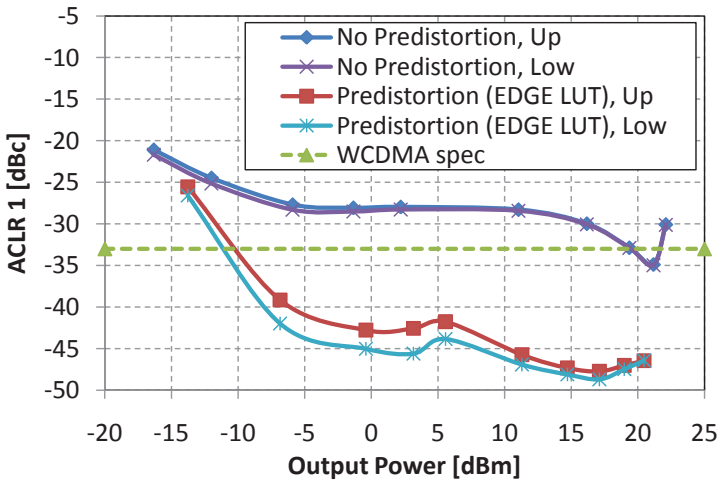


Figure 7.32: Measured adjacent channel leakage power ratio asymmetry (WCDMA) between upper and lower band with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

are calculated using the same polynomial order. As it can be seen from Fig. 7.29 there is a difference between the two predistortion but the improvement using WCDMA LUT is small. This is due to the limiting capabilities of the linearization of very small amplitudes. The maximum output power dynamic range of the cascode modulation is 39 dB (based on the "No predistortion" curve in Fig. 7.29).

The adjacent (ACLR1) and alternate (ACLR2) channel leakage ratios are shown in Figs. 7.30 and Fig. 7.31. ACLR1 and ACLR2 are the main linearity indicators. The worse of the two numbers, upper or lower ACLR1 and ACLR2, is used in Fig. 7.31. Both ACLR1 and ACLR2 don't meet the 3rd Generation Partnership Project (3GPP)

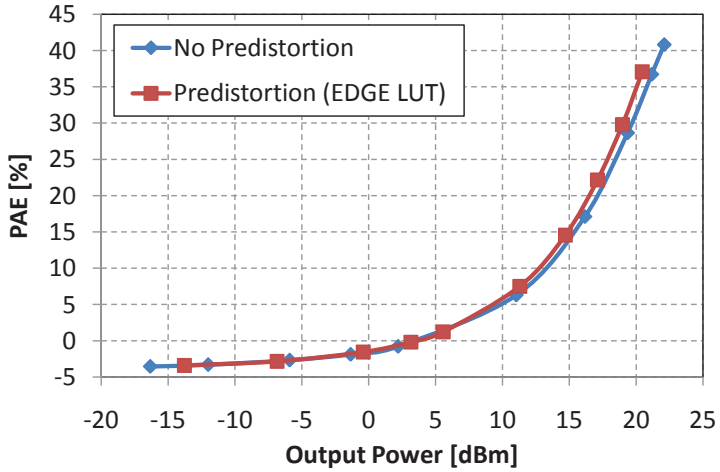


Figure 7.33: Measured power added efficiency (WCDMA) with and without the predistortion as a function of the average output power delivered to a 50 Ω load.

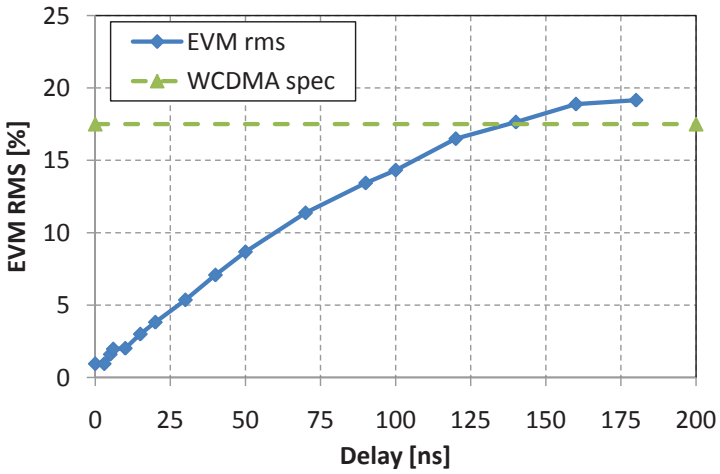


Figure 7.34: Measured EVM RMS (Root Mean Square) as a function of the delay between the amplitude and phase path (WCDMA).

standard without using the predistortion. Even by using the predistortion, the linearity requirement is violated for output powers below -5 dBm. Therefore, in this application the usable output power dynamic range is reduced to 29 dB. At very low output power the predistorted curves are approaching the non-predistorted curve, which means that the predistortion is not effective in this region. As mentioned in Section 7.2.1 the poor predistortion performance at lowest output power levels is caused by that only a single LUT predistortion is used to model the entire AM-AM characteristic of the proposed PA. Both predistortion look-up tables leads to the same linearity improvement and therefore for simplicity in the next figures only the EDGE LUT is considered.

After applying the predistortion the output power spectrum becomes asymmetrical (see Fig. 7.32). This is caused by the non-ideal phase cancellation of the 3rd order

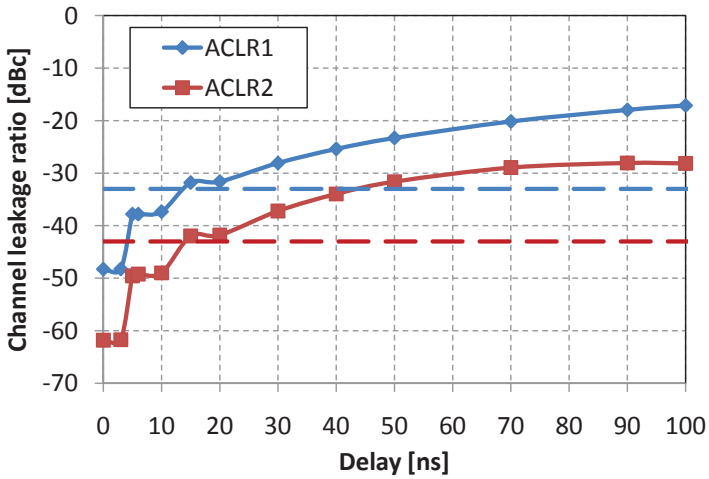


Figure 7.35: Measured alternate (ACLR1) and adjacent (ACLR2) channel leakage power ratio (WCDMA) versus the delay between the amplitude and phase path. The dashed lines are the corresponding specs. The RBW is 30 kHz.

intermodulation products during the predistortion. The alternate channel leakage ration exhibit similar behavior but the asymmetry is lower.

Fig. 7.33 shows the PAE versus output power. The PAE is slightly higher than that using the EDGE modulated input signal (see Fig. 7.26). The PAE exhibits negative numbers for the output powers below approximately 3.5 dBm. This is because the input power of the PA is not adjusted by the power level (available input power is constant for all measurements at 3.5 dBm).

The EVM and channel leakage ratio versus time delay between amplitude and phase signals are shown in Fig. 7.34 and Fig. 7.35. Similar to EDGE, the EVM is not the limiting factor. EVM allows a 135 ns delay but the channel leakage ratio (ACLR1 and ACLR2) limits the delay to 15 ns. Both ACLR1 and ACLR2 are equally sensitive to the amplitude and phase delay mismatch.

Chapter 8

Summary

Contents

8.1 Summary

This thesis is devoted to the RF power amplifiers design and analysis. Modern wireless systems put strong demands on the PAs. Beside the traditional high efficiency and linearity requirements, a number of additional requirements emerges. Multi-band and multi-standard transmitters are attracting more and more research interest.

There are various PA classes traditionally divided into linear and switch-mode groups. Nowadays the linear PAs represent the industrial mainstream but the limited efficiency, especially when signals with high PAPR are amplified, is their main disadvantage. On the other hand, switch-mode PAs offer high efficiency but linearization technique is required to meet the stringent TX linearity requirements. Novel PA classes that are utilizing the waveform engineering approach have recently appeared but this concept still has major limitations when it comes to on-chip implementation.

The polar transmitter topology seems to be a promising candidate for the next generation transmitter. It provides significant advantages but it also has drawbacks that need to be overcome. The major advantage of the polar transmitters is that they can accommodate the switch-mode PAs. Switch-mode PAs have generally high efficiency but also high non-linearity. The main issues are limited dynamic range, sensitivity to the timing mismatch between the AM and PM paths and high BW requirements. It is rather challenging to design a highly efficient high BW supply modulator.

In order to address all these needs a class-E PA utilized in the polar transmitter seems to be good solution. One of the main limitations of the class-E PA is its reliability.

In this thesis a novel concept that addresses the reliability and supply modulation issues is proposed. The proposed cascode modulated class-E PA satisfies the reliability requirement. By modulating the cascode transistor input voltage the output voltage is modulated. A supply voltage modulator used with the conventional supply voltage modulation technique is not needed.

The proposed cascode modulated class-E PA also faces some challenges. It has high AM-AM non-linearity and therefore linearization is required. The implemented CMOS

PAs use bond-wire on-chip inductors that are difficult to control and the repeatability of the process is rather low. The class-E PA is very sensitive to the output network changes and using the manually bonded wire inductors is not the optimum solution. The cascode class-E PA has also lower efficiency than the single transistor class-E PA. Taking into account that single transistor class-E PA requires lossy supply modulator the efficiency of both topologies is approximately on a par.

The model of the cascode class-E PA presented in this work is an important part of the cascode modulated class-E PA concept. Two DC models of the RF cascode PA are proposed. The analytical model is built using the simplified transistor equations. The calculated output current and output power based on the analytical model are in reasonably good agreement with the simulated waveforms.

The concept of the cascode modulated class-E PA is extensively analyzed in this thesis by means of simulations. The experimental chapter contains the measured results that were obtained using the PA prototypes implemented in 0.18 μm CMOS technology.

The thesis offers self-contained analysis and design guidelines for the cascode modulated class-E PA design. Various design aspects are discussed in detail. The thesis also contains an extensive circuit analysis based on simulations. A model of the cascode modulated class-E PA both on circuit level and analytical level is proposed. The performance of the cascode modulated class-E PA is verified by measurements. The performance is tested with CW, EDGE and WCDMA modulated input signals.

8.2 Further research

There are still several aspects of the cascode class-E modulation that can be further investigated. One of the most important is the bandwidth estimation and enhancement. Polar transmitters require much larger BW in both amplitude and phase path and this is becoming more and more critical with recently introduced high bandwidth 4G standard.

From the perspective of practical implementation in RF products it would be interesting to characterize the temperature dependence of the cascode modulated class-E PA. The goal is to minimize the performance change with temperature and process variations. This becomes critical especially in a transmitter with static digital predistortion.

Another research direction can lead towards a fully integrated on-chip PA. In this work the most critical inductors from the efficiency perspective were implemented by bond-wires. The repeatability of manual bonding procedure is low. The output matching circuit can be substituted by a distributed active transformer.

Varying supply voltage modulation can be also utilized in parallel with the cascode modulation and input power level adjustments in order to maximize the efficiency. The supply voltage can be adjusted with the power level signal that has much lower bandwidth than the amplitude modulated signal. This significantly loosens the requirements on the supply voltage modulator design. The input driver power can be also dynamically adjusted exploiting the fact that the input power required to operate the switching transistor can be decreased when the output power (switch current) is low.

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Appendix A

Bond-wire inductor model

The basic wire inductor model can be found in [Bahl 2003]. The free-space inductance of the wire (it is assumed that the wire is a straight line) can be expressed as

$$L\,[nH] = 2 \cdot 10^{-4} l \left[\ln \frac{2l}{d} + \sqrt{1 + \left(\frac{2l}{d}\right)^2} + \frac{d}{2l} - \sqrt{1 + \left(\frac{d}{2l}\right)^2} + C \right] \tag{A.1}$$

and if $l >> d$ then Eq.A.1 reduces to

$$L\,[nH] = 2 \cdot 10^{-4} l \left(\ln \frac{4l}{d} + 0.5\frac{d}{l} - 1 + C \right) \tag{A.2}$$

where d and l is the wire diameter and length respectively. The parameter C is a frequency dependent correction factor and it can be calculated as

$$C = 0.25 \tanh \frac{4\delta}{d} \tag{A.3}$$

$$\delta = \frac{1}{\sqrt{\pi \sigma f \mu_0}} \tag{A.4}$$

where σ, f, μ_0 and δ are conductivity of the wire material, frequency in gigahertz, permeability of free space and skin depth. The resistance of the wire is given as

$$R = \frac{R_s l}{\pi r^2} \tag{A.5}$$

where R_s is the sheet resistance of the wire in ohms per square and r is the radius of the wire. At a frequency of 1 GHz the skin depth of gold is 2.4 μm. Hence, only a part of the actual cross section of the wire conducts the current. The conductive area A can be calculated as

$$A = \pi(r^2 - (r - \delta)^2) \tag{A.6}$$

and Eq. (A.5) can be rewritten as

$$R \doteq \frac{R_s l}{A} \doteq \frac{R_s l}{\delta \pi d} \tag{A.7}$$

For gold bond-wire with radius 12.5 μm and sheet resistance of 23.5 Ωm the series resistance is 0.125 Ω per mm length.

The bond-wire inductor has a vertical bend and also a certain height over the substrate. In the first order approximation the bending and height of the bond-wire can

be translated into an additional wire length. The more complex model that accounts for the bond-wire wire curvature can be found in [Alimenti *et al.* 2001]. The frequency dependent bond-wire characterization was published in [Lee 1995].

The bond-wire inductor has also a parasitic capacitance associated with it. The most significant is the parasitic capacitance of the bond-pad. The bond-pad can be modeled by a series connection of the capacitor and resistor. Their values depend on the size of the bond-pad, number of conductive layers used in the bond-pad and on the CMOS technology process (metallization layers spacing etc.). The typical value of the parasitic capacitance and resistance of the bond pad used in the experimental work (Chapter 7) is a 100 fF and 80 mΩ respectively. There are two types of bond-wire inductors used in the cascode class-E PA: on-chip inductor (chip-to-chip) and chip-to-PCB inductor.

The industrial standard for bond-wire modeling JESD59 is published by EIA/JEDEC in [EIA/JEDEC 1997]. This model is implemented in the three dimensional electromagnetic solver in Agilent ADS (EMDS). The bond-wire inductor is divided into four segments and its parameters are calculated separately. According to this model the inductance of single bond-wire is calculated as

$$L\,[nH] = 2 \cdot 10^2 l \left(\ln \frac{2l}{r} - 1 \right) \tag{A.8}$$

where l and r are in cm. The resistance is the same as in Eq. (A.7). The calculated bond-wire inductance and resistance based on JEDEC model are shown in Fig. A.1.

Due to the unpredictable nature of the manual bonding process the bond-wire model has generally high uncertainty. Therefore, the inductance value of bond-wire will differ from bond to bond.

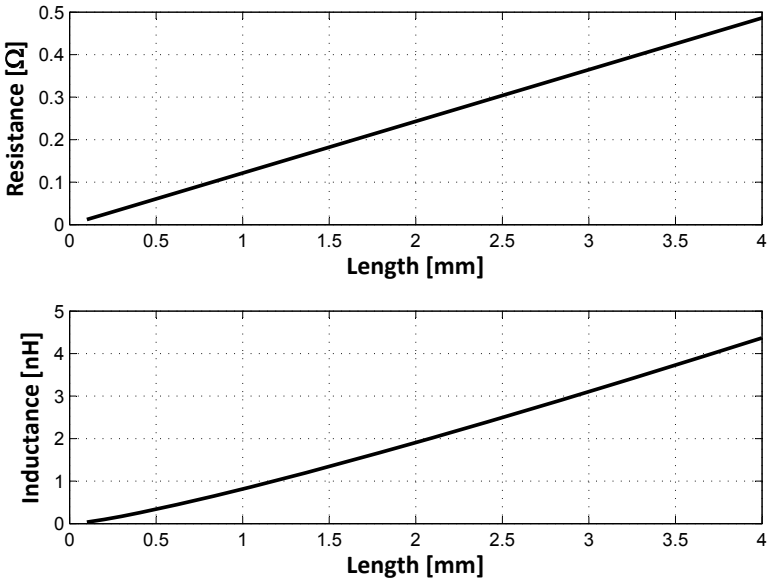

Figure A.1: Calculated resistance and inductance of the bond-wire versus the wire length.

Appendix B

Reprint of publications

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[1] D. Sira, P. Thomsen and T. Larsen, "Output Power Control in Class-E Power Amplifiers," IEEE Microwave and wireless components letters, vol. 20, no. 4, pp. 232-234, Apr. 2010.

[2] D. Sira, P. Thomsen, T. Larsen, "A cascode modulated class-E power amplifier for wireless communications," Microelectronics Journal, vol. 42, no. 1, pp. 141-147, Jan. 2011.

[3] D. Sira, and T. Larsen, "WCDMA/EDGE cascode modulated polar PA," submitted to IEEE Transactions on Microwave Theory and Techniques, 2010

Output Power Control in Class-E Power Amplifiers

Daniel Sira, Pia Thomsen, and Torben Larsen, *Senior Member, IEEE*

***Abstract*—A technique is presented to facilitate power control of cascode class-E power amplifiers (PAs). It is shown that by controlling the signal applied to the gate of the cascode transistor, the transmit power is changed. The main advantage of the proposed technique is a high 36 dB output power control range (PCR) compared to 20 dB for the traditional approach. This fulfills the requirements of the GSM standard on the PCR at all power levels and all frequency bands (for GMSK modulation). The concept of the cascode power control of class-E RF PA operating at 2.2 GHz with 18 dBm output power was implemented in a 0.18 μm CMOS technology, and the performance has been verified by measurements. The PA has been tested by a single tone, and by a GMSK modulated input signal.**

***Index Terms*—Cascode, class-E, CMOS power amplifier, dynamic range, power control.**

I. Introduction

GENERALLY, switch mode PAs are well suited to constant envelope modulation schemes such as Gaussian minimum-shift keying (GMSK) or Gaussian frequency-shift keying (GFSK). In addition, wireless communication standards are employing power control techniques to reduce interference (congestion) in the network, and power consumption of the mobile device.

There have been several fully integrated implementations of class-E PAs in CMOS reported—see e.g., [1]–[4]. The conventional power control of a switch mode PA is implemented by adjusting the supply voltage [5]. The conventional technique offers a limited output power control range, especially at low supply voltage [2]. The PCR can be increased by adjusting the input power, but that is generally not desirable in a switch mode class-E PA.

An alternative to the traditional power control scheme is presented in this letter where a cascode voltage controls the output power of the PA. The main advantage of the proposed technique compared to a conventional supply voltage power control technique is increased output power control range.

II. Power Control Techniques

Power control techniques for a constant envelope modulation schemes can be used to improve the efficiency of the PA. For a switch mode PA, the input power is expected to be constant, and therefore a supply voltage power control technique (SVPCT) is traditionally employed.

Manuscript received October 07, 2009; revised December 04, 2009. First published March 15, 2010; current version published April 07, 2010.

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Digital Object Identifier 10.1109/LMWC.2010.2042562

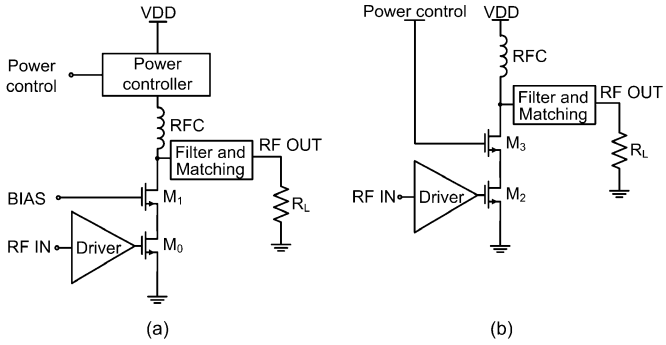

Fig. 1. (a) Conventional power control technique. (b) Proposed power control technique.

A. Supply Voltage Power Control Technique (SVPCT)

The supply voltage power control technique is depicted in Fig. 1(a). The output power is controlled by a power controller.

The output power control range is the maximum range over which the PA output power can be controlled. The GSM900 standard (GMSK modulation) for a mobile station specified by European Telecommunications Standards Institute (ETSI) requires the power control range of 24 dB (class 5) to 34 dB (class 2). In the DCS1800 and PCS1900 frequency bands, the standard requires 24 to 36 dB power control range. The power control range can be written as

$$\mathrm{PCR\,[dB]} = P_{\mathrm{out,max}} - P_{\mathrm{out,min}} = 20\log_{10}\frac{V_{\mathrm{dd,max}}}{V_{\mathrm{dd,min}}} \quad (1)$$

where $P_{\mathrm{out,max}}$ and $P_{\mathrm{out,min}}$ are maximum and minimum average output power in dBm. It is assumed the load impedance is constant. A low voltage class-E PA with a constant input power has a very limited PCR. For a supply voltage range of 0.2 to 1.8 V the PCR is 19.1 dB.

The main drawbacks of SVPCT are limited output power control range, high sensitivity to load variations, and that the switch mode power controller is placed in the high power path [6]. Since the supply voltage power controller pulls a high current to the PA, the placement in the high power path (in series with the RF choke) makes the efficiency the most important parameter. The efficiency of state-of-the-art power converters is up to 90% at the maximum output power [5].

It is important to note, that if the supply voltage drops to zero, there is still some output voltage. This is due to feed-through from the input to the output. In order to maximize the output power control range, the supply voltage controller must be able to reach the positive battery supply rail and also to provide close to zero output voltage. The maximum supply voltage is limited by the reliability of the CMOS PA [1].

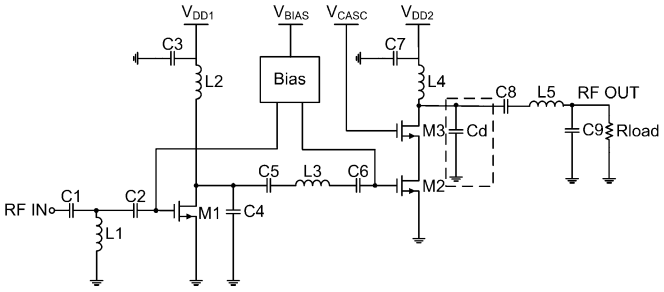

Fig. 2. Class-E power amplifier schematic.

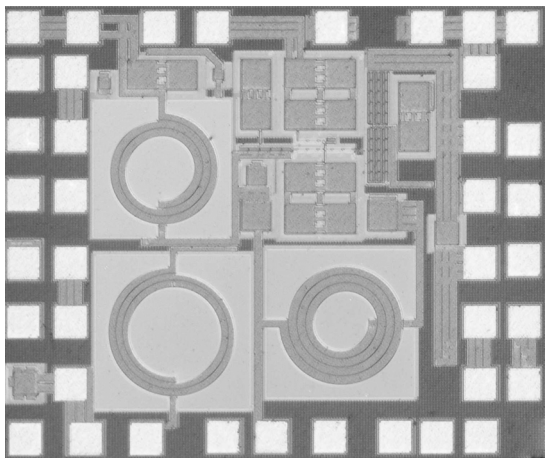

Fig. 3. Microphotograph of the PA.

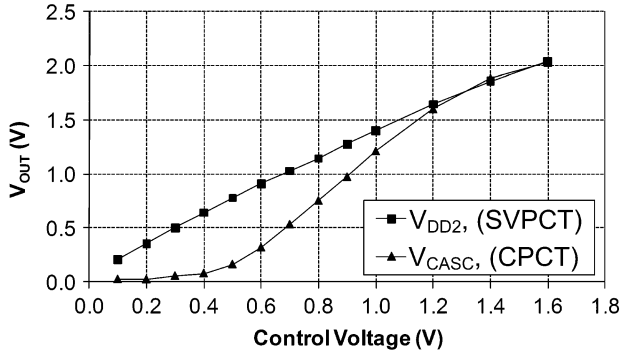

Fig. 4. Measured effective RF voltage ($V_{\rm OUT}$) across a 50 Ω load versus $V_{\rm DD2}$ ($V_{\rm CASC} = 1.6$ V) and $V_{\rm CASC}$ ($V_{\rm DD2} = 1.6$ V). The available input power was 3.5 dBm at a frequency of 2.2 GHz.

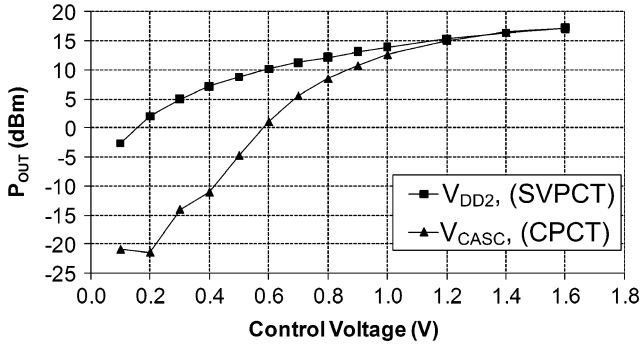

Fig. 5. Measured average in-band power of the PA ($P_{\rm OUT}$) delivered to a 50 Ω load versus $V_{\rm DD2}$ ($V_{\rm CASC} = 1.6$ V) and $V_{\rm CASC}$ ($V_{\rm DD2} = 1.6$ V). The input signal is a GMSK modulated signal ($\rm BT = 0.3$) at a carrier frequency of 2.2 GHz with 3.5 dBm available average input power. The measurement bandwidth is 200 kHz around the carrier.

B. Cascode Power Control Technique (CPCT)

The proposed alternative power control technique is shown in Fig. 1(b). The power control signal is applied to the gate of the cascode transistor M3.

In the CPCT the input voltage on the gate of the cascode transistor M3 is divided between $V_{\rm gs,M3}$ and $V_{\rm ds,M2}$ (see Fig. 2). By decreasing the input voltage, $V_{\rm ds,M2}$ also decreases until $V_{\rm CASC} \approx V_{\rm th,M3}$ when $V_{ds,\rm M2}$ drops close to zero ($V_{\rm th,M3}$ is the threshold voltage of the transistor M3). For the SVPCT, the supply voltage can be decreased almost to zero. Therefore, the input dynamic range of the CPCT is approximately one threshold voltage lower than in the SVPCT. In the technology used for the experimental work in Section III, the threshold voltage is 0.55 V. By taking into consideration the subthreshold region of the transistor, $V_{\rm CASC}$ can be decreased approximately to 0.3 V.

The CPCT also provides higher output power control range than the SVPCT. This is because the capacitive coupling between the input (gate of M2) and the output (drain M3) is reduced, provided the cascode transistor M3 is in saturation. In the CPCT this is fulfilled for the whole $V_{\rm CASC}$ range.

The PAE of the CPCT is higher than of the SVPCT due to the lower power losses associated with parasitic capacitances charging/discharging. The voltage across M2 is limited by the cascode M3. By decreasing the supply voltage in the SVPCT, the transistor M3 goes into the linear region. This increases the voltage swing across M3. Therefore, the dissipated power due to the charging/discharging of parasitic capacitances at the common node of M2 and M3 is also increased. On the other hand, by decreasing the $V_{\rm CASC}$ voltage in the CPCT M3 stays in saturation and M2 stays in the linear region. The voltage swing across M3 is limited and the CPCT has lower power loss than SVPCT.

In the proposed design, the finite RF choke (RFC) technique was used and the maximum drain voltage peak is reduced to 2.5 $\rm V_{dd}$ [3].

III. Measurements

Fig. 2 shows the proposed two-stage PA where the class-E output stage (M2 & M3) is driven by a class-E driver stage (M1). A microphotograph of the implemented power amplifier is shown in Fig. 3. The area of the PA is 1.2×1.0 mm^2. Supply voltages are filtered on the PCB (capacitors C3 and C7 in Fig. 2). Inductors L4 and L5 are realized by bond-wires. The adaptive power control circuit was not implemented in the prototype, and therefore the performance is evaluated for specific values of $V_{\rm CASC}$ and $V_{\rm DD2}$ voltages.

The measured AM-AM characteristic is depicted in Fig. 4. The input dynamic range of the CPCT is 14.5 dB (from 0.3 to 1.6 V) whereas SVPCT offers 24 dB (from 0.1 to 1.6 V). The AM-AM curve of CPCT is non-linear but that is of no major concern in the power control of the constant envelope modulated PA. The available power from the source is chosen as 3.5 dBm

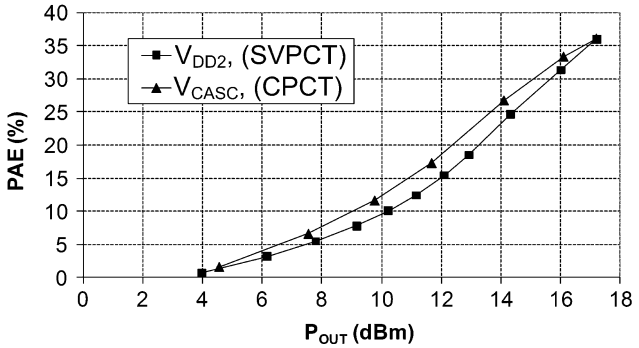

Fig. 6. Measured power added efficiency (PAE) versus output power ($P_{\rm OUT}$) delivered to a 50 Ω load. The input signal is a GMSK modulated signal ($\rm BT = 0.3$) at carrier frequency of 2.2 GHz with 3.5 dBm available average input power. The parameter is $V_{\rm DD2}$ ($V_{\rm CASC} = 1.6$ V) and $V_{\rm CASC}$ ($V_{\rm DD2} = 1.6$ V).

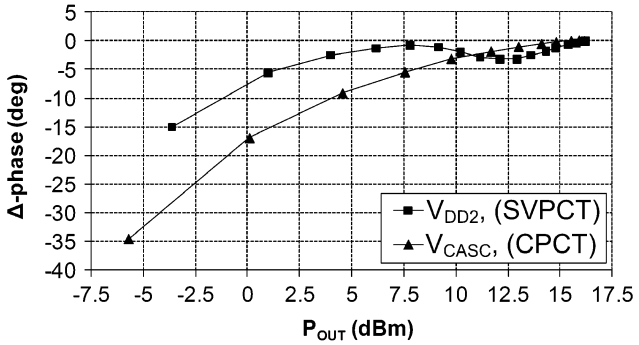

Fig. 7. Measured phase advance across the PA versus power ($P_{\rm OUT}$) delivered to a 50 Ω load. The parameter is $V_{\rm DD2}$ ($V_{\rm CASC} = 1.6$ V) and $V_{\rm CASC}$ sweep ($V_{\rm DD2} = 1.6$ V). The available input power was 3.5 dBm at a frequency of 2.2 GHz.

to ensure that the switching power transistor works as a switch as intended.

Although the prototype was not designed to meet any particular standard, it was tested with a GMSK signal. Fig. 5 shows the measured average in-band output power. It can be seen that the SVPCT provides approximately 20 dB output power control range (from -2 to 18 dBm), roughly the same as [2] and [7]. The CPCT exhibits a much higher output power control range of 36 dB. This is a 16 dB larger control range than of the SVPCT.

The measured results in Fig. 6 show that the cascode modulated PA is more power efficient than the power supply modulated PA, which is in agreement with the analysis made in Section II-B. The PAE of the cascode modulated PA is up to 3% higher compared to the power supply modulated PA. The maximum PAE of the power amplifier is 35%. The measured output spectrum mask was lying below the GSM specification mask with a large margin over the whole $V_{\rm CASC}$ voltage range. The measured RMS phase error is 0.2°.

Fig. 7 shows the AM-PM distortion for a fixed input power. The phase distortion of the CPCT is larger than that of the SVPCT. This is due to the parasitic drain capacitance variation of the cascode transistor (M3) on the $V_{\rm CASC}$ voltage, and due to the Miller drain-gate capacitance of the switching power transistor (M2). The high AM-PM doesn't deteriorate the phase error (or EVM) in the transmitting signal because the power control signal has a very low frequency (for GSM/EDGE it is approximately 16.6 Hz) and its value can be considered constant during the frame period.

TABLE I
PERFORMANCE COMPARISON OF THE SELECTED POWER AMPLIFIERS

	Technology [μm]	Frequency [GHz]	VDD [V]	Peak P_{out} [dBm]	Peak PAE [%]	P_{out} Dynamic Range [dB]
Ref. [2]	0.18	1.9	3.3	32	40	20
Ref. [4]	0.18	2.4	2.4	23	42	-
Ref. [7]	0.25	1.4	1.5	25	49	17
Ref. [8]	0.35	2.4	1.0	18	33	-
This work	**0.18**	**2.2**	**1.6**	**18**	**35**	**35**

The performance comparison between the proposed PA and a published CMOS PAs is shown in Table I [8].

IV. CONCLUSION

This letter presents a power control technique of a cascode class-E PA. The proposed cascode power control technique provides a high 36 dB output power control range. This is about a 16 dB larger control range compared to a conventional supply voltage power control technique. It also provides a slightly higher PAE at high output power than supply voltage power control technique. The cascode power control technique appears attractive because of elimination of the switch mode power switch needed in the supply voltage power control technique. A single tone and GMSK modulated input signals were used to characterize the PA performance. The measurements have been performed on a 0.18 μm CMOS implemented power amplifier capable of delivering 18 dBm output power to a 50 Ω load at 2.2 GHz.

ACKNOWLEDGMENT

The authors thank P. B. Jensen and B. Kroyer, Aalborg University, for technical support, and P. Madsen and J. C. Lindof, Texas Instruments, for helpful discussions.

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Microelectronics Journal 42 (2011) 141–147

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A cascode modulated class-E power amplifier for wireless communications

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ARTICLE INFO

Article history:
Received 16 September 2009
Received in revised form
13 August 2010
Accepted 16 August 2010
Available online 20 September 2010

Keywords:
Cascode
Class-E
CMOS
Dynamic range
EDGE
Polar modulation
RF power amplifier

ABSTRACT

A cascode modulated CMOS class-E power amplifier (PA) is presented in this paper. It is shown that by applying a modulated signal to the gate of the cascode transistor the output power is modulated. The main advantage of the proposed technique is a high 35 dB output power dynamic range. The peak power added efficiency (PAE) is 35%. The concept of the cascode power control of class-E RF PA operating at 2.2 GHz with 18 dBm output power was implemented in a 0.18 μm CMOS technology and the performance has been verified by measurements. The prototype CMOS PA is tested by single tone excitation and by enhanced data rates for GSM evolution (EDGE) modulated signal. Digital predistortion is used to linearize the transfer characteristic. The EDGE spectrum mask is met and the rms error vector magnitude (EVM) is less than 4° in the entire output power range.

1. Introduction

Switch-mode power amplifiers are becoming more and more popular in modern RF transmitter design — especially due to their high efficiency [1]. They are well suited for constant envelope modulation systems such as GSM and Bluetooth. These systems are employing power control techniques to maximize the spectral usage and to reduce the power consumption of the mobile device. More recent communications systems (EDGE, WCDMA, WiMAX, LTE) are all using both amplitude and phase modulation to increase the data rate and spectral efficiency. The polar transmitter topology allows to combine both high efficiency and linearity assuming a highly efficient PA and amplitude modulator is used. The EDGE signal exhibits approximately 17 dB amplitude variation range, whereas the power control range is up to 33 dB. This results in approximately 50 dB output power variation required by the standard. Therefore, the key parameters of an amplitude modulator are the PAE, dynamic range of the output power and reliability.

There have been several fully integrated implementations of class-E PAs in CMOS reported [1–3]. One of the main limitations of a class-E PA in CMOS technology is its decreased reliability due to the low oxide breakdown voltage [4]. To mitigate this problem a cascode configuration [4] has been proposed. The conventional power control of a switch-mode PA is implemented by adjusting the supply voltage [5] (Fig. 1(a)). Note, that the power supply modulation technique depicted in Fig. 1(a) is using a cascode topology (to improve reliability). The very basic supply modulated class-E PA consists of only a single power transistor.

An alternative to the traditional amplitude modulation scheme is presented in this paper, where the cascode voltage is used to control the output power of the PA (Fig. 1(b)). The self-biased cascode topology [4] alleviates the problem of excessive voltage that may damage the power transistor but this architecture is not suitable for the cascode modulation because the cascode voltage is assumed to be constant. It was shown earlier that the cascode class-E PA topology is suitable for the output power control but the concept was limited to the DC power control only [6]. This paper demonstrates that the cascode modulation technique is suitable to amplify varying envelope signals.

The main advantage of the proposed technique compared to a conventional supply voltage modulation technique is the increased output power dynamic range and no need for an external supply modulator. The prototype CMOS PA is tested by single tone and EDGE modulated signal. A predistortion (PD) linearization technique is used to meet the EDGE standard.

The paper is organized as follows. Section 2 describes the power supply and cascode modulation techniques for polar transmitters. In Section 3 the polar modulation implementation and predistortion linearization are discussed. The measurements are summarized in Section 4. The conclusions are presented in Section 5.

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doi:10.1016/j.mejo.2010.08.016

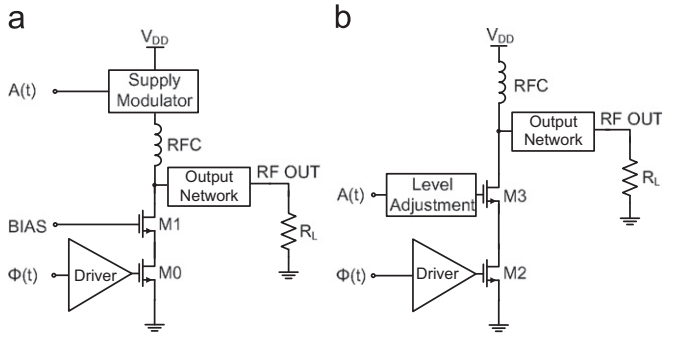

Fig. 1. (a) Conventional power supply modulation technique. (b) Proposed cascode modulation technique.

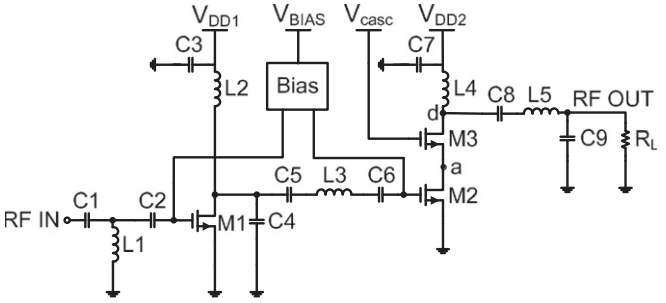

Fig. 2. CMOS class-E power amplifier schematic.

2. Amplitude modulation techniques

For a switch-mode PA the input power is expected to be constant and therefore a linearization technique has to be applied to obtain an amplitude modulated signal at the PA output.

The polar modulation is the most popular linearization technique which enables the use of a switch-mode PA in a varying envelope transmitter [7]. The conventional approach is to modulate directly the supply voltage of the PA [8]. This technique is usually referenced as the supply voltage modulation, power supply modulation or simply drain modulation technique. The supply modulator is a critical part of the RF polar transmitter because it significantly influences the overall efficiency and linearity.

Beside the very basic power control techniques that employ a low drop-out (LDO) regulator or a switching power converter, the supply modulator topology can be implemented using an advanced technique like a pulse-width modulation (PWM), sigma-delta ($\Sigma\Delta$) modulation or delta modulation [8]. The amplitude modulated signal can be converted into pulse-width modulated signal using a sigma-delta modulator [9]. This signal is then applied to the drain of the PA. The common problem of all the advanced techniques is a high quantization noise and hence it is difficult to fulfill the spectral emission mask requirements [8].

An alternative approach to the supply modulation, which is presented in this paper, is to use a cascode modulation technique. The cascode modulation concept can be combined with any of the advanced aforementioned power modulation techniques (PWM, $\Sigma\Delta$ or delta modulation).

2.1. Power supply modulation technique

The power supply modulation technique is depicted in Fig. 1(a). The supply modulator modulates the PA supply voltage according to the amplitude signal $A(t)$.

The power supply modulation of a switch-mode PA is exploiting that the output power is directly related to the supply voltage. The average output power of the class-E PA is proportional to the square of the supply voltage according to

$$P_{\text{out}} = \frac{8}{\pi^2+4}\frac{V_{DD}^2}{R_L} \approx 0.5768 \cdot \frac{V_{DD}^2}{R_L} \tag{1}$$

One of the most important parameters is the output power dynamic range (DR). The DR is the maximum range over which the PA average output power can be controlled. It can be written as

$$DR(dB) = P_{\text{out,max}} - P_{\text{out,min}} = 20\log\frac{V_{DD,max}}{V_{DD,min}} \tag{2}$$

where $P_{\text{out,max}}$ and $P_{\text{out,min}}$ are maximum and minimum output power in dBm. It is assumed the load impedance is constant. The supply voltage variation of 0.1–1.8 V results in 25.1 dB output power dynamic range.

The main drawbacks of the supply modulation technique are limited output power dynamic range, high sensitivity to load variations, and that the supply modulator is placed in the high power path. Since the supply modulator pulls a high current to the PA, the placement in the high power path (in series with the RF choke) makes the efficiency the most important parameter. The efficiency of state-of-the-art switch-mode power converters is around 90% at the maximum output power [5] and falls rather fast when the output power (voltage) is decreasing.

It is important to note that if the supply voltage drops to zero, there is still some output voltage. This is due to feed-through from the input to the output. In order to maximize the output power dynamic range the supply voltage controller must be able to reach the positive battery supply rail and also provide close to zero output voltage.

2.2. Cascode modulation technique

The proposed alternative power control concept is shown in Fig. 1(b). The power control signal is applied to the gate of the cascode transistor M3. The schematic of the proposed cascode modulated class-E CMOS PA is shown in Fig. 2.

In the cascode modulation, the input voltage V_{casc} on the gate of the cascode transistor M3 is divided between $V_{gs,M3}$ and $V_{ds,M2}$ (Fig. 2). By decreasing the input voltage, V_a also decreases until $V_{casc} \approx V_T$ when V_a drops close to zero. The cascode transistor M3 can operate in two regions during the ON period of the switch, the linear or saturation region. Assuming the V_{DD2} is fixed at a nominal value, when the V_{casc} increases from zero the M3 opens into saturation region. By further increasing the V_{casc} the M3 enters the linear region. The transistor M3 is in the linear region when

$$V_{ds,M3} < V_{gs,M3} - V_T = V_{casc} - V_a - 0.55 \tag{3}$$

In the proposed class-E PA (Fig. 2) the M3 is in linear region when $V_{casc} > 1.3$ V (assuming the other voltages are at nominal values).

The power supply modulation technique is exploiting that the supply voltage can be decreased almost to zero. The input dynamic range of the cascode modulation is approximately one threshold voltage lower than in the power supply modulation technique. In the technology used for the experimental work in Section 4 the threshold voltage V_T is 0.55 V. By taking into consideration the sub threshold region of the transistor, V_{casc} can be decreased to 0.3 V.

The minimum output power of the PA is limited by the input power feed-through to the PA output. This is due to the Miller capacitance between the gate and drain of the switching transistor. The feed-through is highest in the single transistor PA. The cascode

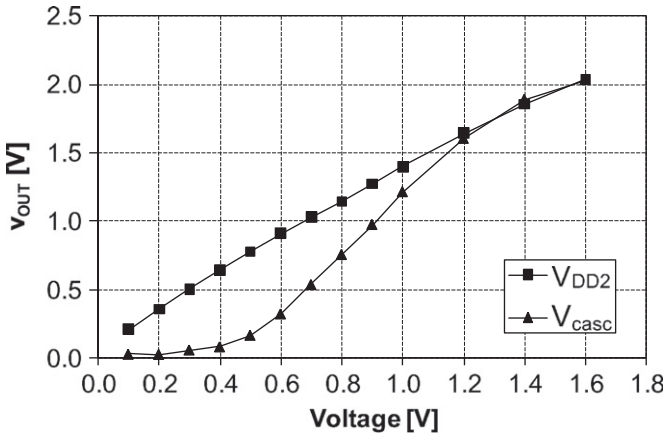

Fig. 3. AM–AM characteristics. The effective output RF voltage (V_{out}) versus V_{DD2} (V_{casc} = 1.6 V) and V_{casc} (V_{DD2} = 1.6 V). The input is a single tone signal of 3.5 dBm at a frequency of 2.2 GHz.

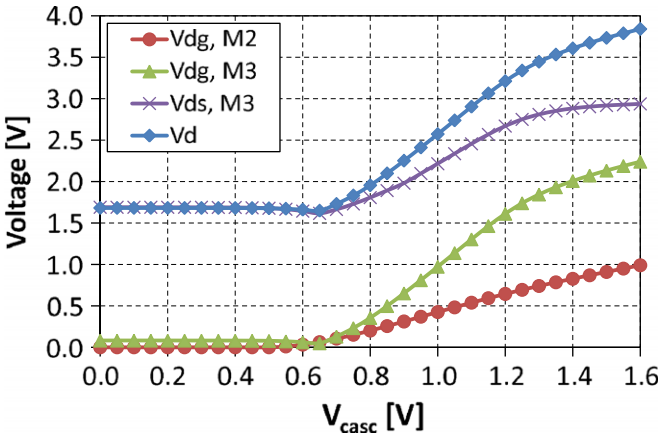

Fig. 4. Simulated peak voltages of CS and CG transistors in the OFF period of the RF cycle as a function of the cascode control voltage V_{casc}.

transistor increases the input–output isolation by reducing the capacitive coupling between the input (gate of M2) and the output (drain M3) nodes. The isolation is improved only when the cascode transistor is in saturation (when it is in the linear region it acts simply as a voltage controlled resistor). The feed-through effect is significant at low output power levels (low V_{casc}) where the cascode transistor is in saturation. At the high output power levels M3 is in the linear region but that has no effect on the dynamic range. The cascode modulation technique provides a higher output power dynamic range than the power supply modulation technique (using either a single transistor or a cascode topology with fixed V_{casc}).

Assuming that all capacitances are voltage independent, the cascode modulated class-E PA will operate as an optimum class-E amplifier. A more realistic model has to include a variation of the parasitic capacitances of M3 when the V_{casc} is modulated. This will lead to a sub-optimum class-E operation. This effect is not investigated in this work.

The AM–AM characteristic of the PA has to meet several criteria in order to amplify an amplitude modulated signal. The attributes like linearity, input and output dynamic range play a crucial role in the PA design for varying envelope signals. The amplitude transfer characteristic is shown in Fig. 3. It can be seen that the AM–AM characteristic is highly non-linear in the entire V_{casc} range.

The exact analytical description of the amplitude transfer function is out of the scope of this paper. A more intuitive approach is to use a polynomial approximation. The AM–AM characteristic can be divided into several sections. From the application point of view the most interesting is the middle part (V_{casc} between 0.4 and 1.6 V). This part can be approximated by

$$V_{\text{out}} = -1.45 \cdot (V_{casc})^3 + 4.08 \cdot (V_{casc})^2 - 1.65 \cdot V_{casc} + 0.15 \quad (4)$$

where the norm of the residuals of this approximation is 0.15. It is obvious that this non-linearity might deteriorate the PA performance to such extent that the telecommunication standard is not met (EVM and the output power spectrum). It is shown in Section 3.1 that the AM–AM characteristic can be linearized by predistortion [2]. Note that the AM–AM characteristic of the supply modulation technique (V_{DD2} curve in Fig. 3) is very linear.

The AM–PM distortion in a cascode modulated PA is mainly due to the parasitic drain capacitance variation of the cascode transistor (M3) on the V_{casc} voltage and due to the Miller drain-gate capacitance of the switching power transistor (M2). The AM–PM predistortion should be applied if the full range V_{casc} variation is used.

2.3. Reliability

The reliability of the CMOS PA is mainly limited by the hot-carrier instability (HCI), and gate-oxide breakdown [10]. If the voltage across the gate-oxide exceeds a certain limit (an IC technology constant) an oxide rapture occurs. Oxide rapture causes a catastrophic and permanent damage to a transistor [11]. HCI is a reliability issue, which leads to a threshold voltage and a drain current shifts over time [12]. Usually, the recommended voltage is 10% above the maximum allowed supply voltage to guarantee a product lifetime of 10 years (given by the technology design rules). In the technology used for experimental work the nominal supply voltage is 1.8 V and the breakdown voltage is 3.5 V.

The main reliability issue for properly designed class-E PA is the gate oxide breakdown [10]. Under ideal class-E operation there is no overlap of high voltage and high current and therefore HCI can be neglected.

The reliability challenge for a class-E RF PA comes from its inherently high drain voltage peaks (theoretically 3.6 V_{dd} [13]). The single transistor class-E PA with the 1.6 V supply voltage exhibits 5.76 V drain voltage (V_d) peaks.

In the proposed design, the finite RF choke (RFC) technique was used. Using the finite RFC technique the maximum V_d voltage peak is reduced to 2.5 V_{dd} [1]. Therefore, if the supply voltage is 1.6 V then the maximum V_d voltage peak (drain of transistor M3 in Fig. 2) is only 4 V (see Fig. 4).

The switching transistor of the basic class-E PA should handle the whole drain voltage peak (4 V). This is much higher than the nominal supply voltage and yet higher than the gate-oxide breakdown voltage. In the cascode topology the drain voltage is divided between both transistors (M2 and M3 in Fig. 2) and therefore the voltage stress on the power transistor is decreased.

The maximum drain voltage peak occurs at high output power which implies a high V_{casc} voltage (Fig. 4). The maximum $V_{dg,M3}$ voltage can be calculated as

$$V_{dg,M3,max} = V_{d,max} - V_{casc} \cong 4\,\text{V} - 1.6\,\text{V} = 2.4\,\text{V} \quad (5)$$

where $V_{d,max}$ is the peak drain voltage. The calculated 2.4 V are still higher than the maximum recommended voltage of the regular gate-oxide transistor. A fully reliable operation can be achieved when the cascode transistor is made of thick gate-oxide device. The reliability for low V_{casc} voltages is automatically satisfied, because with decreasing V_{casc} the drain voltage peak decreases as well (see Fig. 4). By modulating the V_{casc} voltage the reliability does not deteriorate and for $V_{casc} < 1.4$ V the reliability requirement is fully met. If a slight decrease of the maximum

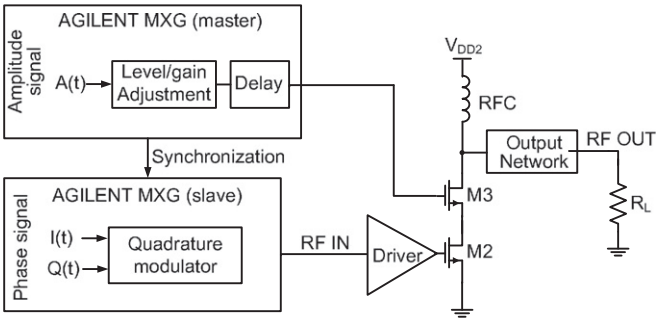

Fig. 5. Block diagram of a polar modulated PA test bench.

output power is acceptable (in the CMOS class-E PA from Fig. 2 it is 1 dBm) than the proposed cascode modulated class-E PA fully fulfills the reliability requirement.

The proposed design combines the cascode topology with the finite RFC technique in order to improve the reliability of the class-E PA.

3. Polar modulation

The class-E PA is well suited for the polar transmitter, where the input of the PA contains only the phase modulated RF signal [8]. Fig. 5 shows the possible implementation of a polar transmitter architecture. The test bench consists of two Agilent MXG signal generators and the CMOS two-stage cascode class-E PA.

The amplitude and phase signals are generated in MATLAB and loaded into the arbitrary baseband generators. The phase signal is simply upconverted into the RF and amplified to the desired power level. The amplitude signal needs to be adjusted to the cascode transistor (M3) input range. The amplitude modulated signal should have a DC bias which equals to the threshold of the M3 and the maximum dynamic range of 1 V. The level adjustments can be performed directly in the Agilent MXG generator.

The polar architecture is very sensitive to any delay that might occur between the envelope and phase path. The phase signal delay is caused by the upconversion in the slave Agilent MXG generator. The two signal generators are precisely synchronized. An additional delay of 24 ns is applied between the phase and envelope paths, to compensate the delay due to the upconversion.

3.1. Predistortion

The predistorter linearizes the PA by generating an inverse non-linear transfer function to the PA, so that the overall transfer function is linear. This can be mathematically written as

$$F_{PD}(v_{in}) \cdot F_{PA}(v_{pd}) = C \tag{6}$$

where F_{PD} and F_{PA} are the predistorter and PA transfer functions, v_{in} is the amplitude input signal which is in the range where the linearization function is valid, v_{pd} is the amplitude signal at the output of the predistorted and C is a constant.

The predistorter output voltage can be expressed as

$$v_{pd} = F_{PD}(v_{in}) \cdot v_{in} \tag{7}$$

In this work, the look-up table (LUT) based predistortion of memoryless PA is implemented. The LUT coefficient calculation using a linear interpolation can be written as

$$y_2 = F_{PA}(x_2) = F_{PA}(x_1 + c_{x1}) = F_{PA}(F_{PD}(x_1)) = g(x_1) \tag{8}$$

where $g(x)$ is the target linear transfer function and c_{xi} is the coefficient stored in LUT for x_i in order to correct the AM–AM

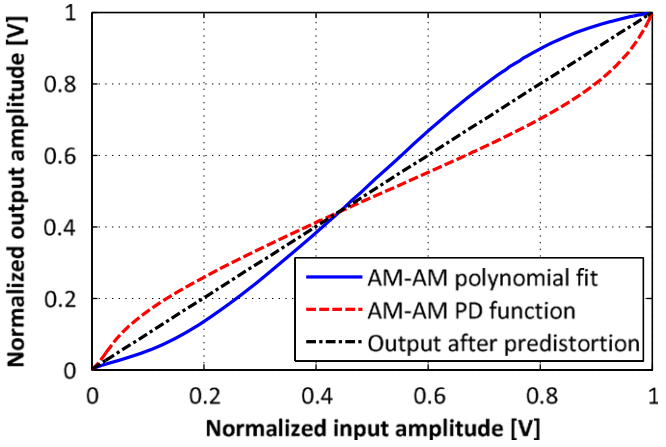

Fig. 6. Simulated AM–AM characteristic after the predistortion, predistorted transfer function and the polynomial fit of the measured AM–AM of the PA.

transfer function. The AM–AM characteristic is the main source of non-linearity on the cascode modulated PA. Fig. 6 shows the measured AM–AM characteristic of the cascode PA, the predistortion function and the simulated transfer characteristic of the PA after the predistortion. The phase predistortion is given by

$$c_{\Phi(x1)} = \Phi_{constant} - \Phi(x_2) \tag{9}$$

where $c_{\Phi(x1)}$ is the phase correction coefficient for x_1 and $\Phi_{constant}$ is a constant target phase.

The AM–AM characteristic and the AM-PM characteristics are measured dynamically using the EDGE input signal as PA stimuli and then characterized in MATLAB. The AM–AM and AM–PM characteristics are modeled by a seventh order polynomial. The order of the polynomial model was chosen as a trade-off between the correlation of the model and measured data (especially at the extremes of the input signal) and keeping the order of the polynomial model as low as possible. The polynomial model is valid within the input parameter range. The LUT coefficients are calculated from 20 ms long data signals, which correspond approximately to four frames long EDGE signal. The predistortion is applied in MATLAB after the modulated input signal is generated.

The predistortion is based on a single behavioral model of the PA and then it is applied to all output power levels. Only a single LUT is used, what makes the digital predistortion easier to implement. The most difficult is to model and predistort the very low input signal amplitudes, especially when the single polynomial function has fit the whole modulation range. Therefore, it can be expected that the predistortion will be not so effective for the low output power region.

4. Measurements

Fig. 2 shows the proposed two-stage PA, where the class-E output stage (M2 & M3) is driven by a class-E driver stage (M1). A microphotograph of the implemented power amplifier is shown in Fig. 7. The area of the PA is $1.2 \times 1.0\,mm^2$. Supply voltages are filtered on the PCB (capacitors C3 and C7 in Fig. 2). The inductor L5 is realized by a bond-wire in order to minimize losses caused by otherwise low quality on-chip spiral inductor. The capacitors are realized as the metal–insulator–metal (MIM) capacitors.

The channel width and length of both transistors M2 and M3 is 1500 and 0.18 μm, respectively. The input matching network consists of spiral on-chip inductor L1 (2.9 nH) and capacitors C1 (0.5 pF) and C2 (10 pF). The width of driver transistor M1 is 500 μm. The output matching network consists of inductor

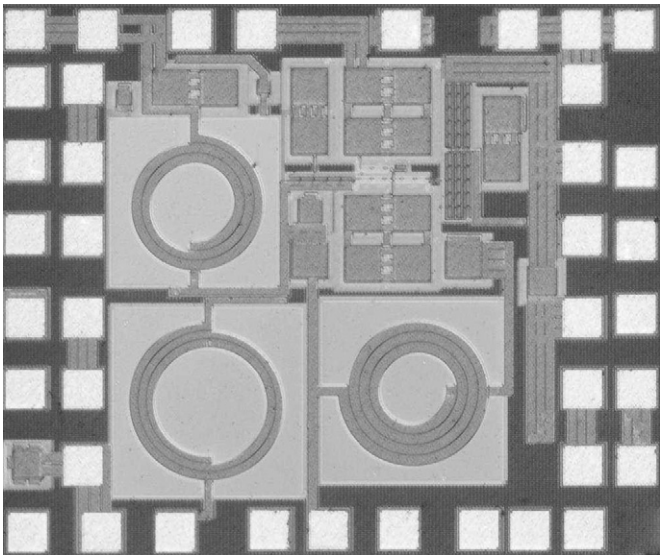

Fig. 7. Microphotograph of the PA.

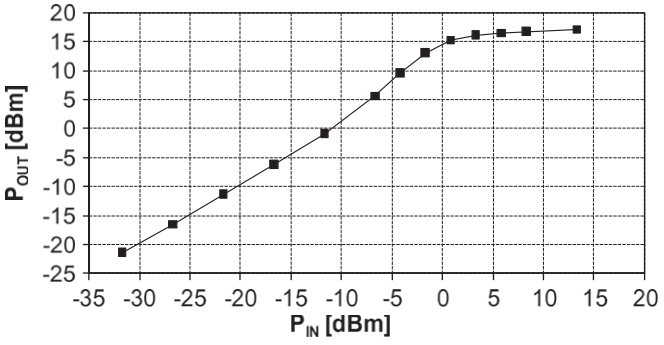

Fig. 8. Measured power (P_{out}) delivered to a 50 Ω load versus available input power (P_{in}) at a frequency of 2.2 GHz.

L5 (2.7 nH), capacitor C8 (3 pF) and capacitor C9 (3.1 pF). The driver and output stage RF choke inductors L2 and L4, respectively, are realized via bondwires. The inductor L3 (3.5 nH) is realized as a spiral on-chip inductor. The capacitors C4 (2 pF), C5 (5 pF) and C6 (4.9 pF) are part of the interstage matching. The bias circuit is realized by a diode connected transistor with a resistor network.

Fig. 8 shows measured P_{out} versus available input power (in Fig. 2 V_{DD1} is 0.6 V, V_{DD2} and V_{casc} are both 1.6 V). A sine wave signal was used as stimulus. The maximum transducer power gain is 14.8 dB. P_{IN} is chosen as 3.5 dBm to ensure that the switching power transistor works as a switch as intended.

Fig. 9 shows average in-band output power (P_{out}). It can be seen that power supply modulation technique provides approximately 20 dB P_{out} dynamic range (from −2 to 18 dBm). The cascode modulation technique exhibits much higher, approx. 35 dB P_{out} dynamic range. This is 15 dB larger dynamic range than in the case of power supply modulation technique.

Fig. 10 shows the AM–PM distortion for a fixed power single tone signal. The phase distortion of the cascode modulation technique is larger than that of the power supply modulation technique.

P_{out} versus frequency for a different V_{casc} voltages is plotted in Fig. 11. The 3 dB bandwidth of the power amplifier is 380 MHz (from 2.00 to 2.38 GHz). As the V_{casc} voltage is decreasing, the resonant frequency of the output network is increasing. This is

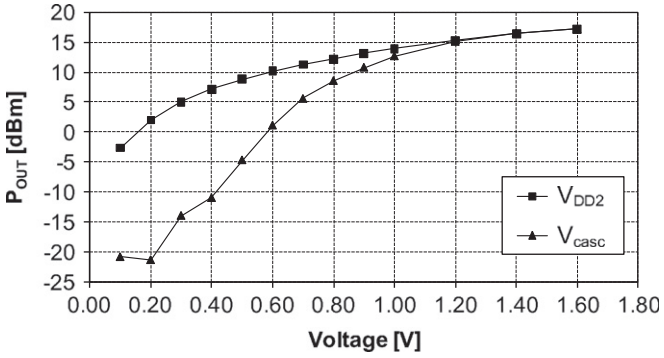

Fig. 9. Measured average output power of the PA (P_{out}) delivered to a 50 Ω load versus V_{DD2} (V_{casc} = 1.6 V) and V_{casc} (V_{DD2} = 1.6 V). The input signal is a single tone at the frequency of 2.2 GHz with 3.5 dBm available input power.

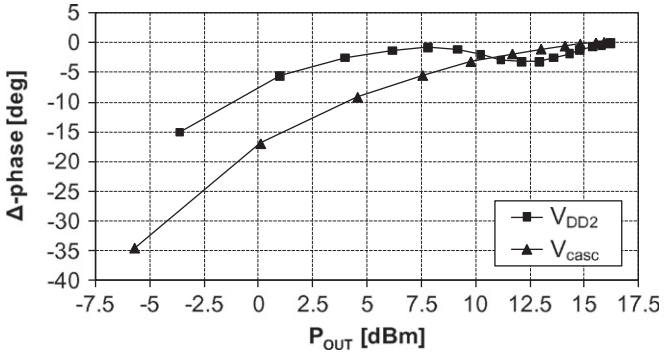

Fig. 10. Measured phase advance change across the PA (Δ−phase) versus V_{DD2} sweep (V_{casc} = 1.6 V) and V_{casc} sweep (V_{DD2} = 1.6 V). The available input power was 3.5 dBm at a frequency of 2.2 GHz.

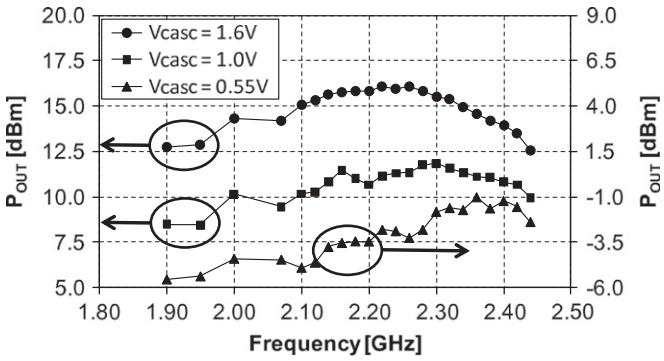

Fig. 11. Measured output power (P_{out}) delivered to a 50 Ω load versus frequency of the input signal at the available input power of 3.5 dBm. The parameter is V_{casc} voltage.

due to strong variation of the cascode transistor (M3) drain capacitance on the V_{casc} voltage.

Although the prototype was not designed to meet any particular standard, it was tested with an 8-PSK modulated signal (EDGE). The measured error vector magnitude (EVM) versus output power is shown in Fig. 12. The EVM without predistortion is below the required 9% imposed by the standard. When the predistortion is employed the EVM is kept below 4% in the whole output power range.

The PAE versus output power is shown in Fig. 13. The peak PAE is 34.6% without predistortion and 30% using predistortion. The decrease is due to that the predistorted PA provides lower peak

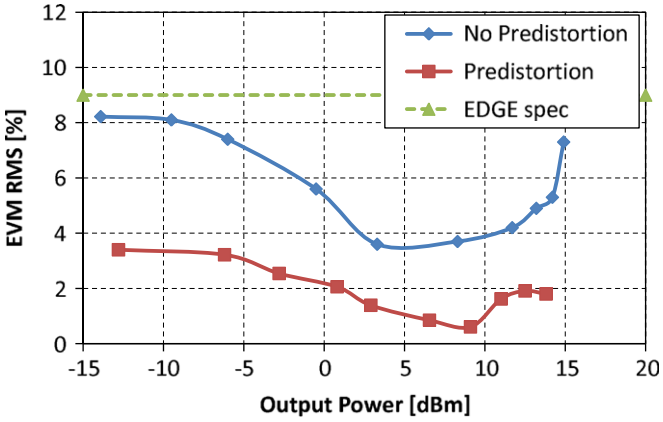

Fig. 12. Measured EVM rms of the PA using the EDGE input signal with and without the digital predistortion versus the average output power delivered to a 50 Ω load.

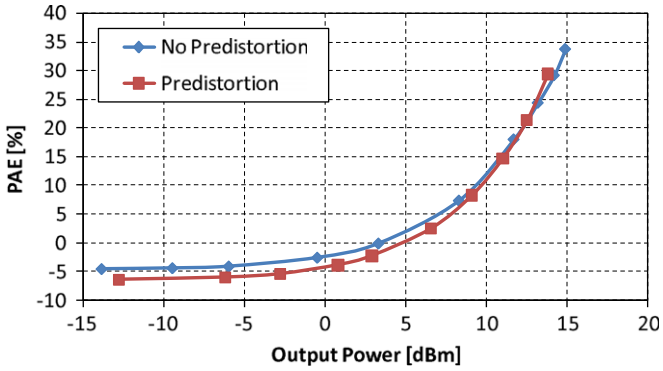

Fig. 13. Measured power added efficiency (PAE) of the PA using the EDGE input signal with and without the predistortion as a function of the average output power delivered to a 50 Ω load.

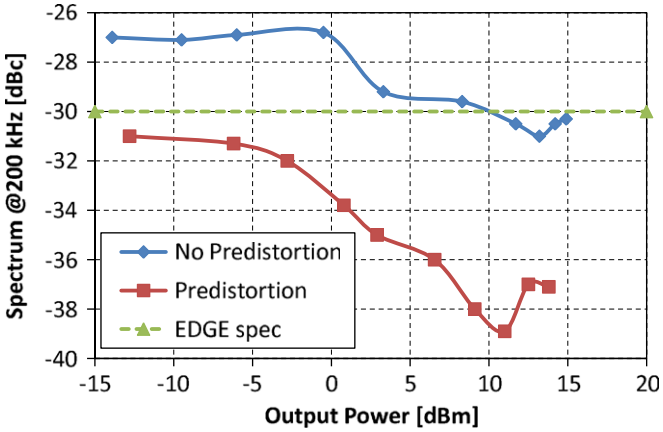

Fig. 14. Measured relative output power spectrum of the PA at 200 kHz frequency offset using the EDGE input signal with and without the predistortion versus the average output power delivered to a 50 Ω load. The resolution bandwidth (RBW) is 30 kHz.

output power than the non-predistorted. The PAE is approximately identical for both predistorted and non-predistorted case. The PAE exhibits negative numbers when the output power drops below the input power.

The next three figures show the spectrum mask measurement versus the output power. In Fig. 14 the spectrum mask at 200 kHz frequency offset is shown. The non-predistorted PA exhibits a very

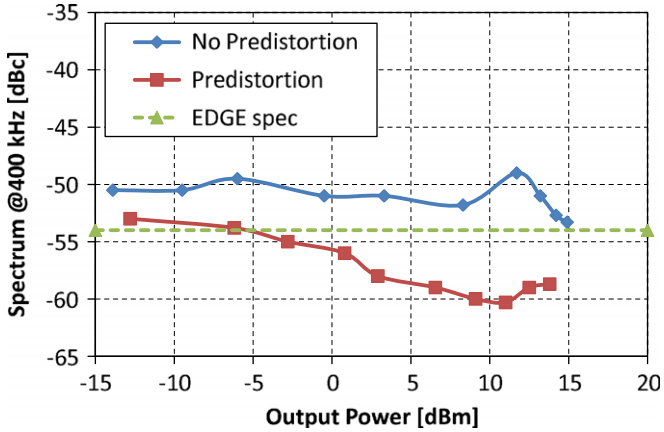

Fig. 15. Measured relative output power spectrum of the PA at 400 kHz frequency offset using the EDGE input signal with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

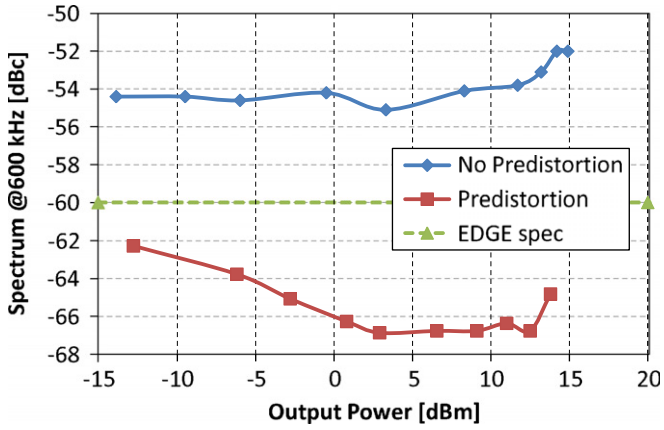

Fig. 16. Measured relative output power spectrum of the PA at 600 kHz frequency offset using the EDGE input signal with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

high out of band non-linearity and therefore the EDGE standard is not met. By applying predistortion the spectrum is confined below the required limit. The measured output spectrum in Fig. 15 shows very similar behavior. It can be observed that the required limit is not met even using the digital predistortion (at the lowest output power level). Low output power levels are difficult to linearize by a single polynomial based AM–AM and AM–PM predistortion. The output spectrum at 600 kHz frequency offset in Fig. 16 violates the standard in the entire output power range. This is corrected by the digital predistortion. The maximum linearity improvement due to the predistortion is approximately 12 dB.

The parameters comparison of the proposed PA with the published CMOS PAs is shown in Table 1.

5. Conclusion

It has been shown that the cascode modulation technique is a suitable technique for the polar modulation of a class-E PA. The proposed cascode modulation provides a high 35 dB output power dynamic range. This is by 15 dB larger than the 20 dB output power dynamic range of the conventional supply voltage power control technique. A single tone and EDGE modulated input signals are used to characterize the PA performance. The digital predistortion is implemented to linearize the AM–AM and AM–PM characteristics. This allows to meet the EVM and output

Table 1
Comparison of the selected CMOS power amplifiers.

	Technology (μm)	Frequency (GHz)	VDD (V)	Peak P_{out} (dBm)	Peak PAE (%)	P_{out} dynamic range (dB)
Ref. [3]	0.18	1.9	3.3	32	40	20
Ref. [4]	0.18	2.4	2.4	23	42	–
Ref. [14]	0.25	1.4	1.5	25	49	17
Ref. [15]	0.35	2.4	1.0	18	33	–
This work	**0.18**	**2.2**	**1.6**	**18**	**35**	**35**

spectrum mask as required by EDGE standard. The measurements have been performed on a 0.18 μm CMOS PA capable of delivering 18 dBm output power to a 50 Ω load at 2.2 GHz.

Acknowledgements

The authors thank Peter Boie Jensen and Ben Kroyer of Aalborg University for technical support, and Per Madsen and Jens Christian Lindof from Texas Instruments for helpful discussions.

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WCDMA/EDGE cascode modulated polar PA

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***Abstract*—Cascode modulation technique suitable for a polar transmitter with the envelope signal applied to the gate of the cascode transistor is presented in this paper. Discussed approach is an alternative to the power supply modulation method. It exhibits approximately twice the output power dynamic range in comparison with the power supply modulation method using the same input signal swing. A conceptual class-E RF power amplifier (PA) operating at 1.75 GHz with 25 dBm peak output power is implemented in a 0.18 μm CMOS process. At the nominal supply voltage 1.8 V reliable operation within the technology device stress limits is guaranteed for the entire output power control range. Obtained measured controllable output dynamic range reaches 39 dB. The PA is tested using single tone, Wideband Code Division Multiple Access (WCDMA) and Enhanced Data rates for GSM Evolution (EDGE) modulation input signals. The linear response of the described cascode modulated class-E PA is achieved by the means of digital predistortion.**

***Index Terms*—Cascode, class-E, CMOS, dynamic range, EDGE, power amplifier, power control, radio frequency amplifiers, WCDMA.**

I. Introduction

THERE is a great demand for high efficiency RF front-ends for modern mobile wireless devices. The power consumption is one of the most important parameters in a mobile device [1]. Furthermore, the RF front-end should support several standards and several frequency bands.

Switch-mode power amplifiers (PAs) are very attractive due to their high efficiency. In [2] a 30 dBm cascode class-E PA with 60% peak power added efficiency (PAE) in 65 nm CMOS technology is demonstrated.

The polar transmitter topology combines high efficiency and linearity [3]. This topology enables the use of a non-linear but highly efficient switch-mode PAs in varying envelope modulation schemes. The conventional envelope modulation is implemented by a power supply voltage modulation [4], [7]. Choi et al. [6] have combined a harmonic-tuned GaAs class-AB/F PA with a CMOS programmable hysteretic-controlled hybrid switching supply modulator. The supply modulator with a programmable hysteretic comparator enables the support of multi-standard applications.

Several studies have been presented where an alternative envelope modulation technique was introduced. In [13] a two-point modulation technique is proposed. The amplitude modulation is implemented by controlling the current of the PA and simultaneously the supply voltage is adjusted in order to improve the efficiency of the PA. Another approach is presented in [14], where a low pass delta-sigma modulator with a phase modulated clock is used to modulate the envelope. A digitally modulated CMOS PA concept [15] employs the amplitude modulation by properly turning on and off a large array of gain cells according to a digital amplitude control signal.

This work was supported by the Danish High Technology Fund.

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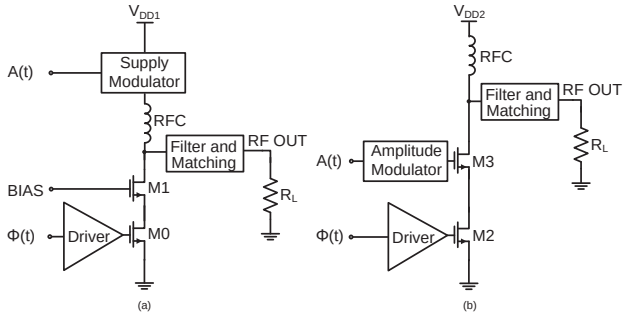

Fig. 1. (a) Conventional power control technique. (b) Proposed power control technique.

An alternative to the traditional power control scheme is presented in this paper. The cascode modulation in contrast to the supply modulation is using the cascode transistor to control the output power. It was shown earlier that the cascode class-E PA topology is suitable for the output power control but the concept was limited to the DC power control only [8]. This paper demonstrates that the cascode modulation technique is suitable to amplify varying envelope signals.

The main advantage of the proposed technique compared to a conventional supply voltage power control technique is a high output power dynamic range and that the amplitude modulator simply controls the gate voltage of the cascode transistor instead of the power supply of the whole PA as in the power supply modulation technique (Fig. 1). The drawback of the cascode modulation is a higher AM-AM distortion compared to the supply modulation. It is demonstrated that the linearity can be significantly improved by digital predistortion (where a single look-up table is used for both WCDMA and EDGE modulated signals).

As the technology scales down, the breakdown voltage is reduced. Therefore, the supply voltage is limited to avoid breakdowns. In order to deliver high output power under low supply voltage, the load impedance has to be low. To mitigate this problem a cascode configuration has been proposed [5]. Another approach is to increase the nominal supply voltage by a using a thick gate-oxide transistor [4] but this limits the RF performance of the power transistor. The cascode topology presented in this paper combines a thick gate-oxide transistor with a regular transistor in order to improve reliability without limiting the RF performance. The power amplifier is implemented in a 0.18 μm CMOS technology and operates at a frequency of 1.75 GHz.

The paper is organized as follows. The principle of the cascode modulation technique and a simplified analytical model

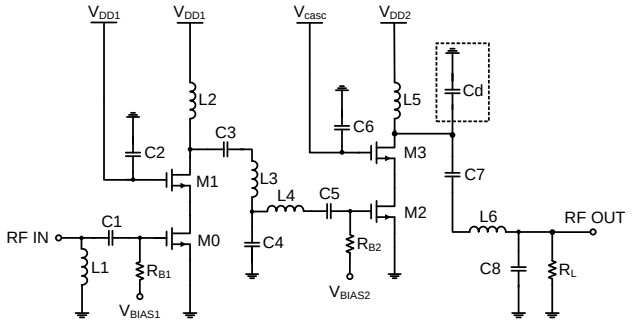

Fig. 2. Schematic of the cascode class-E CMOS PA.

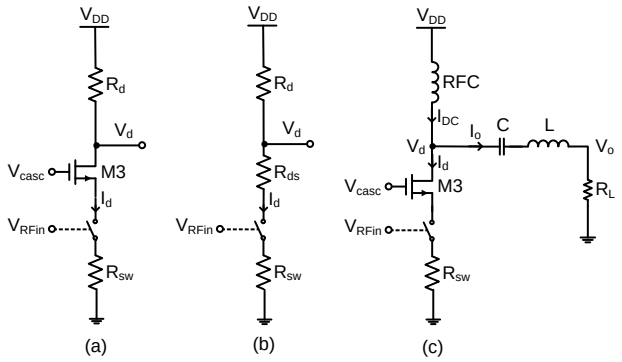

Fig. 3. Equivalent DC cascode circuit (a) in saturation region (b) in triode region and (c) the simplified RF model of the cascode PA.

is described in Section II. The non-linearity characterization and linearization is discussed in Section III. In Section IV experimental results are presented and compared with the published PAs.

II. Cascode Modulation Technique

The proposed cascode modulated PA is shown in Fig. 2. It is a two stage class-E power amplifier. Both stages are using the cascode topology.

The cascode modulation principle is based on application of the amplitude modulated signal to the gate of the cascode transistor M3. The common-source (CS) transistor M2 is designed to operate as a switch. The common-gate (CG) cascode transistor M3 operates in both, saturation and triode region. The phase modulated constant envelope signal is applied to the gate of the CS transistor. The current in the cascode cell is controlled by the V_{casc} voltage.

Other state-of-the-art cascode class-E PA implementations use DC bias voltage applied to the gate of the cascode transistor [1] or employ the self-biased topology [5].

The difference between the proposed cascode modulation concept and the two-point modulation concept introduced by Shameli et al. in [13] is that in their topology the current through the cascode cell is controlled by the CS transistor, whereas in this paper the current control is employed by the CG transistor.

A. Cascode Modulation

The basic operation of the cascode modulated class-E PA is similar to a single balanced mixer. The amplitude varying signal is multiplied by the RF phase modulated signal. The current through the cascode cell is controlled by the V_{casc} voltage.

During the OFF state, the drain voltage of the CS transistor is limited by the cascode transistor. Its drain-source voltage equals to $V_{casc} - V_{GS,M3}$. The maximum voltage stress is on the CG transistor (see Section II-C). During the ON state, the CS transistor operates in the linear region.

The supply voltage modulation technique is depicted in Fig. 1(a). The supply modulator modulates the PA supply voltage according to the amplitude signal $A(t)$. Several modulator topologies can be used to implement the supply modulator [3]. The main advantage of supply modulation is a linear AM-AM characteristic. The drawback is the limited output power dynamic range and a stringent requirement on the power converter (high BW and low noise).

The proposed cascode modulation technique offers a high dynamic range [8]. The direct capacitive coupling (Miller effect) between the RF input (gate of M2) and the RF output (drain M3) is reduced. Therefore a lower output power level can be reached compared to the single transistor PA. This results in the high dynamic range [8]. In cascode modulation the amplitude modulator simply controls the V_{casc} voltage of CG transistor instead of the power supply of the whole PA. The main drawback is a non-linear AM-AM characteristic.

The size of the CG transistor is chosen so that the required drain capacitance C_d is fully implemented by the parasitic capacitance of the CG device. The size of the CS transistor is given by the trade-off between the ON-resistance and the input capacitance. To maximize the efficiency of the PA, the ON-resistance of the CS transistor has to be low. The width of the switch transistor is limited by the gate capacitance and parasitic drain capacitance. The switch transistor with large width imposes high driving current requirements on the PA driver. The switching transistor M2 is realized as thin gate-oxide transistor. The cascode transistor uses a thick gate-oxide option. The thin gate-oxide transistor has a better RF performance and lower input capacitance in comparison to thick gate-oxide transistor. This improves the efficiency and also alleviates the requirements on the driving stage.

B. Simplified Cascode Model

A simplified analysis and model of the cascode PA is proposed in this subsection. The main goal is to obtain a simplified analytical expression for the drain current I_d as a function of V_{casc}. This current can be used to calculate the output power as a function of V_{casc}.

It is assumed that the cascode current is zero during the OFF state (independent of the V_{casc} voltage). Therefore only the current during the ON state is investigated. It is also assumed that the switch transistor operates as an ideal switch with the ON-resistance R_{sw} (Fig. 3). R_d is the equivalent load resistance for DC simulations.

The cascode transistor M3 operates in two states. M3 is in saturation for low V_{casc} voltage. The cascode transistor enters

and remains in the linear region when

$$V_d \leq V_{casc} - V_T \tag{1}$$

where V_T is the threshold voltage. The equivalent circuits for the saturation and linear regions are shown in Fig. 3(a) and 3(b) respectively. The following equations are based on a simplified model of the MOSFET transistor.

1) Saturation region: The drain current of the cascode device in saturation is given by

$$I_d = \frac{1}{2}\mu_0 C_{OX} W/L_{eff}(V_{GS} - V_T)^2 \tag{2}$$

where μ_0 and C_{OX} are the mobility of the carriers and the gate oxide capacity respectively. W is the channel width and L_{eff} is the effective channel length. Note that only the channel length modulation is considered. The gate-source voltage V_{gs} of the M3 transistor can be written as

$$V_{GS} = V_{casc} - I_d R_{sw} \tag{3}$$

The effective mobility can be expressed as [20]

$$\mu_{eff} = \frac{\mu_0}{1 + (E_{eff}/E_0)^{\nu}} \tag{4}$$

where the E_0 and ν are constants. The average electrical field E_{eff} experienced by the carriers in the inversion layer is approximated as [20]

$$E_{eff} \cong \frac{V_{GS} + V_T}{6T_{OX}} \tag{5}$$

For simplicity $V_{GS} = V_{casc}$ is assumed in (6). The effective channel length is given by [20]

$$L_{eff} = L_{drawn} - 2\left(L_{INT} + \frac{L_l}{L^{L_{ln}}} + \frac{L_W}{W^{L_{wn}}} + \frac{L_{Wl}}{L^{L_{ln}} \cdot W^{L_{wn}}}\right) \tag{6}$$

where L_{drawn} is the drawn transistor channel length and all the other parameters are technological constants.

By substituting of (3) – (6) into (2) and solving for I_d the following result is obtained

$$I_d = \frac{L_{eff} + C_{OX} R_{sw} V'_{eff} W \mu_{eff}}{C_{OX} R_{sw}^2 W \mu_{eff}} - \frac{\sqrt{L_{eff}(L_{eff} + 2C_{OX} R_{sw} V'_{eff} W \mu_{eff})}}{C_{OX} R_{sw}^2 W \mu_{eff}} \tag{7}$$

where

$$V'_{eff} = V_{casc} - V_T \tag{8}$$

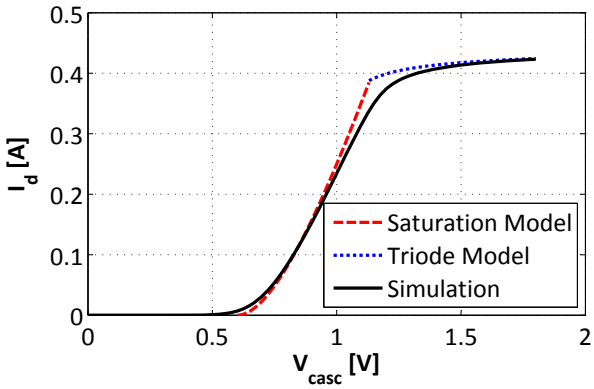

Fig. 4. The comparison of simulated and calculated drain current as a function of the cascode control voltage V_{casc}.

2) Linear region: In the linear region the cascode transistor can be substituted by the equivalent drain-source resistor R_{ds} (Fig. 3(b)). The drain current is given by the Sah equation as

$$I_d = \mu_0 C_{OX} \frac{W}{L_{eff}} \left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{9}$$

The drain-source voltage can be found using

$$V_{DS} = V_{DD} - I_d R_d - I_d R_{sw} \tag{10}$$

By substituting of (10) into (9) and solving for I_d gives (11). The coefficient α and β are defined as

$$\begin{aligned} \alpha &= R_d^2 - R_{sw}^2 \\ \beta &= \mu_{eff} C_{OX} \frac{W}{L_{eff}} \end{aligned} \tag{12}$$

Utilizing equations (7) and (11) the drain current can be calculated as a function of V_{casc}. Fig. 4 shows the comparison of the calculated model and the simulation result. The correlation between the model and the simulation is limited in the region where the transistor translates from the saturation to the linear region. This is due to the simplified assumptions used in the model. The technology constants were obtained from the BSIM 3v3 transistor model provided by the IC foundry, the switch ON-resistance R_{sw} and the equivalent drain resistance R_d are 0.35 Ω and 3.75 Ω respectively.

The roll-of of the transfer characteristic in Fig. 4 at high drain current is caused by the cascode device entering the linear region where $V_{DS.M3} < V_{DS.M3,sat}$. The significance of this effect depends on the current level through the cascode device, on the device physical dimension (W/L) and on the magnitude of the modulation voltage V_{casc}. The supply voltage level has a direct impact on the headroom of the cascode device and therefore significantly influences the shape of the transfer characteristic. For some applications it might be beneficial to limit the V_{casc} voltage so that the cascode transistor doesn't enter the deeper triode region.

$$I_d = \frac{\sqrt{\alpha(2V'_{eff} - V_{DD})V_{DD}\beta^2 + (1 + V'_{eff}(R_d + R_{sw})\beta - R_d V_{DD}\beta)^2} + R_d V_{DD}\beta - V'_{eff}\beta(R_{sw} + R_d) - 1}{\alpha\beta} \tag{11}$$

3) Output power: The equivalent circuit for output power calculation is shown in Fig. 3(c). It is assumed that the PA operates as an ideal class-E PA. The current through the cascode transistor M3 can be written as

$$I_d = I_{DC} - I_o \sin(\theta + \phi) \tag{13}$$

where I_{DC} is the input DC current, I_o is the output current amplitude, $\theta = \omega t$ and ϕ is the phase relative to switching cycle. For ideal class-E operation $\phi = -32.49°$ [19]. The output current amplitude can be obtained as [19]

$$I_o = \frac{I_{DC}}{\sin(\phi)} = I_o \sin(\phi) - I_d \tag{14}$$

where [19]

$$\sin(\phi) = -\frac{2}{\sqrt{\pi^2 + 4}} \tag{15}$$

Using equation (14) the amplitude of the output current can be expressed as

$$I_o = -\frac{I_d}{1 - \sin(\phi)} = -\frac{I_d}{1 + \frac{2}{\sqrt{\pi^2+4}}} \tag{16}$$

Therefore, using (16) the output power can be expressed as

$$P_{OUT} = \frac{1}{2} I_o^2 R_L = \frac{1}{2} (\frac{-I_d}{1 + \frac{2}{\sqrt{\pi^2+4}}})^2 R_L \cong 0.211 {I_d}^2 R_L \tag{17}$$

One can notice that the output voltage V_o changes linearly with respect to I_d according to

$$V_o = I_o R_L = -(\frac{1}{1 + \frac{2}{\sqrt{\pi^2+4}}}) I_d R_L \tag{18}$$

C. Reliability

The reliability of the CMOS PA is mainly limited by the hot-carrier instability (HCI) and the gate oxide breakdown [10]. If the voltage across the gate oxide exceeds a certain limit (for given technology) the oxide rapture occurs. Oxide rapture causes a catastrophic and permanent damage [11]. The performance degradation at DC is caused by the channel hot-carrier effect when both, the gate voltage and drain voltage, are simultaneously high [16].

HCI is a reliability issue, which leads to threshold voltage and drain current shifts over time [12]. The dominant degradation at RF is due to Fowler-Nordheim or direct tunneling [16]. The main reliability issue for a properly designed class-E PA is the gate oxide breakdown [10]. This can be explained by that in the ideal class-E operation there is no simultaneous overlap of high voltage and high current and therefore HCI can be neglected. Usually, the recommended voltage is 10 % above a maximum allowed supply voltage to guarantee a product lifetime of ten years (given by the technology design rules). As the technology scales down the breakdown voltage is reduced as well.

In the technology used for experimental work the nominal supply voltage is 1.8 V and the gate-oxide breakdown voltage is 3.5 V. The 0.34 μm thick gate-oxide transistors allow a higher supply voltage of 3.3 V and the device gate-oxide breakdown voltage is increased to 6 V.

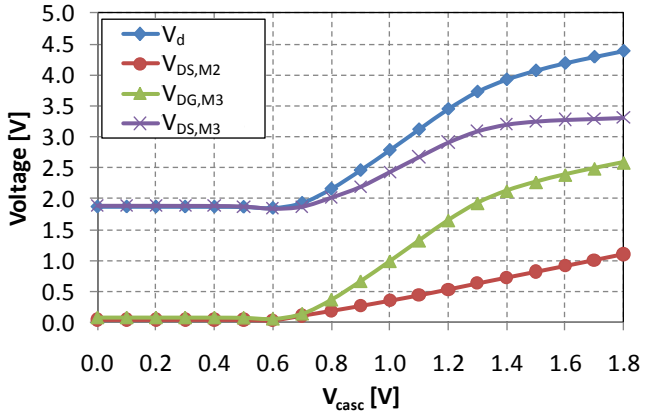

Fig. 5. Simulated peak voltages of CS and CG transistors in the RF cycle as a function of the cascode control voltage V_{casc}.

The reliability challenge for a class-E RF PA comes from its inherently high drain voltage peaks (theoretically $3.6\,V_{DD}$ [9]). The single transistor class-E PA with 1.8 V supply voltage exhibits 6.5 V drain voltage peaks. Using the finite RFC technique the maximum drain voltage peak is reduced to $2.5\,V_{DD}$ [1]. Therefore, if the supply voltage is 1.8 V then the maximum drain voltage peak (drain of transistor M3 in Fig. 2) is 4.5 V. This is still higher than the above mentioned recommended voltage of the regular or the thick gate-oxide transistor.

In the cascode topology the drain voltage is divided between both transistors (M2 and M3 in Fig. 2). The drain voltage of the switch transistor M2 is directly controlled by the V_{casc} voltage and it has to be kept below the recommended voltage. The supply voltage is limited by the gate-oxide breakdown of the transistor M3. Assuming that $V_{casc} = 1.8\,\text{V}$ and $V_{DD} = 1.8\,V$ then drain-gate voltage of M3 is given by

$$V_{DG,M3} = V_d - V_{casc} \cong 2.5 \cdot 1.8\,V - 1.8\,V = 2.7\,V \tag{19}$$

This is still higher that the recommended voltage of the regular gate-oxide transistor. Therefore the cascode transistor is made of the thick gate-oxide device. The reliability for low V_{casc} voltages is automatically satisfied, because with decreasing V_{casc} the drain voltage peak decreases as well (see Fig. 5). In order to improve the reliability of class-E PAs the proposed design combines the cascode topology together with the finite RFC technique.

III. Linearization

The predistorter linearizes the PA by generating an inverse nonlinear transfer function to the PA so that the overall transfer function is linear. This can be mathematically written as

$$F_{PD}(v_{in}) \cdot F_{PA}(v_{pd}) = C \tag{20}$$

where F_{PD} and F_{PA} are the predistorter and PA transfer functions, v_{in} is the amplitude input signal which is in the range where the linearization function is valid, v_{pd} is the amplitude signal at the output of the predistorter and C is a constant.

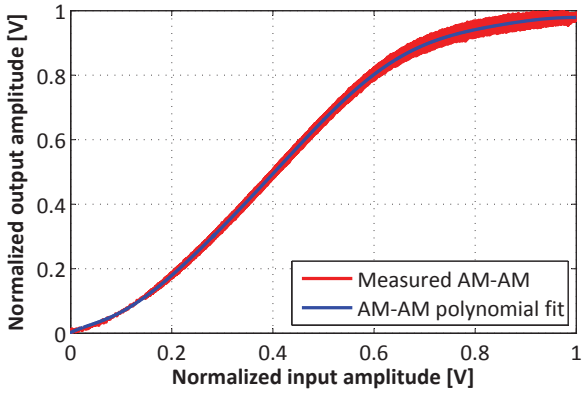

Fig. 6. Measured AM-AM characteristic and its polynomial fit.

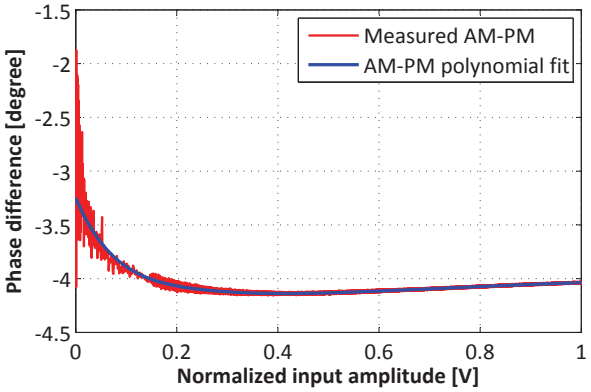

Fig. 7. Measured AM-PM characteristic and its polynomial fit.

The predistorter output voltage can be expressed as

$$v_{pd} = F_{PD}(v_{in}) \cdot v_{in} \tag{21}$$

In this work, the look-up table (LUT) based memoryless predistortion of the PA is implemented. The LUT coefficient calculation using a linear interpolation can be written as

$$\begin{aligned} y_2 &= F_{PA}(x_2) = F_{PA}(x_1 + c_{x1}) \\ &= F_{PA}(F_{PD}(x_1)) = g(x_1) \end{aligned} \tag{22}$$

where $g(x)$ is the target linear transfer function and c_{xi} is the coefficient stored in LUT for x_i in order to correct the AM-AM transfer function. The phase predistortion is given by

$$c_{\Phi(x1)} = \Phi_{constant} - \Phi(x_2) \tag{23}$$

where $c_{\Phi(x1)}$ is the phase correction coefficient for x_1 and $\Phi_{constant}$ is a constant target phase.

The AM-AM characteristic (Fig. 6) and the AM-PM characteristic (Fig. 7) are measured dynamically using the EDGE and WCDMA input signals as PA stimuli. Since the linearization model is memoryless, the LUT coefficients are calculated directly in MATLAB. The AM-AM characteristic is modeled by a 9-th order polynomial and the AM-PM characteristic by the polynomial of 8-th order. The order of the polynomial model was chosen as a trade-off between the correlation of the model and measured data (especially at the extremes of the input signal) and still keeping the order of the polynomial model as low as possible. The polynomial model is valid within the input parameter range. The LUT coefficients are calculated from 20 ms long data signals, which corresponds approximately to 4 frames long EDGE signal or to 2 frames long WCDMA signal. The predistortion is applied in MATLAB after the modulated input signal is generated.

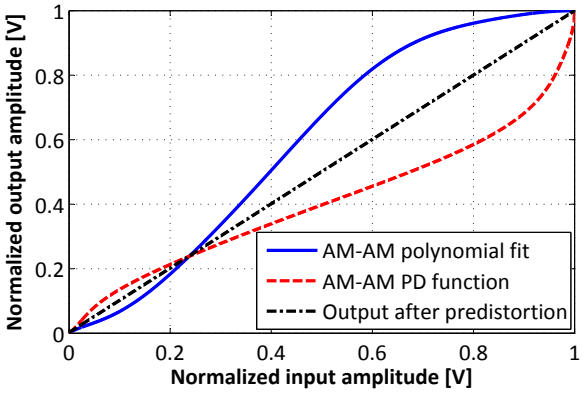

Fig. 8. Simulated AM-AM characteristic after the predistortion, predistorted transfer function and the polynomial fit of the measured AM-AM of the PA.

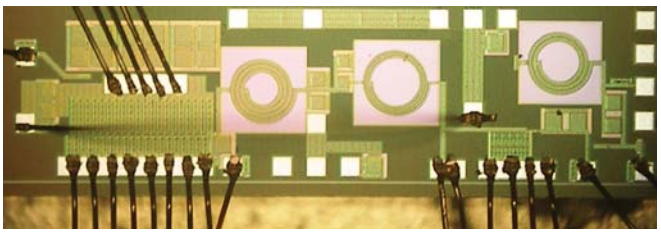

Fig. 9. Microphotograph of the chip.

The predistortion is based on a single behavioral model of the PA which is used for all power levels. Therefore only a single LUT is used, which makes the digital predistortion easier to implement.

The main difference between the EDGE and WCDMA signals is that WCDMA has higher BW, dynamic range and power control range. WCDMA signal using quadrature phase-shift keying (QPSK) modulation has approximately the same 3.4 dB PAR as the EDGE signal. It is very challenging to model the AM-AM response of the WCDMA modulated PA by a single polynomial curve. From the shape of the curves in Fig. 6 and Fig. 7 is obvious that it is problematic to model the very low input signal amplitudes. The modeled AM-AM and AM-PM characteristics of EDGE and WCDMA are practically identical, which means that the implemented cascode PA has no significant memory effects in the frequency band from 200 kHz to 3.84 MHz.

Fig. 8 shows the measured AM-AM characteristic of the cascode PA, the predistortion function and the simulated transfer characteristic of the PA after the predistortion.

IV. Experimental Results

It this section the measured results of the cascode modulated class-E PA are presented. The PA was tested using WCDMA

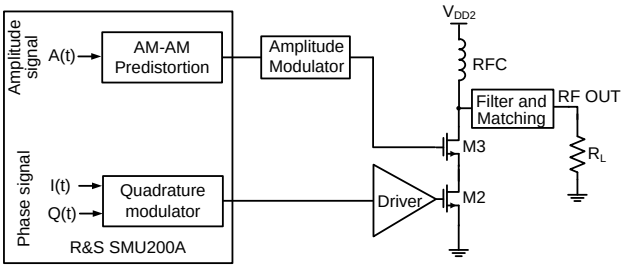

Fig. 10. Block diagram of a polar modulated PA

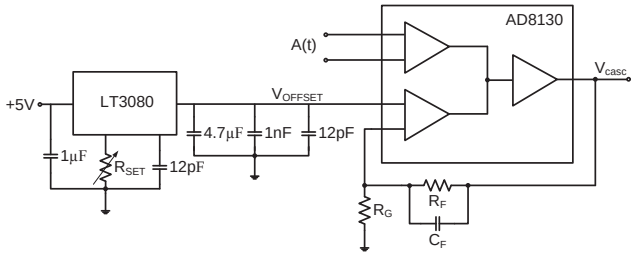

Fig. 11. Amplitude modulator schematic

and EDGE modulated signals. The circuit was fabricated in 0.18 μm CMOS technology. The process offers two gate-oxide thickness options (4.2 nm for 1.8 V and 7 nm for 3.3 V operation). The channel length of all transistors is 0.18 μm except of the two cascode transistors (M1 and M3) with 0.34 μm. The process has 5 metal layers plus thick top layer. The microphotograph of the realized power amplifier is shown in Fig. 9. The chip dimensions are 1.5 x 3 mm.

The width of transistors M2 and M3 is 5000 μm and 8000 μm respectively. The input matching network consists of spiral on-chip inductor L1 (2.1 nH) and capacitor C1 (8 pF). The output matching network consists of inductor L6 (2.7 nH) and capacitor C8 (4 pF). The inductor L6 is a part of the series resonant output tank (with C7) and also a part of the matching network (with C8). L6 is realized by an on-chip bondwire. The driver and output stage RF choke inductors L2 and L5 respectively are realized via bondwires. The interstage inductors L3 (5 nH) and L4 (3.1 nH) are realized as spiral on-chip inductors. Capacitors C3 (2 pF), C4 (2 pF) and C5 (4.9 pF) are also part of the interstage matching. The interstage matching topology is more complex because the driver and output stage were tested separately and have to be impedance matched. The capacitors C2 (10 pF) and C6 (60 pF) should provide RF ground at the gates of cascode transistors.

The envelope adjustment circuit is implemented off-chip. The main function of this circuit is to provide a voltage shift and amplification. This is implemented by the differential receiver amplifier AD8130 by Analog Devices (Fig. 11). It has a 200 MHz bandwidth and it can be connected as a voltage level shifter. The gain can be set by the feedback resistors. The signal applied to the cascode transistor M3 contains both amplitude modulated signal and power control signal (Fig. 10).

The nominal operation conditions are as follows: available input power 3.5 dBm, frequency 1.75 GHz, output stage power supply 1.8 V, driver stage power supply and cascode voltage

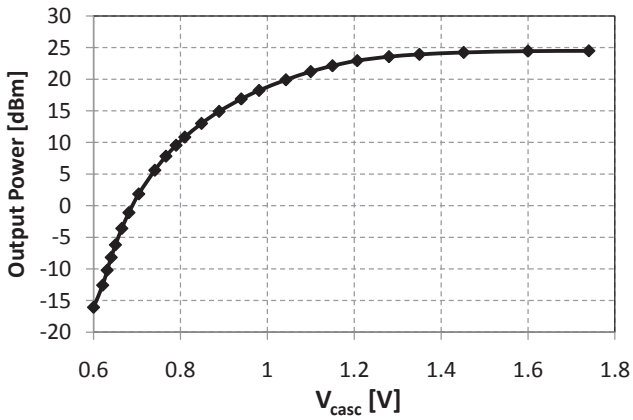

Fig. 12. Measured average RF output power delivered to a 50 Ω load versus DC cascode voltage V_{casc}. The RF input is a single-tone with available input power of 3.5 dBm at a frequency of 1.75GHz.

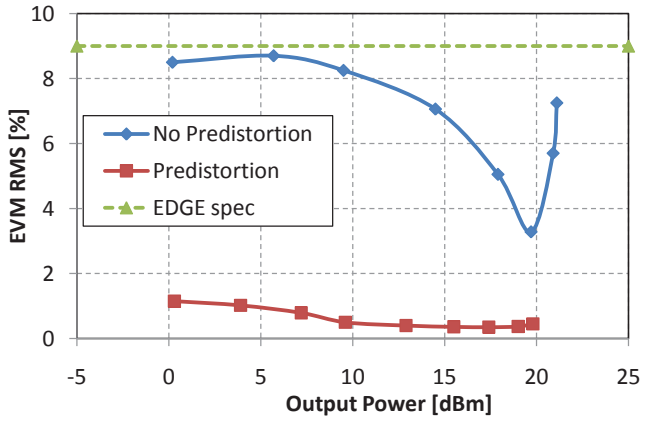

Fig. 13. Measured EVM rms (EDGE) with and without the digital predistortion versus the average output power delivered to a 50 Ω load.

1 V, bias voltage (for each stage) 0.675 V. The maximum cascode voltage in output stage equals to the supply voltage (1.8 V). The PA is designed to have 25 dBm peak output power.

The measured output power versus V_{casc} voltage is shown in Fig. 12. The DC V_{casc} voltage (which is close to the effective voltage of the amplitude modulated signal using EDGE or WCDMA modulation) is swept from 0.6 V to 1.8 V. The output power control range is 42 dB. The output power DR of the amplitude modulated cascode PA is limited by the linearity requirements of the particular wireless standard. The lowest output power levels are significantly distorted (that can be observed for example in Fig. 21) because the peak-to-peak output power dynamic range using a varying amplitude signal is limited when the cascode transistor operates in the ”knee” region. Furthermore, using only single LUT based PA predistortion the linearization of this region of the AM-AM characteristic is difficult (Section III).

The target of this work is not to meet every aspect of a particular wireless standard. The measured results using varying envelope signals (EDGE and WCDMA) demonstrate the feasibility of the cascode modulation concept.

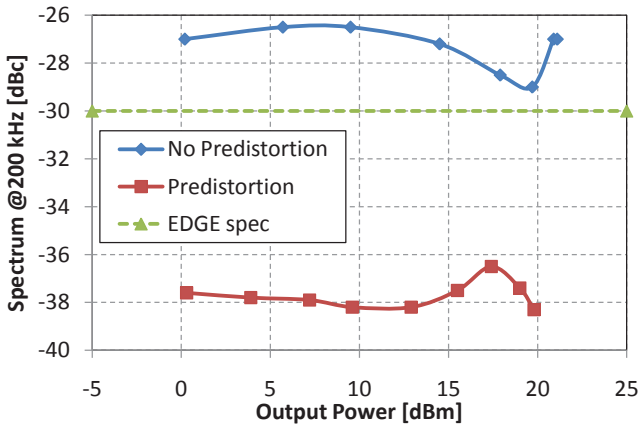

Fig. 14. Measured relative output power spectrum (EDGE) at 200 kHz frequency offset with and without the predistortion versus the average output power delivered to a 50 Ω load. The resolution bandwidth (RBW) is 30 kHz.

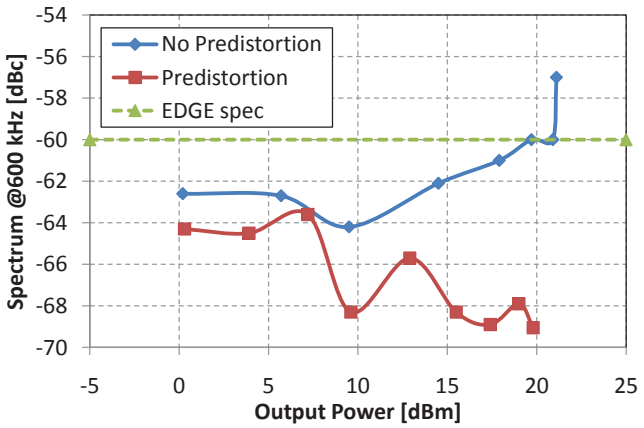

Fig. 16. Measured relative output power spectrum (EDGE) at 600 kHz frequency offset with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

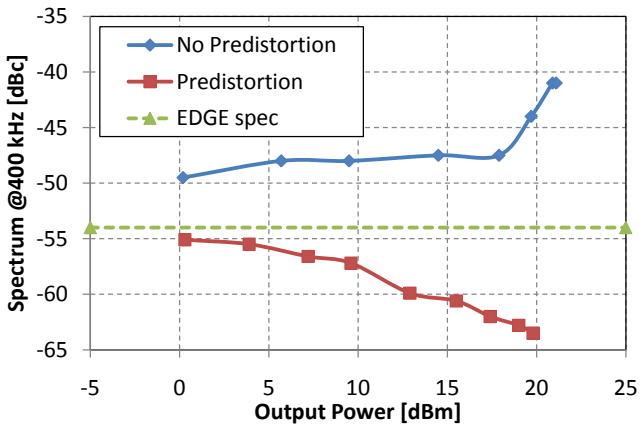

Fig. 15. Measured relative output power spectrum (EDGE) at 400 kHz frequency offset with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

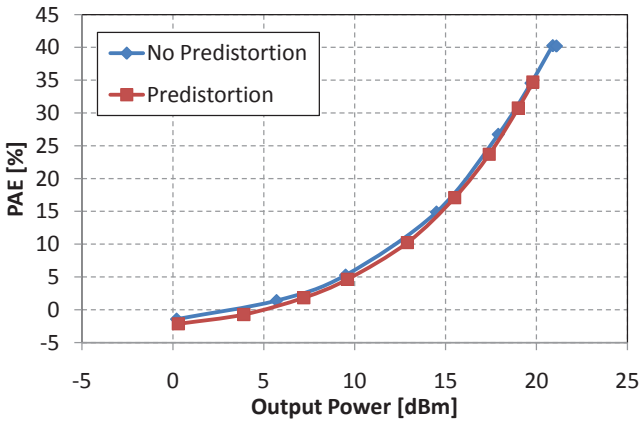

Fig. 17. Measured power added efficiency (EDGE) with and without the predistortion as a function of the average output power delivered to a 50 Ω load.

A. EDGE

The measured results show the performance comparison using no digital predistortion or using the static predistortion based on the dynamic AM-AM characteristic, which was described in Section III. The measured error vector magnitude (EVM) versus output power is shown in Fig. 13. Even though, the EVM without predistortion is below the required 9 % imposed by the standard, it is much higher than that of state-of-the-art PAs. When the predistortion is employed the EVM is kept below 1.2 %.

The next three figures show the spectrum mask measurement versus output power. In Fig. 14 the spectrum mask at 200 kHz frequency offset is shown. The non-predistorted PA exhibits a very high out of band non-linearity and therefore the EDGE standard is not met. By applying predistortion the spectrum is well confined below the required limit. The measured output spectrum in Fig. 15 shows very similar behavior. It can be observed that the required limit is met very tightly even using the digital predistortion (with almost no headroom at lowest output power). The low output power can be difficult to linearize by a single polynomial based AM-AM and AM-PM predistortion. The output spectrum at 600 kHz frequency offset in Fig. 16 violates the standard only for the highest output power. This is corrected by the digital predistortion.

The PAE versus output power is shown in Fig. 17. The peak PAE is 40 % without pre-distortion and 35 % using predistortion. The decrease is due to that the predistorted PA provides lower peak output power than the non-predistorted. The PAE in the 0 dBm to 20 dBm range is approximately identical for both pre-distorted and not predistorted case. The PAE exhibits negative numbers when the output power drops below the input power.

The effect of delay between amplitude and phase paths is shown in Fig. 18 and Fig. 19. The EVM is not as sensitive to the time delay as is the output spectrum [4]. The EDGE standard is met even the time delay of 1 μs is introduced between the amplitude and phase paths. The spectrum mask requirement is much more stringent and allows only 50 ns delay. The limit on the maximum allowable delay between the phase and amplitude in the cascode modulated PA is set by the spectrum mask at 400 kHz and 600 kHz frequency offset.

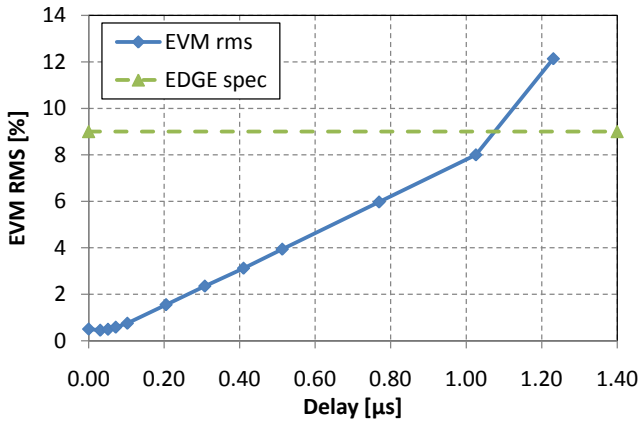

Fig. 18. Measured EVM RMS (Root Mean Square) as a function of the delay between the amplitude and phase path (EDGE).

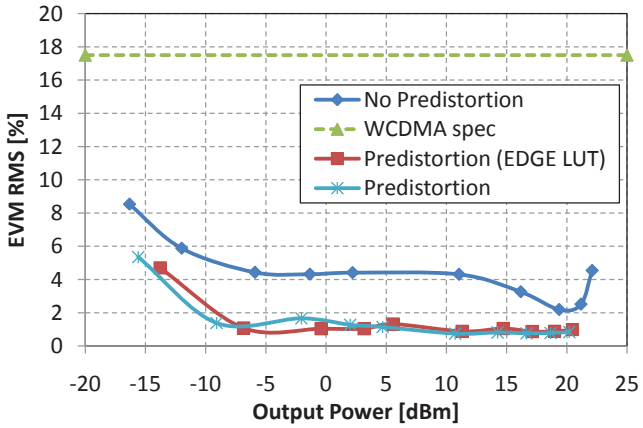

Fig. 20. Measured EVM RMS (Root Mean Square) with and without the digital predistortion versus the average output power delivered to a 50 Ω load (WCDMA).

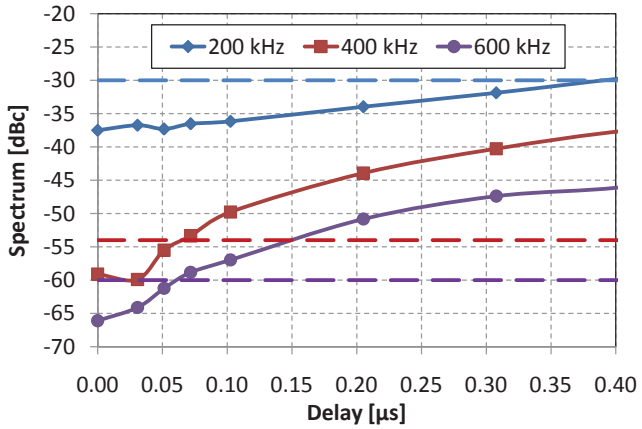

Fig. 19. Measured relative output power spectrum (EDGE) at 200/400/600 kHz frequency offset versus the delay between the amplitude and phase path. The dashed lines are the corresponding specs. The RBW is 30 kHz

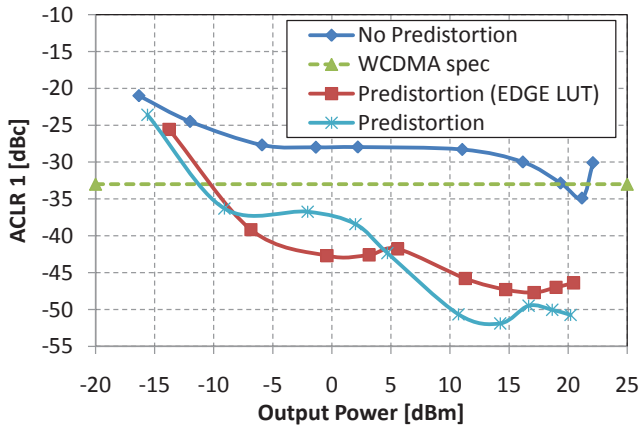

Fig. 21. Measured adjacent channel leakage power ratio (WCDMA) with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

B. WCDMA

The measured EVM versus output power of WCDMA modulated cascode PA is shown in Fig. 20. The figure shows the results without predistortion, with predistortion using EDGE LUT and with predistortion LUT based on the WCDMA signal. The main differences between the EDGE and WCDMA look-up tables are that the EDGE LUT is based on the input signal with narrower modulation bandwidth and higher minimum output power than the WCDMA one. Both modulations have the same 3.4 dB PAR. Generally, a better performance using WCDMA LUT can be expected (for output power below 0 dBm the EDGE LUT coefficients are constant). Both predistortion coefficients are calculated using the same polynomial order. As it can be seen from Fig. 20 there is a difference between the two predistortion but the improvement using WCDMA LUT is small. This is due to the limiting capabilities of the linearization of very small amplitudes. The maximum output power dynamic range of the cascode modulation is 39 dB (based on the "No predistortion" curve in Fig. 20).

The adjacent (ACLR1) and alternate (ACLR2) channel leakage ratios are shown in Figs. 21 and Fig. 22. ACLR1 and ACLR2 are the main linearity indicators. The worse of the two numbers, upper or lower ACLR1 and ACLR2, is used in Fig. 22. Both ACLR1 and ACLR2 don't meet the 3rd Generation Partnership Project (3GPP) standard without using the predistortion. Even by using the predistortion, the linearity requirement is violated for output powers below -5 dBm. Therefore, in this application the usable output power dynamic range is reduced to 29 dB. At very low output power the predistorted curves are approaching the non-predistorted curve, which means that the predistortion is not effective in this region. As mentioned in Section III the poor predistortion performance at lowest output power levels is caused by that only a single LUT predistortion is used to model the entire AM-AM characteristic of the proposed PA. Both predistortion look-up tables leads to the same linearity improvement and therefore for simplicity in the next figures only the EDGE LUT is considered.

After applying the predistortion the output power spectrum becomes asymmetrical (see Fig. 23). This is caused by the non-ideal phase cancellation of the 3rd order intermodulation products during the predistortion. The alternate channel leakage ration exhibit similar behavior but the asymmetry is lower.

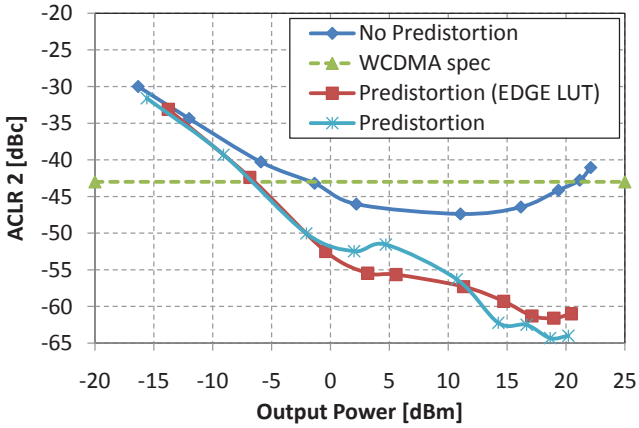

Fig. 22. Measured alternate channel leakage power ratio (WCDMA) with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

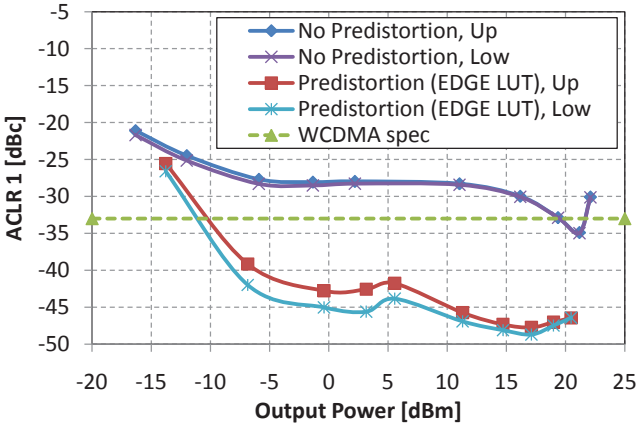

Fig. 23. Measured adjacent channel leakage power ratio asymmetry (WCDMA) between upper and lower band with and without the predistortion versus the average output power delivered to a 50 Ω load. The RBW is 30 kHz.

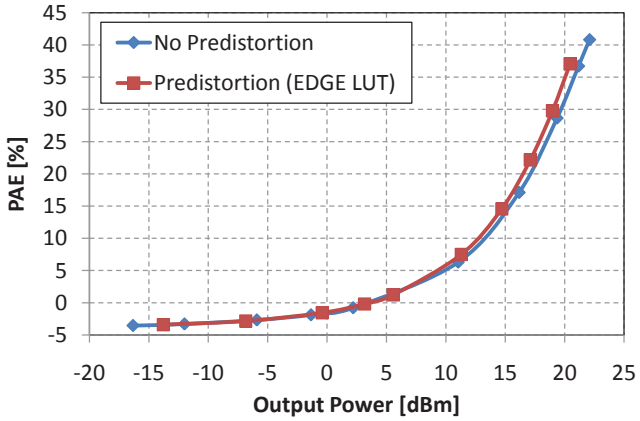

Fig. 24. Measured power added efficiency (WCDMA) with and without the predistortion as a function of the average output power delivered to a 50 Ω load.

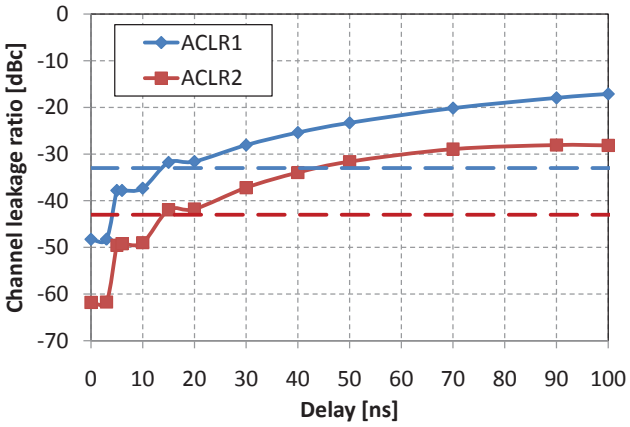

Fig. 25. Measured alternate (ACLR1) and adjacent (ACLR2) channel leakage power ratio (WCDMA) versus the delay between the amplitude and phase path. The dashed lines are the corresponding specs. The RBW is 30 kHz.

Fig. 24 shows the PAE versus output power. The PAE is slightly higher than that using the EDGE modulated input signal (see Fig. 17). The PAE exhibits negative numbers for the output powers below approximately 3.5 dBm. This is because the input power of the PA is not adjusted by the power level (available input power is constant for all measurements at 3.5 dBm).

The EVM and channel leakage ratio versus time delay between amplitude and phase signals are shown in Fig. 26 and Fig. 25. Similar to EDGE, the EVM is not the limiting factor. EVM allows a 135 ns delay but the channel leakage ratio (ACLR1 and ACLR2) limits the delay to 15 ns. Both ACLR1 and ACLR2 are equally sensitive to the amplitude and phase delay mismatch.

The performance comparison of the proposed PA and a published WCDMA or EDGE PAs is shown in Table. I.

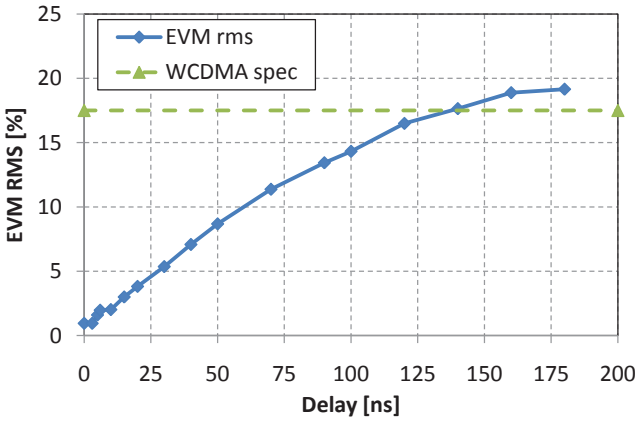

Fig. 26. Measured EVM RMS (Root Mean Square) as a function of the delay between the amplitude and phase path (WCDMA).

V. Conclusion

In this paper the cascode modulation concept suitable to amplify varying envelope signals has been presented. The cascode modulation technique is proposed as an alternative to the power supply modulation technique. The concept was verified by measurements. The cascode modulation technique appears attractive because it has a high output power dynamic range and the amplitude modulator simply controls the gate voltage of cascode transistor instead of the power supply of the whole PA as in the power supply modulation technique.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE SELECTED STATE-OF-THE-ART EDGE/WCDMA POWER AMPLIFIERS.

	Modulation	Frequency [GHz]	Max P_{out} [dBm]	Gain [dB]	VDD [V]	Peak PAE [%]	Linearization	TX power control [dB][1]	Controllable circuit topology[2]	Technology
Ref. [6]	WCDMA/EDGE	1.88	29 / 27.8	27.8 / 29.4	3.3	46 / 45	NO	$\sim$ 25 dB [3]	NO	GaAs + CMOS
Ref. [13]	WCDMA/EDGE	0.9	27.8	N.S.	3.3	34	YES	>33 dB	Yes (Digitally controlled current sources)	$0.18\,\mu m$ CMOS
Ref. [15]	WCDMA/EDGE	1.9	21.7	14.5	2.1	38	YES	>70 dB	YES (Digitally modulated PA)	$0.13\,\mu m$ SOI CMOS
Ref. [17]	EDGE	0.9 & 1.8	10	N.S.	1.4	38	YES	44	YES (Controllable switch array)	90 nm CMOS
Ref. [4]	EDGE	1.75	23.8	30	3.3	22	YES	12	NO	$0.18\,\mu m$ CMOS
Ref. [18]	WCDMA	1.95	27	25	2.9	46	NO	10	NO	$0.25\,\mu m$ BiCMOS
This work	**WCDMA/EDGE**	**1.75**	**21.6 / 21.1**	**21.5**	**1.8**	**37 / 35**	**YES**	**39**	**NO**	$0.18\,\mu m$ **CMOS**

[1] Average output power controllability excluding AM dynamic range. If the PA works with both WCDMA and EDGE signal, only the WCDMA control range is considered.
[2] The output power control is achieved by adaptive or digitally controlled circuits in the PA.
[3] Estimated value.

The designed two stage CMOS class-E PA operates at 1.75 GHz. The experimental results show the PA has an output power of 21.6 dBm and 37 % PAE using the WCDMA input signal. Using the EDGE input signal the PA delivers an output power of 21.1 dBm and has a PAE of 35 % PAE. The output power control using cascode modulation technique is high (approx. 39 dB) but still not high enough to meet the requirement given in 3GPP standard (-71 dBm for WCDMA class 4 transmitter). Therefore this technique has to be combined with another one in order to achieve the output power control range required by 3GPP. The PA was linearized using digital predistortion with a single LUT in order to meet the linearity requirements of GSM/EDGE and 3GPP standards.

ACKNOWLEDGMENT

The authors thank Peter Boie Jensen from Aalborg University and Peter Krogsgaard Jensen from Rohde & Schwarz Denmark for technical support, and Ole Kiel Jensen from Aalborg University for technical discussions.

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