Flexible and Printed Electronics

Active matrix-based pressure sensor system with a 4 × 16 printed decoder designed with a flexible hybrid organic process design kit

To cite this article: Palak Gupta *et al* 2024 *Flex. Print. Electron.* **9** 015006

Flexible and Printed Electronics

PAPER

Active matrix-based pressure sensor system with a 4 × 16 printed decoder designed with a flexible hybrid organic process design kit

Palak Gupta[1,*], **Justas Lukosiunas**[2], **Gabriel Cadilha Marques**[1], **Sebastian Raths**[3], **Sebastian Stehlin**[4], **Stefan Schlisske**[4], **Kai Exner**[3], **Karl-Phillip Strunk**[4], **Christian Melzer**[4], **Peter Erk**[5], **Josef Mittermaier**[2], **Anton Klotz**[2] **and Jasmin Aghassi-Hagmann**[1,*]

[1] Institute of Nanotechnology (INT), Karlsruhe Institute of Technology (KIT), Eggenstein-Leopoldshafen 76344, Germany
[2] Cadence Design Systems GmbH, Mozartstrasse 2, 85622 Feldkirchen, Munich, Germany
[3] BASF SE, Carl-Bosch-Strasse 38, 67056 Ludwigshafen, Germany
[4] InnovationLab, Speyerer Strasse 4, 69115 Heidelberg, Germany
[5] erConTec GmbH, Roter-Turm-Weg 3, 67157 Wachenheim an der Weinstrasse, Germany
[*] Authors to whom any correspondence should be addressed.

E-mail: palak.gupta@kit.edu and jasmin.aghassi@kit.edu

Keywords: large area electronics, organic process design kits, printed OFETs, active-matrix pressure sensing

Supplementary material for this article is available online

OPEN ACCESS

RECEIVED
20 September 2023

REVISED
13 December 2023

ACCEPTED FOR PUBLICATION
22 January 2024

PUBLISHED
9 February 2024

Abstract

The innovative field of printed sensor with a demand for high accuracy, sensitivity and durability has enabled a wide application area in sensing, healthcare etc. A large-area printed sensor system on a flexible foil substrate emplying p-type organic field-effect transistors (OFETs) is presented. Thereby, the OFET is fabricated through a hybrid manufacturing process, including photolithographically structured source- and drain-electrodes, ink-jet printed organic semiconductor, and spin-coated dielectric. Moreover, a dedicated device model, derived from the variable range hopping model, is developed and integrated together with process related design rules, materials properties and geometric information into a comprehensive process design kit (FH_OPDK). The FH_OPDK is integrated in a commercial electronic design automation tool and is used to design and perform post-layout simulations on logic gates, such as INV, NAND2, and NOR2 as well as circuitry such as ring oscillators and a 4 × 16 digital decoder. Several circuit topologies have been tested and evaluated in a detailed model-hardware correlation analysis. Finally we have optimized logic gates and the decoder in a PMOS only, pseudo CMOS design style. To demonstrate the feasibility of the full sensor system in hardware a 16 × 16 active matrix pressure sensor on a flexible substrate integrated with a 4 × 16 binary decoder was fabricated and tested. We have integrated our flexible hybrid sensor system with a PCB board and a microcontroller to demonstrate the hardware readout platform capable of detecting the weight of objects and visualizing a digital map of applied forces.

1. Introduction

Printed organic electronics has been an active research field for decades now [1–3], but still poses many challenges concerning materials, fabrication and circuit design to scientists worldwide [4, 5]. At the same time many attractive opportunities in flexible sensing [6], medical wearables or diagnostics [7] and IoT-applications [8] arise but are not yet realized due to multiple scientific challenges on material, device and circuit level. Besides the constant quest for better, high-performance materials and reliable printing technologies also circuit primitives, accurate models and hardware verified macrocells/circuit blocks are highly needed for real world applications and hybrid systems. In addition, a reliable material stack with precise process control and modest variations during all fabrication steps (lithography and solution processable techniques) is a pre-requisite for further efforts such as the development of so-called process design kits (PDKs). These software kits can map all technology relevant information and verified designs of circuit primitives together with a physical layout into an electronic design system.

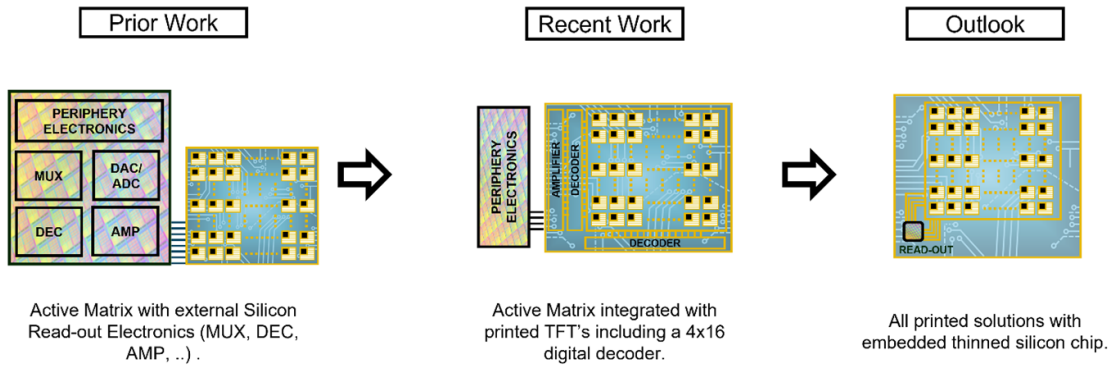

Figure 1. The transition of hybrid electronics from a separated printed active-matrix sensor and delocalized bulky Si-electronics to printed thin film electronics including a printed 4 × 16 binary decoder on flexible substrates. In future, all logic components could be integrated with printed TFTs and a flexible thinned silicon chip in foil.

A wide range of application possibilities such as large area sensing [9], artificial skin [10], on-body wearables [11] are engineered due to material developments in the field of organic material engineering such as structural flexibility, ability to be printed on various substrate (plastic, paper etc), low cost and large coverage area. Large area sensing platforms based on organic field effect transistor (OFET) sensors have shown high sensitivity and competitive performance [12, 13], demonstrating the potential to be used in medical [14, 15], AI application [16], photovoltaics [17], etc. An underlying limitation observed during comprehensive literature review is the constrain on the density of the transistor for logic and computing circuit [18]. Even though printed sensors have carved a niche in the field of large area sensing as can be seen in [19, 20] the periphery circuit still needs to be developed to realise a system on chip printed on a flexible substrate and reduce the strain on interfacing output lines (figure 1). Huge performance variations, due to the printing process also makes it difficult to predict the circuit performance. This issue can be resolved by modelling the behaviour and variation of the transistor in an appropriate device model and further integrated in an electronic design automation (EDA) tool to create a design flow for designing complex printed electronic circuits.

Significant progress has been made in developing PDKs for printed electronics [21–26]. As an example, the organic PDK (OPDK) [21] is a design flows based on ion gel gated organic transistor. Until now, the available PDK, for printed electronics, have successfully integrated various device models to allow for circuit designs based on transistor, resistors and capacitors. Table 1 provides an overview of the PDK specific to organic hybrid printed transistors. Apart from designing the circuit at schematic level and verifying the design concept using simulation, the design kit is equipped with display resources and layer stack information to create the circuit layout. As the design tool have been adopted from silicon-based electronics, circuit designers in printed electronics still need to do a lot of manual tasks such as dielectric placement, routing, among others. Another challenge that circuits designers face is the estimation of parasitic effects due to various fabrication techniques. This issue can be mitigated by integrating the material and parasitic information for each layer in the PDK. Also, within printed electronics, circuits based on only a monotype transistor is well known [27–29]. To implement logic gates, various topologies are available to compensate for the complementary behaviour. The design layout and synthesis tools used for silicon electronics needs to be adapted for design topologies created using single monotype transistor. To further support the designer in complex circuit design, a reusable standard cell library based on the most optimal topology for the technology can further save time and efforts. The standard cell library is not available in case of printed electronics based PDK till yet [21–25, 27]. Even though progress has been made with the available PDKs, improvements such as accurate mathematical model containing capacitance and variation information, parasitic information, standard cell blocks etc. can be made to add enhanced functionalities, which are better suited for printed electronics. Until now, the PDKs are integrated into silicon-technology-supported EDA tools as the basic functionalities are similar to the ones of state-of-the-art silicon technology. But features such as complementary mask generation, automatic routing, need to be adapted according to the requirements in printed electronics.

In this regard, a PDK is created based on a OFET technology discussed in a following subsection. Based on a solution compatible process, a p-type OFET is fabricated and characterized. The fabricated OFET is modelled to be used in simulations and circuit design flows based on the OFET. Furthermore, the model is integrated together with layout information, design rules, and film properties into a PDK, which is named as FH-OPDK, here. The FH-OPDK is then

Table 1. Comparison between presented FH-OPDK and other organic PDK available in the market.

	FH_OPDK	OPDK, University of Minnesota [21]	Process design kit for flexible hybrid electronic [27]	Fully-additive printed electronics [24]	OPDK, Nguyen *et al* [25]
Pcell for transistor, resistor, capacitor	✓	✓	✓	✓	✓
Schematic editing support	✓	✓	✓	✓	✓
Automatic grid-snapping tailored to the substrate	✓	✗	✗	✗	✗
Automatic generation and deletion of di-electric and mirrored metal	✓	✗	✗	✗	✗
Implementation of various circuit topologies	✓	✓	✗	✗	✓
Reusable standard cells based on multiple circuit topologies for complex circuit design	✓	✗	✗	✗	✗
Parasitic extraction information	✓	✓	✓	✓	✓
Model hardware correlation with focus on variation	✓	✗	✗	✗	✗
Post-layout simulation	✓	✓	✓	✓	✓
High complexity IP acheived	16 × 16 pressure sensor matrix, with two 4–16 binary decoder and a 16 × 1 multiplexer	8 × 8 DRAM array [22]	D flip-flop, shift register, amplifier [27]	4-bit DAC [24]	6-bit organic fully differential SAR ADC [25]

integrated in Cadence as a part of the front-to-end design flow. The front-to-end design flow is customized specially for the hybrid printed technology. The assistive layout features such as automatic grid snapping, connectivity-driven layout feature, and automatic layer generation toolbar helps circuit designers to design complex circuits and is largely missing in state-of-the-art PDKs developed for printed electronic [21–25].

To justify applicability of the FH-OPDK, a sensor system is designed with the help of the FH-OPDK. Apart from the sensor matrix, electronic circuits, such as decoders and multiplexers are printed on the same substrate to support first-level computation. Thereby, the wiring complexity between silicon electronic components and printed electronic components is reduced by a factor of 4. Further progress in this direction can enable a fully printed system, where the sensors and the read-out electronics are printed on the same substrate. The research presented in the paper is a step forward toward developing an integrated system on a flexible substrate using organic hybrid printed technology.

2. Materials and experimental methods

The FH-OPDK is primarily based on an organic field effect transistor. The organic thin film p-type channel transistor is realized as a top gate bottom contact architecture. The materials used for the organic semiconductor (XPRD01B06) and dielectric (XDRD41L01) are proprietary materials of BASF. The fabrication process combines different low temperature techniques such as PVD, Photolithography and ink-jet printing to form the OFET on the employed PEN-substrates. For the FH-OPDK a mix of printing

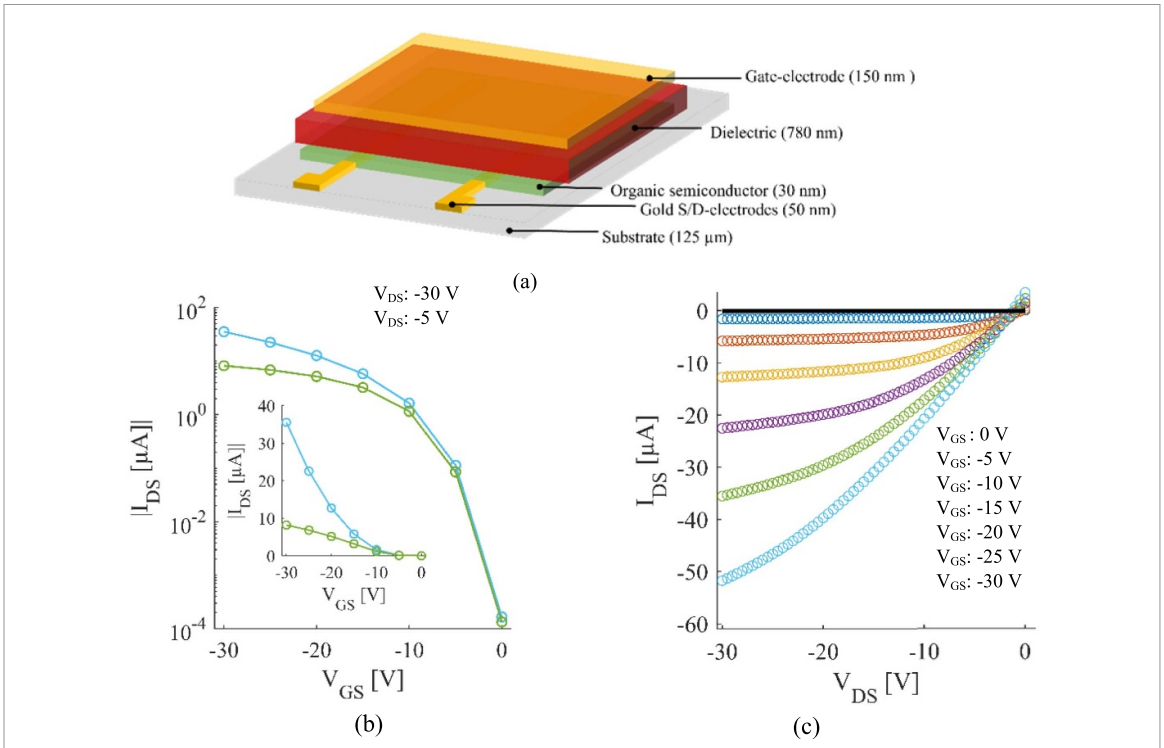

Figure 2. (a) Layer diagram of the top gate bottom contact organic p-channel transistor, (b) transfer characteristic and (c) output characteristics of OFET.

and non-printing techniques was chosen to establish a solid baseline of the envisioned technology. In parallel, technology variants were developed where select processing steps were exchanged for others bearing the potential for roll-to-roll processing (e.g. gravure printing and inkjet instead of photolithography for the electrodes).

First, source and drain gold contacts (∼50 nm) are evaporated and lithographically structured on the flexible Substrate. Then, the semiconductor material (∼30 nm) and standard dielectric material (∼780 nm) are deposited from solution through inkjet printing and spin coating, respectively. Finally, the top gate layer is deposited using PVD and Photolithography. The fabricated OFETs shows high yield and stable electric performance at mobility values up to 0.3 cm^2 Vs^{-1} as well as threshold voltages (Vth) ∼2 V ± V.

2.1. Transistor characterisation

The OFET devices exhibit stable electrical characteristics, as can be observed from figures 2(b) and (c). The V_{GS}–I_{GS} characteristics (transfer curves) show that the p-type transistor is operating in enhancement mode as the device is completely switched off at $V_{GS} = 0$ V. The voltage operating range is between −30 V and 5 V. The field-effect mobility is measured to be 0.359 cm^2 Vs^{-1} and the threshold voltage is between −3 V and 1 V. These key parameters are the mean value over 705 OFETs.

3. Modelling

In order to design applications based on the introduced OFET technology, it is crucial to have a reliable transistor model that can mimic the electrical characteristics of the OFETs. Moreover, it is important that the model is compatible with state-of-the-art EDA tools. For that reason, the presented model is implemented in Verilog-A and integrated into the FH-OPDK that contains all the technology relevant information. However, the transistor model itself consists of a DC and a capacitance model. The capacitance model describes the parasitic capacitances at the drain- and source-terminals and allows for transient simulations.

First, the DC drain-source current (I_{ds}) of the presented OFET is modelled through a derivative of the variable-range-hopping model presented in [28]:

$$I_{DS} = -\frac{\beta}{2}\left(F(V_{th} - V_{Gs})^{2+\gamma} - F(V_{th} - V_{GD})^{2+\gamma}\right) - I_{off}.$$

Where β is the transconductance parameter, γ is the power law parameter, I_{off} is the off-current, V_{th} is the threshold voltage, V_{GS} is the gate-source voltage, and V_{GD} is the gate-drain voltage. Furthermore, the function F is defined as:

$$F(x, S) = \frac{\log\left(e^{\frac{x}{S}} + 1\right)}{\frac{1}{S}},$$

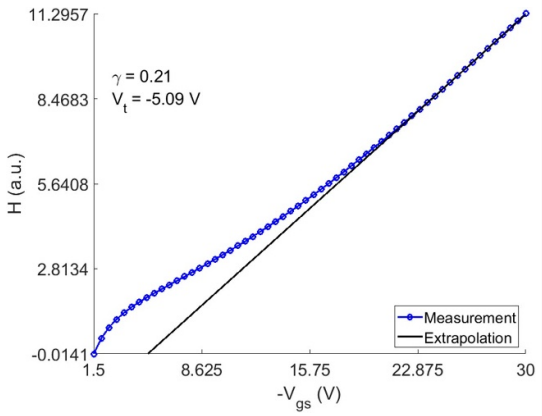

Figure 3. H-integral function of the transfer curve at a maximum drain-source voltage (−30 V) to extract the power law parameter and the threshold voltage.

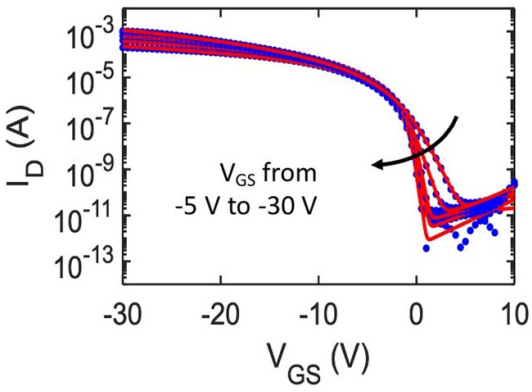

Figure 4. Comparison between measurement and simulation of a OFET with a W/L ratio of 1000 μm/100 μm at various drain-source voltage values. The doted blue curve is the measurement while the red solid line is the simulation.

where x is the variable representing V_{GS} or V_{GD}. Following the approach in [27], most of the parameters are extracted through the H-integral function (figure 3):

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(V)\,dV}{I_{DS}(V_{GS})}.$$

By extrapolating the linear part of the H-integral function and approximation of the linear part, the slope m of the approximation is defined as:

$$m = \frac{1}{2+\gamma}.$$

Thereby, the power-law parameter is extracted, through the slope(m) of the linear part. In addition, the intercept with the x-axis yields the threshold voltage. Further details on the parameter extraction routine with the help of the H-integral function can be found in literature [29]. After extracting these empirical parameters, it is recommended to optimize the extracted parameters through an optimization algorithm, such as the Levenberg–Marquardt algorithm [30].

The presented model is semi empirical, since physical parameters such as the channel width (W), channel length(L), gate-capacitance (C_g), and the field-effect mobility (μ_{eff}) are included to estimate the transconductance parameter (β):

$$\beta = \frac{W}{L} C_g \mu_{eff}.$$

In figure 4 the measured and simulated curves for a OFET with a W/L-ratio of 1000 μm/100 μm are shown. A great agreement between the measured and simulated curves are observable.

Second, with the help of a Mayer-capacitance-like model, the overlap capacitances of the OFETs are described as follows:

$$C_{GS} = \frac{2}{3}\cdot C_{GG}\cdot\left[1-\left(\frac{V_{GT}-V_{DSe}}{2V_{GT}-V_{DSe}}\right)^2\right]$$
$$C_{GD} = \frac{2}{3}\cdot C_{GG}\cdot\left[1-\left(\frac{V_{GT}}{2V_{GT}-V_{DSe}}\right)^2\right].$$

The details of the model can be found in [31]. By combining the presented DC model with the capacitance model, it is possible to simulate the DC and transient behaviour of circuits.

3.1. Implementation in industrial EDA tool

The presented FH-OPDK is a design library, containing the discussed OFET technology, mirroring the fabrication process. The library includes the architecture of the OFET, the design rules, as well as the device model. Each layer is specified by its dimension and boundary conditions so that transistor layer architecture is replicated by a digital twin. The FH-OPDK integrated in an EDA tool makes it possible to establish front-to-back design flow in printed electronics. The FH-OPDK supports circuit designers in creating circuits and optimizing them based on the presented OFET technology.

The design flow is tailored specifically to meet the challenges of printed electronics. In addition to basic EDA features, assistive layout design, grid-snapping, global optimisation, auto-layer generation, etc. are possible within the presented design flow. With a hierarchical schematic editor, the circuit topology is designed without considering the layout. The circuit designer has the freedom to evaluate various design topologies. With each view from schematic to layout, provide multiple interactive features, making it a state-of-art design flow for printed technology.

The adherence to the defined dimension within a particular layer and the inter-layer spacing is verified with the design rule check flow. The metal layer design for source and drain fingers as well as for routing are laid out to avoid additional parasitic effects. The p-cell for the resistor allows to select different shapes, namely meander and block patterns. For each pattern the effective resistance is calculated. Material properties like the sheet resistance (resistor-200 Ω/[], metal- 4 Ω/[]), dielectric constant (4.3) are included as constant parameters.

4. Circuit design and standard cell libraries

To demonstrated the efficacy of FH-OPDK, various circuits are designed ranging from Inv, Nand, Nor to decoder and multiplexer. As mentioned before, one of the limitations within the presented transistor technology, is that only p-type transistors are available to design circuits. For that reason different topologies are evaluated to compensate for the lacking n-type OFET [32–34], which are referred as 2-transistor and 4-transistor topology.

The circuits are characterized and the measured data is used to perform a model-hardware correlation as well as to assess the power performance of the present technology

Each inverter has 5 independent contact pads for the power supply (V_{DD}), connected to the source of the pull-up OFET, the input (V_{IN}), connected to the gate of the pull-up OFET, supply voltage (V_{SUP}) for the totem-pole stage, connected to the gate of the pull-down OFET, ground (V_{SS}) connected to the drain of the pull-down OFET, and output (V_{OUT}), connection between source and drain of the two OFETs, as shown in figures 5(a) and (d). The pulse input signal is applied using a Voltcraft 8202 function generator to the V_{IN} node. The supply voltage and biasing voltage (V_{SUP}) are provided by a Keithley 2602 source-meter to the V_{DD} and V_{SUP} node, respectively. A passive probe with a 10 MΩ input resistance and 10.5 pF input capacitance is used as the output load. The transient measurement is performed, the input pulse and oscillating output are recorded over time on a Yokogawa DL6104 digital oscilloscope [35].

The inverter input pulse has two logic levels i.e. logic '0' is equal to the level of the source supply, and logic '1' which is equal to the level of the supply voltage. An important parameter of logic gates is the propagation delay time which determines the speed of a circuit and describes how long it takes for an input signal to cause a change at the output signal. The propagation delay is calculated by averaging the rise and fall times, the time differences between the input and its corresponding output period crosses the 50% level [36]:

$$t_{delay} = \frac{t_{rise\_delay} + t_{fall\_delay}}{2}.$$

4.1. 2-Transistor topology

First, inverter structures designed with 2-Transistor topology using two p-type OFETs connected in series are evaluated. Thereby, the pull-up OFET is bigger in size and is turned on, once the input is at the logic '0' level. Moreover, the pull-down transistor is biased with a voltage (V_{SUP}) at the source supply as depicted in figure 5(a). The V_{SUP} voltage is regime. When the input is logic '0', the pull-up OFET goes into saturation and the output is pulled up to logic '1'. On the other hand, when the input is logic '1' the pull-up OFET is in the cutoff region enabling the pull-down network and switching the output signal to logic '0'. The performance of the inverter is optimized through the presented PDK. The inverter has a good switching characteristic as shown in figure 5(b) with a measured propagation delay per stage of 0.03 ms.

4.2. 4-Transistor topology

The 4-Transistor topology is more commonly known as the pseudo-CMOS topology [32]. The pseudo-CMOS topology is based on four OFET's arranged as shown in figure 5(d).

The OFETs T1 and T2 are known as the totem pole stage. T1 is connected to the input and T2 is connected in a diode load configuration through a negative VSUP voltage. For that reason, the OFET T2 always operates in the saturation region. The output of this stage is the input of T4. When the input is logic '0', T1 is in conductive state and the input to T4 is in logic '1', which switches T4 to the cut-off region. T3 is in saturation and the output is pulled-up to logic '1'. On the other hand, when the input is logic '1', T1 is in cut-off and the input of T4 is pulled-down, turning T4 into the cut-off region. In addition, T3 is in the cut-off region and T4 is in the saturation, pulling down the signal to logic '0'. With the presented circuit topology, the voltage level for logic '1' is closer to V_{DD}.

Apart from Inverters, other standard digital gates NAND- and NOR-gates are also designed and characterised using the described measurement setup. Similarly, other standard digital logic gates, namely NAND- and NOR-gates are designed. The NAND- and NOR- are based on the diode load configuration with a level shifter stage. Thereby, the negative V_{SUP} voltage controls the pulldown function. The schematics for NAND- and NOR-gates are shown in figures S1 and S2, in the supplementary information.

The topologies were modified in accordance to simulation to improve the performance of the logic gates. The respective circuit topologies were simulated and the results were evaluated to optimize the parameters. The power supply and input voltages were selected based on the transistor characteristic to ensure that the respective OFETs operate in the

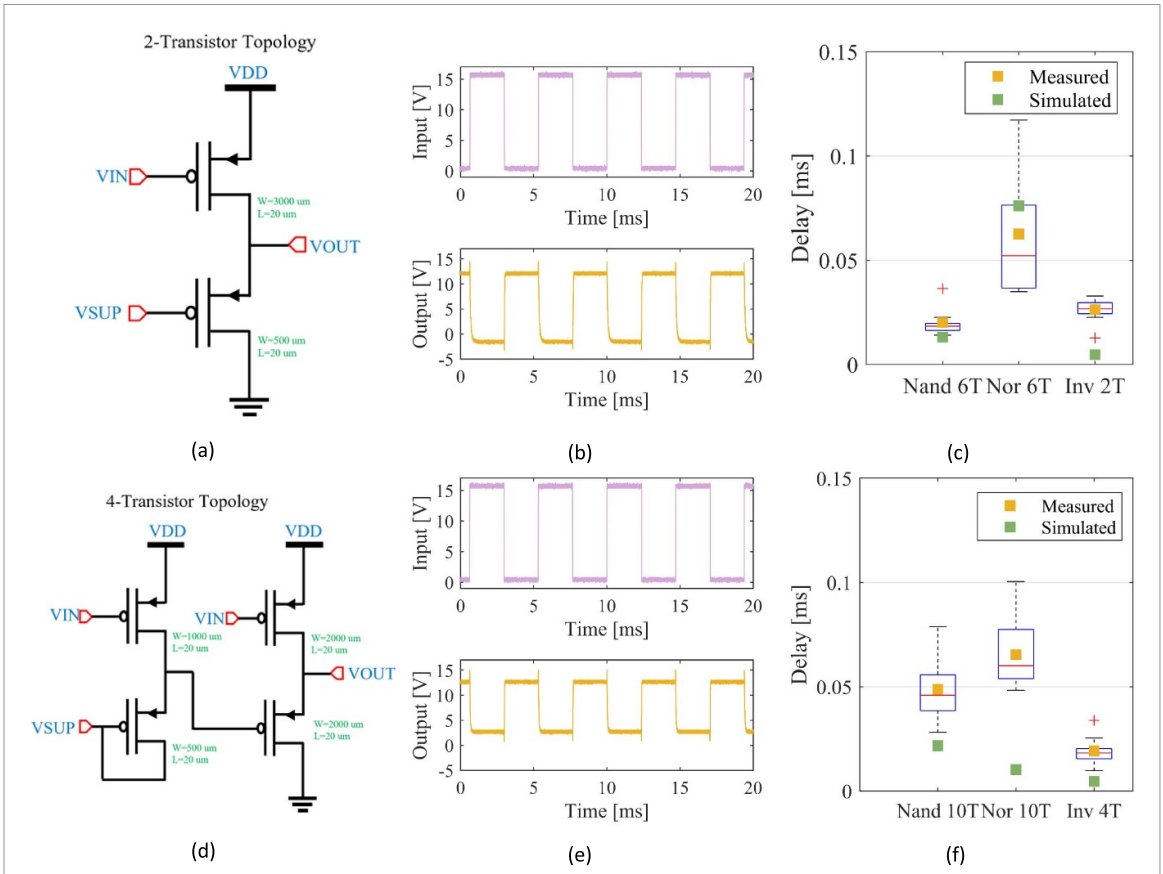

Figure 5. (a) Schematic and, (b) measured transient characteristics of 2-transistor inverter, (c) model-hardware correlation of logic gates (Inverter, Nand, Nor) designed using 2-T topology based on calculated and simulated delay, (d) schematic and, (e) measured transient characteristics of 4-transistor inverter, (f) model-hardware correlation of logic gates (Inverter, Nand, Nor) designed using 4-T topology based on calculated and simulated delay.

cut-off and the saturation regions. To select the most appropriate device geometry, a parameterized sweep was performed on the channel width (W). The delay analysis is presented in figures 5(c) and (f).

A tradeoff between the symmetry of the output characteristics, the rail-to-rail behaviour, and the gain of the inverter needs to be made. Depending on the requirements, 2-transistor or 4-transistor topologies need to be evaluated. The 4-transistor topology improves the rail-to-rail transistor but the higher transistor count could lead to a lower yield, due to the process variation.

5. Result and discussion

5.1. Model hardware correlation, ring oscillator

By comparing the 2 transistor topology with the 4-transistor topology, it can be seen that the switching behaviour and delay show significant improvements within the 4-transistor topology due to the level shifting stage. Due to the more accurate signal propagation, the circuit can be used to explore more complex digital and combinational circuits.

Both topologies are further explored with the help of a 5-stage ring oscillator. The ring oscillator is designed by connecting an odd number of inverters in series as shown in figure 6(a). The output of the last inverter is connected to the input of the first inverter to provide the feedback loop and create a self-oscillating output. Here we designed with the help of the PDK a five-stage ring oscillator. The supply voltage of the ring oscillator is connected to the V_{DD} pin of the respective inverters, the biasing voltage for the pull-down OFET of each inverter is applied to the V_{SUP} pin and the ground is connected to the common ground of the measurement setup. The output frequency of the ring oscillator quantifies the propagation delay of each inverter stage as shown:

$$t_d = \frac{1}{2 * n * f},$$

where t_d refers to propagation delay per stage, n refers to the number of stages in ring-oscillator and f refers to the frequency.

From figures 5(c) and (f) we observe that the mean value of the delay for 4T topology is lower as compared to the 2T topology. The variation is in the 4T topology higher due to a higher transistor count. From the ring oscillator measurements shown in figure 6(c), we observe a similar behaviour for the

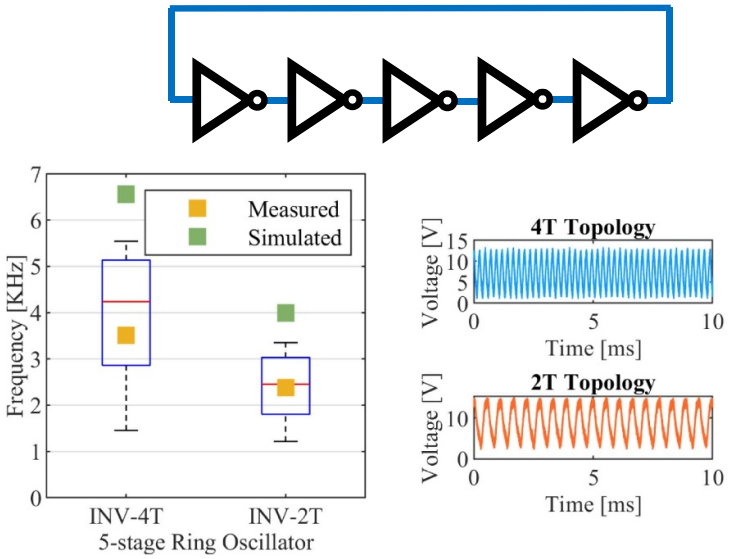

Figure 6. (a) Schematic of ring oscillator and, (b) measured transient characteristics of ring oscillator based on 2-T and 4-T inverter topology, (c) model-hardware correlation for single stage delay of ring oscillator based on different topologies.

performance. The 4T based rings are slightly faster (Mean frequency = 12 KHz) as compared to the 2T Transistor (Mean frequency = 10 KHz).

By extracting the propagation delay time of the two circuit topologies, the speed of the circuits are characterized. This could be required to avoid timing violations when circuits are designed. Moreover, the 4-transistor topology shows a better rail to rail behaviour with the output voltage showing almost full swing.

To optimising the process of circuit design, the standard cell library was created and characterised. These cells can be used by circuit designer to create complex circuits. Using these standard cells, a large area sensing platform consisting of pressure sensor based on an active matrix combined with decoder and a multiplex for addressing the sensor sensel is designed and demonstrated.

5.2. 4–16 binary decoder

An address decoder is a combinational circuit used for addressing the matrix elements It determines the address location to be reported for further processing. Using the input line, logic circuitry, enable output lines, output driver lines, it identifies the location in matrix from a predefined address range where a pressure change is experienced. Within a sensing matric, intersection of each row and column represent a sensel. It constantly scans and evaluated each sensel of the matrices. For each row and column, a unique address is assigned. When a sensel is activates, the change is electrical state is detected and the address is generated to determine which sensel is selected. The data is further processed to be able to map the information on a read-out screen.

The 4-to-16-line binary decoder is designed using a 4-transistor topology-based logic gate. The architecture includes 16 NAND gates with 4 inputs each and 4 inverters as shown in figure 7(a). The decoder is designed, optimised and layout is implemented using the FH-OPDK within the cadence EDA tool. The decoder is used to detect the location of the sensory change in the matrix by changing the read-out bits. The decoder is optimized to operate at a supply voltage of 40 V.

5.3. Large area sensing platform

The large area sensing platform circuit consist of a 16 × 16 pressure sensor matrix with two 4–16 binary decoder and a 16 × 1 multiplexer as shown in figure 8. Each individual sensel in the matrix consist of a pressure sensor combined with an OFET. The 16 rows and 16 columns of this matrix is attached to a respective decoder. These decoders are used for communicating the pressure distribution over the matrix. Two 4–16 decoders are a part of the demonstrator circuit for addressing the activated Sensel row and column. The decoder is designed using an inverter and a 4-input NAND gate as shown in the schematic diagram (figure 7(a)). The decoders help to reduce the number of interface wires to the silicon periphery circuit. The sensel are addressed as binary input and the data is delivered as an analogue stream using a 16 × 1 multiplexer consisting of 16 single transistors. With an external output device, it is possible to resolve pressure level applied to the sensor matrix.

When one sensel is active, the logic state is '0' for that column and row output line. The output is transmitted to the processing circuitry which is

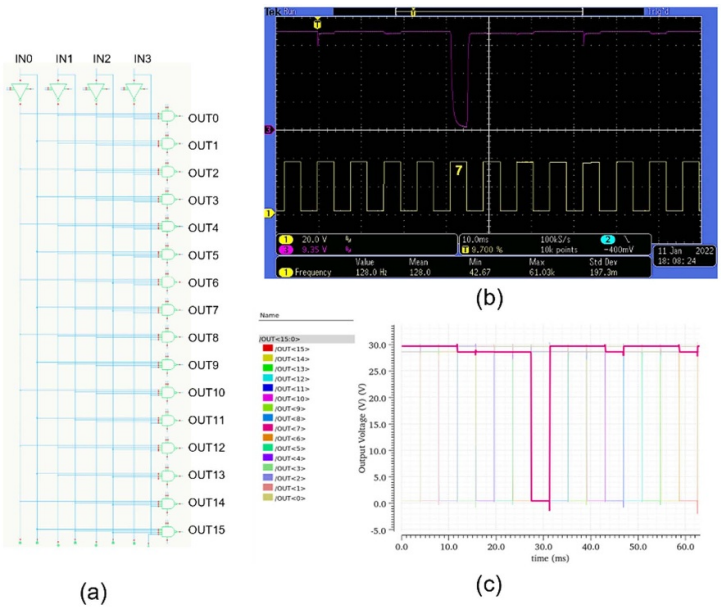

Figure 7. (a) Schematic, (b) measured transient characteristics, (c) simulated characteristic of 4–16 decoder.

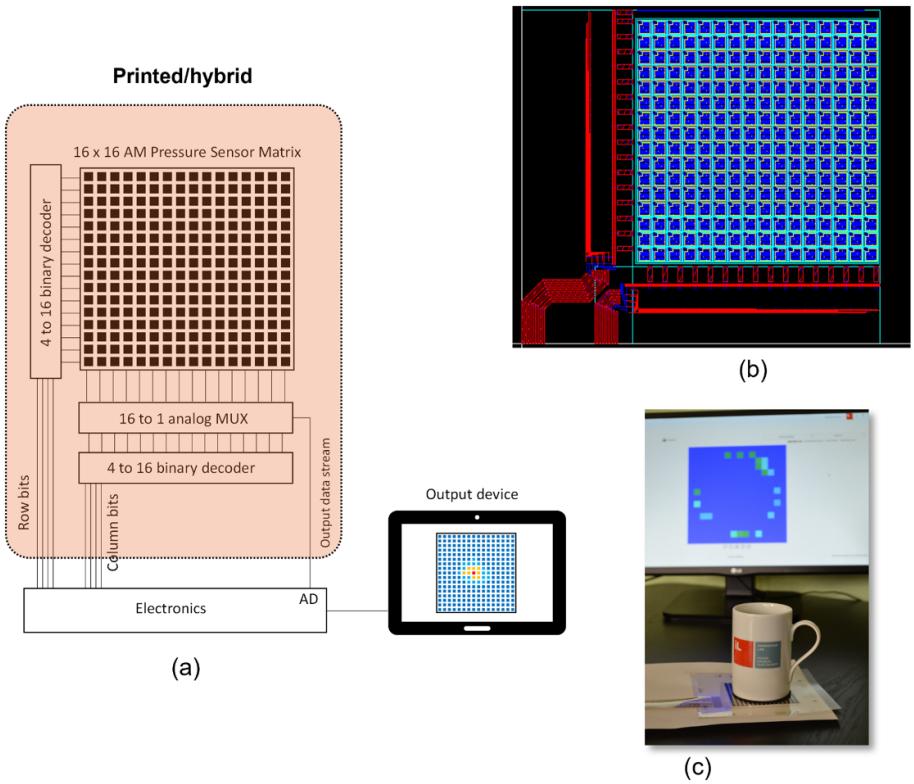

Figure 8. (a) Block diagram of sensing active matrix-based demonstrator with printed periphery circuit, (b) layout of the sensor matrix and decoder (c) demonstration of active-matrix demonstrator to sense the pressure of a coffee mug.

connected to a screen to observe the output on the screen.

The readout platform was an in house designed system to connect and control the printed circuitry. Due to limitations of printed organic electronics, it is not possible to print the whole readout system yet. For that reason, the readout system is based on traditional electronic components. However, the readout system is the driver for the flexible hybrid sensor system and enables a connection to a computer.

6. Conclusion

An organic hybrid printed technology is used to manufacture a p-type field effect transistor on a flexible substrate. The characterized data is used to create an accurate device model. Using the model, a PDK is developed for the presented transistor technology. The PDK is integrated in an EAD tool to create a full front-to-back circuit design flow. The design flow is adapted to the requirement of the presented technology by incorporating features such as assistive layout design, auto-layer generation for dielectric, etc. The design flow is used to construct a re-usable standard based on different circuit topologies cell library for designing complex circuitry. The standard cell based on digital logic gates is designed to understand the performance in terms of delay and the effect of variation due to fabrication. The delay of 0.03 ms for 2T topology and 0.02 ms for 4T topology establish itself as a high-performing organic hybrid technology. The PDK design flow is further used to design a 4–16 decoder. The large area sensor platform is achieved by integrating 2 decoders with a 16 × 16 active matrix and a single transistor per column connected as an amplifier. The demonstrator using an external output device can represent the spatial resolve pressure level applied to the sensor matrix.

The printed periphery circuit with matrix on one single substrate is a milestone achieved towards a fully integrated printed system on a chip based on a flexible substrate.

Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: https://radar.kit.edu/radar/en/dataset/sfIlFgiRZWyvsPRi.

Acknowledgments

The results are derived from the work under the Project 2-HORIZON. We thank Bundesministerium für Bildung und Forschung (BMBF) for the funding for this Project.

ORCID iDs

Palak Gupta https://orcid.org/0009-0000-2890-9249
Gabriel Cadilha Marques https://orcid.org/0000-0003-3718-7780

References

[1] Klauk H 2006 *Organic Electronics: Materials, Manufacturing, and Applications* 1st edn (Wiley) (https://doi.org/10.1002/3527608753)
[2] Luczak A, Mitra K Y, Baumann R, Zichner R, Luszczynska B and Jung J 2022 Fully inkjet-printed flexible organic voltage inverters as a basic component in digital NOT gates *Sci. Rep.* **12** 10887
[3] Gelinck G H *et al* 2004 Flexible active-matrix displays and shift registers based on solution-processed organic transistors *Adv. Mater.* **3** 106–10
[4] Chang J S, Facchetti A F and Reuss R 2017 A circuits and systems perspective of organic/printed electronics: review, challenges, and contemporary and emerging design approaches *IEEE J. Emerging Sel. Top. Circuits Syst.* **7** 7–26
[5] Loo Y-L and McCulloch I 2008 Progress and challenges in commercialization of organic electronics *MRS Bull.* **33** 653–62
[6] Wang L, Jiang K and Shen G 2021 A perspective on flexible sensors in developing diagnostic devices *Appl. Phys. Lett.* **119** 150501
[7] Wang X, Liu Z and Zhang T 2017 Flexible sensing electronics for wearable/attachable health monitoring *Small* **13** 1602790
[8] Logothetidis S and Laskarakis A 2009 Towards the optimization of materials and processes for flexible organic electronics devices *Eur. Phys. J. Appl. Phys.* **46** 12502
[9] Parashkov R, Becker E, Riedl T, Johannes -H-H and Kowalsky W 2005 Large area electronics using printing methods *Proc. IEEE* **93** 1321–9
[10] Wu X, Ma Y, Zhang G, Chu Y, Du J, Zhang Y, Li Z, Duan Y, Fan Z and Huang J 2015 Thermally stable, biocompatible, and flexible organic field-effect transistors and their application in temperature sensing arrays for artificial skin *Adv. Funct. Mater.* **25** 2138–46
[11] Gao W, Ota H, Kiriya D, Takei K and Javey A 2019 Flexible electronics toward wearable sensing *Acc. Chem. Res.* **52** 523–33
[12] Tariq Beigh N T, Beigh F T and Mallick D 2023 Machine learning assisted hybrid transduction nanocomposite based flexible pressure sensor matrix for human gait analysis *Nano Energy* **116** 108824
[13] Sekitani T and Someya T 2010 Stretchable, large-area organic electronics *Adv. Mater.* **22** 2228–46
[14] Liao C, Zhang M, Yao M Y, Hua T, Li L and Yan F 2015 Flexible organic electronics in biology: materials and devices *Adv. Mater.* **27** 7493–527
[15] Kciuk M, Kowalik Z, Lo Sciuto G, Sławski S and Mastrostefano S 2023 Intelligent medical velostat pressure sensor mat based on artificial neural network and arduino embedded system *Appl. Syst. Innov.* **6** 84
[16] Zang Y, Zhang F, Di C-A and Zhu D 2015 Advances of flexible pressure sensors toward artificial intelligence and health care applications *Mater. Horiz.* **2** 140–56
[17] Sun L, Fukuda K and Someya T 2022 Recent progress in solution-processed flexible organic photovoltaics *npj Flex. Electron.* **6** 89
[18] Matsui H, Takeda Y and Tokito S 2019 Flexible and printed organic transistors: from materials to integrated circuits *Org. Electron.* **75** 105432
[19] Parameswaran C and Gupta D 2019 Large area flexible pressure/strain sensors and arrays using nanomaterials and printing techniques *Nano Converg.* **6** 28
[20] Karimov K S, Nabi J-U, Ali R, Fatima N, Khan A, Muqeet Rehman M M and Mehran Bashir M M 2020 Resistive and impedimetric properties of elastic composite based on graphene and CNT under uniaxial compressive displacement *Adv. Compos. Mater.* **29** 559–68
[21] Zhang W*et al* 2010 The organic process design kit (OPDK) (available at: http://opdk.umn.edu/)
[22] Zhang W, Ha M, Braga D, Renn M J, Frisbie C D and Kim C H *A 1V Printed Organic DRAM Cell Based on Ion-Gel Gated Transistors with a Sub-10nW-per-Cell Refresh Power* (https://doi.org/10.1109/ISSCC.2011.5746339)
[23] Xia Y, Zhang W, Ha M, Cho J H, Renn M J, Kim C H and Frisbie C D 2010 Printed sub-2 V gel-electrolyte-gated polymer transistors and circuits *Adv. Funct. Mater.* **20** 587–94

[24] Zhou J, Ge T and Chang J S Fully-additive printed electronics: process development kit 2016 *2016 IEEE Int. Symp. on Circuits and Systems (ISCAS)* (*15 June 2023*) (IEEE) pp 862–5 (available at: https://ieeexplore.ieee.org/document/7527377)
[25] Pham H T *et al* 2016 Design and simulation of a 6-bit successive-approximation ADC using modeled organic thin-film transistors *Act. Passiv. Electron. Compon.* **2016** 7201760
[26] Arnal A, Terés L and Ramon E 2021 Organic and printed process design kits: review, analysis and comparison *Flex. Print. Electron.* **6** 033001
[27] Huang T, Lei T, Shao L, Sivapurapu S, Swaminathan M, Bao Z, Cheng K-T and Beausoleil R 2020 Process design kit and design automation for flexible hybrid electronics *J. Soc. Inf. Disp.* **28** 241–51
[28] Schliewe R R, Yildirim F A, von Emden W, Witte R, Bauhofer W and Krautschneider W 2006 Static model for organic field-effect transistors including both gate-voltage-dependent mobility and depletion effect *Appl. Phys. Lett.* **88** 233514
[29] Estrada M, Cerdeira A, Puigdollers J, Reséndiz L, Pallares J, Marsal L F, Voz C and Iñiguez B 2005 Accurate modeling and parameter extraction method for organic TFTs *Solid-State Electron.* **49** 1009–16
[30] Levenberg K 1944 A method for the solution of certain non-linear problems in least squares *Q. Appl. Math.* **2** 164–8
[31] Feng X, Punckt C, Marques G C, Hefenbrock M, Tahoori M B and Aghassi-Hagmann J 2019 Impact of intrinsic capacitances on the dynamic performance of printed electrolyte-gated inorganic field effect transistors *IEEE Trans. Electron Devices* **66** 3365–70
[32] Huang T-C, Fukuda K, Chun-Ming L, Yeh Y-H, Sekitani T and Someya T 2010 Pseudo-CMOS: a novel design style for flexible electronics *2010 Design, Automation & Test in Europe Conf. & Exhibition (DATE 2010)* (*15 June 2023*) (IEEE) pp 154–9 (available at: http://ieeexplore.ieee.org/document/5457220/)
[33] Huang T-C and Cheng K-T 2009 Design for low power and reliable flexible electronics: self-tunable cell-library design *J. Dispers. Sci. Technol.* **5** 206–15
[34] Myny K, Beenhakkers M J, van Aerle N A J M, Gelinck G H, Genoe J and Dehaene W Robust digital design in organic electronics by dual-gate technology *2010 IEEE Int. Solid-State Circuits Conf.—(ISSCC) 15 June 2023* (IEEE) 2010 pp 140–1 (available at: http://ieeexplore.ieee.org/document/5434020/)
[35] Yokogawa User's Manual 2011 *Yokogawa test and measurement Equipment* Model 701944/701945 (Yokogawa Test & Measurement Corporation) (available at: https://cdn.tmi.yokogawa.com/IM701944-01E.pdf)
[36] Rabaey J M 1996 Digital Integrated Circuits: a Design Perspective 1st edn (Prentice-Hall Inc.) (https://doi.org/10.5555/227375)