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A Switched-Capacitor Multilevel Inverter with Modified Pulse-Width Modulation and Active DC-Link Capacitor Voltage Balancing

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***Abstract*—Although switched-capacitor (SC) multilevel inverters (MLIs) offer self-voltage balancing of flying capacitors and voltage gain higher than unity, the advantages come at the cost of high current stress and power loss in the SC circuit and DC source. Moreover, the voltage balancing is often restricted to a limited range of modulation index. Another problem of MLIs with neutral-point clamped (NPC) front end is with DC-link capacitor voltage balancing under unbalanced load conditions, imploring sensor-based closed-loop control. This paper proposes a unity gain five-level active-NPC SC-MLI with inrush charging current attenuation and actively balanced DC-link capacitor voltages under all load conditions and over the entire range of modulation index and power factor. The modified pulse-width modulation results in most switches operating at a low switching frequency, minimizing switching losses in the SC circuit. The proposed MLI attains a maximum efficiency of 98.04% at an output power of 510 W. Experiments on a 2 kVA laboratory prototype validate the theoretical analysis. Results from transformerless grid-connected solar PV system show that the proposed MLI can inject power into the grid with a unity power factor under conditions of varying irradiance and provide the grid with reactive power as well.**

***Index Terms*—resonant power conversion, switched capacitor circuits**

I. Introduction

A. Motivation and incitement

SWITCHED-CAPACITOR (SC) multilevel inverters (MLIs) [1], [2] address the problem of sensor-based flying capacitor voltage balancing in conventional MLIs [3], [4] and improve DC-link voltage utilization. Common-ground (CG) and active-neutral-point-clamped (ANPC) SC-MLIs are extendible to multiple phases from a single DC source. The leakage current in CG MLIs is zero as it finds a path through the neutral or negative bus. However, they have a DC offset in the output voltage due to the non-ideal characteristics of the virtual DC bus capacitor, which is undesirable in transformerless grid-connected photovoltaic (PV) systems [5] and limits its application to a low power rating. An ideal ANPC MLI would have a minimum leakage current due to a constant common-mode voltage (CMV) and has potential industrial applications. They have a front end where the DC-link is split into two equal-valued capacitors to obtain the neutral point. SC circuits are integrated into the series ANPC MLI structures to eliminate the sensor-based closed-loop control for balancing the voltage across the floating capacitor and boosting the output voltage.

B. Literature review

A five-level ANPC SC-MLI shown in Fig. 1(a) with double the voltage gain of [3] is proposed in [6], which uses six switches, two discrete diodes, and three capacitors. The modular ANPC SC-MLI shown in Fig. 1(b) is proposed in [7] and produces a five-level output voltage but at the cost of ten switches and four capacitors. A five-level variant [8] is shown in Fig. 1(c), which replaces two switches in the SC circuit with discrete diodes. A five-level ANPC SC-MLI is formed in [9] by adding two switches and two capacitors in a 3-level NPC module. However, it does not provide any voltage gain over the MLI shown in [3]. The MLI in [6] has been improved in [10], as shown in Fig. 1(d), which reduces the voltage stress on the components to bring down the cost of the MLI. A six-level ANPC SC-MLI with 2.5 times voltage gain is shown in [11], which uses six switches, four discrete diodes, and three floating capacitors. The MLI in [12] dispenses with the need for a switch in the T-type module and uses a single floating capacitor reducing the number of components and the voltage stress even further while producing a seven-level output voltage.

The advantages of SC-MLIs are ruled out over fractional kilowatt power levels by the high current stress on the SC circuit and DC source. Several methods of inrush charging current attenuation have been proposed, which include introducing an inductor in the SC circuit [6], [9], [13] – [17], using a frontend DC-DC converter [18], [19], and using an input LC filter [20]. While [13], [14], [16] – [18] are H-bridge-based MLIs, the CG SC-MLIs [15], [19], [20] and ANPC SC-

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MLIs [6], [9] and [12] are of present interest.

SC-MLIs often replace the switches in the SC circuit with discrete diodes and appear to have fewer switches [21], [22]. This leaves the switched capacitors in a floating state below a specific modulation index, and the voltage balancing of capacitors is restricted [23]. The capacitor voltages diverge from the steady-state value, and the MLI becomes inoperative. The DC-link capacitor voltage balancing continues to be another problem in NPC MLIs [24], [25]. Most conventional and SC MLIs depend on the load to draw a balanced alternating current; the load current averaged over a fundamental cycle should be zero. This is only theoretical since unbalanced loads, and DC components in grid voltage will cause an imbalance in DC-link capacitor voltages [5]. In three-phase three-wire applications, a controlled zero-sequence voltage is injected to balance the DC-link voltages, which cancels out in line voltages [26], [27]. However, zero-sequence voltage injection is not permitted for single-phase applications as this will result in DC components in the reference current in transformerless grid-connected MLIs [5], [28].

C. Contribution and paper organization

The contribution of this paper is the design of an MLI with

(a) zero DC injection and minimum leakage current,

(b) balanced DC-link capacitor voltages tolerant to the load imbalance,

(c) operation over the entire range of modulation index, and

(d) inrush charging current attenuation and minimum switching losses in the SC circuit.

A unity gain five-level ANPC SC-MLI is proposed in this paper. The input current and capacitor charging current are attenuated by a quasi-resonant circuit that links the DC-link capacitors to the floating capacitor. Introducing an inductor does not distort the output voltage since the link is independent of the load current path. The bidirectional link also provides for the active balancing of the DC-link capacitor voltages throughout the entire range of modulation index and power factor. Section II of the paper describes the inverter circuit and switching states. The modified pulse-width modulation is described in Section III, followed by the active DC-link capacitor voltage balancing in Section IV. The equations for sizing passive components are derived in Section V. Section VI shows the operation of the proposed MLI in a single-phase, single-stage, 240 V, 2000 W transformerless PV system connected to the electrical utility grid. Section VII shows the simulation results and power loss analysis. Section VIII compares the proposed MLI with recently published ANPC SC-MLIs with a similar number of voltage levels. The experimental results on a 2000 VA laboratory prototype are shown in Section IX. The possible applications and further development have been discussed in Section X, and the paper is finally concluded in Section XI.

II. Proposed Five-Level SC-MLI

The proposed five-level SC-MLI in Fig. 2 shows a DC voltage source (V_{dc}), two DC-link capacitors C_1 and C_2, six switches S_1 – S_6, a quasi-resonant circuit (in blue), and a switched capacitor C_3. The four switches S_7 – S_{10} of the quasi-resonant circuit form a bidirectional path between the midpoint of the DC-link and C_3 through the resonant inductor L_r and conduct the charging current only and not the load current. The six switches S_1, S_2, S_7 – S_{10} operate at low frequency and just four switches S_3 – S_6 operate at high frequency. The steady-state voltage across C_1 (V_{C1}), C_2 (V_{C2}), and C_3 (V_{C3}) are $V_{dc}/2$.

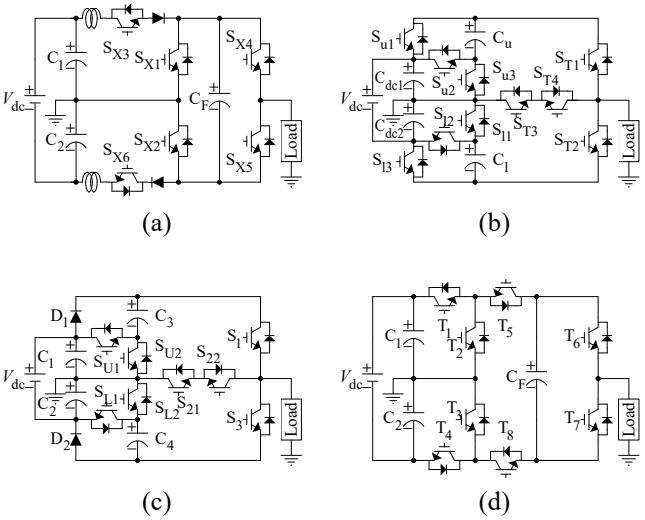


Fig. 1. Five-level ANPC SC-MLIs shown in **(a)** [6], **(b)** [7], **(c)** [8], and **(d)** [10].

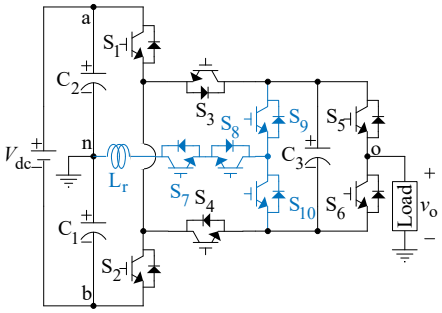


Fig. 2. Circuit of the proposed five-level ANPC SC-MLI.

The switching states of the SC-MLI in Fig. 3 show the path of the load current (in red) and the charging current (in blue) for a load of arbitrary power factor. In State 1, S_1, S_4, and S_5 connect C_2 and C_3 in series to give the positive peak output voltage (v_o) of V_{dc}. S_4 turns off and S_3 turns on in State 2 and connects C_2 to the load to give $v_o = V_{dc}/2$. As S_7, S_8, and S_{10} turn on, L_r, C_2, C_3, and the parasitic resistances form a resonant circuit and initiate the charging current (i_{ch}) from C_2 to C_3. The current i_{ch} first increases to the peak value and then begins to decrease and crosses zero in State 3a. S_1, S_3, and S_6 connect C_2 and C_3 in anti-series give $v_o = 0$.

The current i_{ch} continues to conduct from C_1 to C_3 through L_r in State 3b as S_{10} turns off and S_9 turns on. S_2, S_4, and S_5 connect C_1 and C_3 in anti-series to give $v_o = 0$. In State 4, S_5 turns off and S_6 turns on and connects C_1 to the load to give $v_o = V_{dc}/2$. The current i_{ch} increases to the peak value and begins to decrease and finally extinguishes at the zero crossing in State 5. S_2, S_3, and S_6 connect C_1 and C_3 in series to give the negative

peak output voltage v_o = -V_{dc}. The current i_{ch} conducts continuously from State 2 to State 4 except for the interruption between States 3a and 3b due to the dead-time in a practical inverter.

III. Modified Pulse-Width Modulation

This Section discusses the modified pulse-width modulation method for the proposed five-level MLI and highlights the differences from conventional schemes.

This paper takes the phase disposition PWM (PDPWM) [29] as an example to describe the modulation method as it has the least line voltage harmonics for three-phase applications. A sinusoidal reference signal, four level-shifted triangular carrier signals, and three constant values have been used to generate the gate pulses for a single phase of the proposed MLI. The generation of gate pulses from the comparison of the reference signal with the carrier signals and the constant values is shown in Fig. 4. The reference signal is represented by a green sinusoidal waveform at the fundamental frequency. The four triangular carrier signals at the switching frequency are represented in blue, and the constant values are represented in red. Based on this depiction, the generation of gate pluses from the modulated waveform has been analyzed.

The reference signal is compared with the level-shifted carrier signals. The resultant is the modulated multilevel waveform at the switching frequency. Fig. 4(b) shows the generation of the gate pulses for S_3 – S_6 by the lookup table from the level information and the pulse pattern of the modulated waveform and the switching states for each voltage level in Fig. 3. Alternatively, the switching sequence can be decomposed into logical equations and implemented using logic gates as shown in [30].

The gate pulses for S_1, S_2, S_7 – S_{10} are generated by comparing the reference signal with three constant values. The two AND gates and an OR gate generate the gate pulses from the resultant output of the comparators as shown in Fig. 4(c). The pattern of the gate pulses shows that S_1 and S_2 operate at just the fundamental frequency and S_7 – S_{10} operate at twice the fundamental frequency only. The distinct rising and falling edges and continuous conduction of the charging current allow for quasi-resonant capacitor charging. The recurrent gating of these switches in the intermittent time duration is disabled to contain the charging current within the continuous conduction period thus avoiding switching losses. Consequently, most of the switching losses are incurred by just four switches S_3 – S_6. The operation of these switches at a high frequency is indispensable for the synthesis of the multilevel output voltage waveform.

Limiting the switching of S_1, S_2, S_7 – S_{10} to a low frequency reduces the switching losses to the minimum possible in a SC-MLI reported in the literature. The voltage transients due to the high-frequency switching of current through the charging inductor L_r are also avoided.

IV. Active DC-Link Capacitor Voltage Balancing

The active DC-link capacitor voltage balancing of the proposed MLI inherently provided by the topology is discussed in this Section.

The switching States 3b and 3a producing zero voltage levels

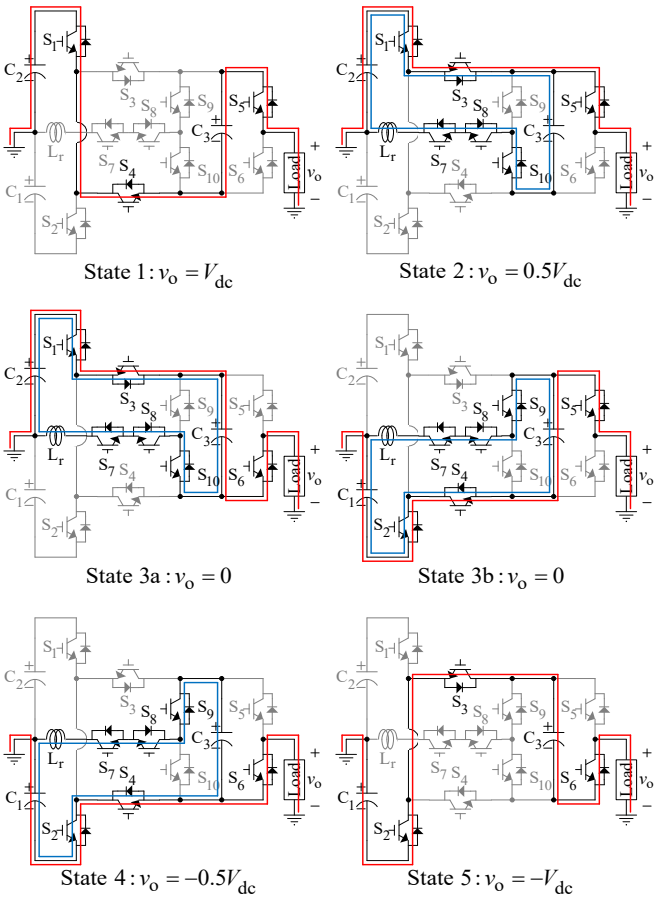


Fig. 3. Switching states of the proposed MLI.

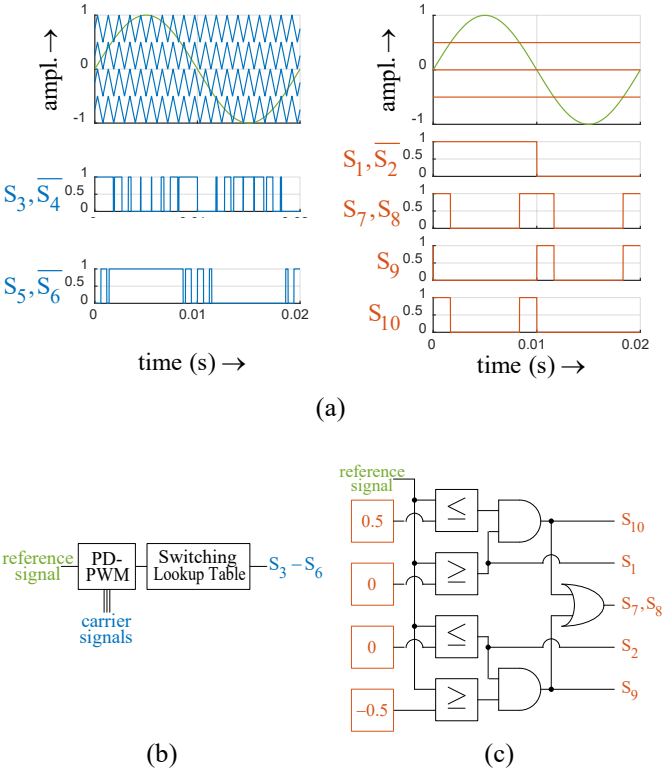


Fig. 4. (a) Modified PDPWM, **(b)** generation of gate pulses for S_3 – S_6, and **(c)** generation of gate pulses for S_1, S_2, S_7 – S_{10}.

are considered in Fig. 5. The paths of the load current are omitted for the simplicity of depiction. The flow of the charging current that discharges a DC-link capacitor is represented in red and that charges a DC-link capacitor is represented in green in the two zero voltage levels and are discussed in detail.

State 3b (v_o = 0): The switches S_2 and S_4 connect the switched capacitor C_3 to the DC-link capacitor C_1 through the switches S_7 – S_9 and the inductor L_r that constitute the quasi-resonant link. For this demonstration, the capacitor C_1 is considered to be at a higher potential than the capacitor C_2. The voltages across the capacitors are such that $v_{C1} > v_{C2} > v_{C3}$ at the start of State 3b. The difference between v_{C1} and v_{C3} (v_{C1} - v_{C3} > 0) causes the charging current i_{ch} to initiate from C_1 and flow towards C_3 through the resonant inductor L_r. The current i_{ch} continues to conduct without interruption until v_{C3} becomes approximately equal to v_{C1} (v_{C1} - $v_{C3} \approx 0$).

State 3a (v_o = 0): The switches S_2, S_4, and S_9 turn off and the S_1, S_3, and S_{10} turn on at the transition from switching states 3b to 3a. The difference between v_{C3} and v_{C2} (v_{C3} - $v_{C2} > 0$) causes i_{ch} to continue conducting through L_r in the same direction from C_3 towards C_2 until the difference between v_{C2} and v_{C3} becomes approximately equal to zero (v_{C3} - $v_{C2} \approx 0$). Hence it can be concluded that the voltages across the capacitors are balanced at the end of the switching cycle ($v_{C1} \approx v_{C3} \approx v_{C2}$).

It is seen that the bidirectional quasi-resonant circuit in effect allows C_3 to act as a buffer and transfer energy from C_1 to C_2 and actively restores the DC-link capacitor voltage balance. It can be demonstrated similarly that the voltage balance is actively restored when $_{vC3} > v_{C2} > v_{C1}$ or when any voltage gradient exists between the DC-link capacitors. This feature is inherently provided by the topology throughout the entire range of modulation index and power factor since the zero voltage levels act towards restoring the DC-link capacitor voltage balance and the charging current path is independent of that of the load current. This method is verified through rigorous experimentation in Section IX.

V. Sizing of Capacitors and Resonant Inductor

A. Determination of capacitances

The capacitances are determined from the waveforms of v_o, v_{C1}, and v_{C3} in Fig. 6 showing the longest discharging time (*LDT*) of C_1 (LDT_{C1}) and C_3 (LDT_{C3}) in fundamental time period (T) [32]. At fundamental frequency ($\omega = 2\pi/T$) and modulation index (m_i), time t_2 and t_3 are given by (1).

$$t_2 = \frac{1}{\omega} \times \sin^{-1}\left(\frac{1}{2m_i}\right);\ t_3 = \frac{T}{2} - t_2 \tag{1}$$

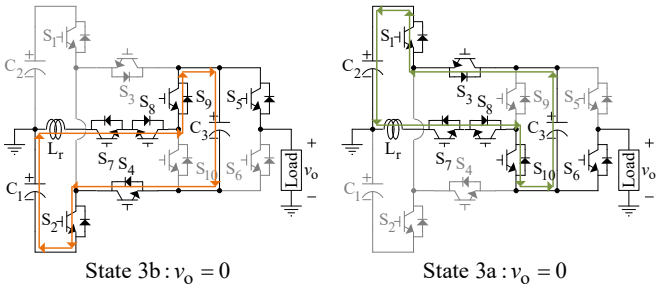
For an inductive load of apparent power (S), peak load current (I_{opk}), and impedance angle (ϕ), the instantaneous load current ($i_o(t)$) is given by (2).

$$i_o(t) = I_{opk} \sin(\omega t - \phi) \tag{2}$$

The charge drawn from C_1 (Q_{C1}) and C_3 (Q_{C3}) for load current i_o are given by (3).

$$Q_{C1} = \int_{t_4}^{t_1} i_o(t)dt = \int_0^{T/2} i_o(t)dt;\ Q_{C3} = \int_{t_2}^{t_3} i_o(t)dt \tag{3}$$

The LDT_{C2} is equal to LDT_{C1} and phase displaced by $T/2$.



(a) (b)

Fig. 5. (a) Switching State 3b and **(b)** switching State 3a.

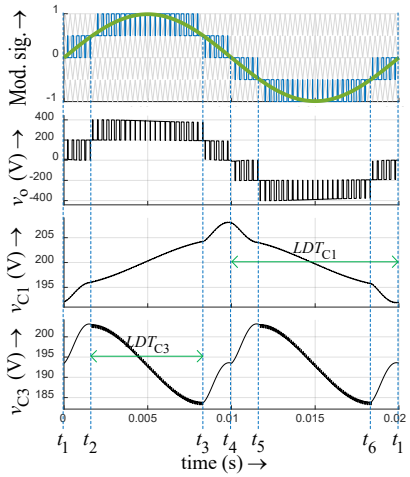


Fig. 6. Waveforms of modulated signal and voltages v_o, v_{C1}, and v_{C3}.

Using (1) – (3), the optimum capacitance of C_1 (C_{1opt}), C_2 (C_{2opt}), and C_3 (C_{3opt}) for voltage ripple (ΔV) per unit are determined as (4) and (5).

$$C_{1opt} = C_{2opt} = \frac{Q_{C1}}{\Delta V \times V_{C1}} = \frac{8S}{\omega \times \Delta V \times V_{dc}^2} \times \cos(\phi) \tag{4}$$

$$C_{3opt} = \frac{Q_{C3}}{\Delta V \times V_{C3}} = \frac{8S}{\omega \times \Delta V \times V_{dc}^2} \times \sqrt{1 - \frac{1}{4m_i^2}} \times \cos(\phi) \tag{5}$$

In a m-phase SC-MLI, the DC-link capacitors are charged and discharged m number of cycles in time T. The optimum capacitances are given as C_{1opt}/m and C_{2opt}/m.

B. Determination of resonant inductance

The equivalent circuit of the path of charging current i_{ch} in State 2 to 3a in Fig. 7 shows an ideal switch (SW) and the resonant inductance L_r in series with the equivalent voltage (v_{eq}), equivalent capacitance (C_{eq}), and equivalent resistance (r_{eq}) given by (6) – (8).

$$v_{eq} = v_{C2} - v_{C3} - 2v_f - 3v_d \tag{6}$$

$$C_{eq} = \frac{C_2 \times C_3}{C_2 + C_3} \tag{7}$$

$$r_{eq} = r_{C2} + r_{C3} + 2r_{on} + 3r_d \tag{8}$$

Here v_{C2} and v_{C3} are the voltage across C_2 and C_3 at the beginning of State 2; r_{C2} and r_{C3} are the equivalent series resistance (ESR) of C_2 and C_3; v_f and r_{on} are the forward voltage

and internal resistance of the IGBTs; v_d and r_d are the forward voltage and internal resistance of the antiparallel diode of the IGBTs.

The waveform of i_{ch} in Fig. 8 shows that in State 2, S_7, S_8, and S_{10} turn on at t_3 and i_{ch} first increases to the negative peak value ($-I_{chpk}$) and then begins to decrease. The current i_{ch} decreases further in State 3a and crosses zero at t_4 and subsequently continues to conduct in State 3b through S_7, S_8, and S_9. In State 4, i_{ch} increases to the positive peak value (I_{chpk}) and begins to decrease, and finally extinguishes at the zero crossing at t_5 at the beginning of State 5.

The ringing time period (t_r) and ringing frequency (ω_r) of the quasi-resonant circuit are given by (9) and (10).

$$t_r = \frac{2}{\omega} \times \sin^{-1}\left(\frac{1}{2m_i}\right) \tag{9}$$

$$\omega_r = \frac{2\pi}{t_r} = \sqrt{\frac{1}{L_r \times C_{eq}} - \left(\frac{r_{eq}}{2L_r}\right)^2} \tag{10}$$

Using (9) and (10), the optimum resonant inductance (L_{ropt}) is determined as (11) [31].

$$L_{ropt} = \frac{1+\sqrt{1-(\omega_r \times r_{eq} \times C_{eq})^2}}{2 \times \omega_r^2 \times C_{eq}} \tag{11}$$

The damping factor (ξ) and resonant frequency (ω_0) of the circuit given by (12) show that the circuit is underdamped ($\xi < \omega_0$).

$$\xi = \frac{r_{eq}}{2L_r};\ \omega_0 = \frac{1}{\sqrt{L_r \times C_{eq}}} \tag{12}$$

The peak resonant inductor current (I_{chpk}) is given by (13).

$$I_{chpk} = \frac{v_{eq}}{\omega_r \times L_r} \times \exp\left(-\xi \times \frac{t_r}{4}\right) \tag{13}$$

The peak charging current without L_r (I_{pk}) and the charging current attenuation (k_{Ich}) are given by (14).

$$I_{pk} = \frac{v_{eq}}{r_{eq}};\ k_{Ich} = \frac{I_{pk}}{I_{chpk}} \tag{14}$$

The variation of optimum capacitances C_{1opt} and C_{2opt}, resonant inductance L_{ropt}, and peak resonant inductor current I_{chpk} with apparent power S for various values of ΔV at unity power factor $\cos(\phi)$ and modulation index m_i as an example are shown in Fig. 9. It is seen that L_{ropt} decreases with an increase in S. The increase in I_{chpk} is linear with an increase in S as opposed to the exponential increase without L_r. By properly sizing the capacitors and inductor, and controlling the value of m_i to 0.8 – 0.9 [6], a low to medium power system using reasonably rated semiconductors can be designed with the proposed MLI. Moreover, various combinations of the values of $\cos(\phi)$ and m_i may be chosen for a broader range of operating conditions.

Eqns. (4), (5), and (11) give the optimum capacitances and inductance. These values are resilient to the parameter deviation of the components and rounding to commercially available values according to the IEC 60063:2015 preferred number series for resistors and capacitors. Systematic calculations considering the engineering tolerances are expected to yield a good design.

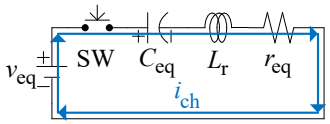


Fig. 7. Equivalent circuit of the path of charging current.

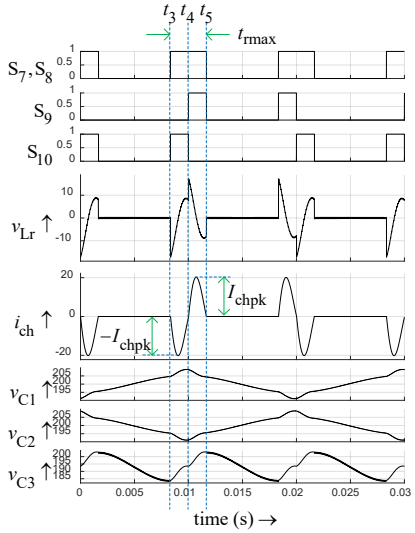


Fig. 8. Gate pulses of switches S_7 – S_{10}, waveforms of inductor voltage v_{Lr} and current i_{ch}, and capacitor voltages v_{C1}, v_{C2}, and v_{C3}.

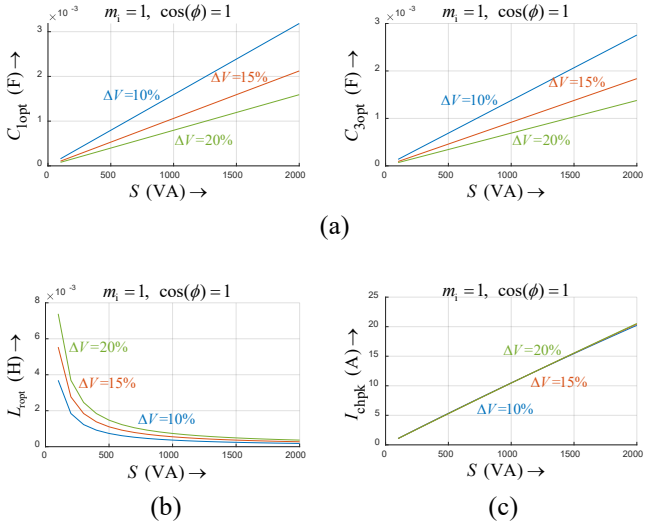


Fig. 9. Variation of **(a)** capacitances C_{1opt} and C_{3opt}, **(b)** inductance L_{ropt}, and **(c)** current I_{chpk} with power S.

C. Design of line filter

A line filter is customary for an inverter to meet the IEEE Std 1547™-2018 of interfacing distributed energy resources to the grid. Although the design of *LCL* filters for conventional two-level inverters has been discussed extensively in the literature, there is a gap in providing a systematic methodology for the design of *LCL* filters for multilevel inverters.

A *LCL* line filter is designed for the proposed MLI as shown in Fig. 10. In an N_L-level inverter with a peak output voltage (V_{op}) operating at a switching frequency (f_s), the minimum filter

inductance (L_{fmin}) for a maximum allowable peak ripple current (ΔI_{opmax}) per unit of the rated peak output current (I_{op}) is given by (15) [33].

$$L_{\text{f min}} = \frac{V_{\text{op}}}{(N_{\text{L}}-1)/2} \times \frac{1}{4 \times f_{\text{s}} \times I_{\text{op}} \times \Delta I_{\text{op max}}} \tag{15}$$

The switching frequency f_{s} refers to the frequency of the carrier signals discussed in Section III. This is reflected as the frequency of the most dominant harmonic component in the N_{L}-level inverter output voltage as seen in the later Sections. This value is constant along the entire operating range.

With a rated rms output current (I_{o}) and fundamental frequency ω, the maximum filter inductance (L_{fmax}) for a maximum voltage drop of (ΔV_{Lf}) per unit of the rms output voltage (V_{o}), is given by (16).

$$L_{\text{f max}} = \frac{\Delta V_{\text{Lf}} \times V_{\text{o}}}{\omega \times I_{\text{o}}} \tag{16}$$

The filter inductance (L_{f}) is selected to have a value between L_{fmin} and L_{fmax} ($L_{\text{fmin}} < L_{\text{f}} < L_{\text{fmax}}$). The inverter side filter inductance (L_{f1}), and the load side filter inductance (L_{f2}) are given by (17).

$$L_{\text{f1}} = L_{\text{f2}} = \frac{L_{\text{f}}}{2} \tag{17}$$

The resonant frequency of the filter (ω_{fr}) is selected to have a considerable separation between the fundamental frequency ω and the switching frequency ($\omega_{\text{s}} = 2\pi f_{\text{s}}$). An initial guess for the value of ω_{fr} can be obtained from (18) and can be adjusted to have a reasonable value of filter capacitance.

$$\omega_{\text{fr}} \approx \sqrt{\omega \times \omega_{\text{s}}} \tag{18}$$

For the filter resonant frequency ω_{fr}, the minimum filter capacitance (C_{fmin}) is given by (19). The maximum filter capacitance (C_{fmax}) for a maximum reactive power (ΔQ_{Cf}) per unit of the rated power S is given by (20)

$$C_{\text{f min}} = \frac{4}{\omega_{\text{fr}}^{\,2} \times L_{\text{f}}} \tag{19}$$

$$C_{\text{f max}} = \frac{\Delta Q_{\text{Cf}} \times S}{\omega \times V_{\text{o}}^{\,2}} \tag{20}$$

The filter capacitance (C_{f}) is selected to have a commercially available value between C_{fmin} and C_{fmax} ($C_{\text{fmin}} < C_{\text{f}} < C_{\text{fmax}}$). For a quality factor (QF), the damping resistance (R_{d}) is given by (21).

$$R_{\text{d}} = \sqrt{\frac{L_{\text{f}}/(4 \times C_{\text{f}})}{QF^2 - 1}} \tag{21}$$

The internal resistance of the inductors L_{f1} and L_{f2} are obtained from the datasheet. For metalized film capacitors, the ESR of the capacitor C_{f} is neglected.

The procedure discussed above may be followed for all small to medium-scale grid-connected renewable energy conversion systems employing MLIs.

VI. Single-Phase Transformerless Grid-Connected Solar PV System

This Section shows the operation of the proposed MLI in a single-phase, single-stage, 240 V, 2000 W transformerless PV system connected to the electrical utility grid.

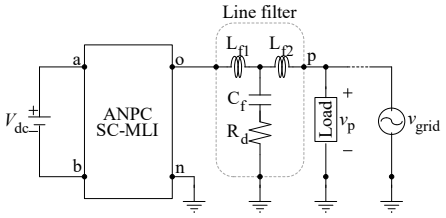


Fig. 10. *LCL* line filter designed for the proposed MLI.

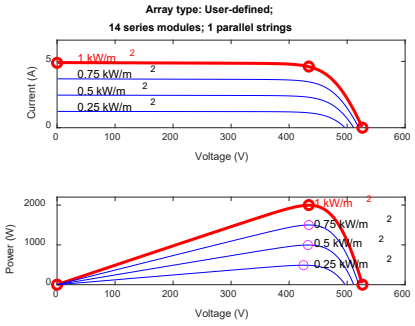


Fig. 11. I-V and P-V characteristics of the PV array.

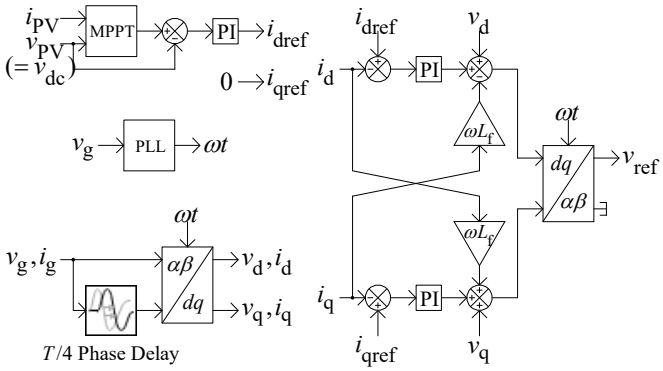


Fig. 12. Control strategy of the single-phase grid-connected PV system.

The equivalent single-diode model shown in [35] is used to implement the PV module. The PV array consists of one string of 14 modules connected in series. Assuming uniform solar irradiance of 1000 W/m^2 and temperature of 25°C across all the solar panels, the string can produce a steady-state output of approximately 2000 W at a terminal voltage of 434 V. The current-voltage (I-V) and power-voltage (P-V) characteristics of the PV array are shown in Fig. 11.

The control system shown in Fig. 12 comprises a nested control scheme with a maximum power point tracking (MPPT) controller, an outer voltage control loop, and an inner current control loop. The MPPT controller based on the 'Perturb and Observe' technique [36] influences the current supplied to the grid by automatically varying the v_{dc} reference signal of the voltage controller to obtain a DC voltage which will extract maximum power from the PV array.

The outer voltage control loop maintains the DC-link voltage at the reference set by the MPPT controller. The voltage controller determines the grid current amplitude reference. Since the converter initially injects power into the grid with a unity power factor, the generated current reference equals the

d-axis current (i_{dref}) in the synchronous reference frame, and the q-axis current reference (i_{qref}) is set to zero.

The synchronous transformations reduce the complexity by transforming the AC (time-varying) quantities to equivalent DC (time-invariant) quantities and implementing PI controllers for the d- and q-axis, respectively. The grid quantities are assumed to align with the α-axis, and the β-axis quantities are emulated by phase shifting the α-axis quantities by a quarter of the fundamental period ($T/4$) [37]. The measured α and derived β quantities are transformed into the dq-axis using the angle ωt generated by a phase-locked loop (PLL). The synchronous reference frame PI controllers calculate the $\alpha\beta$ voltage vector reference (v_{ref}). This vector is scaled by the peak grid voltage amplitude to generate the modulation index.

VII. Simulation Results and Power Loss Analysis

The proposed MLI is modeled using PLECS Blockset in MATLAB/Simulink for S = 2000 VA, V_{dc} = 400 V, fundamental frequency (f) = 50 Hz, switching frequency f_s = 10 kHz, and ΔV = 10%. The ratings of capacitors, resonant inductor, IGBTs, and discrete diodes are listed in Table I. The equivalent circuit and thermal description of the IGBT and discrete diodes, ESR of the capacitors, and internal resistance of the inductor were parameterized from the datasheets.

The waveforms of output voltage v_o, current i_o, and capacitor voltages (v_C) for load resistance $R_L = 40\ \Omega$ and $m_i = 1$ are shown in Fig. 13. The voltage and current waveforms have five distinct levels and the capacitor voltages are balanced in steady-state.

Due to the pulsed nature of capacitor currents and high-frequency switching, the power losses computed by analytical methods yield inaccurate results [34]. To determine the power losses, the converter has been modeled using the PLECS Blockset in MATLAB/Simulink which uses a lookup table approach to calculate the losses. The input power (P_i) of the MLI is 2078 W. The breakup of the total conduction loss of 49.15 W and total switching loss of 3.750 W is shown in Fig. 14(a) and the contribution of the components to the total power loss is shown in Fig. 14(b). The switching losses of S_1, S_2, S_7 – S_{10} are less than 2% of the total switching loss and most of the switching losses are limited to just four switches S_3 – S_6 that operate at high frequency. The total power loss (P_L) is 52.91 W and the output power (P_o) and efficiency (η) are given by (22).

$$P_o = P_i - P_L = 2025\ \text{W};\ \eta = \frac{P_o}{P_i}\times 100 = 97.45\% \qquad (22)$$

To provide a better understanding of the impact of the passive damped LCL line filter on the overall system efficiency, the model is simulated with an inverter side filter inductance L_{f1} and load side filter inductance L_{f2} of 2.7 mH, filter capacitance C_f of 4.7 µF, and damping resistance R_d of 6.8 Ω as enlisted in Table I. The R_d contributes to an additional power loss of 2.004 W. The value of P_L increases to 54.90 W, and the values of P_o and η decrease to 2023 W and 97.36%, respectively. Hence active damping methods may be preferred to passive damping from an efficiency point of view [38].

TABLE I
Components Used for Simulation and Experiment

Components	Part No.	Specifications
Switches (IGBTs)	Infineon IKW75N60T	V_{CE} = 600 V, I_C = 75 A
Capacitors C_1, C_2	Alcon PG-8K	250 V, 2200 µF
Capacitor C_3	Alcon PG-8K	250 V, 2200 µF
Inductor L_r	Rishab Industries	180 µH, 30 A
Inductors L_{f1}, L_{f2}	Rishab Industries	2.7 mH, 10 A
Capacitor C_f	WIMA MKS 4	4.7 µF, 400 VAC
Resistor R_d	Dale CP	6.8 Ω, 5 W

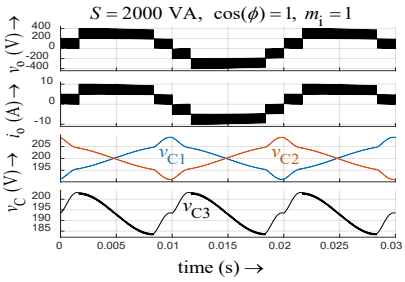


Fig. 13. Waveforms of voltage v_o, current i_o, and capacitor voltages v_C.

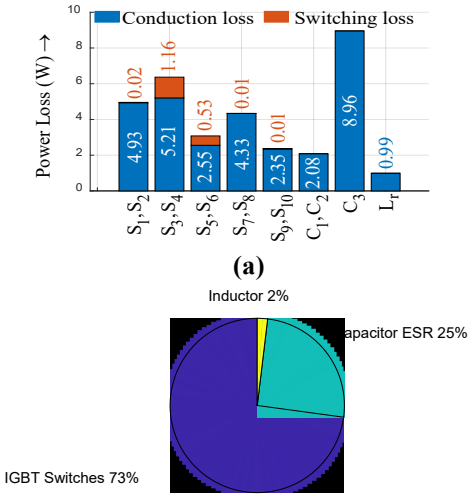


Fig. 14. (a) Conduction and switching loss of the components, and **(b)** distribution of the total power loss.

TABLE II
Comparison of the Proposed MLI with Recently Published ANPC SC-MLIs

Ref.	N_L	N_S	N_{DD}	N_C	G_v	TSV_{pu}	BD	CA	VB
[6]	5	6	2	3	1	6	N	Y	N
[7]	5	10	0	4	1	8	Y	N	N
[8]	5	8	2	4	1	8	N	N	N
[9]	5	6	2	4	0.5	7	N	Y	N
[10]	5	8	0	3	1	5	Y	N	N
[11]	6	6	4	5	2.5	7	N	N	N
[12]	7	9	0	3	1.5	5.3	Y	N	N
[P]	5	10	0	3	1	6	Y	Y	Y

BD: bidirectional capacitor charging path, **CA:** charging current attenuation, **VB:** active neutral-point voltage balancing ability.

TABLE III
COMPARISON OF VOLTAGE STRESS, CURRENT STRESS, AND SWITCHING FREQUENCY OF THE COMPONENTS

Ref.	Voltage stress								Current stress						Switching frequency			
	Switches			Diodes		Capacitors			Switches			Diodes			Switches		Diodes	
	$3V_{op}/2$	V_{op}	$V_{op}/2$	V_{op}	$V_{op}/2$	V_{op}	$V_{op}/2$	$V_{op}/4$	I_{ch}	$I_{ch}+I_o$	I_o	I_{ch}	$I_{ch}+I_o$	I_o	f	f_s	f	f_s
[6]		4	2		2	1	2			2	4		2		2	4		2
[7]	2	2	6				4		2	2	6					10		
[8]	2	2	4		2		4		2		6		2			8		2
[9]		4	2	2			2	2		2	4		2		2	4		2
[10]		2	6			1	2			4	4				2	6		
[12]			9			1	2			4	5					9		
[P]		2	8				3		4	4	2				6	4		

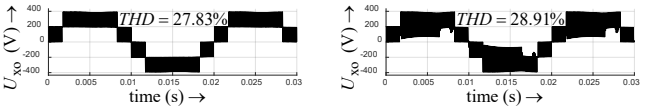
VIII. COMPARATIVE STUDY

The proposed MLI [P] is compared with some of the most recently published ANPC SC-MLIs in Table II in terms of the number of output voltage levels (N_L), number of switches (N_S), number of discrete diodes (N_{DD}), number of capacitors (N_C), voltage gain (G_v), bidirectional capacitor charging path (BD), charging current attenuation (CA), and active neutral-point voltage balancing ability (VB). Total standing voltage per unit (TSV_{pu}) is the ratio of the summation of the blocking voltage of all semiconductor devices to the peak output voltage. The MLIs are modeled using PLECS Blockset for $S = 2000$ VA following the design guidelines in the papers.

The MLIs in [6], [8], and [11] replace switches in the charging current path with discrete diodes and appear to have a lesser number of switches. These MLIs are incapable of bidirectional power flow which is necessary for regenerative braking in motor drives [10].

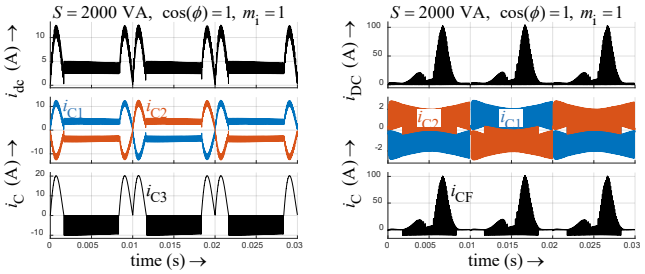
The comparison of voltage stress, current stress, and switching frequency of the components of the proposed MLI with the MLIs in comparison are shown in Table III. The voltage stress is normalized to the peak output voltage V_{op}. The MLI in [11] could not be shown since it uses switches of a wider variety of voltage ratings than the other MLIs in comparison. The is MLIs in [7] and [8] require switches rated above V_{op} making them suitable only for low-voltage applications. The MLIs in [6], [10], [11] – [12] require capacitors rated at V_{op} increasing the insulation requirements and making the inverter bulky. The MLIs in [6] – [12] have numerous switches operating at the switching frequency f_s. The chopping of capacitor charging current i_{ch} at a high frequency, together with the blocking voltage causes high switching losses in the semiconductor components and low power conversion efficiency, which is one of the reasons why the application of SC-MLIs is limited to a low power rating. In comparison, the modified PWM ensures that just four semiconductor components operate at f_s and i_{ch} is conducted without interruption through the quasi-resonant circuit which is switched at a low frequency and the switches operate at the zero-crossing intervals of i_{ch}.

The MLIs in [6] – [12] share the charging current and load current path. The voltage waveforms in Fig. 15 show the effect of a 1 µH charging inductor on the output voltage of the MLI in [6]. The output voltage with a charging inductor in Fig. 15(b) is



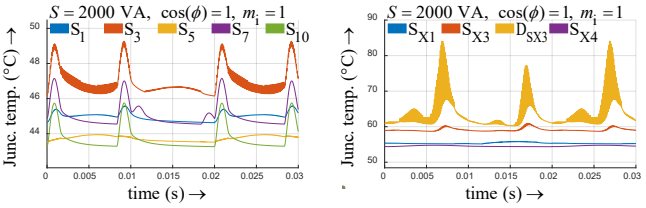
(a) (b)

Fig. 15. Waveforms of output voltage of the MLI shown in [6] **(a)** without and **(b)** with a 1 µH charging inductor.



(a) (b)

Fig. 16. Waveforms of input and capacitor current of **(a)** proposed MLI and **(b)** MLI shown in [6].



(a) (b)

Fig. 17. Junction temperature of the semiconductor devices of **(a)** proposed MLI and **(b)** MLI shown in [6].

visibly distorted from the voltage waveform without a charging inductor in Fig. 15(a) and the THD increases from 27.83% to 28.91%. Moreover, the interruption of charging current at high frequency induces high voltage transients in the associated semiconductor devices and has to be accounted for. The charging inductor should be very small and usually ranges from 10 nH to 1 µH to avoid the breakdown of semiconductor devices due to the induced high voltage transients [22]. This shows that the charging current attenuation in [6] – [12] is not as straightforward as introducing an inductor in the charging current path. In contrast, the charging inductor in the proposed MLI is placed on a path that is independent of load current. An inductor of 180 µH is used with a 2000 VA MLI to attenuate the charging current by 4.71 times without affecting the output

voltage.

The waveforms of the input current (i_{dc}) and capacitor currents (i_C) of the proposed MLI are compared in Fig. 16 to the input current (i_{DC}) and capacitor currents (i_C) of the MLI in [6]. The peak value of i_{DC} is 104 A and i_{CF} is 101 A even with a 1 µH charging inductor. In contrast, the peak value of i_{dc} is 12.6 A and i_{C3} is 20.3 A only for the same values of S, cos(ϕ), and m_i. The i_{dc} of the proposed MLI has a double line frequency harmonic component of 31.50% which significantly improves over the value of 105.4% for the MLI in [6]. The MLI in [6] will require a significantly sized input filter to interface with a battery or PV array whereas the proposed MLI may be interfaced with minimum input filter requirements.

The variation of junction temperatures of the semiconductor devices of the proposed MLI in Fig. 17(a) shows an average temperature of 44.9°C and the MLI in [6] with 1 µH charging inductor in Fig. 17(b) shows an average temperature of 58.0°C. The proposed MLI runs 13.1°C cooler and will require less cooling effort.

The power loss distribution among the semiconductor devices of the proposed MLI is shown in Fig. 18(a) and is compared to that of the MLI in [6] in Fig. 18(b) at S = 2000 VA, cos(ϕ) = 1, and m_i = 1. The switching loss of the proposed MLI is limited to just four switches and is much lower in magnitude than the MLI in [6], where the switching loss is spread across four switches and two discrete diodes and is substantially higher.

Moreover, the proposed MLI integrates active DC-link capacitor voltage balancing while maintaining the least capacitor count and a reasonable TSV_{pu}. The MLIs in [6] – [12] will need a specialized PWM [28] for balancing the DC-link capacitors.

To compare the efficiency of the proposed MLI, the recently published MLIs listed in Table II were modeled using PLECS Blockset for S = 2000 VA. The design guidelines laid out in the papers were strictly adhered to while sizing the passive components. The semiconductor components and thermal parameters are uniform throughout all the models to facilitate a fair comparison. The variation of efficiency η of the proposed MLI with output power P_o in Fig. 19 shows a significant improvement over the MLIs in comparison. This difference is attributed to the topological differences and not to the specific devices used in the simulation. The proposed MLI has the maximum simulated efficiency of 98.15% at P_o = 513.0 W.

IX. Experimental Results

A 2000 VA prototype of the proposed MLI is built using the components listed in Table I. The experimental setup in Fig. 20. shows a ET System LAB/SMS 8600 8 kW programmable DC laboratory power supply used as the DC source of voltage V_{dc} = 400 V. A 2 kW variable resistive load box and an 80 mH, 10 A inductor are used as the load.

The PWM and the dead-time generator to generate firing signals for the IGBTs are implemented on a Xilinx Spartan-6 XC6SLX9 FPGA development board. Broadcom HCPL-J312 gate drive optocouplers are used to drive the IGBTs. The

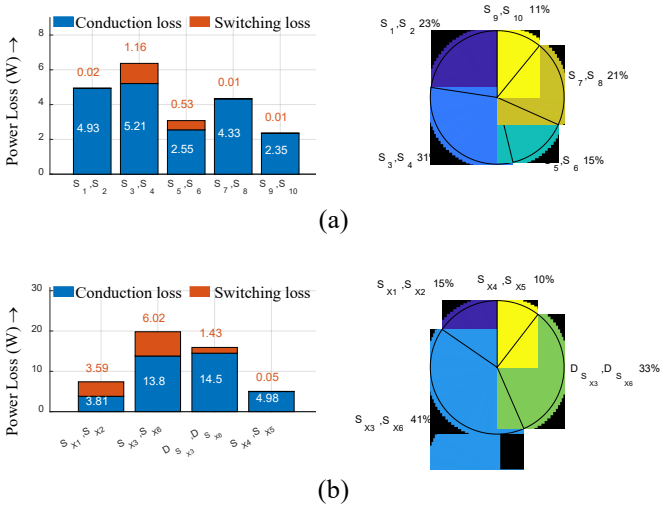


Fig. 18. Power loss distribution among the semiconductor devices of **(a)** proposed MLI and **(b)** MLI shown in [6] at S = 2000 VA, cos(ϕ) = 1, and m_i = 1.

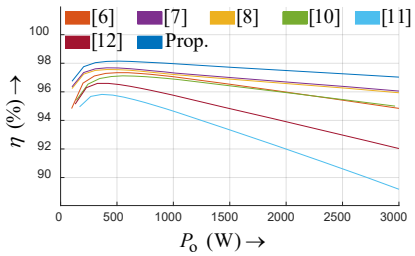


Fig. 19. Comparison of efficiency of the proposed MLI with recently published MLIs in Table II.

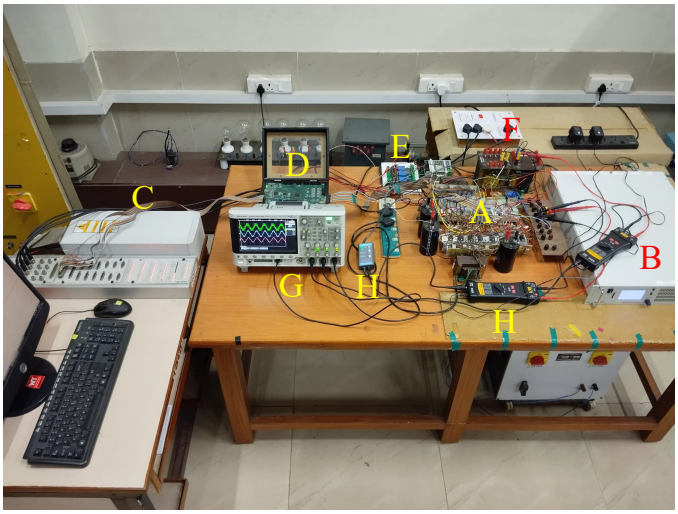


Fig. 20. Hardware-based experimental setup showing **A:** proposed MLI, **B:** power supply, **C:** dSPACE DS1103, **D:** FPGA development board, **E:** voltage and current sensors, **F:** line filter, **G:** digital storage oscilloscope, and **H:** voltage and current probes.

voltage and current waveforms are captured on a Keysight DSO-X 2024A digital storage oscilloscope.

The experimental output voltage v_o and current i_o for a resistive load of R_L = 40 Ω, fundamental frequency f = 50 Hz, switching frequency f_s = 10 kHz, and modulation index m_i = 1 are shown in Fig. 21(a). The five-level voltage of peak value 400 V and current of peak value 10 A can be distinctly seen. The experimental capacitor voltages v_C and currents i_C in Fig. 21(b) show that the capacitor voltages are at a steady-state value of 200 V. The peak-to-peak ripple of V_{C1} and V_{C2} is 18.0 V (9.00%) and the peak-to-peak ripple of V_{C3} is 20.0 V (10.0%) which are within the specified voltage ripple ΔV = 10%. The peak value of i_{C1} and i_{C2} is 12.6 A, and the peak value of i_{C3} is 20.3 A. This verifies the simulation results in Fig. 16(a).

Fig. 21(c). shows that the experimental resonant inductor voltage v_{Lr} has a peak value of 13.8 V. The inductor insulation requirements in terms of the dv/dt stress are reduced with the modified pulse-width modulation as compared to V_{dc} = 400 V. The experimental resonant inductor current i_{ch} and input current i_{dc} have peak values of 20.2 A and 12.6 A.

An 80 mH load inductor is connected in series with the load box of 40 Ω (cos(ϕ) = 0.84 lagging). The experimental waveforms in Fig. 21(d) show the five-level output voltage v_o of peak value 400 V and sinusoidal output current i_o of peak

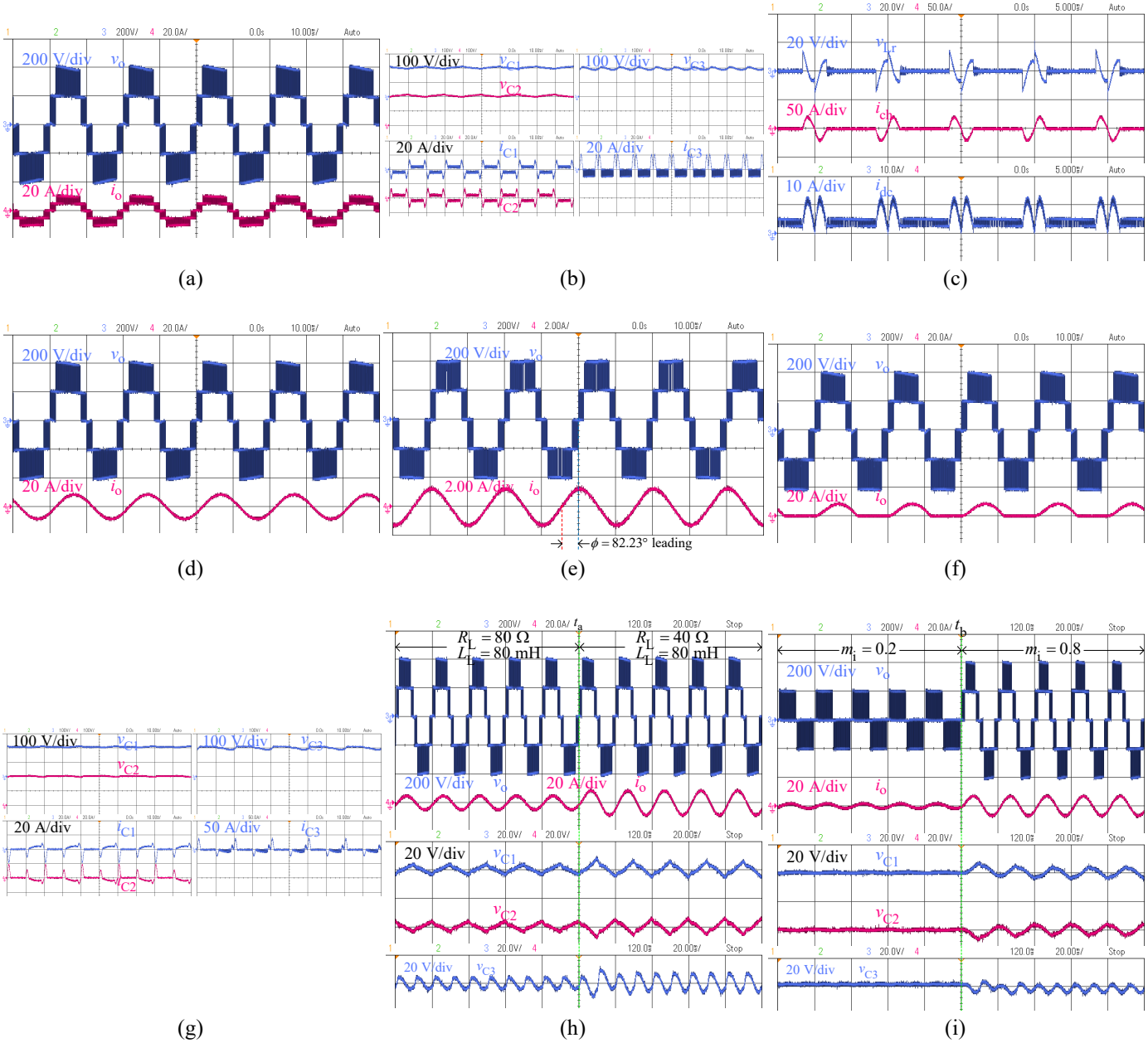


Fig. 21. Measured waveforms of **(a)** output voltage v_o and current i_o for resistive load, **(b)** capacitor voltages v_C and currents i_C for resistive load, **(c)** resonant inductor voltage v_{Lr}, current i_{ch}, and input current i_{dc}, **(d)** output voltage v_o and current i_o for lagging power factor load, **(e)** output voltage v_o and current i_o for leading power factor load, **(f)** output voltage v_o and current i_o for unbalanced load, **(g)** capacitor voltages v_C and currents i_C for unbalanced load, **(h)** output voltage v_o, current i_o, and capacitor voltages v_C for dynamic change in load impedance, **(i)** output voltage v_o, current i_o, and capacitor voltages v_C for dynamic change in modulation index.

value 8.31 A. To validate the performance of the proposed MLI with a capacitive load, a 10 μF power film capacitor is connected in series with the 80 mH load inductor and load box of 40 Ω (cos(ϕ) = 0.14 leading). The experimental waveforms in Fig. 21(e) show a five-level output voltage v_o of peak value 400 V and a sinusoidal output current i_o of peak value 1.39 A. This verifies the reactive load capability of the proposed MLI at both lagging and leading power factors.

Subsequently, a Vishay VS-60APU06-N3 diode is added in series with the load box and load inductor to present an unbalanced load to the MLI. The experimental waveforms in Fig. 21(f) show the five-level output voltage v_o and half-wave rectified sinusoidal output current i_o with an average value of 2.80 A and RMS value of 4.23 A. The experimental capacitor voltages v_C shown in Fig. 21(g) are at a steady-state value of 200 V. Compared to Fig. 21(b), the capacitor currents i_C have unequal positive and negative peak values but the values of i_C averaged over a fundamental cycle are zero. This shows an instantaneous exchange of energy between the capacitors to actively balance the neutral-point voltage but there is no net transfer of charge to or from the capacitors over a fundamental cycle and the capacitor voltages are balanced in steady-state.

The proposed MLI is subjected to a dynamic change in load impedance. The load resistance R_L is decreased from 80 Ω to 40 Ω at time t_a while operating at modulation index m_i = 1 and with load inductor L_L = 80 mH as shown in Fig. 21(h). There is no change in the number of levels and peak value of output voltage v_o. The peak value of load current i_o increases from 4.68 A to 8.35 A. The peak-to-peak capacitor voltage ripple increases at a steady-state value of 200 V. In Fig. 21(i), m_i is increased from 0.2 to 0.8 at time t_b while operating with R_L = 40 Ω and L_L = 80 mH. The number of levels of v_o increases from three levels with a peak value of 200 V to five levels with a peak value of 400 V. The peak value of i_o increases from 3.36 A to 6.72 A. The capacitor voltages are at a steady-state value of 200 V both at a m_i of 0.2 and 0.8.

It is seen that the capacitor voltages are stable under dynamic changes in load impedance and the MLI can operate over a wide range of modulation index.

The variation of measured efficiency η with output power P_o at unity power factor cos(ϕ) and modulation index m_i as an example shown Fig. 22 shows a maximum efficiency of 98.04% at P_o = 510 W. The measured efficiency at the rated power of 2015 W is 97.02% which is 0.43% less than the simulated efficiency from Fig. 19. The difference increases with P_o due to the resistive losses in the conducting wires and wire joints. The measured efficiency is among the highest at the corresponding value of output power to have been reported in the literature.

Subsequently, the *LCL* line filter with the parameters enlisted in Table I is introduced with the load box. The harmonic spectrum of filtered output voltage (v_p) in Fig. 23(b) shows the true rms value (V_p) of 278.6 V and rms value of fundamental component (V_{p1}) of 278.5 V. The total harmonic distortion of voltage v_p (THD_V) is given by (23).

$$THD_V = \sqrt{\frac{V_p^2 - V_{p1}^2}{V_{p1}^2}} \times 100 = 1.895\% \qquad (23)$$

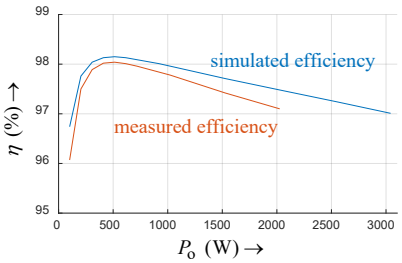
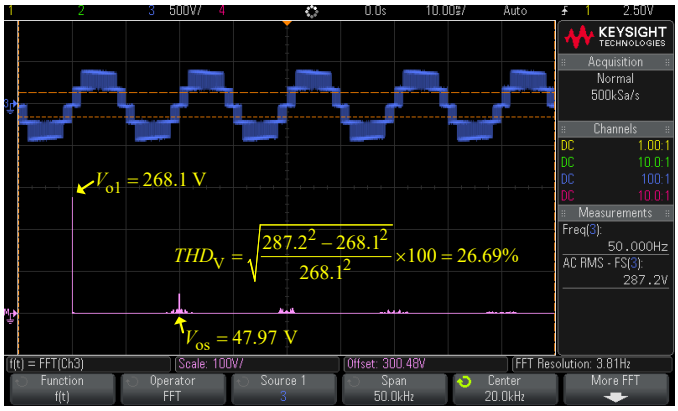
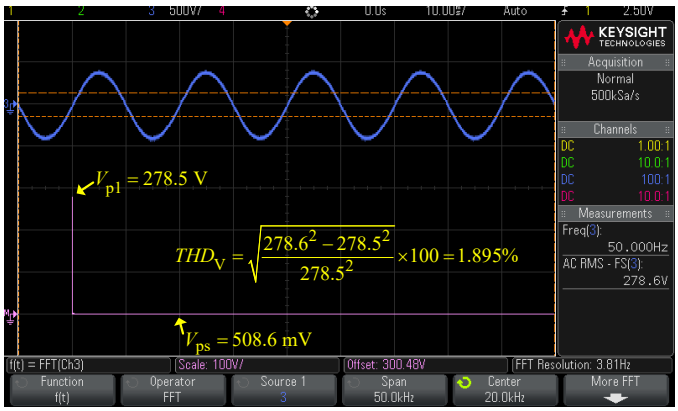


Fig. 22. Variation of measured and simulated efficiency with output power P_o.



(a)



(b)

Fig. 23. (a) Measured harmonic spectrum of inverter output voltage v_o, **(b)** measured harmonic spectrum of filtered output voltage v_p.

The measured efficiency with the *LCL* line filter is 96.93%. This reduction is attributed to the impact of the damping resistor R_d in the *LCL* filter as discussed in Section VII.

The rms value of the switching frequency harmonic component (V_{ps}) is 508.6 mV which is 0.18% of the fundamental component V_{p1} and is below 0.30% as mandated by the IEEE Std 1547™-2018 standard. This shows that the modified PWM does not affect the output voltage waveform and qualifies for the power quality standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces.

The proposed MLI is experimented with for interfacing the single-phase grid with the PV array. The PV module model is

implemented on the ET System LAB/SMS 8600 8 kW programmable DC laboratory power supply. Two 100 nF capacitors, connected on the positive and negative terminals of the power supply, are used to model the parasitic capacitance between the PV modules and the ground. The maximum power point tracking (MPPT) controller, the voltage control loop, and the current control loop are implemented on the dSPACE DS1103 PPC Controller Board. The PWM modulator and the dead-time generator to generate firing signals for the IGBTs are implemented on the Xilinx Spartan-6 XC6SLX9 FPGA development board. The PWM carrier frequency f_s is set to 10 kHz. The grid-side filter is the *LCL* configuration with the inductors split equally between the line and the neutral branches, as shown in Section V. *C*. The single-phase electrical utility in the laboratory acts as the grid. The neutral terminal of the grid is locally grounded with a 10 Ω resistor.

The power supply is programmed to simulate an initial irradiance of 1000 W/m^2 at an operating temperature of 25°C. The ANPC SC-MLI extracts a power (P_{dc}) of 1996 W from the array at a DC-link voltage v_{dc} of 434.0 V. Fig. 24 shows the 5-level stepped inverter output voltage waveform v_o of 256.9 V, filtered output voltage at the point of common coupling v_p of 238.9 V, and sinusoidal grid current i_p of 8.080 A. It is seen that the ANPC SC-MLI MLI injects power into the grid with a unity power factor.

To verify the dynamic performance, the irradiance is reduced to 250 W/m^2 at time t_c. The MPPT controller decreases the v_{dc} to 424.4 V, and the ANPC SC-MLI extracts a power P_{dc} of 489.2 W from the PV array. The variation in irradiance, v_{dc}, and P_{dc} measured from the dSPACE DS1103 are shown in Fig. 25(a). These values correspond well to the expected values in Fig. 11. The voltage and current waveforms measured at the terminals of the MLI are also shown in Fig. 25(a), and the instant of dynamic change t_c is shown in the magnified view. The 5-level stepped inverter output voltage v_o of 255.7 V, point of common coupling voltage v_p of 238.8 V, and sinusoidal grid current i_p of 1.999 A are seen in steady-state. As the irradiance is restored to 1000 W/m^2 at t_d, the voltages and currents increase to their previous steady-state values.

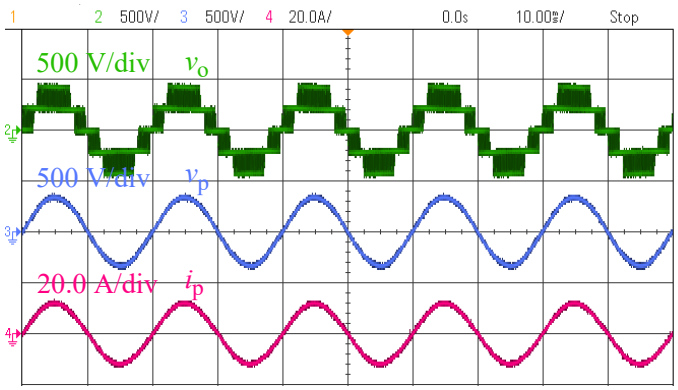
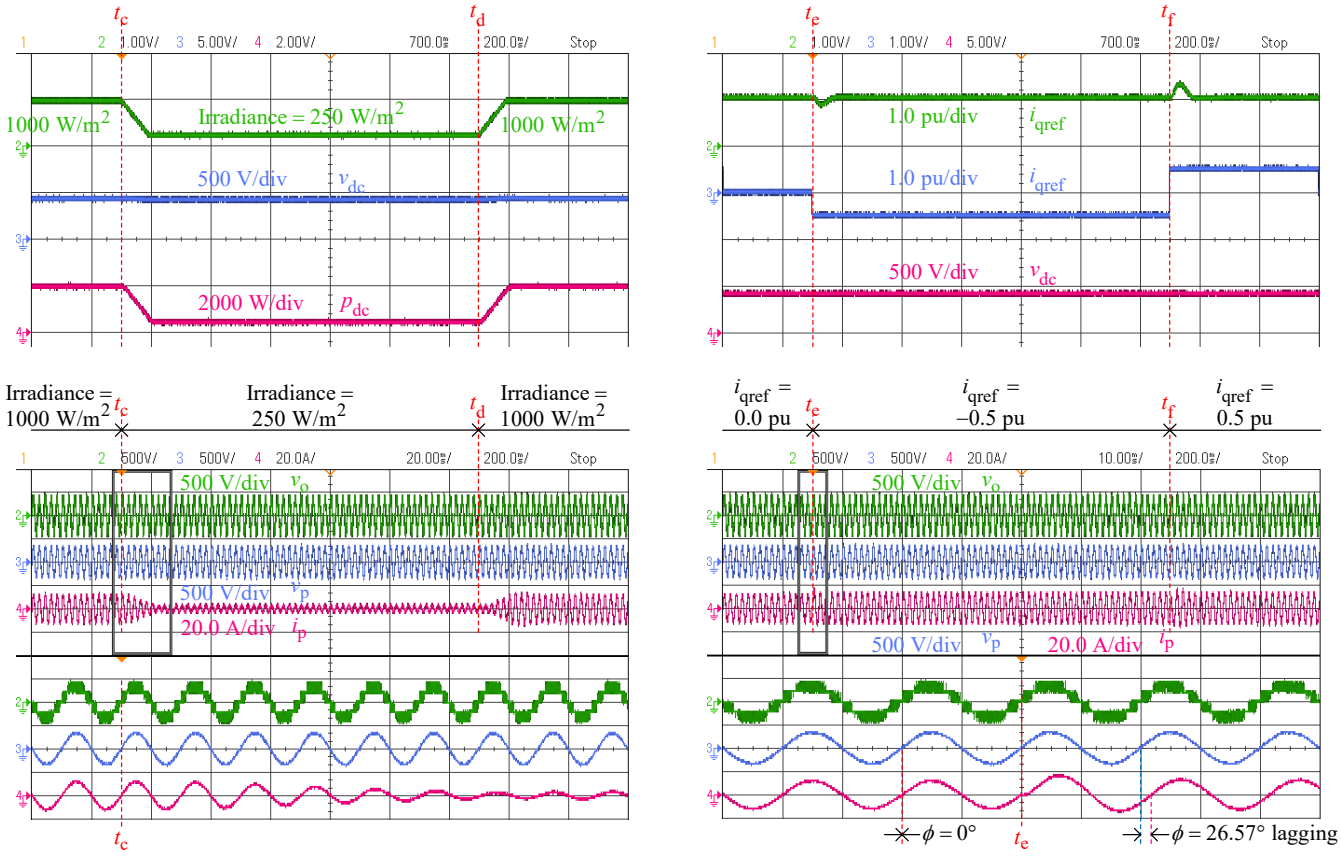


Fig. 24. Measured waveforms of inverter output voltage v_o, voltage at the point of common coupling v_p, and sinusoidal grid current i_p.



(a) (b)

Fig. 25. Measured waveforms under dynamic change in **(a)** irradiance and **(b)** *q*-axis current reference i_{qref}.

Subsequently, to verify the reactive power capability of the proposed MLI, the q-axis current reference i_{qref} is set to -0.5 pu at time t_e, as shown in Fig. 25(b) measured from the dSPACE DS1103. The magnified view of the measured inverter terminal voltage and current waveforms at the time instant in Fig. 25(b) shows that the converter acts like an alternator with an increased excitation level to provide the grid with reactive power, which in turn results in operation at a lagging power factor ($\cos(\phi)$ = 0.89 lagging). Furthermore, at t_f, i_{qref} is set to 0.5 pu, and the converter starts operating at a leading power factor ($\cos(\phi)$ = 0.89 leading) and absorbs reactive power from the grid. The waveform of v_o retains the 5-level stepped nature, and i_p is sinusoidal throughout the entire range of operation.

Fig. 26 shows a total CMV (v_{CMV}) of 217.0 V measured across the terminals n and b and a leakage current (i_{lk}) of 3.20 mA which can be mainly attributed to the noise in the measurement and complies with the industry standards. The harmonic spectrum of the grid current i_p in Fig. 27 shows a true rms value (I_p) of 8.080 A and a rms value of fundamental component (I_{p1}) of 8.078 A. The total harmonic distortion of grid current (THD_I) is given by (24).

$$THD_I = \sqrt{\frac{I_p^2 - I_{p1}^2}{I_{p1}^2}} \times 100 = 1.573\% \tag{24}$$

The rms value of the switching frequency harmonic component of grid current (I_{ps}) is 19.04 mA which is 0.23% of I_{p1} and is below 0.30% as mandated by the IEEE Std 1547™-2018 standard.

The measured efficiency at the irradiance of 1000 W/m^2 and the ANPC SC-MLI operating with a unity power factor is given by (25), which corresponds well to the efficiency with resistive load and LCL line filter with the same power rating.

$$\eta = \frac{V_p \times I_p}{P_{dc}} \times 100 = 96.71\% \tag{25}$$

Similarly, the efficiency at the irradiance of 250 W/m^2 is measured to be 97.58%.

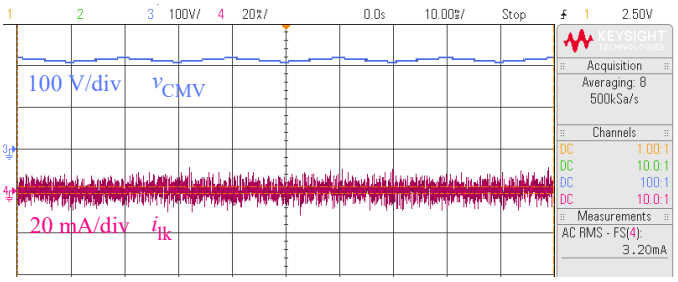


Fig. 26. Waveforms of common-mode voltage v_{CMV} and leakage current i_{lk}.

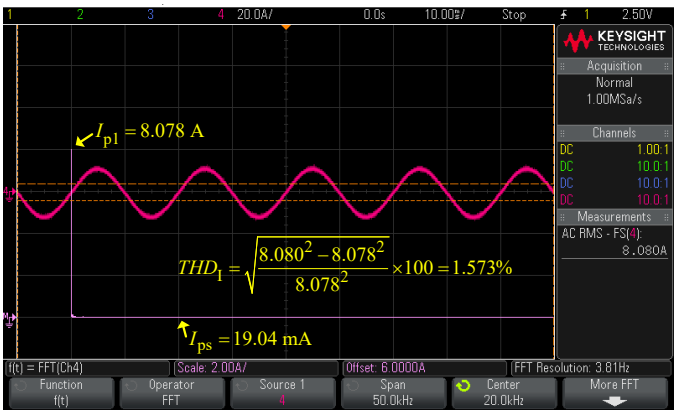


Fig. 27. Measured harmonic spectrum of grid current i_p.

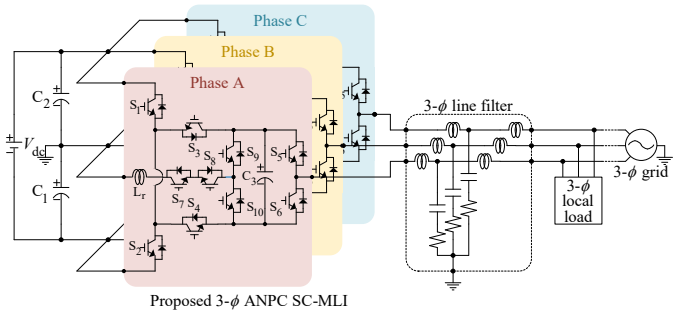


Fig. 28. Possible three-phase extension of the proposed MLI.

X. Possible Applications and Further Development

The proposed MLI does not depend on the load to draw a balanced alternating current or on injecting a zero-sequence component to balance the DC-link capacitor voltages [26], [27]. Transformerless grid-connected PV systems do not have an isolation transformer to prevent the DC injection to the grid that arises from the non-ideal characteristics of the virtual DC bus capacitor in CG MLIs or the DC-link voltage imbalance in ANPC MLIs [5], [28]. The proposed MLI is ideally suitable for transformerless grid-connected PV systems where international Standards mandate low THD and zero DC injection. By properly sizing the passive components, and controlling the modulation index, a low to medium-power system using reasonably rated semiconductors can be designed with the proposed MLI [39].

The DC-link capacitor voltage imbalance in motor drives is also a persistent problem in NPC and ANPC MLIs that have a split-capacitor front end. Several specialized PWM methods have been proposed to actively balance the capacitor voltages which would require additional voltage and current sensors, signal conditioning circuits, ADC converters, and auxiliary power supplies [24], [25]. A three-phase extension of the proposed MLI shown in Fig. 28 is readily applicable to high-performance motor drives as well. The additional voltage gain provided over the conventional MLIs [3], [4] may also be leveraged for implementing a zero-common mode voltage space vector PWM [40] that requires a higher DC-link voltage magnitude due to reduced modulation depth.

A challenging and crucial task for single-phase PV applications is active power decoupling, which is the mitigation of the double-line frequency harmonic component of the input current i_{dc} [41]. Contradictorily, the i_{dc} of SC-MLIs have an inherent pulsating nature. The i_{dc} of the proposed MLI has a double line frequency harmonic component of 31.50% at modulation index m_i = 1, which significantly improves over the value of 105.4% for the MLI in [6]. It is further reduced to 12.73% for a practical value of m_i = 0.85 for the proposed MLI and 85.15% for the MLI in [6]. Nonetheless, a minimal input

filter is still necessary to avoid the ripple in the DC-link voltage that reduces the MPPT efficiency, causes overheating of batteries, or shortens fuel cell's lifetime. Integrating active power decoupling with SC-MLIs may be considered in the future roadmap of the research.

XI. Conclusion

A unity gain five-level ANPC SC-MLI has been proposed in this paper. The MLI is capable of inrush charging current attenuation and providing a half-wave rectifier load while the DC-link capacitor and flying capacitor voltages are balanced in steady-state. The proposed MLI can operate in the entire range of modulation index. The MLI has full reactive power capability and allows bidirectional power flow. The component count and TSV are competitive as compared to the recently published MLIs. The modified pulse-width modulation minimizes the switching losses in the SC circuit and the MLI attains a maximum efficiency of 98.04% at an output power of 510 W. The proposed MLI is equally suitable for motor drives where high efficiency and four-quadrant operation are necessary as well as transformerless grid-connected PV systems where low THD and zero DC current injection are mandated by international Standards.

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