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Aniktar, Huseyin

Publication date:
2007

Document Version
Publisher's PDF, also known as Version of record

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Hüseyin Aniktar

Aalborg, 2007
PhD Thesis

Aalborg University
Department of Electronic Systems
Technology Platforms Section
Niels Jernes Vej 12, DK-9220 Aalborg, Denmark
Phone +45 96358673, Fax +45 98151583
tech-platforms@es.aau.dk
www.es.aau.dk

Acknowledgements

First and foremost, I would like to thank my advisor Torben Larsen for the guidance and inspiration. I would also like to thank Robert S. Karlsson, Henrik Sjoland, and Jan H. Mikkelsen for their great contribution to my PhD research.

I thank my colleagues in RF Integrated Systems and Circuit Division (RISC) for the help, encouragement and pleasant working environment. I would like to thank Svetoslav R. Gueorguiev, and Ole Kiel Jensen for the fruitful technical discussions. A special 'thank you' goes to the administrative and technical staff at the department, for help with paper work, computers, programs and lab assistance, specifically Peter Boie Jensen, Eva Hansen, and Rikke D. Klemmensen.

Finally this work would not be possible without the financial support from the Danish Technical Research Council.

Preface

This thesis was prepared at the Technology Platforms Section, Department of Electronic Systems, Aalborg University in partial fulfillment of the requirements for acquiring the Ph.D. degree in engineering.

The thesis covers wireless system analysis, integrated circuit design, analysis and verification in the field of RF CMOS. The thesis consists of a summary report and a collection of five research papers written during the period 2004–2007.

Multi-hop cellular networks are currently being explored for use in future generation cellular networks. In multi-hop cellular networks (MCN), communication is not established directly between the user equipment (UE) and the base station (BS). Instead, intermediate devices act as repeaters between the BS and a UE. Using multiple hops in a cellular system is one way to decrease the required transmission power for UE and possibly mitigate interference and coverage problems. Reductions in transmission power decrease the power consumption in the UE; this increases the time between battery recharges. MCNs can also provide service in 'dead spots' in a cell, which are not reachable by the BS in a single hop.

The thesis studies the overall (the whole TX+RX link) power efficiency of existing cellular networks with and without multi-hop as a function of transmit power. Based on these investigations new RF requirements have been identified in both transmitter

and receiver parts for user equipment. These requirements specifically relate to adjacent channel leakage ratio (ACLR) and power control range characteristics. These new requirements reflect to RF parts as a need for a highly linear power amplifier with a wide power control range and sharp transmit/receive filter.

Highly linear power amplifier design clearly seems a challenging issue in multi-hop cellular network systems. However, there is a critical trade off between the linearity and efficiency in power amplifier design. To improve this trade off, there are different approaches. High efficiency switching amplifier with linearization techniques and the linear class of amplification with efficiency improvement techniques are some of them. Efficient but nonlinear power amplifiers (switching amplifiers) with the use of linearizing circuits may improve this trade off, but at the price of high complexity and additional power consumption, which can be critical in the case of low or medium power amplifiers (User equipment). Therefore the thesis studies linear class of amplification with adaptive biasing technique to improve this trade off.

In addition to this critical trade off, a power amplifier design with a reasonable output power, efficiency, and linearity still remains a major challenge in CMOS technology. Standard CMOS substrate is very lossy and it will degrade the performance of the amplifier greatly. CMOS technology also has low breakdown voltage and high knee voltage features which limit the maximum voltage swing at transistor drains. This voltage swing limitations make a large impedance transformation necessary in order to deliver large powers and consequently lower efficiency.

Moreover, the inductance of the ground bondwires is also one of the most serious problems in multi-stage single-ended integrated amplifier design. Ground bounce inductance plays an important role on the amplifier stability. If all stages in a multi-stage amplifier share the same on-chip ground, they will also share the same inductance to PCB ground. Signal current in the output stage converted to voltage by this inductance will thus be fed back to the input with a risk of instability. The thesis proposes on chip ground separation technique to solve this problem.

The thesis consists of a summary report and a collection of five research papers. The summary report is organized as follows: In Chapter 1, different wireless communication standards are presented, and then standard CMOS technology and its features

are discussed. This chapter aims to give the reader some background information on the thesis's main subjects. In Chapter 2, multi-hop cellular network systems are investigated. Multi-hop functionality is analyzed in terms of power efficiency and outage performance. This chapter identifies the new RF requirements for multi-hop functionality. Chapter 3 deals with different classes of amplification, stability and matching issues. This chapter also gives the efficiency enhancing techniques in detail. Chapter 5 discusses the design details of an amplifier together with RF PCB design, interconnection elements (i.e., bondwire inductance, pad capacitances) and the other peripheral components (i.e., decoupling capacitances, choke inductances). This chapter deals with the experimental investigation on efficiency and linearity performance of amplifier with adaptive biasing technique based on GSM-EDGE standard.

The main research directions of the published five papers can be briefly expressed as follows:

NORCHIP'04 Paper [Appendix A]:
Multi-hop cellular networks are currently being explored for use in future generation cellular networks. This paper is a step towards identifying overall system requirements for the radio frequency (RF) part of terminals for such multi-hop cellular networks. Multi-hop cellular networks offer trade-offs between coverage, capacity and power consumption. Multi-hop networks are also expected to place new requirements on the RF parts of the transceivers of both repeating and mobile devices. In this paper, a set of system requirements are derived for multi-hop enabled RF front-ends. For this purpose, the uplink transmit power distributions and the uplink outage performance for multi-hop networks are investigated. According to simulation results, some RF requirements have been identified in both transmitter and receiver sections.

PIMRC'05 Paper [Appendix B]:
Cellular multi-hop networks has the potential to decrease power consumption, increase coverage and/or enable higher data rates. We propose using in-band transmissions for the connection between a fixed repeating device and the cellular base station. A user connected via the repeater use one frequency band (fq2) for the communication to the repeater and the repeater uses an adjacent frequency band (fq1) for the communication to the base station. There is strong interference in the repeater due to

transmitting and receiving on adjacent frequency bands, and strong interference from users connected directly to the base station on fq2. It is demonstrated that the method can be used to introduce multi-hop functionality into a WCDMA FDD cellular system with only small changes. In a pessimistic scenario repeated users can lower their transmit power, but others have to increase their power. The multi-hop system requires no extra frequency spectrum but it has a small capacity penalty, and it requires a high adjacent channel leakage ratio in the repeaters. The results are reasonable for this pessimistic study and suggest further studies of alternative scenarios to improve the performance.

NORCHIP'05 Paper [Appendix C]:

In this paper a single stage broadband CMOS RF power amplifier is presented. The power amplifier is fabricated in a $0.25\,\mu m$ *CMOS process. Measurements with a* $2.5\ V$ *supply voltage show an output power of* $18.5\ dBm$ *with an associated PAE of 16% at the 1-dB compression point. The measured gain is 5.1* $\pm\ 0.5\ dB$ *from 1.65 to* $2\ GHz$*. Simulated and measured results agree reasonably well.*

With 2.5V supply voltage, 18.5dBm output power with 16% PAE, a broad frequency band and a high linearity were measured. An amplifier with these performance characteristics might be suitable for use in multimode radio terminal applications.

EuMW'06 Paper [Appendix D]:

In the future GSM and other parallel 2G systems are likely to be replaced with 3G and beyond, that is the bands that today are used for GSM will then be used for WCDMA and other standards. WCDMA in the 900 MHz band is a cost effective way to deliver a high-speed wireless coverage. This work demonstrates a $850/900/1800/1900$ *MHz quad-band WCDMA power amplifier.*

The power amplifier is designed as a two-stage common source Class-AB amplifier. The amplifier is fabricated in a $0.25\ \mu m$ *CMOS process. The measured 1-dB compression point between* 800 *and* 900 *MHz is* $15\ dBm \pm 0.2\ dB$ *with maximum 18% PAE, and between* 1800 *and* 1900 *MHz is* $17.5\ dBm \pm 0.7\ dB$ *with maximum 17% PAE. The measured gains in the two bands are* $23.6\ dB \pm 0.7\ dB$ *and* $13\ dB \pm 2.1\ dB$*, respectively.*

The quad-band characteristics was obtained with a single CMOS power amplifier while getting medium output power, and reasonable efficiency and linearity. The chip size

is $1280\,\mu m \times 420\,\mu m$.

SiRF'07 Paper [Appendix E]:
This work presents an on-chip ground separation technique for power amplifiers. The ground separation technique is based on separating the grounds of the amplifier stages on the chip and thus any parasitic feedback paths are removed. Simulation and experimental results show that the technique makes the amplifier less sensitive to bondwire inductance, and consequently improves the stability and performance.
A two-stage CMOS RF power amplifier for WCDMA mobile phones is designed using the proposed on-chip ground separation technique. The power amplifier is fabricated in a $0.25\,\mu m$ *CMOS process. It has a measured 1-dB compression point between* 1920 *MHz and* 1980 *MHz of* 21.3 ± 0.5 *dBm with a maximum PAE of* 24%. *The amplifier has sufficiently low ACLR for WCDMA (*-33 *dB) at an output power of* 20 *dBm.*

Aalborg, February 2007

Hüseyin Aniktar

Papers included in the thesis

[A] Robert S. Karlsson, Hüseyin Aniktar, Torben Larsen, and Jan H. Mikkelsen, "RF Requirements for Multi-Hop Cellular Network Repeaters", *IEEE Norchip Conference*, Oslo, Norway, November 2004.

[B] Robert S. Karlsson, Hüseyin Aniktar, Jan H. Mikkelsen, and Torben Larsen, "Performance of a WCDMA FDD Cellular Multihop Network", *IEEE International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC)*, Berlin, Germany, September, 2005.

[C] Hüseyin Aniktar, Henrik Sjöland, Jan H. Mikkelsen, and Torben Larsen, "A Class-AB 1.65GHz-2GHz Broadband CMOS Medium Power Amplifier", *IEEE Norchip Conference*, Oulu, Finland, November 2005.

[D] Hüseyin Aniktar, Henrik Sjöland, Jan H. Mikkelsen, and Torben Larsen, "A 850/900/1800/1900MHz Quad-Band CMOS Medium Power Amplifier", *European Microwave Week (EuMW)*, Manchester, England, September 2006.

[E] Hüseyin Aniktar, Henrik Sjöland, Jan H. Mikkelsen, and Torben Larsen, "A CMOS Power Amplifier using Ground Separation Technique", *7th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (IEEE SiRF'07)*, California, USA, January 2007.

Scientific achievements

1. In this work it is shown that the multi-hop achieves lower transmit powers for user equipments by splitting the transmission into several hops. The thesis studies the overall (the whole TX+RX link) power efficiency of existing cellular networks with and without multi-hop as a function of transmit power. Based on these investigations new RF requirements have been identified in both transmitter and receiver parts for user equipment. These requirements specifically relate to adjacent channel leakage ratio and power control range characteristics. These new requirements reflect to RF parts as a need for a highly linear power amplifier with a wide power control range and sharp transmit/receive filter.

2. A power amplifier design with a reasonable output power, efficiency, and linearity still remains a major challenge in CMOS technology. The main obstacles in CMOS technology are the low breakdown voltages and the large parasitics associated with the lossy substrate. These obstacles degrade the performance of the amplifier greatly. During the project several CMOS Class-AB amplifier has been designed and reported. Their power added efficiencies are measured from about 17% to 28% at 1-dB compression points. Different power levels have been obtained at the amplifier outputs. Maximum measured output power level is 21.8dBm. Besides the efficiency and output power characteristics, good linearity performances have been also measured with these amplifiers.

3. In this work an on-chip ground separation technique has been proposed for

multi-stage single-ended amplifiers. The ground separation technique is based on separating the grounds of the amplifier stages on the chip and thus any parasitic feedback paths are removed. Simulation and experimental results show that the technique makes the amplifier less sensitive to bondwire inductance, and consequently improves the stability and performance.

4. This work also demonstrates that the power amplifier efficiency can be improved at mid-power ranges by dynamically biasing the amplifier with slightly reduction on the PAE at 1-dB compression point. In linear power amplifiers, the quiescent bias of the amplifier is set for maximum linear power and DC power is wasted at lower output power levels. The adaptive biasing method is based on adaptation the supply voltage to the envelope of the signal. In this way, it is expected improvement on the efficiency of the power amplifier while maintaining the required high degree of linearity.

5. Multi-mode radio terminals are needed more and more as the number of radio systems on the market increases. Realization of multi-band, multi-mode radio terminals requires technical progress in several areas. Design of broadband multi-mode power amplifiers is one of them. In this work both broadband and quad-band amplifier characteristics have been obtained by properly designing the matching networks. The matching networks are designed to give the best input and output VSWR characteristic over a wide frequency range by using passive network synthesis techniques.

Contents

List of Abbreviations

$2G$	Second Generation
$3G$	Third Generation
$3GPP$	3rd Generation Partnership Project
$ACLR$	Adjacent Channel Leakage Ratio
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
BS	Base Station
CDF	Cumulative Distribution Function
$CMOS$	Complementary Metaloxidesemiconductor
$CWTS$	China Wireless Telecommunication Standards group
DL	Downlink
$ECSD$	Enhanced Circuit-Switched Data
EER	Envelope Elimination and Restoration
$EGPRS$	Enhanced GPRS
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
FDD	Frequency Division Duplex
$GPRS$	General Packet Radio Service
GSM	Global System for Mobile communication
HBT	Heterojunction Bipolar Transistor

$HEMT$	High Electron Mobility Transistor
$HSCSD$	High Speed Circuit-Switched Data
ISM	Industrial, Scientific and Medical
LOS	Line-of-Sight
MCL	Minimum Coupling Loss
MCN	Multi-hop Cellular Networks
$MMIC$	Monolithic Microwave Integrated Circuit
$NADC$	North American Digital Cellular
$ODMA$	Opportunity Driven Multiple Access
$OQPSK$	Offset Quadrature Phase-Shift Keying
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PWM	Pulse Width Modulator
Q	Quality Factor
RF	Radio Frequency
$RFIC$	RF Integrated Circuit
RRC	Root Raised Cosine
RX	Receiver
SIR	Signal-to-Interference Ratio
TDD	Time Division Duplex
TX	Transmitter
UE	User Equipment
UL	Uplink
$UMTS$	Universal Mobile Telephone System
$UTRA$	Universal Terrestrial Radio Access
$VLSI$	Very Large Scale Integration
$VSWR$	Voltage Standing Wave Ratio
$WCDMA$	Wideband Code Division Multiple Access

Chapter 1

Introduction

Radio frequency integrated circuits in CMOS are developing a strong presence in the commercial world by springing out of university research. The evolution of wireless technologies together with technological advancements for CMOS technologies, has resulted in increased research and development activities in so-called Radio Frequency CMOS circuits. Most important for this development is the drive for highly integrated, low cost mobile handsets, i.e., both the RF, analog and digital part of a transceiver can be implemented on a single chip with CMOS technology.

This chapter deals with different wireless communication standards and their evolutions. Specifically, UMTS (UTRA-FDD and UTRA-TDD) and GSM-EDGE standards and their specifications are studied in detail in this chapter. In this work UTRA-FDD standard has been used to analyze the multi-hop functionality. For this, multi-hop cellular network system has been introduced into a UTRA-FDD cellular system with small changes. This is explained in Chapter 2 in detail.

In this study, both UMTS and GSM-EDGE standards are taken as reference for

power amplifier designs. CMOS technology parameters which are required for amplifier design and fabrication are also given in this chapter. Since technology parameters are given in detail, the technology provider name is not given because of confidentiality. CMOS power amplifier designs for UMTS and GSM-EDGE standards are explained in Chapters 3, 4 and publications.

1.1 Wireless Communication Systems

Second generation mobile radio systems have shown great success in providing wireless service worldwide with the use of digital technology, in contrast to the analog first generation systems [47]. The most important second generation systems are global system for mobile communication (GSM), North American Digital cellular NADC (IS-54, IS-136) and personal digital cellular in Japan.

GSM was initially introduced as a pan-European system. Since its commercial introduction in the early 1990s, GSM has been constantly upgraded, as evidenced by the introduction of High Speed Circuit-Switched Data (HSCSD), GPRS, EDGE, Enhanced Circuit-Switched Data (ECSD) and Enhanced GPRS (EGPRS) [46]. The introduction of the third generation UMTS, based on WCDMA technology, is a further step towards satisfying the ever increasing demand for data/internet services. 3G is quickly moving on to 3.5G, 3.9G, and 4G and is changing the way the world communicates.

Multiple wide area and local area wireless systems are deployed in various places around the world, many of which are outlined in Table 1.1. These mobile systems include cellular (e.g., GSM/GPRS, EDGE, WCDMA, 1xRTT, 1xEV/DO), local area networks (e.g., IEEE 802.11-b, -a, and -g (Wi-Fi), IEEE 802.16 (WiMAX)), personal area networks (e.g., Bluetooth, Zigbee), and specialized networks (e.g., TETRA, iDEN) [46]. Characteristics of these systems span a broad combination of constant-envelope and varying-envelope signals, time-division (half duplex) and code-division (full duplex) multiplexing, and high (several watts) to very low (microwatts) transmitter output powers.

Table 1.1: Some key parameters of various wireless communication standards [46].

System	Frequency (MHz)	Modulation	Max. Average Antenna Power (dBm)	Spectral Quality (dB)
GSM-850	UL: 824-849 DL: 869-894	GMSK	33	−60 @400 kHz
GSM-900	UL: 890-915 DL: 935-960	GMSK	33	−60 @400 kHz
GSM-1800 (DCS)	UL: 1710-1785 DL: 1805-1880	GMSK	30	−60 @400 kHz
GSM-1900 (PCS)	UL: 1850-1910 DL: 1930-1990	GMSK	30	−60 @400 kHz
WCDMA (FDD)	UE: 1920-1980 BS: 2110-2170	UL: HPSK DL: QPSK	24	−33 @5 MHz
TD-SCDMA	UE: 1900-1920 BS: 2010-2015	QPSK	24	−33 @1.6 MHz
TETRA		$\pi/4$-DQPSK	36	−60 @25 kHz
Bluetooth	ISM Band: 2400-2483.5	GFSK	20	−20 @500 kHz
IEEE802.11b	ISM Band: 2400-2483.5	DQPSK	20	−30 @11 MHz
IEEE802.11a	5150-5350 5725-5825	OFDM	20	−20 @20 MHz

All of these wireless systems consist of a radio frequency or microwave front-end. These front-end blocks require some system specifications such as bit error rate, minimum detectable signal (sensitivity), blocking and interference performance, channel bandwidth, modulation scheme, output power range, frequency bands, etc. For each system the value of these requirements may differ.

1.1.1 UMTS

Universal mobile telecommunications system (UMTS) is generally referred to as the third generation mobile phone system, set out to replace existing digital systems in the world today (GSM, D-AMPS, PDC, etc.). It is one of the most important

third generation mobile communication systems being developed within the IMT-2000 frame work [36, 5].

The first generation mobile communications systems were all based on analog communications using frequency division multiple access. These systems, of which most were based on regional standards, are all characterized by the low spectral efficiency, low security, and limited quality. The second generation mobile phones introduced digital communication in form of time division multiple access except for cdmaOne which uses direct sequence code division multiple access (DS-CDMA). Second generation mobile communications offered good security, quality, and roaming.

The third generation mobile telecommunication standard UMTS uses a combination of TDMA and CDMA technology. UMTS aims to provide a broadband, packet-based service for transmitting video, text, digitized voice, and multimedia at data rates of up to 2 megabits per second while remaining cost effective [36].

UMTS comprises two air interfaces. One of these interfaces utilizes CDMA combined with frequency division duplex (UTRA-FDD). The other uses CDMA/TDMA and time division duplex to achieve two way communication (UTRA-TDD) [36]. UTRA-FDD is based on a harmonized version of WCDMA technology. UTRA-TDD is likely to experience further harmonization related to the TD-SCDMA standard proposed by the Chinese standards body CWTS.

The spectrum allocation for UTRA-TDD is split into two bands: 1900-1920 MHz for uplink and 2010-2025 MHz for downlink. The UTRA-FDD uplink frequency band is between 1920-1980 MHz and the UTRA-FDD downlink uses the frequency band in the range of 2110-2170 MHz [13].

UTRA-FDD UE Transmitter Specifications:

In this section UTRA-FDD UE transmitter specifications are given briefly [13]. In specifications, transmitter characteristics are specified at the antenna connector of the UE. There will likely be some devices between the PA output and the antenna terminals such as circulator, duplex filter, and switch(es) with several dB of loss.

A. UTRA-FDD UE Transmit Power: The power classes in Table 1.2 define the maximum average output power of UE [13].

Table 1.2: UE output power levels.

Power Class	Average output power	Tolerance
1	+33 dBm	$+1/-3$ dB
2	+27 dBm	$+1/-3$ dB
3	+24 dBm	$+1/-3$ dB
4	+21 dBm	± 2 dB

B. Adjacent Channel Leakage Power Ratio: Adjacent Channel Leakage power Ratio is the ratio of the root raised cosine filtered mean power centered on the assigned channel frequency to the RRC filtered mean power centered on an adjacent channel frequency [13]. If the adjacent channel power is greater than -50dBm then the ACLR shall be higher than the value specified in Table 1.3 [13].

Table 1.3: UE ACLR [13].

Power Class	Adjacent channel frequency relative to assigned channel frequency	ACLR limit
3	+5 MHz or -5 MHz	33 dB
3	+10 MHz or -10 MHz	43 dB
4	+5 MHz or -5 MHz	33 dB
4	+10 MHz or -10 MHz	43 dB

C. Error Vector Magnitude: The Error Vector Magnitude is a measure of the difference between the reference waveform and the measured waveform. This difference is called the error vector. Both waveforms pass through a matched RRC filter with bandwidth 3.84 MHz and roll-off $\alpha = 0.22$ [13]. Both waveforms are then further modified by selecting the frequency, absolute phase, absolute amplitude and chip clock timing so as to minimize the error vector. The EVM value shall not exceed 17.5% in RMS [13].

UTRA-TDD UE Transmitter Specifications:

The UTRA-TDD mode includes two different transmission modes in the physical layer: TDD high chip rate with 3.84 Mcps and TDD low chip rate with 1.28 Mcps. TDD high chip rate mode is known as TD-CDMA and TDD low chip rate is known as TD-SCDMA. TD-SCDMA was proposed by China Wireless Telecommunication Standards group (CWTS) and approved by the ITU in 1999. UTRA-TDD UE transmitter specifications are given below briefly [15].

A. UTRA-TDD UE Transmit Power: The power classes in Table 1.4 define the maximum average output power of UE [15].

Table 1.4: UE output power levels [15].

Power Class	Average output power	Tolerance
1	+30 dBm	$+1/-3$ dB
2	+24 dBm	$+1/-3$ dB
3	+21 dBm	$+2/-2$ dB
4	+10 dBm	± 4 dB

B. ACLR and EVM requirements: The ACLR performance for UE is listed in Table 1.5. The error vector magnitude value for UE shall not exceed 17.5% both in RMS and peak [15].

Table 1.5: UE ACLR [15].

Power Class	Adjacent channel frequency relative to assigned channel frequency	ACLR limit
2, 3	+1.6 MHz or -1.6 MHz	33 dB
2, 3	+3.2 MHz or -3.2 MHz	43 dB

1.1.2 GSM-EDGE

EDGE (Enhanced Data rates for GSM Evolution) technology is an upgrade to the GSM standard, providing higher data rates in the same frequency spectrum by using higher density modulation. EDGE promises to allow service providers to deliver

theoretical data rates up to 384 kilobits/sec, and enable wireless services such as multimedia and other broadband applications [4].

The EDGE and GSM signal spectrums are nearly identical with the primary difference being that the EDGE signal has deeper nulls at the edges of the main lobe [4]. GSM is a constant envelope modulation - that is, carrier power does not vary with modulation. The EDGE signal has the same spectral characteristics as GSM, as well as the same symbol rate and frame structure. To achieve higher data rates, the EDGE signal makes use of both amplitude and phase modulation [4]. The addition of amplitude modulation translates into more stringent requirements for the power amplifier than GSM, as well as a different approach for measuring modulation quality and power. In Table 1.6, a brief comparison between the EDGE and GSM standards is given.

Table 1.6: GSM and EDGE comparison [4].

	GSM	EDGE
Modulation	GMSK	$3\pi/8$ rotated 8PSK
Bits/symbol	1	3
Data bits per burst	114	342
Symbol rate	270.833 kHz	270.833 kHz
Pulse shaping filter	0.3 Gaussian	Linearized Gaussian

There are eight frequency bands defined for GSM; GSM 450 band, GSM 480 band, GSM 850 band, standard or primary GSM 900 band (P-GSM), extended GSM 900 band (E-GSM), railways GSM 900 band (R-GSM), DCS 1800 band, and PCS 1900 band. Each of them has a spectrum allocation and it is split into two bands for uplink and downlink. The spectrum allocation for DCS 1800 is 1710-1785 MHz for uplink and 1805-1880 MHz for downlink [3].

In Tables 1.7 and 1.8 the UE maximum average output power levels and tolerances are given according to 8-PSK modulation.
The maximum average output power for 8-PSK in any one band is always equal to or less than GMSK maximum average output power for the same equipment in the same band [3]. For instance, 33 dBm maximum average output power for GSM corre-

Table 1.7: Maximum average output power for EDGE UE [3].

Power class	GSM 400, GSM 900 and GSM 850 bands Max. average output power	GSM 400, GSM 900 and GSM 850 bands Tolerance (dB)
E1	33 dBm	±2 (normal), ±2.5 (max)
E2	27 dBm	±3 (normal), ±4 (max)
E3	23 dBm	±3 (normal), ±4 (max)

Table 1.8: Maximum average output power for EDGE UE [3].

Power class	DCS 1800 band Max. average output power	PCS 1900 band Max. average output power	DCS 1800, PCS 1900 Tolerance (dB)
E1	30 dBm	30 dBm	±2 (normal), ±2.5 (max)
E2	26 dBm	26 dBm	-4/+3 (normal), -4.5/+4 (max)
E3	22 dBm	22 dBm	±3 (normal), ±4 (max)

sponds to 27 dBm maximum average output power for EDGE which is power class-E2.

The modulation accuracy requirement for 8-PSK modulation is defined according to RMS and peak EVM values, and also the 95:th percentile requirement. The measured RMS EVM over the useful part of any burst, excluding tail bits, shall not exceed 9% for the user equipment [3]. The measured peak EVM values shall also be less than 30% for the user equipment [3]. The 95:th percentile is the point where 95% of the individual EVM values, measured at each symbol interval, is below that point. That is, only 5% of the symbols are allowed to have an EVM exceeding the 95:th-percentile point [3].

The required spectral quality for EDGE standard is -54 dB at 400 kHz offset and maximum power for GSM 400, GSM 850, GSM 900, DCS 1800, and PCS 1900 bands [3].

1.2 CMOS Technology

In order to provide signal gain, an amplifier must contain at least one active device. In this work complementary metaloxidesemiconductor (CMOS) transistors are used as active devices. The CMOS technology, throughout the years, has increasingly widened in the field of analog and RF integrated circuits by providing low cost and high performance solutions [18]. The low cost of fabrication and the possibility of placing both analog/RF and digital circuits on the same chip make CMOS technology more attractive. Over the years, the intrinsic speed of MOS transistors has been increased by scaling down the channel length. This makes possible multi gigahertz analog circuits [55]. The main obstacles in CMOS technology are the low breakdown voltages and the large parasitics associated with the lossy substrate.

In this work 0.25μm 2.5V single poly five metal (1P5M) RF CMOS process is used for fabrication. Some parameters of this process are discussed in this chapter. Some limitations, advantages, and disadvantages of CMOS technology are also discussed and compared to other technologies in this chapter.

In order to represent the behavior of N/P MOSFET transistors in circuit simulations, SPICE requires an accurate model for each device. There are a number of simulation models for MOS transistors, but only some of them are suitable for RF circuits. These models are BSIM3v3, BSIM4, MOS9, MOS11, and EKV [63, 62]. The BSIM3v3 model is the most widely used model for analog circuits and in this work as well.

1.2.1 I-V Characteristics

The MOS transistor is usually modeled with four terminals: gate, bulk, drain and source. The transistor can be made symmetric, so that there is no physical difference between the drain and the source. For both symmetric and non-symmetric transistors, it depends on the driving conditions which terminal is called drain and which is called source [60].

There are two types (polarities) of MOS transistors, n-channel and p-channel. The N device conducts when the gate-source voltage is more positive than the threshold voltage V_{Tn}, which is dependent on parameters such as doping concentrations, oxide thickness, gate material, surface charge density, and source/substrate bias [22]. The P device conducts when the gate-source voltage is more negative than the threshold voltage V_{Tp}. The source has higher potential than the drain [60].

The relationship between the drain current of a MOSFET and its terminal voltages is simple for long channels, but it is very complicated for short channels. The relation for n-channel MOSFET can be briefly given as follows [22]. The p-channel MOSFET shows similar behavior. In the equations, drain current is denoted by I_d, drain-source, gate-source, and threshold voltages are denoted by V_{DS}, V_{GS}, V_T, respectively. All are the large signal parameters.

- Cutoff region: $I_D = 0$ (ignoring sub-threshold current), $V_{GS} - V_{Tn} < 0$
- Triode (or ohmic) region: $V_{GS} - V_{Tn} \geq 0$, and $V_{DS} \leq V_{GS} - V_{Tn}$

$$I_D = K_p \cdot (\frac{W}{L}) \cdot [(V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{V_{DS}^2}{2}] = \beta \cdot [(V_{GS} - V_{Tn}) \cdot V_{DS} - \frac{V_{DS}^2}{2}] \quad (1.1)$$

- Saturation region: $V_{GS} - V_{Tn} \geq 0$, and $V_{DS} \geq V_{GS} - V_{Tn}$,
  If ignoring channel modulation effect:

$$I_D = \frac{1}{2} \cdot K_p \cdot (\frac{W}{L}) \cdot (V_{GS} - V_{Tn})^2 = \frac{1}{2} \cdot \beta \cdot (V_{GS} - V_{Tn})^2 \quad (1.2)$$

  With channel modulation effect:

$$I_D = \frac{1}{2} \cdot \beta \cdot (V_{GS} - V_{Tn})^2 \cdot (1 + \lambda_c \cdot (V_{DS} - V_{DSsat})) \quad (1.3)$$

where $\beta = K_p \cdot \frac{W}{L}$ and $K_P = \mu_n \cdot C_{OX} = \mu_n \cdot \frac{\varepsilon_{OX}}{t_{OX}}$.

In equations, λ_c is the channel length modulation coefficient and its typical values range from greater than 0.1 for short channel devices to 0.01 for long channel devices [22]. t_{OX} is the gate oxide thickness, C_{OX} is the oxide capacitance, μ_n is the

mobility of electrons, and the ε_{OX} is the dielectric constant of the gate oxide. W and L shows the transistor width and length, respectively [55, 22, 63]. Triode region is the amplification region for power amplifiers.

In 0.25μm 2.5V 1P5M CMOS technology, the typical threshold voltage (V_{Tn}) for NMOS transistor ($W/L = 10/0.24$) is 0.54 V and the typical threshold voltage (V_{Tp}) for PMOS transistor ($W/L = 10/0.24$) is -0.58 V. The typical drain current density for the same NMOS transistor is 630μA/μm and the typical drain current density for the same PMOS transistor is -280μA/μm. These values can be extended to any size of the transistors.

Besides the current density limitation of MOSFET, metal layers and vias have also limitations for the maximum current density. The 0.25μm 2.5V 1P5M CMOS technology has five metal layers and each of them has different maximum current density. The maximum current density of the Metal 1, Metal 2, Metal 3, and Metal 4 layers is 0.8 mA/μm and it is 1.5 mA/μm for Metal 5 layer. The maximum current density for vias is 1 mA/via. This means that if the output transistor draws about 150 mA through the choke from the supply, the required inductance trace thickness is at least 100μm on Metal 5 layer. This size inductance is huge for integration, that is why the chokes are generally off-chip components.

1.2.2 Gate-Oxide Breakdown Effect

The low breakdown voltage in a modern CMOS technology poses a major limitation in PA realization. The oxide breakdown occurs when a large voltage is applied over the gate oxide of a MOSFET. The effect on the transistor is a permanent short circuit through the insulator [22]. Since RF devices are usually quite large, and are fingered, different fingers of the device may go through breakdown at different times. Thus even a single gate-oxide breakdown can be fatal to the functioning of an RF circuit. The oxide breakdown can be caused by static charge, which means that ESD protective circuits should be used if an input is connected directly to the gate of a MOSFET.

In the 0.25μm CMOS process, the estimated gate oxide breakdown voltage is approx-

imately 5 V under 2.5 V supply voltage and 50 $\AA$ oxide thickness. Having a lower breakdown voltage means that the maximum voltage swing on the drain terminal is also limited and this limitation requires a lower load impedance at the output terminal to deliver more power. A lower load impedance makes necessary large impedance transformation and consequently more power loss over the impedance transformation network.

Breakdown voltage levels for different semiconductor technologies can be approximately given as follow: GaAs MESFET - from 16 to 20 Volts breakdown is possible. GaAs PHEMT - 12 Volts breakdown is the best and 5 - 6 Volts is typical [17]. GaAs MHEMT - the breakdown voltage is much lower than PHEMT. SiGe HBT - the breakdown voltage is as bad as 1.5 Volts. InP HEMT has also low breakdown voltage. GaN - the breakdown voltage can reach up to 100 Volts. LDMOS - high breakdown voltage is one of its most important advantages [17]. For a given output impedance the power output is the square of voltage swing, therefore it is possible to get over 7 dB more power going from 12 to 28 Vdd [17].

As CMOS technology continues to scale down, allowing operation in the gigahertz region, it provides the more opportunities for RF implementations. On the other hand, decreasing device length in CMOS technologies results in a lower breakdown voltage because the oxide thickness is decreasing as well. At present, GaAs and BiCMOS technologies constitute the major section of the RF market, especially in power amplifiers and switches. While GaAs processes offer useful features such as higher breakdown voltage, semi-insulating substrate, and high quality inductors and capacitors, CMOS process can potentially provide both higher levels of integration and lower overall cost [54]. So there is no single technology meets all market requirements.

1.2.3 Knee Effect

The knee voltage is the drain-source voltage at which the MOSFET starts to operate as an amplifier [22]. Assuming the PA consists of one single MOSFET, the knee voltage is the same for the PA as for the MOSFET. If a cascade stage is used the PA knee

voltage will be increased. Traditionally the knee voltage is taken to be the voltage where the PA has reached 90% of its drain current in a typical I-V characteristic.

One of the consequences of the knee voltage (V_{knee}) is a reduction of the maximum voltage swing at the drain, from $2V_{DD}$ to $2(V_{DD} - V_{knee})$. This has a negative impact on the efficiency.

1.2.4 Substrate Effect

The low-resistivity substrate that is used in standard CMOS processing has limited the integration of high-quality passive components. At high frequencies the current flows through C_{ox} and into the lossy substrate [55, 63, 62]. The resulting dissipation adds a real component to the imaginary impedance and degrades the quality factor (Q). As the frequency increases to where the skin depth is on the order of the substrate thickness, eddy currents in the substrate become a major loss mechanism [55, 63, 62].

The use of high-resistivity substrates has been proposed as a solution for suppressing substrate noise and for increasing the quality factor. In the 0.25μm CMOS process, the substrate resistivity is $20\Omega - cm$, the substrate thickness is 29 Mils, and the relative dielectric constant (ε_r) is 4.1. For the other technologies these features can be approximately given as follow: GaAs MESFET - it has a high bulk resistivity and the dielectric constant is 12.9 [17]. InP HEMT - the dielectric constant is 12.4. LDMOS - it utilizes epitaxial silicon, low-doped P-type layers grown on low-resistivity (i.e. highly doped) silicon wafers [17]. Since the epitaxial layer is used to ground the source to the substrate, each source is comfortably grounded to the baseplate.

To have a high dielectric constant and thick substrate gives an opportunity to implement the transmission lines on chip. The approximate relation between the substrate thickness, relative dielectric constant and the microstrip line width can be given as

follows:

$$\frac{W}{d} = \begin{cases} \frac{8 \cdot e^{A}}{e^{2A}-2}, & \text{for } W/d < 2 \\ \frac{2}{\pi}[B - 1 - \ln(2B-1) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\ln(B-1) + 0.39 - \frac{0.61}{\varepsilon_r}], & \text{for } W/d > 2 \end{cases} \tag{1.4}$$

where

$$A = \frac{Z_o}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}(0.23 + \frac{0.11}{\varepsilon_r}) \tag{1.5}$$

$$B = \frac{377\pi}{2Z_o\sqrt{\varepsilon_r}} \tag{1.6}$$

where d is the substrate thickness, ε_r is the relative dielectric constant, Z_o is the characteristic impedance, and the W is the microstrip line width [50]. W and d are in the same units.

From Equation 1.4, it is found that the microstrip line width is approximately proportional to $1/\sqrt{\varepsilon_r}$ and d, and the use of a thick substrate with a larger permittivity thus can result in a smaller microstrip line.

The utilization of CMOS technology for RF applications is becoming more and more established. It is made possible mainly by the channel length decreasing to submicron sizes, providing an opportunity to increase the cut-off frequency f_T and maximum oscillation frequency f_{max} [63, 62]. The advantages of scaling down the transistor dimensions are apparent in digital design, where a steady decrease is seen in the power-delay product [63, 62]. However, in analog design some disadvantages appear. One disadvantage is that the breakdown voltage decreases with reduced physical dimensions, so that lower supply voltages must be used and stacking of transistors is less efficient [63, 62].

In this chapter wireless communication standards, CMOS technology and MOSFET operation are briefly discussed. UMTS and GSM-EDGE standards are described in detail. The influence of scaling, and some problems related to deep-submicron technology are also described in this chapter.

Chapter 2

Multi-Hop Communication Systems

Relaying is found in Packet Radio and Ad-Hoc networks whereby communications between mobile terminals are carried out in a distributed manner through intermediate relay nodes. When employed in a cellular network, this technique can be regarded as an Opportunity Driven Multiple Access (ODMA) [2] or more generally Multi-hop Cellular Network scheme where relaying is turned to when communications to and from the base station for a certain mobile terminal are poor due to a lack of LOS (Line-of-Sight) or severe multipath fading.

Multi-hop communication systems combine the benefits of having a fixed infrastructure of base stations and the flexibility of ad-hoc networks. They are capable of achieving much higher throughput than current cellular systems, which can be classified as single hop cellular networks. In multi-hop wireless communication systems messages are not transmitted directly from a user equipment to a base station. Instead intermediate devices repeat the messages between BS and UE. Figure 2.1 (a) illustrates the classical direct communication and multi-hop communication systems.

Figure 2.1 (b) illustrates the circumventing shadowing (dead spot) by multi-hop. Figure 2.2 (a) illustrates an example of multi-hop communication network.

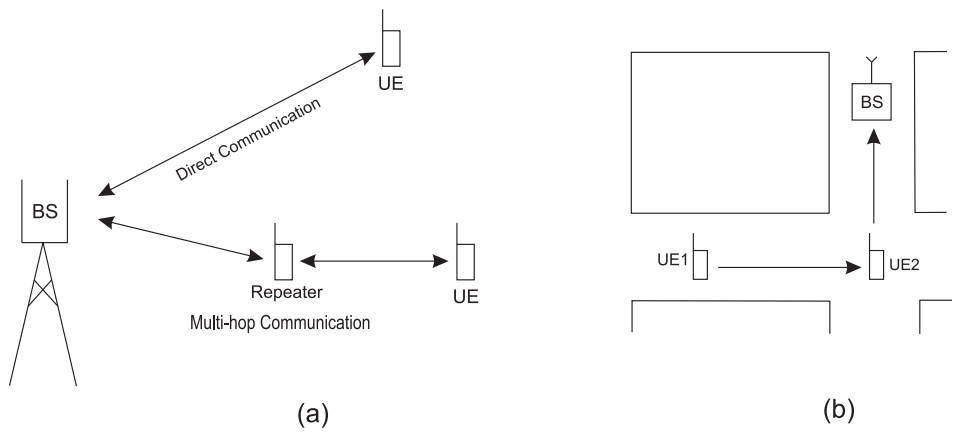

Figure 2.1: (a) Multi-hop and direct communication systems (b) Circumventing shadowing (dead spot) by multi-hop.

Using multiple hops, in a cellular system, is a way to decrease the required transmission power for user equipments and possibly mitigate interference and coverage problems [41]. Reductions in transmission power decrease the power consumption in user equipments; this increases the time between battery recharges. Also for health reasons transmission power reductions are attractive, though there are not yet any conclusive proofs of the health effects of cellular phones. Multi-hop communication can also provide service in 'dead spots' in a cell, which are not reachable by the BS in a single hop. However, any UE which is close to BS might face up to excessive communication traffic between the BS and any other distant UEs. This might result in less battery life time, more interference and security problems for the UEs which are closer to BS. At this point, well developed routing algorithms (optimum path selection) and user's cooperation and security issues are important and necessary for better overall multi-hop cellular network performance.

Multi-hop communication offers trade offs between coverage, capacity and power consumptions. To investigate the performance of multi-hop cellular networks and

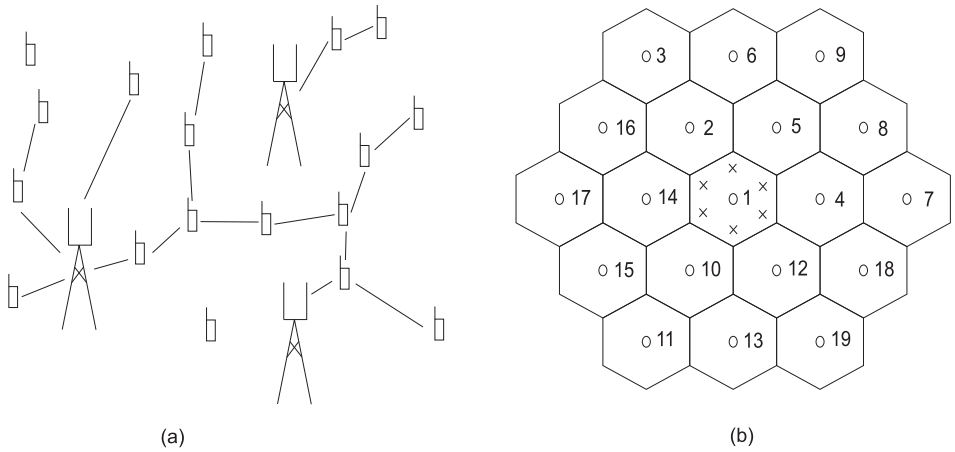

Figure 2.2: (a) Example of a multi-hop communication network (b) The network layout. Macro base stations are indicated by o and repeaters by x.

the resulting RF requirements a system model suitable for analyzing multi-hop networks is introduced. The adopted model has been chosen to reflect an urban high traffic scenario and is taken from 3GPP Radio Frequency Systems Scenarios with some additions necessary to model the multi-hop functionality [12]. Detailed system parameters, scenarios and simulation results are discussed in the following sections.

2.1 Radio Resource Provisioning

Splitting the transmissions between BSs and UEs into two or more hops increases the delay of the communications. Depending on the type of service considered, this can be acceptable or not. Multi-hop systems could be made in at least two different ways; 1. using fixed repeaters, and 2. using mobile repeaters. Fixed repeaters are special devices that an operator place at strategic places in the coverage area - they are assumed to be connected to a power source. A mobile repeater is any UE that acts as a repeater for other UEs - thus they run on battery power. This work concentrates on fixed repeaters using two hops.

When the transmission is split into two hops between a UE and a BS there are four transmission directions: from the BS to the repeater, from the repeater to the UE, from the UE to the repeater, and from the repeater to the BS. To provide radio resources for these transmissions at least three different methods can be used: Separation in time, separation in space, and separation in frequency.

Systems with separation in time end up being similar to time division duplex systems. There should only be additions in the protocols (e.g., routing and scheduling is needed) to add multi-hop functionality to an existing TDD cellular system. There is a potential capacity problem with this method if slots used for the extra hop are not reusable for other users.

Examples of cellular systems with separation in space are the traditional repeater systems where a repeater with a donor antenna directed at a BS (or an optical fiber directly from the BS) and a serving antenna directed towards the UEs. The attenuation between server and donor antenna must be in the order of 10 to 15 dB larger than the gain in the repeater [8]. Traditional repeaters are used for coverage inside buildings, in tunnels, and along highways or in other areas with bad coverage. The requirement for attenuation between antennas makes this method unsuitable here because we are interested in small user installed repeating devices with ideally only one antenna, or maximum two with a short distance between them. Thereby, separation using space diversity is not an option here.

Separation in frequency is the option in this work since this will put new requirements on the RF parts of the transceivers of both repeating and mobile devices. The question where to get this extra spectrum for the multi-hop can be solved in several ways. Below some examples are given on how multi-hop functionality can be introduced into an existing WCDMA-FDD network where the operator has access to either one carrier (2x5 MHz, i.e., 5 MHz for uplink and 5 MHz for downlink) or two adjacent carriers (2x10 MHz). The frequency bands could be, e.g., for pair one 1930-1935 and 2120-2125 MHz (with possible center frequencies 1932.4 and 2122.4 MHz), and for pair two 1935-1940 and 2125-2130 MHz (with possible center frequencies 1937.4 and 2127.4 MHz). In Figures 2.3 and 2.4 the possible center frequencies for different setups of the multi-hop system are stated.

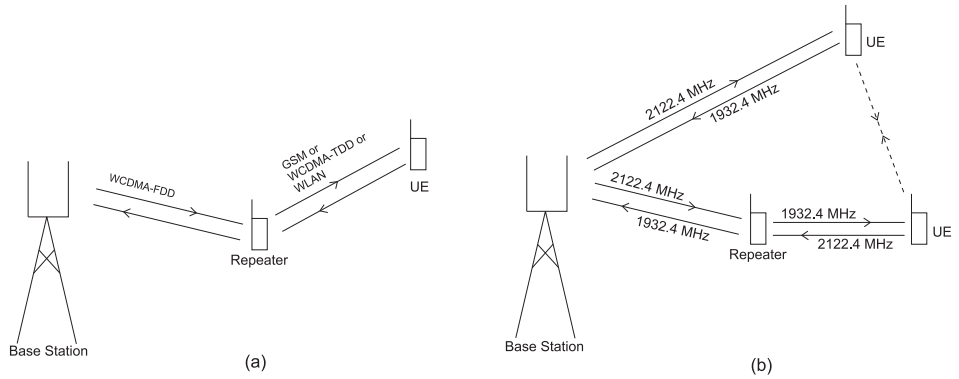

Figure 2.3: (a) Multi-hop system based on using other type of system (e.g., GSM/EDGE, WCDMA-TDD or WLAN) for the multihop part. (b) Multi-hop system where the repeater acts as a UE towards the BS and UE using the same frequencies. Transmission paths (solid) and interference (dashed).

To get extra spectrum for the multi-hop cellular network, one option is to use a system on a different frequency band for the part between the repeater and the UE, e.g., GSM, WLAN, Bluetooth or WCDMA-TDD mode could be used for that part, see Figure 2.3 (a). The challenge for the RF part is the efficiency of simultaneously transmitting and receiving on two different systems for the repeater.

The other option to get extra spectrum is that repeater acts as a user equipment. If it is assumed that UEs can switch receive and transmit bands (i.e., transmit in the normal receive band and receive in the normal transmit band), then the repeater can transmit as a UE towards both the BS and the repeated UE, as seen in Figure 2.3 (b). For operators with 2x10 MHz, or more, of available spectrum the second frequency band could be used for the second hop, as seen in Figure 2.4 (a). For both of these options there will be strong interference between the repeated UE and other UEs that communicate directly with the BS when they happen to come close to the repeated UE see the dashed lines in Figure 2.3 (b) and 2.4 (a). This can be solved with a fast intra-cell handover to the other frequency band. Another unavoidable source of interference is the extra interference at the BS created by the repeater's transmission to the UE, and the strong interference at the repeater created by the

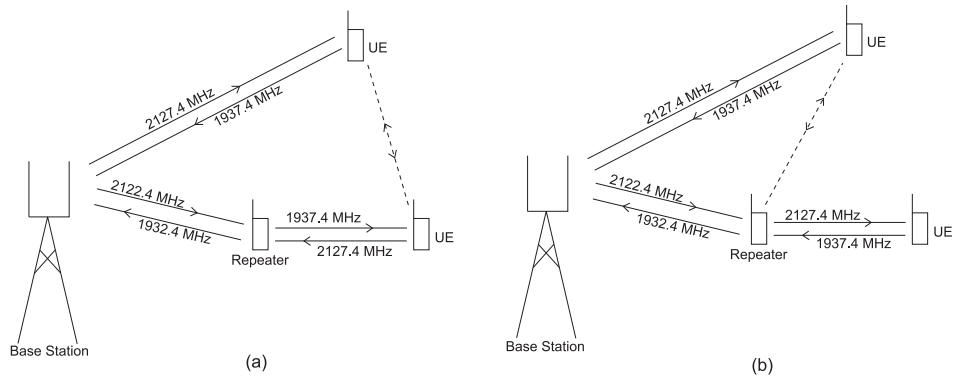

Figure 2.4: (a) Multi-hop system where the repeater acts as a UE towards BS and UE on different frequencies. (b) Multi-hop system where the repeater acts as an UE towards BS, and as a BS towards UE.

BS transmission to other UEs. These latter interferences can not be avoided and will result in problems for the repeater to receive the UE correctly. The challenge for the RF part is the ability for the UEs to switch the transmit and the receive frequency band.

Another option is when the repeater works as a UE towards the BS, and as a BS toward the UE on a second frequency band, see Figure 2.4 (b). In this scenario there will be strong interference between the repeater and UEs that communicate directly with the BS when they happen to come close to the repeater. This can be solved with fast intra-cell handover. An advantage, of this solution, is that existing UEs probably only will need updates to the protocols. The challenge for the RF part is the simultaneous transmission and reception on adjacent frequency bands in the repeater. This option is the case in this work.

2.2 System Models

In this section, system models suitable for analyzing multi-hop functionality are introduced into a WCDMA-FDD network as described in Section 2.1.3. Thus the

Table 2.1: System parameters [12, 14, 9].

PARAMETER	VALUE
Site to site distance	1000 m.
User bit rate	12200 bit/s
Chip rate	3.84 Mchip/s
Processing gain	3840/12.2
Noise factor UEs and repeater (for both frequencies)	9 dB
Noise factor BS	5 dB
Maximum UE output power	125 mW
Maximum BS output power	20 W
BS output power used for common channels (20% of maximum)	4 W
Maximum repeater output power (0.5 W in each band)	500 mW
SIR target in UE, and in repeater (downlink)	7.9 dB
SIR target in BS, and in repeater (uplink)	6.1 dB
ACLR when UE transmits	33 dB
ACLR when BS transmits	45 dB
Antenna gain in BS	11 dB
Antenna gain in repeater and in UE	0 dB
Downlink orthogonality factor	0.4
MCL between two repeaters, and between repeater and UE	45 dB
MCL between BS and repeater, and between BS and UE	53 dB
Repeater distance from BS 1	375 m.

system has 2x10 MHz of available spectrum. The models have been chosen to reflect an urban high traffic scenario, and are taken from 3GPP Radio Frequency Systems Scenarios [12] with some additions necessary to model the multi-hop. The model parameters are summarized in Table 2.1.

It is interested in the capacity aspects and therefore disregarded the mobility and used independent snapshots [19] to analyze the performance. A snapshot is a randomly chosen time interval that is long enough to let the power control converge but short enough that large scale propagation does not change.

The uplink (from the UEs to the BSs, possibly via a repeater) and the downlink (from the BSs to the UEs, possibly via a repeater) are independently investigated. The term link is used to denote the communication from a transmitter to a receiver. Thus a user communicates with two links: to and from the BS (or with four links if the user is repeated). All links are numbered with a unique integer tag.

2.2.1 Network Layout

It is assumed that a WCDMA-FDD system with 19 macro base stations placed in a hexagonal pattern as shown in Figure 2.2 (b). In the center cell six fixed repeaters have been introduced. As a reference case the same system without the repeaters is also investigated. We let all base stations in the system use both frequency bands. The communication between BS number one and the repeaters is located on frequency band one (1930-1935 and 2120-2125 MHz), and the communication between repeaters and repeated UEs is located on frequency band two (1935-1940 and 2125-2130 MHz). To avoid border effects, in the macro network, a wrap-around technique is used.

2.2.2 Propagation Model

In this section the path gain (G) is modeled. A transmitter transmitting with power P_{tx} is received with power $G.P_{tx}$ at the receiver. The path gain includes distance dependent attenuation, shadow fading, the antenna gains and the effect of minimum coupling loss (MCL). The MCL is due to assumptions on the minimum distance between a transmitter and a receiver; and it is dependent on the type of scenario that we are considering [10].

The propagation models suggested in [1] are used for simulations, the parameters are summarized in Table 2.2. There are four different types of propagation models needed in this scenario:

a) Between a BS and a UE.

b) Between a BS and a repeater.

c) Between a repeater and a UE.

d) Between repeaters.

For a. and b. the COST-Hata-Model is used. This model is suitable for outdoor urban areas where one of the antennas is placed above the roof top level.

Table 2.2: Propagation parameters [12, 1].

PARAMETER	VALUE
Frequency	2000 MHz
Repeater antenna height	4 m.
UE antenna height	1.5 m.
Height of buildings and width of roads	15 m.
Building separation	90 m.
Street orientation with respect to direct path	90°
Base station antenna height	30 m.
Standard deviation of shadow fading	6 dB
Shadow fading spatial correlation distance (Where correlation is equal to 1/e)	110 m.
Shadow fading BS/repeater correlation	0.5

The distance dependent part of the path gain between a BS and a UE/repeater is described, in dB, by

$$(G(d))_{dB} = -28 - 35 \cdot log_{10}(d) \tag{2.1}$$

where d is the distance in meters between communicating devices.

For c. and d. the COST-Walfisch-Ikegami-Model is used. This model is suitable for non-line-of-sight with both antennas placed below roof top level. The distance dependent part of the path gain is given, in dB, by the following equations:

$$(G(d))_{dB} = \begin{cases} -L_{fs} - L_{rts} - L_{msd}, & L_{rts} + L_{msd} > 0 \\ -L_{fs}, & L_{rts} + L_{msd} \leq 0 \end{cases} \tag{2.2}$$

where L_{fs} is the free space loss in dB, L_{rts} is the roof-top-to-street diffraction and scatter loss in dB, and L_{msd} is the multiple screen diffraction loss in dB.

To the distance dependent path gains a log-normal distributed shadow fading is also added [12], using the spatial correlation model of [33]. Moreover, the shadow fading value between a UE and different BSs/repeaters was assumed to be correlated (e.g., this models a user that moves into the basement of a building when the path gain decreases to all BSs and repeaters).

Thus the total path gain between a transmitter and a receiver is given, in linear scale, by

$$G = min(A_t \cdot A_r \cdot G(d) \cdot S; 1/MCL_k) \tag{2.3}$$

where A_t is the antenna gain at the transmitter, A_r is the antenna gain at the receiver, $G(d)$ is the distance dependent path gain, S is the shadow fading factor, and MCL_k is the MCL of this link.

2.2.3 Adjacent Channel Leakage Ratio

In simulation scenario there is severe interference in the repeaters due to the transmissions on adjacent channels. The system performance is investigated for some different values of ACLR in the repeaters, while ACLR of 45dB [9] for the BSs and ACLR of 33dB [14] for the UEs are used. Usually the requirements for the ACLR are lower in the UEs than in the BSs as a result of cost, power consumption, and form factor trade-offs.

2.2.4 Traffic and Service Model

The number of users per cell is assumed to be Poisson distributed and uniform over the coverage area. Because there have access to two frequency bands the traffic is modeled as two independent Poisson processes, each with the same average traffic load of λ (users/cell).

Every user is assigned to one BS (or to a repeater) - the selection is the one with the highest path gain. This models a scenario without handover or where handover has not yet taken place. Admission control or soft handover is not included; these could improve the performance especially for the downlink. It is assumed that the service to be speech however speech activity detection is not modeled.

2.2.5 Signal to Interference Ratio

The uplink signal to interference ratio (SIR), at the receiver of an uplink link i, is defined as:

$$SIR_i^u = \frac{PG \cdot G_{ii}^u \cdot P_i^u}{\sum_{j \in M^u} G_{ij}^u \cdot P_j^u + I_{ext,i}^u + N_i^u} \tag{2.4}$$

where u indicates uplink, PG is the processing gain (modeled as the chip rate divided by the user data rate), G_{ij}^u is the total path gain from transmitter of link j to the receiver of link i, P_j^u is the transmit power of the transmitter of link j, M^u is the set of links using the same frequency as link i (including the link i), and N_i^u is the thermal noise power at the receiver of link i. The interference power in the frequency band of link i at the receiver of link i from all links not using the same frequency as link i is $I_{ext,i}^u$- how to calculate it is described below.

The downlink signal to interference ratio, at the receiver of a downlink link i, it is defined as:

$$SIR_i^d = \frac{PG \cdot G_{ii}^d \cdot P_i^d}{\alpha \sum_{j \in K_i^d} G_{ij}^d \cdot P_j^d + \sum_{j \in M_i^d} G_{ij}^d \cdot P_j^d + I_{ext,i}^d + N_i^d} \tag{2.5}$$

where d indicates downlink, K_i^d is the set of links that are transmitted from the same antenna using the same frequency band as link i (including link i), M_i^d is the set of links using the same frequency as link i excluding the ones in set K_i^d, α is a factor that models the decreased interference due to the orthogonal codes used in the downlink, and the other quantities are defined correspondingly to the uplink.

The interference power in the frequency band of link i, from all links not using the frequency of link i, is

$$I_{ext,i} = \sum_{j \in M_i^e} \frac{G_{ij} \cdot P_j}{ACLR_{ij}} \tag{2.6}$$

where M_i^e is the set of all links not using the same frequency band as link i, and $ACLR_{ij}$ is the ACLR from the frequency band of the transmitter of link j to the

frequency band of the receiver of link i.

The thermal noise power at the receiver of link i is

$$N_i = kT_oWF_i \tag{2.7}$$

where kT_o is the noise spectral density ($-174dBm/Hz$), W is the chip rate, and F_i is the noise factor of the receiver of link i.

2.2.6 Power Control

The power control is modeled using the Distributed Constrained Power Control [32]. It is a distributed iterative algorithm that increase the transmit power for each link when received SIR is below the target for that link, and decrease the transmit power if the SIR is above the target. It is considered that the powers to have converged when the maximum power change between iterations, for any link in the system, is less than 3%. For the uplink we have the power in iteration n for the link i as:

$$P_i^{(n)} = min\left[P_{max,i}; \gamma_{t,i} \cdot \frac{P_i^{(n-1)}}{\gamma_i^{(n-1)}}\right] \tag{2.8}$$

where $P_{max,i}$ is the maximum transmit power of link i, $\gamma_i^{(n)}$ is the resulting SIR after iteration n and $\gamma_{t,i}$ is the target SIR for link i. The power updates are similar for the downlink, except that the constraint is on the total output power of each base station (or repeater). It is assumed that the BSs use 20% of the available downlink power for pilot- and common-channels.

2.2.7 Performance Measures

Uplink: If there are many links to a receiver, or when the path gain is low in one or more links, some links might end up using the maximum transmit power and thus not reaching the target SIR; they are in outage. These links are counted separately

for the two frequency bands and the uplink outage, for each frequency, is defined as:

$$\theta_k^u = \frac{\#\text{ users in outage}}{\lambda \cdot \#\text{ cells}} \tag{2.9}$$

where k indicates either frequency band one or frequency band two. A repeated user is counted in outage if one (or both) of the two links are in outage. Here there are potential improvements by removing some of the uplink users that can not achieve the required SIR target, but this is not investigated further.

Downlink: If there are many links from a transmitter, or when path gain is low in one or more links, then the available transmit power in the transmitter will not be enough to support all links. We then choose the link in the system that want the highest power and remove that user (we set the transmit power of the link to zero and if this link was part of the communication for a repeated user we also set the transmit power of the other link to that user to zero). The removed users are counted separately for the two frequency bands and the downlink outage is defined as:

$$\theta_k^d = \frac{\#\text{ removed users}}{\lambda \cdot \#\text{ cells}} \tag{2.10}$$

where k indicates either frequency band one or frequency band two.

Repeated users: The outage for the repeated users is also investigated. The repeated uplink outage is defined as:

$$\theta_r^u = \frac{\#\text{ repeated users in outage}}{\#\text{ repeated users}} \tag{2.11}$$

where r indicates that this is only the repeated users. The downlink outage for repeated users is defined correspondingly.

Increasing the load gives increasing outage. If a limit is set to the outage, e.g., a maximum acceptable outage of 5% the maximum load, or the capacity, of the system can be found.

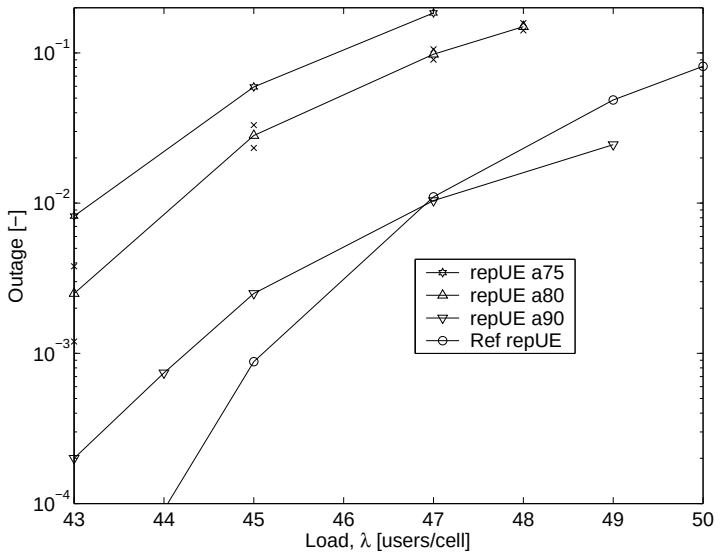

Figure 2.5: Uplink outage for the repeated UEs vs load. 95% confidence interval is shown for repUE a80.

2.3 Simulation Results

To investigate the performance of multi-hop cellular networks, a number of Monte Carlo simulations are performed. First, the uplink and downlink outage performance for some different values of repeater ACLR is investigated. After to get the outage performance, uplink power distribution performance is investigated. By looking at which users are repeated in the case with repeaters, the performance of those users in the case without repeaters is found. In the result figures, "repUE" is used to indicate repeated users, "Ref" indicates the reference case without repeaters, "a75", "a80", "a90" indicate ACLRs of 75 dB, 80 dB and 90 dB respectively, and "fq 1" is used to indicate users on frequency band one. For one of the curves, in most of the figures, it is plotted "x" for the approximately 95% confidence interval; the confidence intervals for the other curves were similar for similar outage level. Each point consists of at least 1000 snapshots.

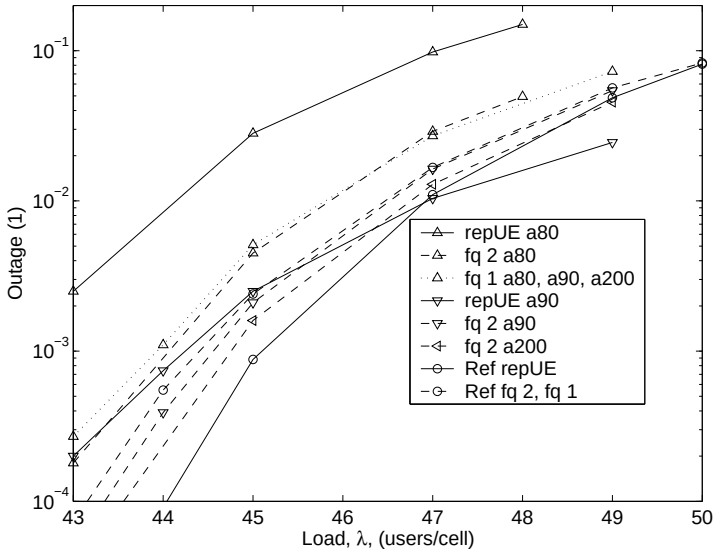

Figure 2.6: Summary of uplink outage vs load.

2.3.1 Uplink and Downlink Outage

In Figures 2.5 and 2.6 the uplink outage versus the load for the multi-hop system is shown together with the reference case without repeaters. The results are presented for some values of the ACLR that gave outage levels in the interesting range between 0.1% and 10%. Based on Figure 2.5 the outage for the repeated users is seen to decrease when the ACLR increases. It is seen that the outage for the repeated users is higher than for the reference case except for ACLR values of 90 dB or higher (The outage for an ACLR of 200 dB -ideal case was zero for this range of loads).

In Figure 2.6, the uplink outage versus load is plotted for all different cases. If the acceptable outage limit is set to 5%, the performance for an ACLR of 90 dB is limited by the outage on frequency band one. The capacity is then approximately 48.2 users/cell and frequency, or 1.2% lower than for the case without repeaters. We could probably reach a higher total load by having a lower load on frequency band one than on frequency band two, but this was not investigated any further.

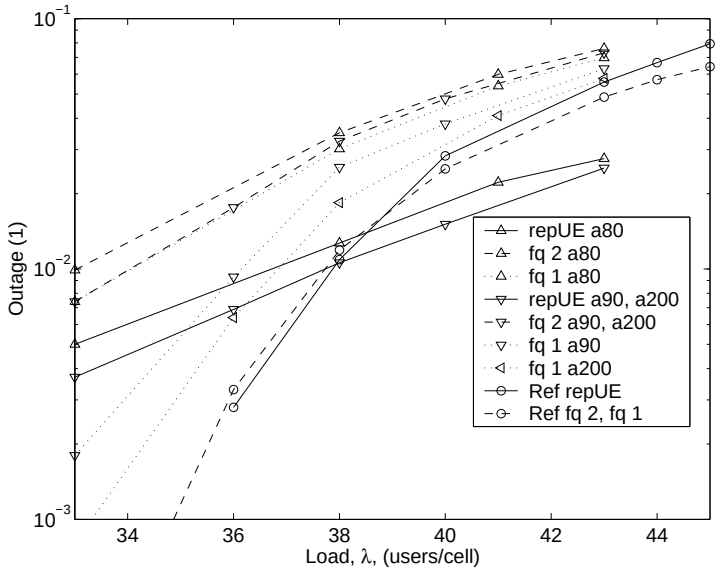

Figure 2.7: Summary of downlink outage vs load.

In Figure 2.7, the downlink outage versus load is plotted for all different cases. If the acceptable outage limit is set to 5%, the performance for an ACLR of 90 dB is limited by the outage on frequency band two. The capacity is approximately 40.4 users/cell and frequency band, or 6.5% lower than for the case without repeaters.

2.3.2 Uplink Power Distributions

First the UEs that are repeated are studied and compared to the transmission powers of the same UEs in the reference case without repeaters. Cumulative distribution functions (CDFs) and densities (using bins of size 0.5 dBm and normalized so that the sum over all bins is one in each figure) are estimated.

In Figure 2.8 the CDF of the repeated UEs is illustrated together with the CDF for the same UE's when no repeaters are included. In this figure, repeated UEs transmission powers are compared to the transmission powers of the same UEs in the reference case without repeaters. The results are based on a load of 49 users/cell and

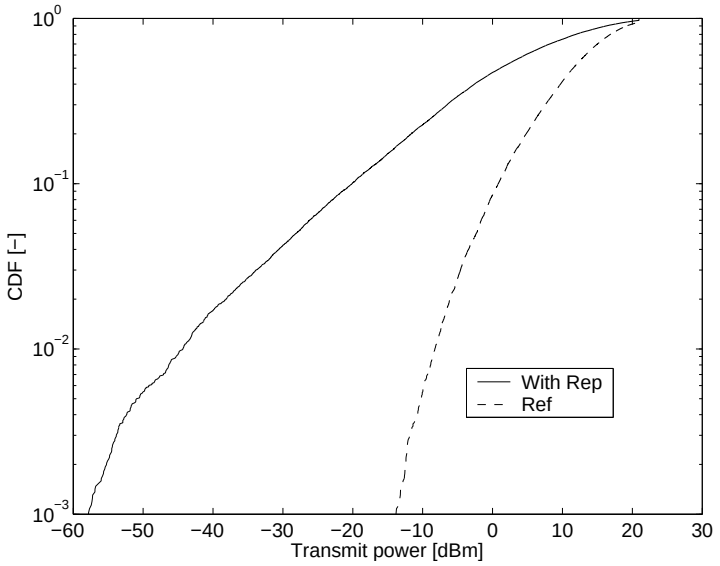

Figure 2.8: Uplink UE power CDF of repeated UEs. A load of 49 users/cell is used and the ACLR is set to 90 dB.

an ACLR of 90dB. Clearly the repeated users operate at much lower transmission power levels than the same UEs in the reference case without repeaters.

The estimated density of the repeated UEs is seen in Figure 2.9. The estimated density for the same UEs in the reference case without repeaters is shown in Figure 2.10. For the same load and ACLR, the outage is higher than for the case with repeaters (see Figure 2.5), and thus the peak at 21dBm is lower in Figure 2.9 than in Figure 2.10. The average power, in linear scale, is found to 28.6mW. Thus, approximately 3 dB is saved for the repeated users at this load and ACLR. Compared to the reference case it can also be seen that the signal power is distributed more evenly and over a larger range when using repeaters.

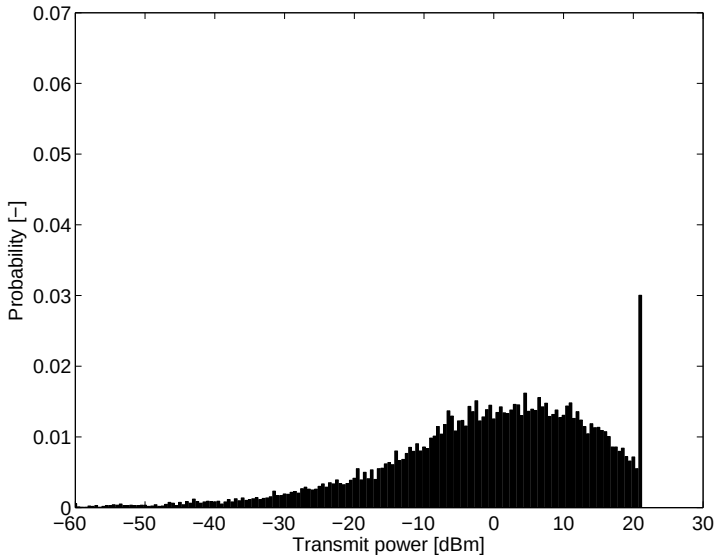

Figure 2.9: Uplink UE power density for repeated users. Load is 49 users/cell and the ACLR is 90 dB.

2.4 Conclusions

Based on simulation results new RF requirements have been identified in both transmitter and receiver sections. These requirements specifically relate to ACLR and power control range characteristics. According to uplink outage results, the multi-hop system performance is better than the reference system performance for an ACLR of 90 dB or higher. Uplink power distribution results also show that repeated users average transmit power is 3 dB less than reference case (direct communication system) and signal power is distributed more evenly and over a larger range when using repeaters. These new requirements are reflected to RF parts as a need for a highly linear PA with a wide power control range and sharp transmit/receive filter.

Besides the high linearity requirement, since the transmit powers are spread over a large power range when using repeaters, a wider power control range and a high accurate power control may be also needed for multi-hop cellular systems. In PA design there are trade-offs between high power efficiency, high linearity, load toler-

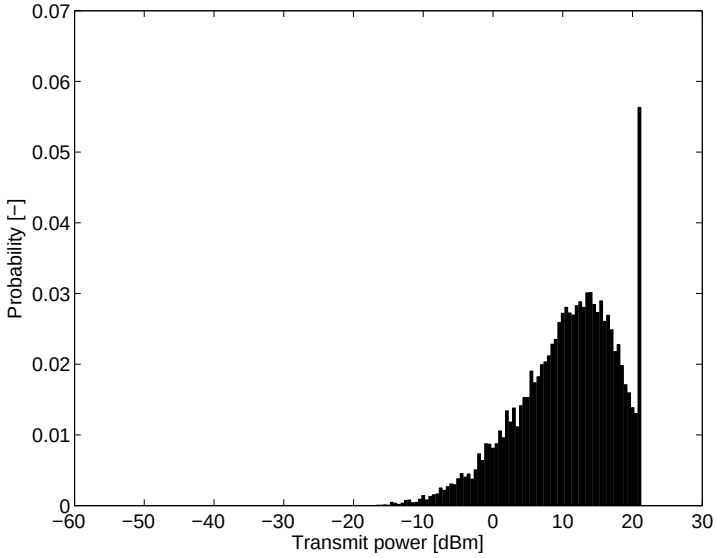

Figure 2.10: Uplink UE power density for reference (without repeater). Load was 49 users/cell, and ACLR was 90 dB.

ance and low cost/high integration. Meeting the high ACLR requirements over a wide power control range without reducing the power efficiency clearly represents a challenging issue in PA design for multi-hop systems. Filter design is another challenging issue for multi-hop system because of the high ACLR/selectivity requirement.

However, available technology sets limits to the ACLR; state of the art today can reach values of approximately 77 dB for a peak output power of +30 dBm (Rohde-Schwarz Vector Signal Generator, May 2003). Another problem, in the repeaters, will be the blocking - the ability to receive low power signals at the same time as transmitting on the adjacent band. This might require fixed sharp RF filters and thus after implementing this systems we might not be able to change the frequencies in the areas with multi-hop.

Chapter 3

RF Power Amplifiers

An amplifier is an assembly of electronic components for the purpose of adding significant power to an input signal, the power being obtained from a DC supply. An RF power amplifier implies in addition that the amount of power involved is relatively large, and that effects due to nonlinear operation of the semiconductor device(s) are important.

All practical RF systems or circuits are nonlinear to some degree: "linearity" is a convenient mathematical abstraction which may be valid for a wide range of conditions (e.g. well designed capacitors, resistors, transmission lines) or over a more or less restricted range (e.g. small-signal models for intrinsically nonlinear devices, such as transistors).

The mathematics of linear system analysis is highly developed (e.g. matrix analysis) and may be said to be essentially "complete". The mathematics of nonlinear systems is only poorly developed, and even simple nonlinear systems have no exact mathematical solution. Topics such as chaos, bifurcations etc. are relatively recent

branches of dynamical analysis. They highlight the fact that nonlinear systems may be unpredictable and exhibit a rich variety of behavior.

A generally distinctive aspect of linear systems is that any frequency component in the input is present in the response, and no new frequencies will be generated. The converse is true for nonlinear systems. A single-input, single-output is linear: if input $X_1(t)$ produces $Y_1(t)$, and input $X_2(t)$ produces $Y_2(t)$ then input $\alpha \cdot X_1(t) + \beta \cdot X_2(t)$ produces $\alpha \cdot Y_1(t) + \beta \cdot Y_2(t)$ for any $\alpha, \beta \in C$.

Examples of important high frequency circuit/systems which are fundamentally nonlinear: RF/Microwave power amplifiers, mixers, oscillators, multiplier/dividers, and limiters.

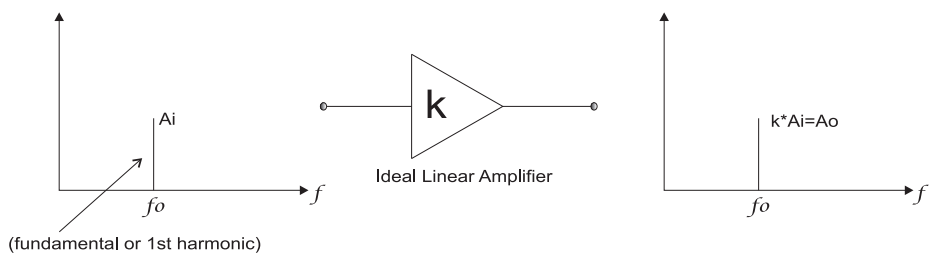

Figure 3.1: Idealized RF power amplifier, single tone excitation.

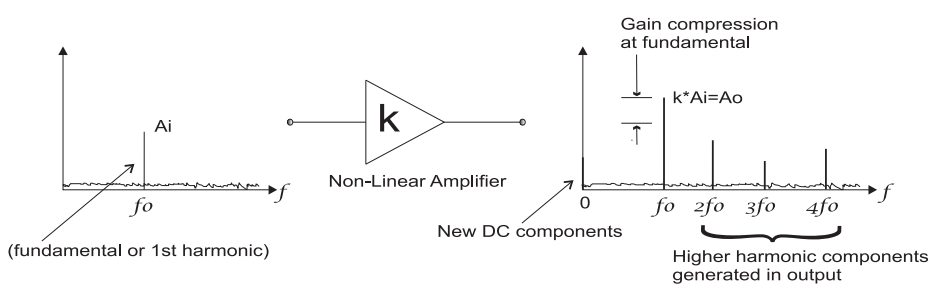

Figure 3.2: Practical RF power amplifier, single tone excitation.

One of the most challenging RF/analog parts to implement in CMOS technology is the power amplifier. Firstly, the transconductance to current ratio (g_m/I) of a CMOS

transistor is generally lower than that of a bipolar or III-V device, implying that for the same gain a higher current is needed. Secondly, with decreasing device length in CMOS technologies the oxide thickness is decreasing as well, resulting in a lower breakdown voltage [26]. Lastly, the low-resistivity substrate that is used in standard CMOS processing has limited the integration of high-quality passive components and consequently degradation on the amplifier performance.

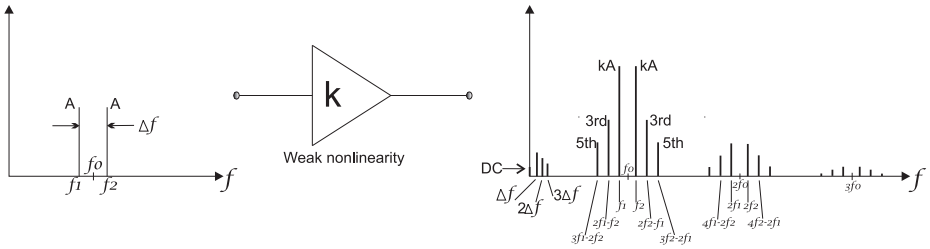

Figure 3.3: Two tone excitation.

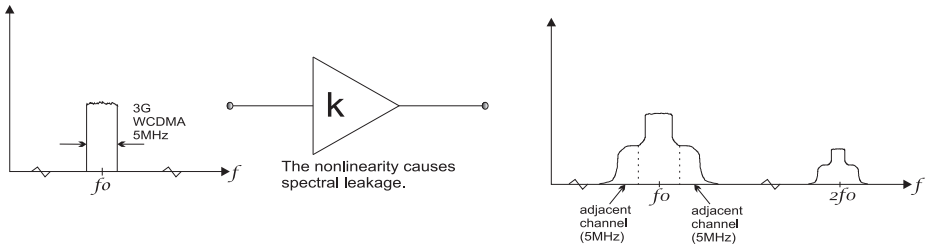

Figure 3.4: Practical RF power amplifier, digitally modulated carrier.

The performance of power amplifiers is a crucial issue for the overall performance of the transceiver's chain. Until now, power amplifiers for wireless applications have been produced almost exclusively in GaAs technologies, with few exceptions in LD-MOS, Si BJT, and SiGE HBT. Submicron CMOS processes are now considered for power amplifier design due to the higher yield, and the lower costs it can provide [54].

In Figures 3.1, 3.2, 3.3, and 3.4, typical amplifier behaviors are illustrated. Figure 3.1 illustrates the idealized RF power amplifier with single tone excitation, Figure 3.2 illustrates the practical RF power amplifier behavior with single tone excitation,

Figure 3.3 illustrates the amplifier behavior with two tone excitation, and Figure 3.4 illustrates the practical RF power amplifier behavior with digitally modulated carrier.

3.1 Classes of Operation

Power amplifier classes can be categorized either as bias point dependent, such as classes A, B, AB, and C, or depending on the passive elements in the output matching network that shape the drain voltage and current, provided that the transistor in this case operates as a switch, such as classes D, E, and F [35].

In linear class of amplification (A, B, C, F1), the transistor is a current source. Transistor "on" voltage does not saturate. In switching mode amplification (D, E, F2, F3, S), the transistor operates as a switch. Transistor "on" voltage saturates to as close to zero as feasible.

3.1.1 Class A, AB, B and C

Class-A amplifiers are generally the most linear and least efficient amplifiers. A class-A amplifier is one in which the operating point and input signal level are chosen such that the output current (drain current) flows at all times. It therefore operates in the linear portion of its characteristic and hence the signal suffers minimum distortion [40].

A class-B amplifier is one in which the operating point is at one or other extreme of its characteristic, so that the quiescent power is small. The quiescent current or the quiescent voltage of a class-B stage is approximately zero and hence if the excitation is sinusoidal then amplification takes place for only one-half of a cycle. Class-B operation is significantly more efficient than class-A for use in linear power amplifiers, whilst still providing useful levels of linearity. The poor availability of high power PNP devices at higher frequencies has tended to restrict the use of complementary class-B amplifiers to the HF bands. A practical class-B amplifier will also exhibit sig-

nificant crossover distortion due to the imperfect (nonlinear) transition from cut-off to the active mode [40].

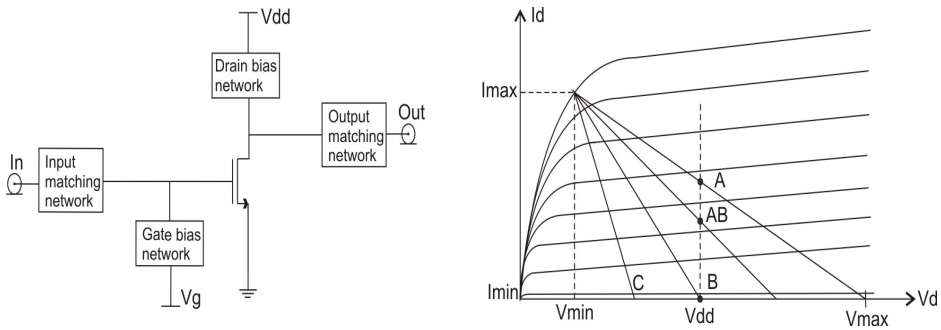

Figure 3.5: Single ended Class-A, B, AB, or C amplifier generic schematic.

A class-AB amplifier is a compromise between the two extremes of class-A and class-B operation. The output signal of this type of amplifier is zero for part, but less than one-half of the input sinusoidal signal. The distortion added by a class-AB amplifier is consequently greater than that of a class-A stage, but less than that of a class-B stage. Conversely the efficiency will be less than that of a class-B stage and greater than that of a class-A stage. The degree of distortion improvement (or degradation) will depend upon the level of standing bias applied and the consequent level of inefficiency which can be tolerated in a given application [40].

A class-C amplifier is characterized by the operating point being chosen such that the output current (or voltage) is zero for more than one-half of an input sinusoidal signal cycle. This class of amplifier will thus result in significant distortion of the input signal wave-shape during the amplification process, thus making it unsuitable for linear amplification applications [40].

The output efficiency and output power for a power amplifier operating in class-A, AB, B, or C are given by [27]:

$$\eta = \frac{v_{dd} - v_{dsat}}{v_{dd}} \frac{\theta - \sin\theta}{4(\sin\frac{\theta}{2} - \frac{\theta}{2}\cos\frac{\theta}{2})} \tag{3.1}$$

$$P_{out} = \frac{1}{2}(v_{dd} - v_{dsat})\frac{I_m}{2\pi}(\theta - \sin\theta) \tag{3.2}$$

The magnitude of the nth harmonic of the output drain current is given by [27]:

$$I_n = \frac{1}{\pi}\int_{\frac{-\theta}{2}}^{\frac{\theta}{2}} \frac{I_m}{1-\cos(\frac{\theta}{2})}(\cos\alpha - \cos(\frac{\theta}{2}))\cos(n\alpha)d\alpha \tag{3.3}$$

where V_{dd} is the supply voltage, θ is the conduction angle of the drain current, V_{dsat} is the pinch-off voltage (knee voltage), and I_m is the maximum drain current in the output transistor. The conduction angle is 2π for Class-A, π for Class-B, $\theta < \pi$ for Class-C, and $2\pi < \theta < \pi$ for Class-AB mode.

3.1.2 Class D, E and F

An optimally efficient amplifier would consist of a controlled switch, in which the on-resistance was zero, the off-resistance was infinite and the transition time was zero. The output signal would then consist of the power supply switched at the rate of the input (carrier) signal, with no losses in the switching device. The efficiency of this system would be 100% since there are no losses within the device either due to its resistance or due to a finite switching time [40].

The class-E amplifier is a single ended switching configuration with a passive load network. The simplest form of load network consists of a series tuned L-C circuit and a shunt capacitance. A class-F amplifier has a load network which is resonant at one or more harmonic frequencies in addition to its resonance at the fundamental frequency. The addition of harmonics, at the correct level, to the fundamental causes a flattening of the drain voltage waveform. The drain voltage waveform thus begins to approximate a square-wave with a consequent improvement in both efficiency and output power [40].

Class-S amplification utilizes a PWM input waveform, with the desired output waveshape contained in its mean value, and amplifies this switching waveform efficiently

before low pass filtering it to leave the desired output waveform. Two difficulties are immediately apparent with this type of amplifier. Firstly, the frequency at which the transistors must switch is many times that of the final output frequency of the amplifier and hence very wide bandwidth devices are required. This currently limits such techniques to low RF frequencies at best. Secondly, since there are few RF PNP devices available, this again limits the maximum frequency of operation of these amplifiers [40].

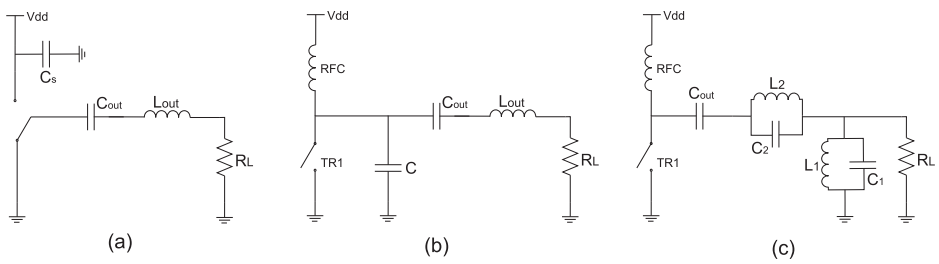

Figure 3.6: (a) Equivalent circuit of Class-D amplifier (b) Equivalent circuit of Class-E amplifier (c) Equivalent circuit of Class-F amplifier [40].

3.2 Stability Analysis

The stability is one of the most important criteria in the design stage. This is especially important when working at the lower frequencies where the high frequency transistors are usually conditionally stable.

The stability analysis is based upon the following fact: Any two-port network is unconditionally stable if the input or output reflection coefficient is less than one in magnitude for all passive load and source impedances. In terms of reflection coefficients, the basic conditions for unconditionally stability can be stated as follows [31]:

$$|\Gamma_S| < 1 \tag{3.4}$$

$$|\Gamma_L| < 1 \tag{3.5}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{3.6}$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{3.7}$$

These conditions can be more useful if they are grouped into a simpler set of conditions known as Rollet's stability factors [31]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \tag{3.8}$$

$$|\Delta| < 1 \tag{3.9}$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.10}$$

If the two-port does not satisfy these conditions then it is said to be conditionally stable. The source and load impedances for which the two-port is stable are found by setting the input and output reflection coefficients to one and solving the Eqs. (3.4)-(3.7) for the source and load reflection coefficients. The solutions for Γ_S and Γ_L lie on stability circles [31].

$$\left| \Gamma_L - \frac{(S_{22} - \Delta S^*{}_{11})^*}{|S_{22}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{3.11}$$

$$\left| \Gamma_S - \frac{(S_{11} - \Delta S^*{}_{22})^*}{|S_{11}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{3.12}$$

These circles determine the border between the stable and unstable regions in the input plane and the output plane, respectively. The determination of which side of the circle, for example the input stability circle, is stable is made by looking the magnitude of the input scattering parameter (S_{11}). If the magnitude of this quantity is smaller than 1 then the center of the Smith chart ($R = 50\,\Omega, X = 0$) shows a stable point and vice versa. Then, the side of the circle that encompasses the center is considered to be stable [50]. The same is valid in the output plane for the parameter

S_{22}. In simulation programs, all these stability calculations are made automatically and the designer can see the results in a graphical environment.

A potentially unstable transistor can be made unconditionally stable by either resistively loading the transistor or by adding negative feedback. In narrowband amplifiers, these techniques will end up degradation in power gain, noise figure, and VSWRs [31].

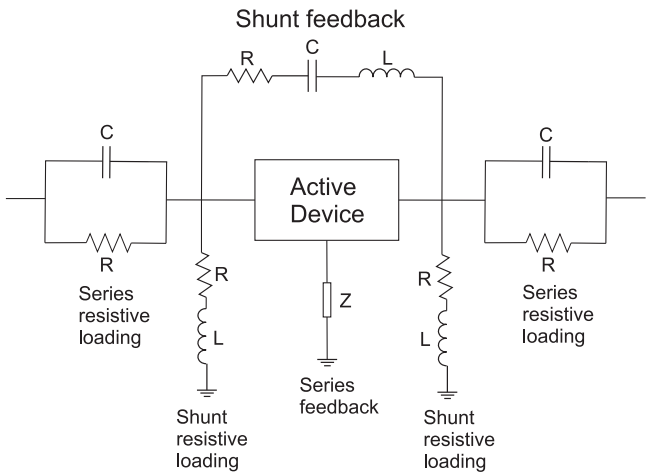

Figure 3.7: Serial, shunt and feedback resistive loading.

Figure 3.7 shows the different resistive loading configurations for the stabilization. Serial gate resistance with parallel capacitance and the output shunt inductance with serial resistance are the most common ones.

3.3 Impedance Matching Networks

For optimum power transfer efficiency in the passband it is desirable to match impedances of sections connected together in a passive or an active circuit. Passive as well as active microwave circuits require impedance matching of complex loads with reactive constraints. Single frequency or narrowband (less than 10% typical)

impedance matching is simply achieved using a single fixed tuned network or, at most, a two-element network depending upon the Q of the structure. Broadband matching network design, particularly for bandwidths greater than 50%, is a difficult and challenging task due to prescribed reactive constraints, broadband impedance transformations of large impedance ratios, and prescribed tapered magnitude characteristics [21].

Broadband impedance matching was first introduced by Bode and Fano to enhance the bandwidth of antennas [23, 29]. Fano has derived a complete set of integrals that predicts the gain-bandwidth restrictions for lossless matching networks terminated in an arbitrary load impedance [29]. Fano's broadband method is hence a natural solution to extend the bandwidth of narrowband circuits.

Basically, the design of a constant gain amplifier over a broad frequency range is a matter of properly designing the matching networks, or the feedback network, in order to compensate for the variations of $|S_{21}|$ with frequency [31]. Two techniques that are commonly used to design broadband amplifiers are the use of compensated matching networks and the use of negative feedback. The technique of compensated matching networks involves mismatching the input and output matching networks to compensate for the changes with frequency of $|S_{21}|$. The matching networks are designed to give the best input and output VSWR.

3.4 Efficiency Enhancing Techniques for Power Amplifiers

Linear digital modulation techniques in modern communication systems generate carrier signals with relatively high peak-to-average ratio. For linear amplification of such a signal, power amplifier must be operated at excessive back off, thus sacrificing the overall amplifier efficiency. Efficiency boosting schemes can be used to enhance the efficiency of power amplifier.

3.4.1 Outphasing

The outphasing technique (LINC) combines two nonlinear RF power amplifiers into a linear RF power amplifier system. The two PA's are driven with signals of different phases, and the phases are controlled so that the addition of the PA outputs produces a system output of the desired amplitude. The outphasing technique can be classified into two categories: simple (transformer coupler) and Chireix (transmission line coupler with shunt reactance) outphasing [51].

Class-A power amplifiers have constant dc input current and, hence, constant dc power consumption. The efficiency of an outphasing system with class-A PA's is therefore the same as that of a linear class-A PA. For saturating class-B and class-C power amplifiers, the efficiency at lower output voltages can be considerably improved by the Chireix system. For class-D power amplifiers whose efficiency remains high regardless of the load impedance, simple outphasing system is quite satisfactory [51].

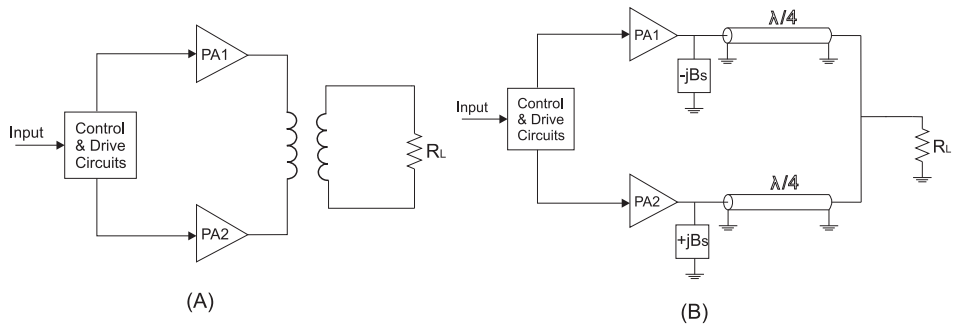

Figure 3.8: (A) Simple outphasing system (B) Chireix outphasing system.

Figure 3.8 illustrates the simple and Chireix outphasing systems. Despite the both techniques are very useful to enhance the efficiency of class-B, class-C, and class-D amplifiers, these two techniques have drawback because of the implementation problems in CMOS technology. Implementation of simple outphasing system with integrated low loss transformer, and the implementation of Chireix outphasing system with integrated quarter wavelength transmission lines are critical issues in CMOS technology.

Monolithic transformers have been used in silicon radio frequency integrated circuit designs to perform impedance matching, signal coupling, phase splitting, low-loss feedback, and single-ended to differential signal conversion. A monolithic transformer can be realized either by tapping into a series of turns of microstrip lines or by interwinding two identical spiral inductors [66]. However, high quality passive components (e.g. inductors) are hard to achieve in a standard CMOS technology. The inductance and Q depend on various factors such as frequency, geometry of the metal wire, properties of the metal and the insulating layer, and properties of the substrate. In CMOS VLSI technology the Si substrate generally is heavily doped, i.e. lossy compared to a more lightly doped Si bipolar substrate [24]. This typically limits the Q to be less than 10, while discrete inductors can reach a Q of 100 and bondwires between 25 and 50 [26].

3.4.2 Doherty Technique

The Doherty amplifier is a technique for improving the efficiency of backed-off linear amplifiers. In a Doherty amplifier, the output powers of two amplifiers operating at a proper phase alignment and bias level, are combined using appropriate power combining techniques. Figure 3.9 illustrates the schematic of a Doherty amplifier [40].

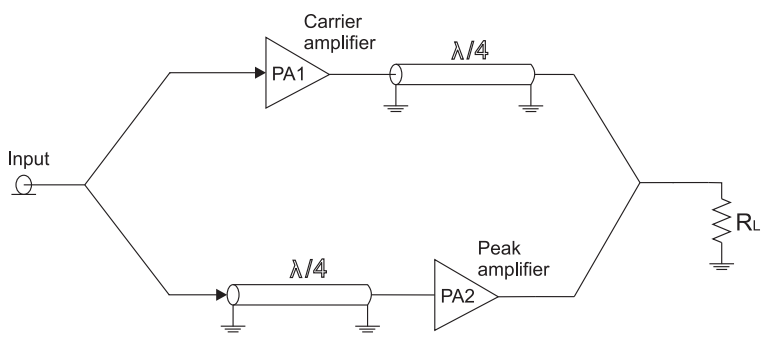

Figure 3.9: Schematic of a Doherty amplifier.

The Doherty amplifier consists of one main (carrier) and one auxiliary (peaking)

power amplifier. The main amplifier is typically biased class-B and the auxiliary amplifier is typically biased class-C, so that the auxiliary amplifier turns on at the power when the main amplifier reaches saturation. The current contribution from the auxiliary amplifier reduces the effective impedance seen at the main amplifier's output. This "load-pulling" effect allows the main amplifier to deliver more current to the load while it remain saturated. Since an amplifier in saturation typically operates very efficiently, the total efficiency of the system remains high in this high power range until the auxiliary amplifier saturates [39].

Because the Doherty amplifier requires quarter-wave transmission line and input splitter circuits, the integrated circuit implementation of the Doherty amplifier is not easy and practical. Many published papers show that $\lambda/4$ impedance transformer can be replaced by π-type L-C lumped components [59]. However, the size and loss problems especially due to large inductors are still burdens to achieve integrated transmission lines in CMOS technology.

Figure 3.10 shows that a quarter wavelength transmission line with f_o carrier frequency and Z_o characteristic impedance can be approximated to n segments of L-C ladder [59]. Inductance and capacitance values of L-C ladder can be given as follow:

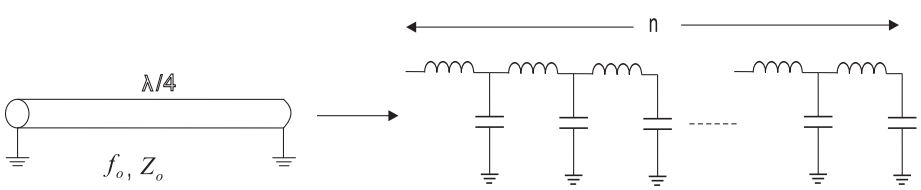

Figure 3.10: Quarter wavelength transmission line with n segments of LC ladder.

$$L = \frac{Z_o}{4nf_o} \tag{3.13}$$

$$C = \frac{1}{4nf_oZ_o} \tag{3.14}$$

Besides the size and loss problems especially due to inductors, minimum coupling effect between inductors requires some reasonable distance between them and consequently extra chip size.

The Doherty technique appears to offer some useful possibilities for solving some of the problems that arise in both mobile and base station amplifiers in modern wireless communication systems. It would appear to be especially relevant to systems using nonzero crossing modulation schemes, such as OQPSK and $\pi/4$DQPSK. In the latter case, for example, the low point of the envelope is only about 12 dB below the global peak power; thus, the efficiency improvement would be significant for most of the envelope power range [27].

3.4.3 Kahn Envelope Elimination and Restoration

The Kahn Envelope Elimination and Restoration technique is particularly attractive as it can utilize power efficient amplifiers, while also providing high linearity. An input RF signal is split into its polar components, envelope and phase, by an envelope detector and a limiter respectively. The limiter output is a constant envelope signal that can be amplified by a power efficient but nonlinear power amplifier such as class-C, class-D, class-E or class-F. Figure 3.11 illustrates a Kahn EER architecture [49].

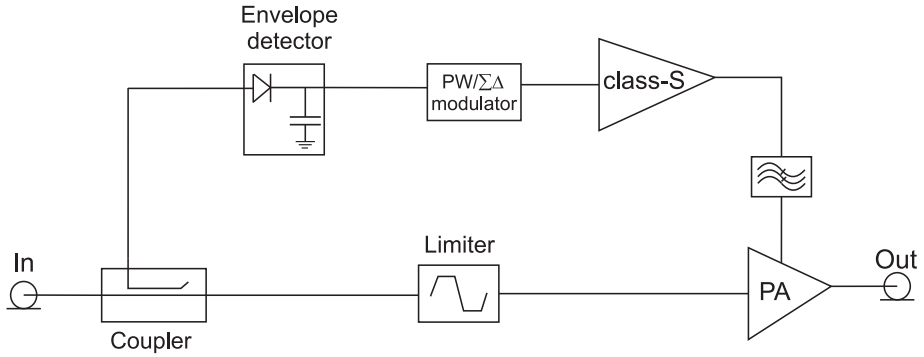

Figure 3.11: Kahn EER architecture.

In theory, a well-saturated amplifier can be approximated by an RF voltage generator whose output amplitude is proportional to the DC supply voltage [49, 52]. The envelope information is restored at the output by modulating the supply voltage of

the PA, where the modulating signal is derived from the envelope detector. Thus, EER shifts the linearity issue away from the PA, but places demands on how accurate the envelope and phase information can be recombined. An accurate delay matching is critical .

3.4.4 Envelope Tracking

When the amplifier's output power decreases, its efficiency also drops sharply. Deep class-AB or class-B amplifiers improve their efficiency by a self adaptation of the current drawn from the power supply [57]. However in many cases, neither deep class-AB or class-B provides enough linearity as, for instance, in CDMA applications where spectral regrowth is of primary concern. From class-A to class-B, RF PAs face the linearity and efficiency tradeoff. The class-A is linear but power inefficient, whereas class-B is efficient but has a poor linearity.

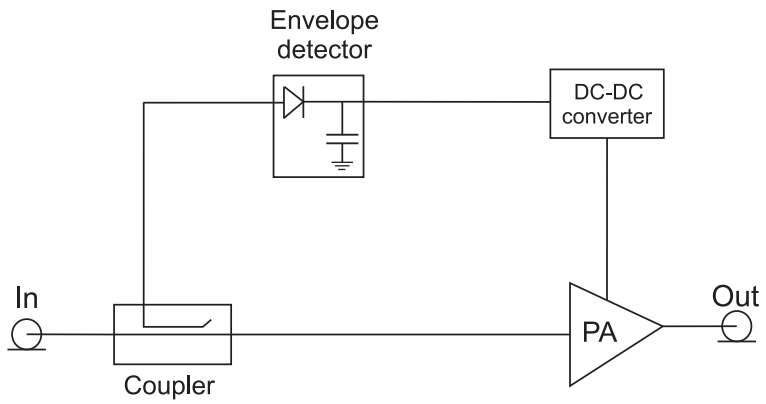

Figure 3.12: Dynamic supply PA architecture.

An alternative solution to improve the linearity-efficiency tradeoff is to adapt the power supply voltage of a linear PA with respect to input RF signal envelope. The supply voltage is varied dynamically to conserve power, but with sufficient excess to allow the RF PA to operate in a linear mode. Figure 3.12 illustrates the dynamically biased power amplifier architecture. Typically, the envelope is detected and used to

control a DC-DC converter. The efficiency is significantly better than that of a linear RF PA operating from a fixed supply voltage.

In dynamically supplied power amplifier, DC-DC converter efficiency is one of the key parameter in total system efficiency. State of the art today can reach values of approximately 95% efficiency in DC-DC converter. The another issue is in band harmonics produced by pulse width modulator switching. Pulse width modulators will produce extra harmonics and these will effect the linearity of the system.

The main problem in DC-DC converter is to integrate the output L-C low pass filter on chip.

3.5 State of the art in CMOS PAs

Performance comparison of some previously reported CMOS power amplifiers is given in Table 3.1. To date, there are few reported fully integrated power amplifiers with high output power, efficiency and linearity. The disadvantages of scaling down the transistor dimensions also appear in analog/RF design, specifically in PA design because the breakdown voltage decreases with reduced physical dimensions. For frequencies up to several GHz and low to medium output power, CMOS may be an alternative to stand-alone power amplifiers, in exchange for less efficiency and a lower maximum output power.

Table 3.1: State-of-the-art in CMOS PAs.

Ref.	**Pout (dBm)**	**Freq. (GHz)**	**PAE (max.)**	**Tech-nology**	**Output matching**	**Class**
[56] VLSI'94	15 @1-dB	0.9	$< 30\%$ (η)	1μm CMOS	off-chip	C
[30] RFIC'00	23.5 max.	1.9	35% (PAE)	0.35μm (Bi)CMOS	off-chip	AB
[20] IJSSC'02	33.4 max.	2.4	31% (PAE)	0.35μm (Bi)CMOS	on-chip	E/F3
[45] MTT-T'01	28.2	1.9	30% (PAE)	30 GHz BiCMOS	off-chip	AB
[59] IJSSC'02	24.8 max.	1.4	49% (PAE)	0.25μm CMOS	off-chip (transm. lines)	F
[42] ISSCC'01	31.8 max.	0.9	43% (PAE)	0.2μm CMOS	off-chip	F
[28] ISSCC'01	30 max.	1.8	45% (PAE)	0.35μm CMOS	off-chip	AB
[25] MTT-S'00	20 max.	1.9	16% (η)	0.8μm CMOS	on-chip	F?
[25] MTT-S'00	22 max.	2.4	44% (η)	0.25μm CMOS	off-chip	F?
[38] RAWCON'01	17.5 max.	2.4	16.4% (PAE)	0.35μm CMOS	partly on-chip	A
[61] ISSCC'02	23 max.	2.4	42% (PAE)	0.18μm CMOS	off-chip	AB
[48] IJSSC'02	30 max.	0.7	62% (PAE)	0.35μm CMOS	partly on-chip	E
[64] IJSSC'01	9 @5-dB	2.4	16% @5-dB	0.18μm CMOS	partly on-chip	AB?
[34] IJSSC'01	18.6 max.	0.9	30% (PAE)	0.6μm CMOS	on-chip	C

Chapter 4

Dynamic Supplied CMOS Power Amplifier for GSM-EDGE Transmitters

Most modern digital modulations with high spectral efficiency present a non-constant envelope, which requires RF circuits with high linearity to prevent signal degradation. Efficient but nonlinear power amplifiers are thus not suitable for such linear modulations. The use of linearizing circuits can alleviate this issue, but at the price of high complexity and additional power consumption, which can be critical in the case of low or medium power amplifiers [30, 58]. In order to satisfy the linearity requirement for preserving modulation accuracy with minimum spectral regrowth, power amplifiers are typically operated in highly linear Class-A or -AB configurations. One of the major problems with these linear power amplifiers is their low power efficiency. Therefore, achieving high efficiency in power amplifiers while maintaining the required high degree of linearity is a challenging issue [65].

In this work a two-stage Class-AB CMOS RF power amplifier is designed and mea-

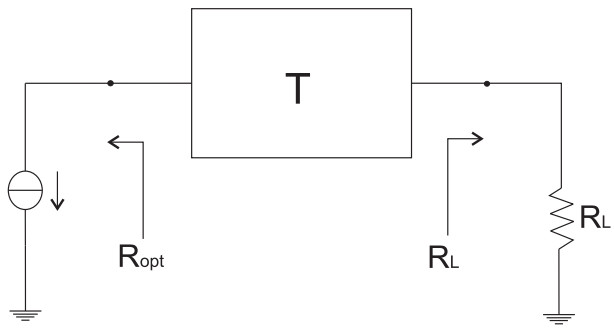

Figure 4.1: Impedance transformation network.

sured. The amplifier is measured according to EDGE requirements which required high degree of linearity, and hence linear class of amplification is necessary.

This work also analyzes efficiency improvements obtainable using a DC-DC converter which lets the power supply voltage track the envelope of the signal. The idea is to adapt the supply voltage to the envelope of the signal. In this way, it is expected to improve the efficiency of the power amplifier while maintaining the required high degree of linearity.

4.1 Analysis

A two-stage single-ended class-AB power amplifier is designed and implemented in 0.25 μm CMOS technology. It is intended for medium output power ranges such as EDGE E3, and has an operating frequency of 1.75 GHz. The UE maximum average output power levels for EDGE E3 is 22 ± 3 dBm. The EVM requirements for mobile terminals are maximum 9% in RMS and 30% in peak, and the required spectral quality is -54 dB at 400 kHz offset.

In Figure 4.1 a current source with impedance transformation network T is shown. This serves as a model for an ideal output stage, where the transistor operates as a controlled current source driving R_{opt}, the transformed load impedance R_L. The

power supply voltage is V_{DD}, the rms value of the load voltage is V_L, and the ideal maximum output power is given by

$$P_{out} = \frac{V_L^2}{R_{opt}} = \frac{V_{DD}^2}{2R_{opt}} \tag{4.1}$$

where V_L is the $V_{DD}/\sqrt{2}$. For $P_{out} = 20$dBm, and $V_{DD} = 2.5$ V, the optimum load resistance R_{opt} is equal to 31Ω. It is 24Ω for $P_{out} = 21$dBm, and 19Ω for $P_{out} = 22$dBm.

One of the most crucial non idealities in any power amplifier implementation is the knee voltage, i.e. the minimum drain voltage necessary to have the PA operating as an amplifier [26, 27]. V_{knee} reduces the maximum voltage swing. The output voltage swing is reduced to $V_{DD} - V_{knee}$, and the maximum output power can be written as

$$P_{out} = \frac{(V_{DD} - V_{knee})^2}{2R_{opt}}. \tag{4.2}$$

Besides the knee voltage effect, there are other non idealities which cause the voltage degradation at the drain. These are the series resistance of the RF choke, finite output impedance of the transistor, and the finite quality factor of the other passive components. To compensate these losses and deliver the required output power, an optimum load should be less than the ideal case in equation 4.1.

In PA analysis and design, power added efficiency (PAE) is used as a measure of efficiency. PAE is described as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{4.3}$$

where P_{out} and P_{in} are the RF output and input powers, and P_{DC} shows the power supplied by the battery.

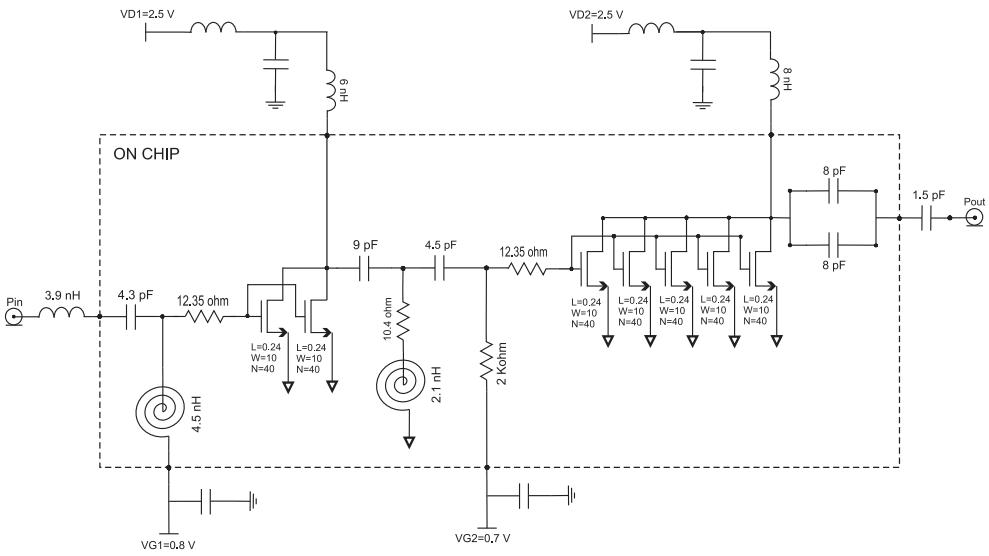

Figure 4.2: Schematic of the two-stage single ended power amplifier.

4.2 Design and Implementation

4.2.1 Core Amplifier

The power amplifier is designed as a single-ended two-stage common source amplifier. It is biased in class-AB to get high linearity and reasonable efficiency. The amplifier is designed and fabricated with 0.25 μm CMOS process under 2.5 V supply voltage. Figure 4.2 shows the schematic of the CMOS power amplifier.

To satisfy the EDGE E3 power specifications (see Chapter 1), an output power of 21 dBm was aimed in the PA design. To achieve this power level with a 2.5 V supply voltage, a transistor width of 2000 μm was used in the output stage. The length of the transistor was set to minimum (0.24 μm) to maximize its high frequency gain. To achieve the 2000 μm transistor width, 5 parallel transistors were used. Each of them has 40 fingers and the finger width is 10 μm. The estimation of the required transistor size and the bias point is an iterative process using the I-V characteristics of the transistor. The bias voltage was set to 0.7 V in the output stage to operate it

in class-AB mode.

The driver stage transistor size is established after simulation of the output stage power gain. To ensure that the driver stage does not enter compression before the output stage, a transistor width of 800 μm was chosen. To achieve the 800 μm transistor width, 2 parallel transistors were used. Each of them has 40 fingers and the finger width is 10 μm. The length of the transistor was set to (0.24 μm). The bias voltage for the driver stage was set to 0.8 V to achieve enough gain and linearity.

The load impedance for maximum output power is determined by simulations using the Agilent-ADS Harmonic-Balance simulator. The optimum load is approximately $11.5 - j6.4\,\Omega$. The input and output matching circuits are designed by using on-chip, off-chip components, and interconnection elements (bond wires, pad capacitances, and PCB board traces), see Figure 4.2.

Load inductances (choke inductances) are implemented as off-chip components. In 0.25 μm CMOS process, Metal-5 layer maximum current density is 1.5mA/μm hence implementing the load inductances on chip will increase the size and cost of the dice on a large scale. On the other hand choke inductances are also part of the interstage and output stage matching networks, that is, the high quality factor is necessary for these components, and it is a difficult issue to obtain it by on-chip components.

Some part of the input and output matching networks was also implemented as off-chip components. In this way it was possible to compensate the on-chip component tolerances and PCB effects.

The stability of the amplifier was ensured with the serial gate resistors, at the cost of a slight reduction in the gain and efficiency and with on-chip ground separation technique. On-chip ground separation weakens the any parasitic feedback between the driver and output stages and in this way the amplifier stability is improved. This technique will be explained in detail in the following section.

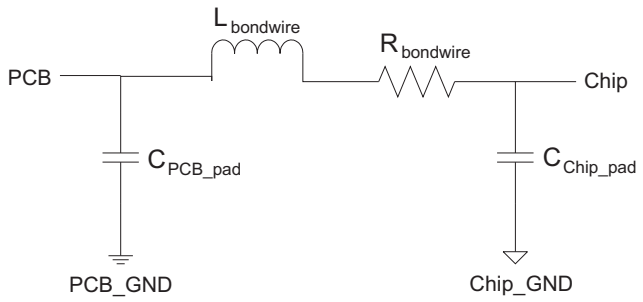

Figure 4.3: Interconnection model for chip signal/bias pad to PCB signal/bias pad.

4.2.2 Parasitics and Interconnection Models

In the circuit simulations, two interconnection models are used; one is from chip signal/bias pad to PCB signal/bias pad, and the other is from chip ground pad to PCB ground pad. These models are shown in Figures 4.3 and 4.4. These models are suitable for the chip-on-board assembly used in the measurements.

Printed Circuit Board:
The chip was bonded to a double-sided PCB with a copper thickness of 35 μm. The substrate material is FR–4 and its thickness is 1 mm. For easy wire bonding, the top layer of the PCB is plated with the soft gold material. In order to improve the grounding of the board, multiple through-hole ground vias were used. To minimize the inductive reactance of passive components, vias were placed as close as possible to components [7]. It is also very important to use efficient capacitive decoupling between the Vdd feed points and ground. This will prevent tendencies toward oscillations. All RF routing is realized using microstrips with 50Ω characteristic impedance. To minimize RF coupling from the output to the input, all RF lines has been kept as short as possible.

PAD Model:
On the chip, 85 μm $\times$ 85 μm pads are used for all connections. The shunt capacitance of a single pad was found to be approximately 65 fF in prior measurements.

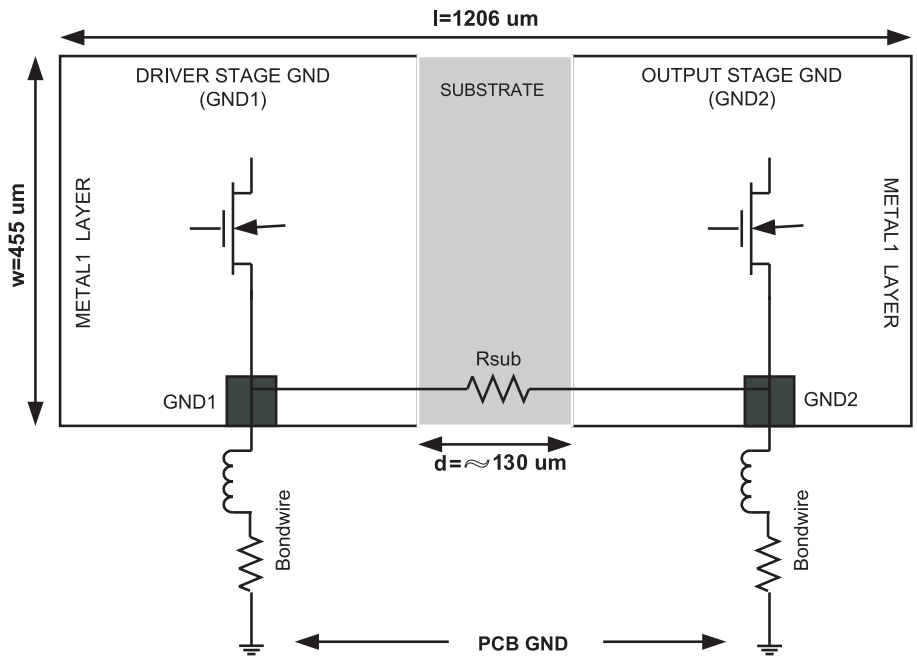

Figure 4.4: Interconnection model for chip ground pad to PCB ground pad.

Bondwire Inductance:

Bondwire material is gold and the diameter is 0.001inch. The inductance value of the bondwires is assumed to equal approximately 1 nH/mm [43]. Multiple bondwires are used in order to reduce the bondwire inductance both in output matching network and ground connections. It is assumed that three parallel connected bondwires has about 0.4 nH/mm inductance [37].

Ground bounce inductance plays an important role on the amplifier stability. If all stages in a multi-stage amplifier share the same on-chip ground, they will also share the same inductance to PCB ground. Signal current in the output stage converted to voltage by this inductance will thus be fed back to the input with a risk of instability. Using the proposed ground separation technique this feedback path is weakened.

Figure 4.4 shows the interconnection model for chip ground pad to PCB ground

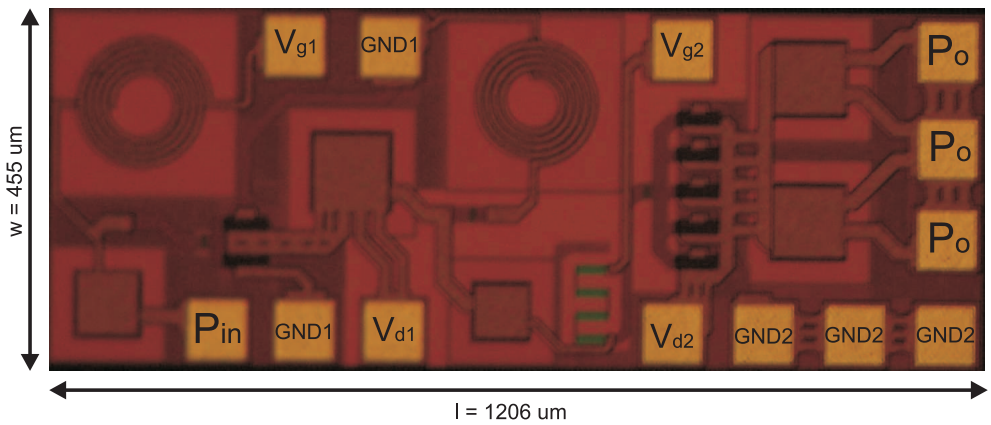

Figure 4.5: CMOS power amplifier die photo.

pad. Different chip grounds are assigned for driver and output stages, GND1 and GND2. PCB ground is assumed to be a perfect ground and is denoted by GND. Driver and output stage grounds are isolated from each other by the substrate resistivity. The on chip ground assignment is also illustrated on die photo, Figure 4.5.

Investigations showed that when driver and output stage grounds are separated, the stability was improved. Figure 4.6 shows the simulated stability factor of the amplifier with and without ground separation. As can be seen the PA with the ground separation technique is stable, whereas without the technique the amplifier is potentially unstable and malfunctioning.

To quantify the stability of the amplifier, the Rollet Stability criteria is used. The Rollet Stability criteria can be expressed as follows [44]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{4.4}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{4.5}$$

- Stable: $K > 1$ and $|\Delta| < 1$

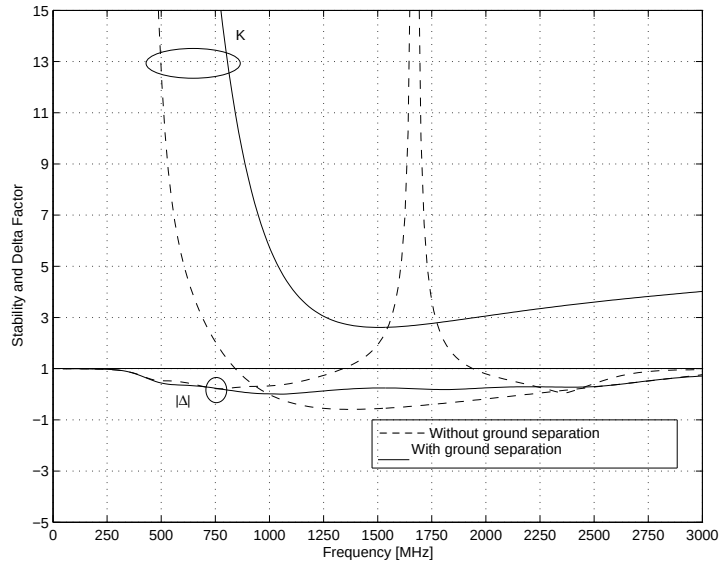

Figure 4.6: Simulated stability factor with and without ground separation technique.

– Unconditionally stable:

$$||c_s| - r_s| > 1 \text{ for } |S_{22}| < 1 \tag{4.6}$$

$$||c_l| - r_l| > 1 \text{ for } |S_{11}| < 1 \tag{4.7}$$

– Conditionally stable:

$$||c_s| - r_s| < 1 \text{ for } |S_{22}| < 1 \tag{4.8}$$

$$||c_l| - r_l| < 1 \text{ for } |S_{11}| < 1 \tag{4.9}$$

- Unstable (potentially): $K > 1$ & $|\Delta| > 1$ and $K < 1$ & $|\Delta| < 1$,

where c_s, c_l, r_s, and r_l parameters represent the center and radius of the source and load stability circles respectively.

Simulations show that about $21\,\Omega$ resistance between GND1 and GND2 is enough to sufficiently isolate them from each other. In the $0.25\,\mu$m CMOS process, the substrate resistivity (R) is $20\,\Omega \cdot$ cm and the substrate thickness (T) is 29 mils. The substrate resistance between GND1 and GND2 can be roughly estimated using the formula:

$$R_{Sub} = R[\Omega \cdot \mathrm{m}] \times \frac{d[\mathrm{m}]}{A[\mathrm{m}^2]}, \tag{4.10}$$

where the substrate distance (d) between the GND1 and GND2 is approximately $130\,\mu$m (See Figure 4.4) and the substrate cross-section area (A) can be found as follow:

$$A = T[\mathrm{m}] \times W[\mathrm{m}] = 335.15 \times 10^{-9}\mathrm{m}^2, \tag{4.11}$$

where the chip width (W) is $455\,\mu$m. Using Eq. (4.10), the resistance (R_{Sub}) between GND1 and GND2 is roughly estimated to $77.6\,\Omega$, which is much larger than the $21\,\Omega$ which is needed. This means that the simple calculation is sufficient in this case, and that there will be no problem to achieve the isolation.

4.3 Simulation and Measurement Results

The simulations were performed with Agilent-ADS and MATLAB simulation tools. The CMOS power amplifier was tested using chip on board assembly. The amplifier is characterized by small signal S-parameters, 1-dB compression point, OIP3 (Third order output intercept point), ACLR, and EVM parameters. Since Class-A and Class-AB amplifiers are weakly nonlinear systems, small signal S-parameters characterization and then 1-dB compression, OIP3, ACLR, and EVM characterization for linearity still is a reasonable approach.

The small signal S-parameters are measured with Agilent Vector Network Analyzer. The absolute power levels are measured with Boonton Power Meter. All cable and connector losses are calibrated before the measurements. Relative power levels, OIP3, ACLR, and EVM parameters are measured with Rohde & Schwarz spectrum analyzer, signal generator, and CMU200 radio and communication tester.

For MOSFET simulation, the BSIM3v3 RF Extension Model was used. The simulation and measurement results are presented in the following sections. Experiments are performed according to fixed and dynamic supply scenarios. Test boards are illustrated in Figure 4.7.

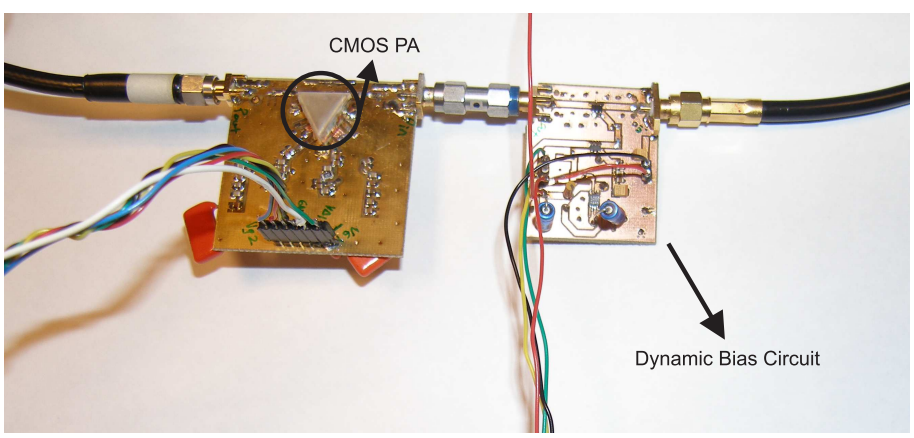

Figure 4.7: CMOS power amplifier and dynamic supply test boards.

4.3.1 Transfer Characteristics

The measured and simulated forward and reverse gain characteristics ($|S_{21}|$ & $|S_{12}|$) and input and output reflection characteristics ($|S_{11}|$ & $|S_{22}|$) of the PA are shown in Figures 4.8 and 4.9. In Table 4.1, some measured values in the GSM-EDGE band are listed.

Table 4.1: Measured S-parameters in the GSM-EDGE Band.

Freq. [MHz]	$\|S_{21}\|$ dB	$\|S_{11}\|$ dB	$\|S_{22}\|$ dB
1700	12.3	−21.46	−20.16
1750	11.75	−19.7	−16.18
1800	11	−17.2	−12.57

While the simulated gain is 14.2 dB at 1.75 GHz, the measured gain is only 11.75 dB. Differences between simulation and measurement results are due to imperfections of parasitic models used in simulations, on-chip and off-chip component tolerances, and also measurement inaccuracy.

4.3.2 Efficiency

A. Efficiency with Constant Bias:

The measured 1-dB compression point at 1700MHz is 20.2 dBm, and the corresponding power added efficiency is 28.2%. The amplifier draws 137 mA current from the 2.5 V supply voltage at the maximum output power. The measured 1-dB compression point at 1750MHz is 19.87 dBm, and the corresponding power added efficiency is 26.5% with 133.8 mA current consumption. It is 19.93 dBm, and the corresponding power added efficiency is 27.2% with 130 mA current consumption at 1800MHz.

The simulated 1-dB compression point is found as 20.92 dBm at 1750MHz, and the simulated PAE and current consumption are found as 30.88% and 156 mA. Figure 4.10 shows a plot of PAE vs. output power at 1750MHz.

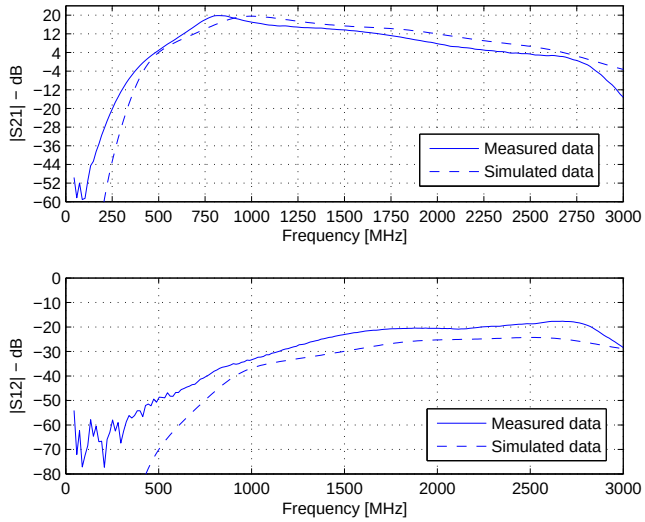

Figure 4.8: Simulated and measured forward and reverse gain characteristics.

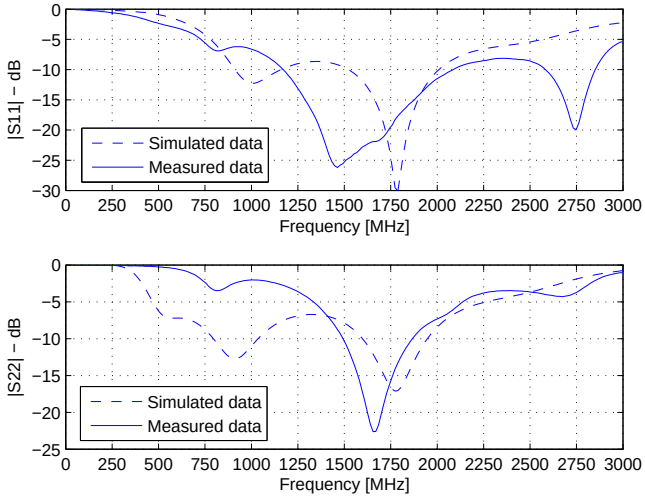

Figure 4.9: Simulated and measured input and output reflection characteristics.

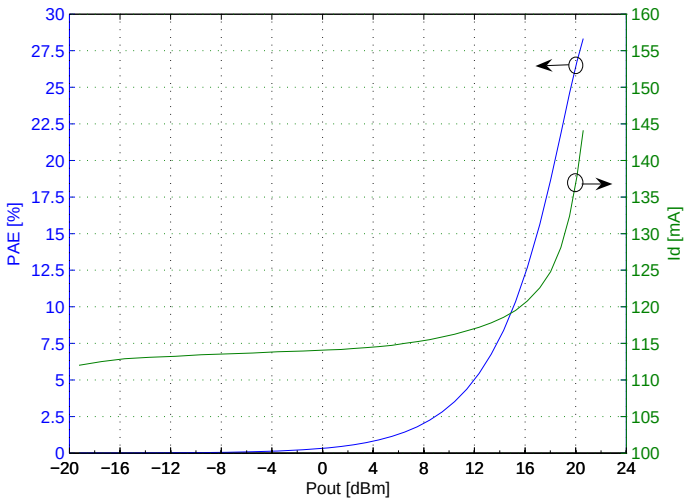

Figure 4.10: Measured power added efficiency and supply current at 1750 MHz.

B. Efficiency with Dynamic Bias:

Adaptive biasing technique is similar to Kahn envelope elimination and restoration technique. EER technique combines a highly efficient, but nonlinear RF PA with a highly efficient envelope amplifier to implement a high efficiency linear RF PA [53]. In adaptive biasing (envelope tracking) technique, the supply voltage is varied dynamically to conserve power, but with sufficient excess to allow the RF PA to operate in a linear mode [53].

The envelope of the input RF signal is detected and used to control a dc-dc converter. In Figure 4.11, an adaptive biasing architecture is shown. DC-DC step down converter and the RF power detector are the commercial off-the-self (COTS) components from Linear Technology [6, 11]. The 18 dB directional coupler is from Mini-Circuits [16]. The DC-DC converter switching frequency is 1.5 MHz which is quite bigger than the bandwidth of the EDGE signal. Therefore there will not be any problem for the pulse width modulator to follow the envelope of the EDGE signal.

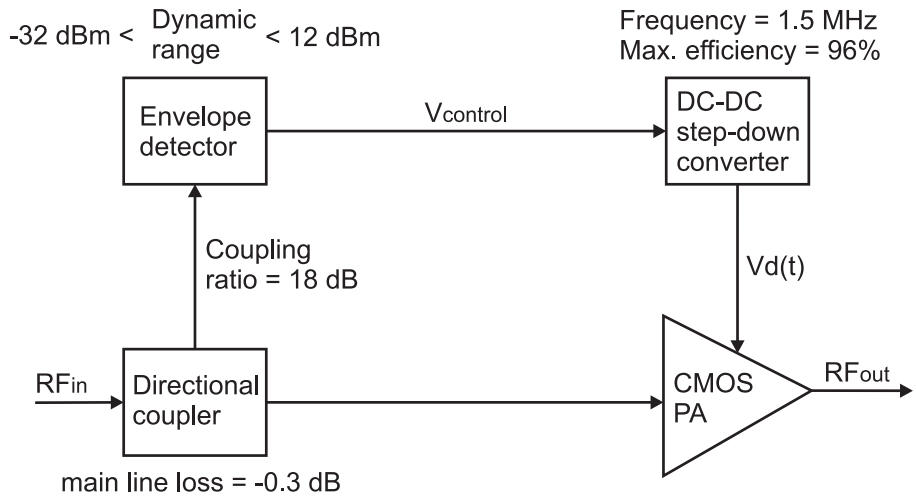

Figure 4.11: Adaptive biasing architecture.

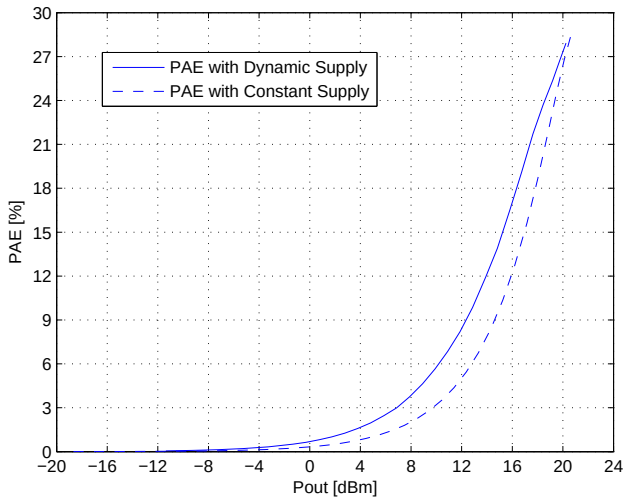

Figure 4.12: Measured power added efficiency with and without adaptive biasing at 1750 MHz.

In Figure 4.12, power added efficiency with adaptive biasing is compared to the PAE without adaptive biasing. From Figure 4.12 it is clear that the amplifier effi-

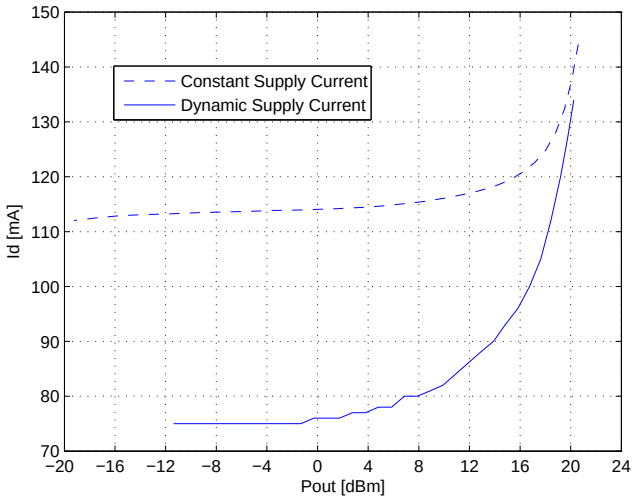

Figure 4.13: Measured supply current at 1750 MHz with and without dynamic supply.

ciency can be improved reasonably using the adaptive biasing technique. Efficiency improvement is largest at low to mid-power ranges. At maximum power, however, the efficiency is a bit reduced due to the DC-DC converter losses. The estimated density for the WCDMA FDD uplink output power is found in Figure 4.14 for a load of 49 users/cell and frequency. According to the probability distribution of the user equipment transmit power levels, Figure 4.14, medium transmit power levels are the most frequently used. The probability distribution of the UE transmit power levels can be expected as similar in GSM-EDGE and the other wireless cellular systems.

Improving the efficiency at mid-power is therefore critical to battery life-time. In this amplifier $3 - 4\%$ improvement is obtained at mid power ranges with adaptive biasing. The quiescent current of the amplifier is 120 mA under 2.5 V supply voltage. It is about 88 mA with adaptive biasing. DC currents drawn by constant supply and dynamic supply are compared in Figure 4.13. Since the dynamic range of the power detector is limited with minimum -32 dBm, the supply current could not measured below some power levels in adaptive biasing scenario (See Figure 4.13).

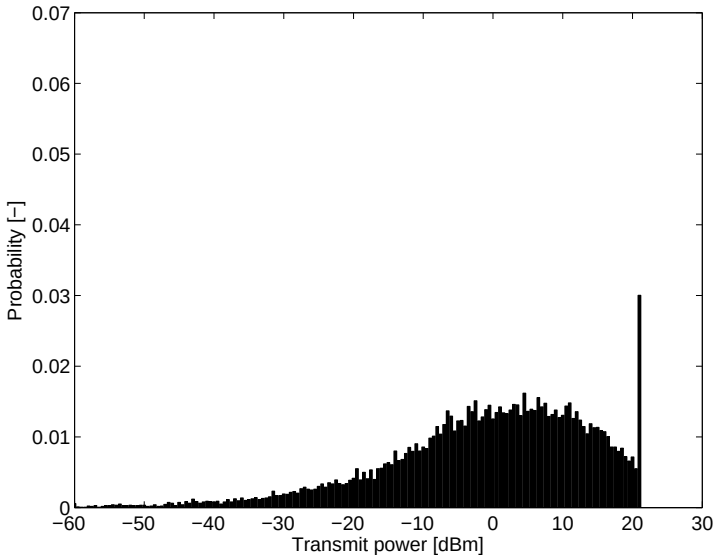

Figure 4.14: W-CDMA uplink UE power density.

4.3.3 Linearity

The linearity performance of the amplifier was analyzed according to the GSM-EDGE user equipment requirements [3]. Third order output intercept point, ACLR, and EVM measurements are performed.

For two-tone measurement the frequencies (tones) are set at $f_c \pm 500$ kHz. The measured third order intercept points are 33.14 dBm, 33.08 dBm, and 31.03 dBm for 1700 MHz, 1750 MHz, and 1800 MHz center frequencies. Measured 1-dB compression point, power added efficiency, and output third order intercept point values for certain frequencies are listed in Table 4.2.

The measured average burst power is 19.8 dBm, and the measured peak burst power is 21.7 dBm. The measured spectral mask at this power level and 1750 MHz frequency with 400 kHz offset is −58.9 dB. The measured RMS and peak EVM is 6.4 and 16.2 respectively. According to GSM-EDGE standards, the spectrum mask has to be better than −54 dB, the RMS and peak EVM values have to be better than 9% and 30%

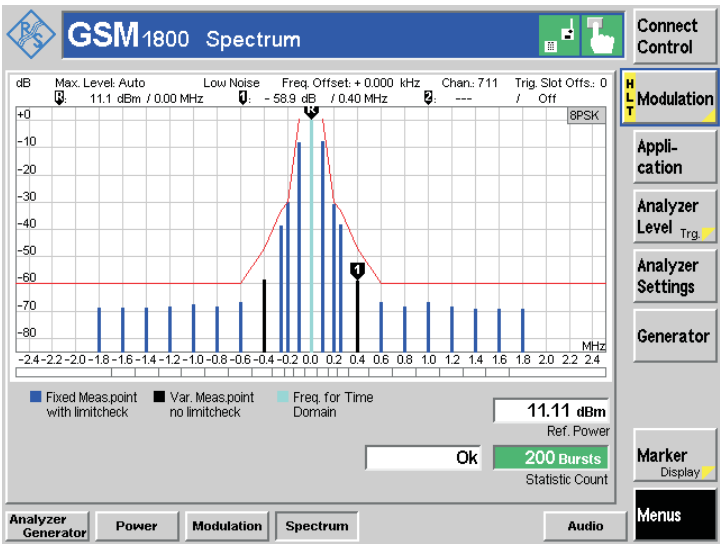

Figure 4.15: Measured spectrum mask at 1750 MHz

Table 4.2: Measured spectrum characteristics for selected frequencies.

Freq [MHz]	$P1dB$ [dBm]	I_d [mA]	PAE [%]	OIP3 [dBm]
1700	20.2	137	28.2	33.14
1750	19.87	133.8	26.5	33.08
1800	19.93	130	27.2	31.03

respectively [3]. In Figures 4.15, 4.16, and 4.17 the spectral mask measurement, and EVM measurements are illustrated.

In Figures 4.18, and 4.19, the spectral mask measurement, and EVM measurements are compared based on constant and dynamic supply cases. As expected, the linearity performance of the amplifier with constant supply is better than that of amplifier with dynamic supply. However, according to the GSM-EDGE user equipment technical specifications [3], the spectrum mask and EVM requirements are satisfied with both constant and dynamic supply scenarios.

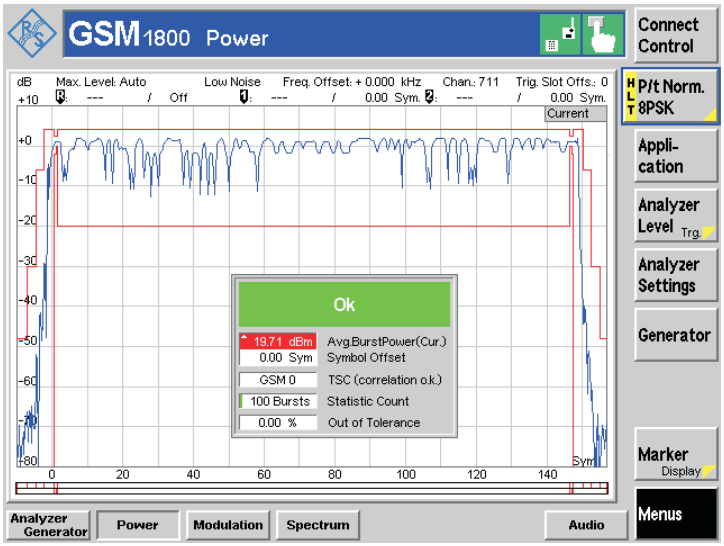

Figure 4.16: Measured power spectrum at 1750 MHz

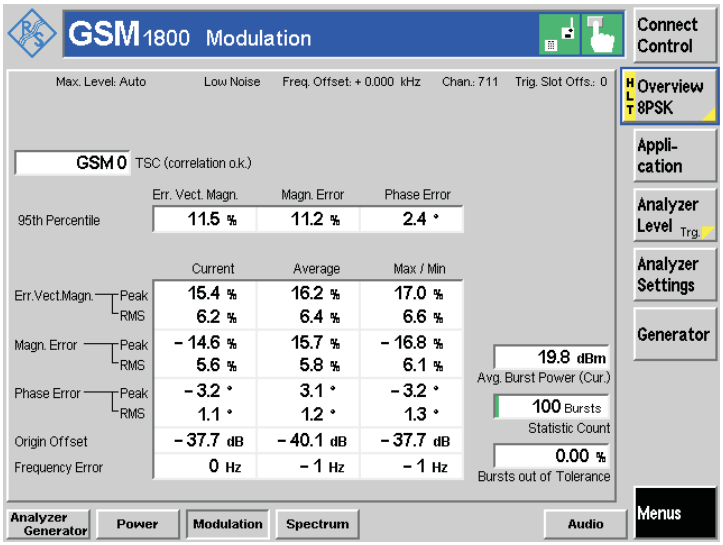

Figure 4.17: Measured EVM performance

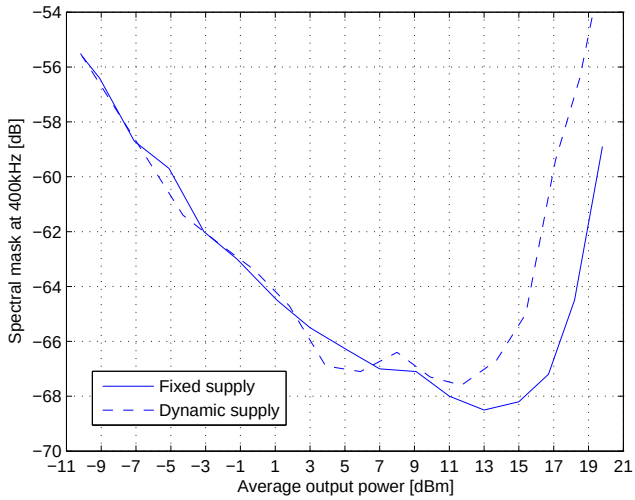

Figure 4.18: Spectrum mask is compared based on constant and dynamic supply cases.

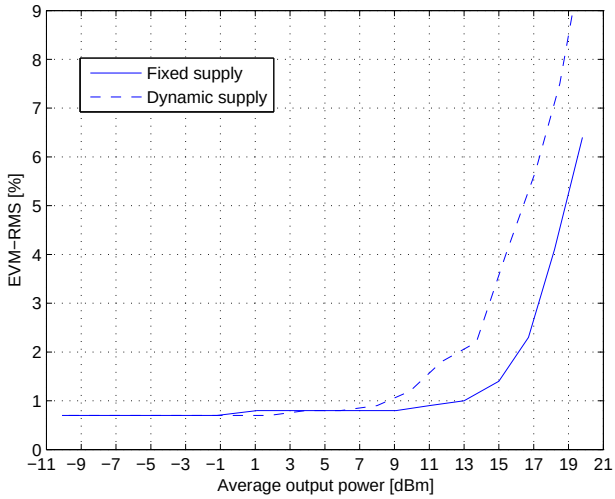

Figure 4.19: RMS-EVM is compared based on constant and dynamic supply cases.

4.4 Discussions

The power amplifier design for modern digital modulations with high spectral efficiency is usually constrained by linearity requirements at the maximum power output, regardless of the average power transmitted by the radio terminal. As a result, the quiescent bias of the amplifier is set for maximum linear power and DC power is wasted at lower output power levels. To overcome this problem, an adaptive biasing approach can be employed, significantly reducing the average DC current and, thereby increasing the power added efficiency.

This work shows that adaptive biasing technique can significantly improve the amplifier's efficiency in mid power ranges, on the other hand there will be slight reductions on the maximum power efficiency because of the DC-DC converter losses (dominantly).

To even improve the linearity, efficiency, and maximum output power trade-off in power amplifiers, parallel amplification technique can be combined with adaptive biasing technique, i.e. two CMOS Class-AB amplifiers can be combined by power splitter/combiner and the supply voltages dynamically controlled by the DC-DC converter. This architecture can be called as "Turbo Class-AB Amplifier". In this way, first, the output power level can be increased approximately 3 dB, secondly, the linearity of the Turbo class-AB amplifier is 3 dB backed off the single class-AB amplifier (i.e. the linearity performance of Turbo class-AB amplifier at 20 dBm will be same as it in 17 dBm output power in single class-AB amplifier.), and lastly, the efficiency of Turbo class-AB amplifier is expected to be same as the efficiency of single class-AB amplifier.

In this work it is also demonstrated that the ground separation technique improves the amplifier's stability and performance. The inductance of the ground bondwires is one of the most serious problems in single-ended integrated amplifier design. The inductance creates parasitic feedback which can cause the amplifier to self-oscillate. This feedback path can be broken using the ground separation technique, and consequently amplifier's stability and performance can be improved.

As a future work, the linearity performance of the amplifier can be investigated according to with and without ground separation technique. How the geometrical arrangement of the amplifier's layout and stages affect the stability and performance. The answer of this question also might be investigated as a future work.

Chapter 5

Conclusion

This work concentrates on investigation of multi-hop cellular network functionality and designing linear power amplifiers which will be the critical part for efficient multi-hop cellular networks.

In this work it is shown that multi-hop can be introduced into a WCDMA-FDD cellular system with small changes. Investigations show that the multi-hop achieves lower transmit powers for user equipments by splitting the transmission into several hops.

According to uplink outage simulation results, the multi-hop system performance is better than the reference system (direct communication system) performance for an ACLR of 90 dB or higher. Uplink power distribution results also show that repeated users average transmit power is 3 dB less than reference case and signal power is distributed more evenly and over a larger range when using repeaters. These new requirements are reflected to RF parts as a need for a highly linear power amplifier with a wide power control range and sharp transmit/receive filter.

Linear power amplifiers in CMOS, however, generally have much lower efficiency at linear output power. This work concentrates on CMOS Class-AB amplifiers with adaptive biasing scenario. Several CMOS Class-AB amplifier designs have been published during this work and their power added efficiencies are measured from about 17% to 28% at 1-dB compression points. The power amplifiers deliver reasonable output powers with good linearity characteristics.

In this work it is also shown that the power amplifier efficiency can be improved at mid-power ranges by dynamically biasing the amplifier with slightly reduction on the PAE at 1-dB compression point. The idea is to adapt the supply voltage to the envelope of the input signal. In this way, the average DC current is reduced and thereby the power amplifier's PAE is improved at mid-power ranges.

This work also demonstrates that using on-chip ground separation technique improves the stability and performance of the amplifier. The inductance of the ground bondwires is one of the most serious problems in single ended integrated amplifier design. Any parasitic feedback paths between stages via ground bondwire inductance can be broken using the on-chip ground separation technique, and consequently amplifier's stability and performance can be improved.

Appendix A

RF Requirements for Multi-Hop Cellular Network Repeaters

A

Published in the Proceedings of IEEE Norchip Conference, Oslo, November 2005. Authors are Robert S. Karlsson, Huseyin Aniktar, Torben Larsen, and Jan H. Mikkelsen.

RF Requirements for Multi-hop Cellular Network Repeaters

Robert S. Karlsson, Huseyin Aniktar, Torben Larsen, and Jan H. Mikkelsen

RISC Division, Center for TeleInFrastructure (CTIF),
Aalborg University, Niels Jernes Vej 12, 9220 Aalborg East, Denmark
E-mail: risc@kom.aau.dk

Abstract

Multi-hop cellular networks are currently being explored for use in future generation cellular networks. This paper is a step towards identifying overall system requirements for the radio frequency (RF) part of terminals for such multi-hop cellular networks. Multi-hop cellular networks offer trade-offs between coverage, capacity and power consumption. Multi-hop networks are also expected to place new requirements on the RF parts of the transceivers of both repeating and mobile devices. In this paper, a set of system requirements are derived for multi-hop enabled RF front-ends. For this purpose, the uplink transmit power distributions and the uplink outage performance for multi-hop networks are investigated. According to simulation results, some RF requirements have been identi ed in both transmitter and receiver sections.

1. Introduction

Existing cellular systems suffer from interference problems related to the centralized nature of the radio communication [1]. Typically, within a cell there are several user equipments (UEs) that are all communicating with the same base station (BS). As these UEs are likely to experience greatly differing propagation losses in the radio transmission, they are forced to use transmission power levels with a similar variance. This is the root of the so-called near-far problem where UEs near a BS may interfere with communication between the BS and UEs further away. In multi-hop cellular networks (MCN), communication is not established directly between the UE and the BS [2]. Instead, intermediate devices act as repeaters between the BS and a UE. Using multiple hops in a cellular system is one way to decrease the total required transmission power and possibly mitigate interference and coverage problems. Reductions in transmission power decrease the power consumption in the UE; this increases the time between battery recharges. MCNs can also provide service in 'dead spots' in a cell, which are not reachable by the BS in a single hop. Reducing the transmission power in MCNs would be bene cial also for medical reasons.

2. System Model

To investigate the resulting RF requirements a system model suitable for analyzing multi-hop networks is introduced. The adopted model has been chosen to re ect an urban high traf- c scenario and is taken from 3GPP Radio Frequency Systems Scenarios with some additions necessary to model the multi-hop functionality [3]. The model parameters are summarized in Table 1. In the model, the repeater can act as a UE towards the BS and as a BS towards the UE. The method is depicted in Figure 1.

Table 1: System parameters [3, 4, 5].

PARAMETER	VALUE
Site to site distance	1000 m
User bit rate	12200 bit/s
Chip rate	3.84 Mchip/s
Processing gain	3840/12.2
Noise factor UEs	9 dB
Noise factor BS	5 dB
Noise factor repeater (for both frequencies)	9 dB
Maximum UE output power	125 mW
Maximum BS output power	20 W
BS output power used for common channels (20(%) of maximum)	4 W
Maximum repeater output power toward BS	500 mW
Maximum repeater output power toward UEs	500 mW
SIR target in UE (downlink)	7.9 dB
SIR target in BS (uplink)	6.1 dB
SIR target in repeater (from UE uplink)	6.1 dB
ACLR when UE transmits	33 dB
ACLR when BS transmits	45 dB
Antenna gain in BS	11 dB
Antenna gain in repeater	0 dB
Antenna gain in UE	0 dB
Downlink orthogonality factor	0.4
MCL between repeaters	45 dB
MCL between repeater and UE	45 dB
MCL between BS and repeater	53 dB
MCL between BS and UE	53 dB
Repeater distance from BS 1	375 m

2.1. Network Layout

The network simulation model assumes a WCDMA FDD system with 19 macro base stations placed in a hexagonal pattern. The network layout is illustrated in Figure 2. The frequency bands are 1930-1935 and 2120-2125 MHz for pair one (FB1), and 1935-1940 and 2125-2130 MHz for pair two (FB2). Center frequencies are 1932.4, 2122.4, 1937.4 and 2127.4 MHz respectively (see Figure 1). Six xed repeaters are placed in the center cell hosted by BS one. A reference case is also investigated by using the same system set-up as described above but without the repeaters. All BSs in the system are allowed to use both frequency bands. The communication between BS one and any one of the repeaters is located on FB1 and the communication between repeaters and repeated UEs is located on FB2. To avoid border ef-

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fects in the macro network a wrap-around technique is used. Wrap-around implies that any user that crosses the edge of the macro-network is re-entered in the corresponding cell on the opposite edge.

2.2. Propagation Model

The propagation models suggested in [6] are used, and the relevant parameters are summarized in Table 2. Four different types of propagation models are needed in this multi-hop scenario:

a) Between a BS and a UE.

b) Between a BS and a repeater.

c) Between a repeater and a UE.

d) Between repeaters.

For cases (a) and (b), the COST-Hata-Model is used [6]. This model is suitable for outdoor urban areas where one of the antennas is placed above the roof top level. For cases (c) and (d), the COST-Wal sch-Ikegami-Model is used [6]. This model is suitable for non-line-of-sight scenarios where both antennas are placed below roof top level.

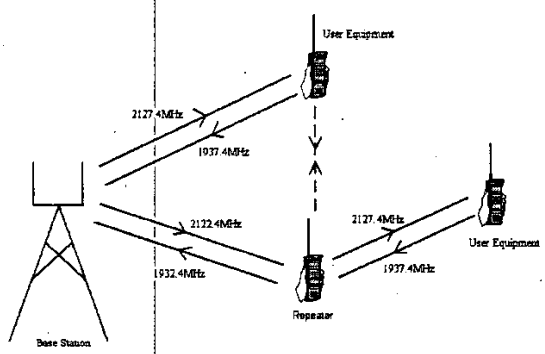

Figure 1: Multi-hop system where the repeater acts as an UE towards BS, and as a BS towards the UE. Transmission path (solid) and interference (dashed).

Table 2: Propagation parameters [3, 6].

PARAMETER	VALUE
Frequency	2000 MHz
Repeater antenna height	4 m
UE antenna height	1.5 m
Height of buildings	15 m
Width of roads	15 m
Building separation	90 m
Street orientation with respect to direct path	90°
Base station antenna height	30 m
Standard deviation of shadow fading	6 dB
Shadow fading spatial correlation distance (Where correlation is equal to 1/e)	110 m
Shadow fading BS/repeater correlation	0.5

2.3. Adjacent Channel Leakage Ratio

The adjacent channel leakage power ratio (ACLR) is the ratio of the Root-Raised Cosine (RRC) ltered mean power centered on the assigned channel frequency to the RRC l-tered mean power centered on the adjacent channel frequency

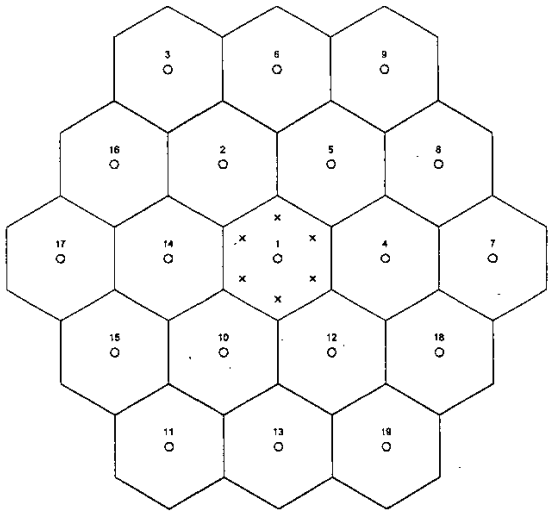

Figure 2: The network layout. Macro BSs are indicated by 'o' and repeaters with 'x'. The site to site distance is 1000 meters.

[5]. A high ACLR results from high linearity of the transmitter. Usually the requirements for the ACLR are lower in the UEs than in the BSs as a result of cost, power consumption, and form factor trade-offs. In simulation scenario there is severe interference in the repeaters due to the transmissions on adjacent channels. The system performance is investigated for some different values of ACLR in the repeaters, while ACLR of 45dB [5] for the BSs and ACLR of 33dB [4] for the UEs are used.

3. Results

Based on the model presented in section 2, a number of Monte Carlo simulations are performed. First, the uplink outage performance for some different values of repeater ACLR is investigated. If there are many links to a receiver, or when the path gain is low in one or more links, some links might end up using the maximum transmit power and thus not reaching the target SIR; they are in outage. After to get uplink outage performance, uplink power distribution performance is investigated. In Figures 3 and 4, "repUE" is used to indicate repeated users, "Ref" indicates the reference case without repeaters, and "a75", "a80", "a90" indicate ACLRs of 75 dB, 80 dB and 90 dB respectively. In Figure 3 the 95% con dence interval is indicated for the 'repUE a80' case. As the con dence intervals in the other cases are similar for similar outage they are not included. Each simulation point consists of at least 1000 independent snapshots. A snapshot is a randomly chosen time interval that is long enough to let the power control converge but short enough to ensure that the large scale propagation does not change.

3.1. Uplink Outage

In Figure 3 the uplink outage versus the load for the multi-hop system is shown together with the reference case without repeaters. The results are presented for some values of the ACLR that gave outage levels in the interesting range between 0.1% and 10%. Based on Figure 3 the outage for the repeated users is seen to decrease when the ACLR increases.

It is seen that the outage for the repeated users is higher than for the reference case except for ACLR values of 90 dB or higher (The outage for an ACLR of 200 dB -ideal case was zero for this range of loads).

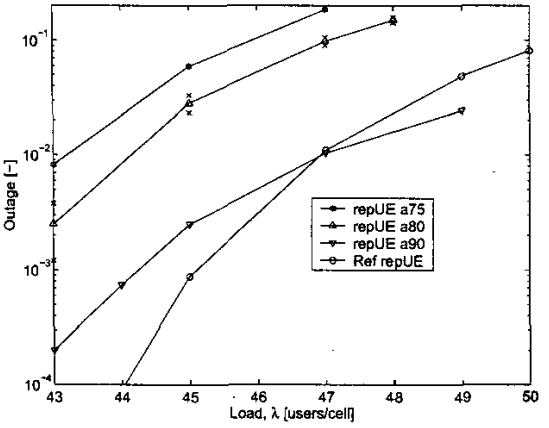

Figure 3: Uplink outage for the repeated UEs vs load. 95% confidence interval is shown for repUE a80.

3.2. Uplink Power Distributions

In Figure 4 the CDF (Cumulative Distribution Function) of the repeated UEs is illustrated together with the CDF for the same UE's when no repeaters are included. In this gure, repeated UEs transmission powers are compared to the transmission powers of the same UEs in the reference case without repeaters. The results are based on a load of 49 users/cell and an ACLR of 90dB. Clearly the repeated users operate at much lower transmission power levels than the same UEs in the reference case without repeaters.

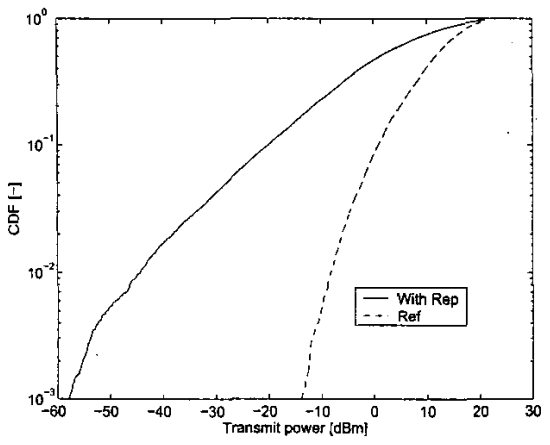

Figure 4: Uplink UE power CDF of repeated UEs. A load of 49 users/cell is used and the ACLR is set to 90 dB.

The estimated density of the repeated UEs is seen in Figure 5. There is a high probability of nding users in the highest bin (at 21dBm). This is because of the UEs that are in outage and end up using the maximum transmission power (125mW). The average power, in linear scale, is 13.2mW. The estimated density for the same UEs in the reference case without repeaters is shown in Figure 6. For the same load

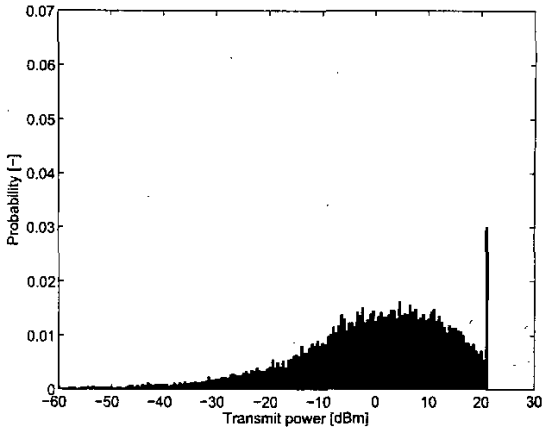

Figure 5: Uplink UE power density for repeated users. Load is 49 users/cell and the ACLR is 90 dB.

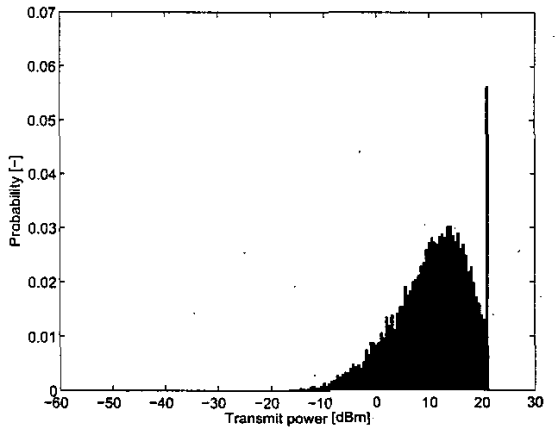

Figure 6: Uplink UE power density for reference (without repeater). Load was 49 users/cell, and ACLR was 90 dB.

and ACLR, the outage is higher than for the case with repeaters (see Figure 3), and thus the peak at 21dBm is lower in Figure 5 than in Figure 6. The average power, in linear scale, is found to 28.6mW. Thus, approximately 3dB is saved for the repeated users at this load and ACLR. Compared to the reference case it can also be seen that the signal power is distributed more evenly and over a larger range when using repeaters. The estimated density for the repeater uplink output power is found in Figure 7 for 49 users/cell and ACLR of 90dB. The average repeater power was 96.2mW. In Figure 8 the CDF of the repeated UEs with and without repeaters is illustrated for a load of 47 users/cell and an ACLR of 90 dB. As expected it is very similar to Figure 4 but shifted to the left (towards lower powers) in comparison to the load 49 users/cell. The average power for the repeated users is found to 6.6 mW (8.2 dBm), and for the repeated users without the repeaters it is found to 10.8 mW (10.3 dBm). Similar results were achieved for other loads and ACLRs.

4. Discussion

According to the uplink outage performance results the system performance is highly dependent on the ACLR perfor-

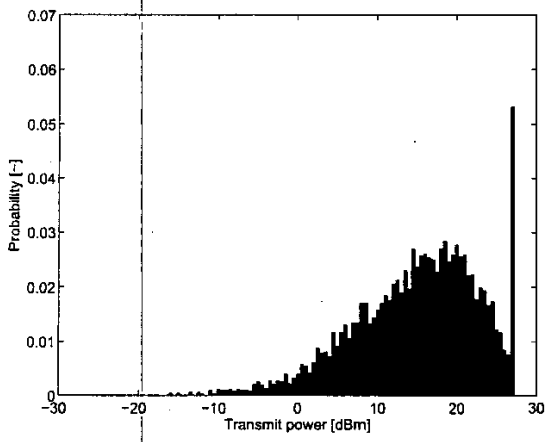

Figure 7: Uplink repeater power density. Load is 49 users/cell and the ACLR is 90 dB.

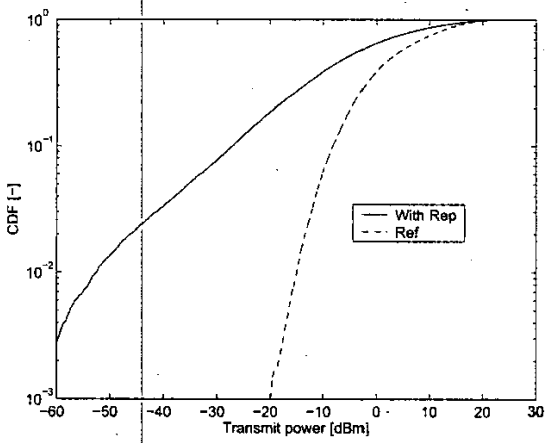

Figure 8: Uplink UE power CDF of repeated UEs. A load of 47 users/cell is used and the ACLR is set to 90 dB.

mance of the repeaters. For 49 users/cell and a 90 dB ACLR the uplink outage performance of the multi-hop system is 2.5%-point better than the reference system performance. In the transmitter section the ACLR performance depends on especially the power ampli er (PA) linearity and transmit lter characteristics. In the receiver section, ACLR depends mainly on receiver lter characteristic. Another problem for the repeaters is the self-blocking performance - that is the ability to receive a low power signal while at the same time transmitting a high power signal in an adjacent frequency band. This might also require xed sharp RF lters which could make these systems unable to exibly change frequency in the areas with multi-hop capability. It is found that the average transmission power for multi-hop systems is reduced compared to a reference system where no repeaters are used. In the multi-hop system, approximately 3 dB of transmit power is saved for the repeated users. The average transmit power is 11.2 dBm for multi-hop systems while the same value is 14.6 dBm for the reference system. It is also found that the transmit powers are spread over a large power range when using repeaters. These results also place new requirements on PA design besides the high linearity requirement. A wider power control range may be needed and a highly accurate power control could also be required for multi-hop cellular systems. In PA design there are a number of trade-offs between high power ef ciency, high linearity, load tolerance and low cost/high integration. Meeting the high ACLR requirements over a wide power control range without reducing the power ef ciency clearly represents a challenging issue in PA design for multi-hop systems. Filter design is another challenging issue for multi-hop system because of the high ACLR/selectivity requirement. To meet a ACLR of 90 dB or higher in the lter design, high Q elements are needed. That speci cation might be also achieved by only xed sharp lters or some new technologies like RF MEMS (Micro Electro-Mechanical Systems), BAW (Bulk Acoustic Wave) or SAW (Surface Acoustic Wave) technologies. So lter design is the other important issue for multi-hop systems. Available technology sets limits to the ACLR; State of the art today can reach values of approximately 77 dB for a peak output power of +30dBm [7].

5. Conclusions

In this paper, RF requirements for multi-hop cellular networks have been investigated. For this purpose, some simulations have been performed to nd uplink transmit power distributions and outage performance. Based on simulation results new RF requirements have been identi ed in both transmitter and receiver sections. These requirements specifically relate to ACLR and power control range characteristics. According to uplink outage results, multi-hop system performance is 2.5%-point better than the reference system performance for an ACLR of 90 dB or higher. Uplink power distribution results also show that repeated users average transmit power is 3 dB less than reference case and signal power is distributed more evenly and over a larger range when using repeaters. These new requirements are re ected to RF parts as a need for a highly linear PA with a wide power control range and sharp transmit/receive lter. Furthermore, PAs in MCNs have a higher dynamic range according to the reference case. This, can be illustrated with a relatively at probability distribution, means that high PA ef ciency is needed.

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AALBORG UNIVERSITET

Institut for Elektroniske Systemer
Fredrik Bajers Vej 7
9220 Aalborg Øst
Tlf. 9635 8600
Fax 9815 3662

Co-author statement

With reference to executive order no. 114 regarding the PhD degree §14, article 3, statements from each author about the PhD student's part in the shared work must be included in case the thesis is based on already published articles.

Paper title:	*"RF Requirements for Multi-Hop Cellular Network Repeaters"*
Place of publication:	*IEEE Norchip Conference, Oslo, Norway, November, 2004*
List of authors:	*R. Karlsson, H. Aniktar, J.H. Mikkelsen, and T. Larsen*
PhD student:	*H. Aniktar*
Cpr.nr:	*100777-3559*
Contribution [%, text]:	*R.S. Karlsson: 40%* *H. Aniktar: 20%* *J.H. Mikkelsen: 20%* *T. Larsen: 20%*

R. S. Karlsson is the originator and the main contributor of the paper. H. Aniktar has participated in discussions, data processing, editing and reviewing phases. Main contribution of the paper is the identification of RF requirements for multihop functionality.

R. S. Karlsson	H. Aniktar	J. H. Mikkelsen	T. Larsen

Appendix B

Performance of a WCDMA FDD Cellular Multihop Network

B

Published in the Proceedings of IEEE International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC), Berlin, September 2005. Authors are Robert S. Karlsson, Huseyin Aniktar, Torben Larsen, and Jan H. Mikkelsen.

Performance of a WCDMA FDD Cellular Multihop Network

Robert S. Karlsson, Huseyin Aniktar, Jan H. Mikkelsen, Torben Larsen

Abstract— **Cellular multihop networks has the potential to decrease power consumption, increase coverage and/or enable higher data rates. We propose using in-band transmissions for the connection between a fixed repeating device and the cellular base station. A user connected via the repeater use one frequency band (fq2) for the communication to the repeater and the repeater uses an adjacent frequency band (fq1) for the communication to the base station. There is strong interference in the repeater due to transmitting and receiving on adjacent frequency bands, and strong interference from users connected directly to the base station on fq2. We demonstrate that the method can be used to introduce multihop functionality into a WCDMA FDD cellular system with only small changes. In a pessimistic scenario repeated users can lower their transmit power, but others have to increase their power. The multihop system requires no extra frequency spectrum but it has a small capacity penalty, and it requires a high adjacent channel leakage ratio in the repeaters. The results are reasonable for this pessimistic study and suggest further studies of alternative scenarios to improve the performance.**

I. INTRODUCTION

IN multihop systems communication is not directly from user equipment (UE) to base station (BS). Instead intermediate devices relay the communication. Cellular multiple hop systems has been suggested as a new area of research [1]. They have the potential to decrease the total required transmission power and mitigate interference and coverage problems [1-3]. Multiple hop cellular systems offer trade offs between coverage, capacity and power consumption [4]. Reduction in transmission power may be attractive for health reasons, though there are not yet any conclusive proofs of the health effects of cellular phone usage. In [2] the authors investigate Ad-Hoc functionality introduced into a cellular architecture using the IEEE 802.11 standard with packet traffic. The increased coverage of a CDMA based multihop cellular system with packet traffic was investigated in [4].

Splitting the transmissions between BSs and UEs into two or more hops increases the delay of the communication, which might not be acceptable for some services. Multihop systems can use fixed repeaters or mobile repeaters. Fixed repeaters are special devices that are placed at strategic places in the coverage area - they are assumed to be connected to a power outlet. A mobile repeater is a UE that acts as a repeater for other UEs - they run on battery power.

To keep low delays, enabling voice traffic, and to have small changes to the existing cellular system we concentrate on fixed repeaters and a maximum of two hops. Thus we do not consider Ad-hoc functionality, i.e., all connections has to go through the BSs. We study the system capacity and transmit power distribution, taking into account interference between cells, users and repeaters and also between frequency bands. The contribution in this paper is the circuit switched traffic analysis in multihop CDMA cellular systems and the in-band technique used to introduce repeating into an existing WCDMA FDD system with only small changes.

II. RADIO RESOURCES

When we split the transmissions between a UE and a BS into two hops there are four transmission directions: from the BS to the repeater, from the repeater to the UE, from the UE to the repeater, and from the repeater to the BS. To provide radio resources for these transmissions we can use

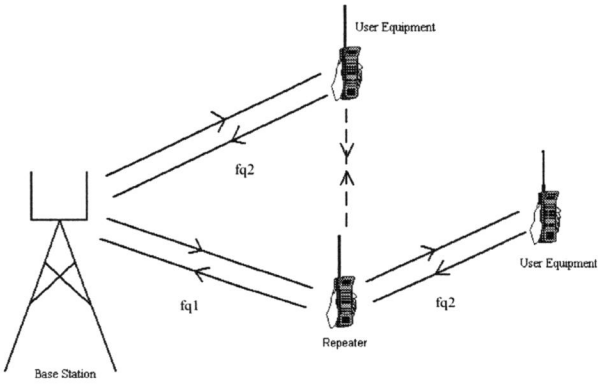

Fig. 1. Multihop system. The repeater acts as an UE towards BS, and as a BS towards UE. Intended transmission paths (solid) and interference (dashed).

This work was supported by the Danish Technical Research Council, Project number 26-03-0030.

R. S. Karlsson was with Aalborg University, Denmark. He is now with ZTE Wistron Telecom AB, Färögatan 33, SE-164 51 Kista, Sweden (e-mail: robert.karlsson@ztewistron.com).

H. Aniktar, J. H. Mikkelsen, and T. Larsen are with Department of Communication Technology, Aalborg University, DK-9220 Aalborg Ø, Denmark (e-mail: {ha, jhm, tl}@kom.aau.dk).

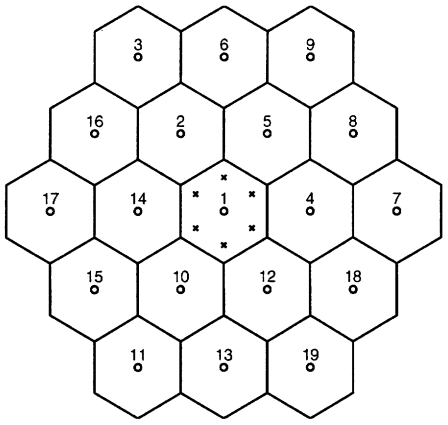

Fig. 2. Network layout. Macro base stations are indicated by o and repeaters with x. The site to site distance is 1000 meters.

three different methods: separation in time, separation in space, and separation in frequency. We concentrate on the separation in frequency as only small changes to an existing system are needed, and we will benefit from the separation in space that naturally exist in a cellular system.

We let the repeater act like a BS toward the UE and as a UE toward the BS. This means there will be strong interference between transmit and receive frequency bands in the repeater, and strong interference for the receiver in the repeater from users connected directly to the base station on frequency band fq2, see dashed line in Fig. 1. Thus we depend on the DS-CDMA systems good ability to withstand interference. This relaying system is classified as a *decode-and-forward* system in [3], it differs from the system investigated in [4] in that we consider continuous transmission instead of packet traffic and that we consider two frequency bands instead of one.

For the uplink a user connected via the repeater use one frequency band for the communication to the repeater (fq2 see Fig. 1), and the repeater uses an adjacent frequency band for the communication to the base station (fq1 see Fig. 1). Other users connected directly to the same base station can communicate on either of these two frequency bands. This method can be used in a WCDMA FDD system when the operator has access to two or more carriers (that is a minimum of 10 MHz for the uplink and 10 MHz for the downlink). The only change to an existing system, besides the repeaters, is the extra information necessary: either location information (UE positions) in the BSs or one extra measurement for the UEs to report to the BSs (one more cell in monitored set).

TABLE I KEY SYSTEM PARAMETERS

Parameter	Value
Noise factor BS	5 dB
Noise factor repeater and UE	9 dB
Maximum BS output power	20 W
BS output power used for common channels	4 W
Maximum UE output power	0.125 W
Maximum repeater output power (0.5 W in each band)	0.5 W
SIR target in BS, and in repeater (uplink)	6.1 dB
SIR target in UE, and in repeater (downlink)	7.9 dB
ACLR when UE transmits	33 dB
ACLR when BS transmits	45 dB
Antenna gain in BS	11 dB
Antenna gain in repeater and in UE	0 dB
Downlink orthogonality factor	0.4
MCL between two repeaters, and between UE and repeater	45 dB
MCL between BS and repeater, and between BS and UE	53 dB

III. SYSTEM MODELS

Here we introduce models chosen to reflect an urban high traffic scenario; the models are taken from 3GPP Radio Frequency Systems Scenarios [5] with necessary additions to model the multihop. The most important model parameters are listed in Table I. We are interested in the capacity and transmit powers, and therefore we disregard of the mobility and use independent snapshots [6] to analyze the performance. We investigate both the uplink (from the UEs to the BSs, possibly via a repeater), and the downlink. The term link is used to denote the communication from a transmitter to a receiver. Thus a user communicates with one link if it is not repeated and with two links if it is repeated.

A. Network Layout

We investigate a system with 19 hexagonal cells (site to site distance 1000 m) where six fixed repeaters are introduced in the center cell (375 m from center BS), see Fig. 2. For reference we also investigate the same system without the repeaters. The communication between BS number one and the repeaters is located on fq1, and the communication between repeaters and repeated UEs is located on fq2. All base stations in the system use both frequency bands. To avoid border effects, in the macro network, a wrap-around technique is used.

B. Propagation Models

A transmitter transmitting with power P_{tx} is received with power $G \bullet P_{tx}$ at the receiver, G is the path gain. We model the path gain as $G=\min(A_t A_r G(d) S\ ;\ 1/MCL)$, where A_t is the antenna gain at the transmitter, A_r is the antenna gain at the receiver, $G(d)$ is the distance dependent path gain, S is a shadow fading factor, and MCL is the minimum coupling loss [7] of this link.

For $G(d)$ we use the propagation models suggested in [8], the parameters are summarized in Table II. There are four different types of propagation models needed: a) Between a BS and a UE. b) Between a BS and a repeater. c) Between a repeater and a UE. d) Between a repeater and other

TABLE II PROPAGATION PARAMETERS

Parameter	Value
Frequency	2000 MHz
Repeater antenna height	4 m
UE antenna height	1.5 m
Height of buildings	15 m
Width of roads	15 m
Building separation	90 m
Street orientation with respect to direct path	90°
Base station antenna height	30 m
Standard deviation of shadow fading	6 dB
Shadow fading spatial correlation distance (where correlation is equal to 1/e)	110 m
Shadow fading BS/repeater correlation	0.5

repeaters. For a and b we use the COST-Hata-Model suitable for non-line-of-sight outdoor urban areas where one of the antennas is placed above the roof top level. Whereas for c and d we use the COST-Walfisch-Ikegami-Model of non-line-of-sight with both antennas placed below roof top level. In Fig. 3 we have plotted the distance dependent part of the path gain (assuming a co-located BS and repeater) as well as for line-of-sight (LOS, as described in [8]).

The shadow fading is assumed to be log-normal distributed [5] and we use the spatial correlation model of [9]. Moreover, the shadow fading value between a UE and different BSs/repeaters are assumed to be correlated (this model, e.g., a user that moves into the basement of a building when the path gain decreases to all BSs and repeaters).

C. Adjacent Channel Leakage Ratio

The adjacent channel leakage power ratio (ACLR) is the ratio of the Root-Raised Cosine (RRC) filtered mean power centered on the assigned channel frequency to the RRC filtered mean power centered on the adjacent channel frequency [10]. A high ACLR results from high linearity in the transmitter. In polar transmitters, a good time alignment between envelope and phase is needed for high ACLR performance. In the repeaters we will have strong interference due to the transmission and reception on adjacent channels. We investigate the performance for some different values of ACLR in the repeaters, while we use the value from [10] for the BSs and from [11] for UEs.

D. Traffic and Service Model

The number of users per cell is assumed to be Poisson distributed and uniform over the coverage area. We model the traffic (before multihop is considered) on the two frequency bands as two independent Poisson processes, each with the same average traffic load of λ (users/cell).

Every user is assigned to one BS (or to a repeater) - the selection is the one with the highest path gain. This model a scenario with handover based on the average path gain

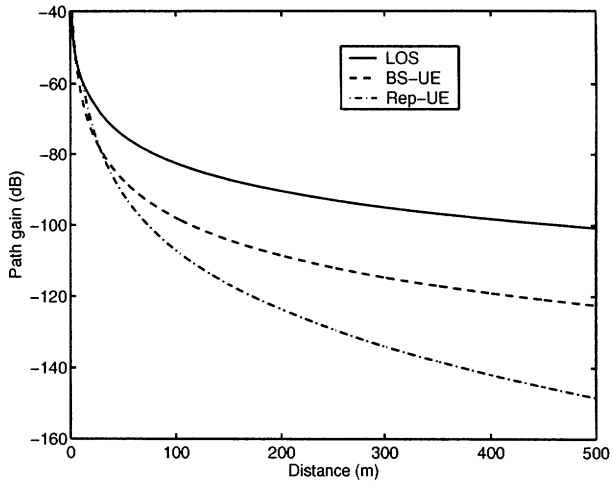

Fig. 3. Distance dependent part of path gain versus distance.

(fast fading is not considered). We do not include admission control or soft handover which could improve the performance, especially for the downlink. We assume the service to be circuit switched speech and we do not model speech activity detection.

E. Signal to Interference Ratio

We define the uplink signal to interference ratio (SIR), at the receiver of a link i, as

$$SIR_i = \frac{W}{R} \cdot \frac{G_{ii} \cdot P_i}{\sum_{j \in M_i} G_{ij} \cdot P_j + I_{ext,i} + N_i} \qquad (1)$$

where W is the chip rate (3.84 Mchip/s), R is the user bit rate (12.2 kbps), G_{ij} is the total path gain from transmitter of link j to the receiver of link i, P_j is the transmit power of the transmitter of link j, M_i is the set of links using the same frequency as link i (including the link i), and N_i is the thermal noise power at the receiver of link i. The interference power in the frequency band of link i at the receiver of link i from all links not using the same frequency as link i is $I_{ext,i}$ - we have

$$I_{ext,i} = \sum_{j \in M_i^c} G_{ij} P_j / ACLR_{ij} \qquad (2)$$

where M_i^c is the set of all links not using the same frequency band as link i, and $ACLR_{ij}$ is the ACLR from the frequency band of the transmitter of link j to the frequency band of link i. The thermal noise power at the receiver of link i is $N_i = kT_0WF_i$ where kT_0 is the noise spectral density (-174 dBm/Hz), and F_i is the noise factor of the receiver.

F. Power Control

We use the iterative Distributed Constrained Power Control [12], which decreases (increase) the transmission power when the SIR is above (below) the target SIR. We consider the powers to have converged when the maximum power change between iterations, for any link in the system, is less

than 3%. For the uplink there is a constraint on the maximum link power, while for the downlink (and in the repeaters) we have a constraint on the total output power from the BS.

G. Performance Measures

When the power control has converged, if there are many links to a receiver or when the path gain is low in one or more links, some links might end up using the maximum transmit power and thus not reaching the target SIR; they are defined to be in outage. We define the outage on band k as

$$\theta_k = \sum_{a \in M^k} X_a / (\lambda \cdot N) \tag{3}$$

where N is the number of cells (19), M^k is the set of users using frequency band k and X_a is equal to one if user a is in outage and zero else. A repeated user is counted in outage if one (or both) of the two links is in outage.

Repeated users: We also investigate the outage for the repeated users. We define the repeated outage as

$$\theta^r = \sum_{a \in M^r} X_a / |M^r| \tag{4}$$

where M^r is the set of repeated users, and $|M^r|$ is the number of repeated users.

Increasing the load gives higher outage. If we set a limit to the outage, e.g., a maximum acceptable outage of 5%, we get the maximum load, the capacity, of the system.

IV. Numerical Results

Here we present numerical result achieved with Monte Carlo simulation of the models presented in last section. As a reference case we investigate the same system but without the repeaters, and by looking at which users are repeated in the system with repeaters, we can find the performance of the same users in the case without repeaters. In the result plots we use "repUE" to indicate repeated users, "Ref" to indicate the reference case without repeaters, "a80" to indicate an ACLR of 80 dB, and "fq1" to indicate users on frequency band one, etc. Each point consists of at least 1000 independent snapshots (more for low outages).

A. Outage

In Fig. 4 we have plotted the uplink outage versus the load for the multihop system as well as for the reference case without repeaters. The results are presented for values of the ACLR that gave outage levels in the interesting range between 0.1% and 10%. The ACLR of 200 dB, in practice infinite, shows the limit of the achievable performance. For the repeated users, as expected the outage decreases when the ACLR increases (the outage for the repeated users is zero for this range of loads at an ACLR of 200 dB). The outage for the repeated users is higher than for the

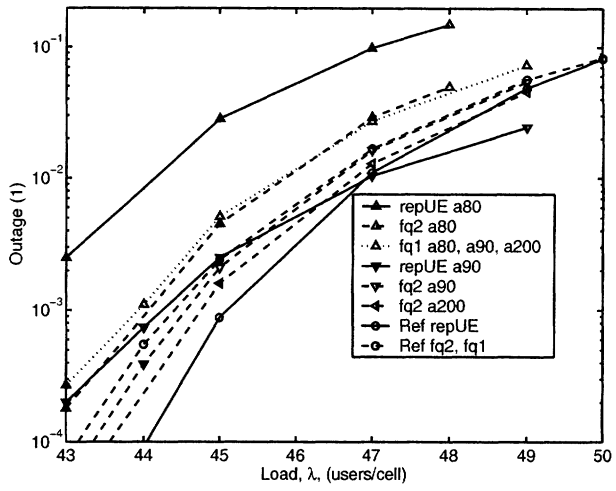

Fig. 4. Outage versus load.

reference case without repeaters, except when ACLR is 90 dB or higher. For fq1, the outage for ACLR of 80, 90, and 200 dB are all within the 95% confidence intervals of each other, therefore they are shown as one curve only. The outage for fq1 and fq2 in the reference case is also within the 95% confidence interval of each other and thus they are shown in one curve. For fq2, performance gets better as we increase the ACLR, and for an ACLR of 90 dB and above we get similar or better performance than for the case without repeaters.

The capacity at 5% outage and an ACLR of 90 dB is approx. 48.2 users/cell on each frequency band (limited by the outage on fq1), or 1.2% lower than for the case without repeaters (48.8 users/cell on each frequency band).

B. Power Distribution

Here we present estimates of the cumulative distribution functions (CDFs) and density functions of the transmission powers, for a load of 49 users/cell on each frequency band and an ACLR of 90 dB (using bins of size 0.5 dBm and normalized so that the sum over all bins is one). We compare the transmission powers of UEs that are repeated to the same UEs in the reference case without repeaters.

In Fig. 5 we have the CDF of the UE transmission powers for the repeated UEs with (solid) and without (dash dotted) repeaters. Clearly the repeated users use lower transmission powers with repeaters. The CDF for all users is also found in Fig. 5; unfortunately the system with repeaters (dotted) uses slightly higher transmission powers than the system without repeaters (dashed). This is due to the interference created by the in-band transmission for the multihop part.

The estimated probability density function of the repeated UEs we find in Fig. 6. There is a high probability of finding users in the highest bin (at 21 dBm); this is because of the UEs in outage ends up using the maximum transmission

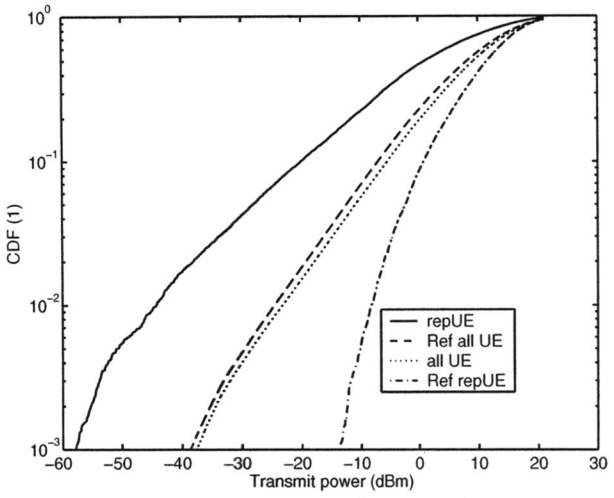

Fig. 5. Power distributions. Load 49 users/cell, ACLR 90 dB.

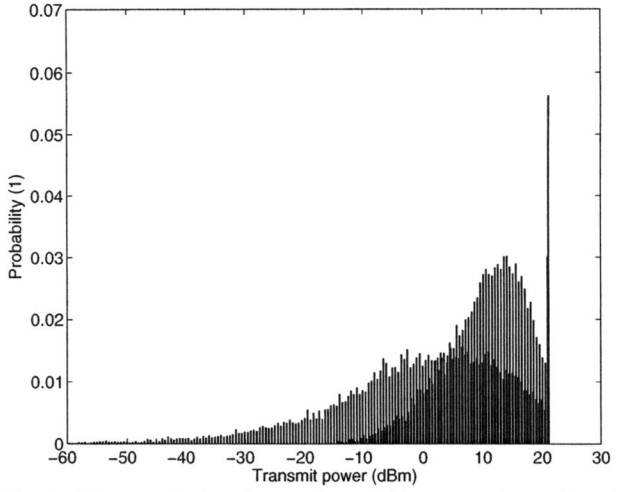

Fig. 6. UE power density of repeated users with repeater (low peak) and without repeaters (high peak). Load 49 users/cell, ACLR 90 dB.

power of 125 mW (20.97 dBm). The average power is 13.2 mW (11.2 dBm).

The estimated probability density function for the repeated UEs without repeaters we also find in Fig. 6. The average power is 28.6 mW (14.6 dBm). Thus we save approximately 3 dB for the repeated users at this load and ACLR. We can also see that the powers are more spread out with than without the repeaters.

We also studied the average power for all users in the system; it is 25.1 mW (14.0 dBm) with and 22.7 mW (13.6 dBm) without repeaters. Thus we loose 0.4 dB transmit power for the case with repeaters.

Similar results were achieved for other loads, other ACLRs and in the downlink. For the downlink there is no power loss using multihop, but the capacity penalty is higher (approximately 6.5%).

V. Conclusion

The scenario we investigated was aimed at investigating the power saving feature and capacity of multihop cellular systems. Using multihop cellular systems for coverage extensions requires a different scenario to evaluate. A scenario where multihop cellular systems are likely to show gains is when repeaters are placed in LOS from the BS and there is LOS between the repeater and the UE but not directly between the BS and the UE. Other methods to improve the performance is: removal of users in outage, multiple antennas at the repeaters, hotspot coverage by repeaters, different propagation scenarios (LOS), and inter-frequency handovers based on received quality instead of path gain to mitigate interference for UEs close to the repeaters. Thus the investigated scenario was pessimistic.

We have shown that multihop can be introduced into a WCDMA FDD cellular system with small changes. The multihop achieves lower transmit powers for repeated users, but others get increased transmission powers. There is a small capacity loss for using the proposed multihop scheme in the pessimistic scenario investigated. We showed a high required ACLR of 90 dB, this can be mitigated if the repeater has separated antennas towards BS and towards UEs. State of the art today is an ACLR of around 77 dB for a peak output power of +30 dBm [13]. We propose further studies to mitigate the high required ACLR by separating receive and transmit antennas in the repeaters, and also include a LOS scenario.

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AALBORG UNIVERSITET

Institut for Elektroniske Systemer
Fredrik Bajers Vej 7
9220 Aalborg Øst
Tlf. 9635 8600
Fax 9815 3662

Co-author statement

With reference to executive order no. 114 regarding the PhD degree §14, article 3, statements from each author about the PhD student's part in the shared work must be included in case the thesis is based on already published articles.

Paper title:	*"Performance of a WCDMA FDD Cellular Multihop Network"*
Place of publication:	*IEEE International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC), Berlin, Germany, September, 2005.*
List of authors:	*R.S. Karlsson, H. Aniktar, J.H. Mikkelsen, and T. Larsen*
PhD student:	*H. Aniktar*
Cpr.nr:	*100777-3559*
Contribution [%, text]:	*R.S. Karlsson: 60%* *H. Aniktar: 10%* *J.H. Mikkelsen: 10%* *T. Larsen: 20%*

R. S. Karlsson is the originator and the main contributor of the paper. H. Aniktar has participated in discussions, data processing, editing and reviewing phases. Main contrubution of the paper is the investigation of radio resources for multihop functionality.

R. S. Karlsson	H. Aniktar	J. H. Mikkelsen	T. Larsen

Appendix C

A Class-AB 1.65GHz-2GHz Broadband CMOS Medium Power Amplifier

C

Published in the Proceedings of IEEE Norchip Conference, Oulu, November 2005.
Authors are Hüseyin Aniktar, Henrik Sjöland, Jan H. Mikkelsen, and Torben Larsen.

A Class-AB 1.65GHz-2GHz Broadband CMOS Medium Power Amplifier

H. Aniktar[1], H. Sjöland[2], J.H. Mikkelsen[1], and T. Larsen[1]

[1]RISC Division, Center for TeleInFrastructure, Aalborg University,
Niels Jernes Vej 12, DK–9220 Aalborg East, Denmark,
E-mail: risc@kom.aau.dk
[2]Department of Electroscience, Lund University, Sweden,
E-mail: Henrik.Sjoland@es.lth.se

Abstract

In this paper a single stage broadband CMOS RF power amplifier is presented. The power amplifier is fabricated in a $0.25\mu m$ *CMOS process. Measurements with a* $2.5V$ *supply voltage show an output power of* 18.5 *dBm with an associated PAE of 16% at the 1-dB compression point. The measured gain is 5.1* $\pm$ 0.5 *dB from 1.65 to* 2 *GHz. Simulated and measured results agree reasonably well.*

1. Introduction

Multi-mode radio terminals are needed more and more as the number of radio systems on the market increases. Multi-mode terminals enable the user to have access to different systems with a single terminal. Realization of multi-band, multi-mode radio terminals requires technical progress in several areas. Design of broadband multi-mode power amplifiers (PA) is one of them [1].

The design of broadband amplifiers introduces difficulties which require careful considerations [2]. Two techniques that are commonly used in the design broadband power amplifiers are the use of compensated matching networks and the use of negative feedback [2]. Basically, the design of a constant-gain amplifier over a broad frequency range is a matter of properly designing the matching networks, or the feedback network, in order to compensate for the variations of $|S_{21}|$ with frequency [2]. In this work, the matching networks are designed to give the best input and output VSWR by using passive network synthesis techniques.

2. Circuit Design

The power amplifier is designed as a single-ended one stage common source amplifier. It is biased in class-AB to get high linearity and reasonable efficiency. To achieve about 20dBm output power with a 2.5 V supply voltage, a transistor width of 1640 μm was used. The estimation of the required transistor size is an iterative process using the DC characteristics of the transistor. The length of the transistor was set to minimum (0.25 μm) to maximize its high frequency gain. The optimum load was determined to 16.5 Ω. After initial transistor size and the load determination, fine tuning was done using the harmonic balance simulation in Agilent-ADS.
The input and output matching networks were designed using passive network synthesis techniques to achieve optimum VSWR characteristics over the broad frequency band. Interconnection elements (bonding wires, pad capacitances, and board traces) were also taken into account in the design of matching networks. Figure 1 shows the schematic of the CMOS power amplifier.

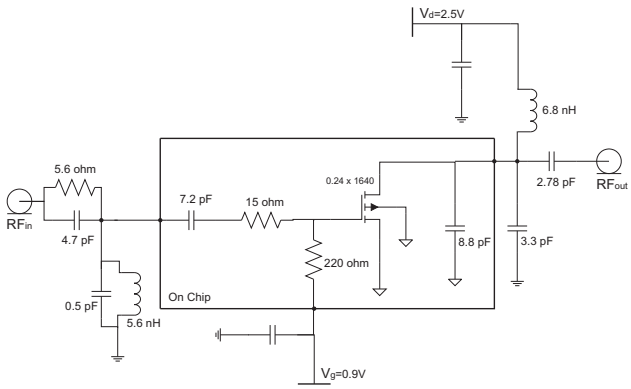

Figure 1: Schematic of the single stage power amplifier.

2.1. Interconnection Models

In the circuit simulations, two interconnection models are used; one is from chip signal/bias pad to PCB signal/bias pad, and the other is from chip ground pad to PCB ground pad. These models are shown in Figures 2 and 3.

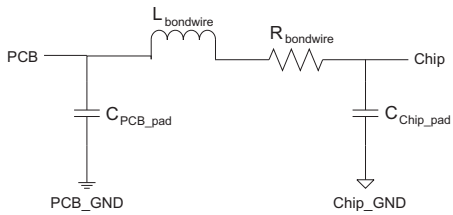

Figure 2: Interconnection model for chip signal/bias pad to PCB signal/bias pad.

The inductance value of the bondwires is assumed to equal approximately 1 nH/mm [3]. Multiple bondwires are used in order to reduce the inductance of the chip ground. It is assumed that three parallel connected bondwires has 0.4nH/mm

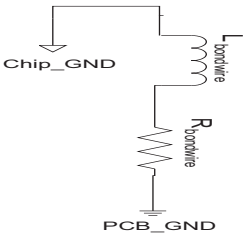

Figure 3: Interconnection model for chip ground pad to PCB ground pad.

inductance [4, 5].

On the chip, 85 μm $\times$ 85 μm pads are used for all connections. The shunt capacitance of a single pad is found to approximately 65 fF based on prior measurements. The chip was bonded to a double-sided PCB with a copper thickness of 70 μm. The substrate material is FR–4 and its thickness is 1 mm. In order to reduce the inductance of the ground plane, vias were used as much as possible. The PCB track capacitance was estimated to 1.5 pF for simulations. To reduce the PCB track capacitance, one solution is to use a thicker substrate. Another solution might be removing the backside ground plane under critical parts.

3. Simulation and Measurement Results

Simulation and measurements were performed to find the S-parameters, 1-dB compression point, power added efficiency (PAE), third order intercept point (IP3), and adjacent channel leakage ratio (ACLR). The simulations were performed with Agilent-ADS, and the measurements with a vector network analyzer, signal generator, and a spectrum analyzer, all from Rohde & Schwarz. For MOSFET simulation, the BSIM3v3 RF Extension Model was used. The simulation and measurement results are presented in the following sections.

3.1. Frequency Response

In this section, the input and output reflection characteristics (S_{11} & S_{22}) and forward and reverse gain characteristics (S_{21} & S_{12}) of the PA are presented. The simulation and measurement results are shown in Figures 4 and 5.

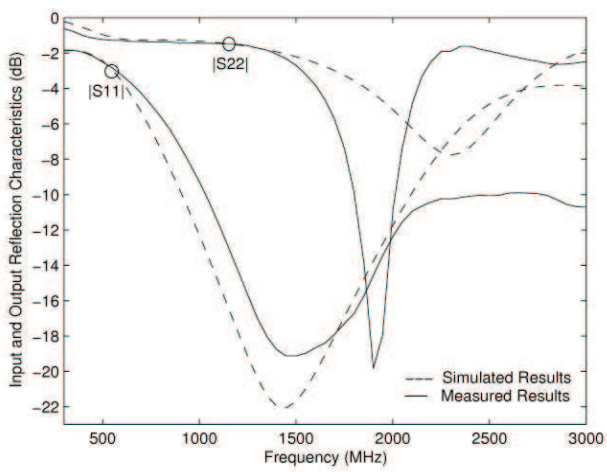

Figure 4: Input and output reflection characteristics.

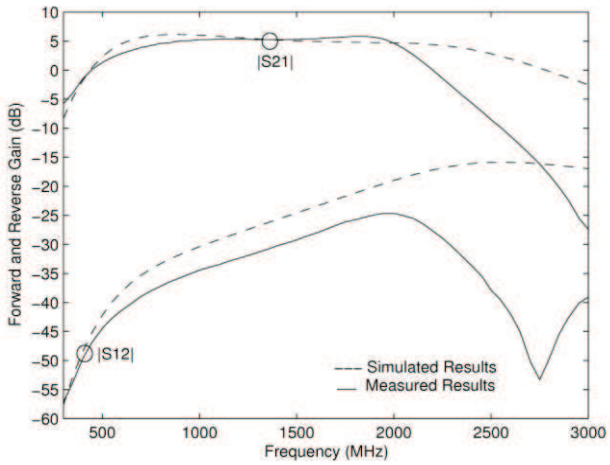

Figure 5: Forward and reverse gain characteristics.

According to the measurement results, the input return loss is more than 10 dB from 1040 MHz to 2600 MHz whereas the output return loss is more than 10 dB from 1800 MHz to 2010 MHz. The forward gain was measured to 5.2 dB at 1 GHz, 5.3 dB at 1.25 GHz, 5.3 dB at 1.5 GHz, 5.7 dB at 1.75 GHz, 5.3 dB at 1.95 GHz, and 4.7 dB at 2 GHz. The gain flatness is 5.2 $\pm$ 0.5 dB from 1 GHz to 2 GHz. Differences between simulation and measurement results are because of the imperfections of parasitic models which are used in simulations, on-chip and off-chip component tolerances, and also measurement inaccuracy.

3.2. Efficiency

The measured 1–dB compression point is 18.5 dBm output for 14dBm input power, and the measured PAE at this power level is 16%. At the output compression point, 114 mA current is drawn from the 2.5 V supply voltage. The simulated 1-dB compression point is found to 20.8 dBm for 17 dBm input power, and the corresponding simulated PAE is found to 23%. Input-output power relation and 1-dB compression point are illustrated in Figure 6. Simulated and measured PAE are illustrated in Figure 7.

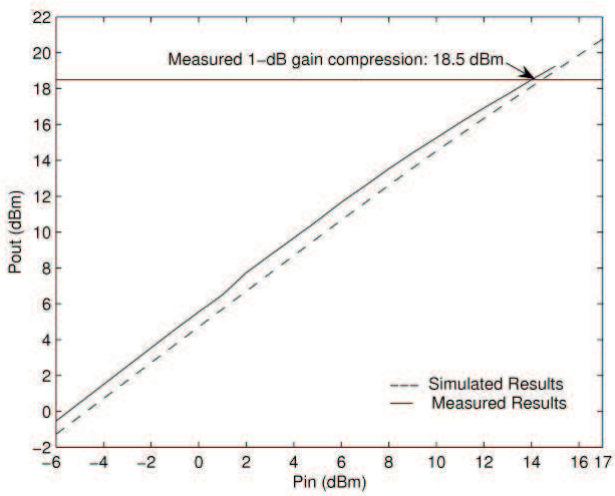

Figure 6: Input and output power relation and 1-dB compression point.

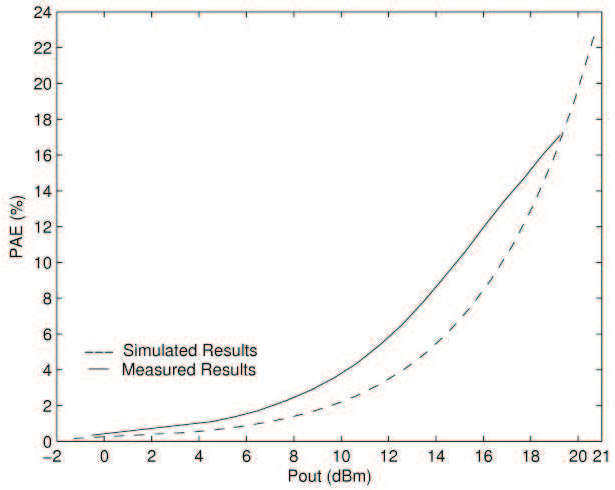

Figure 7: Simulated and measured power added efficiency.

3.3. Linearity

The linearity performance of the amplifier was analyzed for WCDMA/3GPP since linearity is of primary importance for the that system. According to the 3GPP user equipment technical specifications, the uplink frequency band of the WCDMA is $1920 - 1980$ MHz and the transmit power level is 21 dBm $\pm$ 2 dB for power class IV. The required adjacent channel leakage ratio (ACLR) for the user equipment is -33 dB for adjacent channels (± 5 MHz) and -43 dB for second adjacent channels (± 10 MHz) [6].

The output referred third order intercept point (OIP_3) and fifth order intercept point (OIP_5) were measured. In the measurements, the signal generator frequencies (tones) were set at 1950 MHz ± 500 kHz. The levels were set so as not to saturate the amplifier, 15dB below the 1-dB compression point [7]. The measurement results are listed in Table 1. OIP_3 and OIP_5 are calculated according to the following equations by using the measurements of the third order intermodulation product level (P_{IM3}), fifth order intermodulation product level (P_{IM5}) and the output power level (P_o).

$$OIP_3(dBm) = P_o + \frac{P_o - P_{IM3}}{2} \quad (1)$$

$$OIP_5(dBm) = P_o + \frac{P_o - P_{IM5}}{4} \quad (2)$$

Table 1: Measured output intercept points.

	3rd Order Products		5th Order Products	
	$2f_2 - f_1$	$2f_1 - f_2$	$3f_2 - 2f_1$	$3f_1 - 2f_2$
	1951.5MHz	1948.5MHz	1952.5MHz	1947.5MHz
OIP_3	30.2dBm	31.5dBm		
OIP_5			25.5dBm	26.9dBm

The measured ACLR performance of the amplifier is illustrated in Figure 8. The ACLR measurement was performed for 17.5 dBm PA output power level. Measurement results are also listed in Table 2.

Since more advanced measurement instruments are needed for ACLR measurements, it is also possible to calculate the out-of-band spectrum regrowth by using the third order and fifth order intercept point measurements [8].

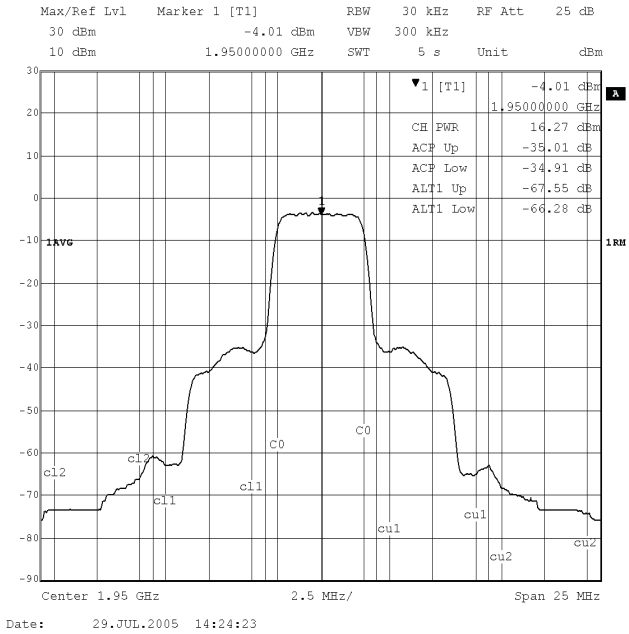

Figure 8: The ACLR performance of the WCDMA/3GPP output signal from the PA.

Table 2: The ACLR performance of the amplifier.

Adjacent Channel			
Bandwidth	3.84MHz	Lower	-34.91 dB
Spacing	5MHz	Upper	-35.01 dB
Alternate Channel			
Bandwidth	3.84MHz	Lower	-66.28 dB
Spacing	10MHz	Upper	-67.55 dB

In Table 3, this work is compared to other published medium power amplifiers. Since there are trade-off's in linearity vs. efficiency and in broadband vs. output power, in this amplifier we reached good linearity while getting lower efficiency and broad frequency range while getting a bit lower output power.

Table 3: Performance comparison.

	Pout (dBm)	PAE (%)	G (dB)	ACLR (dBc)	Vdd (V)	F (GHz)	Proc.
This work	18.5	16	5.1±0.5 1 stage	35.01 @5MHz, 17.5dBm	2.5	1.65-2	CMOS 0.25u
[5]	23.5	35	24.6 2 stages	50 @50kHz, 22dBm	2.5	1.9	CMOS 0.35u
[9]	22.5	29	25 3 stages	55 @600kHz, 21.5dBm	3.4	1.9	GaAs
[10]	18.1		14.5±0.4 1 stage		2	0.8-7.4	GaAs HEMT

4. Chip Layout

A microphotograph of the CMOS PA is shown in Figure 9. The chip was fabricated in a 0.25μm 2.5 V single poly 5-metal layer (1P5M) CMOS technology. The chip size is $750\ \mu m \times 330\ \mu$m.

5. Conclusion

A CMOS RF power amplifier has been realized in a $0.25\,\mu$m CMOS technology. With 2.5 V supply voltage, 18.5 dBm output power with 16% PAE, a broad frequency band and

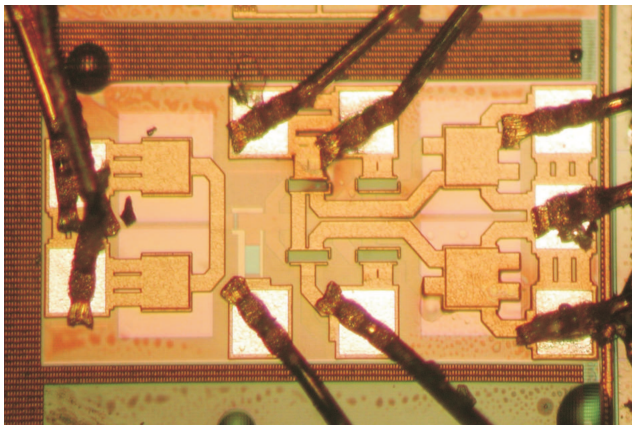

Figure 9: Die photo.

a good linearity were measured. An amplifier with these performance characteristics may be suitable for use in multi-mode radio terminal applications.

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AALBORG UNIVERSITET

Institut for Elektroniske Systemer
Fredrik Bajers Vej 7
9220 Aalborg Øst
Tlf. 9635 8600
Fax 9815 3662

Co-author statement

With reference to executive order no. 114 regarding the PhD degree §14, article 3, statements from each author about the PhD student's part in the shared work must be included in case the thesis is based on already published articles.

Paper title:	*"A Class-AB 1.65GHz-2GHz Broadband CMOS Medium Power Amplifier "*
Place of publication:	*IEEE Norchip Conference, Oulu, Finland, November, 2005.*
List of authors:	*H. Aniktar, H. Sjoland, J.H. Mikkelsen, and T. Larsen*
PhD student:	*H. Aniktar*
Cpr.nr:	*100777-3559*
Contribution [%]:	*85%*
	H. Aniktar is the originator of the paper and he is the main contributor to the paper. H. Aniktar has designed and implemented all test structures and he is responsible for all measurements and subsequent data processing. The main contribution of the paper is the implementation of broadband CMOS medium power amplifier for multi-mode applications.

H. Aniktar	H. Sjoland	J. H. Mikkelsen	T. Larsen

Appendix D

A 850/900/1800/1900MHz Quad-Band CMOS Medium Power Amplifier

D

Published in the Proceedings of European Microwave Week (EuMW), Manchester, September 2006. Authors are Hüseyin Aniktar, Henrik Sjöland, Jan H. Mikkelsen, and Torben Larsen.

A 850/900/1800/1900MHz Quad-Band CMOS Medium Power Amplifier

Hüseyin Aniktar[1], Henrik Sjöland[2], Jan H. Mikkelsen[1], and Torben Larsen[1]
[1]RISC Division, Department of Communication Technology, Aalborg University,
Niels Jernes Vej 12, DK–9220 Aalborg East, Denmark,
E-mail: ha@kom.aau.dk, jhm@kom.aau.dk, tl@kom.aau.dk
[2]Department of Electroscience, Lund University, Sweden,
E-mail: Henrik.Sjoland@es.lth.se

***Abstract*— This paper presents a two-stage quad-band CMOS RF power amplifier. The power amplifier is fabricated in a $0.25\,\mu$m CMOS process. The measured 1-dB compression point between 800 and 900 MHz is 15 dBm $\pm\ 0.2$ dB with maximum 18% PAE, and between 1800 and 1900MHz is 17.5dBm $\pm\ 0.7$dB with maximum 17% PAE. The measured gains in the two bands are 23.6 dB $\pm\ 0.7$ dB and 13 dB $\pm\ 2.1$ dB, respectively.**

I. Introduction

GSM was initially introduced as a pan-European system. In its original form, GSM in the 900, 1800 and 1900 MHz frequency bands uses a Time Division Multiple Access (TDMA) scheme. Since its commercial introduction in the early 1990s, GSM has been constantly upgraded, as evidenced by the introduction of High Speed Circuit-Switched Data (HSCSD), GPRS, EDGE, Enhanced Circuit-Switched Data (ECSD) and Enhanced GPRS (EGPRS) [1].

The introduction of the third generation UMTS, based on WCDMA technology, is a further step towards satisfying the ever increasing demand for data/internet services. 3G is quickly moving on to 3.5G, 3.9G, and 4G and is changing the way the world communicates. The evolution of wireless technologies including CDMA2000, GPRS, EGPRS, WCDMA, HSDPA and 1xEV, allow development of new wireless devices that combine voice, internet, and multimedia services.

In the future GSM and other parallel 2G systems are likely to be replaced with 3G and beyond, that is the bands that today are used for GSM will then be used for WCDMA and other standards. WCDMA in the 900 MHz band is a cost effective way to deliver nationwide high-speed wireless coverage[2].

This evolution will bring new requirements on the RF parts of the transceivers. High linearity because of the modern digital modulations with high spectral efficiency and the multi-band, multi-mode characteristics will be some of them [3]. This work demonstrates a $850/900/1800/1900$ MHz quad-band WCDMA amplifier. The PA shows a good quad-band characteristic and a reasonable linearity and efficiency.

The paper is organized as follows: In Section II, the brief design procedure of the amplifier is given, and then interconnection models of the amplifier are investigated. Experimental results demonstrating the PA performance are offered in Section III. Section IV describes the chip layout, and Section V concludes.

II. Circuit Design

The power amplifier (PA) is designed as a single-ended two-stage common source amplifier. It is biased in class-AB mode to get reasonable linearity and efficiency. Figure 1 shows the schematic of the quad-band CMOS amplifier which is designed to operate from a single 2.5 V supply.

To achieve about 19 dBm output power with a 2.5 V supply voltage, a transistor width of $2460\,\mu$m was used in the output stage. The estimation of the required transistor size is an iterative process using the DC characteristics of the transistor. The length of the transistor was set to minimum ($0.24\,\mu$m) to maximize its high frequency gain [4]. To achieve the $2460\,\mu$m transistor width, 6 parallel transistors were used. Each of them has 41 fingers and the finger width is $10\,\mu$m. The bias voltage was set to 0.6 V in the output stage to operate it in class-AB.

The driver stage transistor size is established after simulation of the output stage power gain. To ensure that the driver stage doesn't enter compression before the output stage, a transistor width of $700\,\mu$m was chosen. To achieve the $700\,\mu$m transistor width, 2 parallel transistors were used. Each of them has 35 fingers. The length of the transistor was set to minimum ($0.24\ \mu$m). The bias voltage for the driver stage was set to 0.75 V to achieve enough gain and linearity.

The load impedance for optimum output power was determined by simulations using the Agilent-ADS Harmonic-Balance simulator. The optimum load was $14\,\Omega$. The output matching network was achieved by using a single filter with two matching pass bands. The two matching pass bands (dual band matching) was realized with on-chip, off-chip components, and interconnection elements (bonding wires, pad capacitances, and board traces) [5], [6].

The stability of the amplifier was ensured with the serial gate and the output shunt resistors, at the cost of a slight reduction in gain and efficiency.

In the circuit simulations, two interconnection models are used; one is from chip signal/bias pad to PCB signal/bias pad, and the other is from chip ground pad to PCB ground pad. These models are shown in Figures 2 and 3. The models are suitable for the chip-on-board technique used in the measurements.

The inductance value of the bondwires is assumed to equal

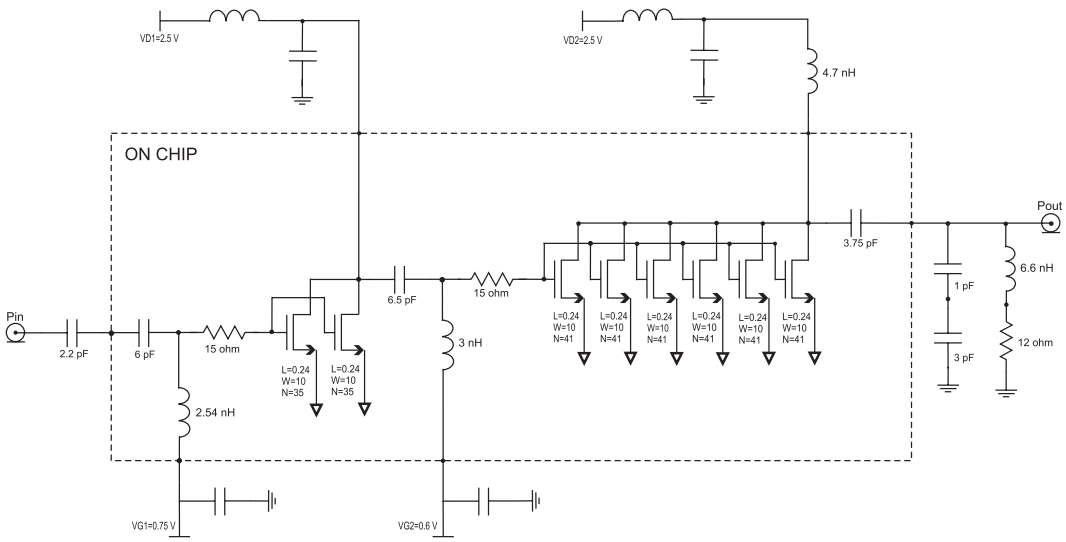

Fig. 1. Schematic of the quad-band power amplifier.

1 nH/mm [7]. Multiple bondwires are used in order to reduce the inductance of the chip ground. It is assumed that three parallel connected bondwires has 0.4 nH/mm inductance [8]. The chip was bonded to a double-sided PCB with a copper thickness of 35 μm. The substrate material is FR–4 and its thickness is 1 mm. In order to improve the grounding of the board, multiple through-hole ground vias were used. To minimize the inductive reactance of passive components, vias were placed as close as possible to components [9]. It is also very important to use efficient capacitive decoupling between the Vdd feed points and ground. This will prevent tendencies toward oscillations. All RF routing is realized using microstrips with 50 Ω characteristic impedance. To minimize RF coupling from the output to the input, all RF lines has been kept as short as possible.

A good PCB ground is essential to avoid oscillations. Large PA currents flowing through the ground impedance can otherwise induce a significant voltage, which could cause stability problems.

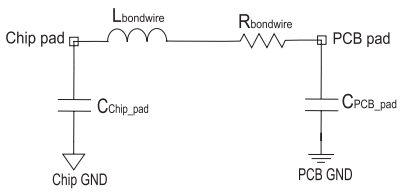

Fig. 2. Interconnect model for chip signal pad to PCB signal pad.

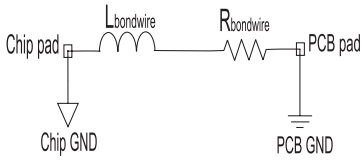

Fig. 3. Interconnect model for chip ground pad to PCB ground pad.

III. Measurement Results

The CMOS power amplifier was tested using chip on board assembly. Measurements were performed to find the S-parameters, 1-dB compression point, power added efficiency (PAE), output third order intercept point (OIP3), adjacent channel leakage ratio (ACLR), and error vector magnitude (EVM).

A. Frequency Response

The measured input and output reflection characteristics ($|S_{11}|$ & $|S_{22}|$) and forward and reverse gain characteristics ($|S_{21}|$ & $|S_{12}|$) of the PA are shown in Figures 4 and 5. Measured values for certain frequencies are listed in Table I.

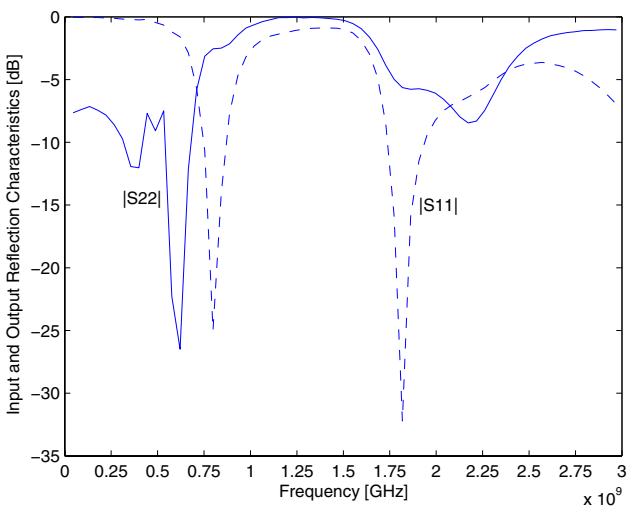

Fig. 4. Measured input and output reflection characteristics.

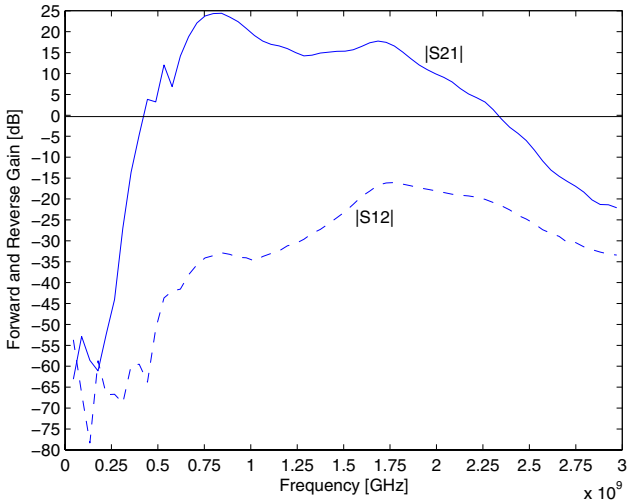

Fig. 5. Measured forward and reverse gain characteristics.

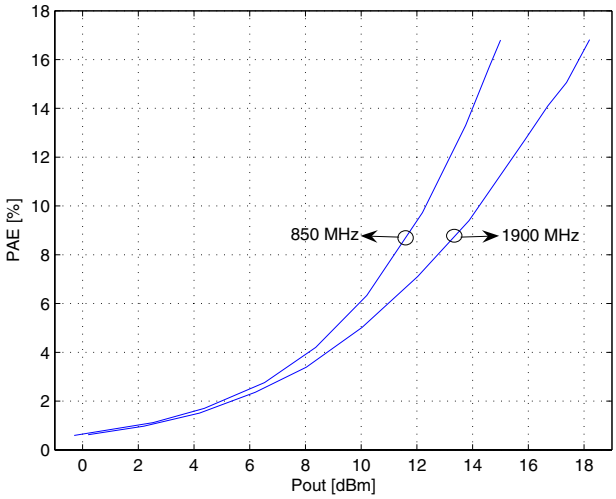

Fig. 6. Measured power added efficiency and output power.

TABLE I

MEASURED NETWORK CHARACTERISTICS FOR SELECTED FREQUENCIES.

Frequency [MHz]	$\|S_{21}\|$ dB	$\|S_{11}\|$ dB	$\|S_{22}\|$ dB
800	24.3	−25	−2.5
850	24.2	−12.7	−2.5
900	22.9	−6.5	−1.8
1800	15.1	−28.4	−5.6
1850	14	−18.5	−5.7
1900	12	−11.5	−5.7
1950	10.9	−9.4	−5.9

B. Efficiency and Linearity

Measured 1-dB compression point, power added efficiency, and output third order intercept point values for certain frequencies are listed in Table II. Figure 6 shows the PAE characteristic of the amplifier. Figures 7 and 8 illustrate DC current consumption of the amplifier.

TABLE II

MEASURED SPECTRUM CHARACTERISTICS FOR SELECTED FREQUENCIES.

Freq [MHz]	$P1dB$ [dBm]	I_d [mA]	PAE [%]	OIP3 [dBm]
800	15.3	74	18.2	25
850	15	75	16.8	24.8
900	14.8	75	16	25.8
1800	16.8	133	14	26
1850	17.8	144	16	26.9
1900	18.2	147	17	27.2
1950	17.8	141	15.6	27

For two-tone measurements, the signal generator frequencies (tones) were set at $f_c \pm 500$ kHz. Two-tone measurements show that the OIP3 between 800 - and 900 MHz is 25.3 dBm ± 0.5 dB, and between 1800 - and 1900 MHz is 26.6 dBm ± 0.6 dB.

The linearity performance of the amplifier was analyzed according to the WCDMA/3GPP user equipment requirements [10]. In Figure 9 and 10, adjacent channel leakage ratio (ACLR) and error vector magnitude (EVM) measurements

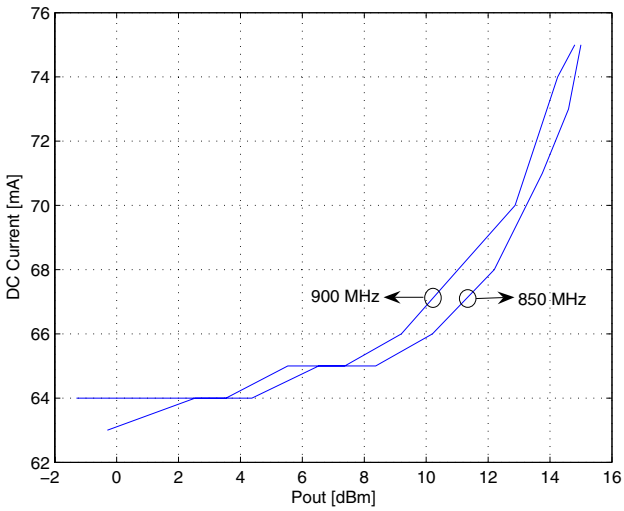

Fig. 7. Measured DC current for 850/900 MHz band.

are illustrated. The measurements have been performed at 1950 MHz with 17 dBm PA output power. For 5 MHz adjacent channel, the measured ACLR is −28 dBc and for 10 MHz alternate channel, the measured ACLR is −58 dBc. The measured RMS EVM is 3.4%, and peak EVM is 8.3%.

IV. CHIP LAYOUT

The chip was fabricated in a 0.25 μm 2.5 V single poly 5-metal layer (1P5M) CMOS technology. The chip size is 1282 μm × 414 μm. A microphotograph of the CMOS PA is shown in Figure 11.

V. CONCLUSION

In this work a quad-band characteristics was obtained with a single CMOS power amplifier while getting medium output power, and reasonable efficiency and linearity. With 2.5 V

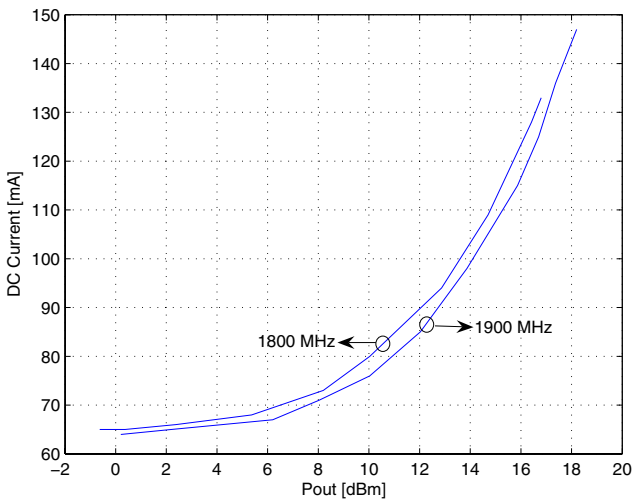

Fig. 8. Measured DC current for 1800/1900 MHz band.

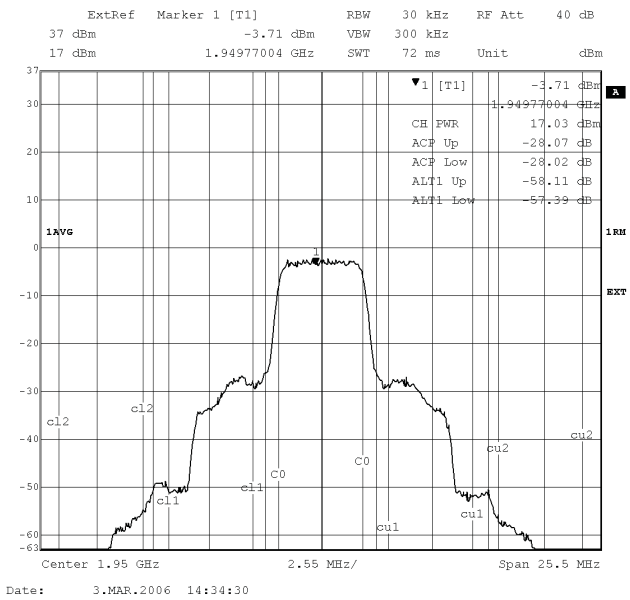

Fig. 9. The ACLR performance of the PA output signal.

supply voltage, the measured 1-dB compression point between 800 and 900 MHz is 15 dBm $\pm$ 0.2 dB with maximum 18% PAE, and between 1800 and 1900 MHz is 17.5 dBm $\pm$ 0.7 dB with maximum 17% PAE. The measured gains in the two bands are 23.6 dB $\pm$ 0.7 dB and 13 dB $\pm$ 2.1 dB, respectively. The chip was fabricated in a 0.25μm 2.5 V single poly 5-metal layer (1P5M) CMOS technology. The chip size is 1280 μm $\times$ 420 μm.

VI. Acknowledgment

The authors would like to thank Peter Boie Jensen for lab assistance. This work was supported by the Danish Technical Research Council, project number 26-03-0030.

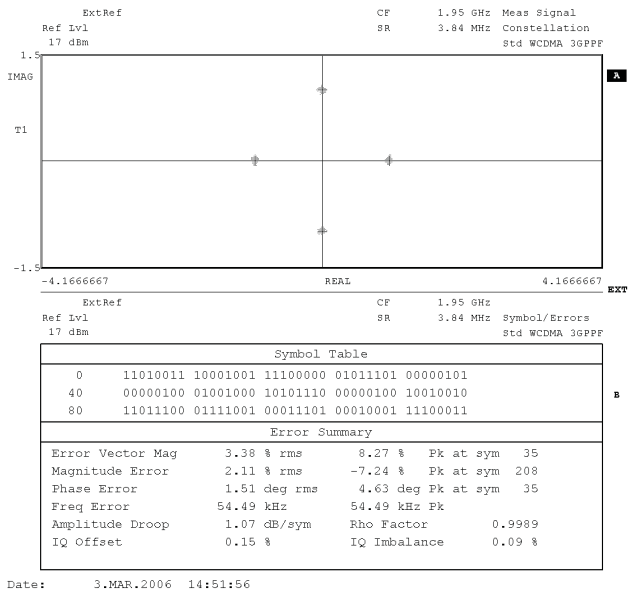

Fig. 10. The EVM performance of the amplifier output signal.

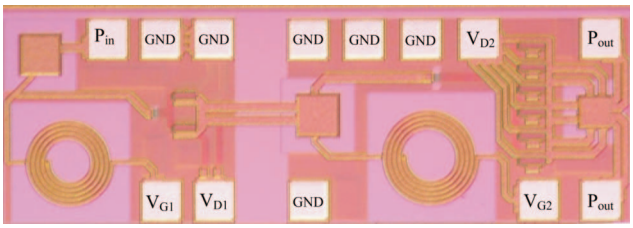

Fig. 11. Die microphotograph.

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AALBORG UNIVERSITET

Institut for Elektroniske Systemer
Fredrik Bajers Vej 7
9220 Aalborg Øst
Tlf. 9635 8600
Fax 9815 3662

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Place of publication:	*European Microwave Conference (EuMW), Manchester, England, September, 2006.*
List of authors:	*H. Aniktar, H. Sjoland, J.H. Mikkelsen, and T. Larsen*
PhD student:	*H. Aniktar*
Cpr.nr:	*100777-3559*
Contribution [%]:	*85%*
	H. Aniktar is the originator of the paper and he is the main contributor to the paper. H. Aniktar has designed and implemented all test structures and he is responsible for all measurements and subsequent data processing. The main contribution of the paper is the implementation of WCDMA-850/900/1800/1900 MHz quad-band power amplifier in CMOS technology.

H. Aniktar	H. Sjoland	J. H. Mikkelsen	T. Larsen

Appendix E

A CMOS Power Amplifier using Ground Separation Technique

E

Published in the Proceedings of 7th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, California, January 2007. Authors are Hüseyin Aniktar, Henrik Sjöland, Jan H. Mikkelsen, and Torben Larsen.

A CMOS Power Amplifier using Ground Separation Technique

Hüseyin Aniktar[1], Henrik Sjöland[2], Jan H. Mikkelsen[1], and Torben Larsen[1]
[1]Department of Electronic Systems, Aalborg University, Denmark, E-mail: risc@kom.aau.dk
[2]Department of Electroscience, Lund University, Sweden, E-mail: Henrik.Sjoland@es.lth.se

***Abstract*— This work presents an on-chip ground separation technique for power amplifiers. The ground separation technique is based on separating the grounds of the amplifier stages on the chip and thus any parasitic feedback paths are removed. Simulation and experimental results show that the technique makes the amplifier less sensitive to bondwire inductance, and consequently improves the stability and performance.**

A two-stage CMOS RF power amplifier for WCDMA mobile phones is designed using the proposed on-chip ground separation technique. The power amplifier is fabricated in a $0.25\,\mu$m CMOS process. It has a measured 1-dB compression point between 1920MHz and 1980MHz of 21.3 ± 0.5dBm with a maximum PAE of 24%. The amplifier has sufficiently low ACLR for WCDMA (-33 dB) at an output power of 20 dBm.

I. Introduction

Most modern digital modulation forms with high spectral efficiency present a varying envelope, which requires RF circuits with high linearity to prevent signal degradation. Efficient but nonlinear power amplifiers are thus not suitable for such linear modulations. The use of linearization techniques can help alleviate this issue, but at the price of high complexity and additional power consumption, which may be critical in the case of low or medium power amplifiers [1]. In order to satisfy the linearity requirement for preserving modulation accuracy with minimum spectral regrowth, such power amplifiers are typically operated in highly linear Class-A or Class-AB configurations. However, high linearity, particularly in CMOS technology, comes at the cost of poor efficiency. Stability requirements place restrictions on PA characteristics, and limitations of CMOS technology such as low breakdown voltage introduce additional challenges for PA realization.

Stability is a key issue in amplifier design. RF oscillations are especially common in single-ended multi-stage designs [2]. The instability occurs when some of the output energy is fed back to the input port with a phase that makes negative resistance appear at the output or input of the amplifier [3]. Ground bounce inductance plays an important role on the amplifier stability. If all stages in a multi-stage amplifier share the same on-chip ground, they will also share the same inductance to PCB ground. Signal current in the output stage converted to voltage by this inductance will thus be fed back to the input with a risk of instability. Using the proposed ground separation technique this feedback path is removed.

The paper is organized as follows: In Section II, the brief design procedure of the amplifier is given, and then interconnection models of the amplifier are investigated. How the amplifier performance improved with ground separation is also discussed in this section. Simulation and measurement results demonstrating the PA performance are offered in Section III. Section IV describes the chip layout, and Section V concludes.

II. Circuit Design

The reported amplifier is designed as a single-ended two stage common source amplifier. It is biased in Class-AB to get high linearity and reasonable efficiency. Simulations are performed using the $0.25\ \mu$m CMOS process library components with Agilent-ADS. Figure 1 shows the schematic of the CMOS PA which is designed to operate from a single 2.5 V supply.

A. Core Amplifier

To achieve about 23dBm output power with a 2.5V supply, a transistor width of 2870μm was used in the output stage. The estimation of the required transistor size is an iterative process using the DC characteristics of the transistor. The length of the transistor was set to minimum ($0.24\ \mu$m) to maximize its high frequency gain. The load impedance for optimum power output was determined to approximately $10 - j11\,\Omega$. The gate bias voltage was set to 0.75 V in the output stage.

The driver stage transistor size is established after simulation of the output stage. To ensure that the driver stage doesn't enter saturation before the output stage, a transistor width of 1120μm was chosen. The bias voltage for the driver stage was set to 0.85 V.

The input and output matching networks were designed using passive network synthesis techniques to achieve optimum VSWR characteristics over the desired frequency band ($1920 - 1980$ MHz). An output impedance transformation network including the MOS output capacitance and interconnection elements (bond wires, pad capacitances, and PCB board traces) is designed to transform the $50\,\Omega$ load into the $10 - j11\ \Omega$ optimum load. The network includes the MOS output capacitance, 6 nH off-chip load inductance, 6 pF on-chip DC blocking capacitance, and interconnection elements (see Figure 1).

To improve the stability and performance of the amplifier, driver and output stage grounds are separated on the chip. This is described in more detail in the following section.

B. Interconnection Models

In the circuit simulations, two interconnection models are used; one is from chip signal/bias pad to PCB signal/bias pad,

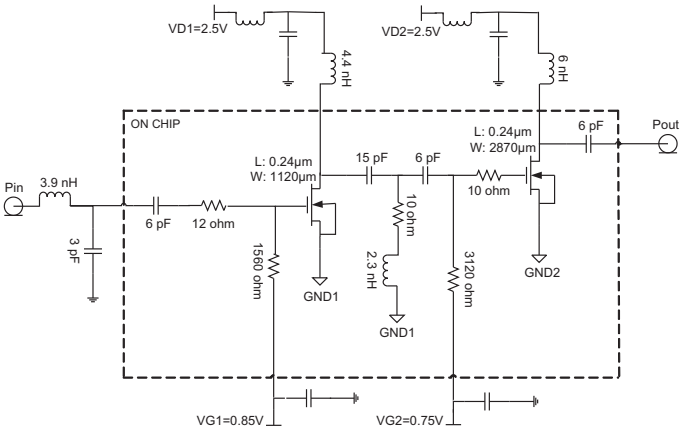

Fig. 1. Schematic of the CMOS power amplifier.

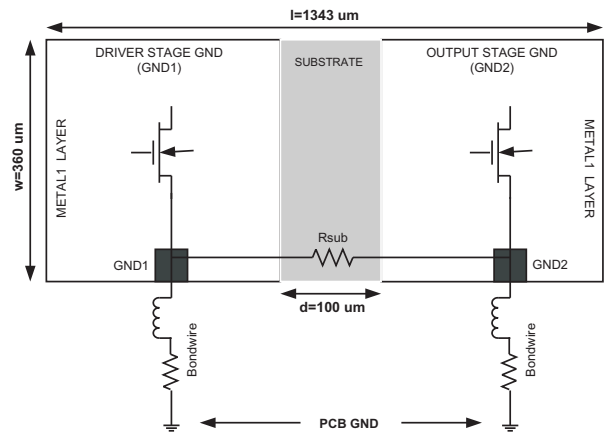

Fig. 3. Interconnection model for chip ground pad to PCB ground pad.

and the other is from chip ground pad to PCB ground pad. These models are shown in Figures 2 and 3. The models are suitable for the chip-on-board technique used in the measurements.

The inductance value of the bondwires is assumed to equal approximately 1 nH/mm [4]. Multiple bondwires are used in order to reduce the bondwire inductance both in output and ground connections. It is assumed that three parallel connected bondwires has about 0.4 nH/mm inductance [5].

On the chip, 85 μm $\times$ 85 μm pads are used for all connections. The shunt capacitance of a single pad was found to be approximately 65 fF in prior measurements. The PCB track capacitance was roughly estimated to 1.5 pF for simulations.

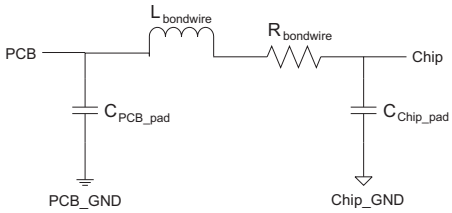

Fig. 2. Interconnection model for chip signal/bias pad to PCB signal/bias pad.

Figure 3 shows the interconnection model for chip ground pad to PCB ground pad. Different chip grounds are assigned for driver and output stages, GND1 and GND2. PCB ground is assumed to be a perfect ground and is denoted by GND. Driver and output stage grounds are isolated from each other by the substrate resistivity.

Investigations showed that when driver and output stage grounds are separated, the stability and performance were improved. Figure 4 shows the simulated stability factor of the amplifier with and without ground separation. As can be seen the PA with the ground separation technique is stable, whereas without the technique the amplifier is potentially unstable and malfunctioning.

To quantify the stability of the amplifier, the Rollet Stability criteria is used. The Rollet Stability criteria can be expressed

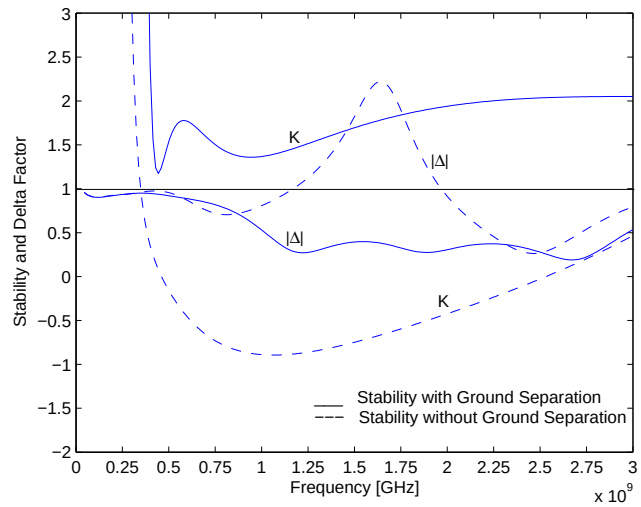

Fig. 4. Simulated stability factor with and without ground separation technique.

as follows [6]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{1}$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{2}$$

- Stable: $K > 1$ and $|\Delta| < 1$
  - Unconditionally stable:

$$||c_s| - r_s| > 1 \text{ for } |S_{22}| < 1 \tag{3}$$

$$||c_l| - r_l| > 1 \text{ for } |S_{11}| < 1 \tag{4}$$

  - Conditionally stable:

$$||c_s| - r_s| < 1 \text{ for } |S_{22}| < 1 \tag{5}$$

$$||c_l| - r_l| < 1 \text{ for } |S_{11}| < 1 \tag{6}$$

- Unstable (potentially): $K > 1$ & $|\Delta| > 1$ and $K < 1$ & $|\Delta| < 1$,

where c_s, c_l, r_s, and r_l parameters represent the center and radius of the source and load stability circles respectively.

Simulations show that $12\,\Omega$ resistance between GND1 and GND2 is enough to sufficiently isolate them from each other. In the $0.25\ \mu$m CMOS process, the substrate resistivity (R) is $20\,\Omega \cdot \mathrm{cm}$ and the substrate thickness (T) is 29 mils. The substrate resistance between GND1 and GND2 can be roughly estimated using the formula:

$$R_{Sub} = R[\Omega \cdot \mathrm{m}] \times \frac{d[\mathrm{m}]}{A[\mathrm{m}^2]}, \tag{7}$$

where the substrate distance (d) between the GND1 and GND2 is 100μm (See Figure 3) and the substrate cross-section area (A) can be found as follow:

$$A = T[\mathrm{m}] \times W[\mathrm{m}] = 36 \times 10^{-9}\mathrm{m}^2, \tag{8}$$

where the chip width (W) is 360 μm. Using Eq. (7), the resistance (R_{Sub}) between GND1 and GND2 is roughly estimated to $76\,\Omega$, which is much larger than the $12\,\Omega$ which is needed. This means that the simple calculation is sufficient in this case, and that there will be no problem to achieve the isolation.

III. Simulation and Measurement Results

The CMOS power amplifier was tested using chip on board assembly. Measurements were performed to find the S-parameters, 1-dB compression point, power added efficiency (PAE), third order intercept point (IP3), adjacent channel leakage ratio (ACLR), and error vector magnitude (EVM).

A. Frequency Response

The measured and simulated forward and reverse gain characteristics ($|S_{21}|$ & $|S_{12}|$) and input and output reflection characteristics ($|S_{11}|$ & $|S_{22}|$) of the PA are shown in Figures 5 and 6. In Table I, some measured values in the WCDMA band are listed.

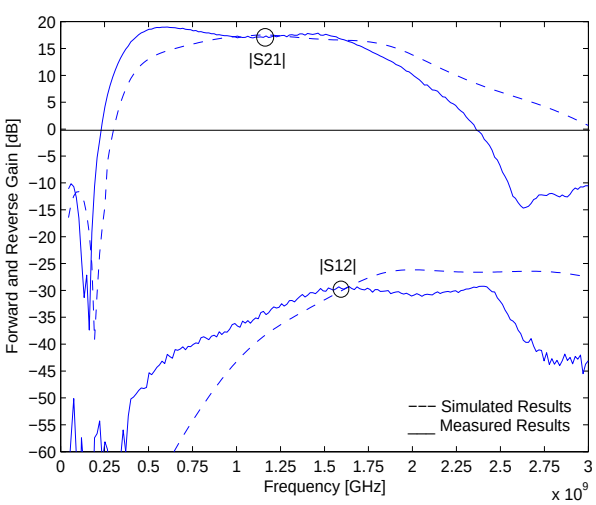

Fig. 5. Simulated and measured forward and reverse gain characteristics.

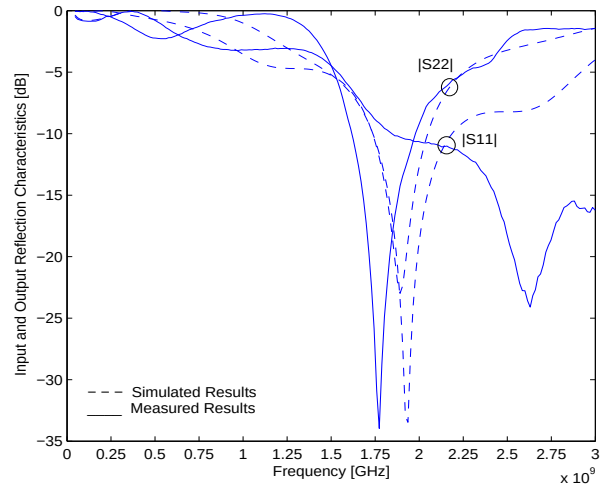

Fig. 6. Simulated and measured input and output reflection characteristics.

TABLE I
Measured S-parameters in the WCDMA Band.

Freq. [MHz]	$\lvert S_{21}\rvert$ dB	$\lvert S_{11}\rvert$ dB	$\lvert S_{22}\rvert$ dB
1920	11.8	−10.4	−12.7
1950	11.2	−10.5	−11.4
1980	10.7	−10.6	−10

While the simulated gain is 14dB at 1.95GHz, the measured gain is only 11.2 dB. Differences between simulation and measurement results are due to imperfections of parasitic models used in simulations, on-chip and off-chip component tolerances, and also measurement inaccuracy.

B. Efficiency

The measured 1-dB output compression point is 21.8 dBm with 24% PAE at 1920 MHz, it is 20.8 dBm with 20.4% PAE at 1950 MHz, and it is 21.4 dBm with 22.4% PAE at 1980 MHz. At the compression point, the current drawn from the 2.5 V supply voltage is 232 mA, 216 mA, and 222 mA respectively. The simulated 1-dB compression point at 1950 MHz is 22.7 dBm with 32% PAE. The difference between the simulated and measured results is related to the measured gain being lower than the simulated one. Simulated and measured PAE are illustrated in Figure 7.

C. Linearity

The linearity performance of the amplifier was analyzed according to the WCDMA/3GPP user equipment requirements [7]. Third order output intercept point (OIP_3), ACLR, and EVM measurements are performed.

For two-tone measurement the frequencies (tones) are set at $f_c \pm 500$ kHz. The measured third order intercept points are 30.9 dBm, 30 dBm, and 30.1 dBm for 1920 MHz, 1950 MHz, and 1980 MHz center frequencies.

In Figure 8, ACLR measurement is illustrated. The measurement has been performed at 1950 MHz with 20 dBm PA output power.

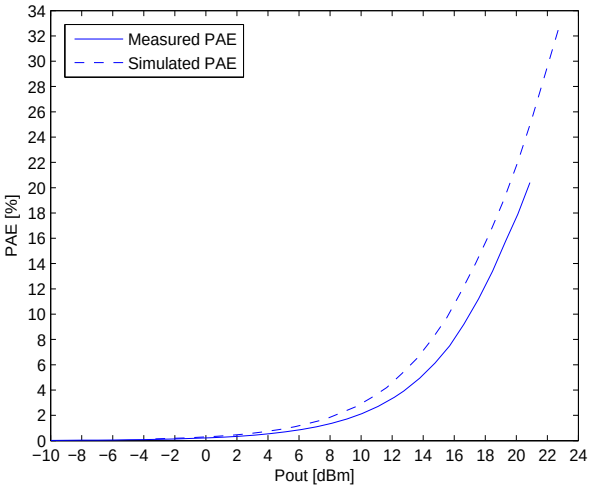

Fig. 7. Simulated and measured power added efficiency.

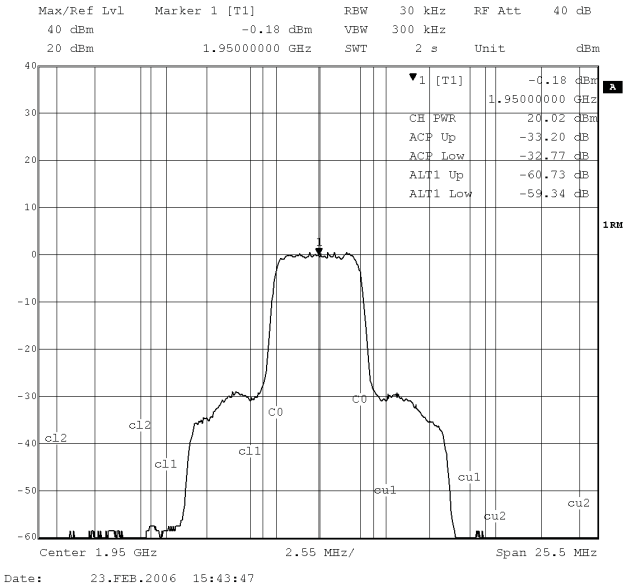

Fig. 8. The ACLR performance of the amplifier output signal.

In Table II, all measured results are listed and compared to system requirements. In WCDMA 3GPP UE document, transmitter characteristics are specified at the antenna connector of the UE. There will likely be some devices between the PA output and the antenna terminals such as circulator, duplex filter, and switch(es) with several dB of loss. When making the comparison, these losses also have to be taken into account.

IV. Chip Layout

A microphotograph of the CMOS PA is shown in Figure 9. The chip was fabricated in a $0.25\,\mu$m 2.5V single poly 5-metal layer (1P5M) CMOS technology. The chip size is $1343\,\mu$m $\times$ $360\,\mu$m. Driver and output stage layouts are separated with $100\,\mu$m distance. Each block is connected to PCB ground with different GND pads. Ground separation increases the overall area of the chip with $0.036\,\mathrm{mm}^2$.

TABLE II

Measured performance and WCDMA/3GPP Specifications.

Parameter	Measured	WCDMA/3GPP Specs
Output Power & PAE		Class 3:
1920 MHz	21.8 dBm & 24%	23dBm $+1/-3$dB
1950 MHz	20.8 dBm & 20.4%	Class 4:
1980 MHz	21.4 dBm & 22.4%	21dBm $\pm$2dB
ACLR Performance		
1950 $\pm$5MHz	-33.2 dB	< -33 dB
1950 $\pm$10MHz	-60.7 dB	< -43 dB
RMS EVM	4%	$< 17.5\%$
Peak EVM	10.7%	

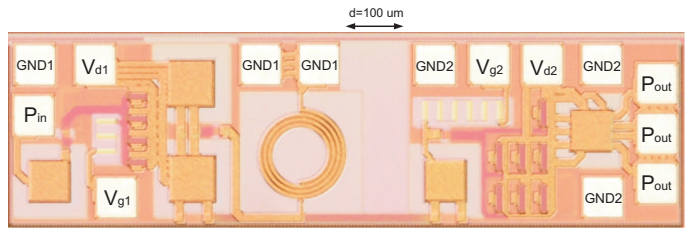

Fig. 9. Die photo.

V. Conclusion

The inductance of the ground bondwires is one of the most serious problems in single-ended integrated amplifier design. The inductance creates parasitic feedback which can cause the amplifier to self-oscillate. In this work it is demonstrated that the parasitic feedback path can be broken using a ground separation technique, and consequently amplifier's stability and performance can be improved.

To demonstrate the technique, a CMOS RF power amplifier with ground separation has been realized. With 2.5 V supply voltage, $21.3\ \pm\ 0.5$ dBm output power with maximum 24% PAE, and a good linearity were measured. At 20dBm it fulfills the WCDMA/3GPP requirements on ACLR and EVM.

VI. Acknowledgment

The authors would like to thank Peter Boie Jensen for lab assistance. This work was supported by the Danish Technical Research Council, project number 26-03-0030.

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AALBORG UNIVERSITET

Institut for Elektroniske Systemer
Fredrik Bajers Vej 7
9220 Aalborg Øst
Tlf. 9635 8600
Fax 9815 3662

Co-author statement

With reference to executive order no. 114 regarding the PhD degree §14, article 3, statements from each author about the PhD student's part in the shared work must be included in case the thesis is based on already published articles.

Paper title:	*"A CMOS Power Amplifier using Ground Separation Technique"*
Place of publication:	*IEEE 7th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF'07), Long Beach, CA, USA, 2007.*
List of authors:	*H. Aniktar, H. Sjoland, J.H. Mikkelsen, and T. Larsen*
PhD student:	*H. Aniktar*
Cpr.nr:	*100777-3559*
Contribution [%]:	*85%*
	H. Aniktar is the originator of the paper and he is the main contributor to the paper. H. Aniktar has designed and implemented all test structures and he is responsible for all measurements and subsequent data processing. In this paper, to improve stability and performance of the CMOS power amplifier, an on-chip ground separation technique is proposed.

H. Aniktar	H. Sjoland	J.H. Mikkelsen	T. Larsen

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