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A 1-5 GHz UWB Low Noise Amplifier in 0.18 μm CMOS

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***Abstract*— A 1-5 GHz ultra-wideband CMOS low-noise amplifier (LNA) is presented. A common-gate topology is adopted for the input stage to achieve wideband input matching, while a cascode stage is used as the second stage to provide power gain at high frequencies. By using two inductors in the LNA, a small chip area is obtained. The LNA has been fabricated in a standard 0.18 μm CMOS technology. The measured maximum power gain is 13.7 dB, and the noise figure is 5.0-6.5 dB in the frequency band of 1-5 GHz. The measured third order (two-tone) input intercept point (IIP3) is -9.8 dBm at 4 GHz. The LNA consumes 9 mW with a 1.8 V supply, and occupies an area of 0.78 mm^2.**

I. Introduction

In 2002, the Federal Communication Committee (FCC) authorized the unlicensed use of the ultra wideband (UWB) frequency band from 3.1 to 10.6 GHz for indoor and hand-held systems [1]. Since then, a considerable effort has been put into the development of devices suitable for UWB applications. As one of the essential components, UWB low noise amplifiers (LNAs) have attracted significant research interest and various approaches to the design of UWB LNAs have been proposed [2–9]. Due to FCC's limitations on bandwidth (no less than 500 MHz) and low power emission (EIRP lower than -41.3 dBm/MHz) of an UWB system, the UWB LNA must fulfill several stringent requirements. The LNA must provide a good input matching over a band more than 500 MHz. A sufficient gain is also mandatory to amplify the weak signal at the receiver and overcome the noise effects from consequent stages. In addition, the noise figure of the LNA must be minimized since it plays a major role in defining the receiver's sensitivity. Moreover, the LNA has to be power efficient and physically small to save power and reduce the cost, respectively.

Cascode configured UWB LNAs using LC bandpass filter to achieve the broad input matching have previously been reported [2]. However, such designs depend on the use of several inductors which in turn increase the size of the circuit (1.1 mm^2). A 0-11 GHz distributed LNA has also been proposed [3]. However, the feasibility of this design is also limited by it large size (1.44 mm^2) and a high level of power consumption (100 mW). Based on the fact that the WLAN signal band is located in the UWB frequency band, UWB systems using the full UWB band could experience interference from in-band WLAN signals. To reduce WLAN related interference problems, an UWB LNA with a stop-band in the response has been proposed [7]. But this method suffers the shortcoming of degraded noise performance in the upper passband (NF>7 dB). A 3-5 GHz UWB LNA using resistive feedback has also been proposed [6]. But its gain is relatively low (Voltage gain of 10 dB), and the power consumption is high (17.5 mW).

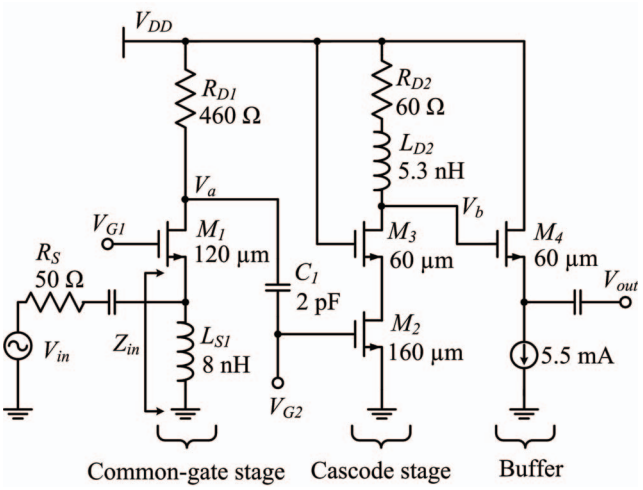

Fig. 1. The schematic for the presented UWB LNA, including an output buffer for measurement purposes.

This work presents the design of an UWB LNA that aims to achieve a low-power (<10 mW) operation, small size (smaller than 0.8 mm^2) and medium-gain (Power gain>10 dB) UWB LNA, providing an $|S_{11}|$ less than -10 dB over the lower UWB passband. A noise figure as low as possible and an IIP3 higher than -10 dBm are also targeted. An UWB LNA with a common-gate stage as the first stage, and a cascode stage as the second stage is proposed. Only two inductors are used in this design, resulting in a miniaturized LNA. A test chip using a standard 0.18 μm CMOS technology has been fabricated for experimental verification, and good results are found.

II. Design of the UWB LNA

The proposed UWB LNA is shown in Fig. 1. To achieve a wideband input matching, a common-gate stage is used as the first stage since it holds the best potential for wideband designs among different circuit configurations [9]. A cascode stage is use as the second stage to provide gain at higher frequencies. In addition an output buffer is added for measurement purposes.

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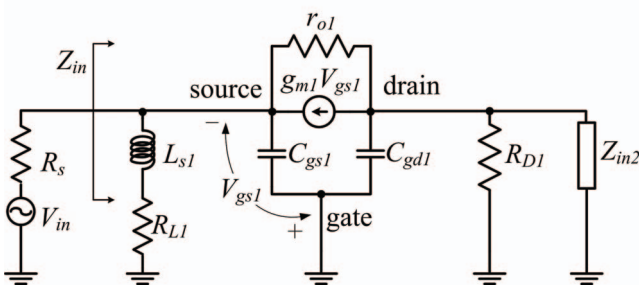

Fig. 2. The small-signal equivalent circuit used for calculating the input impedance of the common-gate stage in Fig. 1.

A. Input matching in the common-gate stage

The small-signal equivalent circuit of the common-gate stage is shown in Fig. 2, where g_{m1} is the transconductance of the transistor M_1. L_{s1} is the inductor used to obtain a wideband input matching with the gate-source capacitor C_{gs1}, and R_{L1} is the resistance of L_{s1}. r_{o1} and C_{gd1} are the output resistance and the gate-drain capacitor of the transistor, respectively. R_{D1} is the load at the drain of the transistor, and Z_{in2} is the input impedance of the next stage. Based on Fig. 2, the input impedance Z_{in} of the common-gate stage can be derived as

$$Z_{in}(s) = \frac{1}{\frac{1+(g_{m1}+sC_{gs1})(R_{L_1}+sL_{s1})}{R_{L_1}+sL_{s1}} + \frac{1-g_{m1}Z_o(s)}{r_{o1}+Z_o(s)}}, \qquad (1)$$

where $Z_o(s) = R_{D1} \parallel Z_{in2} \parallel (1/sC_{gd1})$. Assuming that M_1 has a relatively large output resistance, and neglecting the loading effect of the second stage, Eq. (1) can simplified as

$$Z_{in}(s) = \frac{R_{L_1} + sL_{s1}}{1 + (g_{m1} + sC_{gs1})(R_{L_1} + sL_{s1})}. \qquad (2)$$

Based on Eq. (2), it is easy to determine the characteristics of Z_{in}. At low frequencies, $|sL_{s1}|$ and $|g_{m1} + sC_{gs1}|$ are relatively small, and Eq. (2) approximates as $Z_{in} \approx R_{L_1}$. For frequencies where $|R_{L_1} + sL_{s1}|$ is relatively large and $|sC_{gs1}|$ is still small compared with g_{m1}, Eq. (2) approximates as $Z_{in} \approx 1/g_{m1}$. For very high frequencies where $|sC_{gs1}|$ is considerably larger than g_{m1}, Eq. (2) approximates as $Z_{in} \approx 1/sC_{gs1}$. This indicates that $1/g_{m1}$ only determines the matching level, and that the location of the optimum matching frequency is determined by L_{s1} and C_{gs1}. In order to obtain an optimum input matching at the desired frequency band, the effects of L_{s1} and C_{gs1} on the input matching have been studied. Based on Eq. (2), the calculated $|S_{11}|$ of the common-gate stage with five different values of L_{s1} are shown in Fig. 3. In the calculation, other parameters are kept as constant ($1/g_{m1}$ = 50 Ω, R_{L_1} = 10 Ω and C_{gs1} = 200 fF). It can be seen that the effect of L_{s1} is much stronger at lower frequencies than higher frequencies. This means that a relatively large inductor should be used to ensure a good input matching at lower frequencies. Moreover, the effects of C_{gs1} on $|S_{11}|$ are shown in Fig. 4. In the calculation, $1/g_{m1}$ = 50 Ω, R_{L_1} = 10 Ω and L_{s1} = 2 nH, while C_{gs1} is varying. It is clear

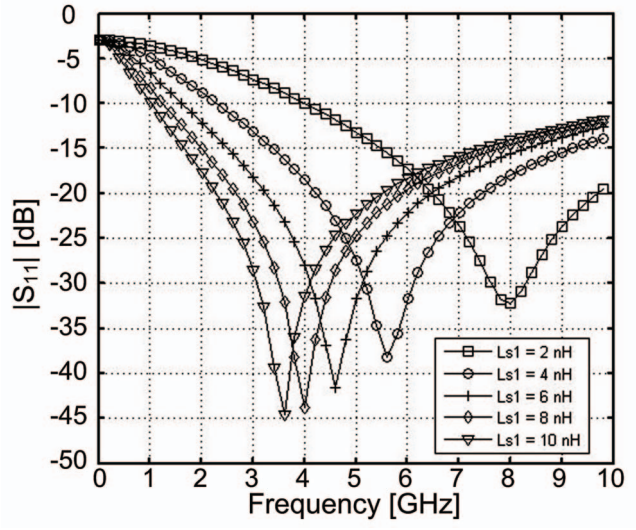

Fig. 3. Calculated $|S_{11}|$ based on Eq. (2) versus frequency with varying L_{s1} ($1/g_{m1}$ = 50 Ω, R_{L_1} = 10 Ω and C_{gs1} = 200 fF.).

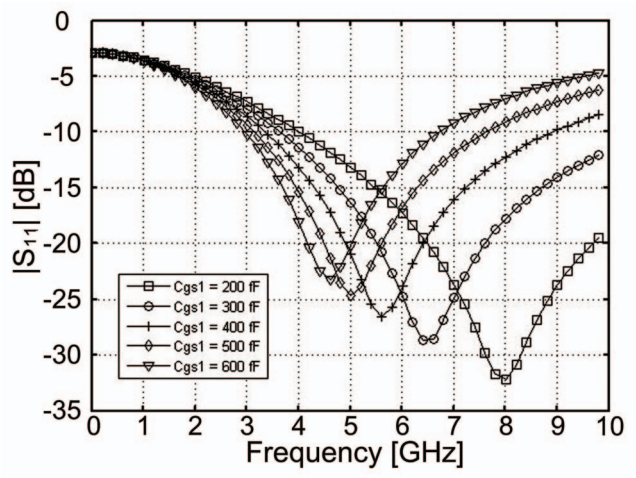

Fig. 4. Calculated $|S_{11}|$ based on Eq. (2) versus frequency with varying C_{gs1} ($1/g_{m1}$ = 50 Ω, R_{L_1} = 10 Ω and L_{s1} = 2 nH.).

that the effects of C_{gs1} on S_{11} are much more obvious at higher frequencies, which indicates that a relatively small C_{gs1} should be used to achieve a good input matching at high frequencies. However, in order to have a proper g_{m1} for optimum input matching without dramatically increasing the power consumption, the minimum size of M_1 is limited by the targeted DC biasing current less than 2.4 mA in this stage. In addition, at the frequency where the input impedance of the common-gate amplifier is largely resistive and g_{m1} is 20 mS, the noise factor of the common-gate stage can be obtained as

$$F = 1 + \frac{\gamma}{\alpha}, \qquad (3)$$

where γ is the coefficient of channel thermal noise and α is the ratio of the transconductance and the zero-bias drain conductance. From Eq. (3), it is clear that the effective way to reduce the noise factor is to increase g_{m1}, since γ is process-

dependent and hence is not a design parameter. However, with the target of $S_{11} < -10\,dB$ over a broad frequency band, g_{m1} must be less than 38 mS ($|S_{11}|$ is -10 dB when $1/g_{m1}$ = 26 Ω). Based on the trade off between input matching, power consumption and noise figure, the width of M_1 is chosen to 120 μm, with a DC biasing current of 2.4 mA, and L_{s1} is chosen as 8 nH, such that g_{m1} is 24 mS and a $|S_{11}|$ less than -10 dB can be guaranteed.

Unlike conventional common-gate LNAs that use an inductor as the drain load of the transistor [9], a resistor, R_{D1} is here used as the load at the drain of M_1. As a result, the chip area needed for the design can be reduced. R_{D1} is here chosen as 460 Ω to obtain a proper gain for the first stage. Owing to the high output impedance of the transistor, R_{D1} has little impact on the input matching performance. The noise figure might be increased by doing so. But as shown by the simulated noise figure of the proposed LNA in section III, a noise figure of 4.3 dB can be maintained.

B. The cascode stage and buffer

The second stage of the UWB LNA is a cascode topology. This stage is adopted to provide the gain at high frequencies. M_3 is helpful for increasing the isolation between the output and the input. L_{D2} is used for output matching. To extend the bandwidth of the cascode stage, a resistor, R_{D2}, is connected in series with L_{D2} to reduce the Q factor of the inductance at the drain of M_3. In this design, the biasing current for both M_2 and M_3 is 2.6 mA to comply with the targeted power consumption of less than 10 mW (2.4 mA has been used in the common-gate stage). M_2 is chosen to 160 μm to optimize the matching with the first stage. M_3 is chosen relatively small, 60 μm, to reduce parasitic capacitance. L_{D2} is chosen as 5.3 nH, and R_{D2} is chosen as 60 Ω.

The buffer is a source follower, which has a voltage gain of

$$\frac{V_{out}}{V_b} = \frac{g_{m4}}{1 + g_{m4}R_L} \tag{4}$$

where V_{out} and V_b are the output and input voltage of the buffer shown in Fig. 1. R_L is the load of the buffer, and its value is 50 Ω in this study. The width of M_4 is chosen to 60 μm to reduce parasitic effects. The DC current of M_4 is chosen as 5.5 mA, such that $1/g_{m4} \approx R_L$ and the source follower has a 6 dB loss in the output power. The complete schematic and parameters of the designed UWB LNA with the buffer are shown in Fig. 1.

III. Test Chip and Measurement Results

The proposed LNA is fabricated using a standard 0.18 μm CMOS process. Including measurement pads the entire design has a compact size of only 1.48 mm by 0.53 mm with measurement pads. Fig. 5 shows the micro-photograph of the test chip. The experimental verification was carried out by on-wafer measurements. The simulated and measured S-parameters of the UWB LNA are shown in Fig. 6. It can be seen that the measured magnitudes of S-parameters match the simulations well. Fig. 6 also shows that the measured gain

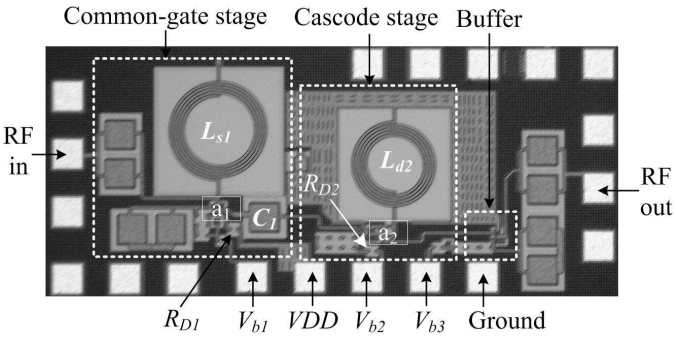

Fig. 5. The micro-photograph of the chip (V_{b1}, V_{b2} and V_{b3} are the DC supply voltages for the biasing networks. a_1 and a_2 are the active areas of the common-gate stage and the cascode stage, respectively.).

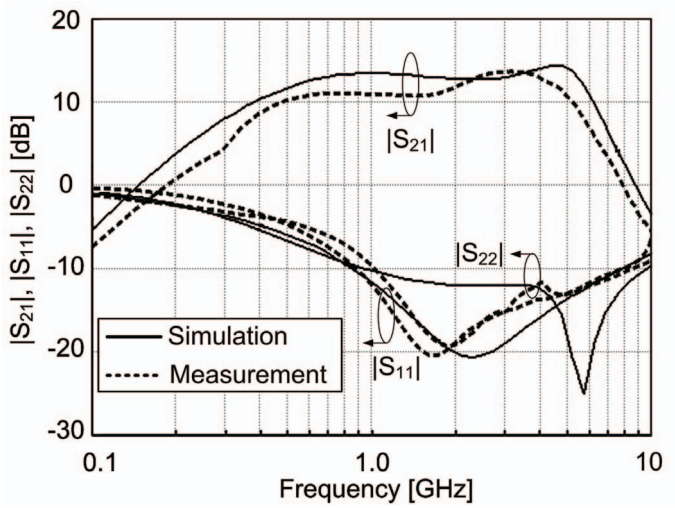

Fig. 6. Simulated and measured magnitudes of S-parameters versus frequency for the circuit in Fig. 1.

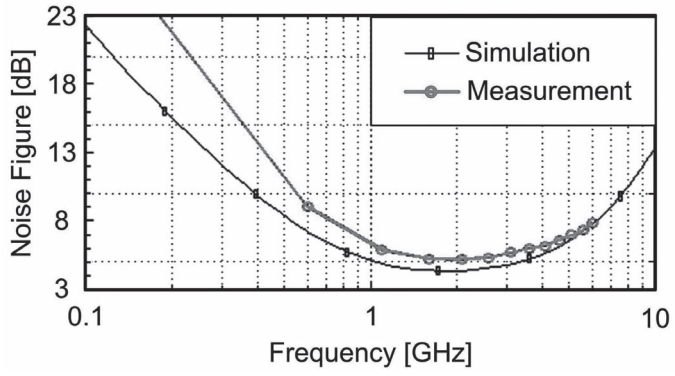

Fig. 7. Simulated and measured noise figures versus frequency for the circuit in Fig. 1.

TABLE I

PERFORMANCE SUMMARY OF THE PRESENT UWB LNA, AND COMPARISON WITH PREVIOUSLY PROPOSED UWB LNAS

	$\lvert S_{11}\rvert$ [dB]	Max $\lvert S_{21}\rvert$ [dB]	Band [GHz]	Max NF [dB]	IIP3 [dBm]	Area [mm^2]	Power [mW]
This work	<-10	13.7	1-5	6.5	-9.8	0.78	9
[2]*	<-9.4	10.4	2.4-9.5	9	-8.8	1.1	9
[3]**	<-20	16	0-11	6	N/A	1.44	100
[4]	<-9.8	18.6	3-6	5	-10.2	N/A	25.2^{+}
[5]	<-8	>10^{++}	3-5	3.3	8	0.4	17.5
[6]	<-12.19	15.91	3-6	6.7	-5	1.1	59.4
[7]	<-10	19.7	3-5, 6-10	>7***	-12.2	1.43	24
[8]	<-9	9.8	2-4.6	5.2^{+++}	-7	0.9	12.6

* TW type; ** High power mode; $^{+}$ With buffer; $^{++}$ Voltage gain; *** Upper band; $^{+++}$ At 5 GHz.

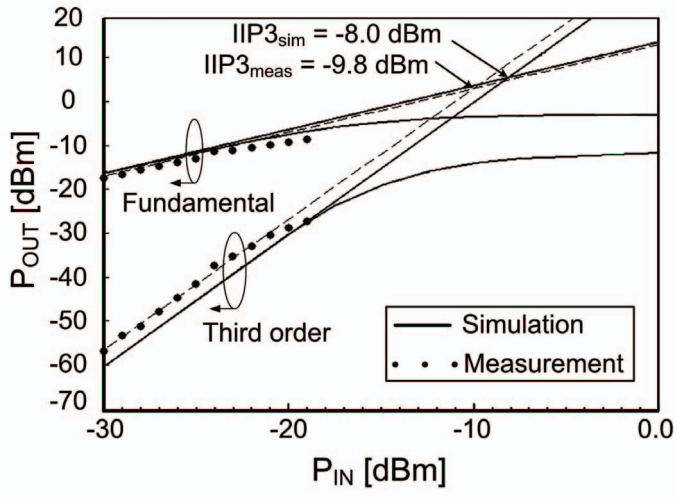

Fig. 8. Measured output power versus input power to determine the 3rd order two-tone input intercept point for the circuit in Fig. 1.

is 11-13.7 dB in 1-5 GHz. The measured $|S_{11}|$ is less than -12 dB from 1 GHz to 5 GHz, and $|S_{22}|$ is less than -10 dB from 1 GHz to 5 GHz. The deviation between the measured and simulated results of $|S_{21}|$ and $|S_{22}|$ might be caused by parasitical components. The simulated and measured NFs are shown in Fig. 7 and the measured NF is 5.0-6.5 dB from 1 to 5 GHz. A third-order intermodulation distortion test is conducted using a 4 GHz signal and a 4.04 GHz signal, which is shown in Fig. 8. The measured IIP3 was -9.8 dBm and the measured 1-dB compression point is -19.5 dBm. Table I summarizes the performance of the presented UWB LNA, with comparison to previously published LNAs. All the LNAs in Table I are based on 0.18 μm CMOS technologies, and the power consumption does not include buffers or biasing circuits except [4]. From the comparison, it can be seen that the present UWB LNA offers a small physical size of only 0.78 mm^2 while providing a low power dissipation of 9 mW. This is achieved while maintaining a medium gain of 13.7 dB. It should be noticed that the chip area includes all the measurement pads and biasing networks.

IV. CONCLUSION

A two-stage UWB LNA has been designed and implemented in a standard 0.18 μm CMOS process. The measured maximum power gain is 13.7 dB and NF is 5.0-6.5 dB in 1-5 GHz, in which the measured $|S_{11}|$ and $|S_{22}|$ are below -12 dB and -10 dB, respectively. The measured IIP3 is -9.8 dBm at 4 GHz, while the power dissipation of the core LNA is only 9 mW with a 1.8 V supply. The design uses only two inductors and as a result a small chip area of 0.78 mm^2 is achieved. The present UWB LNA features low power dissipation and small size compared with previously proposed UWB LNAs.

ACKNOWLEDGMENT

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