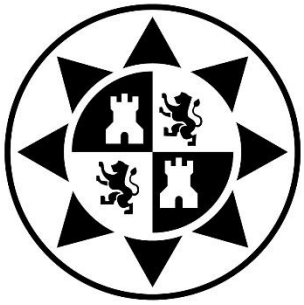

HERIOT-WATT UNIVERSITY – POLYTECHNIC UNIVERSITY OF CARTAGENA

Diseño a 2.45GHz de un Amplificador de Potencia GaN HEMT de Clase A (Resumen en Español)

PROYECTO FINAL DE CARRERA

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Cartagena, Octubre 2015

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Resumen

Hoy en día, la amplificación de estado sólido está dominada por el uso de transistores de tres terminales. Usando un pequeño voltaje aplicado en la entrada del dispositivo, uno puede controlar, de manera eficiente, una gran cantidad de corriente en el terminal de salida cuando el terminal común está conectado a tierra. Este es el origen del nombre transistor, que es la union de las palabras inglesas *transfer* y *resistor*.
Gracias a los transistors, la amplificación existe y este proyecto está enfocado en el proceso de diseño que un ingeniero debe seguir para llevarlo a cabo, desde las primeras simulaciones hasta su testeo en el laboratorio.

Grado	Ingeniería de Telecomunicación
Departamento	Tecnologías de la Información y las Comunicaciones
Fecha de entrega	Octubre 2015

Índice de Contenidos

1. Introducción

1.1. Transistor amplificador

Hoy en día, la amplificación de estado sólido está dominada por el uso de transistores de tres terminales. Usando un pequeño voltaje aplicado en la entrada del dispositivo, uno puede controlar, de manera eficiente, una gran cantidad de corriente en el terminal de salida cuando el terminal común está conectado a tierra. Este es el origen del nombre transistor, que es la unión de las palabras inglesas transfer y resistor.

Los transistores de estado sólido se pueden agrupar en dos categorías: dispositivos unipolares y bipolares. La amplificación de señales es una función fundamental en todos los sistemas de RF y microondas.

Cuando la fuerza de una señal débil es incrementada por un dispositivo usando una alimentación de corriente continua (DC), dicho dispositivo con su circuitería tanto de adaptación como de alimentación es conocido como un amplificador. Aquí, la potencia DC de la alimentación se convierte en potencia RF para mejorar la potencia de la señal de entrada. Si el dispositivo es un transistor, la señal aplicada a la entrada (puerta/base) y la señal amplificada aparece en la salida (drenador/colector) y el terminal común (fuente/emisor) va generalmente a tierra. Las redes de adaptación ayudan excitando el dispositivo y recolectando la señal de salida de una manera más eficiente. La Figura 1.1 nos muestra una representación esquemática de un amplificador (transistor) de una sola etapa. Los constituyentes son un transistor, redes de adaptación tanto en la entrada como en la salida, circuitería de alimentación y conexiones RF de entrada y salida.

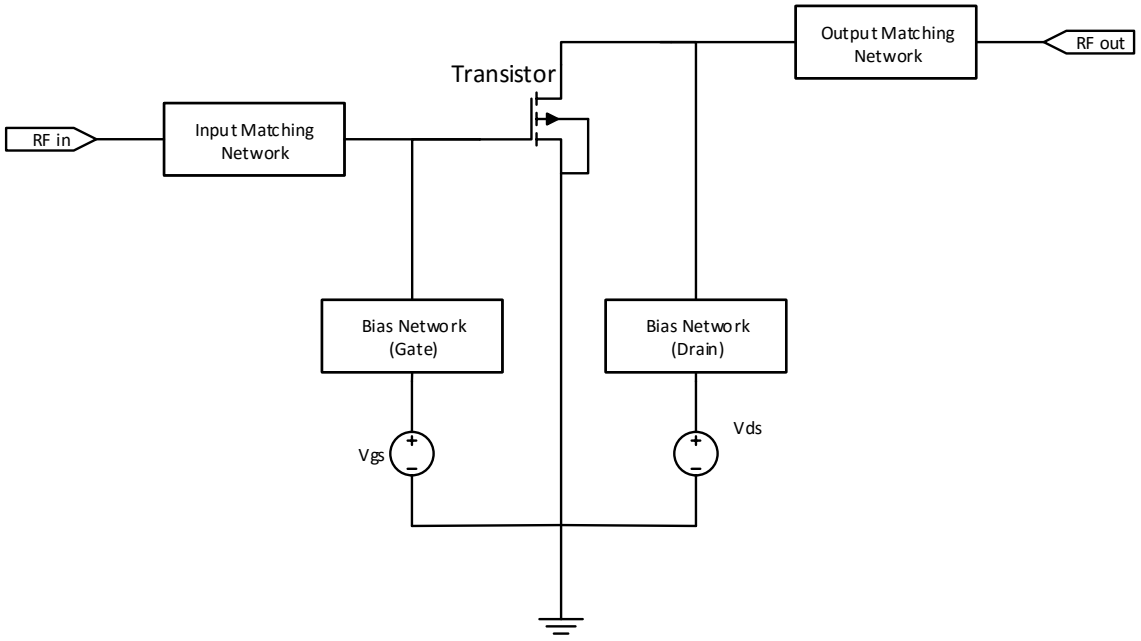


Figura 1.1 – Esquemático de un transistor amplificador.

El diseño de amplificadores requiere esencialmente modelos de dispositivos / parámetros S, herramientas CAD, redes de adaptación y alimentación, y tecnología de fabricación. Amplificadores de RF y microondas tienen las siguientes características:

- Banda limitada de respuesta RF
- Menos del 100% de eficiencia de conversión de DC a RF
- No-linealidades que generan productos de intermodulación entre multiples señales
- Acoplo RF y no respuesta de DC
- Amplitud dependiente de la potencia y diferencia de fase entre la entrada y la salida
- Ganancia dependiente de la temperature, mayor ganancia a bajas frecuencias y viceversa

1.2. Beneficios de los Transistores-Amplificadores

Las principales ventajas de los amplificadores de transistores frente a los amplificadores de tubo son:

- Menor tamaño
- Menor peso

- Mayor fiabilidad
- Alto nivel de capacidad de integración
- Alto volumen y alto rendimiento de capacidad de producción
- Mayor flexibilidad en el diseño
- Menores voltajes de alimentación
- Mantenimiento requerido reducido
- Diversidad de aplicaciones ilimitada
- Tienen mucha más vida operativa (en el orden de millones de horas)
- Requieren mucho menos tiempo de calentamiento

Además, los amplificadores de estado sólido no requieren ajustes en la alimentación o en el circuito tal y como lo requieren los amplificadores de tubo en largos periodos de operación.

1.3. Objetivos

Los principales objetivos y propósitos de este proyecto final son:

- Aprender el trasfondo teórico sobre el diseño de un amplificador de potencia.
- Realizar el diseño y simularlo a través de AWR (Microwave Office).
- Fabricar el prototipo final y testearlo en el laboratorio.

Las especificaciones de nuestro amplificador de potencia serán:

- Trabajar en la banda WiFi (2.45GHz) en una configuración de banda estrecha (100MHz).
- Al menos 14dB de ganancia a esa frecuencia.

1.4. Trasfondo teórico

Toda la teoría básica relativa a este proyecto se encuentra en la versión inglesa de la memoria.

2. Proceso de diseño de un Amplificador de Potencia

2.1. Elección del transistor de microondas

Un dispositivo idóneo que funcione como se pretende es muy esencial. Por ello, un estudio detallado de varios datasheets es imprescindible para no equivocarnos a la hora de elegir nuestro transistor.

Teniendo en cuenta nuestras especificaciones y ya que se han vuelto muy populares en los últimos años hemos decidido usar un GaN HEMT (Gallium Nitride High Electron Mobility Transistor). Los GaN HEMT ofrecen alta eficiencia, alta ganancia y gran ancho de banda haciéndolos ideales para amplificadores tanto lineales como comprimidos. Además de todo lo ya expuesto, otra de sus principales ventajas es el bajo consumo de energía.

Teniendo en cuenta todas estas ventajas, el transistor escogido finalmente es el CGH40010F de Cree Inc. El modelo de dicho transistor ha sido facilitado por la compañía a través de un portal web accesible mediante registro desde el cual nos descargaremos el modelo para su posterior uso en AWR.

2.2. Caracterización del transistor

Una vez que el modelo es importado a AWR, un esquemático con el elemento IVCURVE es necesario para dibujar las curvas IV de nuestro transistor. Dichas curvas las podemos observar en la Figura 2.1.

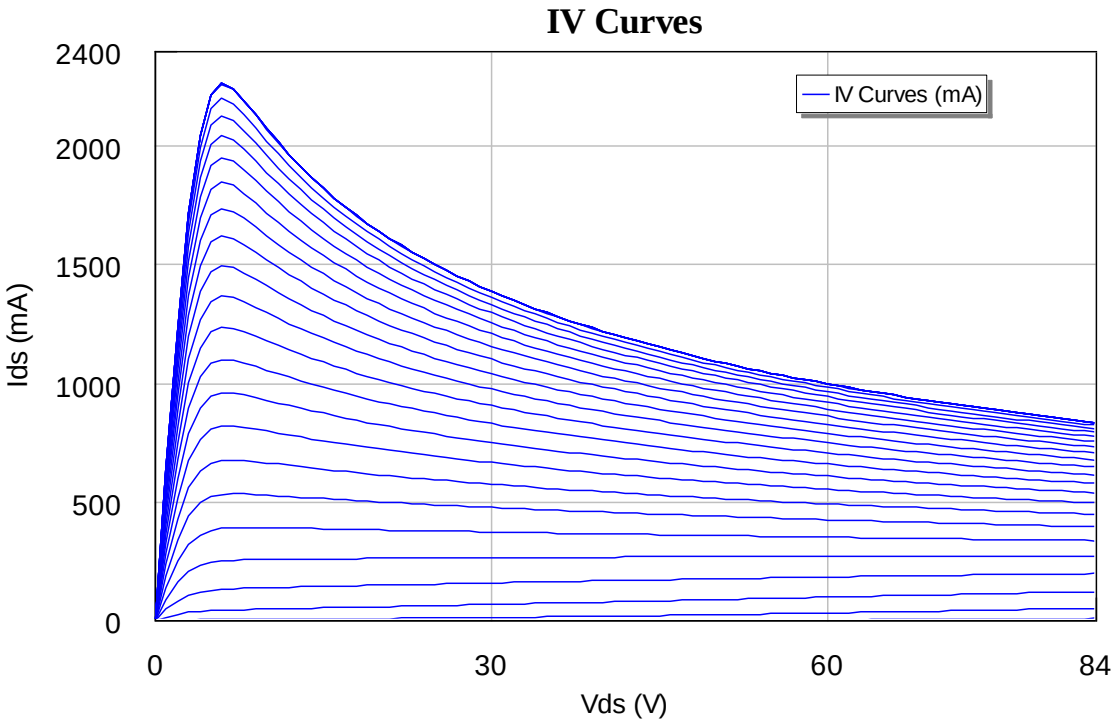


Figura 2.1 – Curvas IV del CGH40010.

2.3. Área de Operación Segura, punto de reposo (Q) y Línea de Carga Dinámica

Ahora debemos fijar las condiciones de alimentación. Fijando los voltajes de alimentación de la puerta (V_{gs}) y el drenador (V_{ds}) determinaremos la posición de nuestro punto de reposo en la región activa de las curvas IV. Para definir el *Área de Operación Segura,* necesitamos marcar en la gráfica de curvas IV los límites que hacen que el transistor o no funcione correctamente o se rompa. Dichos límites son cinco: corte, saturación, máxima corriente de drenador, máximo voltaje de drenador y máxima disipación de potencia.

Los límites de corte y saturación se obtienen de manera orientativa sobre la propia gráfica. La máxima corriente de drenador la obtenemos del datasheet del transistor además de la máxima potencia disipada.

$$P_{diss} = P_{gate} + P_{drain} \approx P_{drain} = V_{ds} \cdot I_{ds}$$

$$P_{dissMax} = 14 \approx V_{ds} \cdot I_{ds}$$

$$I_{ds} \approx \frac{14}{V_{ds}}$$

Esta última ecuación representa la curva de la máxima potencia disipada, con ella seremos capaces de dibujarla sobre las curvas IV y así delimitar la región segura de la región de sobrecalentamiento.

Dado que trabajamos en Clase A hemos decidido tomar los siguientes valores de alimentación:

$$V_{gs} = -2.2\ V$$

$$V_{ds} = 28\ V$$

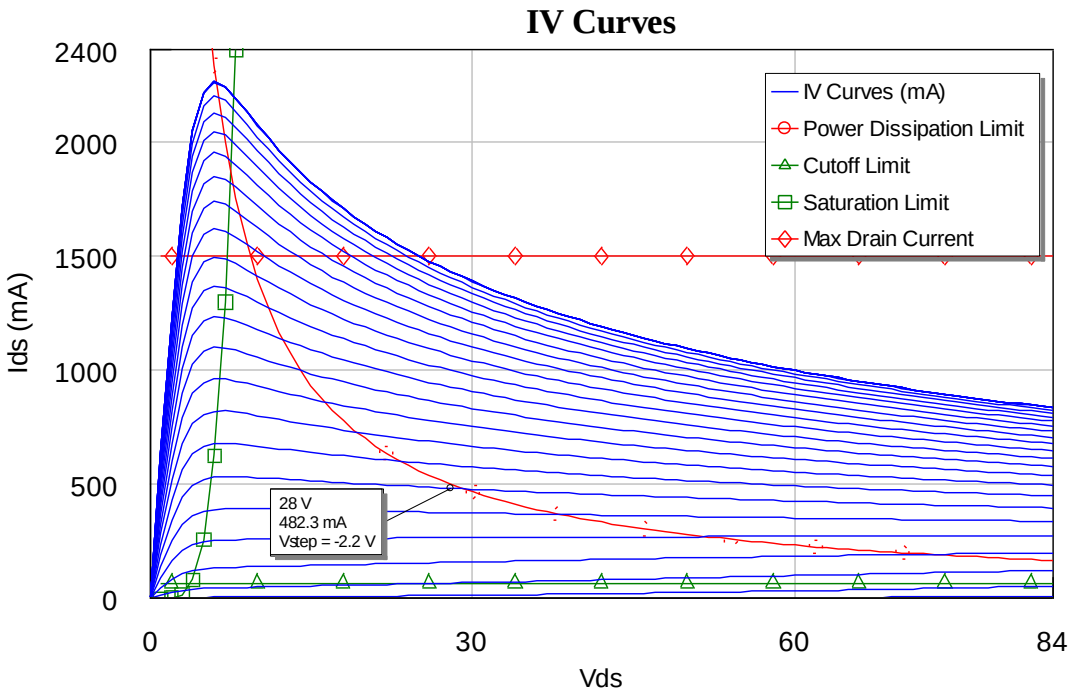


Figura 2.2 – Área de Operación Segura y Punto de Reposo.

Ahora pasamos a obtener el P_{1dB} para así dibujar la línea dinámica de carga con dicha potencia a la entrada.

Como podemos observar en la Figura 2.3, vemos que dicho valor está en 27.6dBm, por tanto, será el que aplicaremos a la entrada tal y como hacemos en la Figura 2.4.

Varias potencias hemos aplicado. Los resultados en términos de líneas dinámicas de carga se pueden observar en la Figura 2.5.

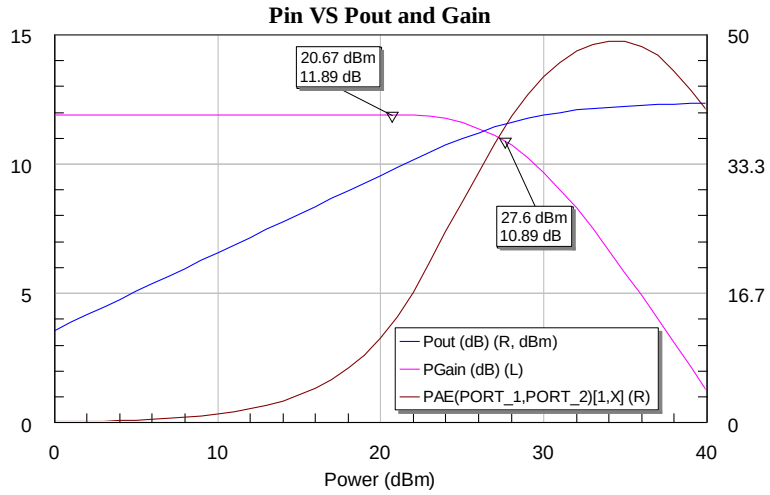


Figura 2.3 – CGH40010 P_{out}, Ganancia y PAE.

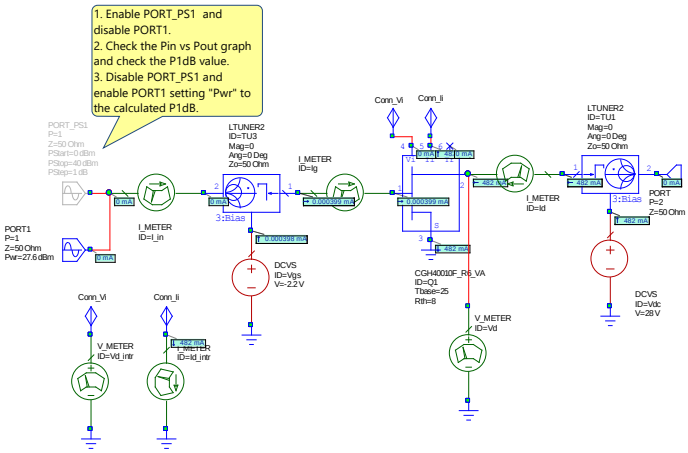


Figura 2.4 – Esquemático para testear, entre otras cosas, la ganancia, PAE y potencia de salida iniciales.

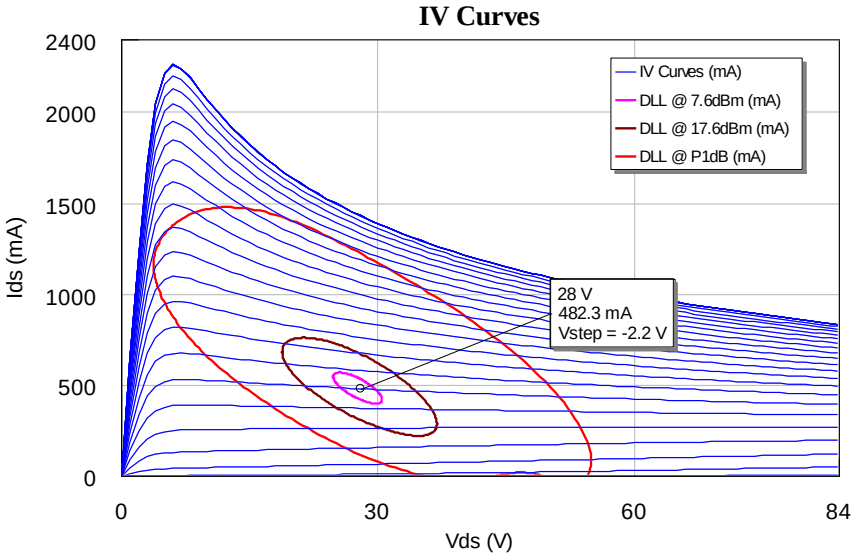


Figura 2.5 – Líneas dinámicas de carga para distintas potencias de entrada.

Aquí podemos observar una comparativa entre trabajar en región lineal (Figura 2.6 – arriba) y trabajar en región de saturación (Figura 2.6 – abajo) donde empiezan a aparecer no-linealidades.

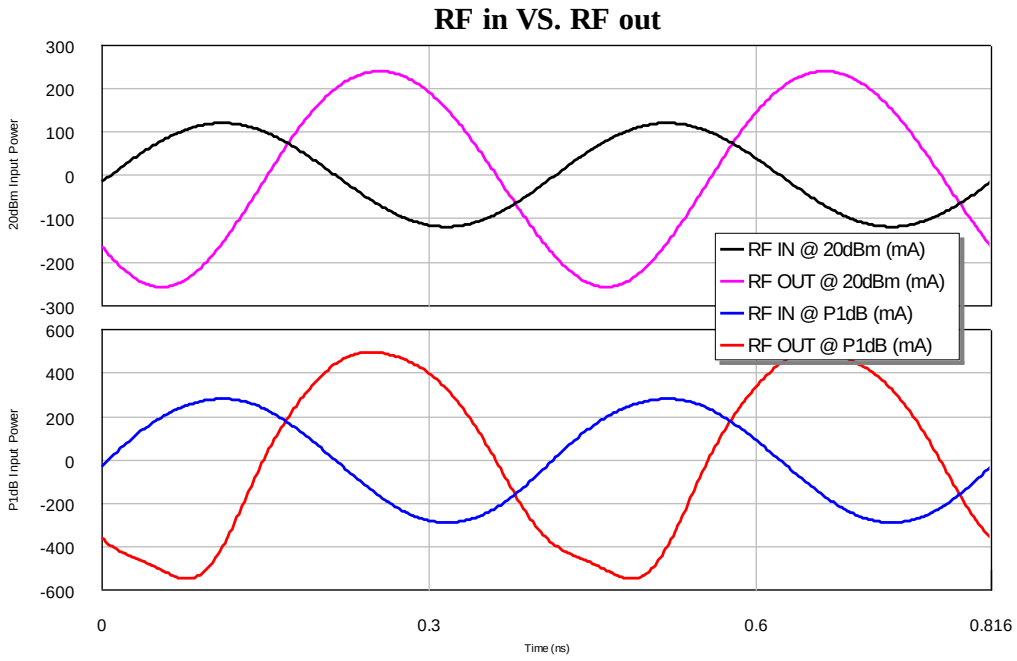


Figure 2.6 – Current waveforms both in linear and saturation.

2.4. Análisis de estabilidad

Realizar este estudio mediante AWR es muy sencillo. En *measurements* elegimos tanto *SCIR1,* para la estabilidad en la entrada, como *SCIR2*, para la estabilidad en la salida. Podemos ver el resultado en la Figura 2.7.

Las líneas discontinuas marcan la región del círculo que es inestable. En nuestro caso, las líneas discontinuas marcan que el interior de las circunferencias son las zonas inestables. Así pues, la intersección entre el interior dichas circunferencias y la carta de Smith serán las zonas que tendremos que evitar a la hora de diseñar tanto la red de entrada como la de salida.

Así que gracias a esta simple medida en AWR, podemos ahorrarnos todos los cálculos analíticos que supondría el llevarlo a cabo a mano.

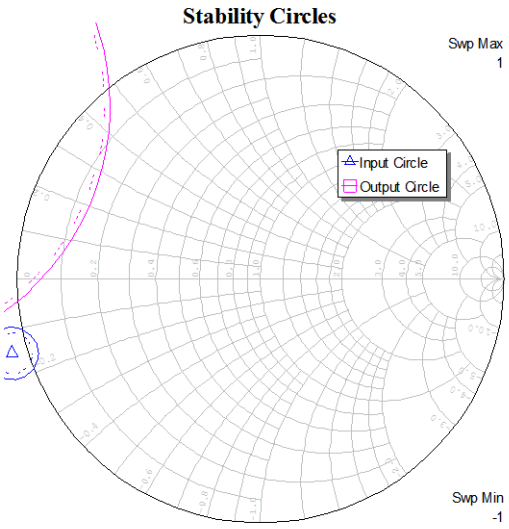


Figura 2.7 – Círculos de estabilidad de entrada y salida a 2.45GHz.

2.5. Simulación Load-Pull

Este método básicamente consiste en utilizar un elemento *LTUNER2,* el cual hace un barrido de coeficientes de reflexión en la red de salida, evaluando para cada punto los valores de PAE, ganancia y potencia disponibles, entre otros, con tal de encontrar el valor óptimo. El valor de coeficiente de reflexión a la salida tiene que entrar en concordancia con el estudio de estabilidad llevado a cabo anteriormente, esto es, no elegir un punto que esté dentro de la región inestable.

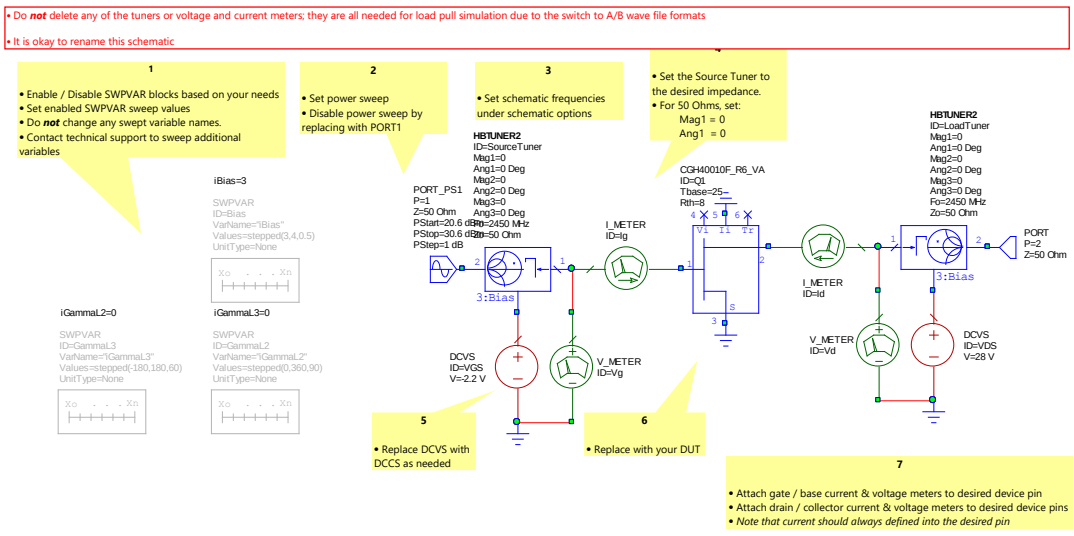


Figura 2.8 – Plantilla de Load-Pull generada automáticamente por AWR.

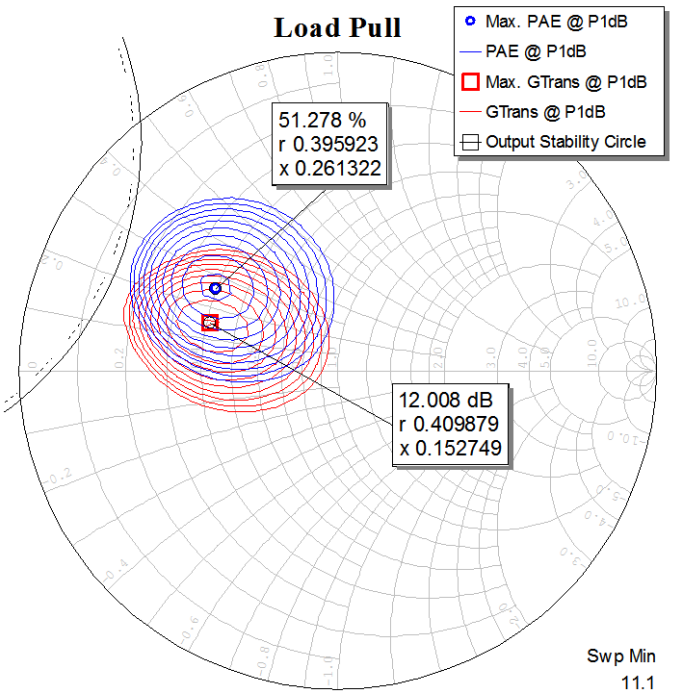


Figura 2.9 – Contornos de G_{Trans} y PAE.

Como podemos observar en la Figura 2.9, tanto el máximo en PAE como el máximo en ganancia están muy cerca, lo que nos hace decidirnos por un punto en esa zona, ya que además se encuentra en la región estable. Este punto es

$$\Gamma_{out} = 0.44152\angle 149.3904°$$

La red de adaptación de salida que nos proporciona dicho coeficiente de reflexión es la mostrada en la Figura 2.10.

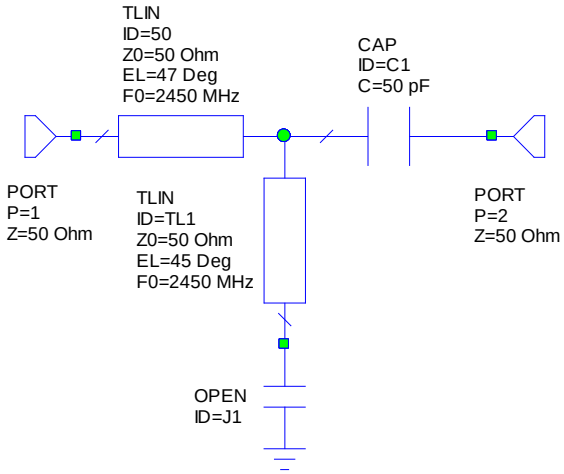


Figure 2.10 – Red de adaptación a la salida.

La función del condensador *C1* es la de bloquear el paso de la DC así la alimentación va directamente al drenador y no se pierde por el puerto de salida.

Ahora, llevamos a cabo un análisis manual con el optimizador de AWR. Los resultados obtenidos concuerdan con lo que dice la teoría: la máxima transferencia de potencia se producirá cuando el coeficiente de reflexión de la carga sea igual al conjugado al coeficiente de reflexión que se ve hacia la puerta del transistor. Dicho valor es el siguiente

$$\Gamma_S = 0.85\angle -163°$$

Este resultado no es exactamente el conjugado, ya que el conjugado estaba muy cerca de la zona de inestabilidad lo que nos hizo escoger un valor un poco más alejado de esa zona y más cercano al centro de la carta de Smith.

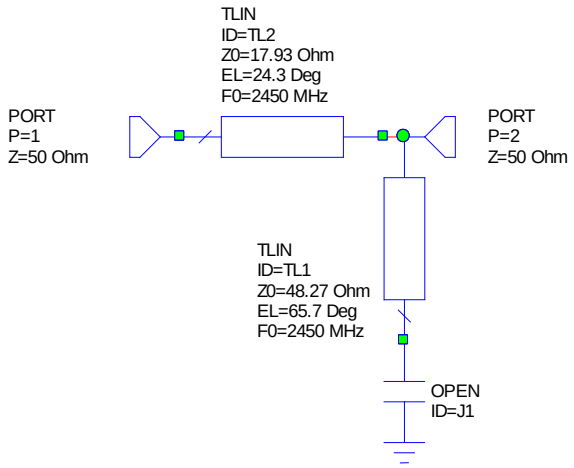


Figura 2.11 – Red de adaptación a la entrada.

2.6. Redes de alimentación

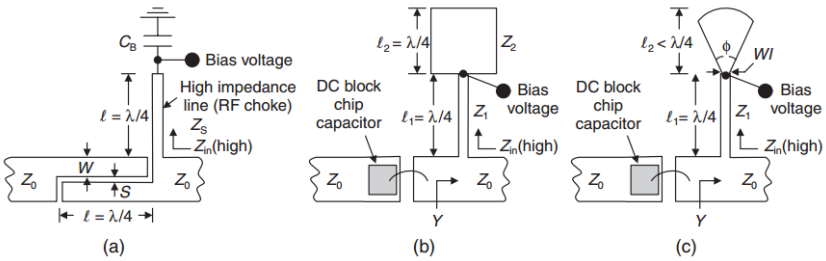


Figure 2.12 – Circuitos de alimentación de microondas simplificados: (a) bloqueo de DC por línea acoplada y transformador de λ/4, (b) bloqueo de DC con condensador MIM y dos transformadores λ/4, y (c) bloqueo de DC por condensador MIM y un transformador de λ/4 en serie con un stub radial.

En el diseño sin pérdidas inicial (ideal) decidimos usar la segunda configuración mostrada en la Figura 2.12. El diseño final sin pérdidas se puede ver en la Figura 2.14 y los resultados de PAE, ganancia y potencia de salida se muestran en la Figura 2.13.

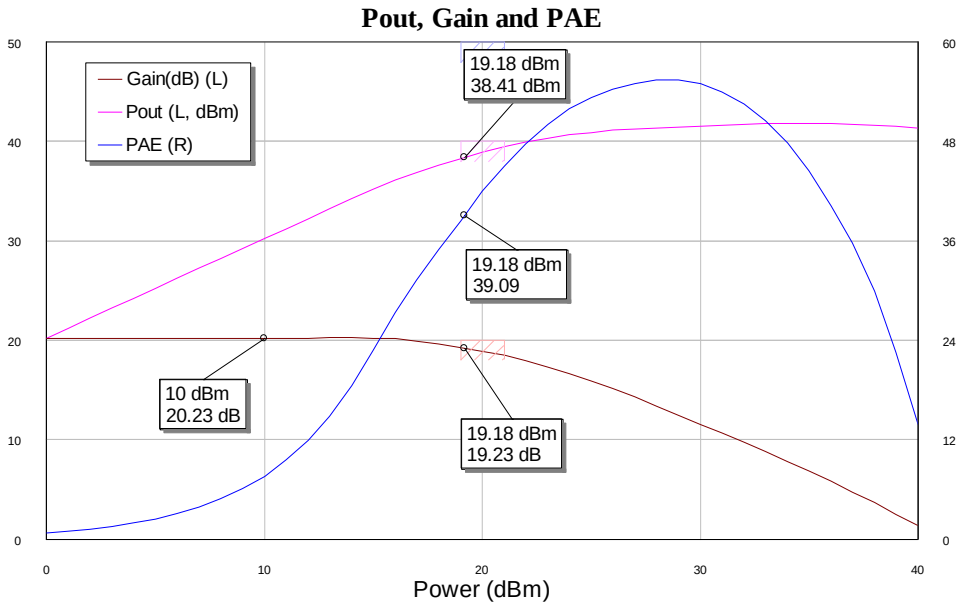


Figura 2.13 – P_{out}, ganancia y PAE obtenidos con el diseño ideal.

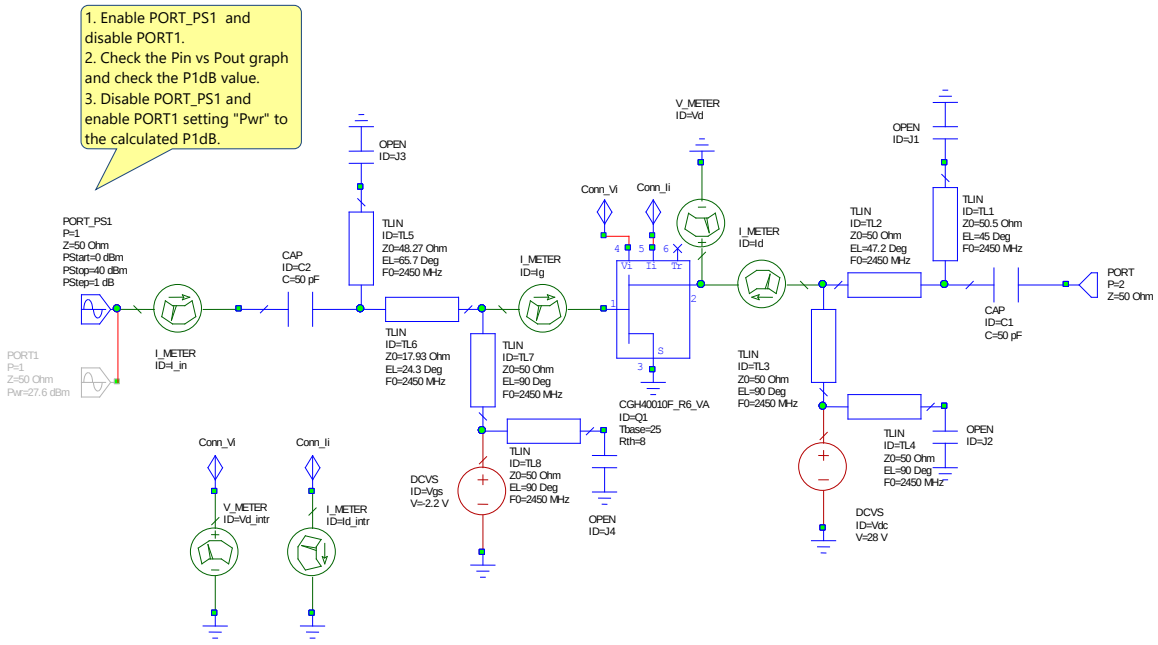


Figura 2.14 – Diseño final con líneas de transmisión ideales.

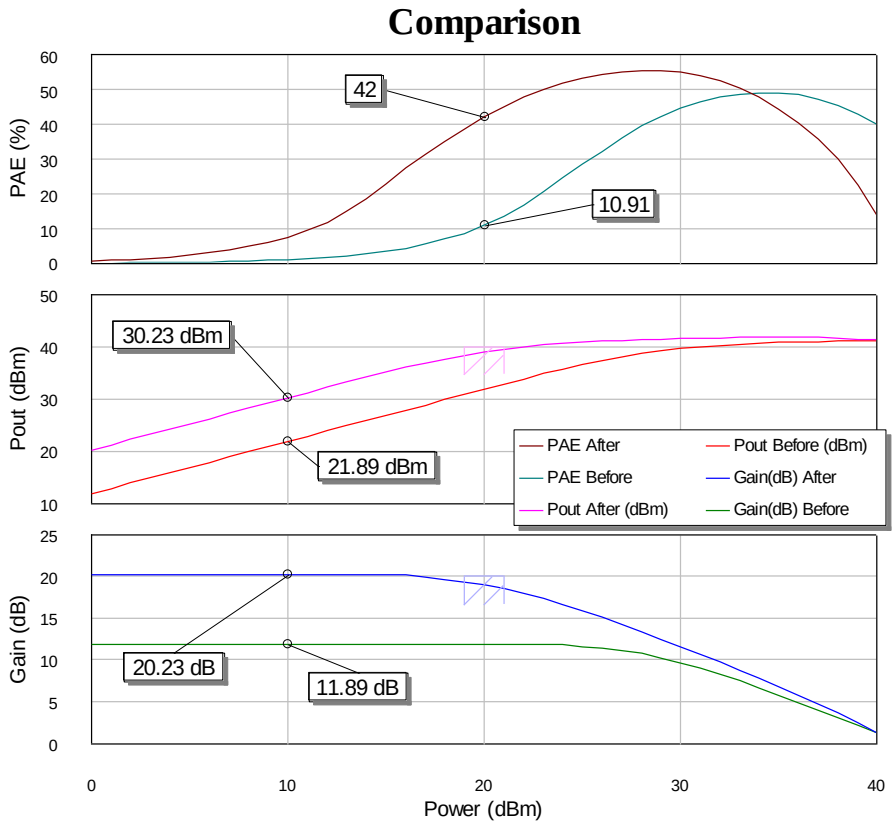


Figura 2.15 – Comparación entre el diseño realizado y el transistor sin ningún tipo de red de adaptación.

Tal y como podemos observar en la Figura 2.15, hemos mejorado el rendimiento de nuestro amplificador con esta configuración final.

Ahora, el principal problema es que hemos obtenido unos parámetros S muy malos, además de poca estabilidad. Dicho problema se puede evitar añadiendo una resistencia a la puerta.

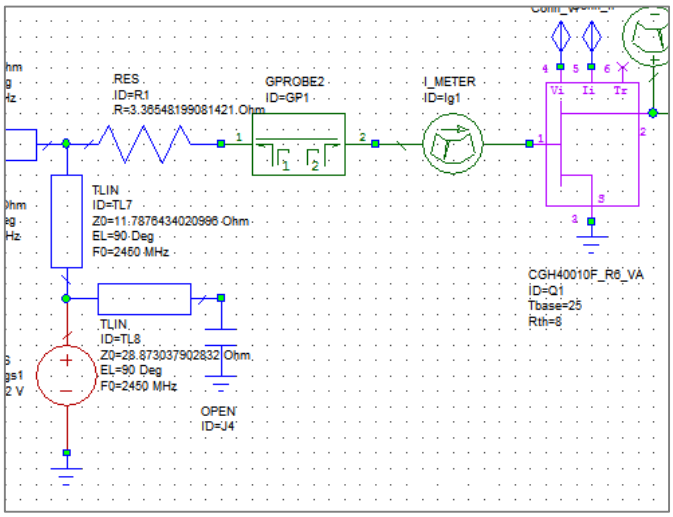


Figura 2.16 – Resistencia añadida a la puerta para mejorar en estabilidad y en adaptación a f_0.

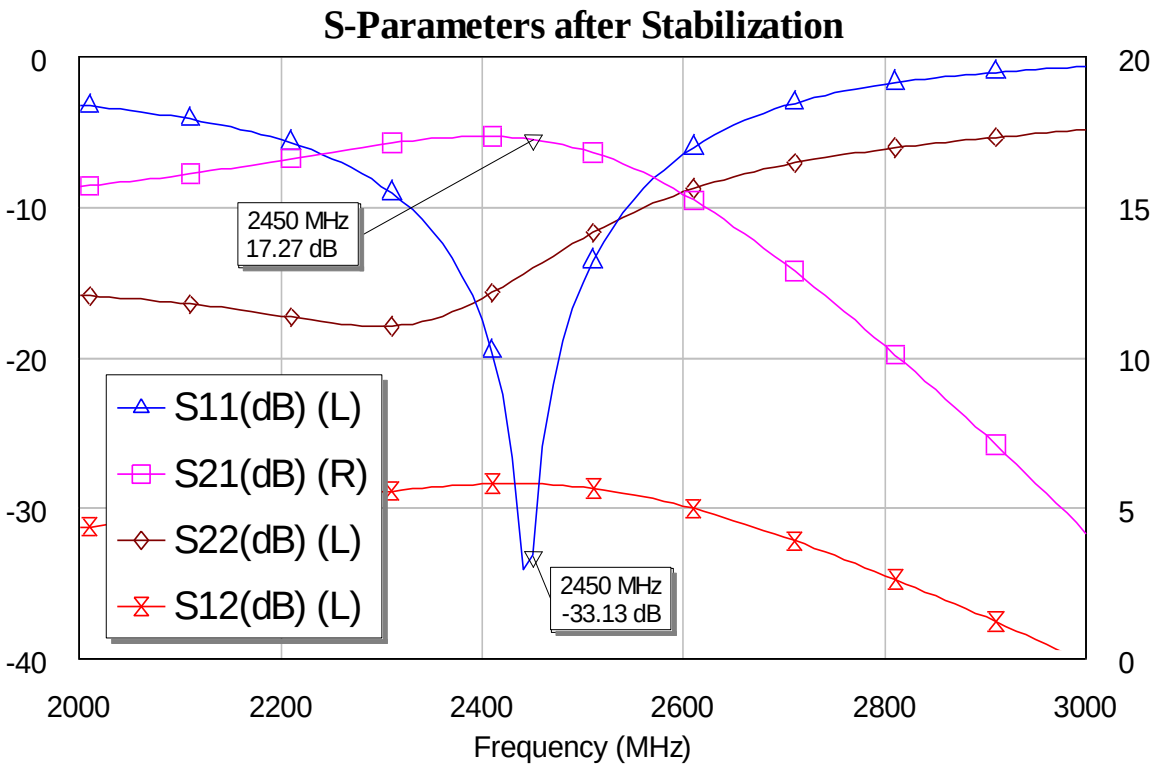


Figura 2.17 – Adaptación mejorada al colocar la resistencia en la puerta.

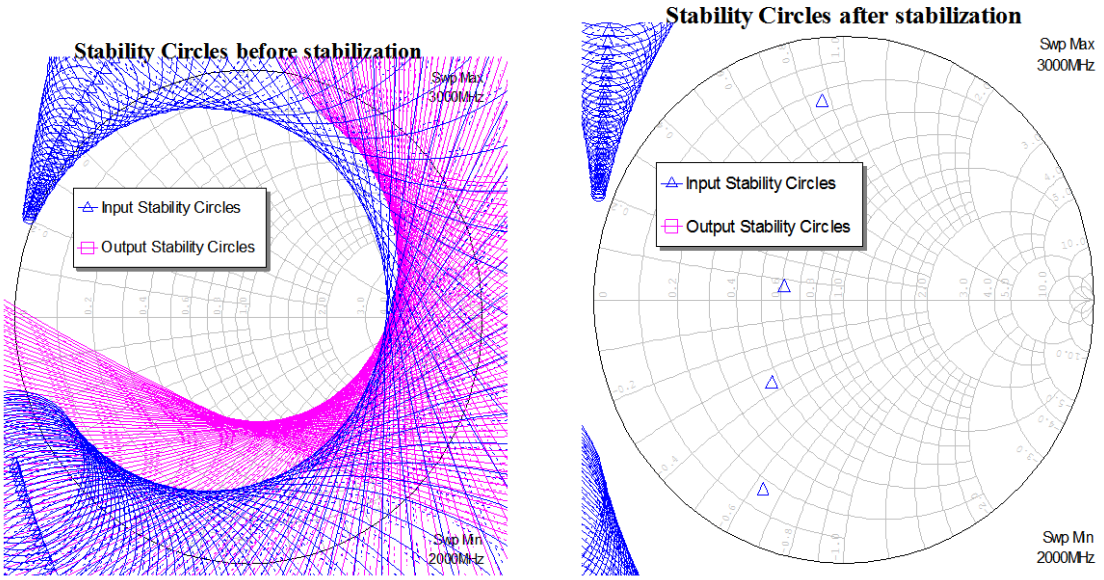


Figura 2.18 – Círculos de estabilidad antes (izquierda) y después (derecha) de colocar la resistencia en la puerta del transistor. Se puede observar que conseguimos estabilidad incondicional entre 2 y 3 GHz.

2.7. Diseño real

Al pasar a un diseño real (con pérdidas) debemos, primero, saber el sustrato que vamos a utilizar. El sustrato elegido ha sido el modelo RO4350B-LoPro de Rogers Corp. (20 micras de grosor). Nos decidimos por este grosor debido a que cuanto más fino sea el sustrato, mejor conductividad térmica tendremos.

Para tener en cuenta dicho sustrato en nuestras simulaciones, debemos incluir en nuestro esquemático el elemento *MSUB*, al cual deberemos darle los parámetros del sustrato que podemos encontrar en el datasheet del mismo.

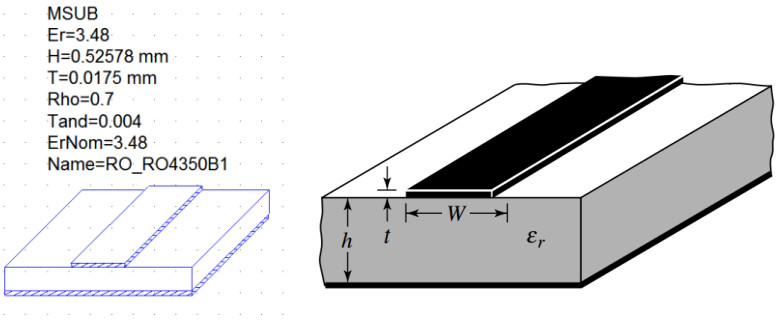


Figura 2.19 – Elemento *MSUB* (izquierda) y parámetros de la línea microstrip (derecha).

Una vez hecho esto, pasamos a reemplazar todas las líneas *TLIN* por líneas que simulan pérdidas, líneas reales, llamadas *MLIN.* Además, debido a la mala respuesta de la red de alimentación, decidimos cambiarla por la tercera configuración de la Figura 2.12, esto es, con stub radial en paralelo además de una línea de alta impedancia que conecta dicho stub radial con la red de adaptación de entrada. Con esta configuración mejoramos el ancho de banda además de que el stub radial hace mejor su función como inductor bloqueando el paso de RF. La red de alimentación la podemos observar en la Figura 2.20.

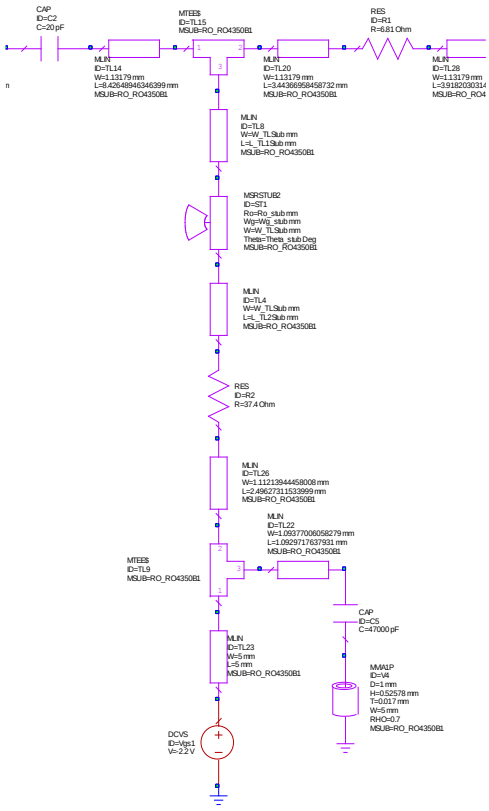


Figura 2.20 – Esquemático de la red de alimentación con pérdidas.

Aparte del stub radial bloqueador de RF, usamos una resistencia entre dicho bloqueador y la alimentación. Su propósito no es más que estabilizar las bajas frecuencias.

Fuera de nuestro ancho de banda habrán ciertas frecuencias que no verán altas impedancias a través de la red de alimentación por lo que es importante usar condensadores de desacoplo en paralelo con la fuente de alimentación. De esta manera, la RF que se cuele quedará cortocircuitada por este condensador.

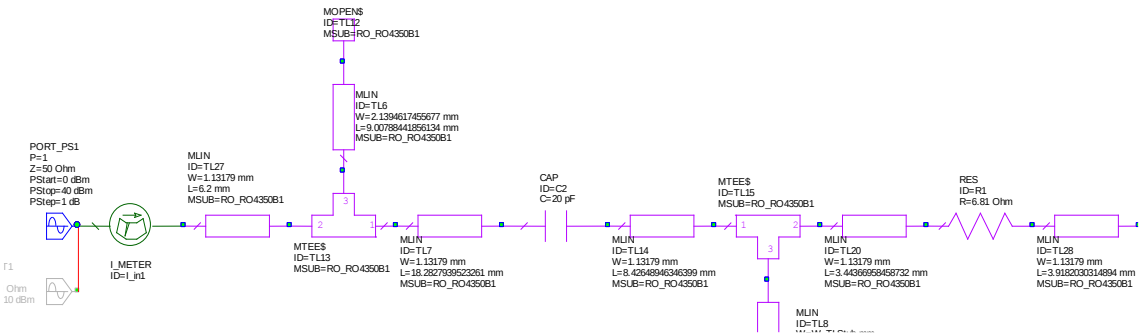


Figura 2.21 – Esquemático de la red de adaptación a la entrada con pérdidas.

Como podemos ver en la Figura 2.21 usamos como red de adaptación un stub acabado en abierto y algunas líneas de transmisión en serie con la misma anchura y, por lo tanto, impedancia (50 Ω).

En la red de adaptación a la salida, como se puede observar en la Figura 2.22, usamos un doble stub acabado en abierto además de un solo stub acabado también en abierto. El condensador responsable de evitar la fuga de DC por el puerto de salida se ha colocado en el centro ya que durante el proceso de optimización nos dio mejores resultados en dicha posición. Dicho proceso de optimización se llevó a cabo teniendo en cuenta la obtención de la mejor adaptación, ganancia y estabilidad.

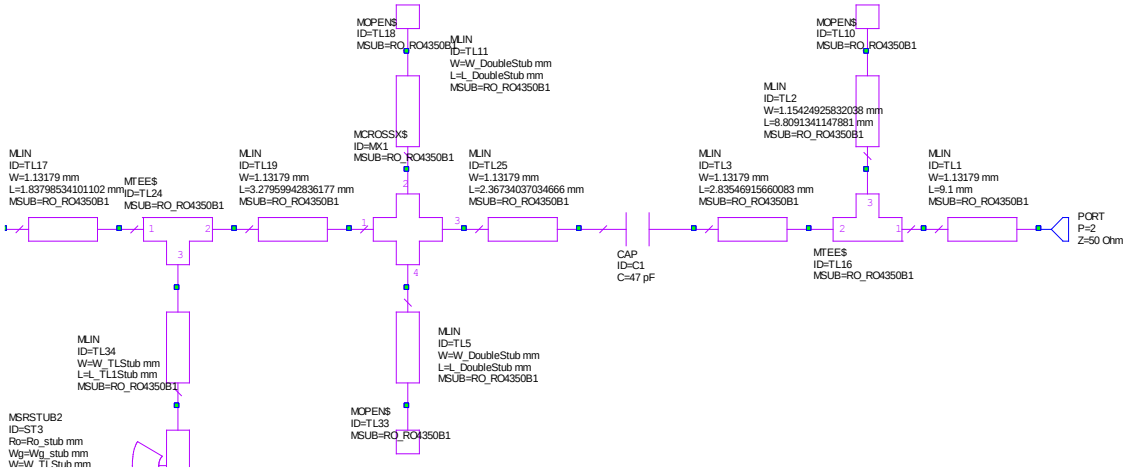


Figura 2.22 – Esquemático de la red de adaptación a la salida con pérdidas.

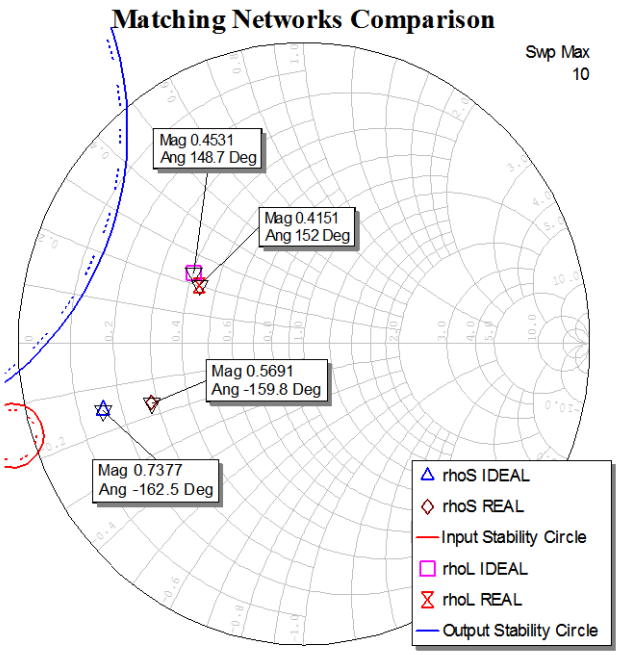


Figura 2.23 – Redes de adaptación reales (con pérdidas) Vs. Redes de adaptación ideales (sin pérdidas).

Para tener una idea de cuán diferentes son las redes de adaptación reales e ideales se ha realizado una comparativa de los coeficientes de reflexión asociados en la Figura 2.23. Se puede observar en dicha Figura que dichos coeficientes están bastante cercanos a lo que se buscaba idealmente.

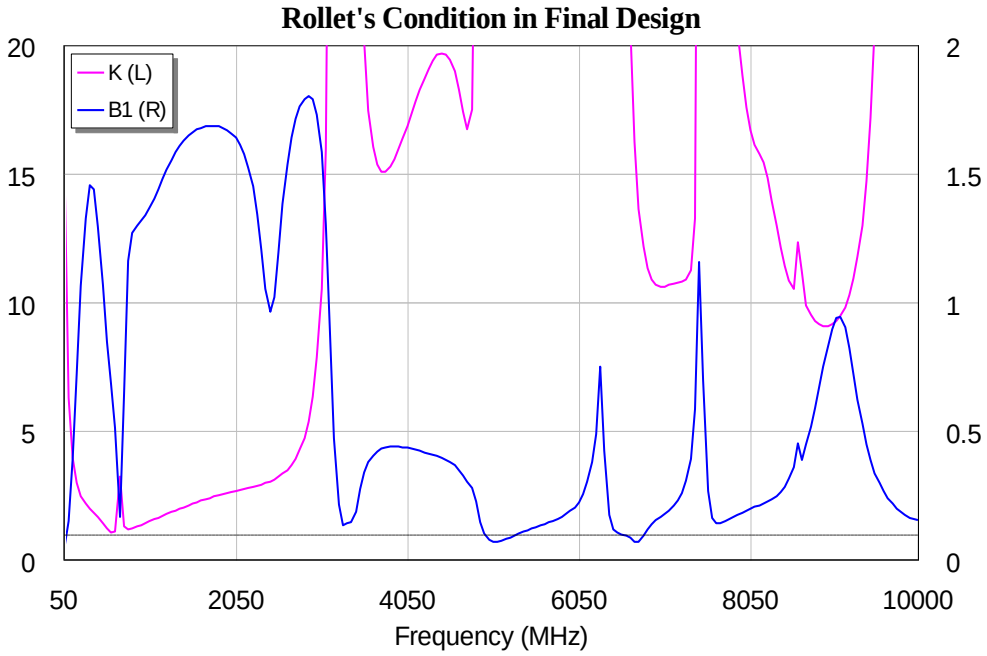


Figura 2.24 – Test final de estabilidad incondicional.

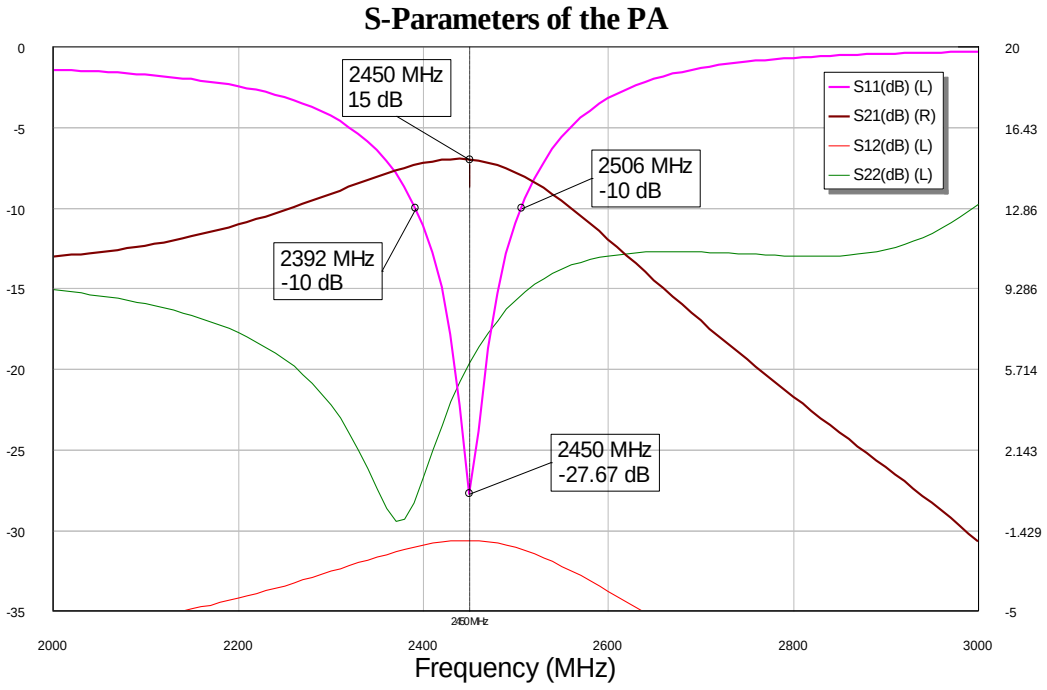


Figura 2.25 – Parámetros S del diseño final.

La estabilidad incondicional se ha comprobado en un amplio rango de frecuencias (entre 0.05 y 10GHz) con resultados muy positivos como se muestra en la Figura 2.24.

Además, los parámetros S, mostrados en la Figura 2.25, nos muestra que alcanzamos una ganancia de unos 15dB a la frecuencia de trabajo (2.45GHz) y alrededor de unos 100MHz de ancho de banda a -10dB.

Finalmente, comparamos el rendimiento del transistor con el que proporciona el diseño realizado con pérdidas. Dicho diseño mejora al transistor unos 3dB, aproximadamente.

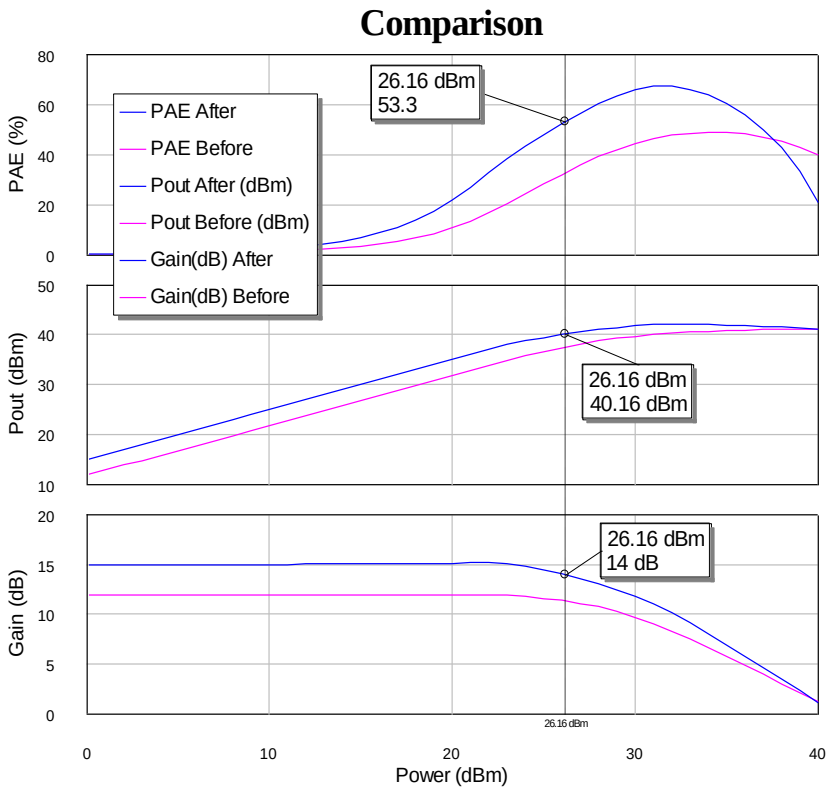


Figura 2.26 – Comparación final – Transistor Vs. Diseño final.

Antes de empezar a trabajar en el proceso de fabricación es importante hacer una simulación final teniendo en cuenta las pérdidas por acoplo y otros fenómenos provocados por la interacción de campos electromagnéticos. Debido a que el análisis llevado a cabo hasta ahora ha sido a nivel circuital, tenemos ahora que incorporar las interacciones de los campos y observar cómo afectan a nuestro diseño final.

La simulación que incorpora estas interacciones es bastante lenta ya que debe tener en cuenta muchas más cosas. Haciendo ahora una comparación sin tener y teniendo en cuenta la interacción de los campos podemos observar que no se manifiesta un cambio significativo.

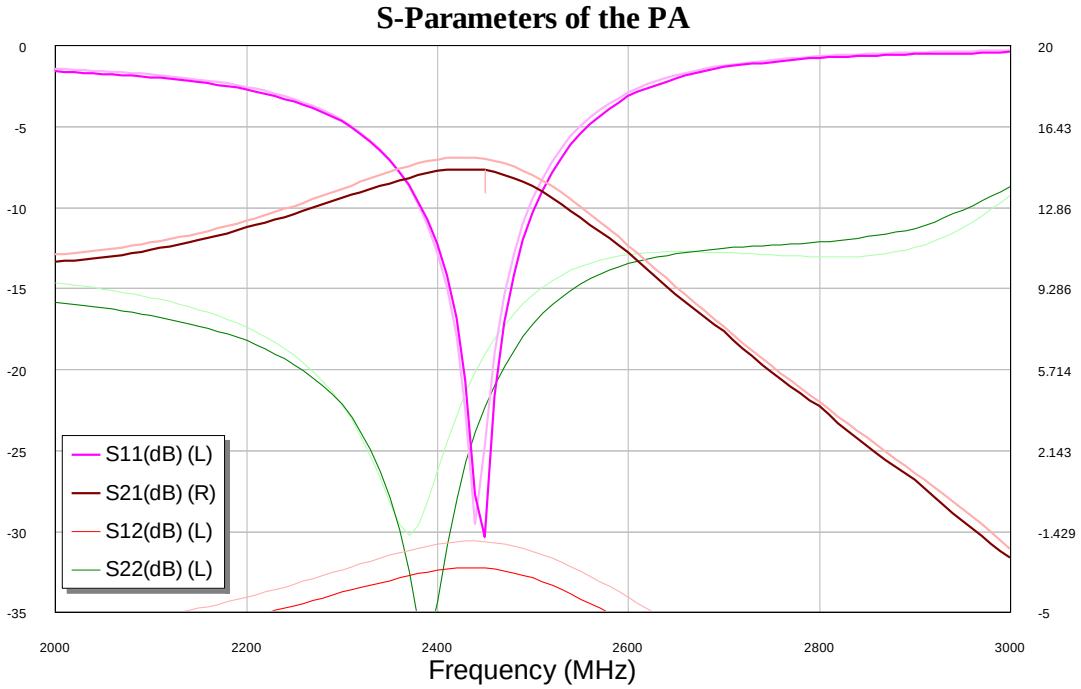


Figura 2.27 – Comparación con y sin extracción electromagnética (EM Extraction).

En la Figura 2.28 podemos observar el aspecto de nuestro diseño final en tecnología microstrip, listo para empezar el proceso de fabricación.

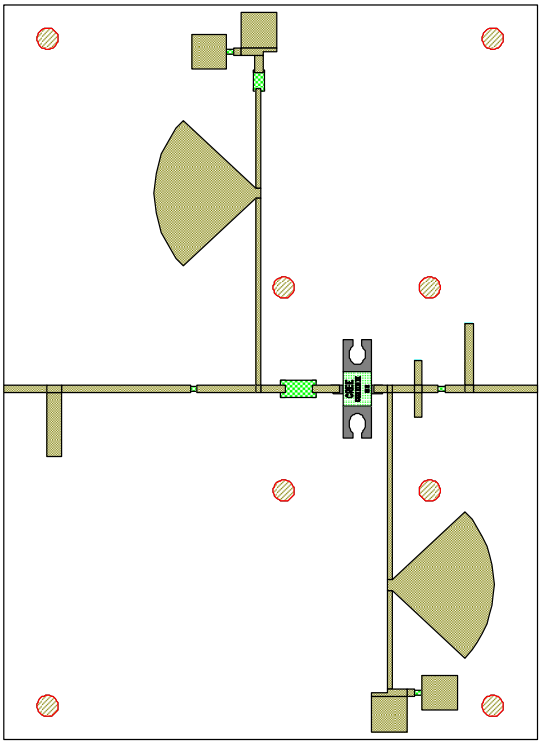


Figura 2.28 – Diseño final.

3. Proceso de Fabricación y Testeo

3.1. Elección del disipador de calor

Buscando un disipador en el catálogo de *Wakefield-Vette* encontramos el modelo *641k*. Dicho modelo tiene unas características de convección natural y forzada como las que muestra la Figura 3.1.

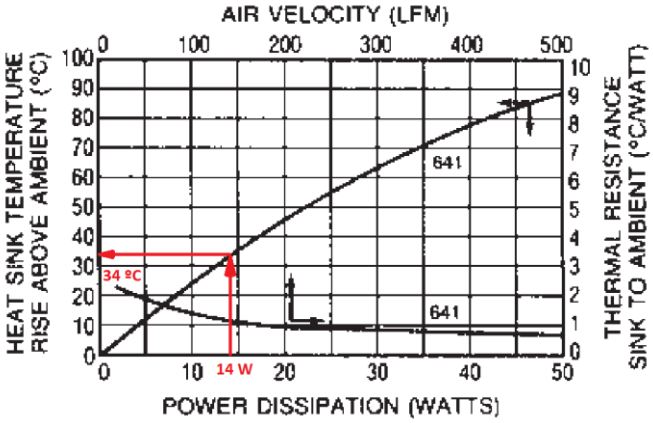


Figura 3.1 – Características de convección natural y forzada de nuestro disipador.

Considerando que disipamos alrededor de 14 vatios, tenemos una subida de temperatura sobre la temperatura ambiente de unos 34ºC, aproximadamente. Así pues,

$$\theta_{sa\ (641k)} = \frac{34\ ºC}{14\ W} \simeq 2.43\ ºC/W$$

Por lo que el nuevo valor θ_{ja} sería

$$\theta_{ja\ (641k)} = \theta_{jc} + \theta_{cs} + \theta_{sa\ (641k)} = 8 + 0.5 + 2.43 = 10.93\ ºC/W$$

Teniendo el peor caso

$$T_{j\ (641k)} = \theta_{ja\ (641k)} \cdot P_D + T_a = 10.93 \cdot 13.496 + 25 \simeq 172.51\ ºC \quad (max. 225\ ºC)$$

$$T_{c\,(641k)} = T_{j\,(641k)} - \theta_{jc} \cdot P_D = 172.51 - 8 \cdot 13.496 \simeq 64.54\,ºC \quad (max.\,150\,ºC)$$

Estos valores corroboran que este disipador trabajará bien incluso en el peor caso.

3.2. Conexión a tierra del transistor

La resistencia térmica del pin de la fuente al disipador es el material interfaz empleado para hacer buen contacto térmico entre el transistor y el disipador, en nuestro caso, pasta térmica. Esto significa que el transistor va en contacto directo con el disipador. Hay dos razones que avalan esta configuración:

1. Rendimiento térmico. Si no realizamos la muesca en el sustrato, entonces tendríamos que usar el sustrato como material interfaz entre el transistor y el disipador. Esto no es aconsejable porque la resistencia térmica del pin de la fuente al disipador aumentaría demasiado aumentando la posibilidad de quemar el transistor por sobrecalentamiento.
2. Reducción de la inductividad asociada a la conexión con tierra. Si optamos por no quitar el sustrato en esa área, deberemos hacer muchos agujeros para evitar que se generen inductancias indeseadas. Es mucho más conveniente quitar esa área de sustrato y “hacer una buena tierra”.

El slot llevado a cabo en el sustrato se puede observar en la Figura 3.2 (derecha) marcado en rojo.

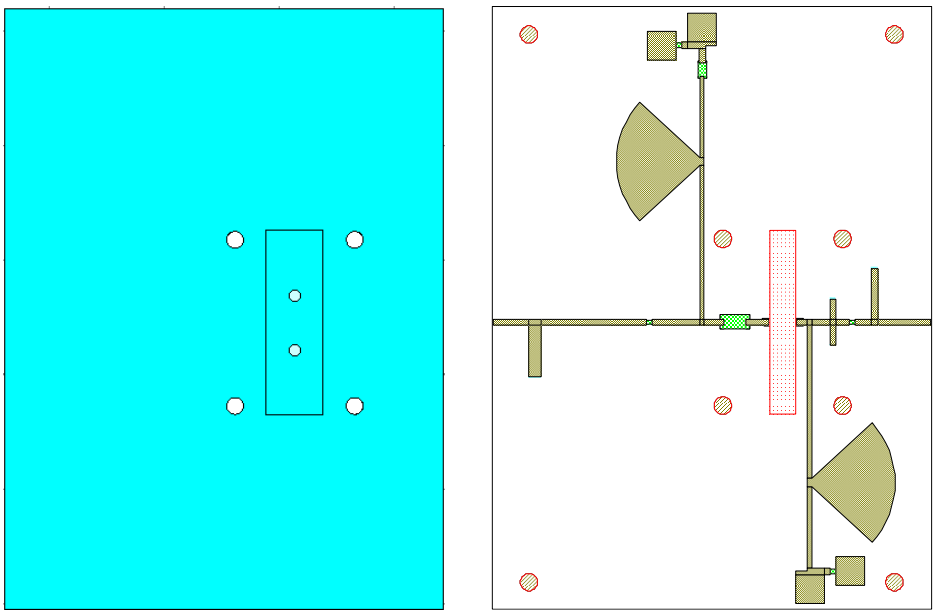


Figura 3.2 – Vista frontal del disipador modificado (izq.) y muesca en el sustrato marcada en rojo (derecha).

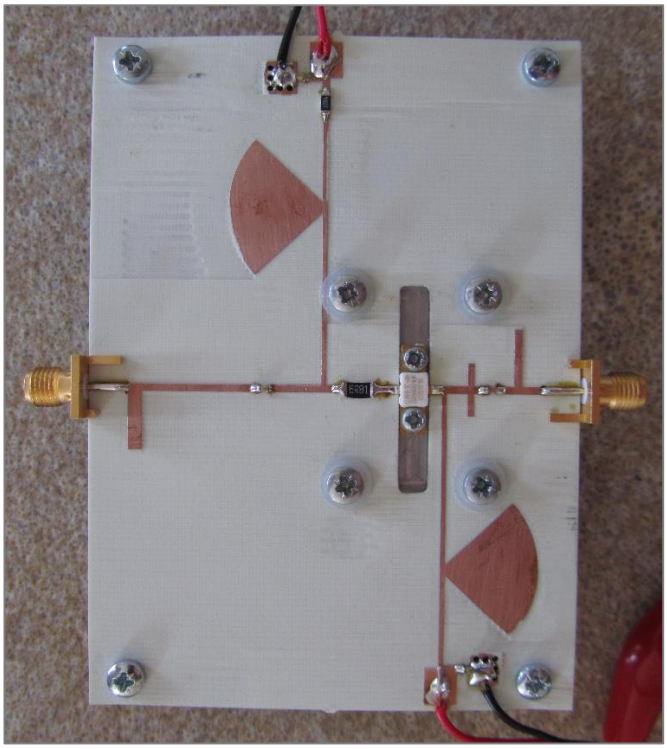


Figura 3.3 – Diseño acabado y listo para el testeo en el laboratorio.

Finalmente montamos el sustrato y el transistor en el disipador junto con todos los componentes. Entre el transistor y el disipador se ha aplicado una fina capa de pasta térmica. El resultado final se puede ver en la Figura 3.3.

3.3. Testeo

Para la alimentación usamos dos fuentes de corriente continua independientes.

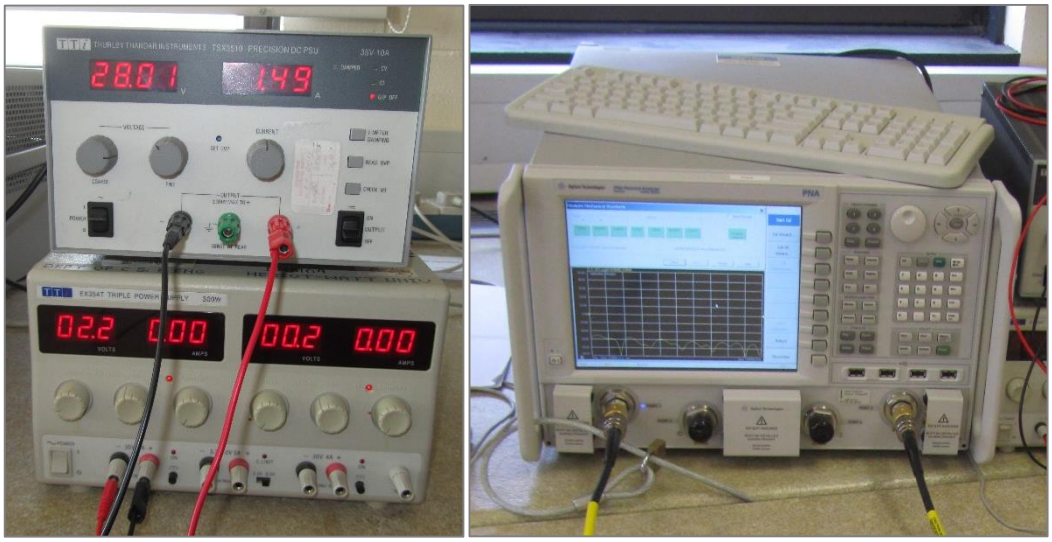


Figura 3.4 – Fuentes de alimentación (izquierda). PNA Agilent N5225A (derecha).

Para el análisis de puertos usamos el PNA (Programmable Network Analyzer) Agilent N5225A.

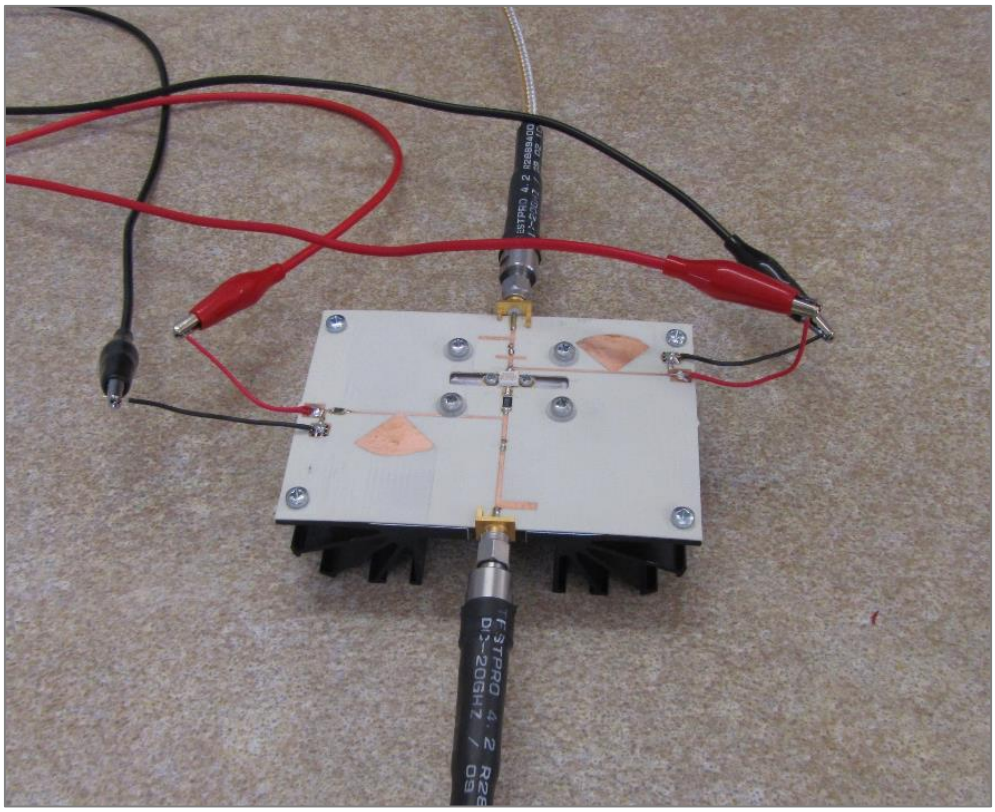


Figura 3.5 – Amplificador alimentado.

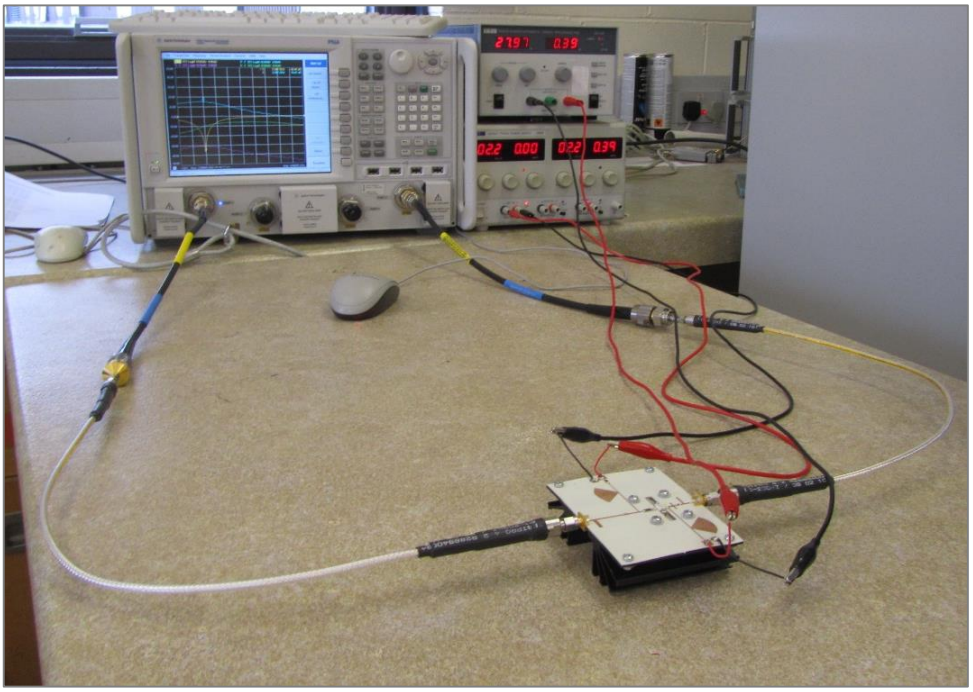


Figura 3.6 – Testeando el amplificador.

3.4. Resultados

Tal y como podemos observar en la Figura 3.7, los parámetros S son muy similares a los simulados, pero tienen la particularidad de que están desplazados en frecuencia unos 250MHz a la izquierda.

La solución a este problema es relativamente sencilla. La técnica empleada para solucionar esto es la de redimensionar el diseño a una escala que se puede calcular de la siguiente manera,

$$Resize\ factor = \frac{f_{shifted}}{f_0} = \frac{2200}{2450} = \frac{44}{49} \simeq 0.898$$

Con este factor re-escalamos el tamaño a un diseño más pequeño, y con ello el problema debería desaparecer. El único parámetro que no coincide con los valores simulados es el S_{22}.

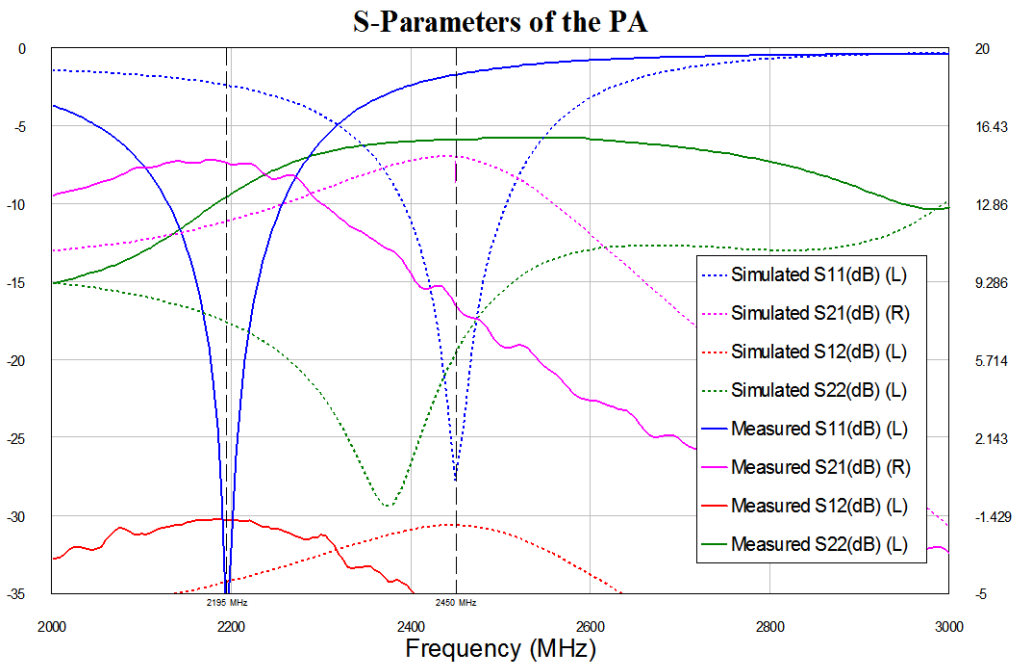


Figura 3.7 – Parámetros S Medidos Vs. Simulados.

3.5. Problema térmico

Cuando el amplificador se encontraba funcionando aproximadamente unos 4 minutos, los parámetros S comenzaron a desplazarse y desde entonces no volvieron a su posición inicial. Las posibles causas a este problema podrían ser:

a. La pasta térmica posiblemente no ha sido aplicada de manera correcta. La cantidad puede haber sido insuficiente también.
b. El punto de reposo elegido (Q-Point) se encuentra casi en el límite de potencia disipada, lo cual hace que el transistor tenga mayores probabilidades de quemarse por sobrecalentamiento.
c. Las medidas de los parámetros S fueron hechas con una potencia de entrada de 0dBm. Bajas potencias de entrada desembocan en baja PAE. Y baja PAE significa que la mayor parte de la potencia suministrada al transistor está siendo disipada en calor.

A causa de este problema no fuimos capaces de medir otros parámetros interesantes como la PAE, ganancia, no-linealidades, etc.

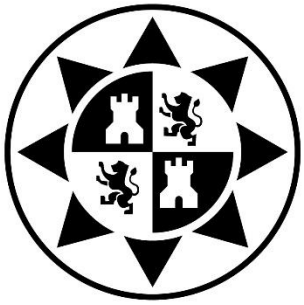
3.6. Conclusiones

El análisis, implementación, simulación, fabricación y testeo de un Amplificador de Potencia de clase A en la banda ISM ha sido propuesto. Los resultados iniciales fueron buenos: 15dB de ganancia, P_{1dB} a 26dBm aproximadamente y estabilidad incondicional en un amplio rango de frecuencias gracias a las resistencias empleadas.
Los malos resultados del final hacen de este trabajo como una fuente potencial de aprendizaje sobre los problemas surgidos para futuros diseños.

3.7. Líneas futuras

Los principales caminos que se deberían tomar con este trabajo deberían ser:

1. Investigar y resolver el problema térmico que hizo sobrecalentar al transistor.
2. Hacer más y variadas medidas para comprobar el correcto funcionamiento y para aprender cómo usar el PNA para este propósito.
3. Intentar estandarizar el proceso de diseño de un amplificador de potencia y hacerlo más práctico.
4. Levar a cabo el diseño de una clase B y AB, entonces seremos capaces de comparar estas tres clases en términos de ruido, no-linealidades, ganancia, eficiencia, etc.



HERIOT-WATT UNIVERSITY – POLYTECHNIC UNIVERSITY OF CARTAGENA

2.45GHz Class A GaN HEMT Power Amplifier Design

FINAL DEGREE PROJECT

Author: Pascual David Hilario Re

Supervisor: José Luis Gómez Tornero

Second supervisor: George Goussetis

Cartagena, October 2015

To my family…

…who made me who I am

To Estela…

…who has supported me so much in difficult times

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Co-director	George Goussetis
Title	2.45GHz Class A GaN HEMT Power Amplifier Design

Abstract

Today, solid state amplification is dominated by use of three-terminal transistors. Using a small voltage applied at the input terminal of the device, one can control, in an efficient manner, a large current at the output terminal when the common terminal is grounded. This is the source for the name transistor, which is a unification of the words transfer resistor.
Thanks to transistors amplification exists and this project is focused in the design process that an engineer must follow in order to create it, from initial simulations in software until testing in the lab.

Degree	Telecommunications Engineering
Department	Communication and Information Technologies
Submission date	October 2015

Contents

1. Introduction

Signal amplification is one of the most important radiofrequency (RF) and microwave circuit functions. The introduction of radar during World War II provided the first significant application requiring amplification of microwave signals. Nowadays, the wireless communication revolution has provided an explosion of RF and microwave amplification applications. During the last two decades, amplifier technology has made tremendous progress in terms of devices (low noise and power), circuit computer-aided design (CAD) tools, fabrication, packaging, and applications. Low-cost power amplifiers for wireless applications are a testament to this explosion.

Early microwave amplifiers were the exclusive province of vacuum tube devices such as Klystrons, traveling-wave tube (TWT) amplifiers and magnetrons (Figure 1.1). Today, microwave amplification is dominated by solid state amplifiers except for applications at high output powers (≥100 watts). Today, the most common vacuum tube application is the 900-watt microwave oven using a 2.45GHz magnetron. The power levels achievable for tube amplifiers are on the order of 103 higher than achievable for solid state amplifiers.

Solid state amplifiers are of two general classes: those based on two-terminal negative resistance diode devices, and those based on three-terminal devices known as transistors. Early solid state amplifiers were dominated by two-terminal devices because diodes are typically much easier to fabricate than transistors. Quite an array of two-terminal amplifier designs have been introduced, including parametric amplification (varactor diodes), tunneling diodes, transferred electron diodes (Gunn and LSA diodes) and avalanche transit-time diodes (IMPATT, TRAPATT and BARITT). Such diodes are used only for special amplifier functions. [1]

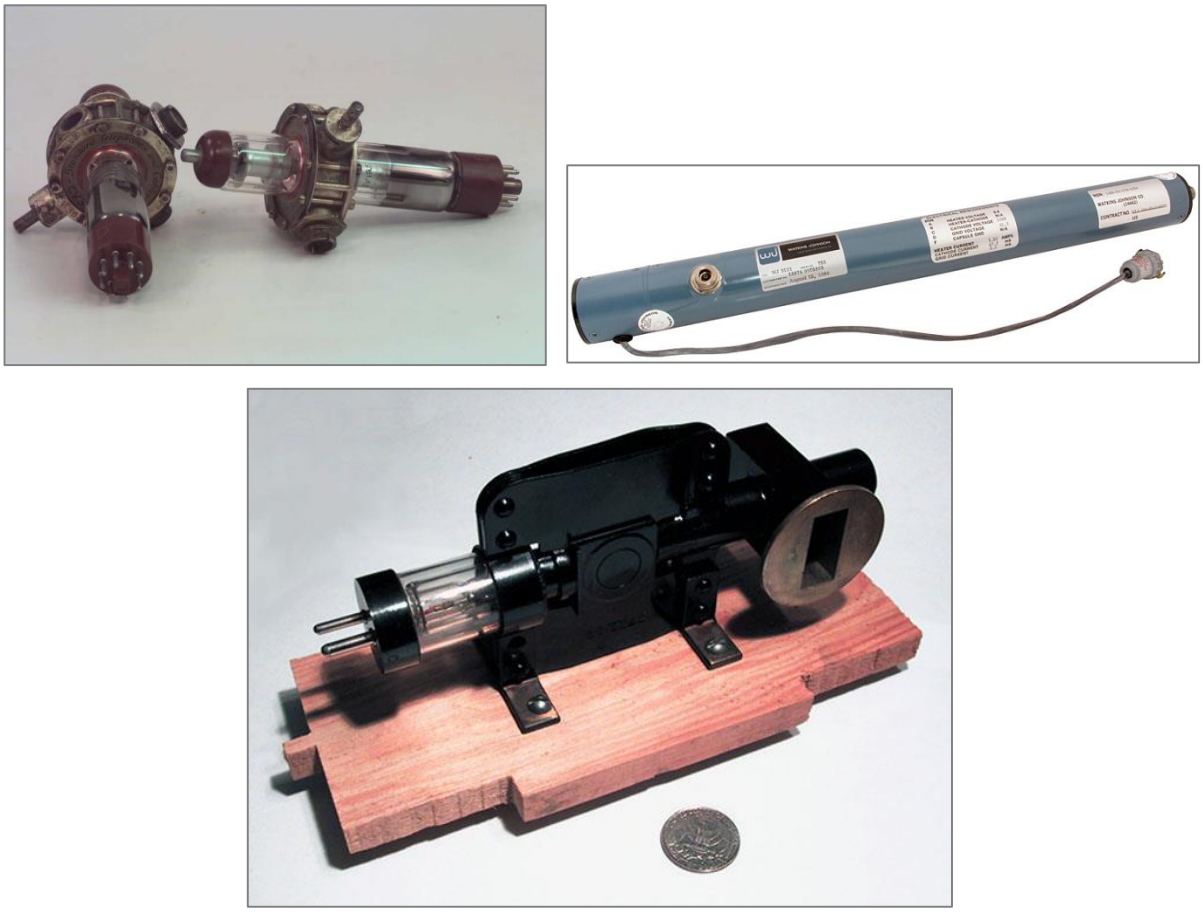


Figure 1.1 – Klynstron (top-left), TWT (top-right) and magnetron (bottom).

1.1. Transistor amplifier

Today, solid state amplification is dominated by use of three-terminal transistors. Using a small voltage applied at the input terminal of the device, one can control, in an efficient manner, a large current at the output terminal when the common terminal is grounded. This is the source for the name transistor, which is a unification of the words *transfer resistor*.

Solid state transistors may be grouped into two categories: bipolar and unipolar devices. The bipolar devices are comprised of silicon (Si) bipolar junction transistors (BJTs) and silicon germanium (SiGe) and gallium arsenide (GaAs) heterojunction bipolar transistors (HBTs). The unipolar devices include Si metal oxide semiconductor field effect transistors (MOSFETs), GaAs metal semiconductor field effect transistors (MESFETs), and pseudomorphic high electron mobility transistors (pHEMTs). The switchover to three-terminal devices was largely due to cost. Diodes are typically less expensive to manufacture than transistors but the

associated circuitry to achieve gain from a two-terminal device is much more expensive than that for a three-terminal device. For example, a transistor (without any matching network) connected between 50-ohm input and output terminals can provide 15–20 dB gain at radiofrequencies and 6–8 dB at 20 GHz. In addition, design of three-terminal amplifiers for stable operation and routine high-yield manufacturing is exceedingly simple. Signal amplification is a fundamental function in all RF and microwave systems.

When the strength of a weak signal is increased by a device using a direct current (DC) power supply, the device along with its matching and biasing circuitry is known as an amplifier. Here the DC power from the power supply is converted into RF power to enhance the incoming signal strength. If a device is a transistor, the signal is applied to the input terminal (gate/base) and the amplified signal appears at the output (drain/collector) and the common terminal (source/emitter) is usually grounded. The matching networks help in exciting the device and collecting the output signal more efficiently. Figure 1.2 shows a schematic representation of a single-stage transistor amplifier. Basic constituents are a transistor, input and output matching networks, bias circuitry, and input and output RF connections. The DC bias and RF connections may be made to connectors if housed in a fixture or to lead frame if assembled in a package depending on the amplifier fabrication scheme. [1]

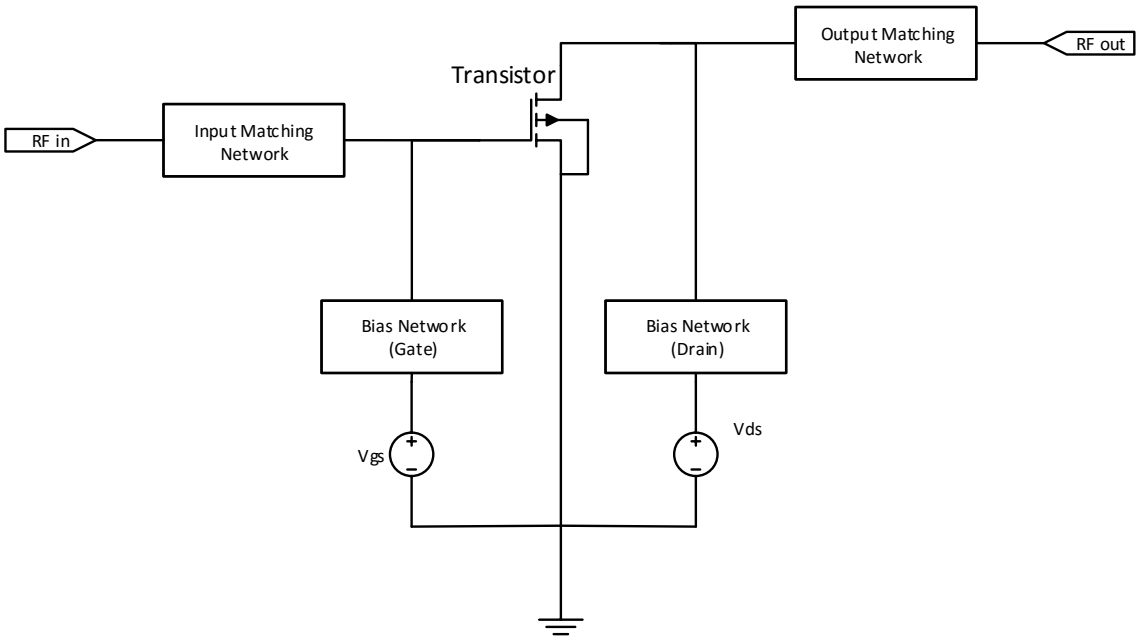


Figure 1.2 – Transistor amplifier schematic.

The design of amplifiers requires essentially device models/S-parameters, CAD tools, matching and biasing networks, and fabrication technology. RF and microwave amplifiers have the following characteristics:

- Band-limited RF response
- Less than 100% DC to RF conversion efficiency
- Nonlinearity that generates mixing products between multiple signals
- RF coupled and no DC response
- Power-dependent amplitude and phase difference between the output and input
- Temperature-dependent gain, higher gain at lower temperatures and vice versa

1.2. Early history of transistor amplifiers

The use of Si based bipolar transistors and GaAs based MESFET for amplifiers have been reported since the mid-1960s and early 1970s, respectively. Most of the initial work on Si based bipolar transistor amplifiers was below C-band frequencies, whereas GaAs based MESFET amplifiers were designed above L-band frequencies. Low-noise HEMTs were reported in the early 1980s. Internally matched narrowband MESFET power amplifiers working from S through X-band were available during the 1980s and Ku-band amplifiers were introduced in the early 1990s.

The GaAs monolithic microwave integrated circuit (MMIC) amplifier was reported in 1976 and since then there has been tremendous progress in both LNAs (Low Noise Amplifiers) and PAs (Power Amplifiers).

Some of the early development milestones in MMIC amplifiers are as follows [1]:

- X-band low-power GaAs MESFET amplifier in 1976
- X-band GaAs MESFET power amplifier in 1979
- K-band GaAs MESFET LNA in 1979
- Q-band GaAs MESFET power amplifier in 1986
- V-band GaAs HEMT LNA in 1988
- X-band GaAs HEMT power amplifier in 1989
- W-band HEMT LNA/power amplifier in 1992

1.3. Benefits of Transistor Amplifiers

Major benefits of transistor amplifiers versus tube amplifiers are:

- Smaller size
- Lighter weight
- Higher reliability
- High level of integration capability
- High-volume and high-yield production capability
- Greater design flexibility
- Lower supply voltages
- Reduced maintenance
- Unlimited application diversity
- Have much longer operating life (on the order of millions of hours)
- Require much lower warming time

Solid state amplifiers also do not require adjustment in the bias or the circuit, as required in tubes, over long periods of operation.

In comparison to solid state diode amplifiers, transistor amplifiers have greater flexibility in terms of designing matching networks, realizing high-stability circuits and cascading amplifier stages in series for high gain. The outstanding progress made in monolithic amplifiers is attributed to three-terminal transistors, especially on GaAs substrates. Monolithic amplifiers are fabricated on wafers in batches, and hundreds or thousands can be manufactured at the same time. Thus monolithic amplifiers have a great advantage in terms of the manufacturing cost per unit. It is worth mentioning that the weight of an individual or discrete chip resistor or a chip capacitor or an inductor is typically more than an entire monolithic amplifier chip. Many of today's high-volume applications using amplifiers are in hand-held gadgets. [1]

1.4. Applications of amplifiers

In general, a microwave system requires a group of amplifiers. Low-noise amplifiers are integral parts of receivers while transmitters are based on several stages of power amplifiers. RF/microwave power amplifiers are important circuit components used in every system

including cordless and cellular telephones, base station equipment, spaceborne, airborne, and ground based satellite communications, wireless local area networks, terrestrial broadcast and telecommunications, point-to-point radio (PPR), very small aperture terminal (VSAT) wideband satellite communications, air traffic systems, global positioning system (GPS), phased array radar (PAR), electronic warfare (EW), and smart weapons. Most of these systems require low-cost (high-volume) and more reliable solid state power amplifiers. Cordless and cellular telephones require low-bias operation (2–5 V), single power supply, and very high-efficiency (analog versions) or high-linearity (digital versions) amplifiers. Cellular telephones may also require dual, triple or quad-mode operation including multiple frequencies in both digital and analog versions. Power amplifiers for point-to-point radio and very small aperture terminal applications are operated typically at 8 V. The output power requirements are in the range of 0.2–4 W. On the other hand, for a phased-array antenna (PAA), the amplifiers are typically operated at 10 V and the output power requirements are in the range of 20–40 W per element.

The power level of amplifiers is dictated by the intended application. For example, for cellular base stations and EW, the power levels are in tens to hundreds of watts, while for satellite and radar systems, their levels may be a magnitude higher. For portable wireless handsets and wireless LANs, the required power levels are an order of magnitude lower, usually less than 1 watt. Based on the modulation schemes, the handset requirements can be grouped into two categories: constant envelope and nonconstant envelope. In the former scheme, there is no information contained in the amplitude of the transmitted signal. In this case, the amplifiers are operated in high-efficiency mode. Common applications are groupe special mobile (GSM) and digital European cordless telecommunication (DECT). The latter scheme enhances the spectral efficiency of the signal by incorporating the intended information in the amplitude of the transmitted signal. Most popular applications are code division multiple access (CDMA), wideband code division multiple access (WCDMA), and local area network (LAN). Usually, the amplifiers are operated in linear mode at the cost of amplifier efficiencies. For wireless base stations, high linearity is of paramount importance in power amplifiers. For example, personal communication service (PCS) (1.8–2.0 GHz) requires power levels in the range of 5–200 W.

Figure 1.3 shows an example of a typical microwave amplifier.

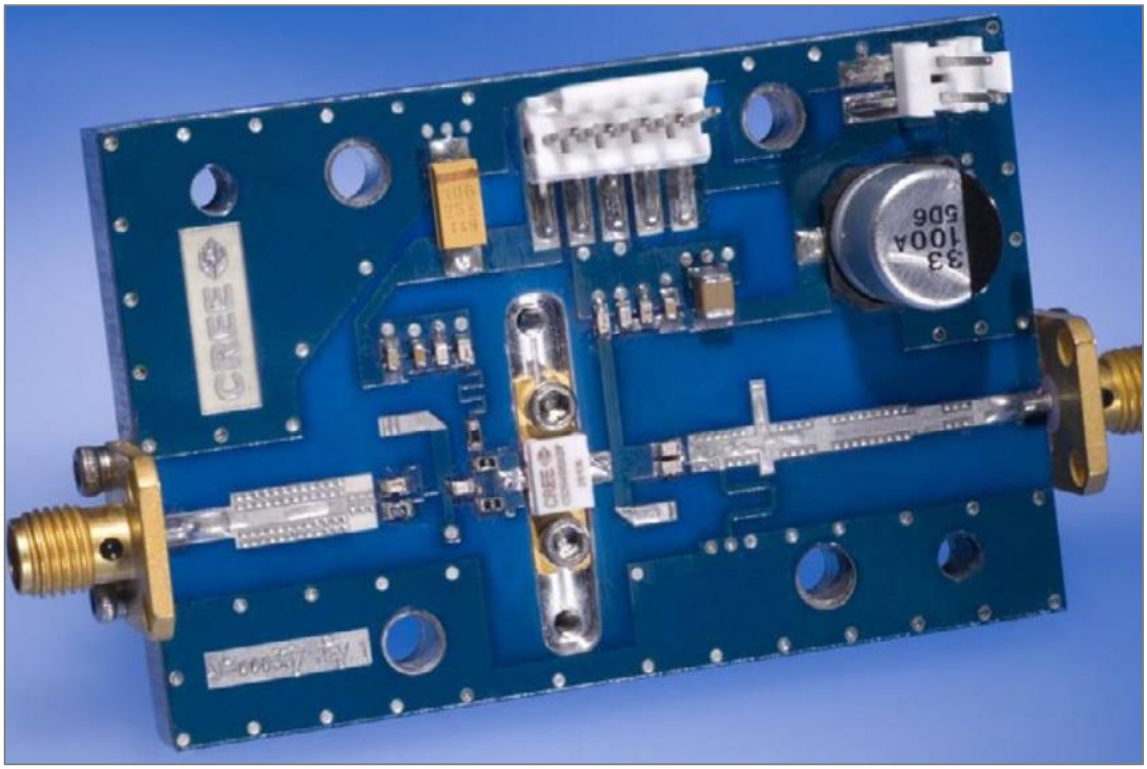


Figure 1.3 – Microwave amplifier.

Requirements for power amplifiers vary drastically from one application to another. Usually communication applications require linear operation, while for radar applications high PAE is of prime importance. Personal communication systems working in the 800-MHz to 2.5-GHz range use different digital modulation and access schemes. They require high-efficiency and linear power amplifiers for hand-held as well as for base station applications.

There are several emerging commercial and military applications that require broadband and high-power amplifiers. These include broadband wireless access systems, communication and electronic warfare. [1]

1.5. Current trends

Microwave and millimeter-wave transistor amplifiers have advanced dramatically. Si based CMOS technology circuits operating up to 70 GHz and GaAs/InP based technology operating up to 280 GHz have been realized. The Si LDMOS transistor is a primary power device for base station transmitters up to S-band frequencies. Devices such as pHEMTs and HBTs made on

InP, SiC, and GaN substrate materials have performed beyond 100 GHz. SiC based GaN pHEMT technology has also advanced rapidly and is finding special application where high-power, high-efficiency, low-noise, broadband, and millimeter-wave operation are required. Extremely high-frequency circuits enable a wide range of new applications to be developed in communications, security, medicine, sensing, and imaging. Power amplifiers are vital components in evolving broadband wireless applications including TV broadcasting, voice over Internet protocol (VoIP), video on demand (VOD), online gaming, mobile streaming, and mobile video telephony.

Recently, SiC based transistors operating at 30–50 V have advanced rapidly. SiC MESFETs have increasing applications in high-power wideband at low microwave frequencies and GaN HEMTs on SiC are finding numerous applications where high-power and high-frequency operation is required. Much higher power densities for such devices meet the current need in reducing the cost of solid state power amplifiers. Another emerging technology is GaN HEMT on SiC. This technology has the potential of meeting cost targets for numerous applications, including base station and radar transmitters. These devices are capable of generating hundreds of watts at C/X-band, tens of watts in the millimeter-wave region, and 1–2 W at 100 GHz. Since this technology has an order of magnitude higher breakdown voltage and power density potentials along with an outstanding thermal dissipation substrate, it has all the ingredients required for high-power amplifiers.

The RF and microwave industry is still growing and there is strong evidence that it is being fully supported to meet current trends. New high-volume applications demand low-cost solutions for transmitters based on transistor amplifiers. Current trends are in the areas of improved device models and integrated CAD tools. In a new competitive business environment, it is essential to have accurate device models and suitable circuit design tools to develop state-of-the-art circuits to meet system requirements, including cost and production schedule. It becomes essentially important for amplifier design engineers to develop amplifier products for specific applications on time. For emerging wideband applications that require very high-power (50–200 W) amplifiers with PAE as high as 50%, new circuit topologies to meet these challenging performance goals will be required.

There are continuous trends for improving the performance of LNAs and PAs in order to make them cheaper for high-volume applications. Thus advancements in RFIC and MMIC technologies and packaging will continue with the pace set in the past decade. For high-

volume applications, a package (plastic or ceramic) has become an integral part of RFICs and MMICs for power amplifiers. Achieving the smallest size and cheapest product cost requires inexpensive and high-performance leadless surface-mount and ball-grid array packages. Plastic packaging is a preferred technique for small-signal amplifiers and more and more power devices are being housed in plastic packages. Low thermal resistance is another important requirement for such packages. [1]

1.6. Objectives

The main objectives and purposes of this final project are:

- Learning the theoretical background about the design of a Power Amplifier.
- Making the design and simulating it through AWR (Microwave Office).
- Manufacturing the final prototype and test it in the lab.

The specifications of our Power Amplifier will be:

- Working at 2.45GHz in a narrowband configuration (100MHz).
- At least 14dB gain at that frequency.

2. Theoretical Background

Before that we start explaining the design process of the proposed Power Amplifier, it is important to make a brief summary of the main theoretical concepts that we will be working with, such as linear network analysis, transistor basics and amplifier characteristics, definitions and classes.

2.1. Linear Network Analysis

Linear network analysis methods are the fundamental topics in RF and microwave circuit design. Basically it consists of mathematical relationships between the voltages and currents at various ports of a component, which may be a transistor or a passive element (bond wire, lumped element, microstrip section, coupler, etc.) or an amplifier. Linear characterization is performed at low power levels, hence the origin of "small-signal" network parameters. [2]
Microwave network theory was originally developed in the service of radar system and component development at the MIT Radiation Lab in the 1940s. [3]

2.1.1. The Concept of Impedance

The term impedance was first used by Oliver Heaviside in the 19th century to describe the complex ratio V/I in AC circuits consisting of resistors, inductors and capacitors. This concept was then applied to transmission lines, in terms of lumped-element equivalent circuits and the distributed series impedance and shunt admittance of the line.
We summarize the various types of impedance and their notation:

- $\eta = \sqrt{\mu/\varepsilon}$ = intrinsic impedance of the medium. This impedance is dependent only on the material parameters of the medium, and is equal to the wave impedance for plane waves.

- $Z_\omega = E_t/H_t = 1/Y_\omega$ = wave impedance. This impedance is a characteristic of the particular type of wave (TEM, TM and TE).
- $Z_0 = 1/Y_0 = V^+/I^+$ = characteristic impedance. Characteristic impedance is the ratio of voltage to current for a traveling wave on a transmission line. Because voltage and current are uniquely defined for TEM waves, the characteristic impedance of a TEM wave is unique. [3]

2.1.2. S-Parameters

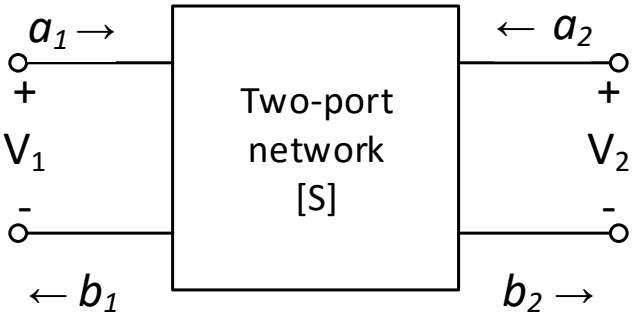


Figure 2.1 – S-parameter representation of a two-port network.

The scattering matrix formulation is a general method for representing microwave networks and the device under test is usually terminated in 50Ω. A scattering matrix represents the relationship between variables a_n (proportional to the incoming wave at the *n*th port) and variables b_n (proportional to the outgoing wave at the *n*th port) defined in the following manner.

$$a_n = \frac{v_n^+}{\sqrt{Z_{0n}}}$$

$$b_n = \frac{v_n^-}{\sqrt{Z_{0n}}}$$

where v_n^+ and v_n^- represent voltages corresponding to the incoming and the outgoing waves in the transmission line (or the waveguide) connected to the *n*th port and Z_{0n} is the characteristic impedance of the line (or waveguide). Knowledge of v_n^+ and v_n^- is not required to evaluate coefficients of the scattering matrix. Relationships between b_n and a_n for the two-port network shown in Figure 2.1 may be written

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

Here

$$S_{11} = b_1/a_1 \qquad S_{21} = b_2/a_1 \qquad a_2 = 0$$

$$S_{12} = b_1/a_2 \qquad S_{22} = b_2/a_2 \qquad a_1 = 0$$

In general, for an *n*-port network, we have

$$[b] = [S][a]$$

At the *n*th port, the total voltage V_n and current I_n are given by

$$V_n = V_n^+ + V_n^- = \sqrt{Z_{0n}}(a_n + b_n)$$

$$I_n = I_n^+ - I_n^- = \frac{V_n^+ - V_n^-}{Z_{0n}} = \frac{1}{\sqrt{Z_{0m}}}(a_n - b_n)$$

Because the current flows in the axial direction, the total (net) current is given by the difference of the currents flowing in the positive and negative directions.

The net average power flow into the network is given by the usual low-frequency relation which is,

$$P_n = \frac{1}{2}Re(V_n \times I_n^*)$$

where V_n and I_n denote the total peak voltage and current, respectively. Using the two equations above, we have

$$P_n = \frac{1}{2}(|a_n|^2 - |b_n|^2) + imaginary\ term = \frac{1}{2}(|a_n|^2 - |b_n|^2)$$

This equation shows that the power delivered to a port is equal to the power in the incident wave minus the power in the reflected wave at that port. This is an important term that defines the delivered, incident and reflected powers. The terms S_{11}, S_{22} and S_{12}, S_{21} are defined as the reflection and transmission coefficients, respectively.

Attenuation in a circuit, α, expressed in *dBs*, is given by

$$\alpha = -20\log\left|\frac{b_2}{a_1}\right|\ dB = -20\log|S_{21}|\ dB$$

For a passive circuit, $b_2 < a_1$ and value of α is a positive quantity. However, for an amplifier with gain, $b_2 > a_1$ and α becomes a negative quantity. In other words, the negative attenuation is nothing but gain. The transmission phase is given by

$$\phi = \angle S_{21}$$

2.2. Transistors

The realization of high power devices requires an appropriate selection of semiconductor materials and a suitable placing of the emitter/gate fingers to properly balance the heat transfer across the device itself and to avoid peaking junction temperature, thus preventing device failures. Large-scale RF and microwave power device production, especially for commercial purposes, is actually based on silicon (Si), gallium arsenide (GaAs) and related compounds, while great research interest is devoted in the development of high power density devices using wide-bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN). The main substrate properties affecting the device performance, reported in Table 2.1, are represented by the material energy bandgap, the breakdown field, the thermal conductivity, electrons and holes transport properties, the saturated electron velocity and the conductivity which affects the loss behaviour at RF frequencies. [4]

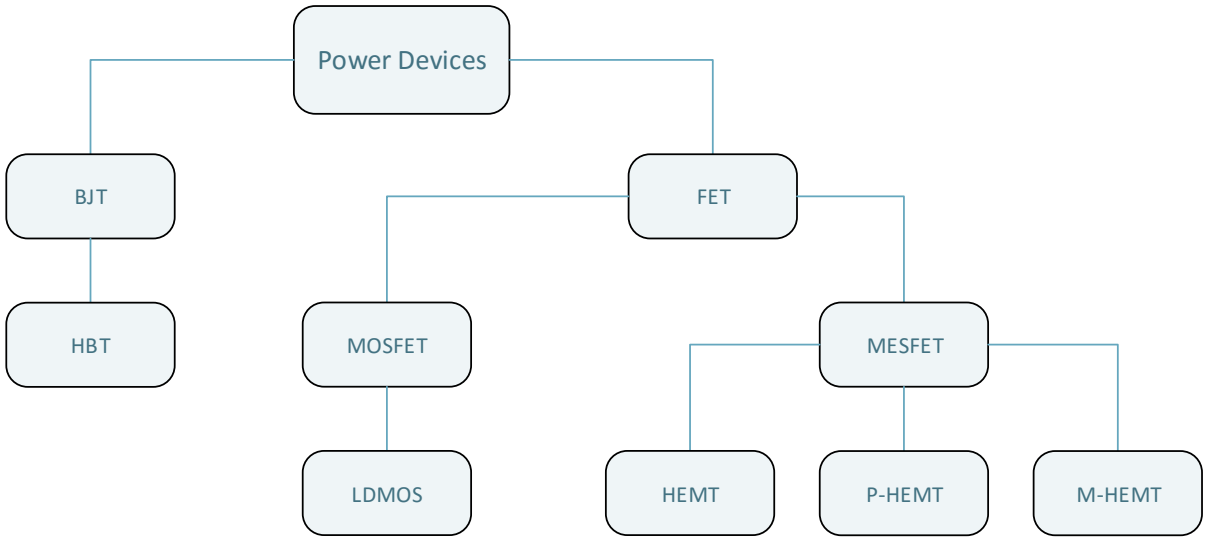


Figure 2.2 – Power transistors classification.

Property	Si	Ge	GaAs	GaN	4H-SiC	InP
Electron mobility ($cm^2 V^{-1} s^{-1}$)	1500	3900	8500	1000	900	5400
Hole mobility ($cm^2 V^{-1} s^{-1}$)	450	1900	400	350	120	200
Bandgap (eV)	1.12	0.66	1.42	3.2	3.23	1.35
Avalanche field (10^5 V/cm)	3.8	2.3	4.2	50	35	5.0
Saturated drift velocity (10^7 cm/s)	0.7	0.6	2.0	1.8	0.8	2.0
Saturation field (10^3 V/cm)	8		3	15	25	25
Thermal conductivity at 25°C (W/cm °C)	1.4	0.6	0.45	1.7	4.9	0.68
Dielectric constant	11.9		12.9	14	10	8
Substrate resistance (Ω cm)			>1000	>1000	1-20	>1000
Transistors			MESFET	MESFET	MESFET	MESFET
			HEMT	HEMT	HEMT	HEMT
			HBT			HBT
			P-HEMT			P-HEMT

Table 2.1 – Semiconductor properties.

2.2.1. BJT

The Bipolar Junction Transistor (BJT) is one of the most essential semiconductor devices, mainly fabricated over silicon in a vertical structure, as schematically depicted in Figure 2.2. The structure is formed by diffusing a p-type region between a heavily doped n+ region and an n-type substrate. The heavily doped n+ region is called the emitter (E), the centre of the p region is called the base (B) and the lightly doped n region is the collector (C).

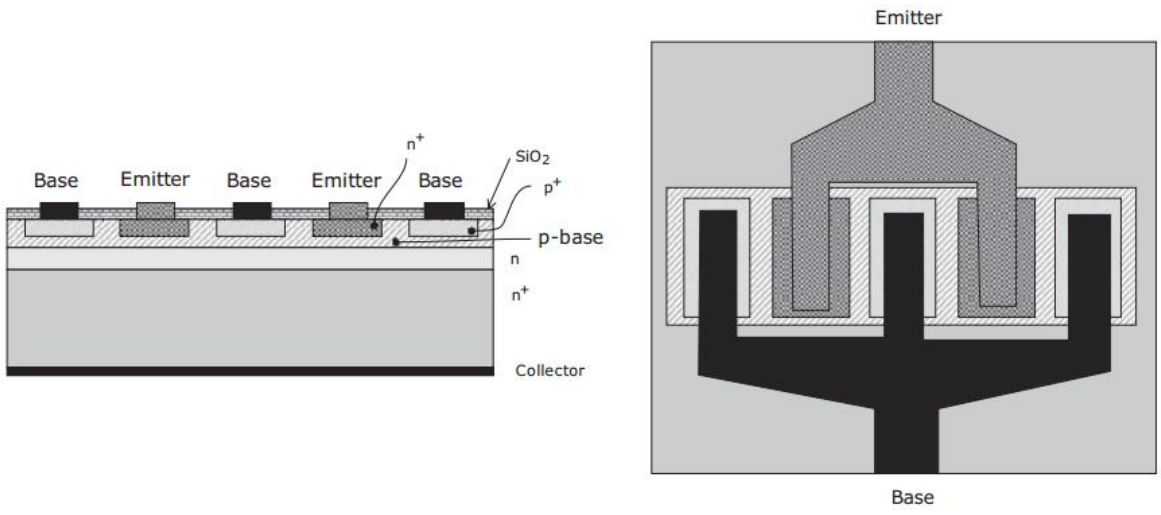


Figure 2.3 – Schematic structure of a BJT (left) and its top view (right).

Since RF power BJTs are usually realized by composing multiple small BJTs, emitter ballasting is generally employed to force even division of the current within a given package. The Si BJT typically operates from 28 V of bias supply and is adopted up to 5 GHz especially in high power (1 kW) pulsed applications (e.g. radar).

2.2.2. HBT

The Heterojunction Bipolar Transistors (HBTs) represent the natural improvement of conventional BJTs, as a result of the exploitation of heterostructure junctions. Such heterostructures are typically based on compound semiconductor materials like AlGaAs/GaAs, SiGe and InP, as schematically depicted in Figure 2.4 for a GaAs HBT. In order to minimize the base resistance, the emitter is realized as narrow as possible, while the barrier is created directly by the heterojunction (AlGaAs/GaAs in Fig. 2.4) rather than by the doping profile.

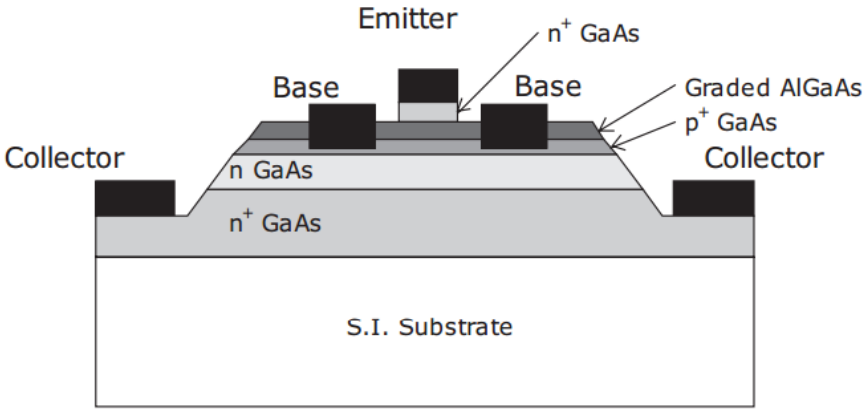


Figure 2.4 – Schematic structure of a HBT.

Unlike conventional BJTs, in HBTs the bandgap difference between the emitter and the base materials results in higher common emitter gain. Base sheet resistance is lower than in ordinary BJTs, and the resulting operating frequency is accordingly higher. The current flow path is vertical, so that surface imperfections affect marginally the device performance. Furthermore, the use of a semiinsulating substrate and the higher electron mobility result in reduced parasitics. GaAs HBT are widely used in MMICs and they operate in PAs at frequencies as high as 20 GHz, while with InP HBT operation up to 50 or 60 GHz has been demonstrated. The main advantage of HBT with respect to FET devices, where PAs are

concerned, is represented by the higher linearity of the former, which seems to be related to the base-emitter junction capacitance and its beneficial effect in reducing the intermodulation products.

2.2.3. FET

The Field-Effect Transistor (FET) family includes a variety of structures, among which are MESFETs, MOSFETs, HEMTS, LDMOS, etc. They typically consist of a conductive channel accessed by two ohmic contacts, acting as a source (S) and as a drain (D) terminals respectively. The third terminal, the gate (G), forms a rectifying junction with the channel or a MOS structure. A simplified structure of a metal-semiconductor n-type FET is depicted in Figure 2.5.

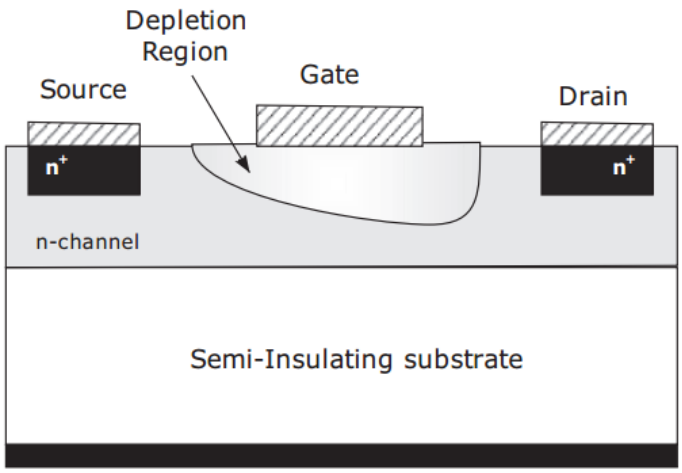


Figure 2.5 – Schematic structure of a FET.

Applying a positive voltage Vds between drain and source terminals, electrons flow from the source to the drain, thus creating a current Id in the channel beneath the gate. Thus the source acts as origin of carriers while the drain becomes the sink, and the current flux can be controlled by the rectifying junction formed by the gate terminal and the channel. The gate electrode is deposited to form a Schottky diode in a JFET or MESFET and a metal-oxide (insulator) system in a MOSFET. FET devices ideally do not draw current through the gate terminal, unlike the BJTs which conversely require a significant base current, thus simplifying the biasing arrangement. Moreover, FET devices exhibit a negative temperature coefficient, resulting in a decreasing drain current as the temperature increases. This prevents thermal

runaway and allows multiple FETs to be connected in parallel without ballasting. The device performance is critically determined, over the material properties, by geometrical parameters like the length, width, depth of the channel and depletion layer width. In general, the length of the channel under the gate determines the transit time, i.e. the time required by electrons to travel through the channel itself. This transit time determines the cut-off frequency f_T and the maximum frequency f_{Max}. At the same time, however, channel length and inter-electrode spacing (eventually with field-plate arrangements) influence the maximum operating voltage of the transistor, being also determined by the breakdown field of the material.

2.2.4. MOSFET

The metal–oxide–semiconductor field-effect transistor (MOSFET) is realized by growing an insulated gate above the channel. The latter, according to the doping profile selected, could be already formed (depletion device) or must be created (enhancement device) by suitable gate voltages. As an example, a typical enhancement structure is depicted in Figure 2.6. The standard material used as substrate to grow MOSFET is silicon, whose technology process is sufficiently mature, allowing also the realization of stable oxide used as the dielectric to realize the oxide insulator beneath the gate.

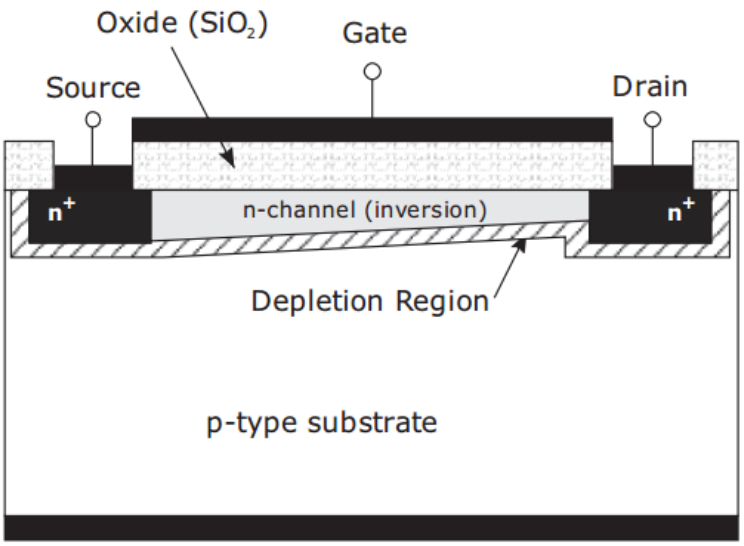


Figure 2.6 – Schematic structure of a MOSFET.

The main issues of MOSFET device are intrinsically related to the oxide insulator, and in particular to the presence of unavoidable traps, which imply a shift in the voltage threshold,

and in the unavoidable parasitics connected with the MOS structure (capacitive in nature) reducing the maximum operating frequency.

2.2.5. LDMOS

The Laterally Diffused MOSFET (LDMOS) is an enhanced MOSFET structure especially suited for high power applications. Its basic structure is schematically indicated in Figure 2.7. In a LDMOS, as in a MOSFET, there are two n+ regions for the source and the drain respectively. The most noticeable difference as compared to a MOSFET is in the low doped and quite long n-drift region realized in the LDMOS, which enhances the depletion region.

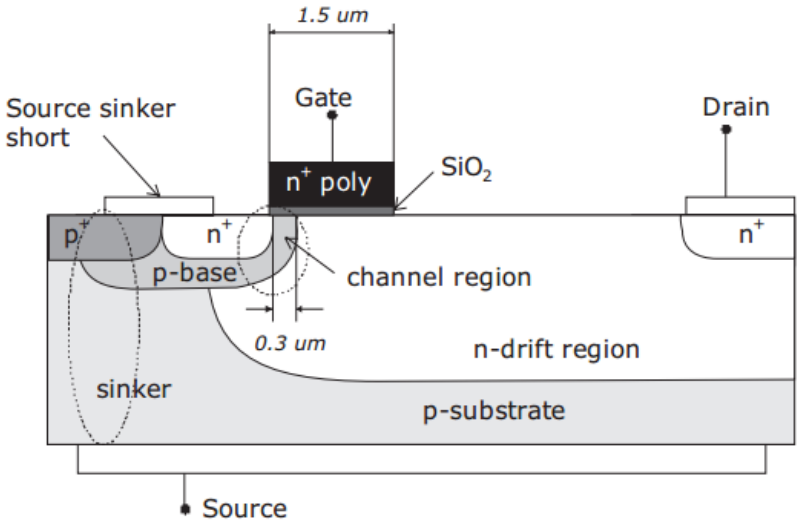


Figure 2.7 – Schematic structure of a LDMOS.

Separating the channel region from the drift region allows designing a short channel device for high frequency operation. At the same time, the increased distance between the drain and source allows higher voltage operation without reaching the breakdown field of the device, thus resulting in higher power capabilities.

The LDMOS drain current follows the same behaviour as in a MOSFET. Applying a positive voltage to the gate, a conductive channel in the p-base region is created. The channel being very short, the device transistor always operates in the saturated velocity region, thus further improving device linearity. Electrons with saturation velocity at the channel flow in the doped n-drift region reaching the drain.

The LDMOS is especially useful at UHF and lower microwave frequencies, since the direct grounding of its source eliminates bond-wire inductance that produces negative feedback and

reduces gain at high frequencies. Currently, packaged LDMOS devices typically operating from 28V supplies and they are available with output powers over 120W at 2GHz.

2.2.6. MESFET

MEtal-Semiconductor Field-Effect Transistors (MESFETs) have a structure and DC characteristics quite similar to MOSFETs, but differing from the latter since in a MESFET the gate electrode uses a metal semiconductor contact instead of a MOS arrangement. A typical structure of a MESFET is depicted in Figure 2.8. There are two n^+ regions, one for source and the other for the drain, while an n-type channel is present between drain and source terminals and connected to the gate by a Schottky junction. This implies that normally a MESFET device is active for $V_{gs} = 0V$, thus operating in a depletion-mode requiring negative gate bias, although also enhancement-mode devices that operate with a positive bias have been developed.

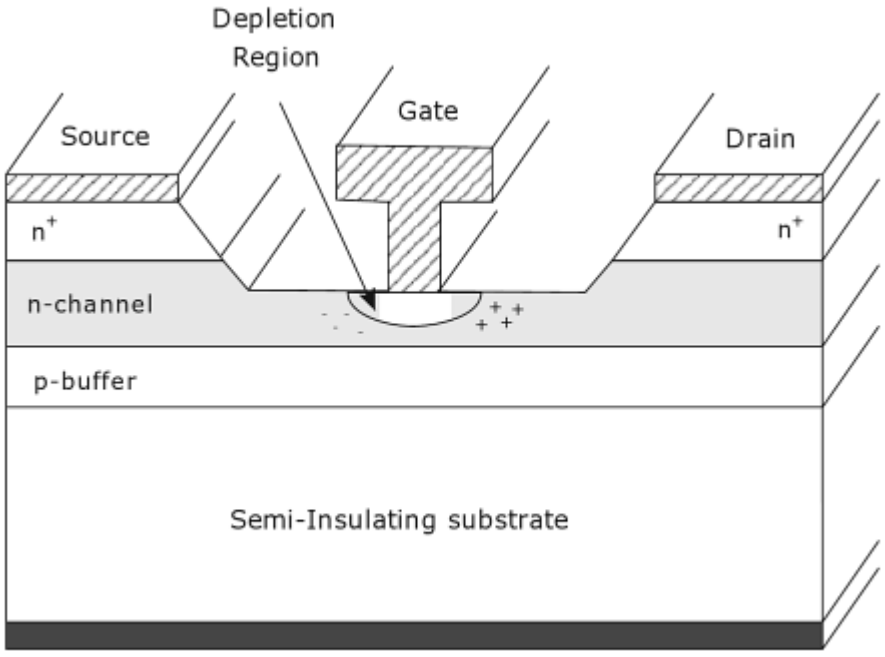


Figure 2.8 – MESFET device cross-section.

The source is usually grounded (common source configuration) and the drain is positively biased. Applying a negative gate source voltage reverse biases the metal semiconductor junction, thus forming a depletion layer in the channel. An increase in the negative gate

voltage causes an increase in the depletion region, and a decrease in the conductive channel width: control of the current flow between the drain and source is thus achieved.

MESFET devices are usually fabricated from III-V compound semiconductors; the predominant is GaAs, or more recently from wide-bandgap semiconductors like SiC.

Since III-V compound semiconductors do not allow stable oxide to make the gate dielectric, a Schottky metal semiconductor contact is instead used for the gate. The adoption of Schottky gate results in two main advantages: to avoid traps in the gate insulator, affecting the threshold voltage shift in the MOSFETs, and the absence of the capacitor formed from the channel (conductor), dielectric (insulator) and metal gate terminal (conductor) in normal MOSFET structure, thus allowing higher frequency operation.

Moreover, MESFET based on a GaAs (or SiC) substrate and a Schottky gate junction, exhibit a higher mobility than Si MOSFET devices, thus making them capable of operating with acceptable gain and efficiently at higher frequencies.

The SiC devices, due to their wide energy bandgap and the higher thermal conductivity, provide higher power desities, up to 10W/mm, with respect to the typical values 0.3-0.5W/mm of GaAs based MESFETs.

SiC MESFETs typically operate from 50 to 60 V of DC voltage supply, with some demonstrations extending to hundreds of volts, while GaAs MESFETs are typically operated from supply voltages (drain biases) of 5-10 V.

The higher operating voltage and associated higher load impedance of SiC greatly simplify output networks and power combining. However, the lower carrier mobility in SiC, together with a lower transconductance value, reduces the frequency range of such devices up to 10-12 GHz maximum, against the 25-30 GHz of GaAs MESFETs.

GaAs MESFETs, however, are widely used for the production of microwave power, with capabilities of over hundreds of watts in the L-band or tens of watts up to K-band for packaged devices.

2.2.7. HEMT

In High Electron Mobility Transistors (HEMTs) devices the conducting layers are epitaxially grown over a semi-insulating substrate realizing a heterostructure alongside the electron flow, as schematically depicted in Figure 2.9 for an AlGaAs/GaAs HEMT.

The typical materials used for HEMTs are AlGaAs, Al/InGaAs and AlGaN.

The heterojunction formed results in a sharp dip in the conduction band edge.
Such a discontinuity in the bandgaps of AlGaAs and GaAs causes a thin layer of electrons, i.e. a high carrier concentration in a confined region below the gate at the interface of the AlGaAs and GaAs layers, forming the so-called two-dimensional electron gas (2-DEG). [4]

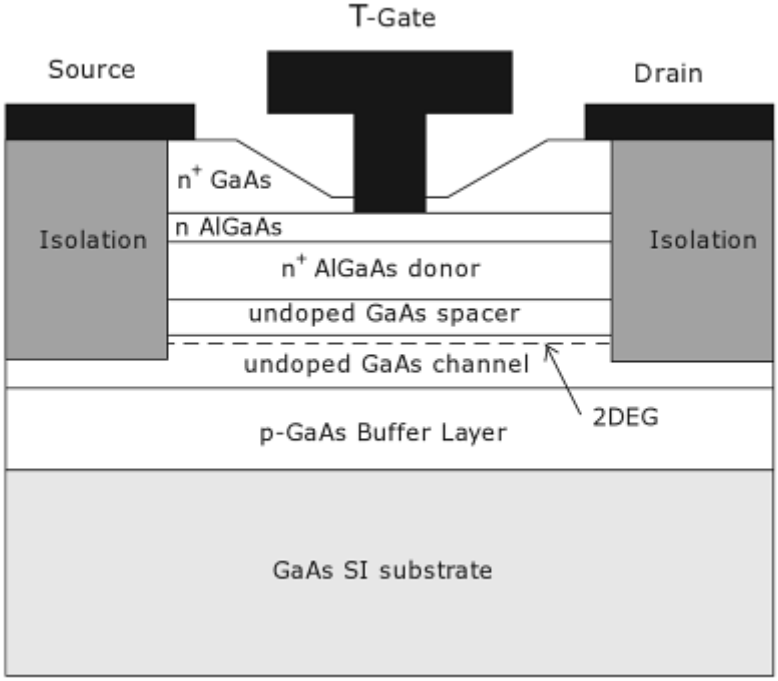


Figure 2.9 – Structure of an AlGaAs/GaAs HEMT.

It is expected that the high electron mobility transistor (HEMT) using gallium nitride (GaN) as its wide band gap semiconductor will be applied in diverse, green ICT systems because of its high efficiency. The GaN HEMT utilizes high-density two-dimensional electron gas (2DEG) accumulated in the boundary layer between GaN and AlGaN through their piezoelectric effect and natural polarization effect. This makes it possible to realize a low on-state resistance (R_{on}). Combined with a high breakdown voltage, the GaN HEMT indicates a superb performance as a power device. After the development of GaN HEMT technology started for power amplifiers of mobile base stations, it was expanded to a radar sensor application. Further expansion of its application is expected in the field of power conversion, in equipment such as server power systems. While the development of GaN HEMT technology has been promoted, focusing on “high output power” conventionally, further advantages such as high efficiency and low energy consumption have been attracting much attention in recent years. [5]

2.3. Amplifier Characteristics and Definitions

Although many characteristics must be considered when designing an amplifier, the most important of these are frequency range or bandwidth, power gain, noise figure, power output, 1-dB gain compression point, input and output VSWR, power added efficiency (PAE), intermodulation distortion, dynamic range and stability.

2.3.1. Bandwidth

Generally, the bandwidth of an amplifier is defined as the frequency range over which the circuit meets the specified minimum/maximum or typical aforementioned requirements.

Consider input impedance and output admittance of a transistor as shown in Figure 2.10. In this case input and output 3-dB normalized bandwidths are given by

$$\frac{\Delta f_{in}}{f_0} = \frac{1}{Q_{in}} = 2\pi f_0 R_{in} C_{in} \qquad \frac{\Delta f_{out}}{f_0} = \frac{1}{Q_{out}} = \frac{1}{2\pi f_0 R_o C_o}$$

where f_0 is the centre frequency. This shows that the bandwidth of the transistor is limited by its input impedance, which can be increased by adding more resistance in series with the device. However, it reduces the transistor gain but improves its stability. [6]

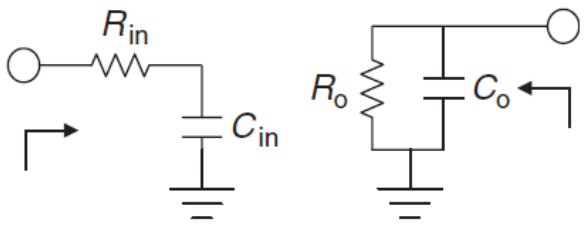


Figure 2.10 – One-port equivalent circuit of a transistor: input (left) and output (right).

2.3.2. Power Gain

The power gain of a two-port network, amplifier in this case, is defined as the ratio of the output power to input power. For a two-port network (shown in Figure 2.11), the power gain can be defined in several ways. The three commonly used definitions are *transducer power*

gain (G_T) or simply *power gain*, *maximum available power gain* (G_A), and *available power gain* (G_P). Their definitions are given below:

$$G_T = \frac{power\ delivered\ to\ the\ load}{power\ available\ from\ the\ source} = \frac{P_L}{P_{avs}}$$

$$G_A = \frac{power\ available\ from\ the\ network}{power\ available\ from\ the\ source} = \frac{P_N}{P_{avs}}$$

$$G_P = \frac{power\ delivered\ to\ the\ load}{power\ delivered\ to\ the\ network} = \frac{P_L}{P_{in}}$$

Here $G_A \geq G_T$ *and* $G_P \geq G_T$.

Developing the power expressions, we have

$$P_L = \frac{|V_S|^2}{8Z_0}\frac{|S_{21}|^2(1-|\Gamma_L|^2)|1-\Gamma_S|^2}{|1-S_{22}\Gamma_L|^2|1-\Gamma_S\Gamma_{in}|^2}$$

$$P_{avs} = \frac{|V_S|^2}{8Z_0}\frac{|1-\Gamma_S|^2}{1-|\Gamma_S|^2}$$

$$P_N = \frac{|V_S|^2}{8Z_0}\frac{|S_{21}|^2(1-|\Gamma_{out}|^2)|1-\Gamma_S|^2}{|1-S_{22}\Gamma_{out}^*|^2|1-\Gamma_S\Gamma_{in}|^2}$$

$$P_{in} = \frac{|V_S|^2}{8Z_0}\frac{|1-\Gamma_S|^2(1-|\Gamma_{in}|^2)}{|1-\Gamma_S\Gamma_{in}|^2}$$

And substituting these expressions in the gain equations we have

$$G_T = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)-S_{12}S_{21}\Gamma_S\Gamma_L|^2}$$

If our amplifier can be considered as unilateral ($|S_{12}| = 0$), our *transducer power gain* becomes in *unilateral transducer power gain* and it is expressed by

$$G_{TU} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L)|^2} = G_S|S_{21}|^2G_L$$

where

$$G_S = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2} \qquad G_L = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}$$

The terms G_S and G_L represent the gain or loss of the input and output matching circuits, respectively.

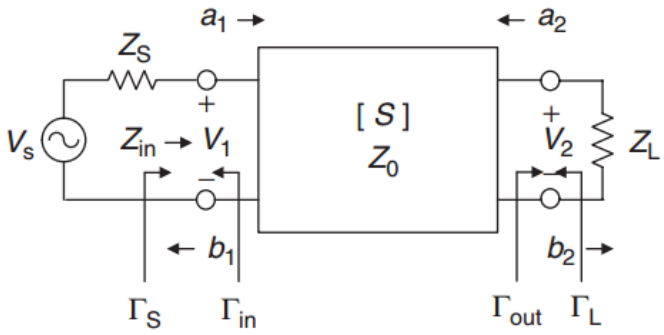


Figure 2.11 – Two-port network for a transistor.

The maximum unilateral power gain is attained when $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$, that is, when the network is matched conjugately at the input and output ports. The maximum unilateral power gain, also called the maximum available gain from a unilateral device, is given by

$$G_A = G_{TUm} = \frac{|S_{21}|^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)}$$

Thus the maximum available gain is the product of the transistor transducer power gain $|S_{21}|^2$ between source and load impedances (usually 50 Ω) and the increase in gain due to matching the input port $(1 - |S_{11}|^2)^{-1}$ and matching the output port $(1 - |S_{22}|^2)^{-1}$. In other words, a single-stage amplifier design consists of (a) designing an input matching network to give $\Gamma_S \approx 0$ and (b) designing an output matching network that simultaneously gives $\Gamma_L \approx 0$. The above conditions fail if the solid state devices are unstable. [6]

The most commonly used gain definition in amplifiers is *transducer power gain*, G_T; other gain definitions are normally used to characterize a transistor. The power gain G is usually expressed in decibels, that is,

$$G(dB) = 10 \log G \ (power\ ratio)$$

2.3.3. Noise Figure

The noise figure of any linear two-port network can be defined as

$$F = \frac{signal\ to\ noise\ ratio\ @\ input}{signal\ to\ noise\ ratio\ @\ output} = \frac{available\ noise\ power\ @\ output}{gain \times available\ noise\ power\ @\ input} = \frac{N_0}{GkTB}$$

where N_0 is the available noise power at output, G is the available gain of the network over the bandwidth B, and T is the operating temperature in kelvin units.

If N_a is the noise power added by the amplifier, then

$$F = \frac{GkTB + N_a}{GkTB} = 1 + \frac{N_a}{GkTB}$$

An amplifier that contributes no noise to the circuit has $F = 1$. [6]

2.3.4. Output Power and 1-dB Compression Point (P_{1dB})

Power delivered to the load (P_L) is known as the output power, P_o or P_{out}, which is a strong function of the input power. When the gain is reduced at higher input power levels (as the device gets saturated or compressed) by 1 dB, the output power is defined as P_{1dB}, which is normally used to characterize nonlinearity in amplifiers. At 3–5dB gain compression, the output power is saturated and known as P_{sat}. Figure 2.12 shows a typical variation of gain with output power of an amplifier. Output power points at 1 and 3dB gain compression are also shown. [6]

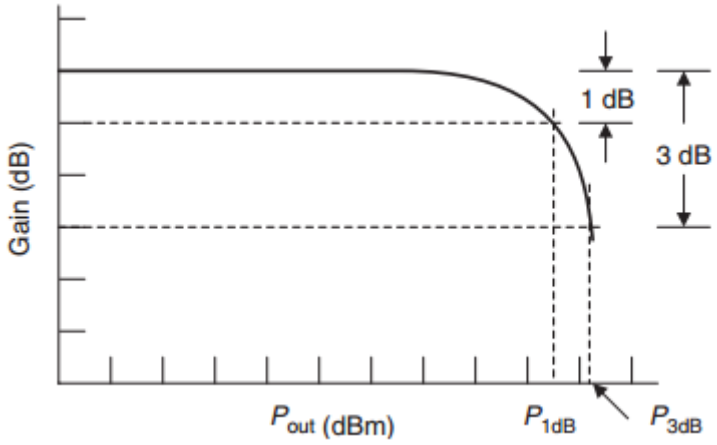


Figure 2.12 – Gain versus output power of an amplifier.

2.3.5. Input and Output VSWR

The input and output VSWR values are commonly used to characterize an amplifier's circuit match to source and load impedance (usually 50Ω). Mismatch between 50Ω and the

amplifier's input, and 50Ω and the amplifier's output are measured as input and output reflection coefficients. When the voltage reflection coefficient $|\rho| = 0.333$ (VSWR = 2), the power reflection coefficient $|\rho|^2 = 0.11$ means 11% power is reflected. In most applications, a VSWR value of 2:1 is acceptable.

The reflection coefficients are measured at small-signal conditions as well as at large-signal conditions. The measurement of output reflection coefficient under high-power conditions is not trivial. The output of power amplifier circuits is designed to provide optimum power performance, not necessarily good VSWR.

Normally, good input and output VSWR values in power amplifiers are achieved by using a balanced configuration or by using a traveling-wave combining technique. [6]

Three related parameters—the return loss (R_L), *VSWR*, and reflection coefficient (ρ)—are commonly used to characterize amplifier reflections. The return loss is the ratio of the input power (P_{in}) to reflected power (P_R):

$$R_L = -10\log\frac{P_R}{P_{in}} = -10\log\left(\frac{VSWR-1}{VSWR+1}\right)^2 = -10\log(|\rho|^2)$$

2.3.6. Power Added Efficiency (PAE)

Power-Added Efficiency (PAE) is a measure of the power conversion efficiency of power amplifiers. Ideally, all supplied power to the amplifier is converted into output power. However, that is not the case in reality. As such, PAE is an important performance parameter for power amplifiers, and is commonly defined as

$$PAE(\%) = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \cdot 100$$

Between linear and saturation regions of operation, there is a point where the power amplifier is most efficient. Up to a certain point, output power is improved while input power is increased. Beyond that point, increased input power will only generate more heat for the device. The objective of PAE measurement is to find this optimal point, the point where the power amplifier is most efficient in transferring input power into output power. [7]

2.3.7. Intermodulation Distortion

An amplifier is called linear when the output power increases linearly with the input power or power gain is constant with input power. As input power increases, the device current

starts reaching its maximum value depending on its size. Near the limiting region the amplifier transfer function becomes nonlinear and a point is reached where the output power does not increase with the input power. One of the measures of nonlinearity of amplifiers is intermodulation distortion. When more than one carrier frequency is present in a nonlinear amplifier, due to mixing, multiple sidebands will be generated as intermodulation products. Intermodulation distortion can also arise from the combined effects of amplitude modulation (AM) introduced by a previous stage and AM to PM (phase modulation) conversion. Intermodulation distortion can be introduced by any nonlinear devices or amplifier stage.

There are a number of different ways to measure the nonlinearity or distortion behaviour of an amplifier. The simplest method is the measurement of the 1-dB gain compression power level, P_{1dB}. This provides a crude estimation of distortion but is not adequate. For a single-carrier system, third-order intermodulation distortion measurement known as IP3 or TOI is performed, whereas for a multicarrier system ACPR, EVM, and NPR measurements are commonly used. [6]

2.3.8. Dynamic Range

The range of an input signal that can be detected by a receiver without much distortion is called the dynamic range (DR). The dynamic range of an amplifier is defined as the ratio of the 1-dB gain compressed power output (P_{1dB}) to the amplified minimum detectable signal (P_{in}^{min}).

The output noise of a two-port device with noise figure *F* can be written as

$$N_o = FGkTB$$

If minimum detectable input signal is *X* (dB) above the noise floor, then

$$P_{in}^{min} = N_o - G + X(dB) \qquad P_{out}^{min} = P_{in}^{min} + G = N_o + X(dB)$$

Dynamic range is defined as

$$DR = P_{1dB} - P_{out}^{min} = P_{1dB} + 171 - 10\log B - NF - G(dB)$$

where P_{1dB} is in decibels above 1 mW (0 dBm). [6]

2.3.9. Stability

Any amplifier with power gain can be made to oscillate by applying external positive feedback, for example, a high-gain MMIC chip in a plastic or ceramic package with poor isolation. At

microwave frequencies unavoidable parasitic effects are often sufficient to cause oscillations if care is not taken in the design and fabrication of the amplifier. Any abrupt change in the DC parameters of the amplifier, output power with no input power, circuits that are very sensitive to their surroundings, and so on are typical indications of unwanted oscillations. Oscillations may occur at frequencies that don't propagate out the amplifier because they are filtered, are blocked by bias capacitors, or are below waveguide cutoff frequencies or at frequencies to which the test equipment is insensitive. It is not unusual for microwave amplifiers to oscillate anywhere between 1 MHz and 40 GHz or higher.

We will be discussing more in detail the stability aspects in the design chapter.

2.4. Amplifier Classes

In general, power amplifier operation classes can be divided into two major groups. The first one depends on the quiescent point or biasing DC point of operation of the transistor (also known as Q-point) and comprises classes A, B, AB and C. The second group is known as switching amplifiers and their operation is configured via the output matching networks with the transistor operating at saturation or cut-off (as a switch). This last group includes classes D, E and F. Despite of the class, there is a trade-off between linearity and efficiency, which will depend on the final application of the amplifier. High linearity generally means low efficiency and vice versa. In Figure 2.13, the biasing Q point for class-A, B and AB is shown.

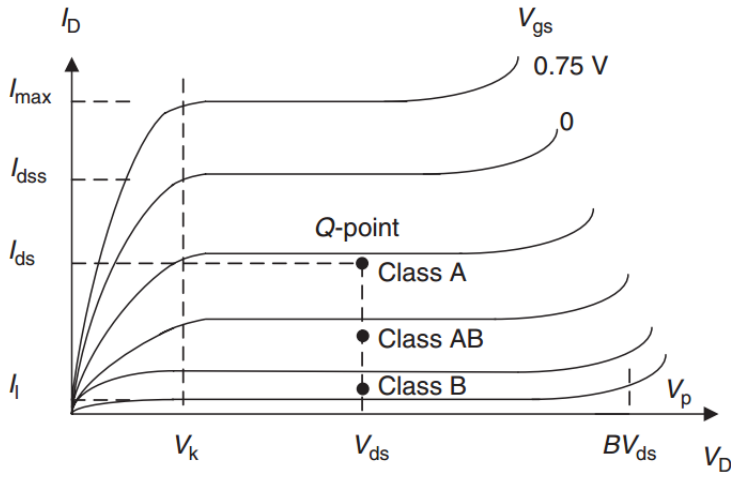


Figure 2.13 – Quiescent point for A, B and AB classes.

2.4.1. Class-A Amplifier

In class-A operation (Figure 2.13), the quiescent point is set near the centre of the load-line in order to achieve a full cycle conducting amplifier (i.e. the transistor is in its active region at all times for an input sinusoidal signal). This class offers the higher linearity as the output signal is an exact amplified replica of the input signal.

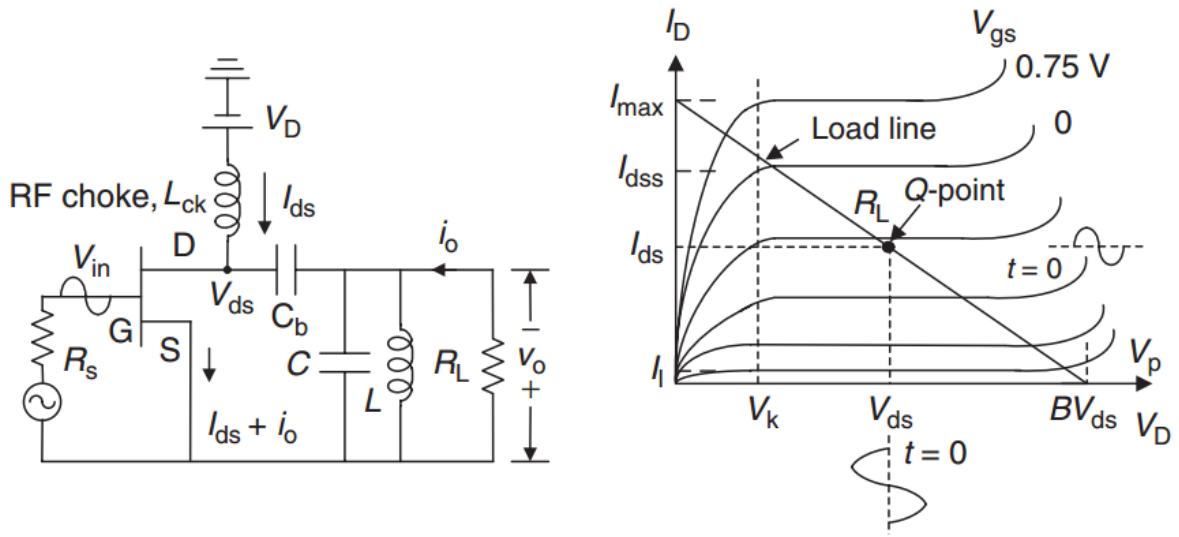


Figure 2.14 – Circuit topology for a class-A amplifier and its load line representation.

However, the maximum efficiency is η = 50%. Class-A amplifiers are very common in audio applications where the output signal must be undistorted, and in RF where the complex modulation schemes impose limitations on linearity, which usually come at the cost of efficiency.

2.4.2. Class-B Amplifier

In class-B operation (Figure 2.15), the quiescent point is set at the cut-off of the transistor. In this situation, the device will only be active for half-cycle for an input sinusoidal signal. Single-ended configuration (using only one transistor) has poor linearity as the output signal differs from the input signal. To overcome this problem, the push-pull configuration is typically used, where two transistors operating in class-B are configured in such a way that each of them is active for half cycle of the input signal, therefore providing a total output signal that is an amplified replica of the input signal. The linearity performance is not as good as class-A due to the non-perfect transitions from one transistor to another. However, the maximum efficiency for class-B amplifiers is improved up to $\eta = \frac{\pi}{4} = 78.5\%$.

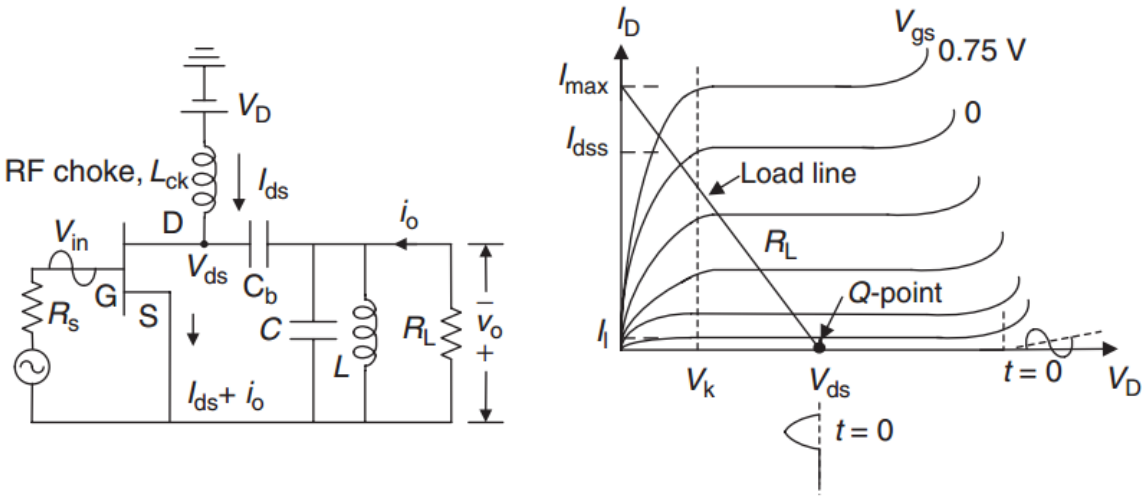


Figure 2.15 – Circuit topology for a class-B amplifier and its load line representation.

2.4.3. Class-AB Amplifier

In class-AB, the quiescent point of the device is set in a region between class-A and class-B operation. Typically used in single-ended configuration, class-AB amplifiers provide higher efficiency than class-A and better linearity when compared to class-B.

2.4.4. Class-C Amplifier

In class-C operation, the quiescent point is set below cut-off. Therefore the transistor is active for less than half-cycle of the input sinusoidal signal. This class of operation is highly non-linear as the output signal is very different from the input signal. However, as the transistor is turned on for a very short time, the efficiency of this class of operation is very high, theoretically reaching 100% when the transistor operates at very low conducting angles.

2.4.5. Class-D Amplifier

In class-D, the transistor operates as an electronic switch, usually using 2 transistors in a complementary architecture for alternating from saturation point (low impedance, ON state) to cut-off (high impedance, OFF). To reconstruct the input fundamental frequency signal, a band-pass filter is placed at the output of the amplifier. An ideal class-D amplifier would have 100% efficiency but the power lost in the harmonics and the switching (transition losses from one state to another as well as the leakage current in the cut-off state) reduce the efficiency.

2.4.6. Class-E Amplifier

Class-E amplifiers are very similar to class-D but they employ only one transistor, reducing the losses by shaping the drain voltage. This is done by including a tuned circuit at its output, so that the drain voltage is forced to be 0 when the switch is turned on.

2.4.7. Class-F Amplifier

Class-F amplifiers use waveform shaping at the output to reduce dissipated power. For shaping the desired output voltage and current waveforms, the even harmonics are short-circuited to produce a half-sinewave current waveform whilst the odd harmonics are open-circuited to produce a square voltage waveform. This is done via output matching networks that provide specific impedances at these harmonics. The transistor operates as a switch and has a theoretical efficiency equal to 100%. The efficiency is reduced in practice because of the impossibility of shorting and opening all infinite harmonics. In practice, only a reduced number of harmonics are controlled.

3. Amplifier Design Method

The design of amplifiers for a particular application and frequency range is complex in the sense that they have to meet the physical, electrical, thermal, and cost requirements. The amplifier performance requirements in terms of frequency band, gain, noise figure, power output, PAE, linearity, input and output VSWR, stability, ruggedness to mismatch, and so on are determined by the transistor type and sizes, the circuit design topology, matching networks, the number of gain stages, the aspect ratio for the devices between the stages, design methodology, biasing schemes, thermal design, fabrication technology, and packaging. More often it involves trade-offs in terms of size, electrical performance, reliability, and cost.

Before following up with the practical design is important to make some clarifications about stability, unilaterality and power gain which will make understand better the decisions made in the design.

3.1. Stability considerations

Any amplifier with power gain can be made to oscillate by applying external positive feedback, for example, a high-gain MMIC chip in a plastic or ceramic package with poor isolation. At microwave frequencies unavoidable parasitic effects are often sufficient to cause oscillations if care is not taken in the design and fabrication of the amplifier. Any abrupt change in the DC parameters of the amplifier, output power with no input power, circuits that are very sensitive to their surroundings, and so on are typical indications of unwanted oscillations.

In the case of power amplifiers, the stabilization of circuits becomes very critical as compared to small-signal amplifiers. Under large-signal conditions and pulsed operation, the devices go through large variations in their characteristics. Thus their design requires accurate nonlinear

transistor models, suitable CAD tools, and appropriate stability analysis techniques. Since most devices are only conditionally stable, and the systems mandate that the amplifiers must be unconditionally stable, the amplifier's stabilization becomes an integral part of the design. The oscillations in RF/microwave power amplifiers may be classified into five categories: even mode, odd mode, parametric, spurious parametric, and low frequency. In this project we will be focused mainly in even mode and a little in odd mode which are the most important.
Although our design is referred to a Class-A (non-pulsed operation), the stabilization is still important and must be performed in any case. [12]
Oscillation is possible if either input or output port has a negative resistance. If a net negative real part exists,

$$Re\{Z_S + Z_{in}\} < 0 \qquad \text{or} \qquad Re\{Z_{out} + Z_L\} < 0$$

the transient response will grow and oscillation will occur.
We can have two different scenarios in terms of stability:

1. Unconditional stability.
2. Conditional stability (or potentially unstable).

Unconditional Stability

$$|\Gamma_S| < 1 \qquad \text{and} \qquad |\Gamma_L| < 1$$

for any passive source and load. Graphically, this is

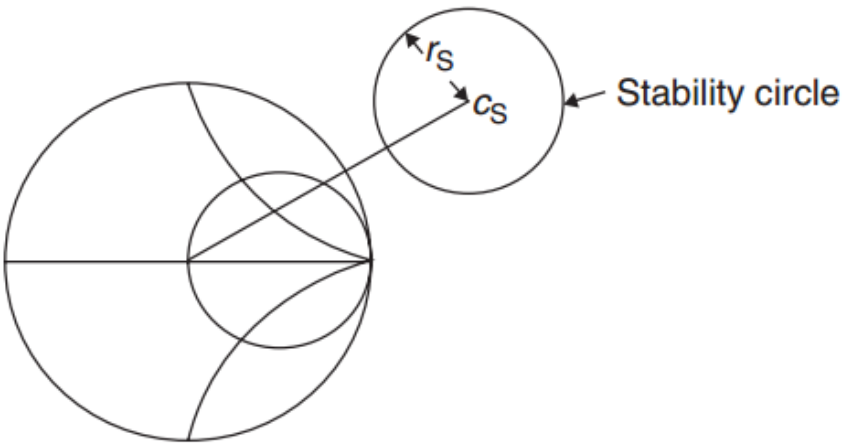


Figure 3.1 – Unconditional stability.

Unconditional stability is rather unusual for most microwave devices of interest. So, we must establish a method to determine regions in the Γ_S and Γ_L planes that are stable. We can either

avoid the unstable regions or modify the transistor with resistive loading to make it unconditionally stable.

Conditional Stability

This is the usual case. Also known as potentially unstable. Conditional stability means that there are a set of values in the Γ_S and Γ_L planes that make the amplifier unstable,

$$|\Gamma_S| > 1 \qquad \text{or} \qquad |\Gamma_L| > 1$$

Graphically, this is

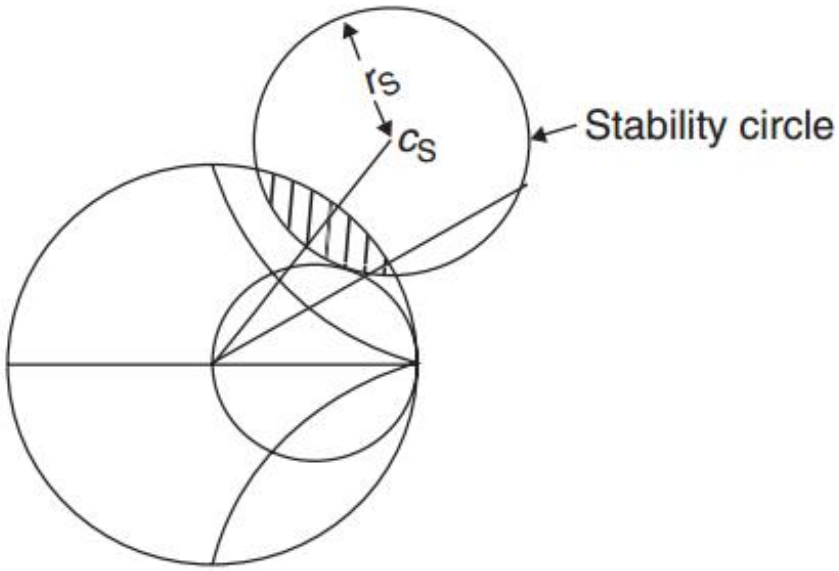


Figure 3.2 – Conditional stability.

Stability Factor

This is a less specific indicator of stability.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

If both conditions are satisfied, the unconditional stability is guaranteed.

Some things to consider about this factor:

1. If a transistor is potentially unstable, typically $|\Delta| < 1$ and $0 < K < 1$
2. Negative *K* values can occur, but result in most of the Smith Chart producing instability. If we try to stabilize to make the design unconditionally stable we must have a tradeoff between stability ($K \gg 1 \Rightarrow G \Downarrow\Downarrow$) and performance ($K \to 1^+ \Rightarrow G \to MSG$).

3. If we decide to work with a potentially unstable design, we must check for stability at all frequencies for which the device has a $K < 1$.

Summarizing we will have to choose one of the two options in order to start the design:

a. Work with a potentially unstable design choosing the right Γ_S and Γ_L values located in the stable region.

b. Make our design unconditionally stable adding resistors in various configurations (Figure 3.3). [14] [15]

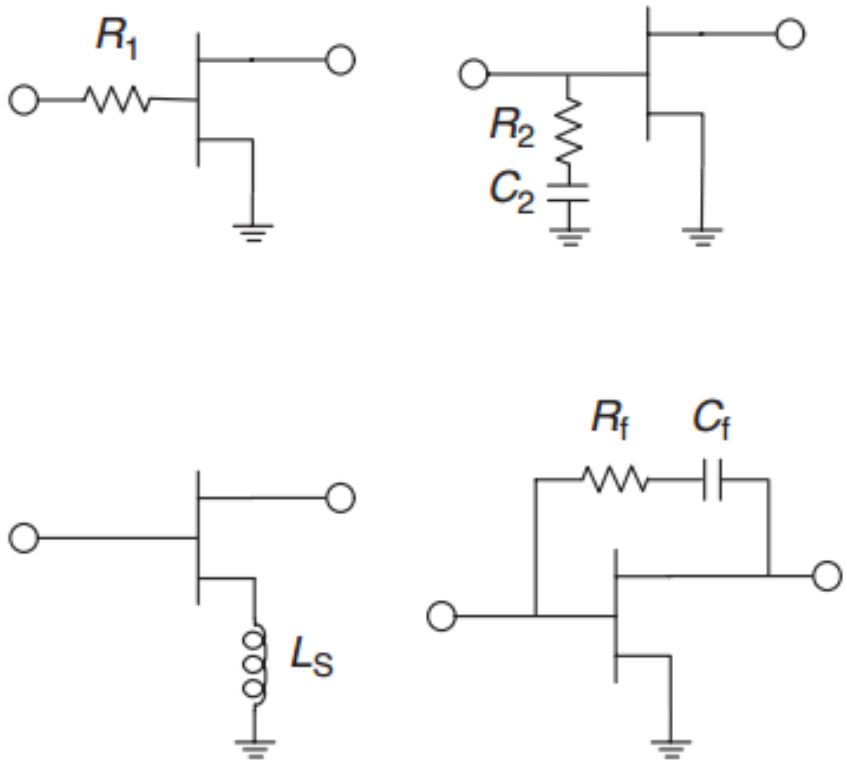


Figure 3.3 – Transistor stabilization schemes.

3.2. Unilateral Approximation

A 2-port network is defined as unilateral if it has no feedback from port 2 to port 1, otherwise it is bilateral. The 2-port network in this case is a transistor and mathematically, if $S_{12} = 0$, then it is said that transistor is unilateral. But it must be noted here that in practical cases, S_{12} is seldom zero. Such a non-zero S_{12} poses difficulties in designing amplifier with gains less than maximum gain. So as to justify simplifications in designing, the transistor can be assumed to be unilateral. But this introduces an error in the gain calculated by this assumption. This has a large effect on the design, as gain calculated at $S_{12} = 0$ and at $S_{12} \neq 0$ will be different. In

order to determine if the approximation is valid or not the ratio of transducer gain in bilateral case (G_T) to that in unilateral case (G_{TU}) is calculated. If S_{12} is actually zero, then the ratio will be unity; but here, S_{12} is assumed to be zero. Hence, the ratio will be some other value but unity. This deviation can be quantified by the *unilateral figure of merit* or '*U*'. It is used to calculate the maximum error range that may occur if a bilateral transistor is approximated to be unilateral.

The error range is given by:

$$\frac{1}{(1+U)^2} \leq \frac{G_T}{G_{TU}} \leq \frac{1}{(1-U)^2}$$

or

$$-20\log(1+U) < G_T - G_{TU}(dB) < -20\log(1-U)$$

Where,

$$U = \left|\frac{S_{11}S_{12}S_{21}S_{22}}{(1-|S_{11}|^2)(1-|S_{22}|^2)}\right|$$

As rule of thumb, the transistor can be assumed unilateral if this ratio of G_T/G_{TU} is between *±0.5dB*.

Though it is not a hard and fast rule, this range can be assumed as suited for the desired design. Hence, the range may vary with the application of the circuit. But, if this assumption is not valid then bilateral approach has to be followed. [8]

3.3. Gain considerations

Overall power gain must be less than G_{max}. This is called the *Maximum Available Gain* or *MAG* and it is defined as

$$G_{T,max} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2-1}\right)$$

Power gain is equal to G_{max} if input and output are conjugately matched using lossless matching networks. Although, amplifiers fail to attain G_{max} because:

1. They fail to match on both input and output.

2. They use lossy elements (resistors) to have stability.
3. They are potentially unstable. In that case, G_{max} is not possible due to oscillation. Then, *MSG*, the *Maximum Stable Gain*, is the upper useful limit for gain.

Maximum Stable Gain

For potentially unstable transistor the maximum allowed gain is one that is on the edge of stability, this is $K = 1$. This is

$$MSG = G_{T,max}\big|_{K=1} = \frac{|S_{21}|}{|S_{12}|}$$

This is used to describe the gain which could possibly be obtained from the device under a stable input and output match selection or after stabilization with resistive loading.

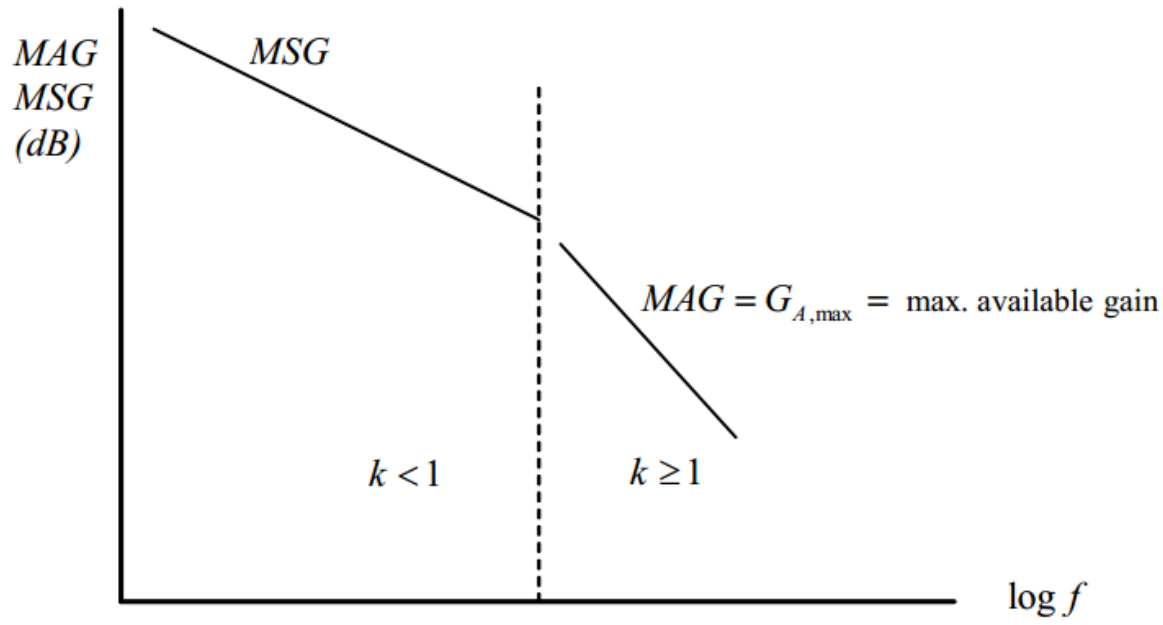


Figure 3.4 – Comparison between *MSG* and *MAG*.

Looking at Figure 3.4 we can see that as we increase in frequency the stability is increasing as well. So from low frequency until the frequency which makes *K = 1*, we will have to consider the *MSG* and from that frequency and above we can now consider the maximum gain possible (*MAG*).

The rest of different types of gain are already explained in Chapter 2 (section 2.3.2).

3.4. Design procedures

Design for Maximum Gain (Conjugate Matching)

Since G_0 is fixed for a given transistor, the overall transducer gain of the amplifier will be controlled by the gains, G_S and G_L, of the matching sections. Maximum gain will be realized when these sections provide a conjugate match between the amplifier source or load impedance and the transistor. Because most transistors exhibit a significant impedance mismatch (large $|S_{11}|$ and $|S_{22}|$), the resulting frequency response may be narrowband.
Thus, we know that maximum power transfer from the input and output matching network to the transistor will occur when

$$\Gamma_{in} = \Gamma_S^* \qquad \text{and} \qquad \Gamma_{out} = \Gamma_L^*$$

In the general case with a ***bilateral*** ($S_{12} \neq 0$) transistor, Γ_{in} is affected by Γ_{out} and vice versa, so the input and output sections must be matched simultaneously.

$$\Gamma_S = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}$$

The variables are defined as

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2,$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2,$$

$$C_1 = S_{11} - \Delta S_{22}^*$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

Solutions to the expressions for Γ_S and Γ_L are only possible if $K > 1$, this is: unconditionally stable. If the device is potentially unstable it will be difficult to apply the conjugate matching, so it will be better to specify a gain less than the MSG.
The results are much simpler for the ***unilateral* case**. When $S_{12} = 0$, *we have*

$$\Gamma_S = S_{11}^* \qquad \text{and} \qquad \Gamma_L = S_{22}^*$$

Design for Specified Gain

In many cases it is preferable to design for less than the maximum obtainable gain, to improve bandwidth or to obtain a specific value of amplifier gain. This can be done by designing the input and output matching sections to have less than maximum gains; in other words, mismatches are purposely introduced to reduce the overall gain. The design procedure is facilitated by plotting constant-gain circles on the Smith chart to represent loci of Γ_S and Γ_L that give fixed values of gain (G_S and G_L).

If our transistor is ***unilateral*** or can be considered as such:
The centres of each family of circles lie along straight lines given by the angle of S_{11}^* or S_{22}^*.
Note that when g_S (or g_L) = 1 (maximum gain), the radius R_S (or R_L) = 0, and the centre reduces to S_{11}^* (or S_{22}^*), as expected. In addition, it can be shown that the 0 dB gain circles (G_S = 1 or G_L = 1) will always pass through the centre of the Smith chart. These results can be used to plot a family of circles of constant gain for the input and output sections.
Then Γ_S and Γ_L can be chosen along these circles to provide the desired gains. The choices for Γ_S and Γ_L are not unique, but it makes sense to choose points close to the centre of the Smith chart to minimize mismatch, and thus maximize bandwidth.

Potentially unstable bilateral case:

1. For a given G_p, draw the constant operating power-gain circle and also draw the output stability circle. Select a value of Γ_L that is in the stable region and not too close to the stability circle.
2. Calculate Γ_{IN} using

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$$

   and determine if a conjugate match at the input is feasible. That is, draw the input stability circle and determine if $\Gamma_S = \Gamma_{IN}^*$ lies in the input stable region.
3. If $\Gamma_S = \Gamma_{IN}^*$ is not in the stable region or is in the stable region but very close to the input stability circle, the value of Γ_S can be selected arbitrarily or a new value of G_p can

be selected. Of course, we must be careful selecting Γ_S arbitrarily since such value affects the output power and the *VSWR*.

Due the great range of possibilities we can see better the procedure that must to be taken in Figure 3.5 depending on our situation.

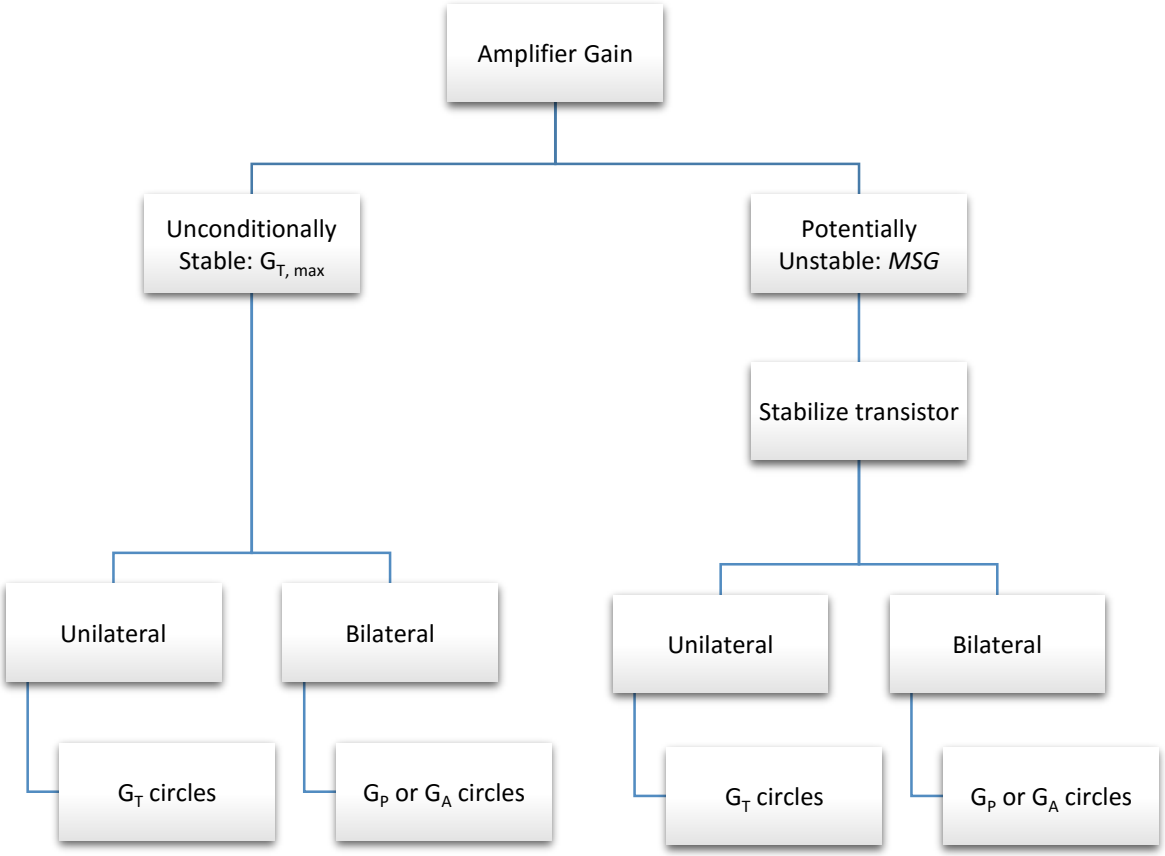


Figure 3.5 – Design procedure depending on stability, gain and unilaterality.

In all cases, we must also verify that the amplifier is stable over a wide frequency range. For further explanations about the design procedure can be found in [14] and [16].

After these fundamental explanations, now we are able to start the design. To make the process guided and have a general idea about the step by step we followed a chart shown in Figure 3.6.

3.5. Selection of the microwave transistor

The first decision that must to be made is obviously the kind of transistor that you will be working with. To meet the required specifications, various families of devices are available

(see Chapter 2, section 2). Selection of a proper family and hence a proper device such that it works as intended is very essential. Thus, a detailed study of various datasheets must be done before selecting a device. [8]

Regarding our specifications and they have become very popular in the last years we decided to use a GaN HEMT (Gallium Nitride High Electron Mobility Transistor). GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making them ideal for linear and compressed amplifier circuits. Apart from that, low energy consumption it is another of its main advantages. [5][9]

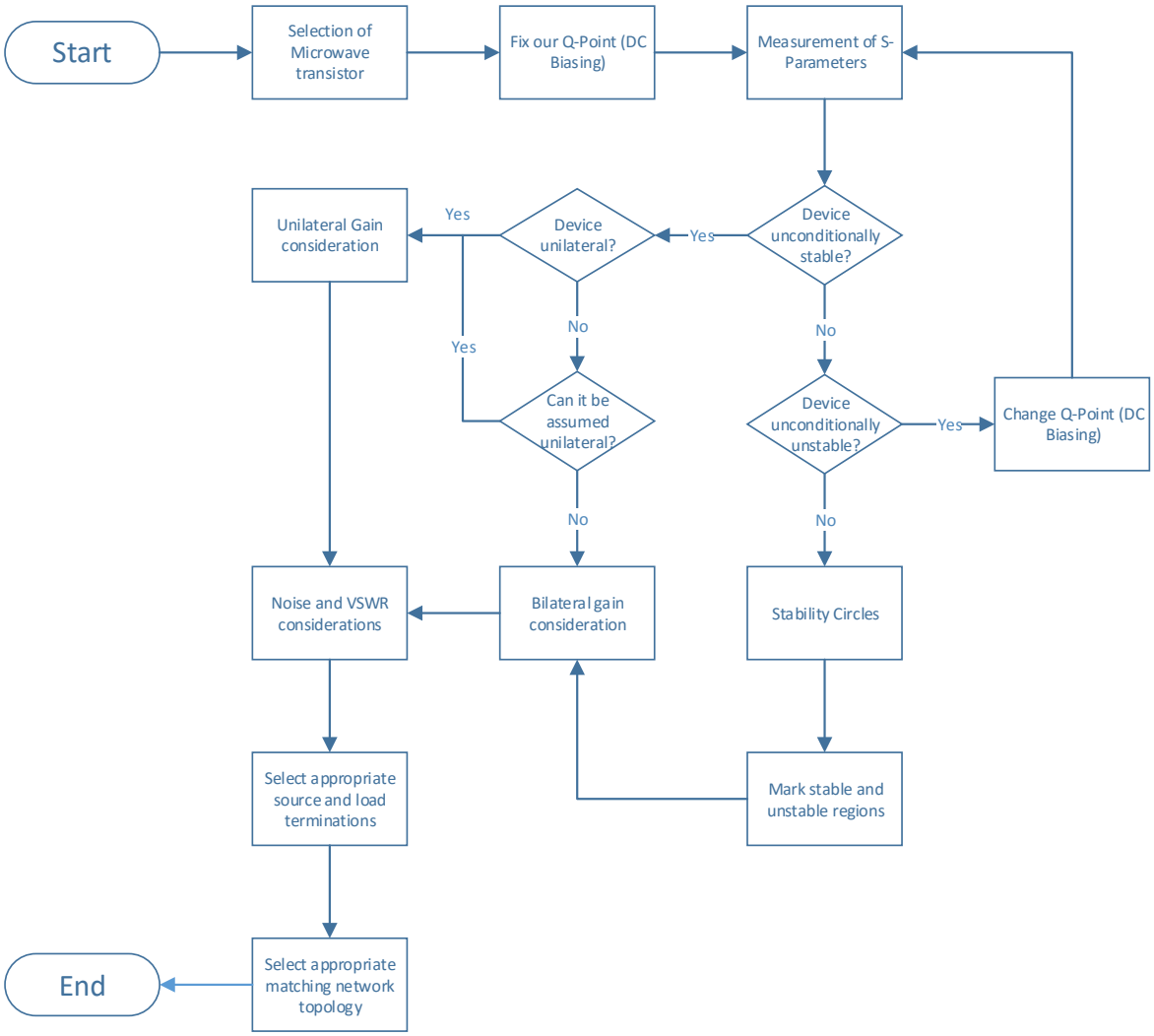


Figure 3.6 – Power amplifier design basic flow chart.

Taking into account of all these advantages, the transistor finally chosen is from Cree Inc. The model is CGH40010F [9], such large signal model for AWR has been downloaded from the RF portal that Cree has on its website. Maximum ratings of this model are shown in Table 3.1.

Absolute Maximum Ratings (not simultaneous) at 25˚C Case Temperature

Parameter	Symbol	Rating	Units	Conditions
Drain-Source Voltage	V_{DSS}	84	Volts	25˚C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25˚C
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	4.0	mA	25˚C
Maximum Drain Current[1]	I_{DMAX}	1.5	A	25˚C
Soldering Temperature[2]	T_S	245	˚C	
Screw Torque	τ	60	in-oz	
Thermal Resistance, Junction to Case[3]	$R_{\theta JC}$	8.0	˚C/W	85˚C
Case Operating Temperature[3,4]	T_C	-40, +150	˚C	

Table 3.1 – GaN HEMT CGH40010 maximum ratings.

3.6. Transistor Characterization

The first thing that must be done is the transistor characterization, which means that plotting de I-V characteristics the designer will be able to see the active region in which he can fix the Q-Point.

A current–voltage characteristic or I–V curve is a relationship, typically represented as a chart or graph, between the electric current through a circuit (in our case the current through the drain and source, I_{ds}), and the corresponding voltage, or potential difference across it (the voltage between drain and source, V_{ds}). Each curve on the graph correspond to different values of voltage at the gate, V_{gs}. Thus, in order to plot the I-V characteristics, the maximum drain-source voltage (84V) and the maximum gate-to-source voltage (-10V, +2V) are taken.

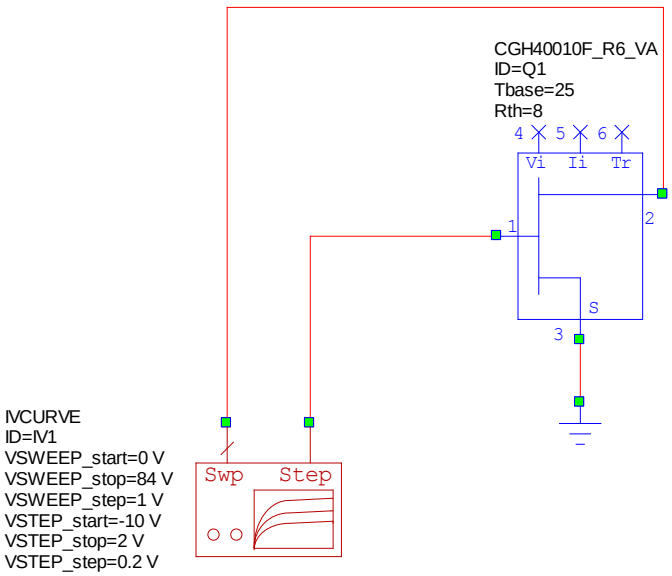


Figure 3.7 – Schematic for measuring the IV curves.

Once the non-linear model is imported to AWR [10], a schematic with the *IVCURVE* element is created. This element is the one which performs the IV characteristics plot shown in Figure 3.7. The resulting IV curves are shown in Figure 3.8.

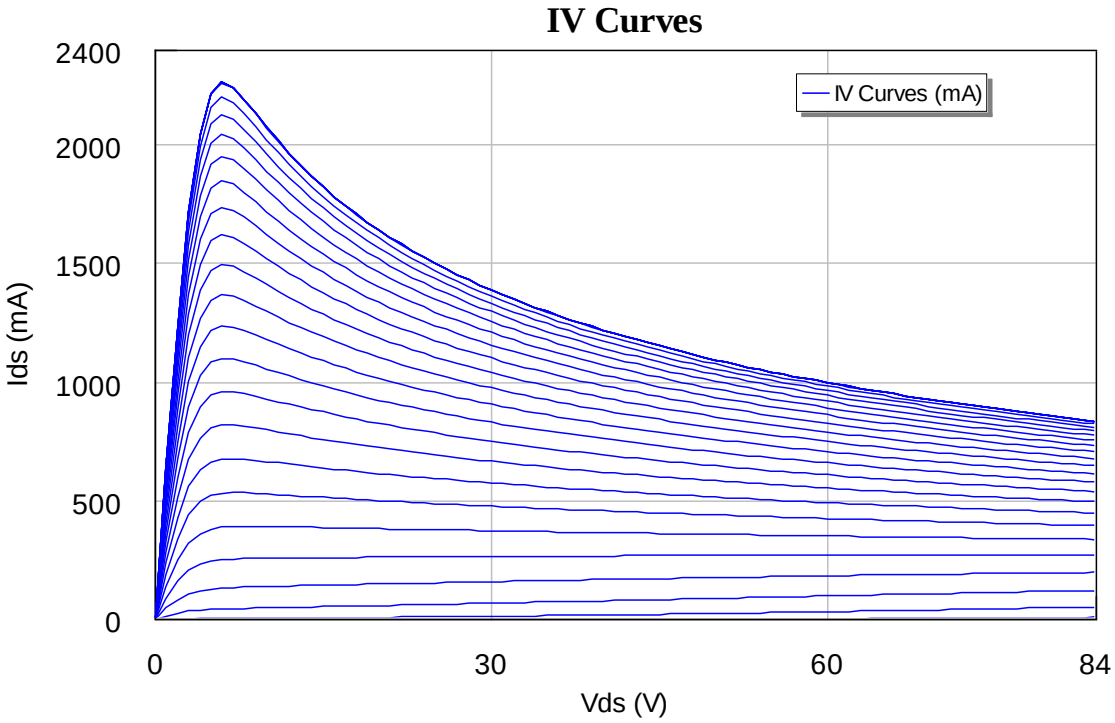


Figure 3.8 – CGH40010 IV curves.

3.7. Safe Operating Area, Q-Point and Dynamic Load-Line

Now we have to choose the bias conditions. We must fix the V_{gs} and V_{ds} voltages which will fix our Q-Point somewhere in our active region. To define the *Safe Operating Area* we need to mark in the IV characteristics graph the limits which makes the transistor break. Such limits are five:

- Cutoff region.
- Saturation region.
- Maximum drain current.
- Maximum drain voltage.
- Maximum power dissipation.

The cutoff and saturation regions are obtained by visual approximation on the IV graph. The maximum drain current and voltage are given in Table 3.1, and the maximum power dissipation can be observed in the *Power Dissipation De-rating* Curve (Figure 3.9) which can be found in the datasheet.

Taking the maximum power dissipation from that graph (14W), we have

$$P_{diss} = P_{gate} + P_{drain} \approx P_{drain} = V_{ds} \cdot I_{ds}$$

As we can see in the equation above, the power dissipated at the gate is so small compared to the power dissipated at the drain that is negligible.

$$P_{dissMax} = 14 \approx V_{ds} \cdot I_{ds}$$

$$\boldsymbol{I_{ds} \approx \frac{14}{V_{ds}}}$$

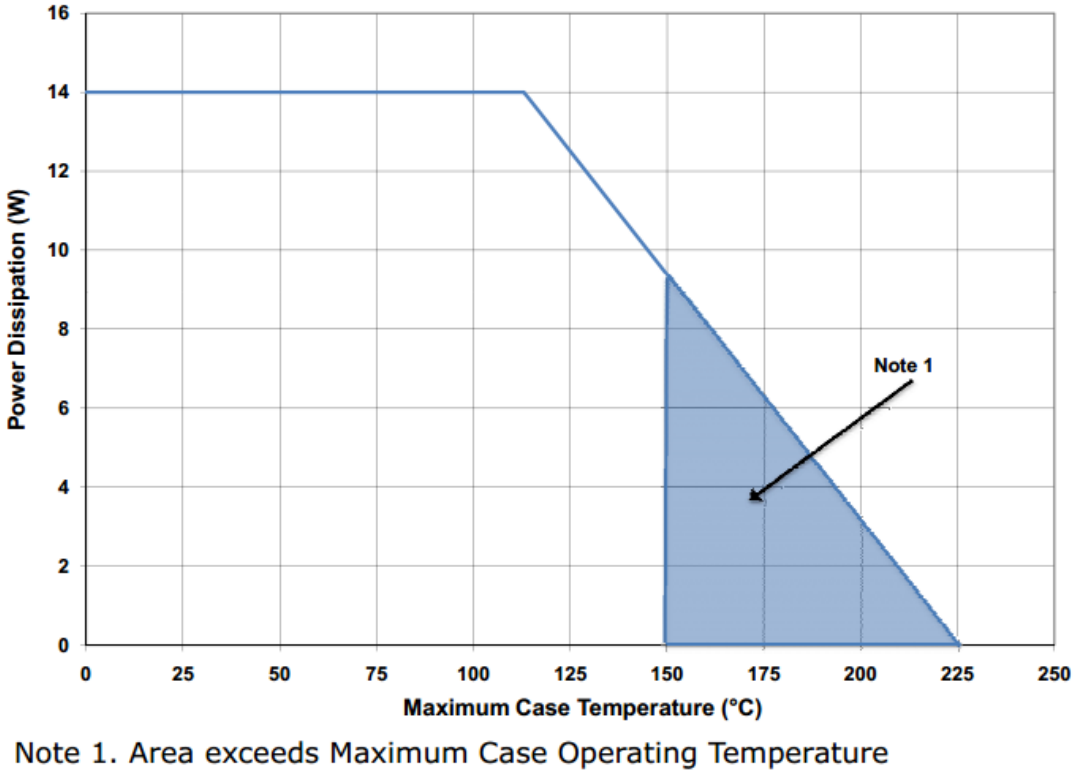


Figure 3.9 – CGH40010 Power Dissipation De-rating Curve.

From the last equation we will be able to plot the power dissipation limit curve. Taking into account about all limits, we have defined the *Safe Operating Area* (SOA). Such area can be observed in Figure 3.10.

Hence, considering the SOA and that we designed our Power Amplifier to work in Class-A, we finally chose the following values (shown in Figure 3.10.):

$$V_{gs} = -2.2\ V$$

$$V_{ds} = 28\ V$$

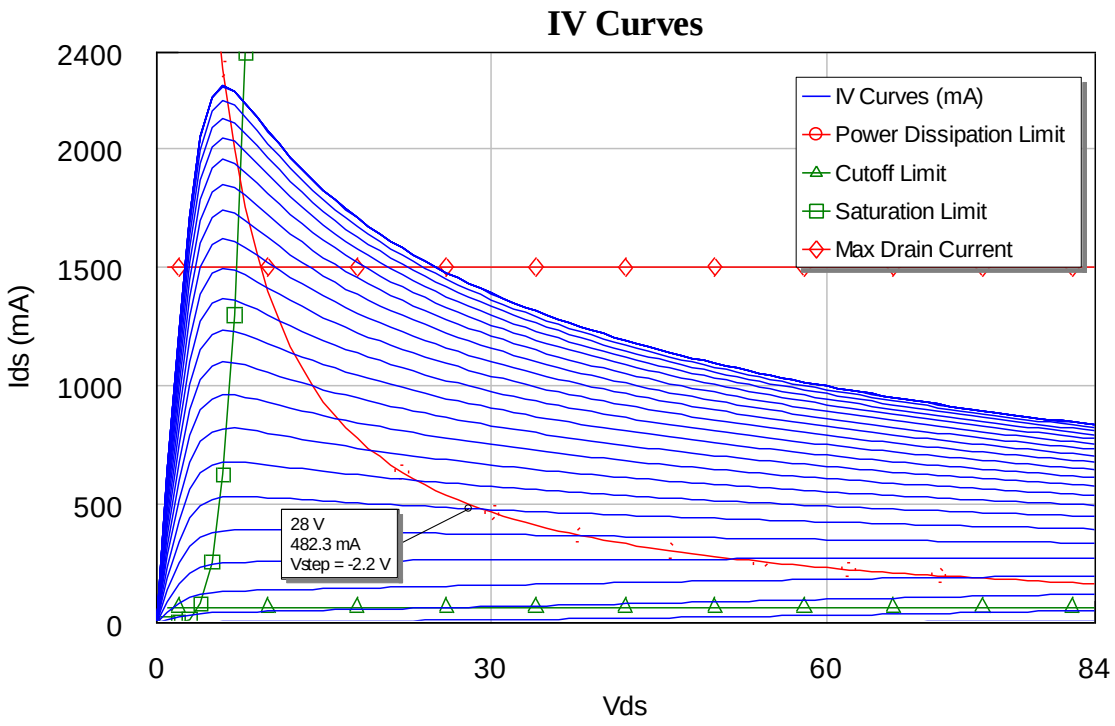


Figure 3.10 – Safe Operating Area and Q-Point.

As we can see, we chose approximately one of the conditions given in the datasheet (Vds=28V and Idq=500mA).

Now we have to plot de *AC* or *Dynamic Load Line* (DLL). We will be able to see the operating region of our transistor in class-A. To plot this line we have to choose the maximum input power just to check the behaviour of the signal swing (worst case). For doing this the typical maximum input power chosen is the P_{1dB}. To calculate it we have first to obtain the Gain response applying a sweep to the input power (see Figure 3.12).

The obtained gain, shown in Figure 3.6, has a value in linear region of 11.89dB, hence the P_{1dB} will be the input power which makes the gain decrease 1dB. As we can see in Figure 3.11, this value is 27.6dBm. So now we enable the fixed input power port (*PORT1*) with that value and thus, we can obtain the DLL at P_{1dB}.

On the other hand, in the schematic in Figure 3.12 we have a couple of things to comment. The *LTUNER2* is the component which will be responsible of either load and source pull simulations. We can see in fact that this component has three ports. The third one is for the biasing, so it can mix DC and RF signals with any problem. After we make the load and source pull simulations we will have to replace this components by the matching and bias networks, including the block capacitors and the RF chokes to avoid the DC or RF leaking, respectively.

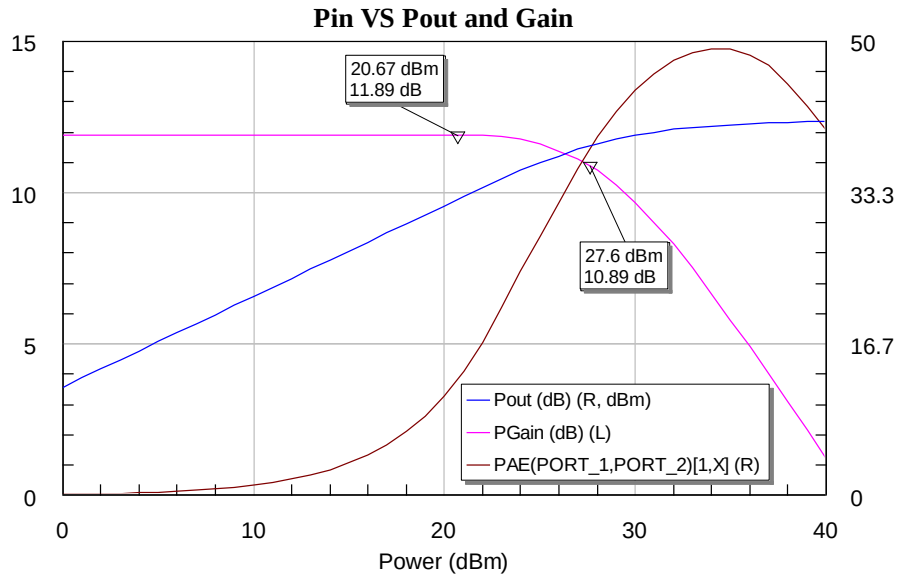


Figure 3.11 – CGH40010 P_{out}, Gain and PAE.

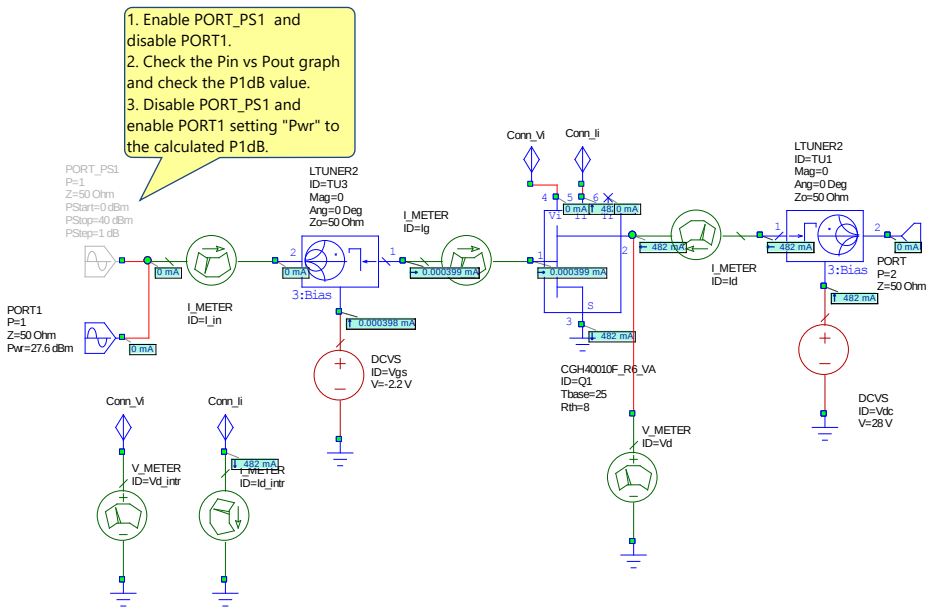


Figure 3.12 – Schematic for testing the P_{out}, Gain and PAE.

Regarding the transistor model, it has six pins. The *Vi* and *Ii* pins are really important when we want to plot the DLL. We know that inside the transistor we have inductive and capacitive parasitics which make *Vds* and *Ids* be out of phase [17]. In other words, our load line will not be a straight line as we saw in theory, it will be an ellipse. [11]

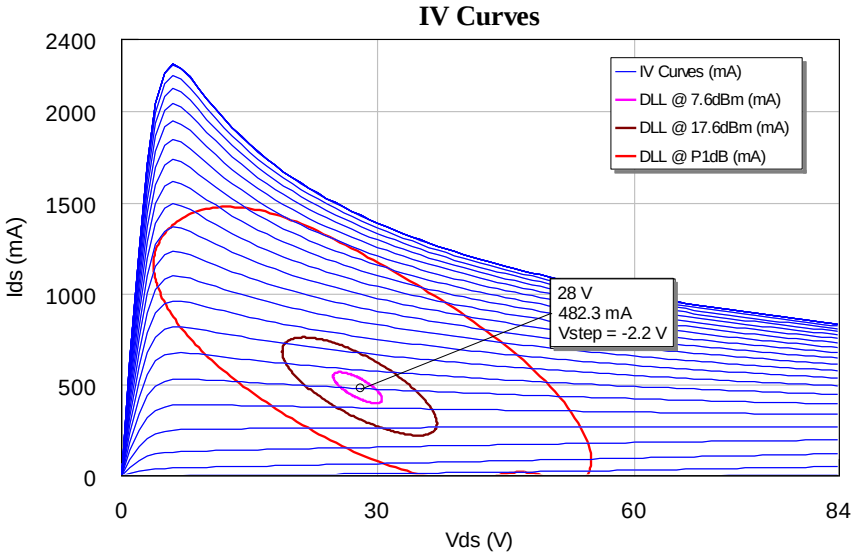


Figure 3.13 – DLLs with different input powers.

We appreciate in Figure 3.13 that when we are working at P_{1dB} (red curve) our transistor starts to saturate leading to nonlinearities.

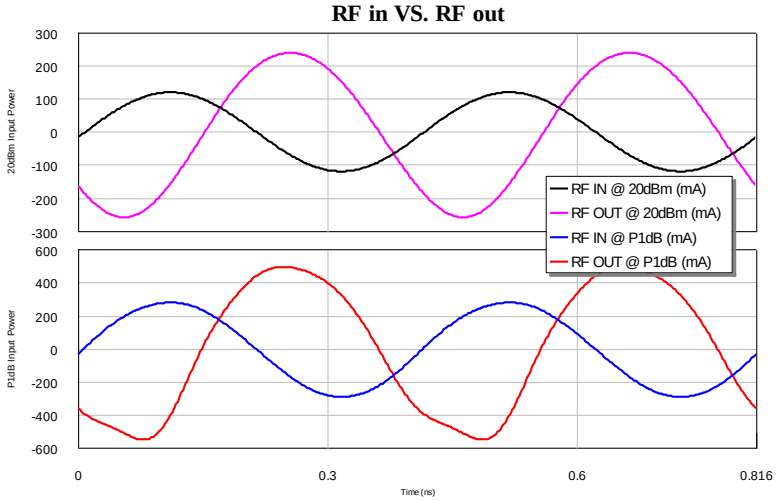


Figure 3.14 – Current waveforms both in linear and saturation.

In Figure 3.14 we can see the input and output current waveforms at two different input powers (at 20dBm and P_{1dB}). We can notice there how the transistor starts saturating at P_{1dB}.

3.8. Stability analysis

To start the stability analysis we need the S-Parameters at our working frequency

At 2.45GHz we obtained in AWR the following values:

Frequency (MHz)	S(1,1)[X,28] Unitless data (Mag) Pwr = 27 dBm	S(1,1)[X,28] Unitless data (Ang: Deg) Pwr = 27 dBm	S(1,2)[X,28] Unitless data (Mag) Pwr = 27 dBm	S(1,2)[X,28] Unitless data (Ang: Deg) Pwr = 27 dBm	S(2,1)[X,28] Unitless data (Mag) Pwr = 27 dBm	S(2,1)[X,28] Unitless data (Ang: Deg) Pwr = 27 dBm	S(2,2)[X,28] Unitless data (Mag) Pwr = 27 dBm	S(2,2)[X,28] Unitless data (Ang: Deg) Pwr = 27 dBm
2450	0.91132	163.05	0.020608	-33.514	3.9334	43.269	0.39584	-160.52

$$S_{11} = 0.91132\angle 163.05° \qquad S_{12} = 0.020608\angle -33.514°$$

$$S_{21} = 3.9334\angle 43.269° \qquad S_{22} = 0.39584\angle -160.52°$$

Now with these values we will check the stability of our transistor. First we must know if it is unconditionally stable that means as we explained before that we can put no matter which matching input and output networks and our system will keep stable.

This condition is checked with *Rollet's condition*, defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

also named K-Δ test.

In AWR are used this two inequalities to check unconditional stability,

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

$$\mathrm{B_1} = 1 + |\mathrm{S_{11}}|^2 - |\mathrm{S_{22}}|^2 - |\Delta|^2 > 0$$

In our case we have the following results using the S-Parameters at 2.45GHz mentioned before:

Frequency (MHz)	K()[X,28] 0_PA_Characteriz... Pwr = 27 dBm	B1()[X,28] 0_PA_Characteriz... Pwr = 27 dBm
2450	0.56435	1.5951

As we can see B1 agrees the inequality but it does not happen with K which is lower than 1. So this proves that there will be potential unstability depending on the load and source matching network reflection coefficients.

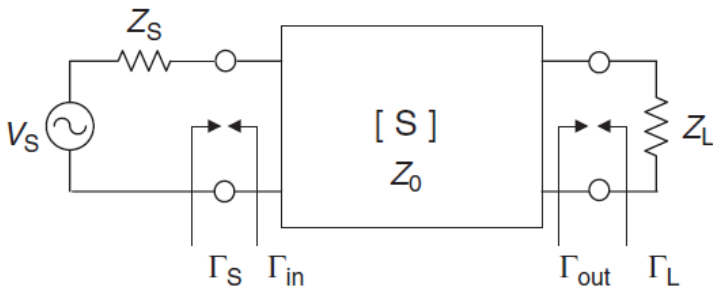


Figure 3.15 – Two-port network of a transistor amplifier.

A region is stable if all its points agrees with the expression

$$|\Gamma_{in}| < 1 \quad \text{and} \quad |\Gamma_{out}| < 1$$

The stability circle are the points which makes as the frontier between stable and unstable regions. This is

$$|\Gamma_{in}| = \left|S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right| = 1$$

$$|\Gamma_{out}| = \left|S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}\right| = 1$$

But we have to know which part of the circle is stable, inside or outside it?

To check this is as simple as taking $\Gamma_L = 0$ (the centre of the Smith Chart), so the center will be stable if

$$|S_{11}| < 1$$

$$|S_{11}| = 0.91132 < 1$$

And for the output the center will be stable if

$$|S_{22}| < 1$$

$$|S_{22}| = 0.39584 < 1$$

Both are stable at the centre of the Smith chart, so that means that the region that belongs there is all stable.

Now if we apply these equations in AWR, the graphical representation of these stability circles is really easy. We do this using the AWR measurement called *SCIR1* for the input (source) and *SCIR2* for the output (load). The result is shown in Figure 3.16.

The intersection between the Smith Chart and the pink circle is the unstable region for the output, the rest are all stable points for the output. And the intersection between the Smith Chart and the blue circle is the unstable region for the input. This reveals that only these little areas makes our amplifier be unstable which is good.

A very useful thing to comment are the dashed lines, whose meaning is to answer the question that we made before. It specifies the unstable region, actually the dashed lines are in such region. So thanks to this simple thing, we can directly graph the stability circles and see the stable regions without using any of the formulas above.

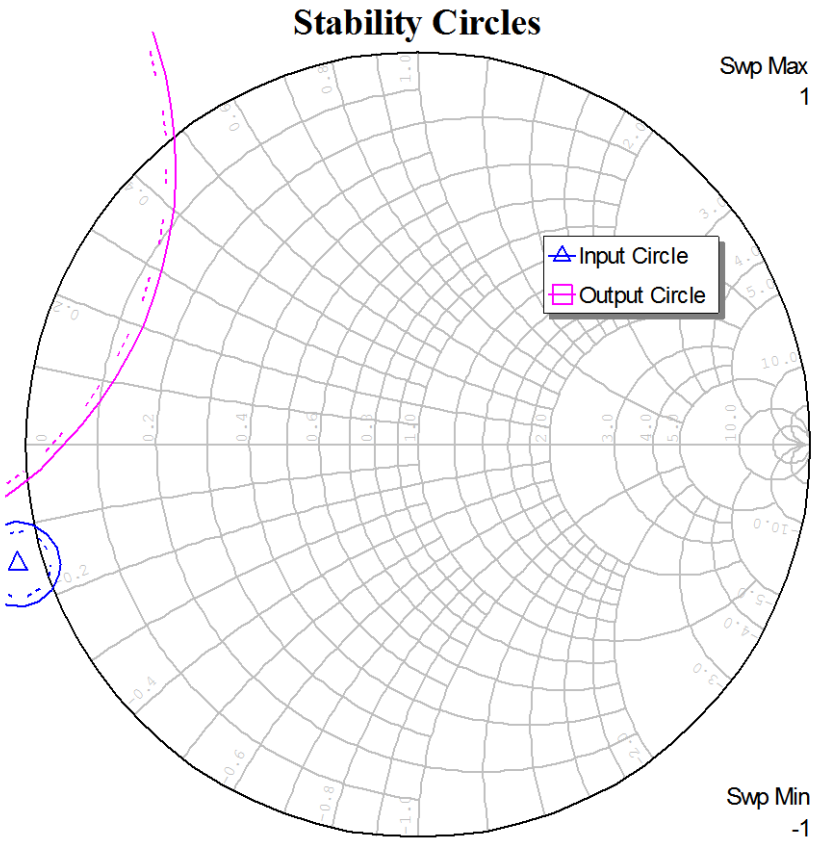


Figure 3.16 – Input and output stability circles at 2.45GHz.

3.9. Unilateral approximation

As we discussed in previous sections, we can approximate our device as unilateral one if the error committed is not too big.

$$U = \left|\frac{S_{11}S_{12}S_{21}S_{22}}{(1-|S_{11}|^2)(1-|S_{22}|^2)}\right| = 0.2046$$

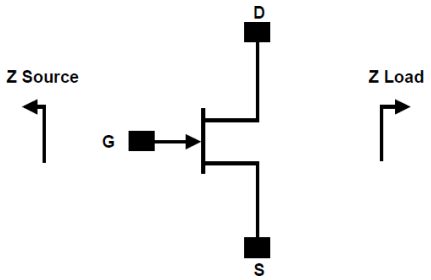
$$-20\log(1+U) < G_T - G_{TU}(dB) < -20\log(1-U)$$

$$-3.7225\ dB < G_T - G_{TU}(dB) < 4.5775\ dB$$

As we can see, the error is too big. Thus, we must considerate the *bilateral* design.

3.10. Load-Pull Simulation

The transistor data sheet from the manufacturer usually specifies a list of optimal source and load impedances of the transistor at different frequencies, under a certain bias setting. The manufacturer obtains these values experimentally. In our case, these impedances are shown in Figure 3.17. If one happens to design under the specified conditions, then the task is simplified into transforming the source and load impedances into those listed in the table. However, the manufacturer can only give these parameters at certain frequencies and a certain bias setting. To get these parameters a design procedure is developed based on *load pull method*. [13]



Frequency (MHz)	Z Source	Z Load
500	20.2 + j16.18	51.7 + j15.2
1000	8.38 + j9.46	41.4 + j28.5
1500	7.37 + j0	28.15 + j29
2500	3.19 - j4.76	19 + j9.2
3500	3.18 - j13.3	14.6 + j7.46

Note 1. V_{DD} = 28V, I_{DQ} = 200mA in the 440166 package.
Note 2. Optimized for power, gain, P_{SAT} and PAE.
Note 3. When using this device at low frequency, series resistors should be used to maintain amplifier stability.

Figure 3.17 – Optimal load and source impedances at some frequencies for the CGH40010.

This method basicaly consists in using an element (*LTUNER2*) which sweeps the reflection coefficient in a set of *gamma* points at the output checking the important parameters such as *PAE*, G_{Trans}, etc, just to find the optimal one. The output reflection coefficient chosen must be one that agrees with our requirements and makes the power amplifier work in a stable region over the whole bandwidth.

Step by step we must make the following

1. Go to the menu in AWR: Scripts -> Load Pull -> Create_Load_Pull_Template
2. In the new schematic you have to follow the instructions given there (such as setting your bias conditions, changing the sample transistor by the DUT, etc.)

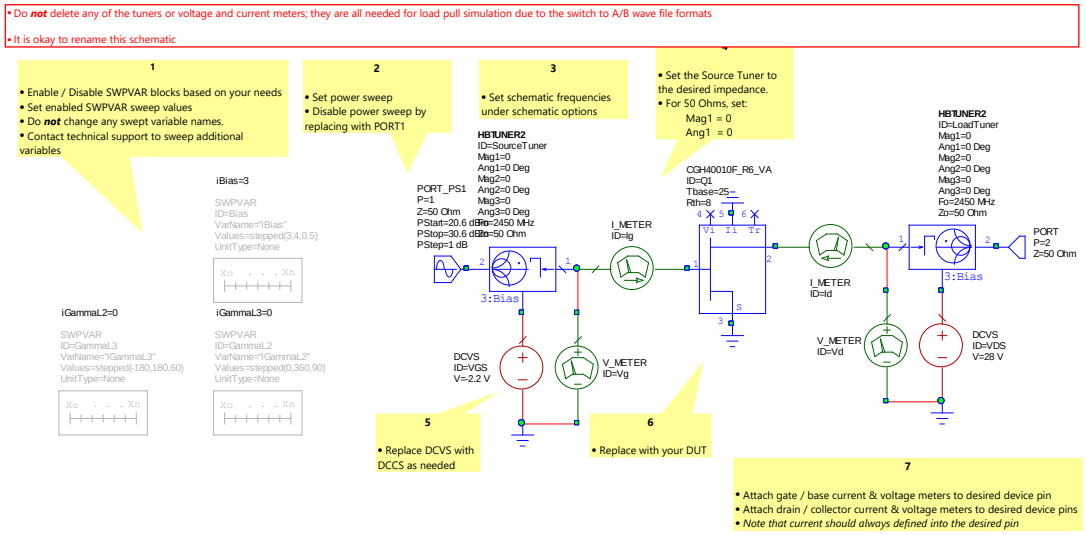


Figure 3.18 – Load-Pull template generated automatically.

3. Once you have finished configuring this schematic, go to the menu in AWR: Scripts -> Load Pull -> Load_Pull
4. Set the points in the Smith Chart that you want to test following the steps given.

When simulation is complete, we will have all the Load Pull data in the *Data Files* folder.

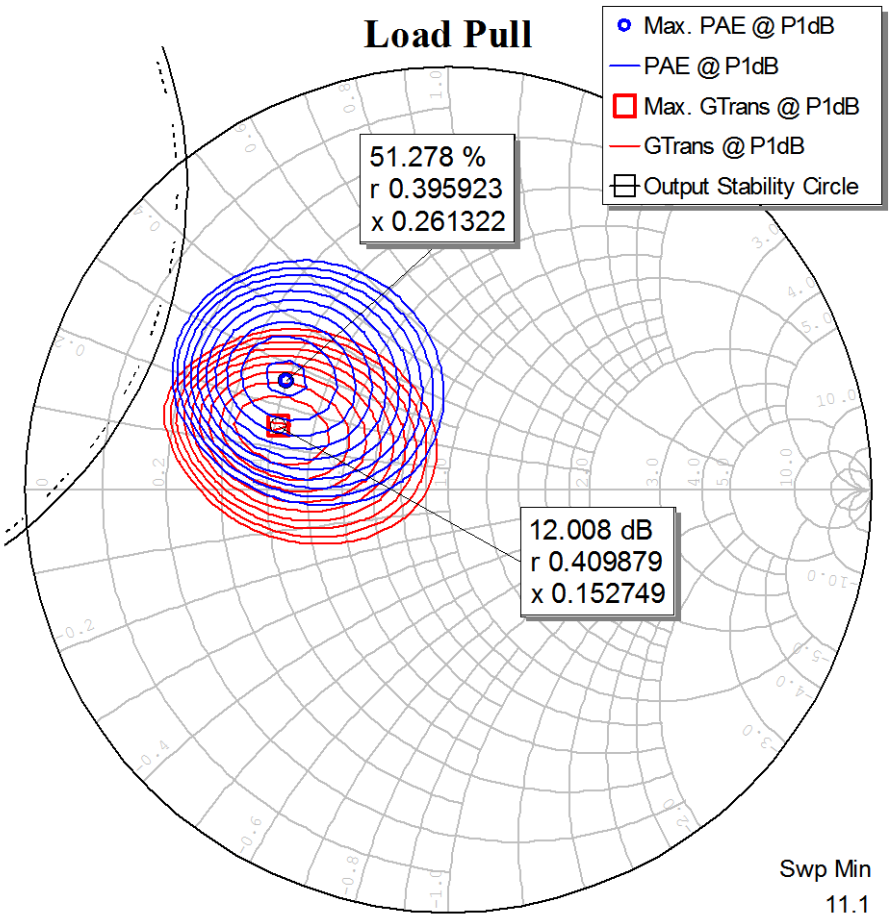


Figure 3.19 – G_{Trans} and PAE contours.

As we can see in the graph above, at P_{1dB} input power we have a maximum PAE of 51.278% and a maximum of Gain of 12.008dB. The good thing is that those points are really close one to each other so we will take the load reflection coefficient in that area.

Making a sweep in the input power from 0 to P_{1dB} de contours don't move too much, so we will take a point between the two maximums (PAE and GTrans). This point is

$$\Gamma_{out} = 0.44152\angle 149.3904°$$

Thus, we designed a matching network with that reflection coefficient. Then we checked if it works as we want in our frequency range,

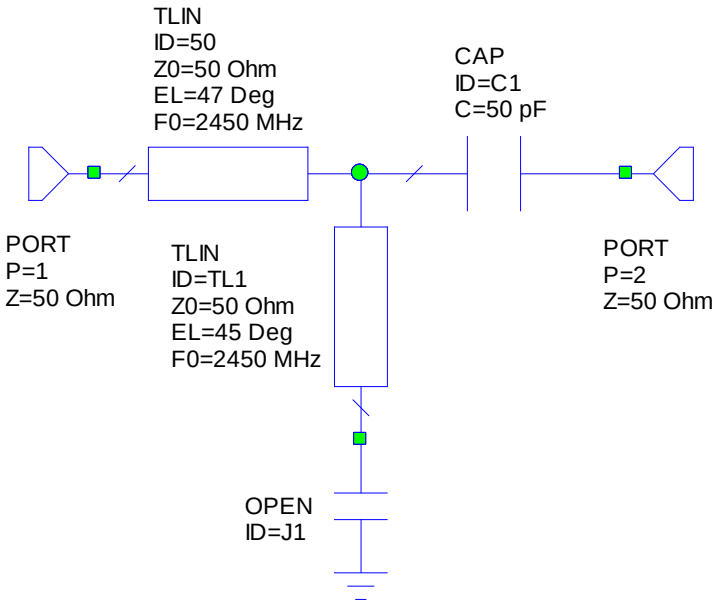


Figure 3.20 – Output matching network.

The capacitor *C1* is a block capacitor just to make sure that there is any DC leakage.

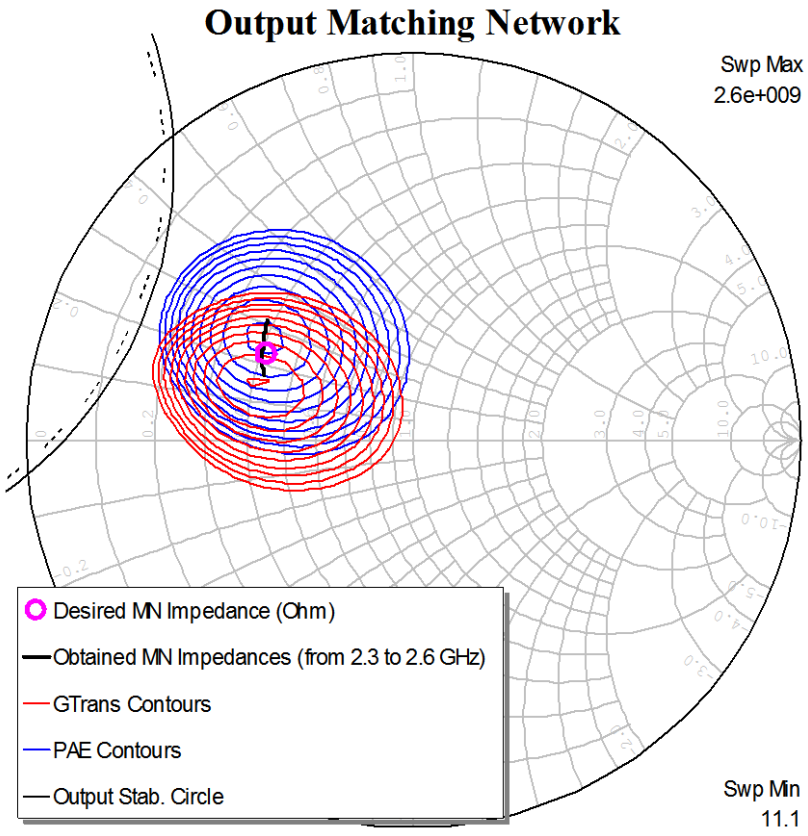


Figure 3.21 – Desired-Obtained OMN comparison.

As we can see in Figure 3.21 our output matching network achieves our desired impedance at the desired frequency range.

Now, we performed a manual analysis with the Optimizer tool provided in AWR in order to get the best reflection coefficient at the input. As we predicted in past sections, to achieve the maximum power transfer between the input and the transistor we must take the Γ_{IN} conjugate. The result was the following

$$\Gamma_S = 0.85\angle -163°$$

This result is not exactly the conjugate because we observed that lied really close to the input stability circle, so we decided to take distance from there to avoid possible unstabilities. Thus, we designed a matching network with that reflection coefficient. Then we checked if it works as we want in our frequency range,

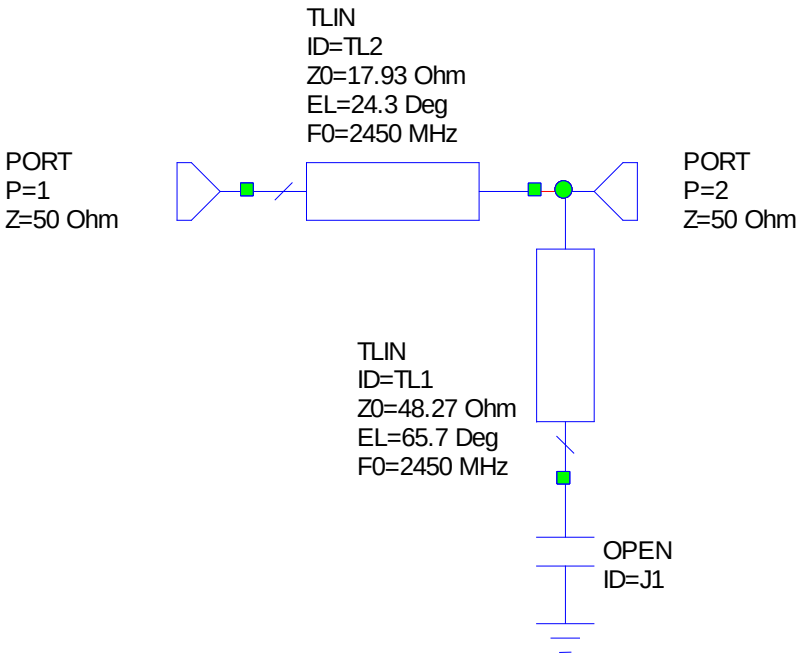


Figure 3.22 – Output matching network.

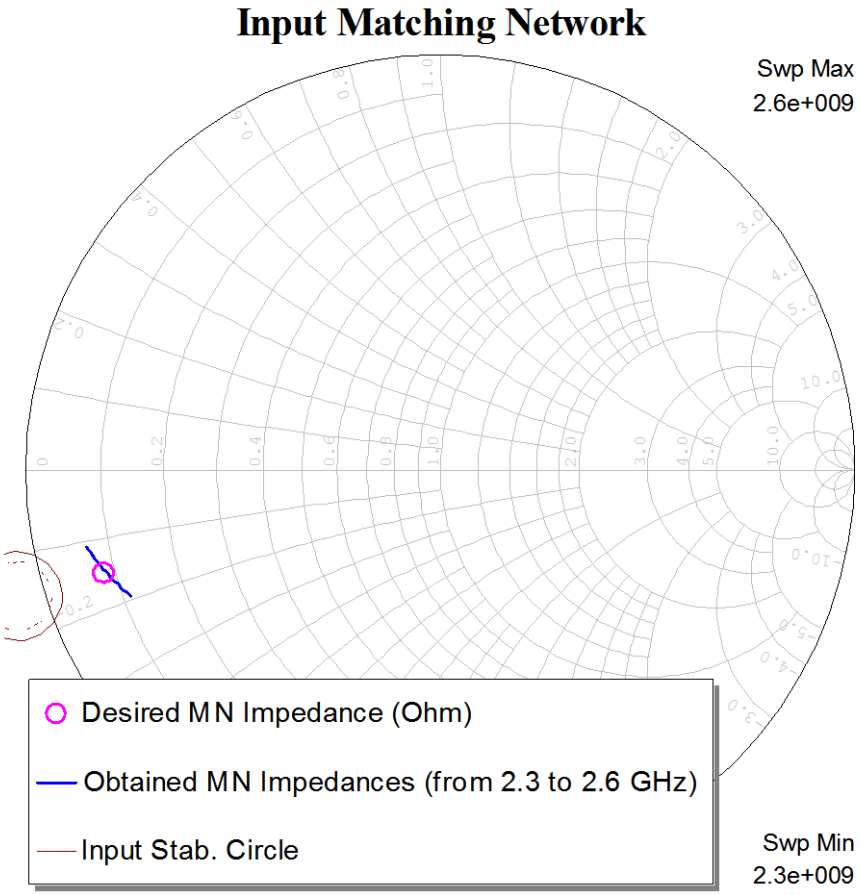


Figure 3.23 – Desired-Obtained IMN comparison.

As we can see in Figure 3.23 our input matching network achieves our desired impedance at the desired frequency range.

3.11. Biasing networks

Biasing of devices is an important part of an amplifier design. The design considerations for biasing circuits are higher gain, lower noise figure, high efficiency, oscillation suppression, single source power supply, RF choking, and desirable impedance matching. Biasing circuit design considerations consist of a proper biasing topology and selection of the conductor dimensions to meet the minimum possible resistance and electromigration requirements.

The RF choke at microwave frequencies is generally realized by using a high-impedance λ/4 line, also known as a shunt stub terminated by an RF bypass capacitor CB as shown in Figure 3.24a. A DC block can be either a capacitor or a 3-dB backward-wave coupler. For low RF leakage through the biasing network, the impedance ratio of the shunt stub (Z_S) and the

through line impedance (Z_0), Z_S/Z_0, must be much greater than unity. The low–high impedance lines serve as a lowpass filter, which prevents the microwave signal leaking into the bias port. In this case, the bandwidth increases when the impedance of the stub increases. For VSWR ≤ 1.05, the bandwidth for $Z_S = 100\Omega$ is about 12%. In order to further increase the bandwidth, two sections of quarter-wave long transmission lines are used. If an open circuit is required across the main line for RF signals, a quarter-wave high-impedance line followed by an open circuited quarter-wave low-impedance line are connected. The configuration is shown in Figure 3.24b.

Commonly, the low-impedance line section is replaced with a radial line section as shown in Figure 3.24c. This arrangement provides better bandwidth than a λ/4 open circuited line section and is smaller in size.

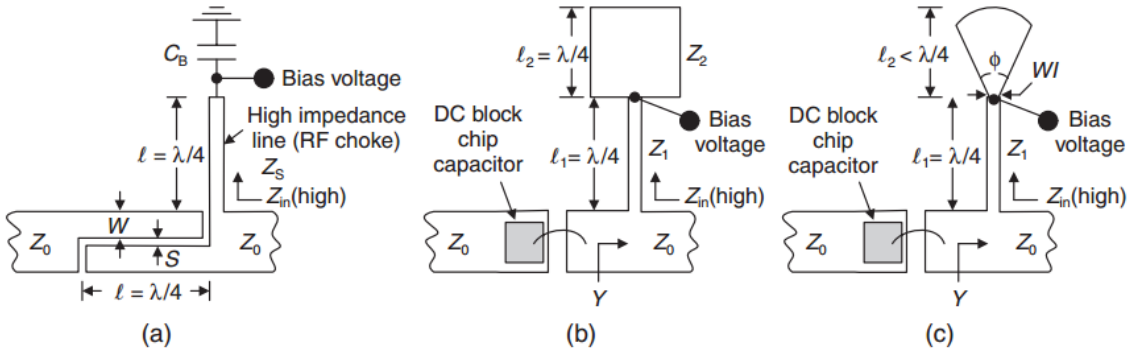


Figure 3.24 – Simplified microwave biasing circuits: (a) coupled-line DC block and λ/4 transformer, (b) MIM capacitor DC block and two λ/4 transformers, and (c) MIM capacitor DC block and a λ/4 transformer in series with a radial line stub.

First, to try with a simpler design we chose the second configuration, we put two impedance inverters (λ/4 long) as we can see in Figure 3.25.

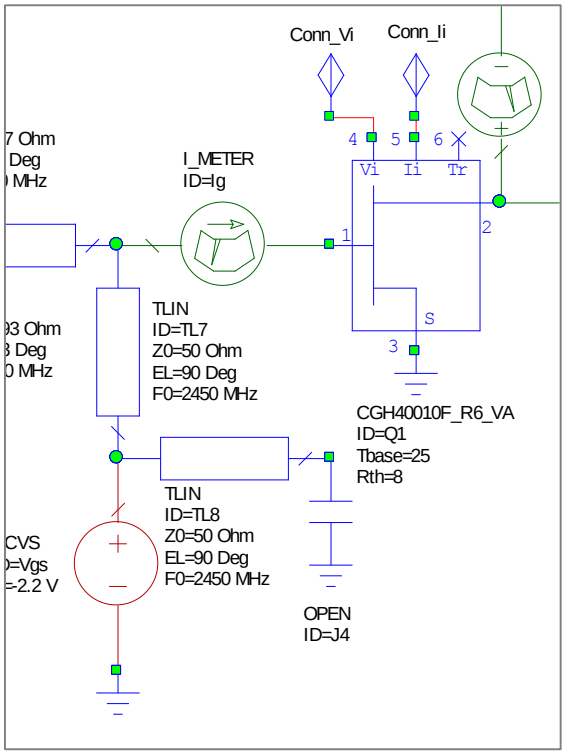


Figure 3.25 – First biasing scheme chosen.

In the end we had the design with ideal transmission lines shown in Figure 3.27 and the results shown in Figure 3.26.

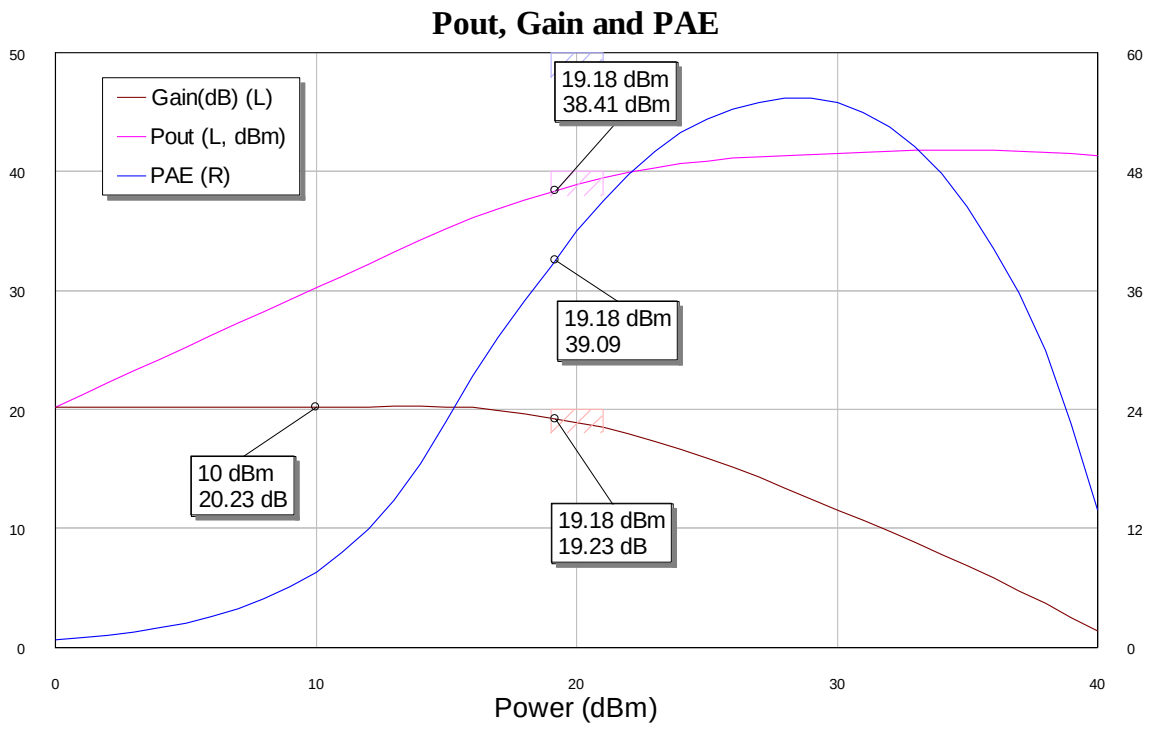


Figure 3.26 – P_{out}, Gain and PAE obtained with ideal design.

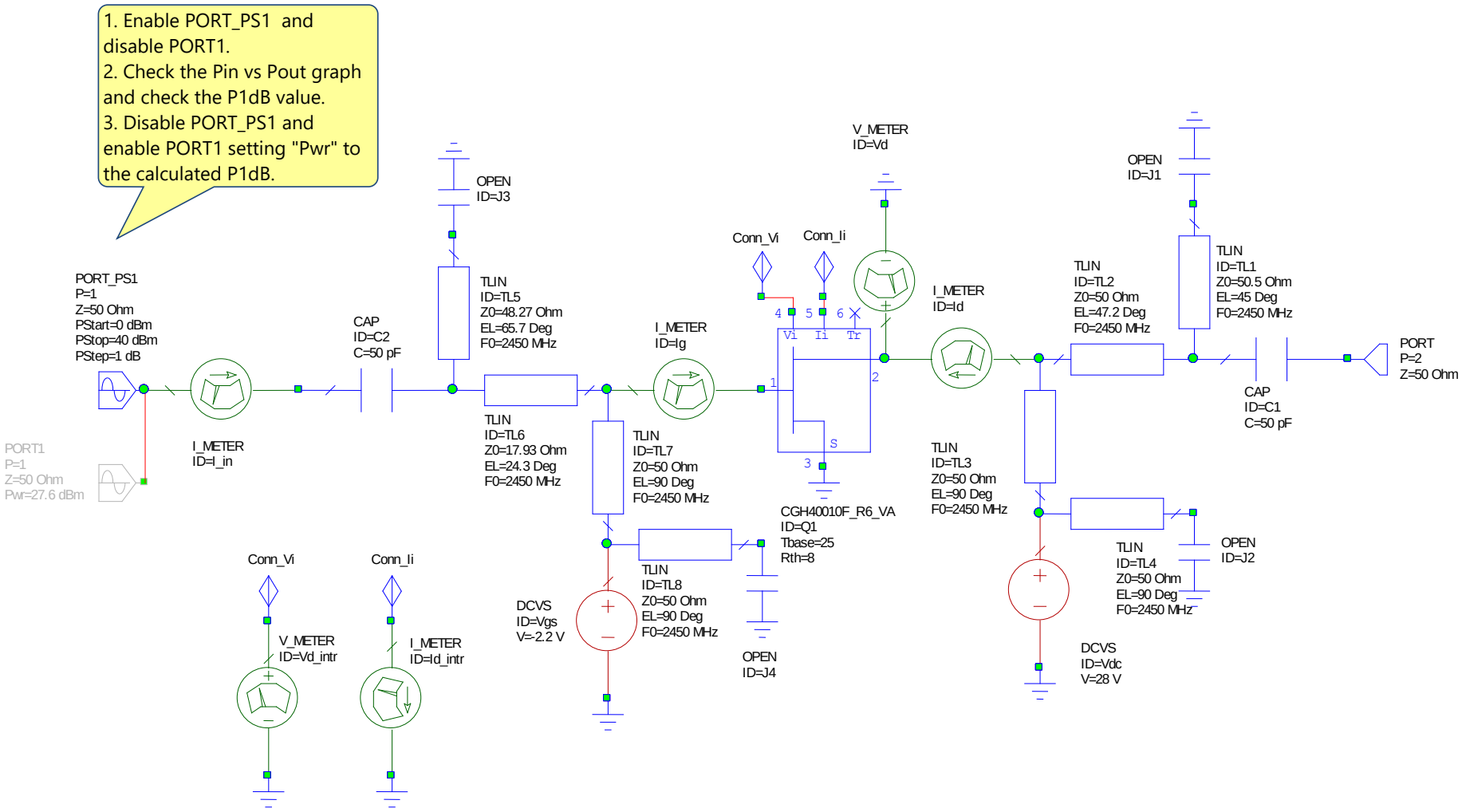


Figure 3.27 – Final design with ideal transmission lines.

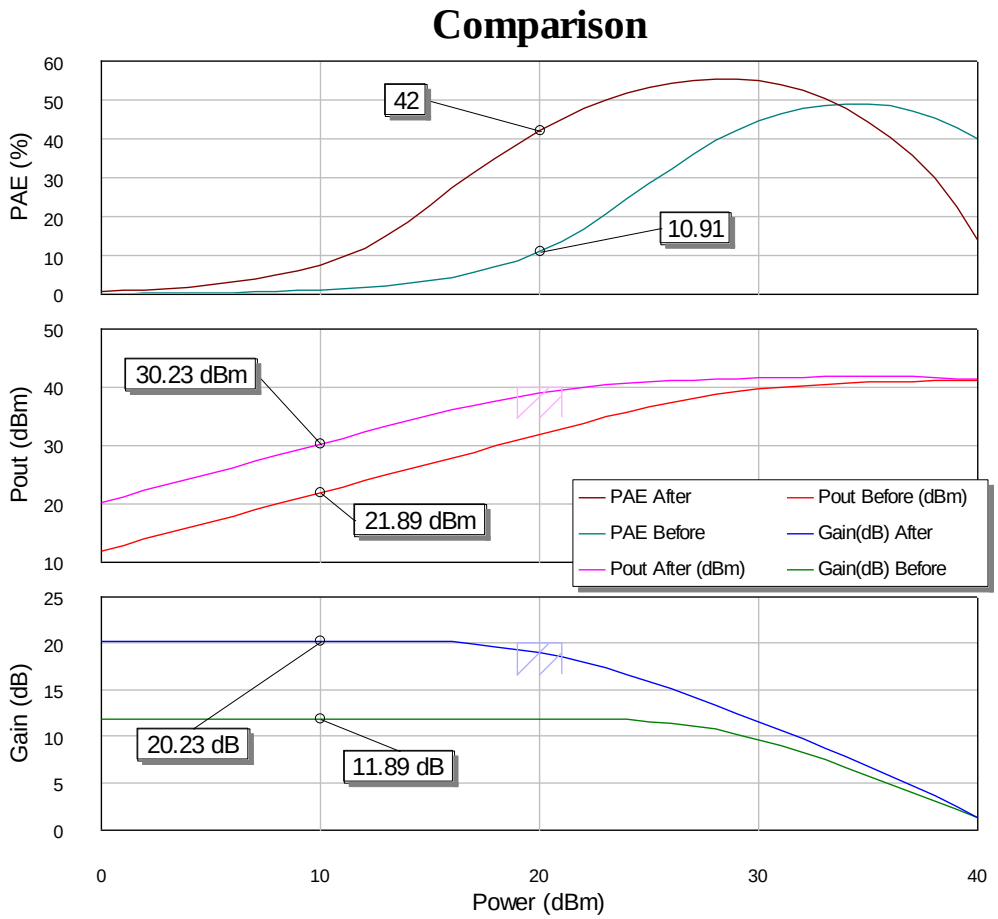


Figure 3.27 – Comparison between ideal design and transistor.

As we can see in Figure 3.27, we have improved the performance of our amplifier with this final configuration. Now we just need 19.18dBm of input power to be at P_{1dB}, this means that with much less power we reach approximately 40dBm in the output. In the gain graph we see an improvement of approximately 10dB which is really good.

Now the main problem that we have are the obtained S-Parameters

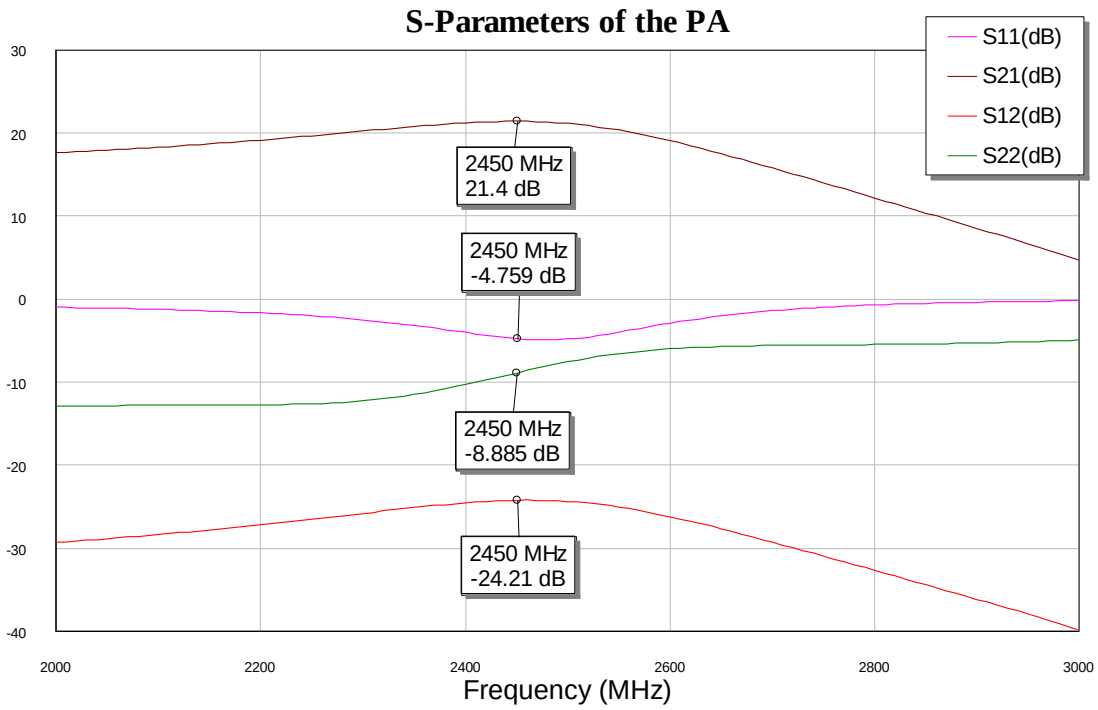


Figure 3.28 – S-Parameters of the ideal design.

As we can see in Figure 3.28 the return losses (S_{11}) are really bad. The reason of this behaviour is that we need to improve the matching. Adding resistance at the gate (Figure 3.29) we improve this matching (Figure 3.30) and stability (Figure 3.31) as well. The value taken for the resistor was obtained using the optimizer.

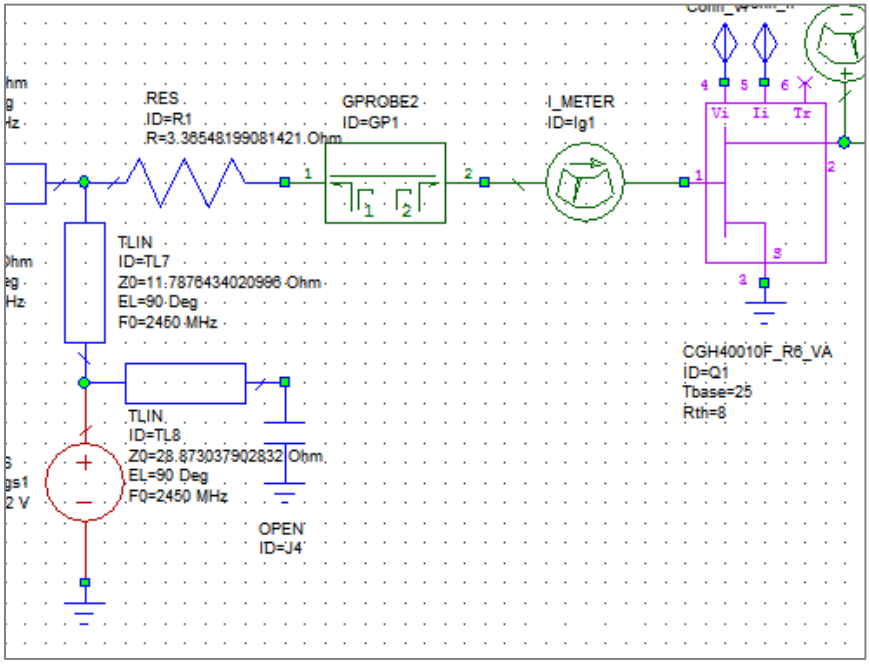


Figure 3.29 – Resistor added to the gate.

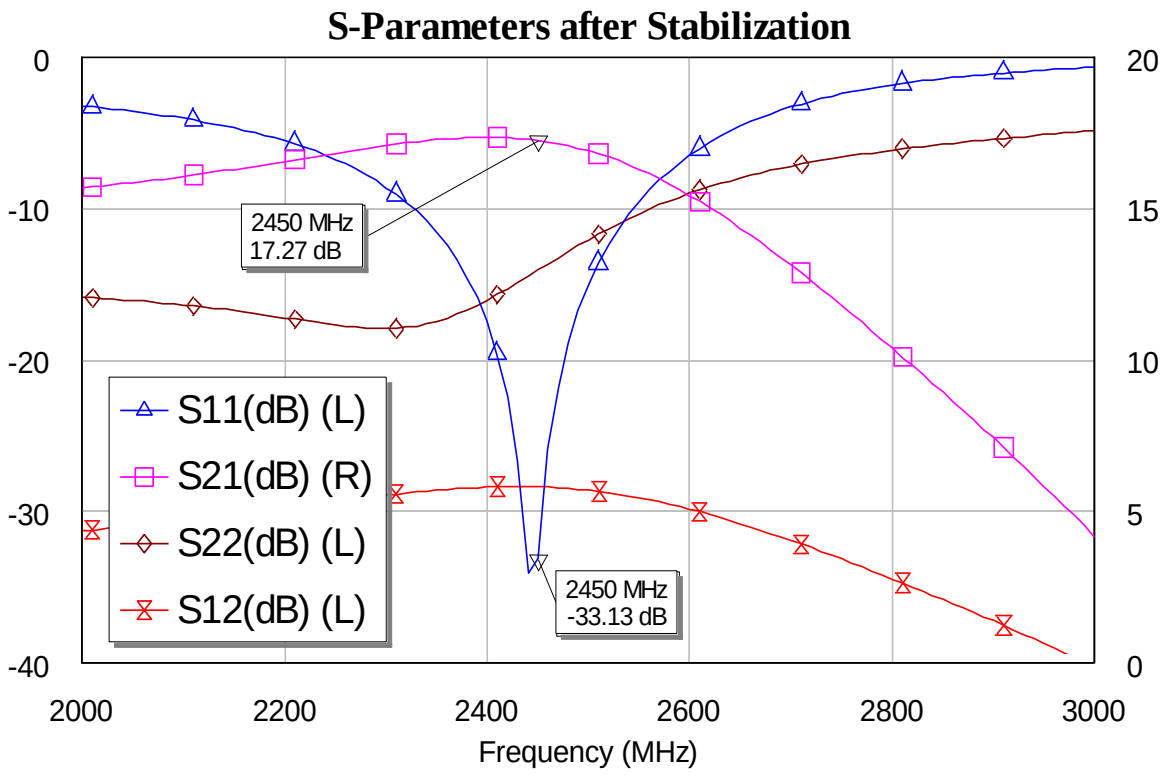


Figure 3.30 – S-Parameters improved with gate resistor.

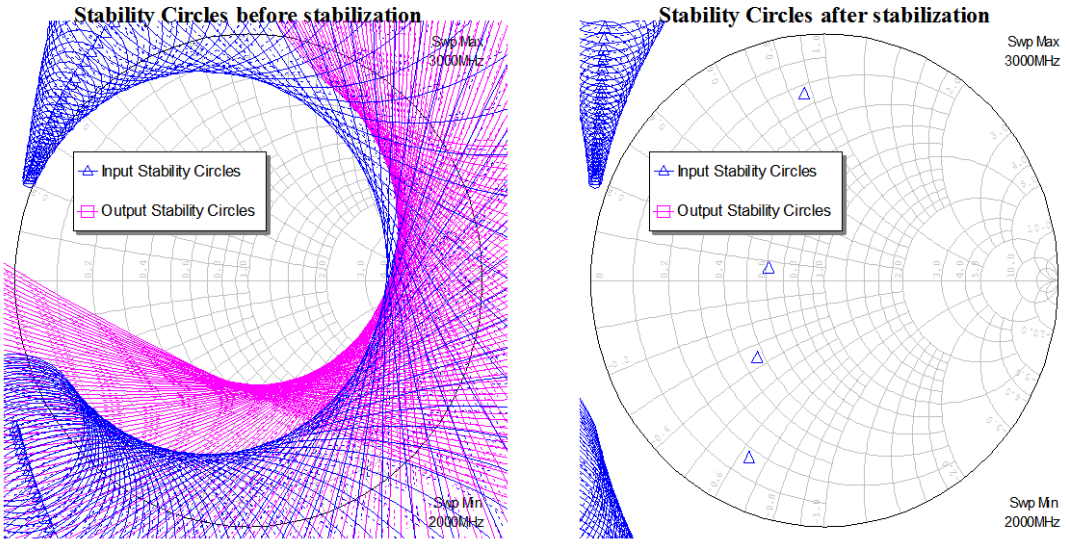


Figure 3.31 – Stability circles from 2GHz to 3GHz before (left) and after (right) putting the gate resistor.

3.12. Real design

After having the first design ready to be built we obviously have to translate all the ideal components into reallistic ones which involve losses.

Substrate selection

Power Amplifiers depend on the characteristics of their active devices , but they also depend a great deal on the behavior and performance of their printed-circuit-board (PCB) materials for such functions as minimizing loss, maximizing gain and efficiently dissipating heat. To make a suitable choice for a PA application can require careful comparison of some key PCB material properties, including the relative permitivity (or dielectric constant, ε_r), the dissipation factor (tanδ), the thermal conductivity, temperature coefficient of dielectric constant (TCDk), copper surface roughness, tolerance of ε_r and even the tolerance of the PCB material's thickness [18].

Although designers may often assume that circuit material ε_r tolerance is the most critical material parameter for achieving good impedance control, this is typically not the case. In fact, the ε_r tolerance will generally be fairly tight and one of the lesser concerns in therms of impedance control. To go further in this topic take a look at [18].

Considering the above we started the process of looking for a real substrate suitable for our design. The most popular brands in this field are Rogers Corporation and Taconic. The most suitable substrates for Power Amplifiers for each brand are RF-35 (Taconic) and RO4350B-LoPro (Rogers) due to the following characteristics:

- These materials are reinforced hydrocarbon/ceramic laminates – not PTFE
- Low dielectric tolerance and low loss
- Stable electrical properties vs. frequency
- Low thermal coefficient of dielectric constant
- CAF resistant

We finally decided to choose the one from Rogers because of its University program to get free substrate samples. To be accurate we chose the model RO4350B-LoPro (20 mils thickness) [19]. We took this thickness because the lower thickness the better thermal conductivity which is a factor to consider in Power Amplifiers design.

Real transmission lines, new biasing and matching circuit configuration and optimization

After having selected the proper substrate for our design, we must include the element *MSUB* in AWR and configure it with the specifications give in the manufacturer´s datasheet.

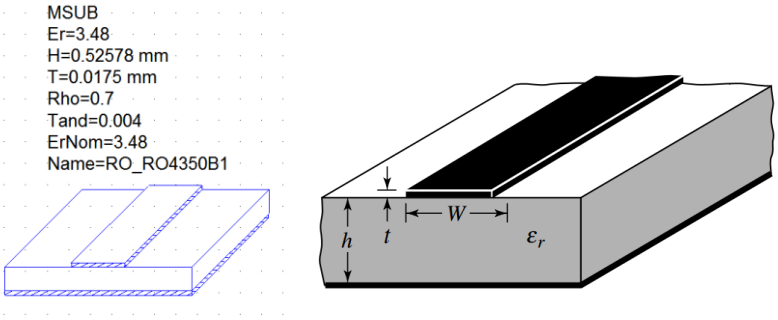


Figure 3.32 – *MSUB* element (left) and microstrip parameters (right).

After that, we changed the ideal transmission lines (*TLIN*) by the lossy ones (*MLIN*) and decided to change the bias configuration due to the bad response with real lines. So as we explained before, the configuration in Figure 3.24c is better in order to improve the bandwidth. It is composed by a radial stub whose function is the same as an inductor, it rejects the high frequencies making them to see an open circuit looking into the bias network.

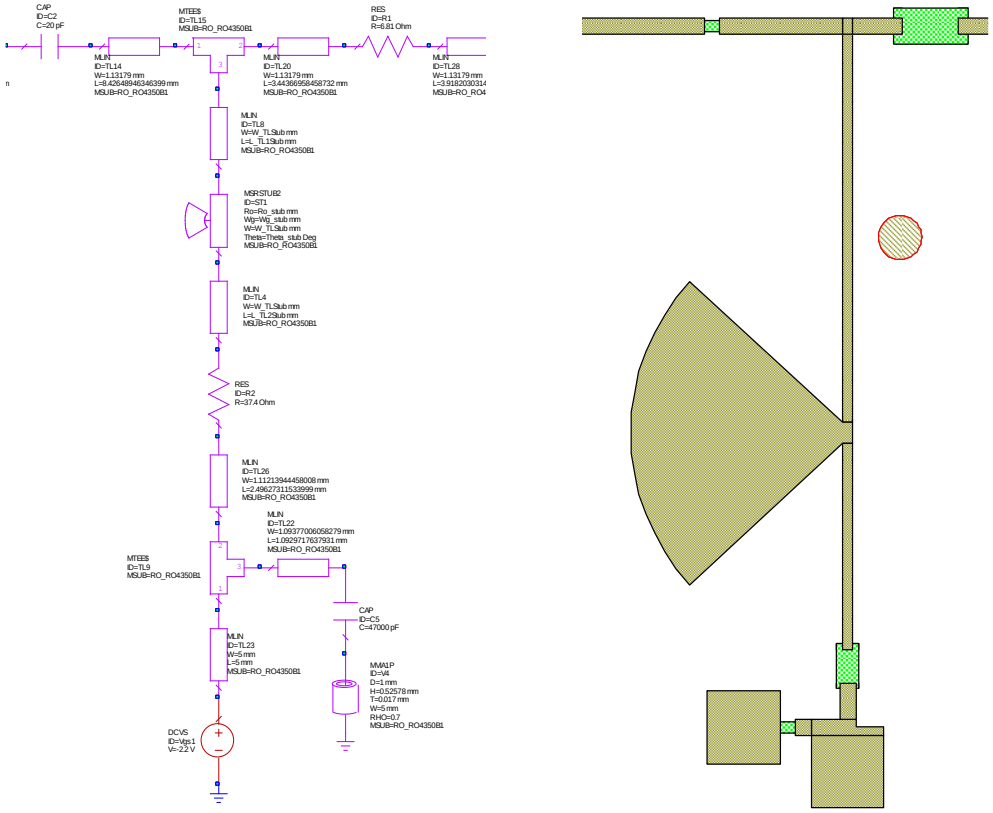


Figure 3.33 – Real Bias Network Schematic (left) and its layout (right).

Apart from the RF choke we use a resistor between it and the supply (Figure 3.33). Its function is to stabilize the low frequencies [15].

Outside our bandwidth there will be some frequencies that does not see a high impedance through the bias network, so it is important to use a decoupling capacitor in order to short this unwanted RF.

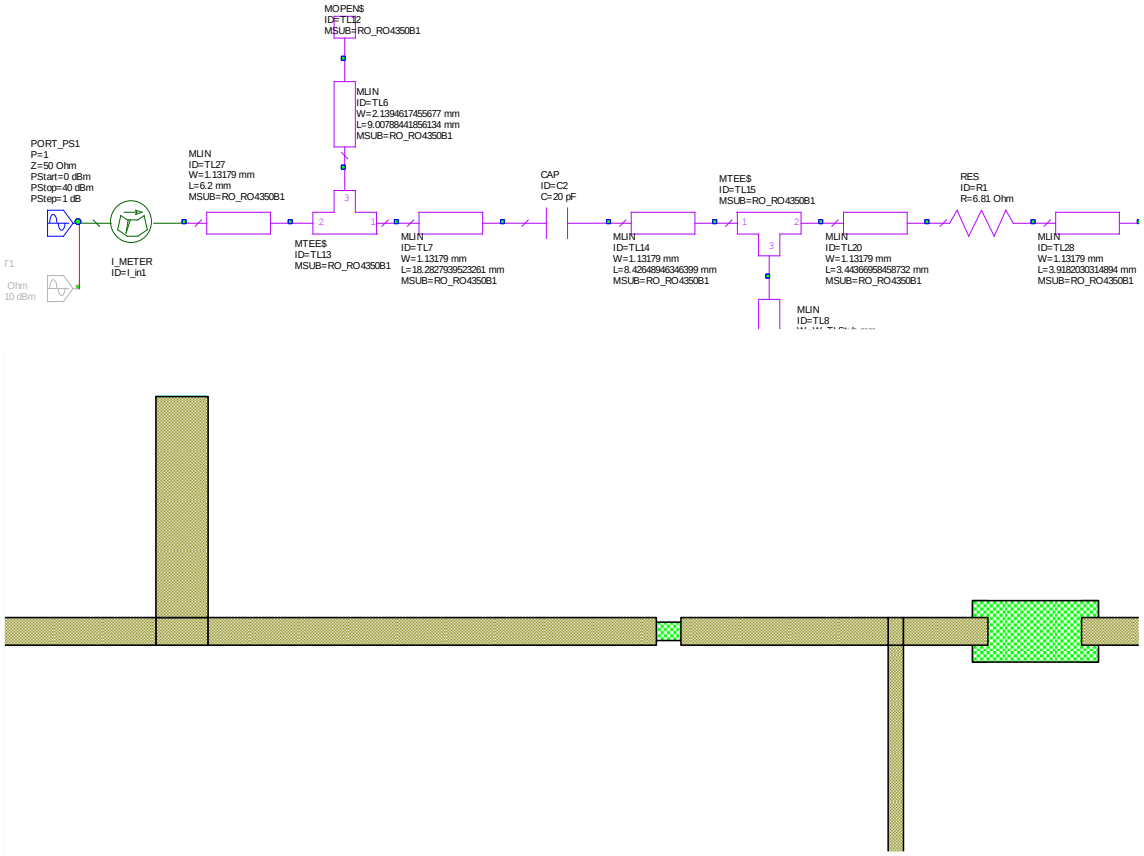


Figure 3.34 – Final Input Matching Network.

As we can see in Figure 3.34 we used as input matching network an open circuited stub and some transmission lines with the same width (50 Ω).

In Figure 3.35 we used an open–circuit double–stub in addition with an open circuited stub. In both matching networks we put the blocking capacitors in the middle just because during the optimization process gave us better results.

The process of optimization was set to obtain the best results taking into account the return losses, gain and stability.

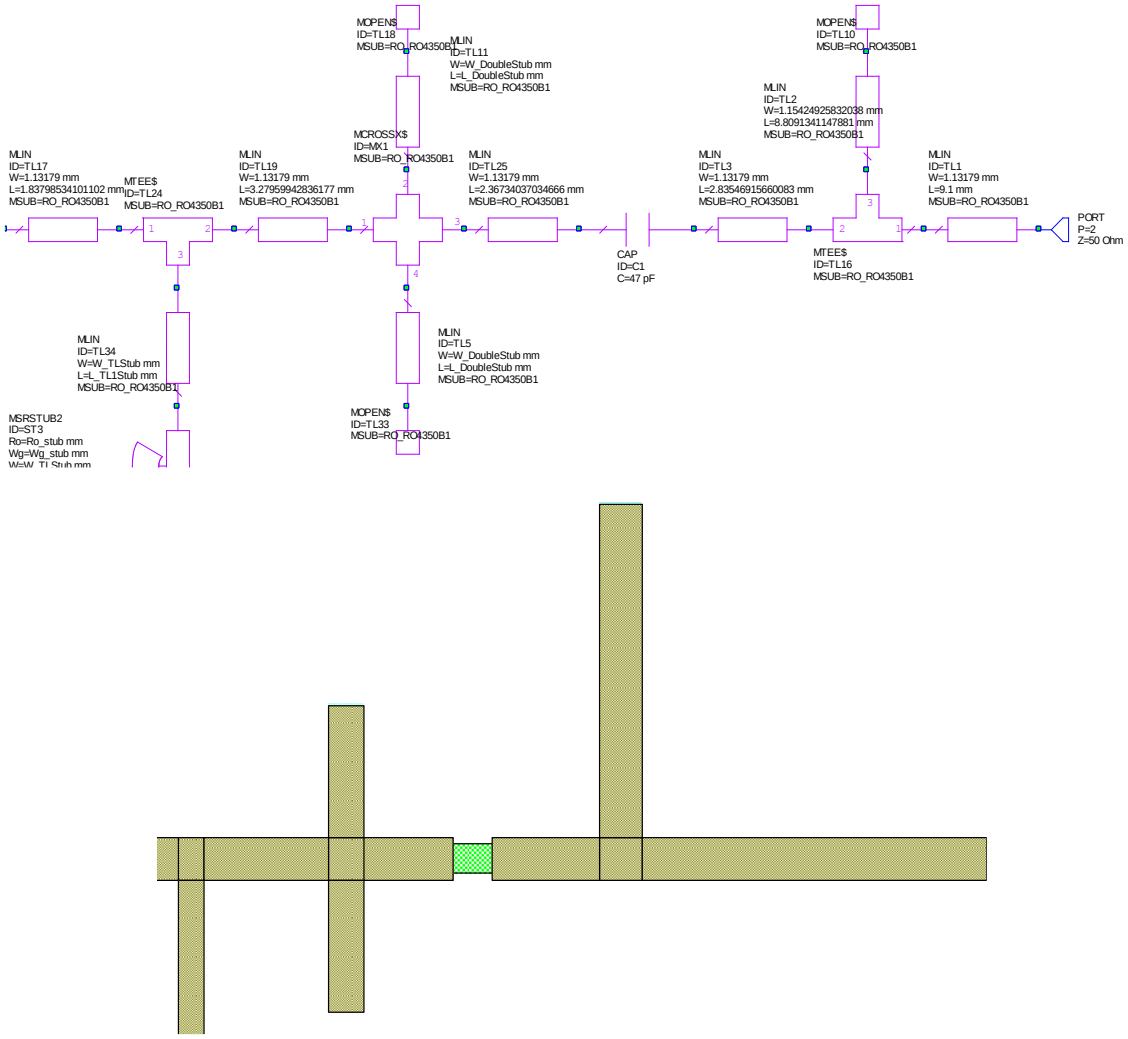


Figure 3.35 – Final Output Matching Network.

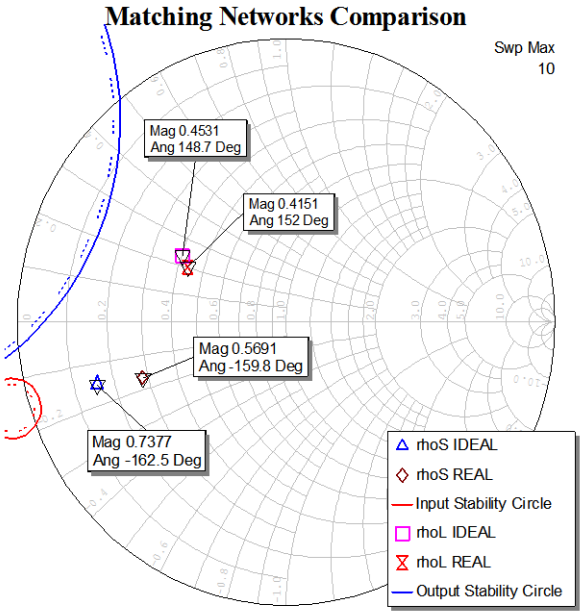


Figure 3.36 – Lossy Matching Networks Vs. Ideal Matching Networks.

To have an idea how different are the ideal matching networks with the new ones we made a plot in a Smith Chart to compare the reflection coefficients as shown in Figure 3.36. It can be seen that they are very close.

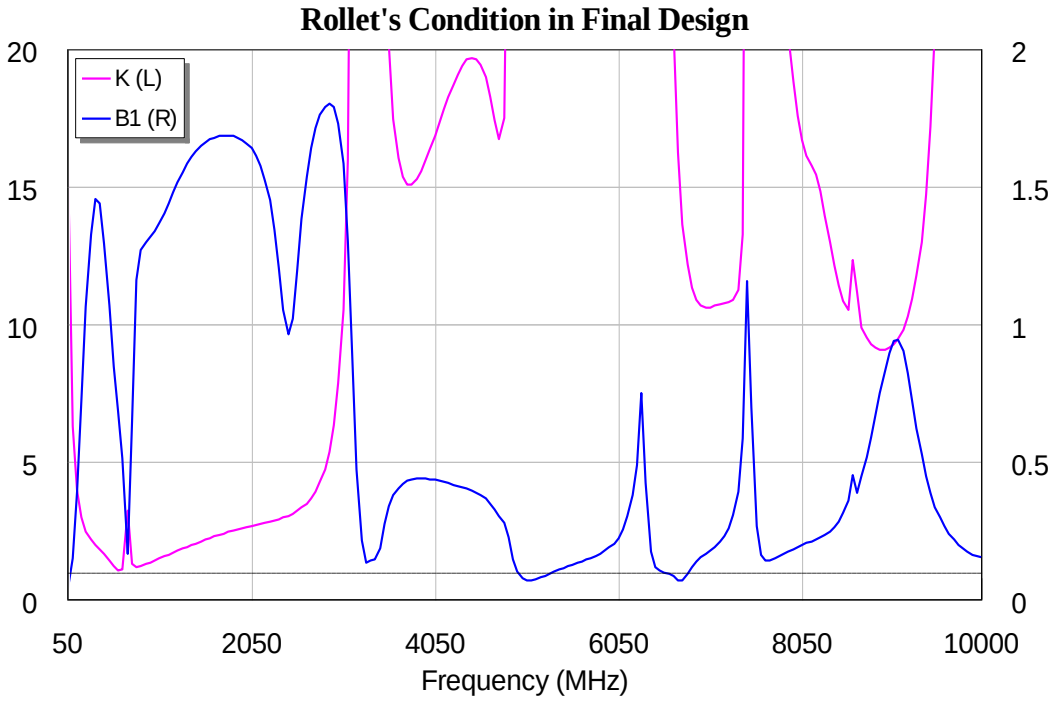


Figure 3.37 – Final design stability test.

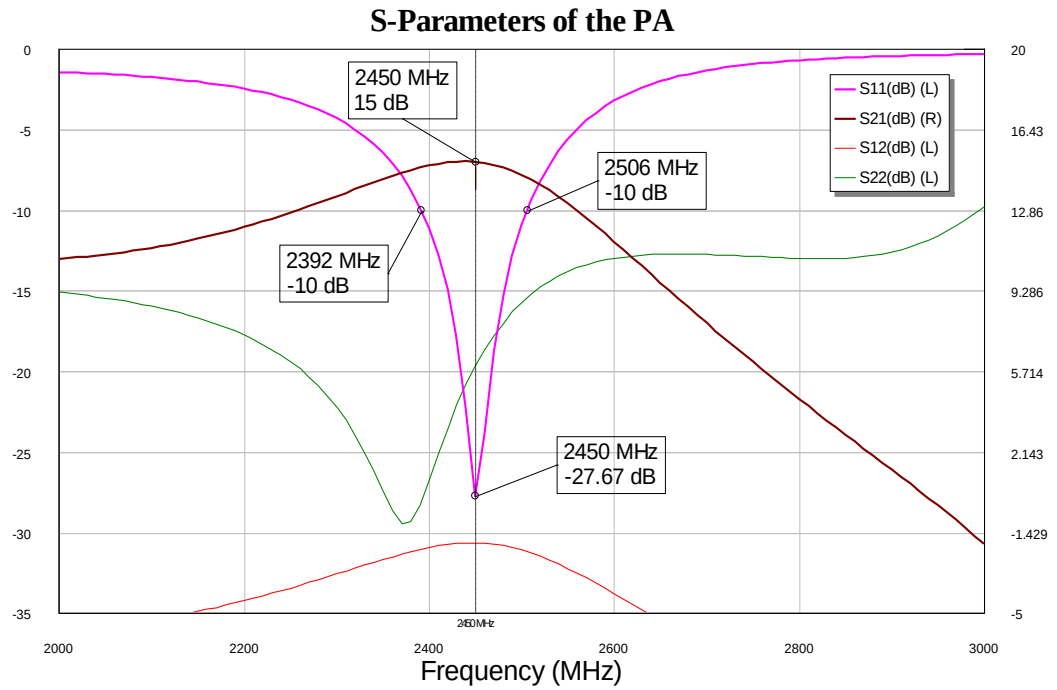


Figure 3.38 – Final design S-Parameters.

The unconditional stability was checked over a wide range of frequencies with successful results as shown in Figure 3.37.

Moreover, the S-Parameters in Figure 3.38 let us see that we reach 15dB gain at f_0 and about 100MHz bandwidth at 10dB.

Finally, we compared the PAE, Pout and Gain. Thus, as we can see in Figure 3.39, the final design improves the transistor by 3dB approximately.

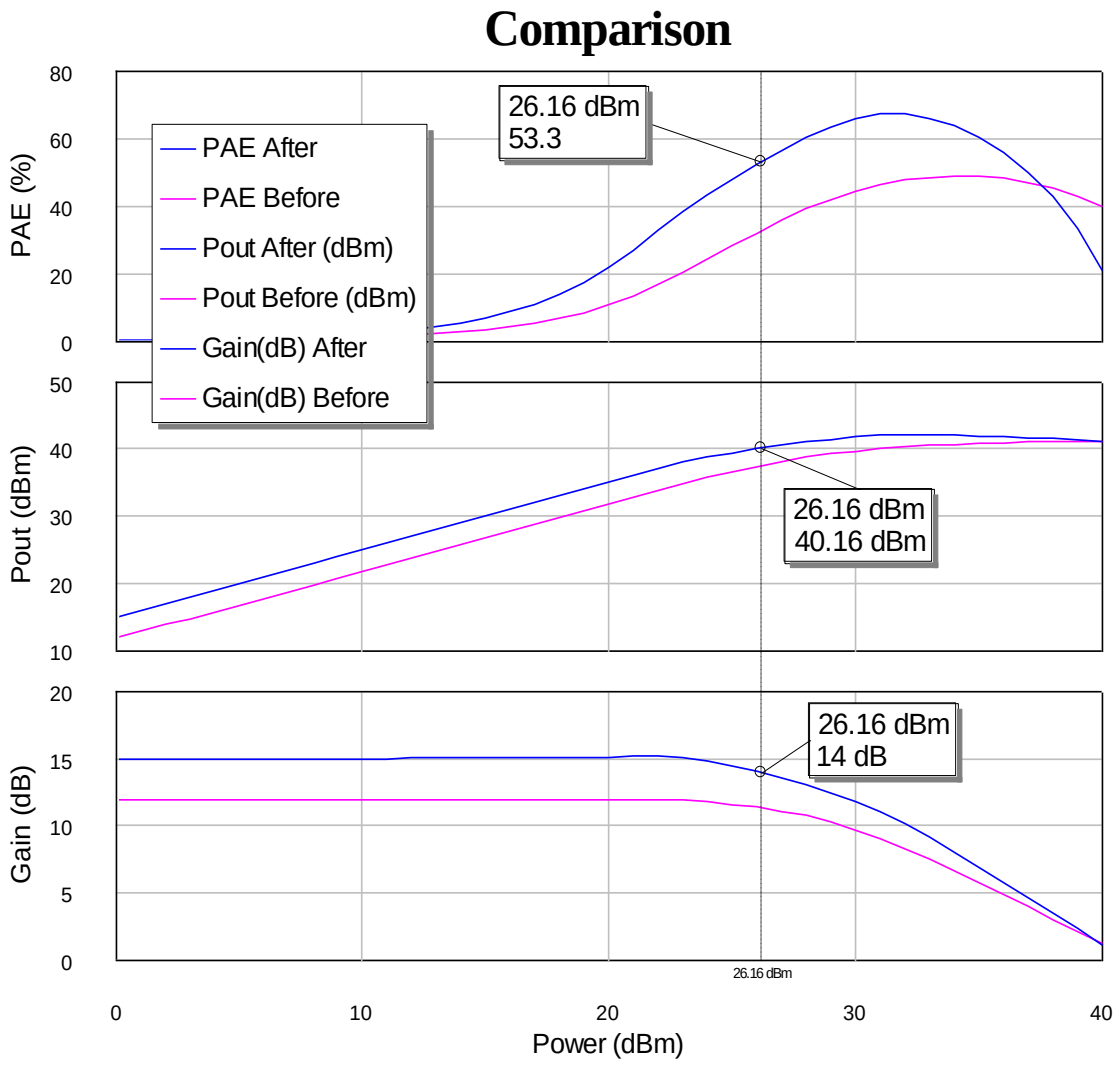


Figure 3.39 – Final comparison – with and without matching and bias networks.

Before we start working on the manufacturing process is important to make a final simulation to take into account about coupling losses and other electromagnetic phenomena that the normal analysis made by AWR does not consider.

EM simulation

MLIN elements used in this design are closed-form models that have limited accuracy. To be sure that we are ready to manufacture our prototype, it is recommended to use EM extraction to EM simulate the board. This is an automated process to generate an EM document based on layout. All MLIN elements that are included in extraction are replaced by EM-simulated data [20].

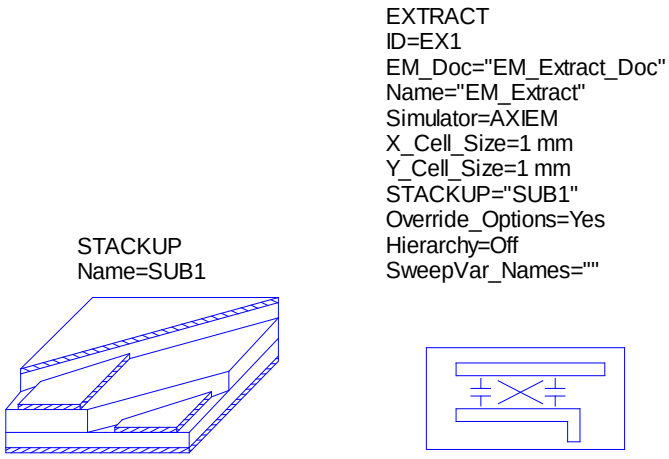


Figure 3.40 – STACKUP and EXTRACT blocks. Forced use in order to perform EM simulation.

Steps to do an EM simulation:

1. Check that the layout is ok.

2. Add STACKUP and EXTRACT blocks (Figure 3.40). There is a script for this. Scripts > EM > Create Stackup.

3. Include all MLIN elements MRSTUBs, MTEEs and such in extraction. Double-click each element to open Element Options and open Model Options. Enable EM extraction. All other elements like transistors, capacitors and resistors are excluded.

The layout shapes and vias should be added to extraction too. Right-click shapes and vias in layout and select Shape Properties. They have an option to include them in extraction.

4. Click EXTRACT block in schematic. All elements included in extraction are highlighted.

5. Set the EM frequencies. Double-click EXTRACT block and open frequencies tab. The frequencies should include DC, project frequencies and their harmonics (the first fives).

6. Increase max AFS points from 40 to at least 120. For that right-click in EXTRACT block. Go to AXIEM tab and click on Show Secondary. Change the 'Max # of sim points' value to 120.

7. Change Explicit_Ground to 'Auto Port' in EXTRACT block parameters. Group de-embedding is used automatically now if needed.

8. Right-click in EXTRACT block and select Add Extraction. This generates the EM document.

After that, when we re-simulated it took a lot of time to finish because of the EM based simulation which is so much slower that the closed one, based on circuit analysis. Making now a comparison taking into account this losses, we can appreciate little changes but no very important as shown in Figure 3.41.

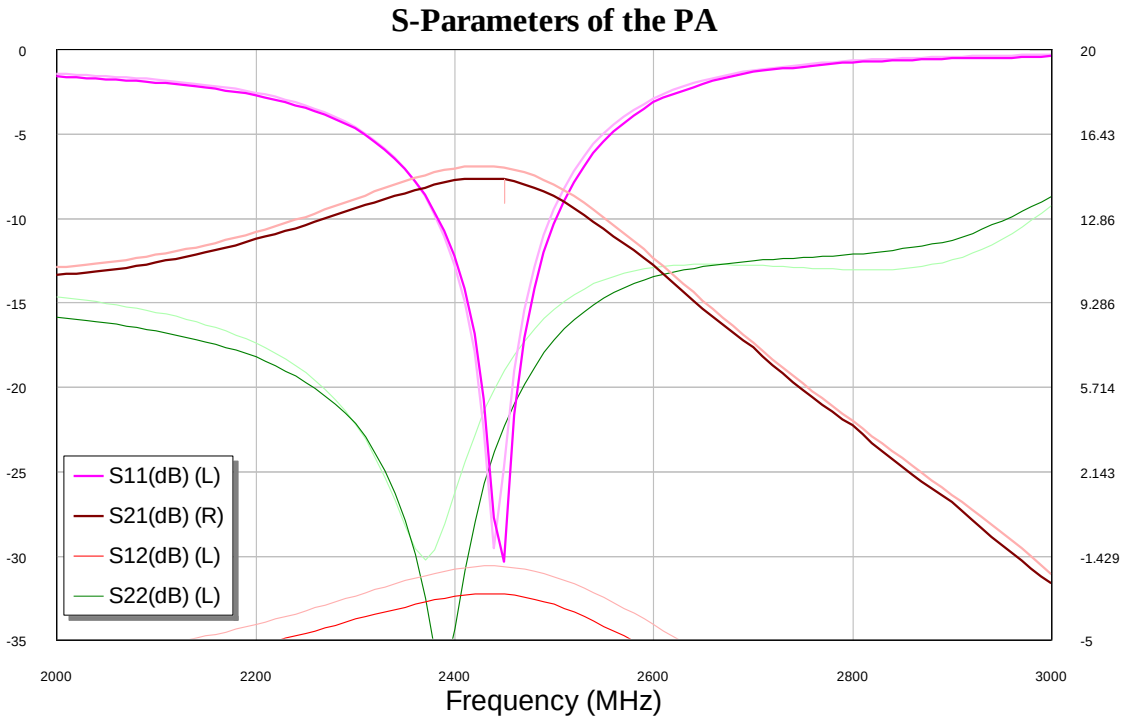


Figure 3.41 – Comparison with and without EM extraction.

Figure 3.42 shows the final layout, ready to start the manufacturing process.

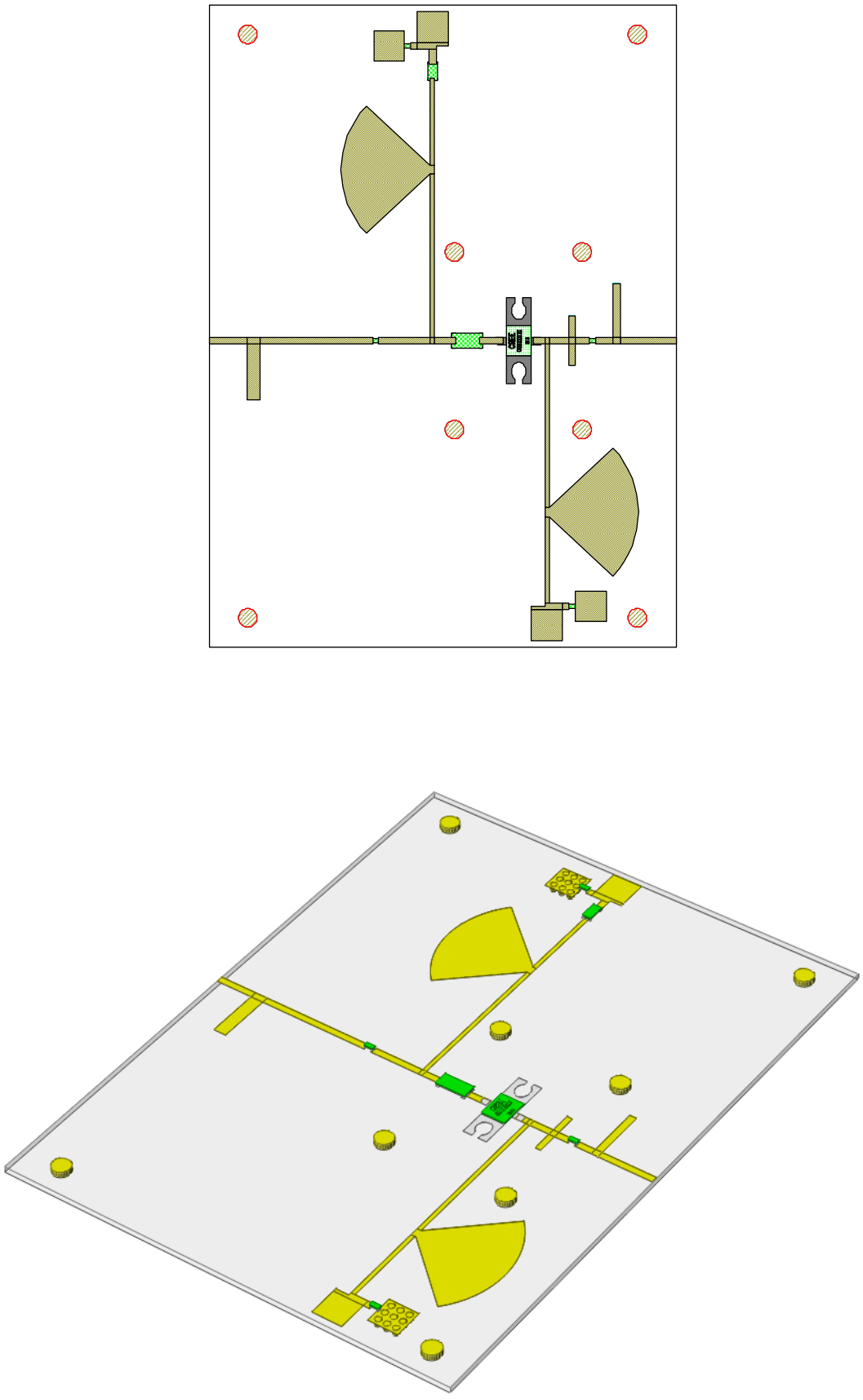


Figure 3.42 – Final layout.

4. Manufacturing and Testing Process

The process of manufacturing a power amplifier having the CAD design is not an easy step. There are various things to consider, such as, a heat sink selection, transistor grounding and machining or subtractive manufacturing method.

4.1. Heat sink considerations

Power transistors handle large currents and high voltages, hence, they produce high amounts of power. One part of that power is used to amplify the signal and the other is wasted in heat known as power dissipation. Such power must be carefully handled in a way that the power transistor must be able to dissipate its associated heat very quickly so it do no overheat. As most heat is generated at the drain/gate junction, the area of this junction is made as large as possible.

The maximum power rating of a transistor is largely governed by the temperature of the drain/gate junction. If too much power is dissipated, this junction gets too hot and the transistor will be destroyed. Hence, the performance of a power amplifier is closely dependant on its ability to dissipate the heat generated.

Minimising the problem of heat is approached in two main ways:

1. By operating the transistor in the most efficient way possible, that is by choosing a class of biasing that gives high efficiency and is least wasteful of power. In our case, because we are working at class A, we know that this is an important handicap, so we will have to be focused in improving the second way.
2. By ensuring that the heat produced by the transistor can be removed and effectively transferred to the surrounding air as quickly as possible.

This last method, highlights the importance of the relationship between a power transistor and its heat sink, a device attached to the transistor for the purpose of removing heat. The physical construction of power amplifiers is therefore designed to maximise the transfer of heat to the heat sink.

Good physical contact between the transistor and heat sink is essential, and a heat transmitting grease is smeared on the contact area before clamping the transistor to the heat sink [21].

In selecting a heat sink to achieve to maintain the transistor temperature below its maximum allowed, four fundamental parameters must be known about the application:

- The amount of heat, *Q*, being generated by the transistor in watts (W).
- The maximum allowable junction temperature, T_j, of the device in ºC.
- The maximum temperature of the ambient cooling air, T_a, in ºC.
- The type of convection cooling in the area of the device: natural or forced. If it is forced convection (fan), the air flow velocity, in linear feet per minute (LFM), must be known.

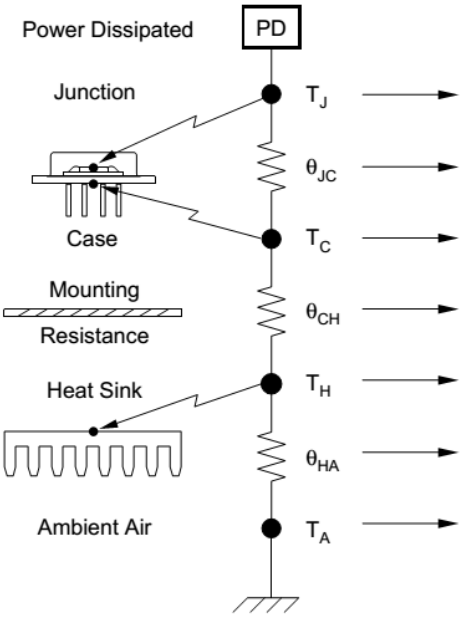
Basic Formulas

Heat will flow from the device to the ambient air through many paths, each of which represents resistance to the heat flow. This resistance is called thermal resistance, denoted as θ in °C/W, and is defined as the ratio between the amount of total heat being transferred and the temperature difference that drives the heat flow. The total thermal resistance of a system for a given device can therefore be expressed as:

$$\theta_{ja} = \frac{T_j - T_a}{Q}$$

where θ is the thermal resistance in degrees C per watt, and where *ja* represents *junction-to-ambient*. A low thermal resistance represents better performance than a high thermal resistance.

Heat sinks lower the overall junction to ambient thermal resistance. The actual thermal path runs through the heat sink when it is mounted on the device by means of an attachment mechanism. In this case, the total thermal resistance, θ_{ja}, is the sum of all the individual resistances which represent the physical aspect of the thermal path (see Figure 4.1) [22].



UNITS	HIGH POWER APPLICATION		LOW POWER APPLICATION	
Watts	100W	10W	10W	1W
°C	145°C	37°C *	158°C *	39°C
°C/Watt	0.8	0.8	0.8	0.8
°C	65°C	29°C	150°C	38°C
°C/Watt	0.1	0.1	0.5	0.5
°C	55°C	28°C	145°C	37°C
°C/Watt	0.3	0.3	12	12
°C	25°C	25°C	25°C	25°C

* Note, the difference in junction temperature that thermal resistance can make even when operating at the same power level.

Figure 4.1 – The complete heat path from junction to ambient with typical values [23].

There are three thermal resistances that are commonly used to express the total resistance:

1. The junction-to-case resistance, θ_{jc}, to account for the thermal path across the internal structure of the device.
2. The case-to-sink resistance, θ_{cs} (or θ_{ch}), which is also called the interface resistance, to account for the path across the interface between the device and the heat sink.
3. The sink-to-ambient resistance, θ_{sa} (or θ_{ha}), to account for the thermal path between the base of the heat sink to the ambient air. It follows that

$$\theta_{ja} = \theta_{jc} + \theta_{cs} + \theta_{sa}$$

Realistically, a typical thermal designer has no access to the internal structure of the device, and can only control two resistances outside of the device, θ_{cs} and θ_{sa}. Therefore, for a device with a known θ_{jc} obtained from the device manufacturer's data book, θ_{cs} and θ_{sa} become the main design variables in selecting a heat sink. Thermal interface between the case and the heat sink is controlled in a variety of manners with different heat conducting materials. The interface resistance between the case and the heat sink is dependent on four variables: the thermal resistivity of the interface material (ρ°C,W-inch), the average material thickness (t, inches), the area of the thermal contact footprint (A, $inch^2$), and the ability to replace voids

due to finish or flatness (sink or chip) with a better conductor than air. The interface thermal resistance is then expressed as:

$$\theta_{cs} = \frac{\rho \cdot t}{A}$$

Once the θ_{cs} is calculated, the required thermal resistance from the sink to ambient (θ_{sa}) is easily calculated by the following equation:

$$\theta_{sa} = \frac{T_j - T_a}{Q} - (\theta_{\mathrm{jc}} + \theta_{cs})$$

Therefore any heat sink with a thermal resistance lower or equal to the calculated value should be ok, but to avoid continually running the transistor close to the maximum permitted temperature, which is almost guaranteed to shorten the life of the transistor, it is advisable to use a heat sink with a lower thermal resistance where possible.

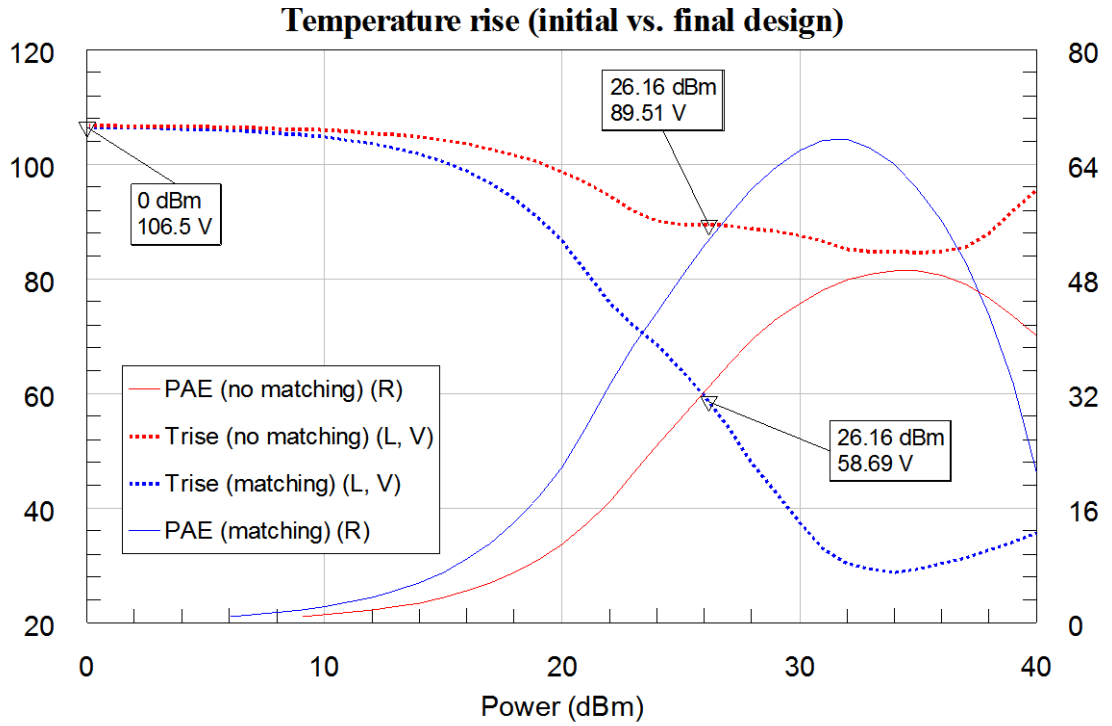


Figure 4.2 – Junction temperature above the ambient.

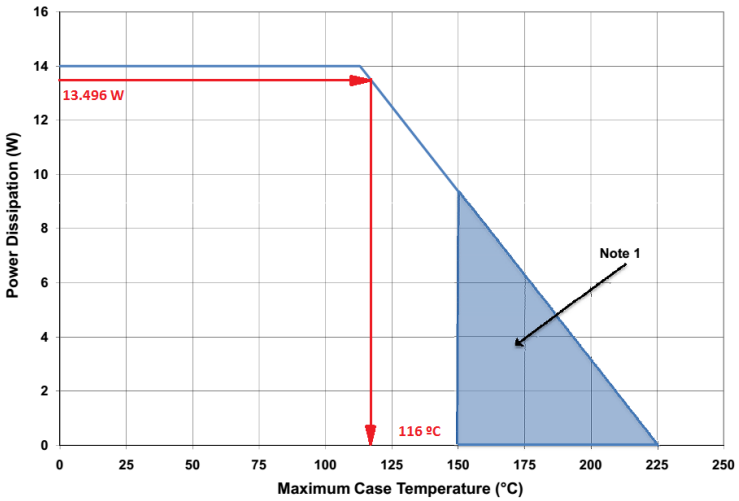
In Figure 4.2 it is shown the temperature rise at the junction which has the highest value

$$106.5 + 25 = 131.5\ ^{\circ}C$$

with low input power. This has a very simple explanation: if you do not introduce any RF to amplify, all the DC power supplied to do so is wasted in dissipated heat. Hence, the higher input RF power the higher PAE and consequently the lower temperature at the junction.

As we said in the previous chapter, our Q-Point was such that we had the following DC power:

$$P_{DC} = I_{DQ} \cdot V_{DS} = 0.482 \cdot 28 = 13.496\ W$$



Note 1. Area exceeds Maximum Case Operating Temperature

Figure 4.3 – CGH40010 Power Dissipation De-rating Curve.

Looking at Figure 4.4 we can see that when dissipating all the DC power (worst case), the power transistor will be able to withstand as maximum 116 ºC at the case, being the maximum allowed in the junction, 225 ºC. Hence,

$$\theta_{ja} = \frac{T_j - T_a}{P_D} = \frac{225 - 25}{13.496} = 14.8192\ ^{o}C/W$$

This value is our top limit. We must not surpass it.

$$\theta_{jc} = 8.0\ ^{o}C/W$$

The typical value for θ_{cs} using silicon grease is about 0.5 ºC/W [23][24].

So, we will have to look for a heat sink with θ_{sa} less than

$$\theta_{saMax} = \theta_{ja} - (\theta_{jc} + \theta_{cs}) = 14.8192 - 8.5 = 6.31921\ ^{o}C/W$$

Looking for a heat sink in the *Wakefield-Vette* catalogue we found the model 641k. That model has the natural and forced convection characteristics shown in Figure 4.4.

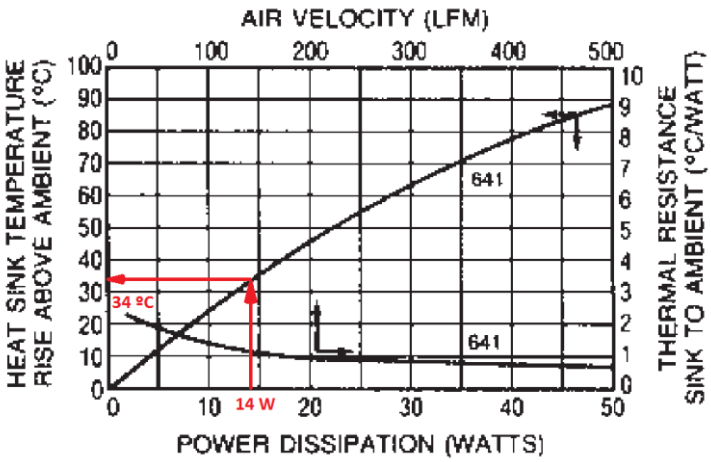


Figure 4.4 – Chosen Heat Sink natural and forced convection characteristics.

Considering that we dissipate about 14 Watts, we have a rise temperature above ambient about 34 ºC approximately. Hence,

$$\theta_{sa\ (641k)} = \frac{34\ ºC}{14\ W} \simeq 2.43\ ºC/W$$

So the new θ_{ja} value would be

$$\theta_{ja\ (641k)} = \theta_{jc} + \theta_{cs} + \theta_{sa\ (641k)} = 8 + 0.5 + 2.43 = 10.93\ ºC/W$$

Having in worst case

$$T_{j\ (641k)} = \theta_{ja\ (641k)} \cdot P_D + T_a = 10.93 \cdot 13.496 + 25 \simeq 172.51\ ºC \quad (max.\ 225\ ºC)$$

$$T_{c\ (641k)} = T_{j\ (641k)} - \theta_{jc} \cdot P_D = 172.51 - 8 \cdot 13.496 \simeq 64.54\ ºC \quad (max.\ 150\ ºC)$$

This value makes valid this heat sink since the temperatures at the worst case are ok.

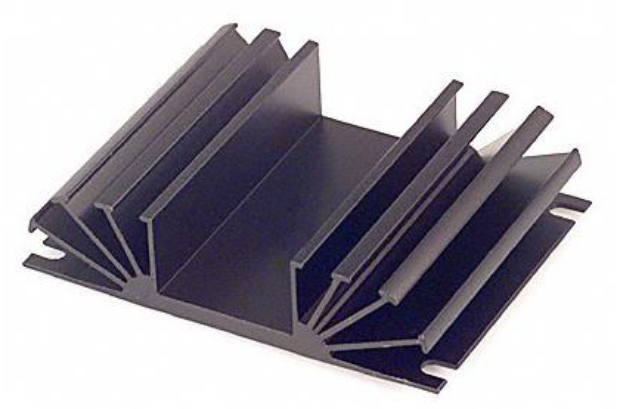


Figure 4.5 – Chosen Heat Sink (641k from *Wakefield-Vette*).

4.2. Transistor grounding and subtractive manufacturing method

Transistor grounding

In the last section we explained how we calculated the total thermal resistance. One of the three, the case-to-sink resistance is the interface material used to make contact between the transistor and the heat sink, in our case, thermal grease. This means that the transistor goes in direct contact with the heat sink. There are two reasons that justify this configuration:

1. Thermal performance. If we don't remove the substrate there, we should have to make a connection with the substrate as interface between the transistor and the heat sink. This is not advisable because the case-to-sink resistance would increase too much increasing the possibility of burning the transistor due overheating.
2. Inductivity reduction. If we decide not to remove the substrate there, we will have to make a lot of vias to avoid inductances generated when grounding the source pin. Is much more suitable to completely remove the substrate in that area and make a good ground.

For these reasons we made a slot in the substrate as shown in red in Figure 4.6 (right).

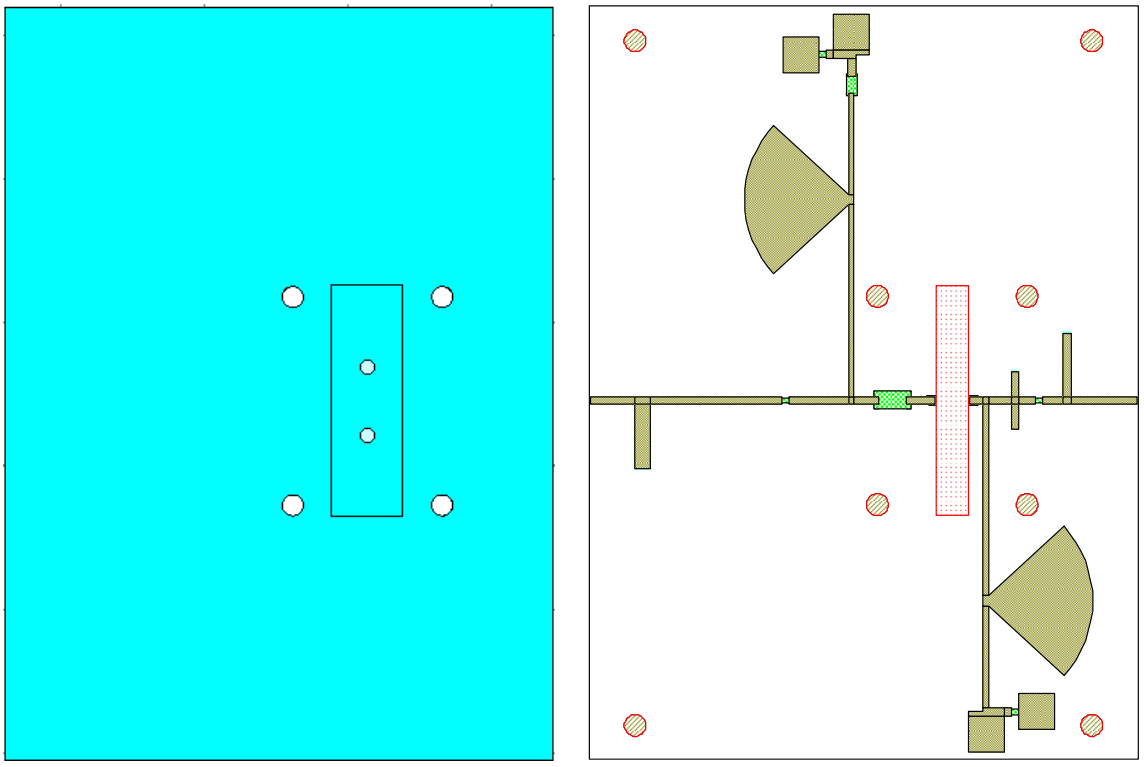


Figure 4.6 – Front view of the heatsink modification (left) and substrate slot in red (right).

Subtractive manufacturing method

Due to the low thickness of the substrate, the process of machining should have been done in chemical milling process because of its high accuracy. This process is an engineering production technique for the manufacture of burr free and stress free flat metal components by selective chemical etching through a photographically produced mask.

Although, because we did not have the needed chemicals, we made the prototype by milling process. This is the machining process of using rotary cutters to remove material from a workpiece advancing (or feeding) in a direction at an angle with the axis of the tool.

In Figure 4.7 it is shown the machine making the shapes of the design.

Figure 4.7 – Starting the milling process with ProtoMat C30s.

During the fabrication process we had to stop the first design and restart again because the low thickness of the substrate made very difficult for the machine to maintain the surface flat. It can be seen in Figure 4.8 the mistake made in the first design because the central part of the substrate was raised in comparison with the external parts due to the substrate flexibility.

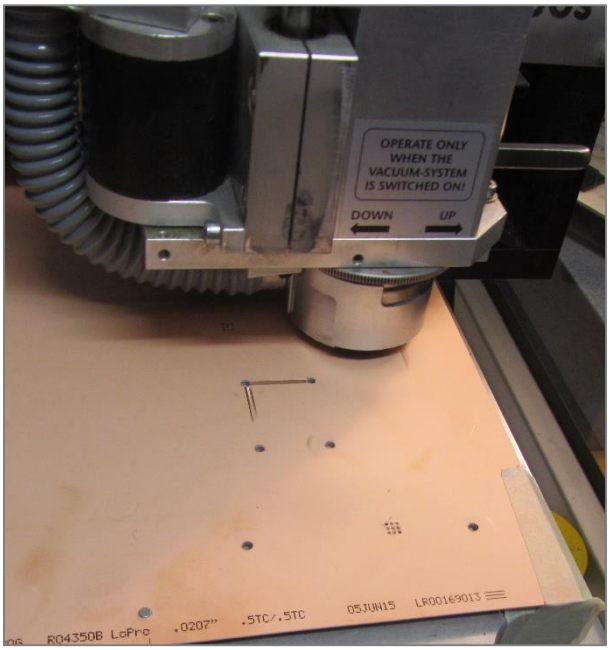


Figure 4.8 – First design attempt failed.

As we can see in Figure 4.9, the finish has not been very good. The circular edge of both RF chokes have imperfections and the transmission line after the RF choke on the left as well.

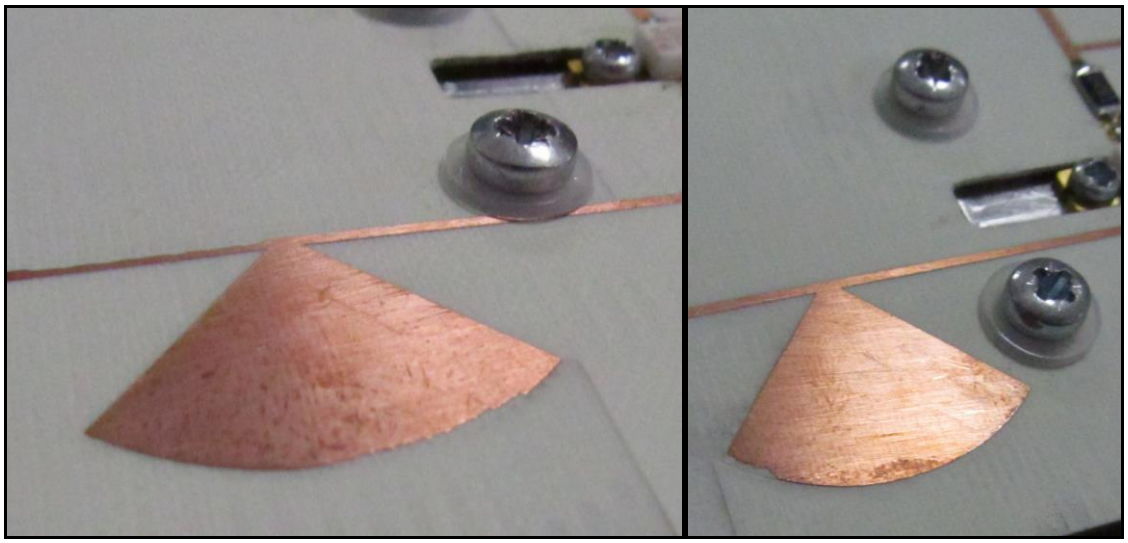


Figure 4.9 – Imperfections at the radius edges.

After the milling process we had to make the soldering of every component, the connectors and the cables for the biasing.

Moreover, we had to make some modifications to the heat sink because the transistor was too thick for the substrate, hence, the gate and drain pins did not get in contact with the copper lines.

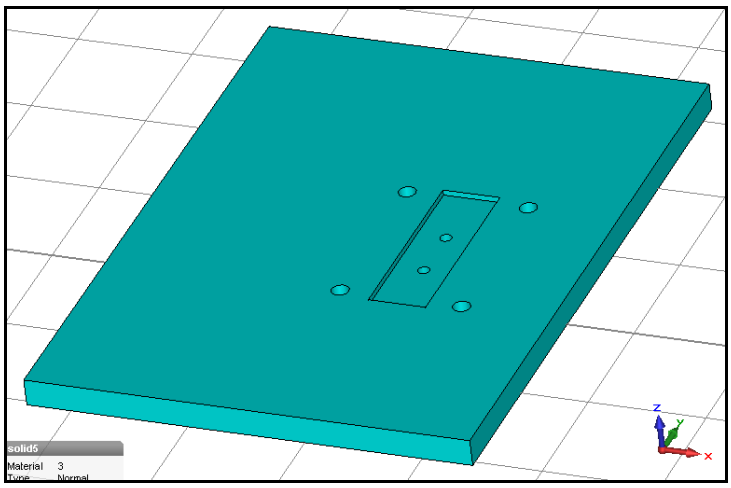


Figure 4.10 – Heat sink modification.

The modification basically consists in making a slot onto the heatsink with the exact dimensions which make the transistor touch at the same time the heat sink with the source pin and the substrate with the gate and drain pins. The modification shown in Figure 4.10 was made in CST and the physical work was made by the guys in the mechanical workshop.

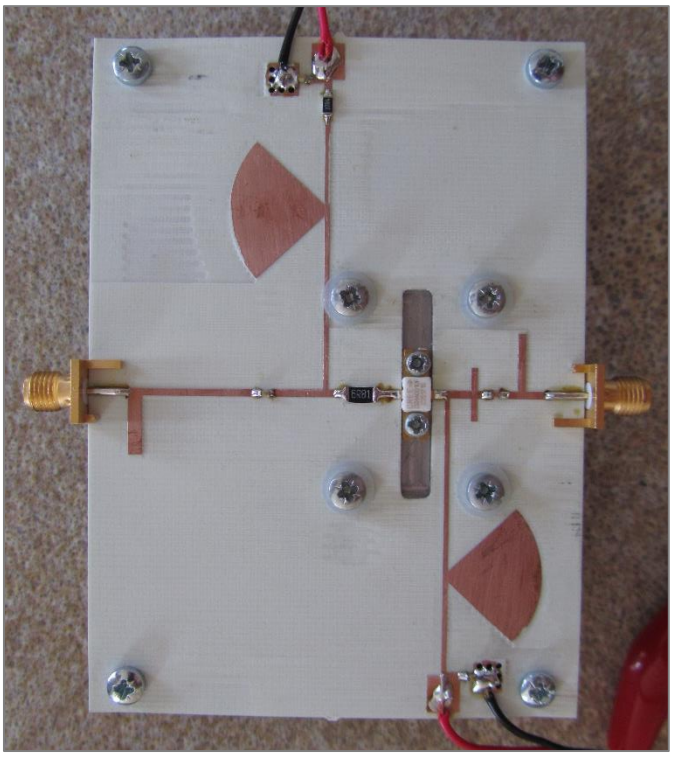


Figure 4.11 – Design finished and ready to test.

Finally we assembled the substrate and the transistor to the heat sink with a thermal grease layer. The final result can be seen in Figure 4.11.

4.3. Testing

For the biasing we used two independent power supply units.

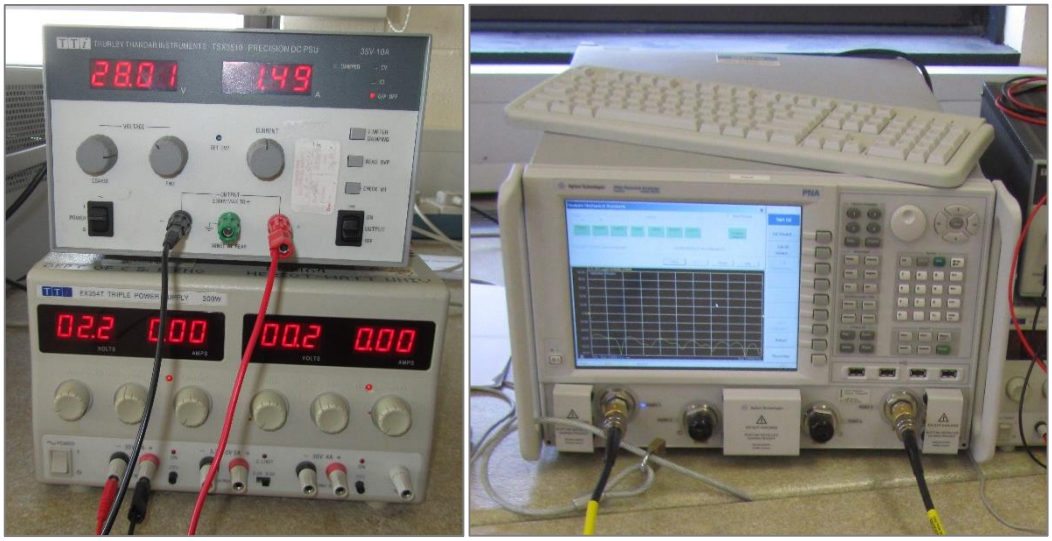


Figure 4.12 – Power supply units (left). Drain bias (top) and Gate bias (bottom). PNA Agilent N5225A (right).

For the port analysis we used the PNA (Programmable Network Analyzer) Agilent N5225A. Before we start using the PNA, it must be first calibrated. With this calibration all the losses caused by the cables and the SMA adaptors from 2.4 to 3.5 mm are compensated.
In the following pictures it can be seen a little about the calibration process.

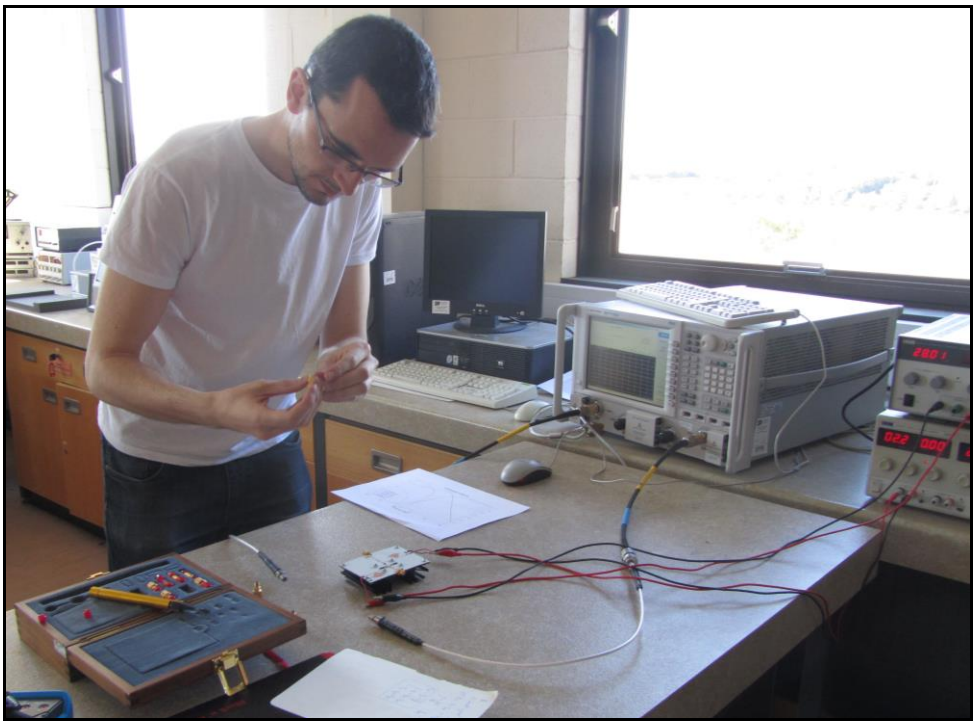


Figure 4.13 – Me, doing the calibration (I).

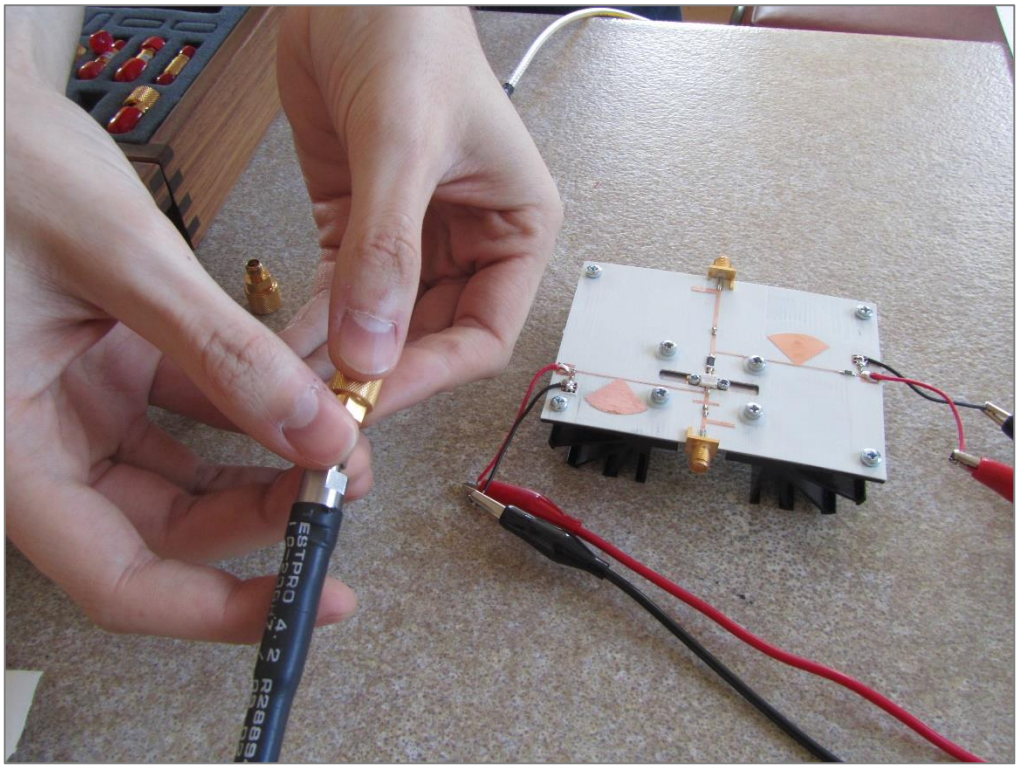


Figure 4.14 – Me, doing the calibration (II).

Figure 4.15 – Me, doing the calibration (III).

Figure 4.16 – Broadband load.

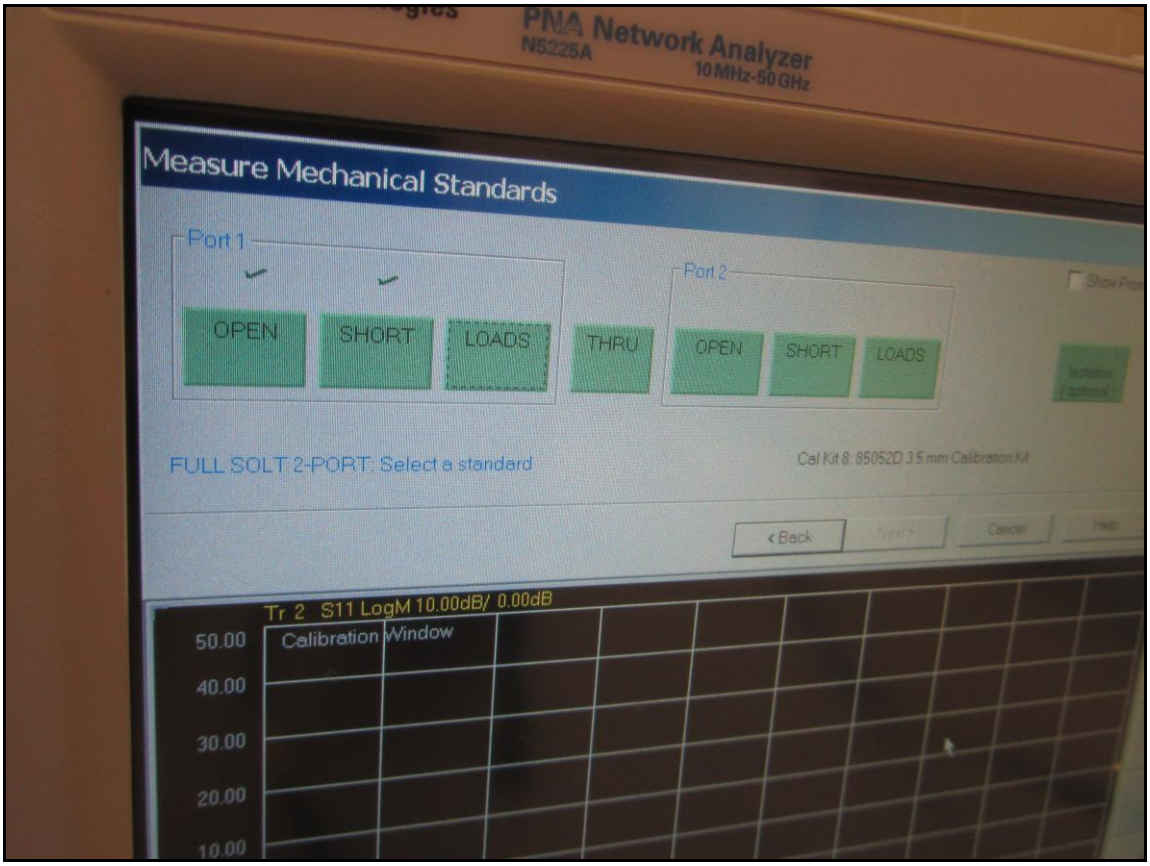


Figure 4.17 – Unguided calibration process.

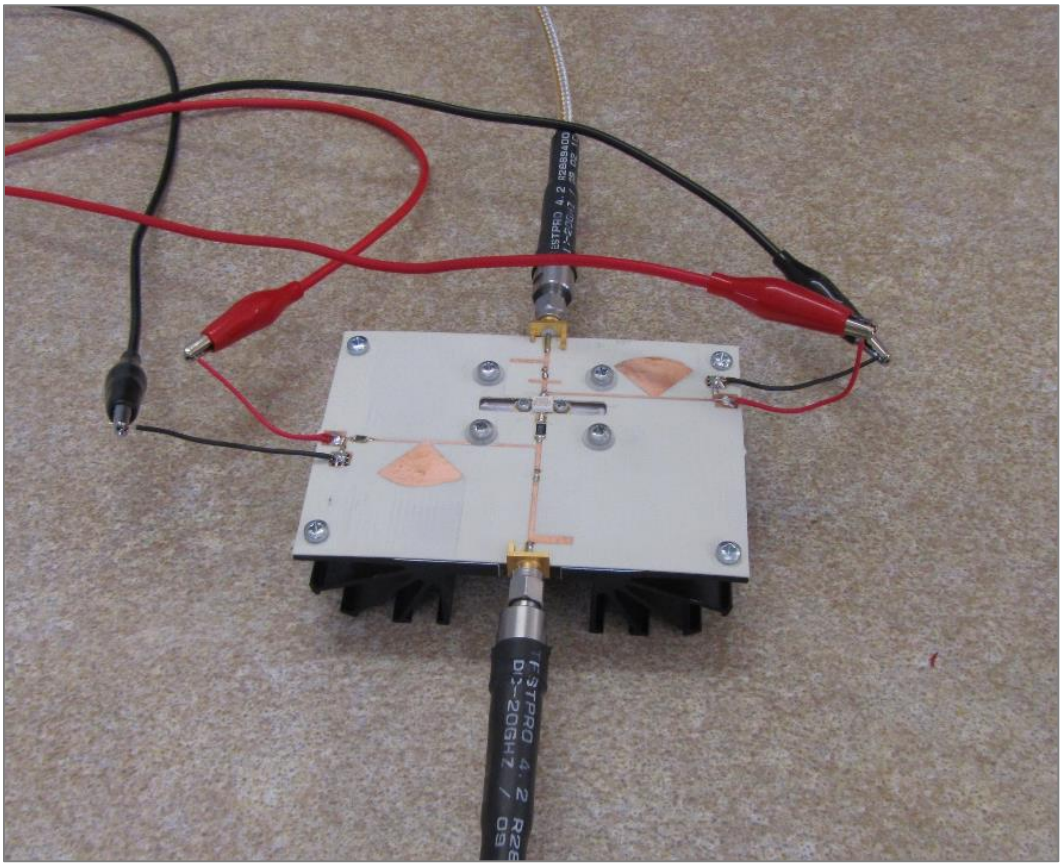


Figure 4.18 – Biased amplifier.

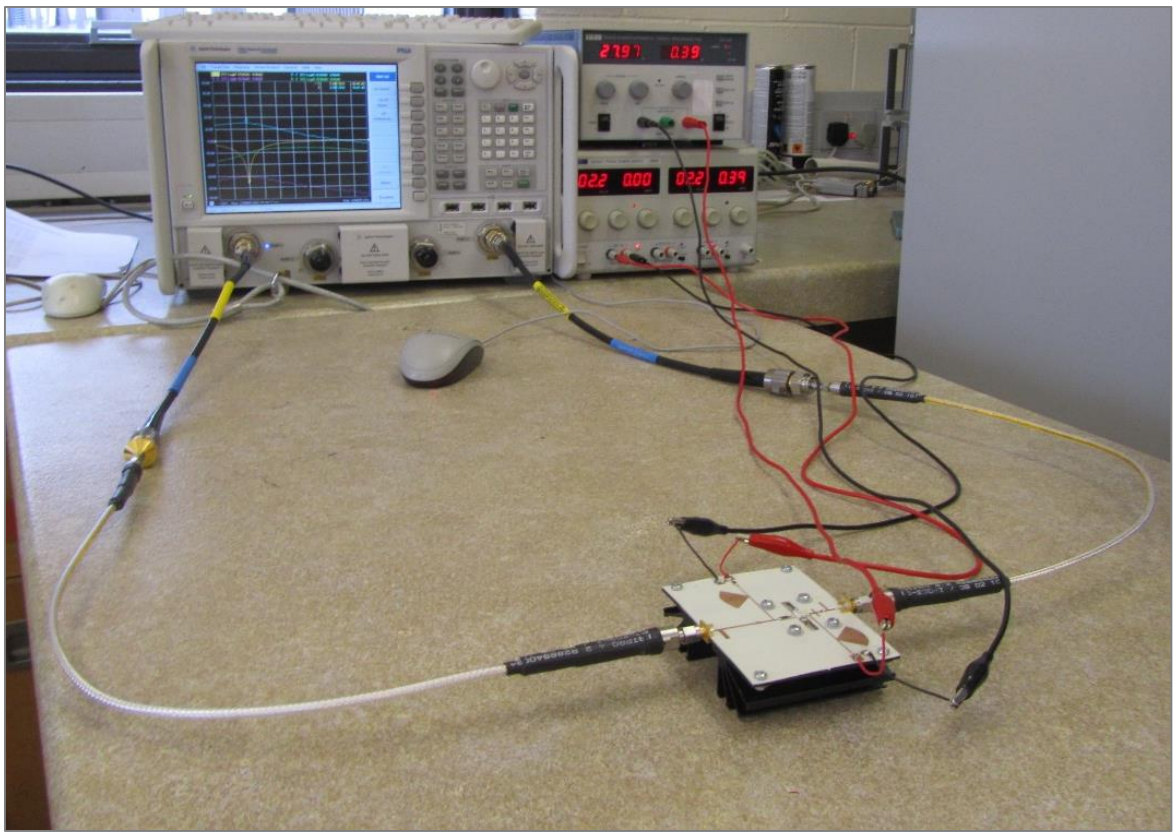


Figure 4.19 – Testing the amplifier.

4.4. Results

As we can see in Figure 4.20 and 4.21, the S-Parameters are very similar to the simulated ones, but they come with a particularity that they are shifted to approximately 2200MHz. The solution for this problem is relatively easy. The technique used to fix this is the resize of the whole amplifier taking into account the frequency desired and the frequency shifted.

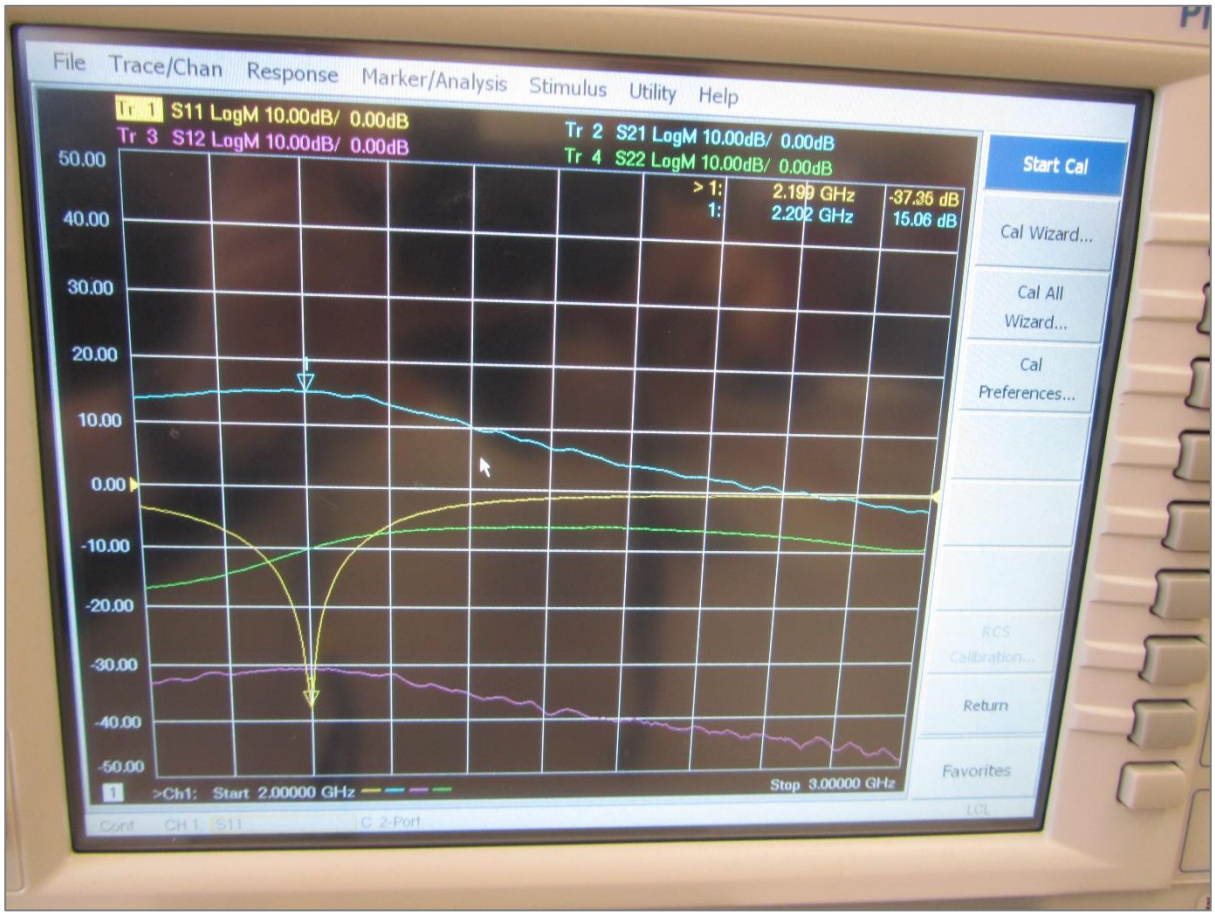


Figure 4.20 – Measured S-Parameters.

This is,

$$Resize\ factor = \frac{f_{shifted}}{f_0} = \frac{2200}{2450} = \frac{44}{49} \simeq 0.898$$

With that factor we rescale the size into a smaller design and the problem should be fixed. Apart from that the S_{22} parameter is the only one that it does not fit with the simulations.

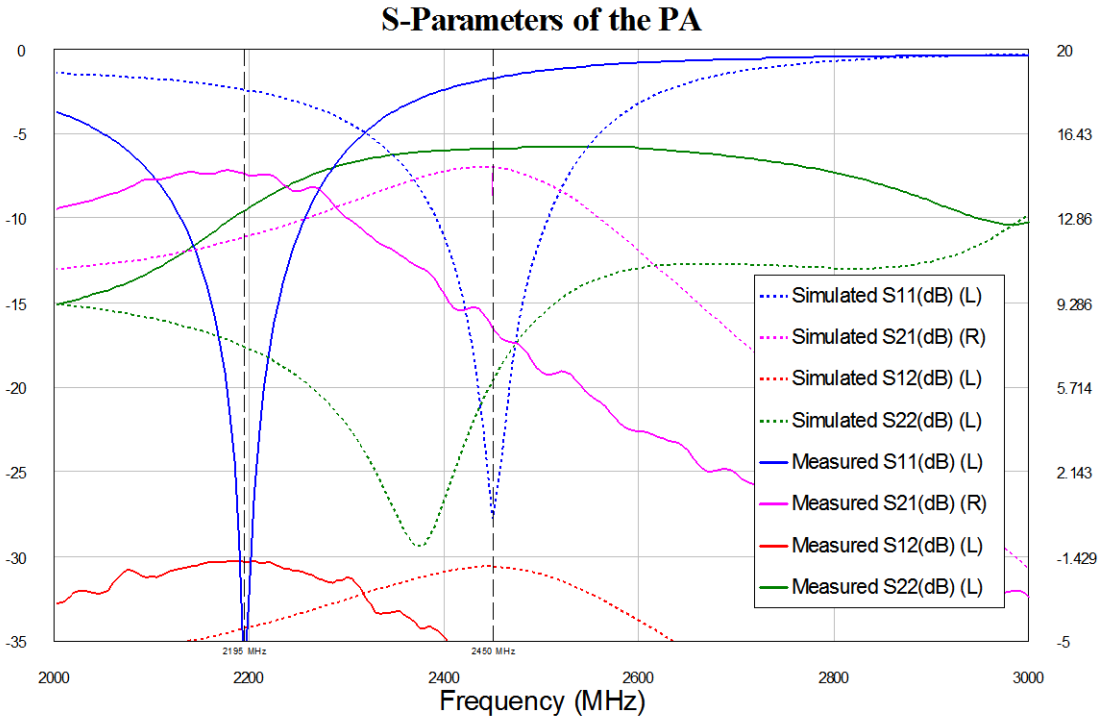


Figure 4.21 – Measured Vs. Simulated S-Parameters.

4.5. Thermal issue

When the amplifier was running during above 4 minutes, the S-Parameters started to move and then they did not come back again to the right values. Possible causes to this problem could be:

a. Interface material between the transistor and the heat sink maybe has not been applied in the right way and/or quantity.

b. The Q-Point chosen is too close to the maximum power dissipation which makes put the transistor on its limits and this makes it burn by overheating.

c. The S-Parameters measurements were made with 0dBm at the input. Low input power involves low PAE. And low PAE means most of the power is being dissipated by the transistor.

Because of this issue we were not able to measure other interesting parameters such as PAE, Gain, nonlinearities and so on.

5. Conclusions and Future Work

The analysis , implementation, simulation, manufacturing and testing of a Class A Power Amplifier working at ISM band (2.45 GHz) has been proposed. Initial good results were obtained, such as, 15dB gain, P_{1dB} at 26dBm approximately and unconditional stability along a very wide range of frequencies due to the stabilization resistors.
The bad results in the end makes this work as a potential source of learning about the issues that happened for the future.

5.1. Future Work

The main paths that should be taken with this work would be:

1. Investigate and solve the thermal issue that made the transistor overheat.
2. Make more and various measurements in order to check the proper operation and to learn about how to use the PNA for this purpose.
3. Try to standardize the power amplifier design process and make it more practical.
4. Make the design of a class B and AB, so then we will be able to compare these three classes in terms of noise, nonlinearities, gain, efficiency, etc.

5.2. Personal Feelings

This work has opened a door to investigation and curiosity in myself despite the testing bad results in the end. Moreover, it made me become more independent and autodidact, in fact, I think this is a really good preparation to the PhD. and makes me have a good work routine and feel more confident to face the challenges of the future.

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