Real Time Test Benchmark Design for Photovoltaic Grid-Connected Control Systems

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Abstract

This paper presents a dual digital signal processor (DSP) hardware architecture for a grid-connected photovoltaic interface test benchmark, based on a cascade DC/DC converter and DC/AC inverter, with coordinated control algorithms. The control hardware has been designed to test distributed generation (DG) interfaces to be integrated in a hierarchical structure of computational agents, to apply distributed control techniques to the power system management. The proposed dual DSP architecture enables the programming of the control software for the DC/DC converter and the DC/AC inverter in the same processor, to keep the other one for additional operations that are required when there is a high degree of interaction between the DG

unit and the rest of the electrical grid components. The hardware architecture has been tested in several real situations such as power factor correction and anti-islanding protection.

Keywords: photovoltaic energy; distributed generation; real time control; test benchmark.

1. Introduction

DG is defined as the integrated or stand-alone use of small, modular electric generation close to the point of consumption. It differs fundamentally from the traditional model of centralized generation and delivery, insofar as it can be located near end-users within an industrial area, inside a building, or in a community. The downstream location of DG in the power-distribution network provides benefits for both customers and the electric-distribution system. The small size and the modularity of DG support a potentially broad range of customer (and grid) applications where central plants would prove impractical.

Interfaces are the point of interaction between DG and the energy infrastructure. The physical interfaces include a DG unit interaction with the electrical infrastructure that are mainly concerned with issues such as safety, protocols, system impacts, reliability, standards, and metering. The complexity of the interface increases with the level of interaction required between the DG unit/owner and the electrical grid/distribution company, but all of them deal with a new situation where the nature of the distribution network changes from a passive behaviour to an active one. Then, to ensure correct operation of the distribution system and adequate service quality to customers, various

technical issues have to be tackled, such as voltage control, power quality, the thermal condition of the lines, and system protection [1].

To test all the capabilities that any interface device may have, a DG simulator prepared to work with real grid operation conditions should be used. The use of real-time systems plays a decisive role in the adaptation of theoretical improvements, without requiring significant extra effort in electronic development. They also avoid the large amount of concentrated and distributed computational resources that are required for the implementation of complex control algorithms, signal processing, communication with the external system and the user interface, diagnosis and protection functions [2,3]. The control hardware that we show in this paper has been designed to test photovoltaic distributed generation (PV-DG) interfaces to be integrated in a hierarchical structure of computational agents, to apply distributed control techniques to the power system management.

Usually, the control subsystem has to manage the PV-DG unit to obtain an optimal efficiency for the DC/DC converter and the DC/AC inverter, and it is mainly determined by the nature of the primary energy source and the power quality restrictions required to be connected to the main grid. In this case, each one of the above mentioned power electronic devices, is controlled by an independent DSP. Additionally, when the level of interaction required between the PV-DG unit and the main electrical grid increases, control tasks become more complex: decision-making depends not only on local parameters but also on external data, for example, the state of the real-time grid, energy pricing and demand forecasting. When a high degree of embedded generation is considered, coordination between PV-DG units is an essential issue. All of these trends

need powerful data processing tools that must be programmed to obtain the corresponding switching signals for contactors and power electronic devices.

To reduce the number of the processing units, we propose in this paper an architecture that integrates the control of the DC/DC converter and the DC/AC inverter in only one DSP (the TMS320F2812 of Texas Instruments), and includes another one (the TMS320C6713) for those extra-functionalities that the grid interface must have to be able to work in an integrated fashion with all the grid suppliers.

2. Description of the PV-DG interface test benchmark

One of the most common control strategies applied to the grid-connected photovoltaic systems is based on a voltage-oriented control, employing a controller for the DC link voltage and a controller to regulate the injected current to the utility network. Based on this idea, the test benchmark design presented in this paper has the characteristics described below.

2.1. PV-DG power subsystem

The power subsystem (Figure 1) has basically three components (the step-up DC/DC converter, the DC bus, the DC/AC inverter and a LCL filter) for power conditioning, two sets of contactors (DC and AC) to operate the hardware platform, the EMI filter and the isolation transformer (Yd5, R_t=0.247Ω, X_t=0,201Ω) The DC/DC converter is used to increase the DC bus voltage required for reducing the number of PV panels with a series connection [4,5]. We have chosen a rated power of 20 kW, following the trends that the Spanish government indicates to obtain a better feed-in tariff with a roof-mounted system [6]. The power electronics for the DC/AC inverter and the DC/DC converter are based on electronic kits from Semikron (SKiiP 513 GD172-3DUL and

SKiiP 642 GB120-2DL). The DC bus has a capacitance of C_{DC}=2300µF, and the LCL filter has the following characteristic: L_f=1.1Mh, R_f= 0.0465Ω and C_f=4µF.

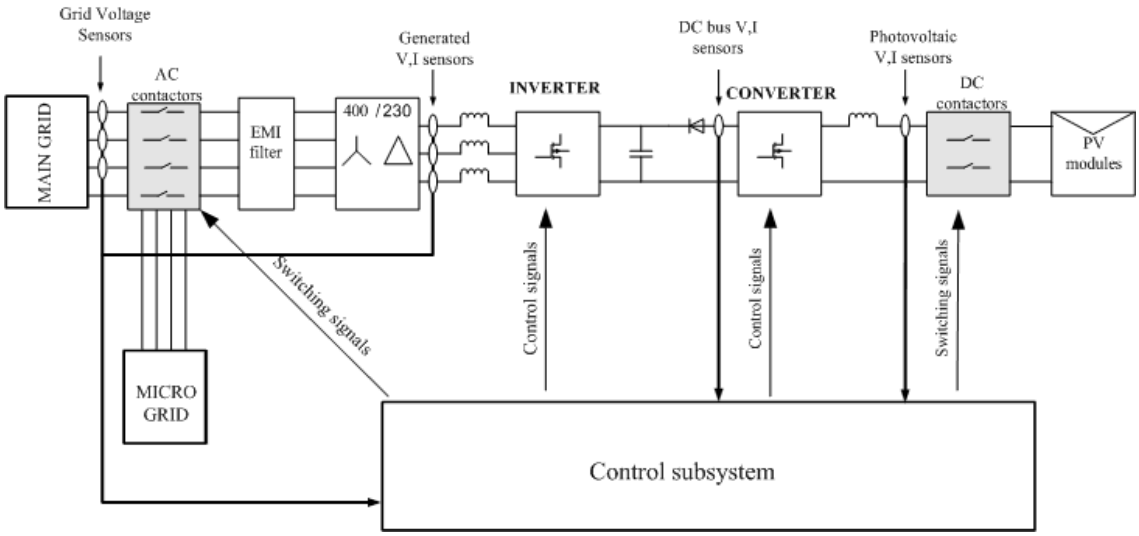

Figure 1. Description of PV-DG power subsystem.

2.2. PV-DG control subsystem.

As we have mentioned, when a high degree of embedded generation is considered, the control hardware must be flexible to move between different operating modes, the control and protection algorithms become more complex and the amount of information that it will have to handle is greater. To get these objectives with the minimum number of processing units, the proposed dual DSP architecture enables one to programme the control software for the DC/DC converter and the DC/AC inverter in the same processor to keep the other one for additional complex operations.

To work with these high-demanding and complex algorithms, such as FIR and IIR filters, neural networks and fuzzy systems, the use of floating-point DSP (for example, the C6000 series of TI) is mandatory [7]; but this DSP series does not have on-chip

peripherals, and the use of programmable logic (for example, FPGAs) is needed for doing real-time industrial control [8]. We have chosen another way to solve this problem: to use one floating-point DSP for high-demanding software, and a fixed-point microcontroller with on-chip peripherals (for example, the C2000 series of TI).

Compatibility between both operating modes also requires the communication between DSPs. The complete sequence of functions for the hardware architecture is represented in the block diagram of Figure 2.

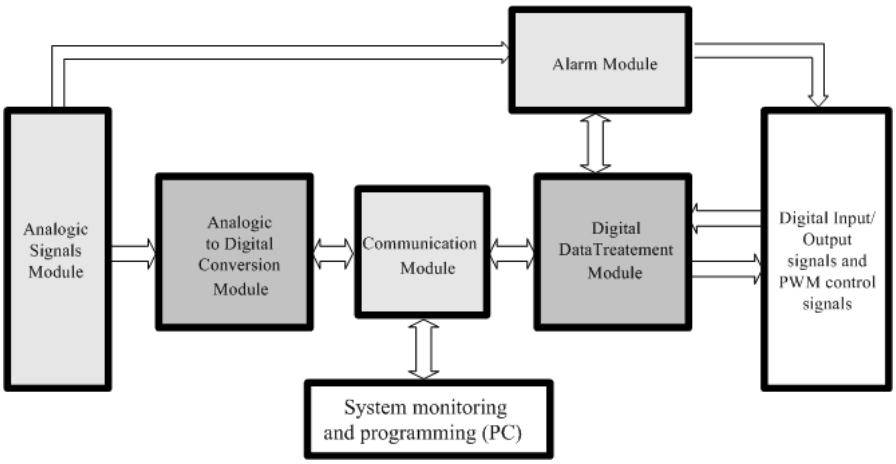

Figure 2. Block diagram for the control hardware functions.

Then, to obtain the control signals, each module has the following tasks:

- **Measurement of analog signals.** This block implements the simultaneous acquisition of the AC and DC voltages and currents required for control algorithms. All sensed signals are floating-point, and the sample frequency is 48 kHz.
- **Analog to digital conversion.** The signals must be converted from analog to digital to be managed in the DSPs. In this prototype, the signal conditioning is different for DC signals and AC signals. DC signals are captured directly by the DSP2812

Analog-to-Digital Converters (ADC), and AC signals are conditioned in electronic PCB designed *ad hoc*.

- **DSP communication interface.** The Multi-channel Buffered Serial Port (McBSP) is selected to obtain a high-speed connection between the two DSPs. The Time Division Multiplexed (TDM) protocol is selected, because it verifies the design requirements dealing with transmission speed, and hardware implementation is easier and less expensive than the other solutions. The TDM protocol does not require additional interfaces, and it only uses 3 lines for the DSP connection. The communication system uses optical fibre transceivers to avoid electromagnetic interferences.

- **Alarm module.** The main function of this module is to check the level of each current and voltage measured in the system and to interrupt the IGBT's PWM signals when threshold levels are violated. The alarm module also acts when the temperature of IGBT rises over the rated values, and when it receives an external order from other protection algorithms implemented like those that detect islanding situations. The control hardware has a redundant alarm system to improve the security when it is used.

- **Power converters control block.** One singularity of the proposed hardware architecture is that the PWM signal generation for the control of the different power converters (DC/DC and DC/AC) is integrated in only one DSP (the TMS320F2812 of Texas Instruments). This operation mode implies there are two relevant problems to be solved.
    - The time interval in which the processor has to make all the computational effort (DC/DC and DC/AC control operations, and coordination) is the time

period equivalent to the IGBT's commutation frequency. High commutation frequencies (better for power quality issues such as harmonic rates) mean low time periods. With the technology used and the DSP communication setup chosen in our case, the commutation frequency was 12.208 kHz and the corresponding time interval is 82 μs.

  - A coordination procedure between the DC/DC and DC/AC power devices is required to avoid mismatch operations that could produce component damage. In our benchmark, this procedure has been implemented by software in the master processing device (DSP2812).

- **DSP-PC communication block:** This block enables the bi-directional communication between the grid interface and a PC for programming DSPs and monitoring the system. The communication is done using RS232-C ports.

2.3. DSP communication interface configuration and coordination procedure.

The control hardware architecture proposed is based in a master/slaver relationship between the two processors. The distribution of the functions programmed in each one and the configuration of the communication system are critical issues that have to be carefully defined to optimize the use of the electronic components. The key points that we have considered to solve the software architecture are the following:

- The communication must be bidirectional. The information must flow from the main grid to the microgenerator and vice versa.
- The master DSP must support the alarm module and the power control module software.

- The slave DSP must support the digital data treatment module and the additional functions considered for the interaction with the main grid. In our benchmark, we have programmed in the slave DSP, the anti-islanding protection and the phase-locked loop algorithms .

2.3.1. DSP communication interface configuration.

To communicate the master and slave processors, McBSP interface is used, and the time-division multiplexed (TDM) protocol is selected to deal with McBSP multichannel operations. The TDM protocol allows a high bi-direction data flow, with a selectable data size (8, 16, 24 ó 32 bit). It is not necessary to convert the transferred data if the communication parameters are correctly adjusted. In this way, the DSP's avoid the use of part of their resources in the conversion and rebuilding of the data. TDM protocol can send and receive until 128 channels in each frame. The frame size is controlled by the synchronization signal and each bit of each channel is synchronized with the clock signal.

To apply these general concepts to the software architecture in order to configure the communication system, there are three technical constraints: the maximum switching frequency of the power electronic devices (14 kHz for the SKiiP 513 GD172-3DUL and 20 kHz for the SKiiP 642 GB120-2DL), the number of input/output registers of the slave processor and the clock speed of McBSP (37.5 MHz). Data words have 32 bits and in our prototype, and 16 registers have been configured as input channels (6 channels for phase currents and voltages, 2 channels for grid surveillance results, 2 channels for reactive power management, 2 channels for sensitivity thresholds of protection algorithms and 4 spare channels). Then the complete data stream has 512

bits. To transmit the 512 bits in the time period between IGBTs switching, the frequency of the synchronization signal should be 7.16 MHz, but it is not compatible with the clock speed of the McBSP. Then, the highest frequency of the synchronization signal compatible with the clock speed of the McBSP is 6.25 MHz that corresponds to a IGBTs switching frequency of 12.2 kHz also inside the technical restrictions of the power electronic device.

2.3.2. Coordination procedure.

The coordination procedure has been implemented in the master processing device. The most relevant tasks of this procedure are the following:

- Starting to check the system to detect a communication failure. If any, the alarm module is then tested and after an OK signal, the ADC function is initialized.
- The ADC function first reads the DC input (from photovoltaic panels) and the grid voltage, and if they are correct an enable signal closes the DC contactor and initializes the DC/DC control software.
- The ADC function now reads the DC bus voltage, and if it is acceptable, then the DC/AC software sends a closing order to the AC contactor.
- The whole system is checked again, and, if there is no alarm signal, the current injection to the grid starts from zero up to the programmed value in a linear progression.

3. Layout of the control hardware.

The functions described are distributed in the printed circuit boards designed for the hardware architecture (Figure 3).

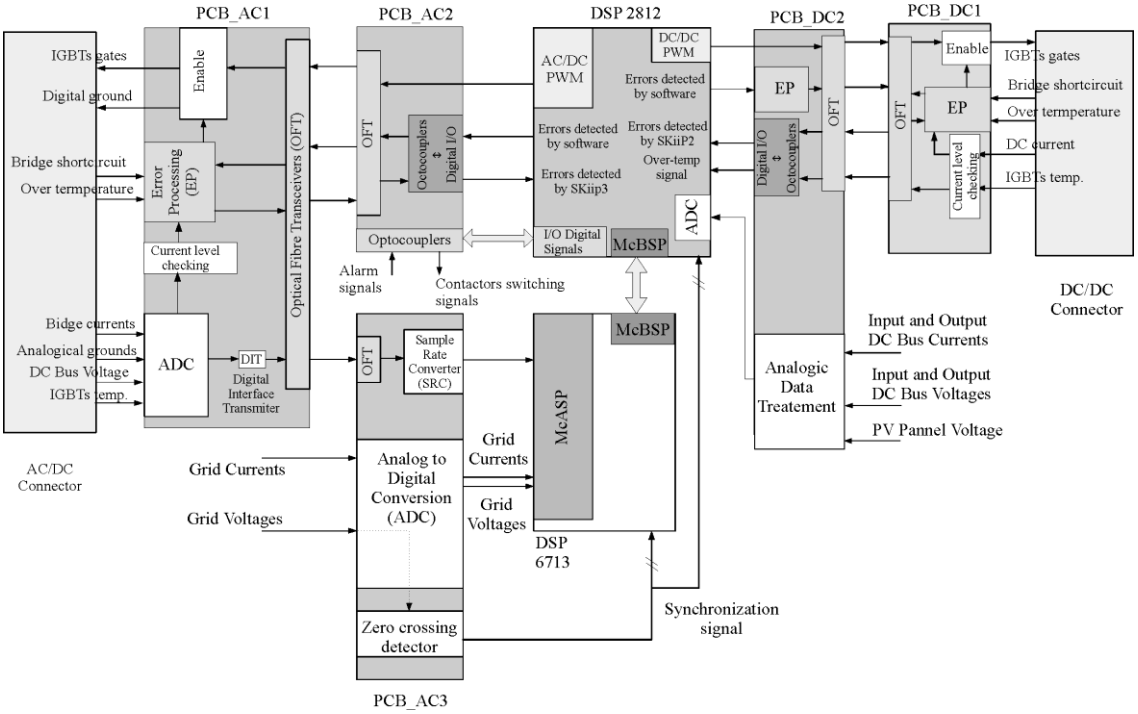

Figure 3. The control hardware architecture.

At the DC/DC side:

- PCB_DC_1: This is the SKiiP 642 GB120-2DL interface board that sends the DC/AC IGBT bridge switching signals from DSP2812, and reads the analog and digital alarm signals from the SKiiP to interrupt the PWM control, if any.
- PCB_DC_2: This is the DSP2812 interface board that reads the analog DC signals from photovoltaic panels and the DC bus adapting them to be digitalized in the DSP2812 analog-to-digital converters. It also has to manage the optical fiber transmission for control and alarm DC side signals.

At the DC/AC side (Figure 4):

- PCB_AC_1: This is the SKiiP 513 GD172-3DUL interface board that sends the DC/AC IGBT bridge switching signals from DSP2812 and reads the analog and digital alarm signals from the SKiiP to interrupt the PWM control, if any.

- PCB_AC_2: This is the DSP2812 interface board. It manages the optical fiber transmission for control and alarm AC side signals. It also receives the alarm signals from the electric security devices through optically coupled devices
- PCB_AC_3: This is the DSP6713 interface board where the analog-to-digital conversion for AC signals received from the grid and the IGBT's bridge is implemented. A zero crossing detector (ZCD) has been implemented in this board to generate the synchronism signal. The synchronism signal updates the pointer that points the phase-shift corresponding to the output current references. The generated pulse starts the phase-shift counter. It is initially loaded from the look-up table for the phase register, the code corresponding to the actual value of the shifted phase according to PWM patterns [9].

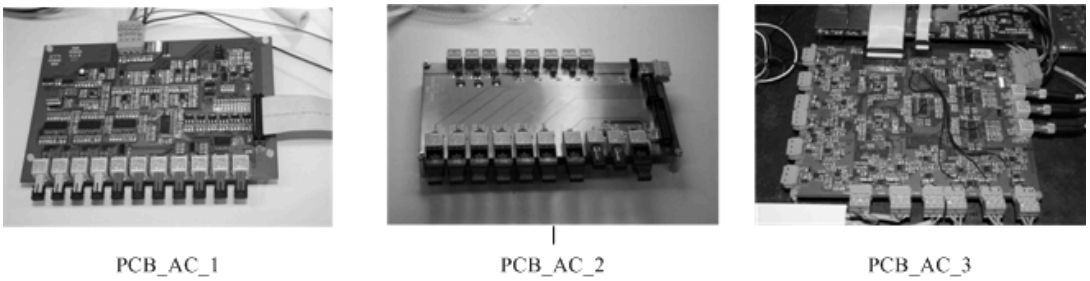

Figure 4. Printed board circuits for the AC/DC interface.

4. Checking the PV-DG interface test benchmark

If we consider that the control architecture allows us the management of the benchmark capabilities, the proposed design must be tested to assure the correct operation of all the components, its integration with the power subsystem and its connection with the utility grid. The PV-DG interface test benchmark has been subjected to several proves for island and grid-tied operation modes.

For laboratory tests, a programmable DC power source AMREL HPS800-180-D013 has been used to simulate PV panels, and a SPITZENBERGER EMC D 15000/PAS to analyze the DG simulator behaviour with ideal conditions (connected to a virtual grid with perfect sinusoidal phase voltages). To simulate load steps we used the resistive load bank, AVTRON LPH-60. For power quality measurements we used a Fluke 430 Series Three-Phase Power Quality Analyzer.

4.1. DC side tests

In this set of tests, we show the DC power subsystem behaviour in the following situations: soft starting, load step, and input voltage fluctuations. In the pictures below, we show the results obtained for the second and third situations.

4.1.1. DC output response to input voltage fluctuations

A typical PI regulator has been implemented to keep the output voltage with a maximum allowed variation of ±5% over the rated voltage. In Figure 5, a situation in which input voltage first grows until it is 250 V and immediately falls down until it is 130 V. The drop in the output voltage is due to the PID regulator limitation fixed by project constraints (a minimum input voltage of 33% of rated voltage is required to guarantee the output voltage).

4.1.2. DC output response to load step

In Figure 6, the output voltage remains inside the ±5% fluctuation band when a 50% load step is applied.

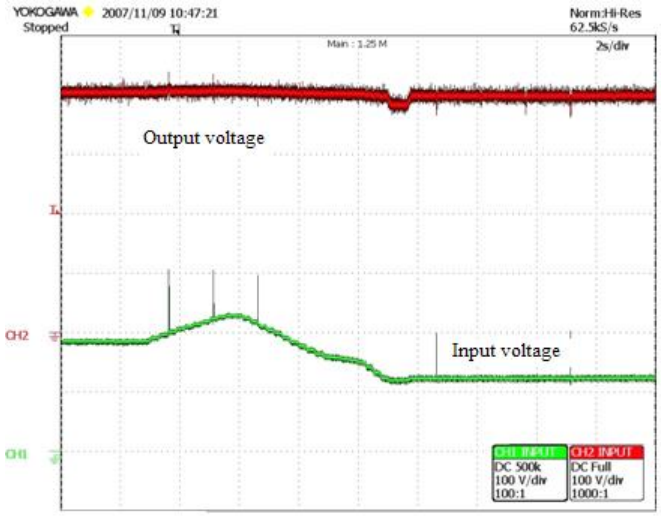

Figure 5. DC output voltage response to input voltage fluctuations.

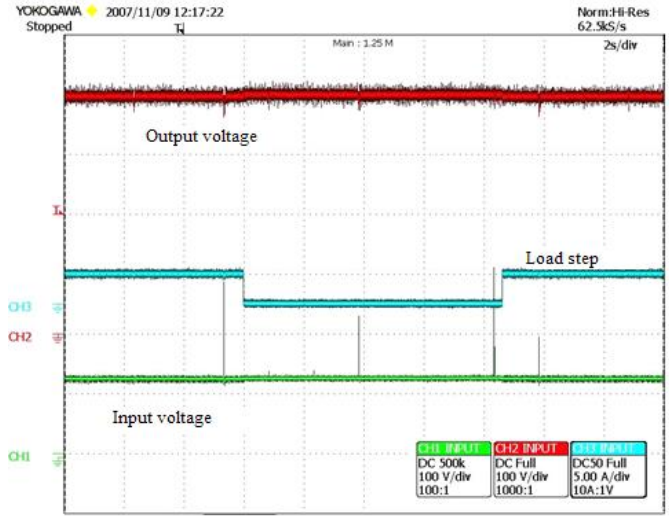

Figure 6. DC output response to a load step.

4.2. AC side tests

For grid-tied operation, the PV-DG simulator has to manage the DC/AC inverter to satisfy not only its own control algorithms, but also the external requirements that the utility grid dispatching could consider (for instance, power quality, active and reactive power control, voltage regulation...), and other additional protection issues such as anti-islanding algorithms. In this paper, we show the behaviour of the test benchmark in

four key issues: grid synchronization, harmonic distortion, active and reactive power control and anti-islanding relaying.

4.2.1. Grid synchronization

For this important issue, the benchmark could work with two different subsystems to obtain grid synchronization. By software, it is possible to programme the slave DSP with, for example, any phase-locked loop (PLL) algorithms [10,11]. To check the benchmark, a PLL is implemented in the d-q synchronous reference frame, as illustrated in Figure 7 [12,13]. This structure uses an abc/dq coordinate transformation, and the lock is realized by setting the U_{d_ref} to zero. A regulator, usually a PI regulator, regulates the error to zero. The voltage-controlled oscillator (VCO) integrates the grid frequency, and outputs the utility voltage angle that is fed back into the α-β to d-q transformation module.

This structure of PLL consists of two major parts, the transformation module and the PLL controller. The transformation module has no dynamics. In fact, the PLL controller determines the system dynamics. Therefore, the bandwidth of the loop filter determines the filter's filtering performance and its time response. As a consequence, the loop filter parameters have a significant influence on the lock quality and the overall PLL dynamics.

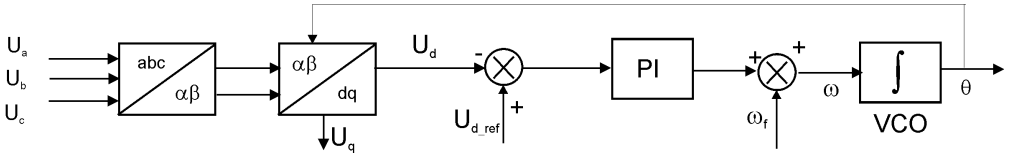

Figure 7. The PLL algorithm.

Under ideal utility conditions, a loop filter with a wide band-width yields a fast and precise detection of the phase angle and the amplitude of the utility voltage vector. This method will not operate satisfactorily if the utility voltage is unbalanced, or distorted by harmonics or frequency variations.

As we have mentioned, a typical zero crossing detector has been implemented in the DSP6713 interface board to have a redundant hardware solution for grid synchronization.

4.2.2. Harmonic distortion rates

The converter must be able to produce a low distortion, high-power factor AC current. The same aspects related to the voltage and current distortion produced by non-linear loads can be considered for the injection of power into the grid. In the absence of a specific standard, this paper takes as a reference the limits for current harmonics given by the IEC61000-3-4 [14]. The justification for this approach is that, from the resulting line voltage degradation, there is no difference between injected and absorbed current.

This fact allows us to analyze the converter input current normalized to a unity fundamental current, so as to obtain results that are independent of the input power. For the test conditions defined in the IEC 61000-4-7 [15], the current waveforms for the full load situation are shown in Figure 8; all the current harmonics are below the IEC 61000-3-4 limits.

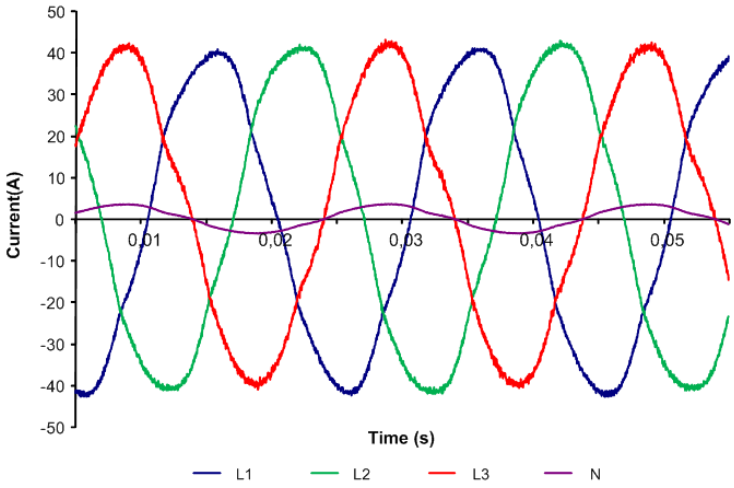

Figure 8. Full load AC output currents.

4.2.3. Active and reactive power control.

Reactive power flow wastes energy and transmission capacity, and causes voltage drop. To correct this lagging power flow, the leading reactive power (current leading voltage) is supplied to bring the current in phase with voltage. Distributed generation is an attractive option for solving reactive power and distribution system voltage problems because of its proximity to load [16]. A fundamental classification of small generators is based on their capability to produce controlled active power on demand. Sources that lack this capability (such as photovoltaic panels or wind turbines) are normally operated under PQ control [17,18], ensuring that maximum active power P is extracted from the prime source, under a constant reactive power Q or power factor (possibly regulated). In our system, reactive power is controlled by the dq algorithm shown in Figure 9.

The control subsystem module is formed by the synchronization algorithm to get a unitary power factor for the connection, the two cascaded control loops, and the SVM module. The two cascaded control loops are formed by the outer one that uses a PI regulator (PI_1) for the dc-link voltage by comparing this to its reference obtained from

the DC/DC control subsystem, and the inner one that uses two PI regulators (PI_2 and PI_3) for the dq components of the 3-phase real currents. The latter uses a synchronous reference frame control approach (dq control), where Park transformation is applied to the line currents for vector control: the d reference component at the output of PI_1 is compared to the d component of the real currents, and the error is regulated by PI_2. The q reference component that is proportional to the desired power factor of the connection, is compared to the q component of the real currents and the error is regulated by PI_3. Finally, the Inverse Clark Transformation is then applied to the outputs of PI_2 and PI_3 to obtain the 2-phase stationary reference frame signals that feed the SVM module for firing the 3-phase power switches of the VSC. If the utility grid vector is aligned with the d axis, as mentioned above, the instantaneous active power is controlled in the d axis, whereas the instantaneous reactive power is controlled in the q axis.

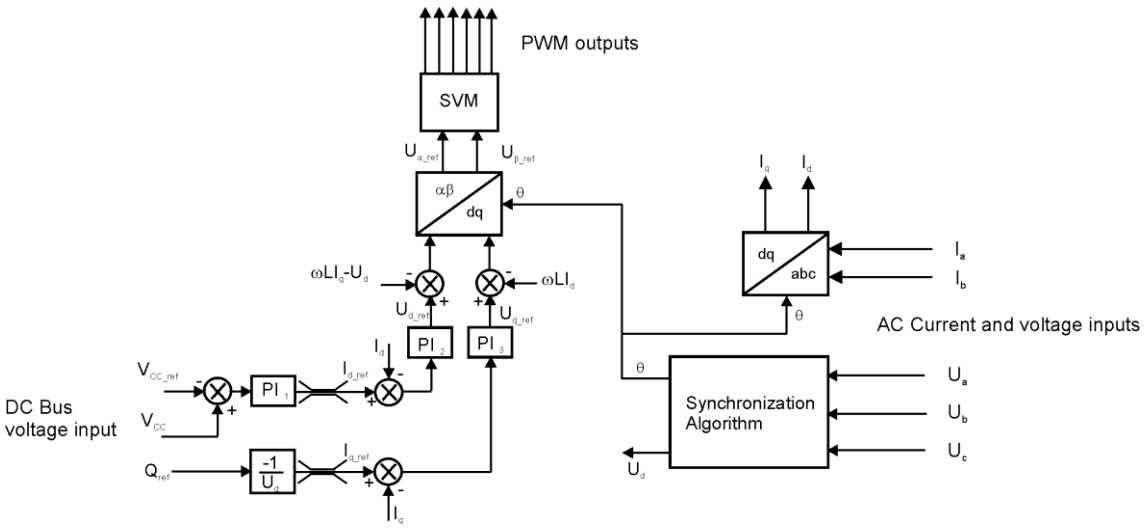

Figure 9. DQ control algorithm for the AC/DC inverter.

To test this issue, we have programmed the hardware to change from a situation with a power factor close to unity to another one with an injected reactive power of 5 kVAr,

and a power factor close to 0.9. Figure 10 shows how the current phase shift increases to get the desired power factor.

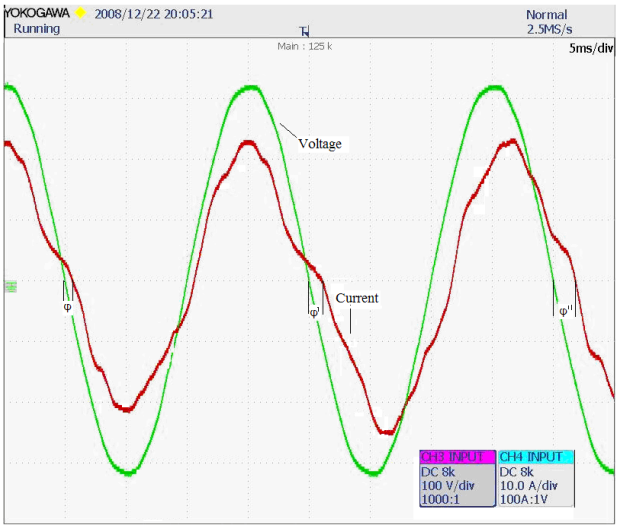

Figure 10. Current phase shift evolution.

4.2.4. Anti-islanding protection

The islanding phenomenon of PV-DG refers to its independent powering to a portion of the utility system even though the portion has been disconnected from the remainder of the utility source. This is because islanding can produce safety problems to utility service personnel or related equipment. Consequently, utility companies and PV system owners require that the grid-connected PV system includes the non-islanding inverter.

The islanding detection is an indispensable feature for DG-systems and many algorithms have been developed in the past decade. These methods may be divided into four categories: passive inverter-resident methods, active inverter-resident methods, active methods not resident in the inverter, and methods based on the use of communications between the grid and PV inverter. Active methods are intrusive and could distort the grid. They are not allowed in all networks, as they may affect power

quality and the correct operation of some equipment [19]. The passive inverter-resident methods implemented in the control hardware subsystem rely on the detection of a disturbance in the voltage at the PCC (Point of Common Coupling) [20]. Following this kind of detection, we studied a generic system for anti-islanding, defined in IEEE Std. 929-2000 [21] and in IEEE Std. 1547 [22].

An essential concept in the study of the system for islanding detection is the parameter non-detection zone (NDZ). This zone is the range in which the islanding detection scheme under test fails to detect islanding (in terms of power mismatch between the DG inverter and the load or load parameters). The aim of all islanding detection methods is to ensure that the NDZ is null, or to reduce the NDZ to near zero.

For islanding protection, all photovoltaic grid-tied systems are provided with over/under voltage protection, and over/under frequency protection. Even considering that this anti-islanding protection does not work well when the generated power is close to power consumption, nowadays it is required by Spanish electrical utilities for the PV system connection [23]. For this reason, we have programmed the slave DSP with over/under voltage and over/under frequency protection to check the designed hardware.

The results obtained when a grid overvoltage of 20% over the rated value is applied to the hardware platform are shown in Figure 12. The islanding protection switches off the inverter before the grid overvoltage relaying devices.

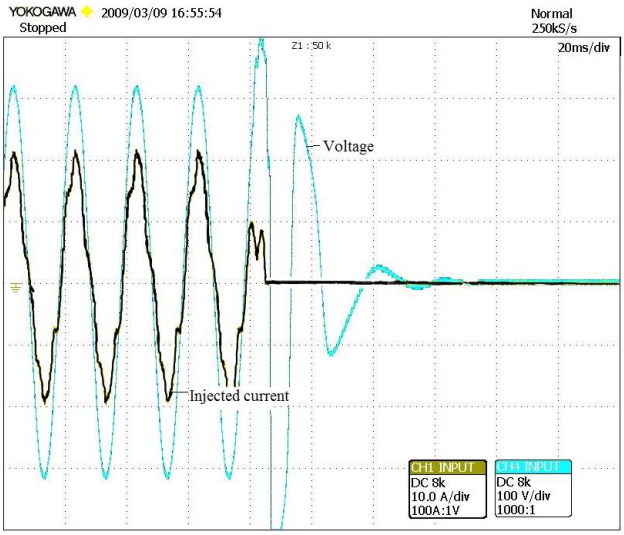

Figure 11. Anti-islanding response for a 20% overvoltage.

CONCLUSIONS

This paper presents the most important issues to be considered in the hardware and software architecture design for a benchmark to test control systems between the main grid and a photovoltaic generation unit. The proposed master-slave architecture enables to programme the control software for DC/DC converter and DC/AC inverter in the master processor to keep the slave one for additional operations that are required when there is a high degree of interaction between DG unit and the rest of the electrical grid components. The keystone of the system is how to make compatible the time interval required for the computational effort, with the corresponding one that the system needs to complete the information transference between DSPs. The test benchmark has been checked following the techniques required by IEC, and also under real conditions (grid-tied operation) with positive results. Future studies will design a hardware device to simulate the dispatching room of the electrical utility to test the real interaction capabilities of the grid interfaces.

ACKNOWLEDGEMENTS

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