Design and Control of a Dynamic Voltage Restorer

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Publication date:
2002

Document Version
Publisher's PDF, also known as Version of record

Design and Control of a Dynamic Voltage Restorer

by

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Dissertation submitted to the Faculty of Engineering & Science at
Aalborg University
in partial fulfilment of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering

Aalborg University, Denmark
Institute of Energy Technology
Marts, 2002

Ph.D. thesis

Design and Control of a Dynamic Voltage Restorer

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ISBN: 87-89179-42-0
This thesis is written in *MiKTeX 1.20e*, available on `http://www.miktex.de`

Preface

This Ph.D. study was carried out at the Institute of Energy Technology Aalborg University. The project was a part of a research program called Local Compensation sponsored by the electric utility companies in Denmark, ELFOR and Aalborg University.

The project has been followed by the main supervisor: Professor Frede Blåbjerg and the supervisors in the project committee: associate professor Birgitte Bak-Jensen, associate professor Hans Nielsen and associate professor John K. Pedersen from Aalborg University. Furthermore, in the technical group Allan Norsk Nielsen from DEFU, Peter Wibek Christensen from Nordvestsjællands Energiforsyning (NVE), Jesper Bak-Jensen from Himmerlands Elforsyning (HEF) and Bent Cramer from ELFOR have participated. The other participants in the research program have been Peter Lykkebo Thomsen, Hoysung Kim and Ph.D. student Martin Høgdahl Jensen. In the summer 2000, I spent three months at the University of Minnesota in Minneapolis, U.S. where I visited Professor Ned Mohan.

The implementation and testing of two prototype DVRs have taken a considerable amount of time and help from a number of people and companies. For the 10 kVA LV-DVR Axel Åkerman in Odense has kindly delivered 3 special designed 3.3 kVA injection transformers with the help of Ph.D. Uffe Borup and the 15 kVA LV-DVR converter was build on the basis of two VLT frequency converters from Danfoss Drives A/S.

For the HV-DVR the 380 kVA converter equipment has been very kindly supplied by American Power Conversion (APC A/S) in Kolding, Denmark. Help and assistance have been given by Søren Rathman, Klaus Moth, Martin Zacho, Jesper W. Petersen from APC A/S. Two 50 kVA 10/0.4 kV distribution transformers have been borrowed from Elforsyningen SydVendsyssel (ESV) and Nordjyllandsværket have sponsored a LV circuit breaker for the short circuit tests at Kyndby. The HV cables are delivered by HEF in Aalborg and the testing of the medium voltage DVR has taken place at DEFU′s test facilities in Kyndby. Assistance has been given from Steen S. Martinsen and Kaj H. Nielsen from NESA. Hans Jørgen Jørgensen and Henrik Weldingh from DEFU and Hans Nielsen from Aalborg University have given valuable help during all the tests at Kyndby.

The research program is motivated by a desire of generating knowledge about power quality, broadband modelling of components in the distribution system, design and control of Custom Power Systems (CUPS) and employment and control of

CUPS.

The aim of this work was to design and control a Dynamic Voltage Restorer (DVR) and experimental verify a high power DVR at the medium voltage distribution system.

Literature references are shown as [XX]. and at the end of the thesis an overall reference list is shown. Figures and tables are numbered as `chapter.number`. Equations are consecutive numbered in each chapter as `chapter.number` and a list of symbols is presented on page xi. At this time it should be mentioned that period is used as a decimal point.

Abstract

This thesis is the main results from a Ph.D. project under the research programme "Local Compensation" at Aalborg University. The main topics in the thesis are the design and control of a Dynamic Voltage Restorer (DVR). The DVR is a series connected device, which primarily can protect sensitive electric consumers against voltage dips and surges in the medium and low voltage distribution grid.

The thesis first gives an introduction to relevant power quality issues for a DVR and power electronic controllers for voltage dip mitigation. Thereafter the operation and the elements in a DVR are described. The advantages and disadvantages are treated by inserting the DVR in either the medium voltage distribution system or in the low voltage distribution system. Different topologies for a DVR are investigated on a converter and system level and the protection issues are treated.

The design of a DVR is treated and two prototype DVRs are designed and specified. The first DVR is a low voltage DVR (LV-DVR) rated for 10 kVA for insertion in a 400 V low voltage grid and the second DVR is a high voltage DVR (HV-DVR) rated for 200 kVA for insertion in a 10 kV medium voltage distribution system.

The control issues are treated and voltage controllers are discussed and designed. The focus is on compensation methods where the phases of the load voltages are unchanged and under normal voltage conditions the DVR is inactive and performs no switchings to reduce losses. If a voltage dip is detected the DVR injects the missing voltage until the energy storage is completely drained or the voltages have returned to normal voltage levels. The control of the HV-DVR is a combined feedforward and feedback control to have a fast response time and load independent voltages. The control is implemented in a rotating dq-reference frame, which gives a very good compensation of the positive sequence component and a damping of the negative sequence to less than 1/4 of the negative sequence component in the supply voltages. Zero sequence components are not detected or compensated with the chosen control method.

System models are build in order to aid the design process and perform simulations on a DVR. The simulations have been compared with measurements in order to be able to test the validity of the models. A good agreement have been found between simulations and measurements, which indicates that the system is sufficiently modelled for the investigations.

The control of the LV-DVR is described and test results with the LV-DVR are

presented. Thereafter the control of HV-DVR is described and the tests of the HV-DVR are divided in high voltage/low power tests at Aalborg University and high voltage/low power tests at DEFU′s test facilities at Kyndby, Sealand. The stationary tests indicate that the DVR can compensate different kind of loads, however can non-linear load lead to oscillations in the line-filter of the DVR and thereby an increased harmonic distortion of the load voltages. The dynamic tests with the LV- and HV-DVR indicate a good compensation of symmetrical and non-symmetrical voltage dips. In most cases the DVR is capable of restoring the load voltages within 2 ms. During the transition phases load voltage oscillations can be generated and during the return of the supply voltages short time over-voltages can be generated by the DVR. Both of the described events can be a potential problem for sensitive loads.

During the thesis knowledge is gathered about power quality and power electronics for voltage quality improvements. In addition knowledge about the design and control of a DVR either connected at the low voltage or the medium voltage level.

During the Ph.D. an extensive amount of measurements are performed to test the operation of a DVR and the potential of a DVR. The testing at a high voltage/high power level at a realistic test location gave insight in placing series compensation equipment at this level. The level is characterized by having a high short circuit level and the system is inductor grounded. The DVR is installed to protect a medium voltage load consisting of a 10/0.4 kV distribution transformer and different low voltage loads. The voltage dips are generated by performing controlled short circuits in the grid and thereby the equipment is well verified with relative realistic voltage dips.

The conclusion is that the DVR is an effective apparatus to protect sensitive loads from short duration voltage dips. The DVR can be inserted both at the low voltage level and at medium voltage level. The series connection with the existing supply voltages makes it effective at locations where voltage dips are the primary problem. However, the series connection makes the protection equipment more complex as well as the continuous conduction losses and voltage drop.

Dansk resumé

Denne afhandling er resulatat af et del-projekt under forskningsprogrammet "Lokal Kompensering" på Aalborg Universitet. Ph.D. rapporten omhandler design og kontrol af en dynamisk spændingskompensator på engelsk kaldet en Dynamic Voltage Restorer (DVR). DVR′en er et seriekoblet apparat, der primært kan beskytte følsomme elforbrugere mod spændingsdyk og spændingsstigninger på lav- og mellemspændingsniveau.

I første kapitel af afhandlingen er elkvalitets parametre for en DVR undersøgt og effektelektronisk udstyr til kompensering af spændingsdyk beskrevet. Dernæst er DVR′ens virkemåde og opbygning beskrevet. Fordele og ulemper behandles ved at indsætte apparatet i distributionsnettet på henholdvis mellemspændings- og lavspændingsniveau. Forskellige topologier for DVR′en er undersøgt på konverter- og systemniveau. Efterfølgende er beskyttelsen af den seriekoblede DVR undersøgt og analyseret.

Design parametre for en DVR er behandlet og to prototyper DVR er designet og specificeret med en effekt på henholdsvis 10 kVA til indsættelse i 400 V lavspændingsnet og på 200 kVA til indsættelse i 10 kV mellemspændingsnettet. Kontrol af en DVR er behandlet, først med analyser af kontrol strategier og design af kontroldelen til de to prototyper.

Der er udviklet kontrol strategier til en DVR, der er primært fokuseret på en kompenseringsmetode, hvor fasen på lastspændingerne ikke ændres. Under normale spændingsforhold er DVR′en inaktiv uden switchninger for at minimere tabene, når et spændingsdyk detekteres går den aktiv ind og kompenserer for den manglende spænding. Kontrol delen er implementeret med en kombineret feedforward/feedback kontrol af spændingen over DVR′en for at en få hurtig svartid og en lastuafhængig spænding til den beskyttede last. Kontroldelen er implementeret i et roterende dq-system, der giver en god kompensering af den synkrone spændings komposant og en dæmpning af en evt. invers komposant til under en 1/4 af den eksisterende inverse spænding. Nulspændinger bliver ikke kompenseret med det anvendte kontrol princip.

Modellerne er implementeret i simuleringsprogrammet Saber og simuleringerne er sammenlignet med målinger for at undersøge evt. uoverensstemmelser i de anvendte modeller. Der er fundet god overensstemmelse mellem simuleringerne og målingerne, hvilket indikerer en tilfredsstillende modeldannelse af systemet.

Et kapitel indeholder resultater og observationer fra forsøg med lavspændings

DVR′en foretaget på Aalborg Universitet. Det efterfølgende kapitel indeholder resultater og observationer fra forsøg med mellemspændings DVR′en. Forsøgene med højspændings DVR′en er opdelt i høj spænding/lav effekt forsøg gennemført i Aalborg Universitets højspændingslaboratorium og dernæst forsøg med høj spænding/høj effekt forsøg gennemført på DEFU′s testanlæg beliggende ved Kyndby Værket på Sjælland.

De stationære forsøg viser at DVR′en kan kompensere forskellige lasttyper, dog kan meget ulineære laster forårsage kraftige oscillationer i DVR′ens net filter, hvilket giver en forvrængning af lastspændingerne.

De dynamiske forsøg med lavspændings- og højspændings DVR′en viser god kompensering af symmetriske og usymmetriske spændingsdyk af forskellige varighed, dybde og phasespring. På under 2 ms formår DVR′en at rekonstruere forsyningsspændingerne, ofte er de dynamiske forløb efterfulgt af svagt dæmpede svingninger på lastspændingerne, hvilket kan give overspændinger til lasten. Svingningerne afhænger af den tilkoblede last, DVR′s net filter og svingningerne kan begrænses ved at reducere svartiden for systemet.

I forbindelse med denne afhandling er der samlet omfattende viden omkring elkvalitet og effektelektronisk udstyr til forbedring af spændingskvaliteten på distributionsniveau. Derudover er der samlet viden omkring design og kontrol af en DVR tilsluttet enten lavspændings- eller mellemspændingsniveau.

Under Ph.D. forløbet er der gennemført et meget omfattende antal målinger af DVR′ens virkemåde og reelle potentiale. Afprøvningen af en højeffekt DVR på et realistisk mellemspændings testanlæg har givet en god indsigt i indsættelse af udstyr på dette niveau, hvor der kan forventes et højt kortslutningsniveau og et slukkespole jordet net. DVR′en blev under forsøgene installeret til beskyttelse af en mellemspændingslast, bestående af en distributions transformer med forskellige lavspændingslaster. Spændingsdykkene blev genereret ved kortslutsforsøg, hvilket har givet realistiske spændingsdyk og en meget god verificering af det udviklede udstyr.

Konklusionen på afhandlingen er at en DVR er en særdeles effektiv kompenserings metode til beskyttelse af spændingsfølsomme el-forbrugere mod kortvarige spændingsdyk. Indsættelse af apparatet kan gennemføres på både lavspænding- og mellemspændingsniveau. Det, der gør den effektiv til kompenseringen er, at den er seriekoblet med det eksisterende forsyningsnet og kan udnytte en ikke afbrudt forsyning, hvor spændingsdyk er det primære problem. Seriekoblingen gør samtidig kortslutningsudrustningen mere kompleks og de kontinuerlige tab og spændingsfald over DVR′en mere aktuelle.

Table of Contents

List of symbols and abbreviations

Capitals

C	Capacitance
E	Energy
H	Field Strength
I	RMS current
L	Inductance
N	Number of Windings
P	Active Power
Q	Reactive Power
R	Resistance
S	Apparent Power
T	Time Constant
U	RMS voltage
Z	Impedance
X	Reactance

Lowercase

$\boldsymbol{a}$	complex operator ($1\angle -120 = e^{-\frac{j2\pi}{3}}$)
d	Duty cycle
f	Frequency
i	Instantaneous current
l	Length
n	Transformer ratio
u	Instantaneous voltage
p	Instantaneous power
s	Laplace operator
t	Time

Uppercase greek

Ω	Resistance
Δ	Difference
θ	Angle

Lowercase greek

ω	Angular velocity
ϕ	Angle

Subscripts

a	Amplitude
af	Anti-aliasing filter
$base$	Base values
$begin$	Start conditions before a voltage dip
$bias$	Bias value
BV	Breakdown voltage
$charger$	Charger
$compensation$	Compensation for the DVR
$conv$	Converter
$controller$	Controller value
$core$	Iron core
d	d-value in the dq-coordinate system
dip	Dip
$diode$	Diode
$delay$	Hardware system delay
DC	DC side
DVR	DVR side
DVR, R	Resistive part of the DVR
DVR, Z	Impedance of the DVR
DVR, X	Reactive part of the DVR
$drop$	Voltage drop across the DVR
$energy\,converter$	Energy converter
end	End conditions after a voltage dip
f	Filter
$fault$	Value during fault
i	Integration part of the PO controller
$IGBT$	IGBT
$load$	Load side
$line, 10$	Impedance of 10 kV cable/wire
$line, 0.4$	Impedance of 0.4 kV cable/wire
$line - filter$	Line-filter
L	Inductor
$losses$	Losses
mag	Magnetization
max	Maximum value
min	Minimum value
$mean$	Mean value
nl	No load
on	On state conditions
off	Off state conditions
p	Proportional part of the PI controller
pri	Primary side
q	q-value in the dq-coordinate system
$rated$	Rated value

Subscripts

ref	Reference value
res	Resonance frequency
$ripple$	Ripple part
sat	Saturation value
sc	Short circuit
sec	Secondary side
$serie$	Series part
sw	Switching frequency
S	Switch
$shunt$	Shunt part
$supply$	Supply side
$supply, before$	Supply side before the insertion of the DVR
sum	Summation
$storage$	Energy Storage
$threshold$	Threshold conditions
tra	Transformer
tri	Triangular
$quant$	Quantization
$upstream$	Upstream
R, S, T	Phase R, S and T
$(d-)$	d negative sequence component
$(q-)$	q negative sequence component
$1, 2, 0$	Positive, negative and zero sequence system
$1f$	Filter inductor close to the converter
$2f$	Filter inductor close to the grid
$50/10$	Short circuit impedance of a 50/10 kV transformer
$10/0.4$	Short circuit impedance of a 10/0.4 kV transformer
α	α-value in the $\alpha\beta$-coordinate system
β	β-value in the $\alpha\beta$-coordinate system

Other

$\underline{U}$	Phasor value
$\overline{\overline{U}}$	Space vector value
U	RMS/DC value
u	Instantaneous value/ pu value
$\widehat{u}$	Peak value
$\mathbf{U}$	Vector/array notation
$\underline{\underline{\mathbf{A}}}$	Matrix notation

Abbreviations

$ASVC$	Advanced Static Var Compensation
BIL	Basic Isolation Level
$CUPS$	CUstom Power Systems
CSC	Current Source Converter
EBS	Electronic Bypass Switch
DVR	Dynamic Voltage Restorer
$FACTS$	Flexible AC Transmission Systems
GTO	Gate Turn Off
HV	High Voltage
$IGBT$	Insulated Gate Bipolar Transistor
$IGCT$	Integrated Gate Commutated Thyristor
LV	Low Voltage
PCC	Point of Common Coupling
PWM	Pulse Width Modulation
PQ	Power Quality
SOA	Safe Operation Area
THD	Total Harmonic Distortion
VSC	Voltage Source Converter
VQ	Voltage Quality

Chapter 1

Introduction

The research documented in this thesis relates to the design and control of power converters for CUstom Power Systems (CUPS). More precisely, focus is put on a special class of CUPS called a dynamic voltage restorer. Further information regarding the background and motivation for the current research on the dynamic voltage restorer is provided below. Also, the aims of the thesis is defined including an outline of the thesis.

1.1 Background and motivation

Power quality has been a topic of great interest for decades and several issues have triggered interest in monitoring and improving the power quality.

1.1.1 Power quality problems

A North American analysis of power quality included data collection from 1057 site-months at 112 locations from 1990 to 1994 [24] [65]. The measured data were analyzed and classified according to the standards of ANSI C84.1-1989 and the Computer and Business Equipment Measurement Association (CEBEMA) curve, illustrated in Fig. 1.1. More than 160,000 power disturbances were recorded over the four monitoring periods, which showed the unavailability of commercial power with an estimated mean value of 6.17 hour per site, per year. The power disturbances were categorized into four major events; low RMS events, high RMS events, transients and interruptions.

The transient events took a major part with around 60 %, while the interruption took minor part with around 1 %. The transients mainly came from capacitive switching operations, when the utility applies a large bank of capacitors on a high voltage power line to help to regulate voltage and to compensate for a poor power factor.

More than 26 % of the power disturbances came from the low RMS events, while 13 % of that came from the high RMS events. Some of the high RMS events were suspected to come from the incorrect setting of the transformers. The majority of the low RMS events (90 %) lasted less than one minute, while 4 % lasted more than thirty minutes.

In a power quality investigation in Denmark from November 1996 to May 1998

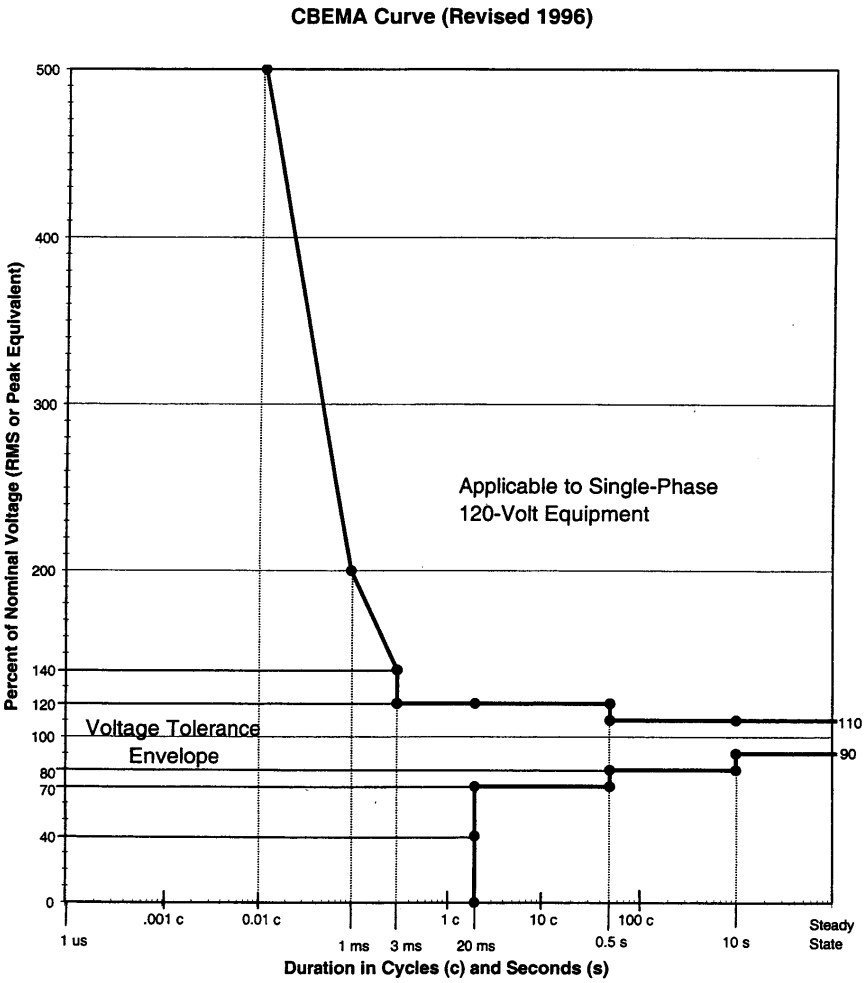


Figure 1.1: *The curve indicates a voltage tolerance envelope for single-phase 120 V equipment. The curve is also referred to as the CEBEMA/ITEC curve.*

around 200 delivery points was measured located in the distribution networks [37]. Medium and large industrial companies were excluded from the survey and more than 60% of the measuring proceeded in urban site. In total 700 data sets, each one of them representing one week of measuring, were analyzed by the new standards, EN 50160, IEC 1000-3-2 and the CBEMA3 curve. All interruptions longer than 3 minutes were removed from the data.

The data were categorized into the events of flicker, total harmonic distortion (THD), dip and swell, unbalance, DC voltage, and transients. Among these events, the dips appeared as a top issue. Around 30 % of the measurements were under 85 % of the nominal voltage, which must be avoided according to the European

Standard EN 50160.

Voltage dips can cause tripping of sensitive loads and the cost associated with short duration voltage dips can in some cases justify the insertion of power electronic equipment to compensate for the poor power quality [14].

1.1.2 New trends in power quality

Some of the issues, which have renewed and triggered the interest in power quality can be stated as:

- Higher demand on supreme power quality. IT-technology, automated production plants and commercial activities require a good and reliable power supply. [14]

- De-regulating and commercializing of the of electric energy markets has made power quality a parameter of interest to achieve a higher price per kilowatt, to increase the profit and share of the market. [32]

- Decentralization of the production of electricity with integration of alternative energy sources and small generation plants have increased certain power quality problems like surplus of power, voltage variations and flickers. [40]

- The improvements in the power electronics area and data processing capability have made improvement in power quality possible by means of relative cost-effective power electronic controllers. [4]

These trends have triggered interest in different types of power electronic controllers to mitigate power quality problems.

1.1.3 Power electronic controllers for voltage dip mitigation

There are two general approaches to mitigate power quality problems. One approach is to ensure that the process equipment is less sensitive to disturbances, allowing it to ride-through the disturbances [10]. The other approach is to install a custom power device to suppress or counteract the disturbances.

Many CUPS devices are commercially available in the market today such as, active power filters (APF), battery energy storage systems (BESS), distribution static synchronous compensators (DSTATCOM), distribution series capacitors (DSC), dynamic voltage restorer (DVR), power factor controller (PFC), surge arresters (SA), super conducting magnetic energy storage systems (SMES), static electronic tap changers (SETC), solid-state transfer switches (SSTS), solid-state circuit breaker (SSCB), static var compensator (SVC), thyristor switched capacitors (TSC) and uninterruptible power supplies (UPS).

Focusing on the compensation of voltage dips the number of devices can be narrowed down, and in [18] three types of devices have been compared, they are:

- UPS; Uninterruptible Power Supply. This could be a static converter with double conversion to mitigate most type of power quality disturbances. The topology is illustrated in Fig. 1.2.
- DVR; Dynamic Voltage Restorer is a series-connected device, which corrects the voltage dip and restore the load voltage in case of a voltage dip. The topology is illustrated in Fig. 1.3.
- SSTS; Solid State Transfer Switch to change from a faulted feeder to a healthy feeder. The topology is illustrated in Fig. 1.4.

Some of the advantages and disadvantages with the three solutions are summarized in Table 1.1.

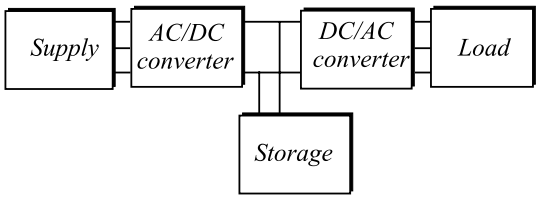


Figure 1.2: *Double conversion Uninterruptible Power Supply (UPS) with an energy storage.*

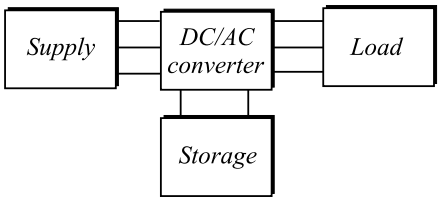


Figure 1.3: *Series connected dynamic voltage restorer (DVR) with an energy storage.*

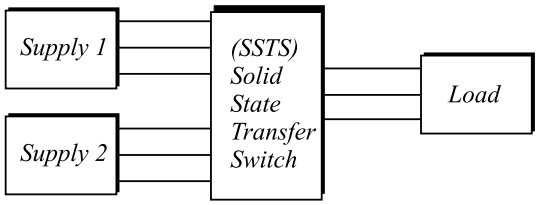


Figure 1.4: *Solid state transfer switch (SSTS) to switch between two supply lines.*

In [18] and economic comparison of the three solutions have been investigated regarding the expected savings, cost of solution per kVA, annual operating cost, total annual cost and a benefit/cost ratio. The SSTS has the highest benifit/cost ratio if a secondary independent feeder is present and if not the DVR is considered to be the most cost effective solution.

1.2 The dynamic voltage restorer

The dynamic voltage restorer is a series connected device, which by voltage injection can control the load voltage. In the case of a voltage dip the DVR injects the missing

Device	Advantages	Disadvantages
UPS	-Can compensate for interruptions.	-High cost per kW. -High losses.
DVR	-Low losses, injects only the missing part of the supply voltage. -Cost effective.	-Difficult to protect. -Cannot compensate for interruptions.
SSTS	-Low standby losses. -Low system cost if the second feeder is present. -Can compensate for interruptions and voltage dips. -High benifit/cost ratio if a second feeder independent feeder is present.	-Needs a second undisturbed feeder. -Difficult to ensure a undisturbed feeder. -Slow response.

Table 1.1: *Comparison of three solutions to protect sensitive loads from voltage deviations.*

voltage and it avoids any tripping the load. Fig. 1.5 illustrates the operation principle of a DVR.

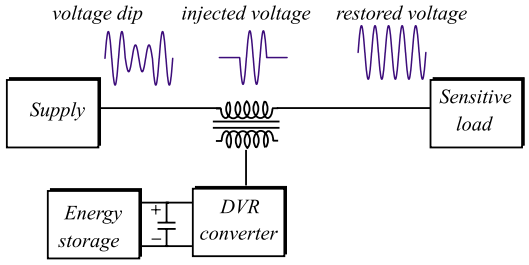


Figure 1.5: *Operation principle of a DVR. The DVR can by series voltage injection compensate for a voltage dip at the supply side and restore the load voltage for a sensitive load.*

The DVR is still very rarely inserted in the grid and only relative few devices have been inserted around the world. Commercial projects/products regarding the DVR have been reported in [1], [3], [14], [18], [23], [55], [72], [77], [60] and [76]. Most of the described projects include limited information about potential problems and a detailed description of the design and control aspects.

Even though the DVR is commercially available today, the DVR is not a matured technology and several areas regarding the design and control of this type of device are at the basic research level. The design of a DVR has been treated in [9], [48] and [66] with focus on the sizing of the voltage, power and current rating. DVR structures have been treated in [26] and [41] addresses the design considerations for

the line-filter for a DVR. The control strategies to limit the energy storage have been treated in [30] and [71] and in [29] some control issues regarding series compensation of unbalanced supply voltages have been treated.

Additionally, the DVR is a series connected device and one of the drawbacks with series connected devices is the difficulties to protect the device during short circuits and avoid interference with the existing protection equipment, which have been treated in [45] and [49].

1.3 Aims of the project

The project was originally entitled "Design and Control Power Converters for Custom Power Systems" and the title have been changed to "Design and Control of a Dynamic Voltage Restorer" where the aim of the project is narrowed down to:

Design and control of a dynamic voltage restorer inserted into the LV or MV distribution system with emphasis put on the mitigation of voltage dips.

The intended solution should be a solution, which could be offered by distribution companies or utilities to customers, which are willing to pay for a value-added power.

1.4 Outline of the thesis

The thesis consist of the following chapters after this introduction:

Chapter 2 Power quality and controllers for voltage dip mitigation gives an overview of power quality issues, which are relevant for the design and control of a dynamic voltage restorer with focus on voltage dips and interruptions.

Chapter 3 The dynamic voltage restorer gives an overview of the dynamic voltage restorer, the location of a DVR and the main system and converter topologies suited for a DVR.

Chapter 4 Design of a DVR deals with the main design process and parameters for the DVR. Included in the chapter are the specifications for the two developed DVRs.

Chapter 5 Control strategy for a dynamic voltage restorer describes the broad aspects of the control of a DVR including modulation and protection strategies for a DVR.

Chapter 6 Simulation of a DVR includes the modelling process and parameters included in the models. The models are implemented in the Saber simulation environment for simulation of the DVR to support the design process and the devel-

opment of the control methods. It also includes a verification of the system models with a comparison between simulations and laboratory measurements.

Chapter 7 Control of the LV-DVR includes control aspects and measurements from the LV-DVR, which have been implemented and tested in the laboratory.

Chapter 8 Control of the HV-DVR. On the basis of the LV-DVR a HV-DVR has been designed, constructed and tested. The chapter includes the operation of the HV-DVR and the testing of the HV-DVR at DEFU′s test facilities at Kyndby.

Chapter 9 Conclusion. Summarizes and concludes on the obtained results and sketches the perspectives and future work regarding the dynamic voltage restorer.

Appendix Includes copies of three already published papers during the Ph.D. work.

Chapter 2

Power quality and controllers for voltage dip mitigation

This chapter explains different issues of power quality with emphasis put on voltage dips and power quality issues, which are relevant for the dynamic voltage restorer. At the end of the chapter basic power electronic controllers for voltage dip mitigation are presented.

2.1 Voltage quality

The voltage quality has an impact on the control and design of a DVR and the DVR performance depends on the voltage quality at the location the DVR is inserted. In this section voltage harmonics, non-symmetry and voltage dips are treated to give a basic introduction to key voltage parameters for a DVR.

2.1.1 Voltage harmonics

Non fundamental voltage harmonics often appear at all levels in the electrical system. In relation with the DVR the harmonic content of the voltage before and after the DVR has major interest. Before the DVR, during no-load conditions the so called background distortion level can be measured and the level of distortion may influence the control of the DVR. The DVR can inject some harmonics and a vectorial addition with the background harmonics gives the resulting load voltage harmonics. The load voltage harmonics and the resulting load voltage distortion is an important evaluation parameter of the DVR performance. Sources to the distortion of the load voltages vary and the three main sources are:

- Background voltage harmonics; Background harmonics can easily be transferred to the load voltage side. During voltage injection harmonics from background distortion can be amplified or damped in the DVR control system. A supply voltage with a high harmonic content can complicate the synchronization to the supply and interfere with the DVR control.

- Harmonics injected by the DVR; The THD of the injected series voltage depends on the DVR hardware. E.g. converter topology, switching frequency,

modulation method, modulation index and filtering. Non-linear effects in the converter can even be a pure fundamental reference voltage inject harmonics, caused by non-linear effects in the DVR such as dead-time, transistor and diode voltage drop. [12].

- Non-linear load currents; A non-linear load current distorts the load voltage, which depends on the strength of the grid, the inserted DVR and the resulting impedance seen by load. This will include impedance in the DVR and the grid.

The voltage distortion U_{dis} can be calculated by a summation of the harmonic components, according to:

$$U_{dis} = \sqrt{\sum_{h=2}^{\infty} U_h^2} \tag{2.1}$$

and the Total Harmonic Distortion (THD) in percent can be calculated by:

$$U_{THD,\%} = \frac{U_{dis}}{U_1} 100\,\% \tag{2.2}$$

The DVR has the potential of improving the load voltage with respect to harmonic distortion, which means both to compensate for background harmonics and to compensate for the distorted load voltage caused by a distorted load current. This type of control is often termed as a harmonic blocking control or series harmonic filtering [25]. In this thesis the main focus is on the control of the fundamental voltage, but still the load voltage THD has to be within acceptable limits.

2.1.2 Non-symmetrical voltages

In a three-phase system the degree of symmetry is very important for a large group of three-phase loads. For a DVR non-symmetry implies hardware and control to be able to detect and correct the unbalanced supply and load voltages. The degree symmetry is a main performance criteria, which can be used to evaluate the DVR.

In the analysis of three-phase systems the decomposition to symmetrical components is useful. (2.3) shows the transformation from phase phasor values to symmetrical components.

$$\begin{bmatrix} \underline{U}_1 \\ \underline{U}_2 \\ \underline{U}_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \underline{U}_R \\ \underline{U}_S \\ \underline{U}_T \end{bmatrix} \tag{2.3}$$

The degree of symmetry is often evaluated as the negative sequence component divided by the positive sequence component, according to:

$$U_{non-symmetri,\%} = \frac{U_2}{U_1} 100\,\% \tag{2.4}$$

It is important to distinguish the non-symmetry from the four different sources:

- Background non-symmetry; Caused by other loads and can be a relative permanent condition, which can interfere with the DVR control and make the load voltages non-symmetrical.

- Non-symmetrical loads; A high non-symmetrical load can, because of the voltage drop across the DVR and the supply, lead to non-symmetrical load voltages.

- Non-symmetrical voltage dip; Short duration non-symmetry caused by a non-symmetrical fault incident in the grid.

- Non-symmetry generated by the DVR; A DVR is inserted to remove symmetrical and non-symmetrical voltage dips, but in some cases the DVR may increase the non-symmetry by voltage injection or by the voltage drop caused by non-symmetrical load currents.

Unlike harmonic compensation the compensation of non-symmetrical dips includes real power transfer from an energy storage, which normally is costly.

2.1.3 Voltage dips

Voltage dips are in many references stated as the most important and costly power quality problem [8] and [22], because of the high risk of tripping devices and a relative frequent occurrence. Voltage dips have been treated in a number of papers for instance [9], [21], [42], [67] and [79].

Symmetrical voltage dips

Voltage dips are usually caused by a short-circuit current flowing into a fault and a simplified model is illustrated in Fig. 2.1. Magnitude and phase of the voltage dip at the Point of Common Coupling (PCC) are determined by the fault and supply impedances, using the following equation [7]:

$$\underline{U}_{dip} = \underline{E}\frac{\underline{Z}_{fault}}{\underline{Z}_{fault} + \underline{Z}_{supply}} \tag{2.5}$$

By the impedance considerations the reduced magnitude and in some cases a phase jump can be estimated. Fig. 2.2 illustrates the used definitions of the voltage at the PCC with $\underline{U}_{dip}$ as the voltage during the dip and ϕ_{dip} is the phase jump at PCC. A simple symmetrical voltage dip can hence be characterized by the following three parameters:

- Voltage during dip (U_{dip})

- Dip duration (t_{dip})

- Phase jump (ϕ_{dip})

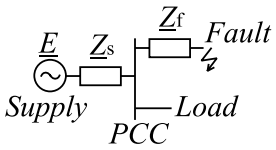


Figure 2.1: *Simplified circuit to calculate the voltage dip in a simple system.*

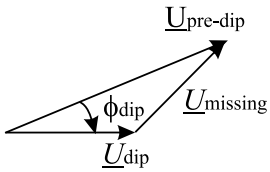


Figure 2.2: *Vector diagram of voltage dip with phase jump and the used definition of pre-dip voltage, dip voltage and missing voltage.*

The definition of a voltage dip with phasors can be stated as:

$$\underline{U}_{dip} = \underline{U}_{pre-dip} - \underline{U}_{missing} \tag{2.6}$$

The voltage dip is with this definition the voltage at PCC during the voltage dip and can be calculated as the pre-dip voltage (often the rated voltage) subtracted the missing voltage. In order to have full compensating, the DVR must inject the missing voltage. If the voltage dip is severe, —$\underline{U}_{dip}$— is low and a shallow voltage dip is characterized as a high —$\underline{U}_{dip}$— value.

Non-symmetrical voltage dips

A very large distribution of voltage dips recorded in a EPRI survey are non-symmetrical [56]. About 68 % resulted from single-phase faults, 19 % from two-phase faults and only 13 % from three-phase faults. Thereby approximately 87 % of the voltage dips were non-symmetrical.

These facts have a considerably impact on the design and control of DVRs, and the voltage dip distribution could justify the design of the DVR for non-symmetrical voltage dips, and therefore focus performance evaluation on the compensation of non-symmetrical dips. Voltage dips are caused by different kinds of faults in the grid. The faults can be categorized as:

1. Three-phase faults.
2. Three-phase faults with ground connection.
3. Two-phase faults.
4. Two-phase faults with ground connection.
5. Single-phase faults.

In a direct or effective grounded systems 3-5 can lead to a non-symmetrical voltage dip and in isolated or high impedance grounded system 3-4 can lead to a non-symmetrical voltage dip. Fig. 2.3 illustrates the voltage dips associated with the faults in a direct grounded system.

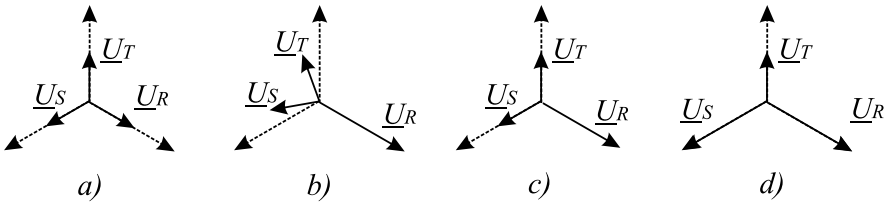


Figure 2.3: *Voltage dips from short-circuit faults. a) Voltage dip from three-phase fault, b) voltage dip from two-phase fault, c) voltage dip from two-phase fault with ground connection and d) voltage dip from single-phase fault.*

The propagation through transformers and the grounding used at each voltage level is essential for the propagation of the voltage dips associated with faults. In the following example the four characteristic faults have been applied at a high voltage level with a direct grounded system and the system is illustrated in Fig. 2.4. From HV to MV a Dy transformer is assumed to be used and the MV-level is inductor grounded. Finally, the connection to LV is made with a Dy transformer and the LV-level direct grounded.

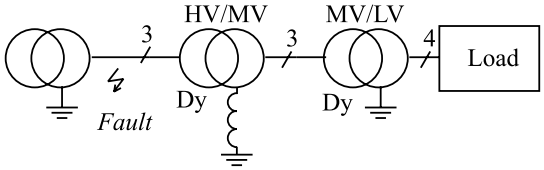


Figure 2.4: *Grid system used to estimate how a fault on the HV-level can propagate to MV and LV-levels.*

For the two-phase fault without the ground connection, the two faulted phases are reduced in voltage and the angle between them are reduced at the high voltage side. At the medium side one of the phases are down to 50 %, nevertheless, the low voltage side is only reduced to 66 %. Table 2.1 illustrates the associated phase voltages and symmetrical component voltages for a two-phase fault at the HV-level and the propagation to MV- and LV-levels.

Voltage	**High Voltage**	**Medium Voltage**	**Low Voltage**
$\underline{U}_R$	$1.00 \quad \angle 0°$	$0.50 \quad \angle 0°$	$1.00 \quad \angle 0°$
$\underline{U}_S$	$0.66 \quad \angle -139°$	$0.90 \quad \angle -106°$	$0.66 \quad \angle -139°$
$\underline{U}_T$	$0.66 \quad \angle 139°$	$0.90 \quad \angle 106°$	$0.66 \quad \angle 139°$
$\underline{U}_1$	$0.75 \quad \angle 0°$	$0.75 \quad \angle 0°$	$0.75 \quad \angle 0°$
$\underline{U}_2$	$0.25 \quad \angle 0°$	$0.25 \quad \angle 180°$	$0.25 \quad \angle 0°$
$\underline{U}_0$	$0 \quad \angle 0°$	$0 \quad \angle 0°$	$0 \quad \angle 0°$

Table 2.1: *Two-phase fault at the HV-side and the voltage propagation down to the LV-side.*

At a two-phase fault with ground connection each phase voltage is reduced in magnitude. Table 2.2 illustrates the associated phase voltages and the symmetrical component voltage for a two-phase fault with ground connection at the HV-level and the propagation to MV- and LV-levels. Table 2.3 illustrates the associated phase

Voltage	High Voltage	Medium Voltage	Low Voltage
$\underline{U}_R$	$1.00 \quad \angle 0°$	$0.50 \quad \angle 0°$	$0.83 \quad \angle 0°$
$\underline{U}_S$	$0.50 \quad \angle -120°$	$0.76 \quad \angle -109°$	$0.60 \quad \angle -134°$
$\underline{U}_T$	$0.50 \quad \angle 120°$	$0.76 \quad \angle 109°$	$0.60 \quad \angle 134°$
$\underline{U}_1$	$0.67 \quad \angle 0°$	$0.67 \quad \angle 0°$	$0.67 \quad \angle 0°$
$\underline{U}_2$	$0.17 \quad \angle 0°$	$0.17 \quad \angle 180°$	$0.17 \quad \angle 0°$
$\underline{U}_0$	$0.17 \quad \angle 0°$	$0 \quad \angle 0°$	$0 \quad \angle 0°$

Table 2.2: *Two-phase fault at the HV-side with ground connection and the voltage propagation down to the LV-side.*

voltages and symmetrical component voltages for a single-phase fault at the HV-level and the propagation to the MV and LV-levels. Fig. 2.5 illustrates graphically

Voltage	High Voltage	Medium Voltage	Low Voltage
$\underline{U}_R$	$0.50 \quad \angle 0°$	$1.00 \quad \angle 0°$	$0.67 \quad \angle 0°$
$\underline{U}_S$	$1.00 \quad \angle -120°$	$0.76 \quad \angle -131°$	$0.93 \quad \angle -111°$
$\underline{U}_T$	$1.00 \quad \angle 120°$	$0.76 \quad \angle 131°$	$0.93 \quad \angle 111°$
$\underline{U}_1$	$0.83 \quad \angle 0°$	$0.83 \quad \angle 0°$	$0.83 \quad \angle 0°$
$\underline{U}_2$	$0.17 \quad \angle -180°$	$0.17 \quad \angle 0°$	$0.17 \quad \angle -180°$
$\underline{U}_0$	$0.17 \quad \angle -180°$	$0 \quad \angle 0°$	$0 \quad \angle 0°$

Table 2.3: *Single-phase fault at the HV-side and the voltage distribution down to the low voltage side*

the faults transformed to the MV voltage level.

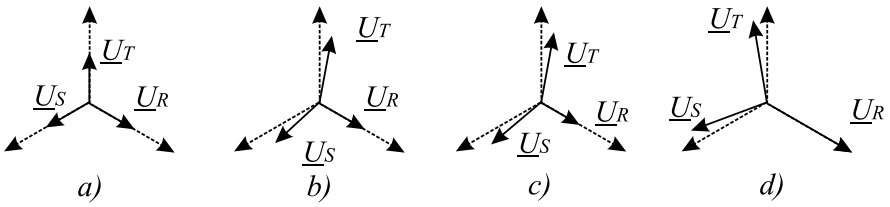


Figure 2.5: *Voltage at the MV-level from faults at the HV-level. a) Voltage dip from three-phase fault, b) voltage dip from two-phase fault, c) voltage dip from two-phase fault with ground connection and d) voltage dip from single-phase fault.*

Non-symmetrical voltage dips very often include a phase shift of two phases and dependent on the circumstances the voltage phasors come closer or more separated. This phase-shift, which is very different from the phase jump from symmetrical voltage dip, must be detected and compensated by the DVR to restore the load voltages.

The magnitude to be injected by a dynamic voltage restorer is important, because the DVR has a finite voltage rating and it sets a limit for the type of non-symmetrical dips, which can be compensated. For some DVR topologies the line voltage values are of greater interest. The positive sequence component is also useful for evaluating the expected power drain for a non-symmetrical voltage dip, because for a symmetrical load current only the injection of positive sequence results in a power drain for the DVR storage.

Voltage dip duration

Voltage dips are mainly caused by faults in the grid and the fault clearing time of various protection devices decides the dip duration time. Fig. 2.6 illustrate how the faults typically are located in which the numbers are referring to the following origin [10]:

1. Transmission system faults.
2. Remote distribution system faults.
3. Local distribution system faults.
4. Starting of large motors.
5. Short interruptions.
6. Fuses.

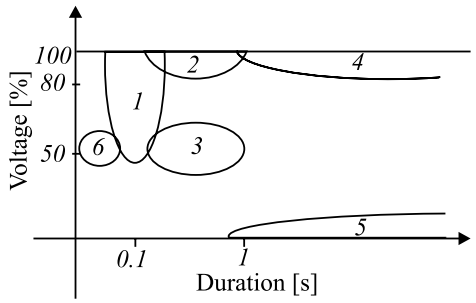


Figure 2.6: *Voltage dips of different origin in a magnitude-duration plot. 1 - transmission faults, 2 - remote distribution fault, 3 - local distribution fault, 4 - starting of large motors, 5 - short interruptions and 6 - fuses. [10]*

2.2 Interruptions

In the European standard EN 50160 two terms are used:

- Long interruptions: longer than three minutes.
- Short interruptions: up to three minutes.

Interruptions are typically caused by different types of faults e.g. malfunction of protection equipment or lightning. In a system without redundancy a fault often leads to a long interruption, which requires manual intervention. Short interruptions are often caused by automatic reclosing after a fault. Short interruptions below three minutes are normally considered a voltage quality problem. Interruptions are a severe power quality problem, but in a wide range of industrial countries

interruptions occur very rare, because of redundancy and high maintenance of the grid.

A correlation can be found between interruptions and voltage dips. Taking measures to decrease the number of interruptions may increase the number of voltage dips. For instance by having a meshed distribution system (high redundancy) the number of interruptions go down, but the voltage dips can occur more frequently and be more severe [10].

During an interruption a DVR can not improve the load voltage and in some cases the DVR can be endangered or endanger neighboring loads during an interruption [43]. The DVR needs a connection with the supply and if the location of interest has a high number of interruptions an UPS solution is necessary to improve the power quality.

2.3 Power electronic controllers for voltage dip mitigation

The section gives a short survey of two main types of controllers to mitigate voltage dips also treated in [57]. First, shunt controllers are treated, thereafter series controllers and finally combined series/shunt controllers.

2.3.1 Shunt controllers

Shunt controllers have the widest use to stabilize the voltage at a certain point and if the controllers are equipped with a VSC the devices are termed Static Compensators (STATCOM), Static Condensers (STATCON) or Advanced Static Var compensators (ASVC) [31], [73].

Shunt devices are effective to compensate small voltage variation, which can be controlled by reactive power injection. The ability to control the fundamental voltage at a certain point depends on the impedance to the supply and the power factor of the load. The compensation of a voltage dip by current injection is very difficult to achieve, because the supply impedance are usually low and the injected current has to be very high to increase the load voltage. Compensation of a voltage dip with a shunt controller is illustrated in Fig. 2.7. Considering a case with a

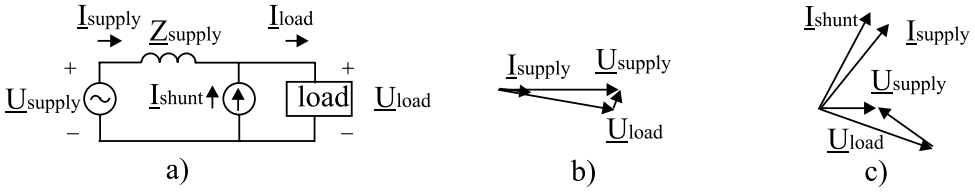


Figure 2.7: *The use of a shunt converter to compensate for a voltage dip. a) circuit diagram, b)vector diagram for normal condition, c) vector diagram for compensation of a voltage dip.*

supply voltage with 1 pu voltage and a supply impedance of 0.1 pu inductively. If

the active load varies from 0 to 1 pu the load voltage vary from 1 - 0.995 pu. Inserting a shunt converter with 1 pu current injection the load voltage can be controlled in the range of approximately 0.9 - 1.1 pu. At a 0.5 pu voltage dip the shunt converter must inject a high reactive current to stabilize the load voltage at 1 pu. Injecting approximately 5 pu reactive current it is possible to compensate a 0.5 pu voltage dip.

Injecting active power by the shunt converter will have a poor effect on the load voltage. If the shunt controller supplies the load with active power, it still has to inject approximately 5 pu. reactive current to stabilize the load voltage. This method requires stored energy and a more than 5 pu rated shunt converter.

Breaking the connection to the supply during a voltage dip can keep the rating of the shunt converter to approximately 1 pu and deliver all the active and reactive power needed by the supply and re-synchronize with the grid, when the voltage dip is over. This simple example indicates the poor effectiveness to compensate voltage dips with shunt controllers.

2.3.2 Series controllers

The series controllers for control of the fundamental voltage are termed as a series connected PWM regulator in [17], a static series regulator in [27], [28] and [33], but mostly the devices are termed dynamic voltage restorers. If the device only injects reactive power the device can be termed as series var compensators [34].

Taken the same simplified model of a supply and a load, the inserting of a series controller to support the load. A 0.5 pu voltage dip can by a series device be restored by a 0.5 pu DVR and only 0.5 pu of the energy absorbed by the load has to be supplied by the DVR. The supply continues to be connected and no re-synchronization is necessary as it is the case with the shunt connected converter.

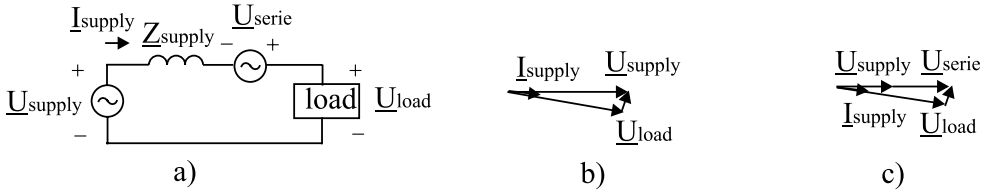


Figure 2.8: *The use of a series controller to compensate for a voltage dip. a) circuit diagram, b) vector diagram for normal condition and c) vector diagram for compensation of a voltage dip.*

2.3.3 Combined shunt and series controllers

The combination of series and shunt controllers to control the load voltage are often referred to as a unified power quality conditioner (UPQC) [25] or line-interactive uninterruptible power supply (UPS) [53].

Fig. 2.9 illustrates the two possible connection methods. The installed rating tends to increase with unified approaches, but the performance can also be improved and some of the benefits with both shunt and series controllers can be utilized. Both controllers can exchange reactive power with the grid and active power can be transferred between the controllers. Most important the energy storage can be significantly reduced with unified approaches.

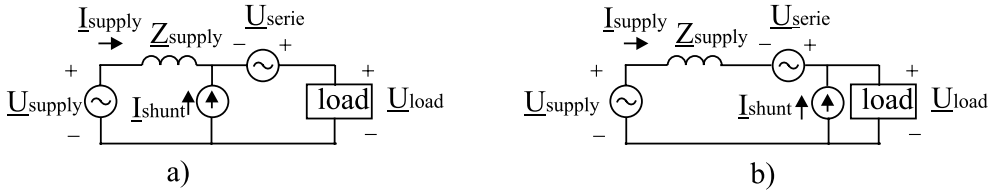


Figure 2.9: *Unified controllers. a) shunt-series controllers and b) series-shunt controllers.*

2.4 Summary and conclusion

In this chapter power quality issues for a DVR has been treated and the focus has been on voltage dips, interruptions and power electronic controllers for voltage dip mitigation.

- Voltage dips can in many cases be the most severe power quality problem, because they can occur very frequently and lead to a load tripping. Voltage dips depth, duration and phase jump depend on the location of the fault and the protection equipment used.
- Voltage dip can be caused by faults at all voltage levels. The voltage dip size and symmetry depend mainly on the type of fault, the grounding principles used at the faulted voltage level and the transformer connections between the fault and the load of interest.
- The DVR cannot be used during an interruption and other mitigation devices must be applied if the number of interruptions is high.
- The mitigation of voltage dips can be achieved with power electronic controllers. The shunt controller can make some voltage correction with reactive power injection, but a compensation of voltage dips is difficult to achieve with a shunt controller. The series controller is recognized as a cost effective solution for voltage dip mitigation. Combining the shunt/series controllers the installed rating increases and the performance can be improved at the expense of higher costs.

Chapter 3

The dynamic voltage restorer

First the chapter describes the basic elements of a DVR and the expected location of a DVR. Thereafter, different DVR system topologies are presented with respect to topologies and methods to have active power access during voltage dips. Finally protection issues are discussed.

3.1 The basic elements of a DVR

Fig. 3.1 illustrates some of the basic elements of a DVR, which are:

- Converter; The converter is most likely a Voltage Source Converter (VSC), which Pulse Width modulates (PWM) the DC from the DC-link/storage to AC-voltages injected into the system.
- Line-filter; The line-filter is inserted to reduce the switching harmonics generated by the PWM VSC.
- Injection transformer; In most DVR applications the DVR is equipped with injection transformers to ensure galvanic isolation and to simplify the converter topology and protection equipment.
- DC-link and energy storage; A DC-link voltage is used by the VSC to synthesize an AC voltage into the grid and during a majority of voltage dips active power injection is necessary to restore the supply voltages.
- By-pass equipment; During faults, overload and service a bypass path for the load current has to be ensured. Illustrated in Fig. 3.1 as a mechanical bypass and a thyristor bypass
- Dis-connection equipment; To completely disconnect the DVR during service etc.

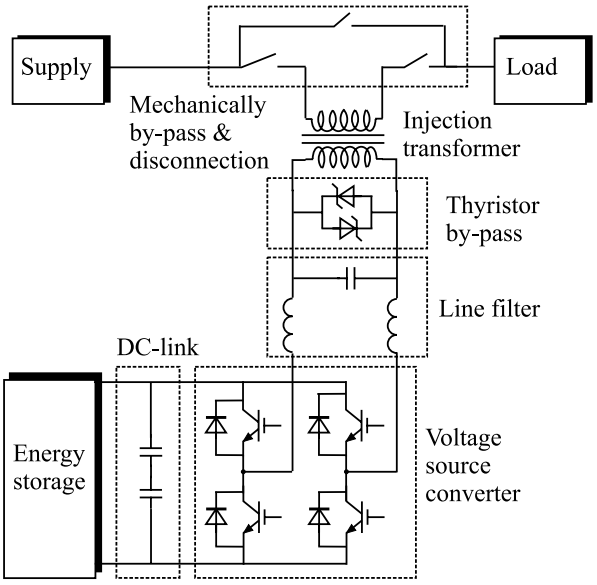


Figure 3.1: The basic elements of a DVR in a single-phase representation.

3.2 Location of the DVR

The DVRs intended location is either at the MV distribution level or at the LV-level close to a LV customer. This chapter discusses the different perspectives with the two alternatives.

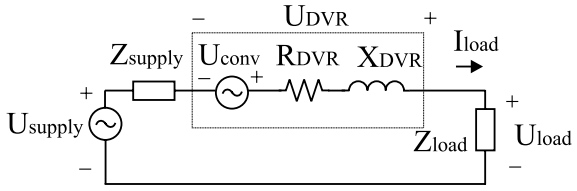


Figure 3.2: Single-phase simplified model of the DVR.

A simplified model of the DVR is illustrated in Fig. 3.2 and can help to evaluate the best location of a DVR. The DVR can be represented as an ideal voltage source (U_{conv}) with an inserted reactive element (X_{DVR}), which mainly represents the reactive elements in the injection transformers and line filters, and an inserted resistive element (R_{DVR}), which represents the losses in the DVR. The size of the inserted impedance is closely related to the DVR voltage rating (U_{DVR}) and the DVR power

rating (S_{DVR}) according to:

$$X_{DVR} = \frac{U_{DVR}^2}{S_{DVR}} \cdot u_{DVR,X} \tag{3.1}$$

$$R_{DVR} = \frac{U_{DVR}^2}{S_{DVR}} \cdot u_{DVR,R} \tag{3.2}$$

$$\underline{Z}_{DVR} = \frac{U_{DVR}^2}{S_{DVR}} \cdot u_{DVR,Z} \tag{3.3}$$

$$u_{DVR,Z} = u_{DVR,R} + j u_{DVR,X} \tag{3.4}$$

$u_{DVR,Z}$ depends on the type of transformer used, the line-filter, losses in the VSC etc. A DVR with high injection capability (high U_{DVR}) and the ability only to protect a small load (low S_{DVR}) has a large equivalent DVR impedance ($\underline{Z}_{DVR}$).

Going from a LV-level DVR to a higher voltage level DVR the pu value of the reactance ($u_{DVR,X}$) tends to increase, and the pu value resistance ($u_{DVR,R}$) tends to decrease.

A high resistive part increases the energy, which should be dissipated from the DVR and the costs associated with the losses. A high total inserted DVR impedance increases the potential load voltage distortion and load voltage fluctuations if the load is non-linear and/or has a fluctuating load behaviour.

3.2.1 The DVR applied to the MV-level

Connected to the MV-level, the DVR protects a large consumer or a group of consumers. The insertion of a DVR in the medium voltage distribution system is illustrated in Fig. 3.3. Inserting a large DVR at the MV-level will only increase the supply impedance for a LV load slightly. Assuming an infinite busbar at the 50 kV level, the impedance for a LV load consists of the summation of impedances from the 50/10 kV transformer, cables and overhead lines at the 10 kV level, the 10/04 kV distribution transformer and finally LV cables to the LV load. The impedance and the increase in impedance by inserting a DVR can be expressed as:

$$Z_{supply,before} = Z_{50/10} + Z_{line,10} + Z_{10/0.4} + Z_{line,0.4} \tag{3.5}$$

$$Z_{supply,after} = Z_{DVR} + Z_{supply,before} \tag{3.6}$$

$$Z_{increase,\%} = \frac{Z_{DVR}}{Z_{supply,before}} 100\% \tag{3.7}$$

For a LV load the dominating impedance is most likely the LV line impedance ($Z_{line,0.4}$) and the impedance of the distribution transformer ($Z_{10/0.4}$). Protecting a large MV load close to the DVR, the increase in impedance experienced by the load can be significant. Inserting one high rated DVR at the MV-level has certain advantages:

- The increased impedance inserted with a DVR seen by a LV load can be relative small if a large DVR is placed at the MV-level.

- The MV distribution systems in Denmark are operated as a three wire system with isolated or inductor grounded system. In such a system injection of positive and negative sequence system is sufficient and a more simple DVR topology and hardware can be used.
- The costs per MVA to protect are expected to be lower if one large central DVR is located at the medium voltage level instead of decentralized low voltage units.

Some of the disadvantages can be summarized to:

- Protecting a large load may require a medium voltage DVR otherwise the losses in the DVR will be to high.
- During ground faults in the MV system the phase to ground voltages can increase with $\sqrt{3}$, and a higher isolation level of the injection transformers must be ensured.
- A part of the DVR rating may be utilized on loads, which do not require a supreme voltage quality.
- The DVR is connected to a voltage level, which requires a high isolation level and the short circuit level is high.

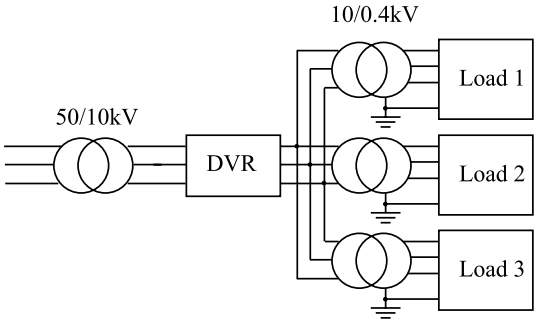


Figure 3.3: *DVR located at the medium voltage distribution system.*

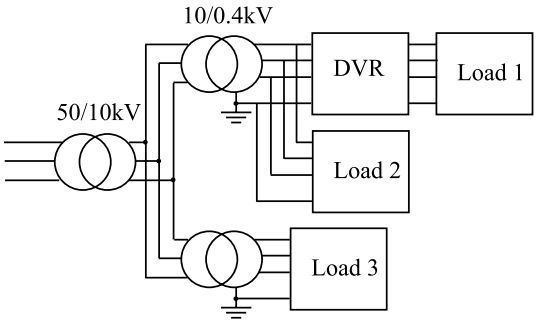


Figure 3.4: *DVR located at the low voltage distribution system.*

3.2.2 The DVR applied at the LV-level

The insertion of a DVR at the low voltage four-wire 400 V level is illustrated in Fig. 3.4. The increase in impedance by insertion of a small rated DVR can be significant for the load to be protected from voltage dips. Thereby, the percent change in the impedance ($Z_{increase,\%}$) in (3.7) can be increased by several hundred percent. Inserting a DVR at LV-level has certain advantages:

- The DVR can be targeted more specifically at voltage dip sensitive loads.
- A majority of electric customers have only access to the LV-level and the DVR can both be placed by the customer at the customer domain or by the utility at the utility domain.
- The short-circuit level is significantly decreased by the distribution transformer and the DVR is easier to protect.

and the disadvantages with a LV solution are:

- The impedance increase after the insertion of the DVR for the protected load can be large, which may influence the site short circuit level and protection. An increased load voltage distortion and load voltage variation can be expected, which may be caused by non-linear and time varying load currents.
- Voltage dips with a zero sequence voltage component can appear and in order to be able to compensate loads connected between phase and neutral adequate, the DVR hardware and control should be able to generate positive, negative and zero sequence voltages.

3.3 DVR topologies

In this chapter the main topologies for DVRs are discussed with focus on methods to connect the DVR to the grid, converter topologies suited for DVRs and methods to ensure active power during the voltage dip mitigation. The section includes a survey and comparison of the different topologies for DVRs, which also have been treated in [5], [50] and [51].

3.3.1 Converter connection

The DVR is going to inject a voltage in series with the supply, which requires either galvanic isolation to the VSC or letting the VSC float at the potential of the supply voltages. Two different approaches are here considered, referred to as a transformer connected converter or a direct connected converter.

Transformer connected converter

Using a low frequency transformer (50/60 Hz) to transfer the VSC voltages to series injected voltages is the most common method, which is illustrated in Fig. 3.5a. In [63] it has been tried to replace the low frequency transformer with a high frequency transformer link together with a floating cyclo-converter based DVR. Ensuring the galvanic isolation with a low frequency transformer the following advantages can be obtained:

- The transformer ratio can be chosen rather arbitrarily, thereby the transformer can be scaled to a standard industrial converter voltage. Either up or down in voltage to achieve the best performance.

- The transformer can be used to ensure the DVRs Basic Insulation Level (BIL).
- The transformer can be used as a part of an important line-filter. Either as the first inductance close to the converter or as an inductor close to the load in a LCL-filter configuration.
- A relative simple converter topology with six active switches can be used to inject the voltages into the grid.
- One DC-link is sufficient, which simplify the DC-link, charging circuit and the DC-link voltage control.

Some of the disadvantages, when using injection transformers are:

- The series injection transformers are not off the shell transformers, because the design differs from mass produced shunt transformers and the voltage rating varies with the required injected voltages.
- The transformers increase losses, have a non-linear behaviour and can be a limiting factor regarding the bandwidth of the DVR system.
- The low frequency injection transformers are bulky with high cost, weight and volume.

The three transformer connection reported for DVRs are open star/open star single-phase transformers, open star/delta transformers and open star/star transformers.

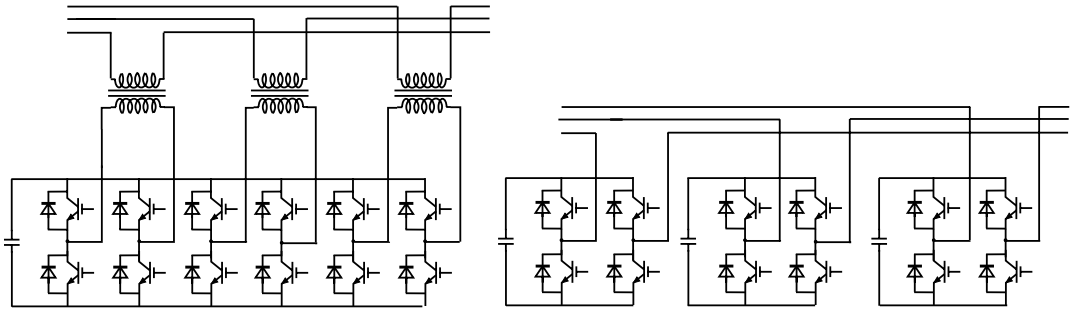


Figure 3.5: *Different converter connection methods. a) DVR including an injection transformer to ensure galvanic isolation between the supply and VSC. b) transformer-less DVR, directly connected to the grid and a separate DC capacitor for each phase leg.*

Directly connected converter

Series injection with transformer-less converters has been reported for VAr compensator in [34]. DVRs using a directly connected converter are stated as an idea in [32] and the concept is used in [63]. Technically, direct connection is the best

suited for series devices, which only exchanges reactive power with the grid, because the transfer of power require charging of three separate DC-links. Fig. 3.5b shows a directly connected DVR converter and the advantages with a directly connected DVR converter are:

- The performance is expected to be improved, because the bandwidth is not decreased by the transformer and the non-linear effects and voltage drop caused by the transformers are removed.
- The bulky transformers can be avoided. A compact DVR solution can be developed with low volume, low weight etc.

Some of the disadvantages are:

- Protection of the power electronics is more complicated and Basic Insulation Level (BIL) must be ensured more actively.
- The converter topology has to be more complex and a high isolation to ground has to be ensured.
- The converter topologies are more complex and a higher number of components is expected to be used.

3.3.2 Converter topologies

The voltage source converter is a main building block for a DVR and choosing a topology suited for the application is essential regarding system performance. The DVR is connected in series and the impedances inserted lead to unwanted voltage drops and losses. The analysis of converter topologies have been limited to include transformer connected converters based on voltage source converters with hard switching and symmetric topologies. The main focus is to describe converter solutions, which are suited for a DVR. The basic converter topologies, which are presented, include:

- Half bridge topologies.
  - Half bridge converter with an open star/star transformer connection - Topology I.
  - Half bridge converter with an open star/delta transformer connection - Topology II.
- Full bridge topology.
  - Full bridge converter with an open star/open star transformer connection - Topology III.
- Multilevel topology.

– Half bridge three level converter with an open star/delta transformer connection -
Topology IV.

The following parameters have been included in the investigation and comparison of the individual topologies:

- The effective switching frequency, which influences the size of the line-filter, and by having a high effective switching frequency the line-filter can be reduced.
- The number of devices in the current path in order to estimate losses and resistive voltage drop across the DVR.
- The number of active and passive devices in the converter in order to have a high reliability, low cost and complexity in the system.
- Ability to handle zero sequence currents and injection of zero sequence voltages. Compensating zero sequence voltages requires individual control of each phase and only certain topologies can comply with this.
- Utilization of the DC-link voltage.
- Control of the DC-link voltage and methods to transfer active power to the DC-link.

These above parameters are very relevant converter parameters for DVR applications and they are investigated for the four converter topologies.

Half bridge converter with an open star/star transformer connection - Topology I

The half bridge converter, illustrated in Fig. 3.6a and used in [33], uses only six switches to generate the three injected voltages and it has three switches in the current path. The converter can only generate two voltage levels and the midpoint of the DC-link is connected to the star point of the series transformers in order to be able to inject a zero sequence voltage into the system. The DC-link voltage must be actively balanced to avoid unbalanced DC-link voltage. Issues with zero sequence components have been treated in [19].

Half bridge converter with an open star/delta transformer connection - Topology II

The half bridge converter, illustrated in Fig. 3.6b and used in [49], can only inject positive and negative sequence components into the system, which is sufficient for a number of applications. Zero sequence currents flowing in the grid will circulate in the delta winding of the transformer. The DC-link voltage is very easy to control and it does not need any active balancing. The utilization of the DC-link can be

higher compared to topology I by adding a third harmonic zero-sequence voltage in the reference to each phase. The converter line voltage has three voltage levels, which are injected into the grid.

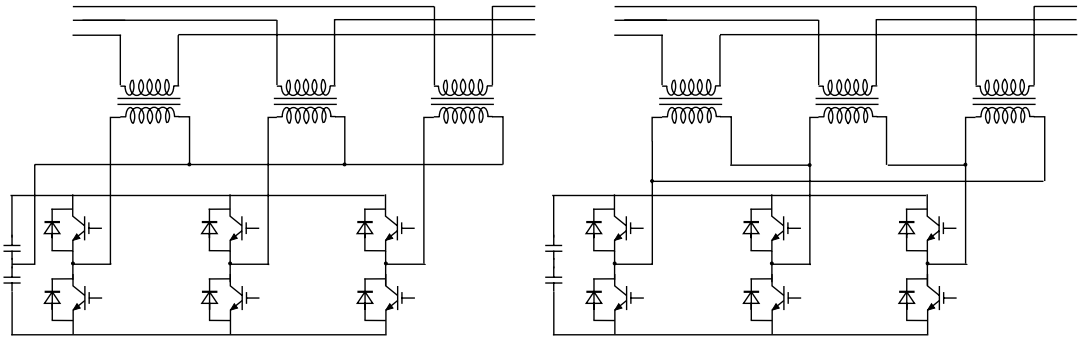


Figure 3.6: *Converter topologies. a) Half bridge converter topology I with the possibility to inject a zero sequence voltage and b) half bridge converter topology II with delta/open star transformer connection.*

Full bridge converter with an open star/open star transformer connection - Topology III

The full bridge converter illustrated in Fig. 3.7a and used in [32], uses 12 active switches and always has two power switches per phase in the current path. With a uni-polar switching scheme the converter can generate three voltage levels and the effective switching frequency is the double of the actual switching frequency. This gives less voltage distortion and the size of the line-filter can be decreased. The full bridge converter can inject zero sequence voltage components and it does not need a split DC-link. Six devices are always in the current path and the DC-link voltage is simple to control, but cannot be utilized as good as topology II, because a third harmonic zero sequence components would be transferred into the grid.

Half bridge three level converter with an open star/delta transformer connection - Topology IV

Fig. 3.7b illustrates the three level converter, also referred to as a neutral point clamped converter [46], for a DVR. It has not been reported used for a DVR application, but it could be the first step towards a multilevel converter used for a DVR application and it is included in the comparison of different systems to illustrate some of the benefits with multilevel topologies. The benefits with multilevel topologies are that higher voltages voltages can be synthesized or power devices with lower device ratings can be used, reduced THD and reduced filter requirements.

An overview of Multilevel topologies is given in [39] and [68]. Besides the diode clamped topologies other generic structures of multilevel converters could be used

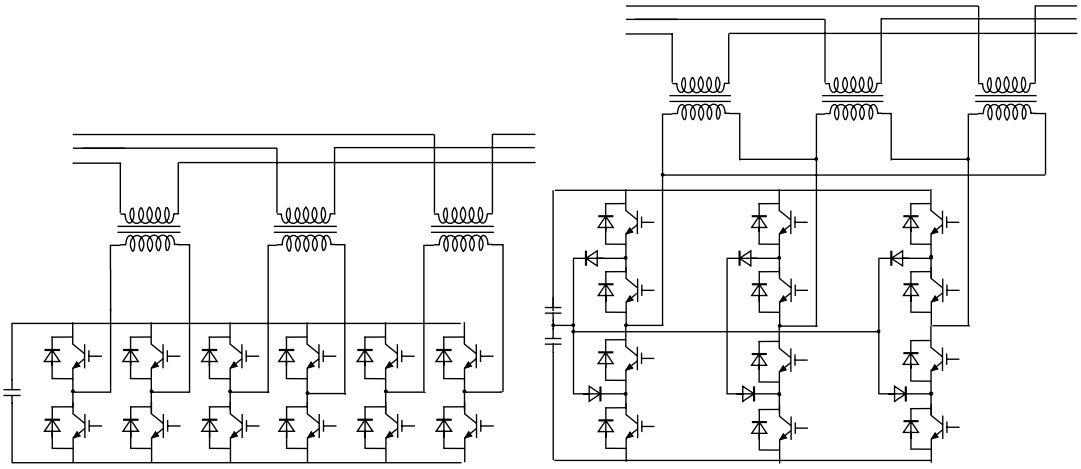


Figure 3.7: *Converter topologies. a) Full bridge converter topology with the possibility to inject a zero sequence voltage and b) three level converter (Neutral Point Clamped) with delta/open star transformer connection.*

e.g. multilevel converters with distributed capacitors or cascaded single-phase full bridge converters.

In the three level converter each phase can be synthesized with three levels and due to the delta transformer the voltage at the primary side is synthesized with five voltage levels. The converter cannot inject zero sequence voltages with the used transformer connection. The three level converter has six neutral point clamping diodes and 12 IGBTs and 12 diodes in the three phase legs.

Comparison of the converter topologies

In this non-detailed comparison of the four topologies some of the main differences can be seen. Zero sequence voltage injection can only be ensured by topologies I and III and it has a negative influence on the DC-link utilization. The more complex topology III and IV have higher component count and components in the current path, which both have a negative influence on complexity and losses. Some of the drawbacks are balanced by the higher power handling capability and that the effective switching frequency is doubled. The line filters can be reduced, which has a positive effect on the size of the passive filters and the filter losses and costs.

Important parameters for the four topologies are tabulated in Table 3.1 and the advantages and disadvantages are summarized in Table 3.2.

The increased number of levels has the main advantage of a decrease in the line-filter size. For the relative simple two and three level topologies the main voltage drop are expected to be caused by the line-filter and the injection transformers, but by increasing the number of levels the line-filter can be reduced and the voltage drop across the semiconductor devices will have a greater importance.

Topology	IGBT/diodes components	Output power*	Components in current path	1. harmonic component	Voltage levels
I	6/6	1	3	f_{SW}	2
II	6/6	1	3	f_{SW}	3
III	12/12	2	6	$2f_{SW}$	3
IV	12/18	2	6	$2f_{SW}$	4

Table 3.1: *Comparison of converter topologies for DVRs.*
* *A higher DC-link utilization has not been used in the output power considerations.*

Topology	Zero voltage injection	DC-link control	DC-link utilization
I	+	-	-
II	-	+	+
III	+	+	-
IV	-	-	+

Table 3.2: *Comparison of converter topologies for DVRs. (+) indicates good performance/possible and (-) indicates poor performance/impossible.*

3.3.3 Topologies to have active power access during voltage dips

During a voltage dip the DVR injects voltages and thereby restores the supply voltages. In this phase the DVR exchanges active and reactive power with the surrounding system. If active power is supplied to the load by the DVR, it needs a source for the energy. Two concepts are here considered, one concept uses stored energy and the other concept uses no significant energy storage. The stored energy can be delivered from different kinds of energy storage systems such as batteries [54], double-Layer-Capacitors [6], super-capacitors, Flywheel storage [74] or SMES. In the no-storage DVR concept, the DVR has practically no energy storage and the energy is taken from the remaining supply voltage during the voltage dip. The four system topologies, which are presented and compared are:

- Topologies with stored energy topologies
  - Constant DC-link voltage.
  - Variable DC-link voltage.
- Topologies with power from the supply
  - Supply side connected passive shunt converter.
  - Load side shunt connected passive shunt converter.

The parameters, which have been focused on in the comparison are:

- DC-link voltage level and control during voltage dips.
- Rating of the converters used for the DVR solution.
- Ability to compensate voltage dips of different character.
- Effect on the supply and neighboring loads.
- System and control complexity.
- Relative cost estimations.

In order to be able to simplify and clarify the comparison the load is assumed to be purely resistive and to absorb rated active power and the load voltages are always restored to rated load voltage. This can be stated as:

$$P_{load} = P_{load,rated},\ \phi_{load} = 0,\ U_{load} = U_{load,rated} \tag{3.8}$$

The voltage dips, which are considered, are symmetrical, have no phase jump and the DVR injects only a voltage in phase with the supply voltage:

$$\underline{U}_{dip,non-symmetry\%} = 0,\ \phi_{dip} = 0,\ \phi_{DVR} = \phi_{supply} \tag{3.9}$$

Some values and equations have been transferred to pu values with rated line load voltage as base voltage and the rated three-phase load power as the base power value. pu values are indicated with lower-case letters.

Topologies with stored energy

In this case all the energy is stored before the voltage dip and a very small scale converter is expected to be used to re-charge the energy storage. Two different control/hardware methods have been considered, which are a DVR operating with a constant DC-link voltage and a DVR operating with a variable DC-link voltage.

Constant DC-link voltage A DVR with constant DC-link illustrated in Fig. 3.8 voltage is expected to have superior performance and an effective utilization of the energy storage. An additional converter is expected to convert energy from the main storage to a small DC-link and thereby control and stabilize the DC-link voltage. The DVR with a constant voltage is here considered to be a reference topology by which the other DVR topologies are evaluated. It offers a constant DC-link voltage at all times and does not increase the current drawn from the supply. Power taken from the grid is reduced according to the dip.

$$P_{supply} = \sqrt{3}|\underline{I}_{load}||\underline{U}_{dip}|cos(\phi_{load}) \tag{3.10}$$

In pu and at rated load:

$$p_{supply} = |\underline{u}_{dip}| \tag{3.11}$$

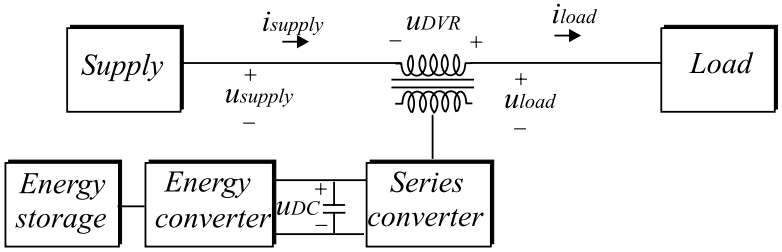


Figure 3.8: *DVR topology with power from stored energy and operating with constant DC-link voltage.*

the rating of the energy converter and the series converter can be estimated to:

$$S_{energy\,converter} = S_{serie} = \sqrt{3}|(1 - \underline{U}_{dip})||\underline{I}_{load}| = \sqrt{3}|(1 - \underline{U}_{dip})|cos(\phi_{load}) \quad (3.12)$$

$$s_{energy\,converter} = s_{serie} = |(1 - \underline{u}_{dip})|cos(\phi_{load}) \quad (3.13)$$

Variable DC-link voltage A DVR with variable DC-link voltage illustrated in Fig. 3.9 offers benefits in simplicity due to only one high rated converter and only DC-link capacitors as the only storage. The voltage injection capacity depends on

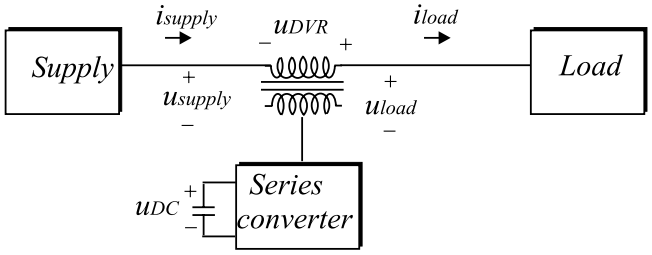


Figure 3.9: *DVR topology with power from stored energy and operating with variable DC-link voltage.*

the actual level of the DC-link voltage, and energy saving control strategies are urgent to fully utilize the energy storage system. The energy content in the storage can be calculated as:

$$E_{storage} = \frac{1}{2} C_{DC} U^2_{DC,rated} \quad (3.14)$$

the DC-link voltage can most likely only to be utilized down to a certain DC-link voltage level and the actual energy storage can be estimated to:

$$\Delta E = \frac{1}{2} C_{DC} (U^2_{DC,begin} - U^2_{DC,end}) \quad (3.15)$$

At severe dips a smaller portion of the stored energy, ΔE can be effectively utilized and the ability to restore the supply voltage decays.

Topologies with power from the supply

Taking power from the remaining supply voltage has the disadvantage of an increase in the supply current. The advantages are cost saving of the energy storage and the ability to compensate long duration voltage dips.

Taking power from the grid can have a negative influence on the neighboring upstream loads, because the DVR protects its downstream loads by taking more current from the supply, which can lead to an even more severe voltage dip for upstream loads.

Topologies for DVR using power from the grid can generally be characterized with the location of the shunt converter e.g. at the supply side of the series converter or at the load side of the series converter [78]. Both passive and active shunt converters can be used. Here, only passive diode converters are considered in a six pulse coupling, which are rated for full power transfer. This will give simple topologies, but passive solutions with diodes are less controllable and absorb non-linear currents.

Considering stationary conditions and active power only, the supply currents increase at a severe dip, because the active power to the load has to be supplied from the supply.

$$|\underline{i}_{supply}| = \frac{1}{|\underline{u}_{dip}|} \tag{3.16}$$

Supply side connected passive converter The supply side connected passive converter illustrated in Fig. 3.10. The shunt current and DC-link voltage are poorly controllable and at non-symmetrical voltage dip the current drawn by the shunt converter will be very uneven distributed between the phases. The DC-link level is

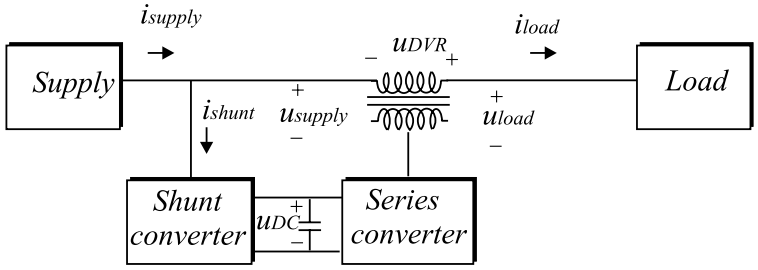


Figure 3.10: *DVR topology with energy from the grid and with a shunt converter at the supply side of the series converter.*

proportional to the voltage dip depth and at severe voltage dips the required voltage injection is high, but the DC-voltage can here be expected to be low according to:

$$u_{DC} \simeq \sqrt{2}|\underline{u}_{supply}| = \sqrt{2}|\underline{u}_{dip}| \tag{3.17}$$

$$\underline{u}_{DVR} = 1 - \underline{u}_{dip} \tag{3.18}$$

In the case of a voltage dip the power is not absorbed by the shunt converter until the DC-link voltage have dropped below a certain dip dependent voltage.

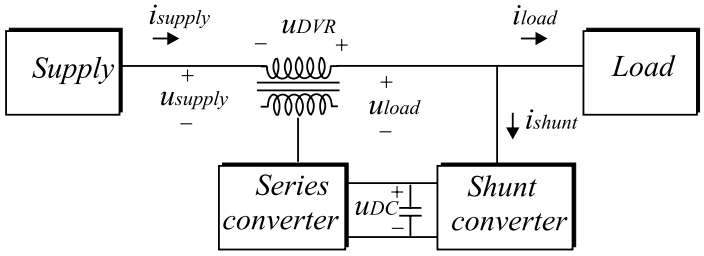


Figure 3.11: *DVR topology with energy from the grid and with the DVR operating with a shunt converter at the load side of the series converter.*

The following equations express the maximum voltage for the shunt and series converter:

$$|\underline{u}_{shunt}| = 1 \tag{3.19}$$

$$|\underline{u}_{serie}| = |1 - \underline{u}_{dip}| \tag{3.20}$$

Current to be handled by the converters in:

$$|\underline{i}_{shunt}| = \frac{|(1 - \underline{u}_{dip})|}{|\underline{u}_{dip}|} \tag{3.21}$$

$$|\underline{i}_{serie}| = 1 \tag{3.22}$$

and power:

$$|\underline{s}_{serie}| = |(1 - \underline{u}_{dip})| \tag{3.23}$$

$$|\underline{s}_{shunt}| = \frac{|(1 - \underline{u}_{dip})|}{|\underline{u}_{dip}|} \tag{3.24}$$

The concept of a passive shunt converter is relative cheap, but the coherence between the DC-link voltage and the dip size is unfavorably and the solution is expected to be unqualified for severe voltage dip compensation in general.

Load side connected passive converter A DVR with a load side connected passive converter [78], illustrated in Fig. 3.11, can basically keep the DC-link voltage almost constant, because the load voltage is controlled by the DVR itself. One disadvantage is the currents handled by the series converter increase significantly during a voltage dip and the load voltages can be more distorted because of the non-linear currents drawn by the passive shunt converter, which have to flow through the series converter. The DC-link voltage is equal to:

$$u_{DC} \simeq \sqrt{2}|\underline{u}_{load}| = \sqrt{2}|(\underline{u}_{dip} + \underline{u}_{DVR})| \tag{3.25}$$

The voltage rating of the converters depends on the injected voltage capability and the restored load voltage level:

$$|\underline{u}_{serie}| = |1 - \underline{u}_{dip}| \tag{3.26}$$

$$|\underline{u}_{shunt}| = 1 \tag{3.27}$$

The current rating of the shunt converter is equal to the supply side topology. At severe dips very high converter current ratings are necessary according to:

$$|\underline{i}_{serie}| = \frac{1}{|\underline{u}_{dip}|} \tag{3.28}$$

$$|\underline{i}_{shunt}| = \frac{1}{|1 - \underline{u}_{dip}|} \tag{3.29}$$

The power rating of the series and shunt converter are equal and can be calculated to:

$$|\underline{s}_{serie}| = |\underline{s}_{shunt}| = \frac{|1 - \underline{u}_{dip}|}{|\underline{u}_{dip}|} \tag{3.30}$$

A DVR with this circuit topology, seems to be a very effective solution, the DC-link can be held relatively constant. In the case of non-symmetrical voltage dip the current can still be taken equally from each phase.

Comparison of the topologies for active power access

In this section a small comparison of the four DVR topologies have been performed. Fig. 3.12 illustrates how the rating of the converters varies with dip size for the four topologies. The load side connected converter requires the highest rated DVR followed by the supply side connected converter, constant DC and variable DC. To be able to compensate a load of 1 pu from a 0.5 pu voltage dip the four solutions require at least an installed rating of 0.5 pu, 1 pu, 1.5 pu or 2 pu, respectively.

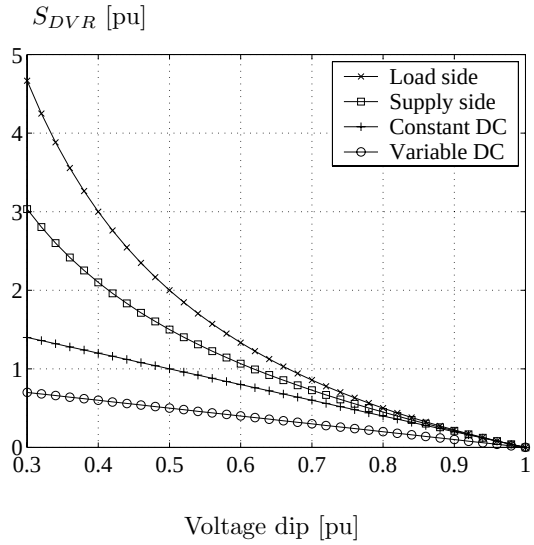


Figure 3.12: *Power rating of the converters used for the four topologies versus voltage dip size in pu.*

In Fig. 3.13a and Fig. 3.13b the two topologies with power from the supply are compared. It includes the current rating of the series converter, power rating of

the series converter and the total DVR rating versus voltage dip size. A difference exists in the rating of the series converter for the two concepts. E.g. at 0.4 voltage dip the current through the series converter is 2.5 pu for the load side converter and 1 pu for the supply side. The associated power ratings for the series converter at this dip size are 0.6 and 1.5, respectively.

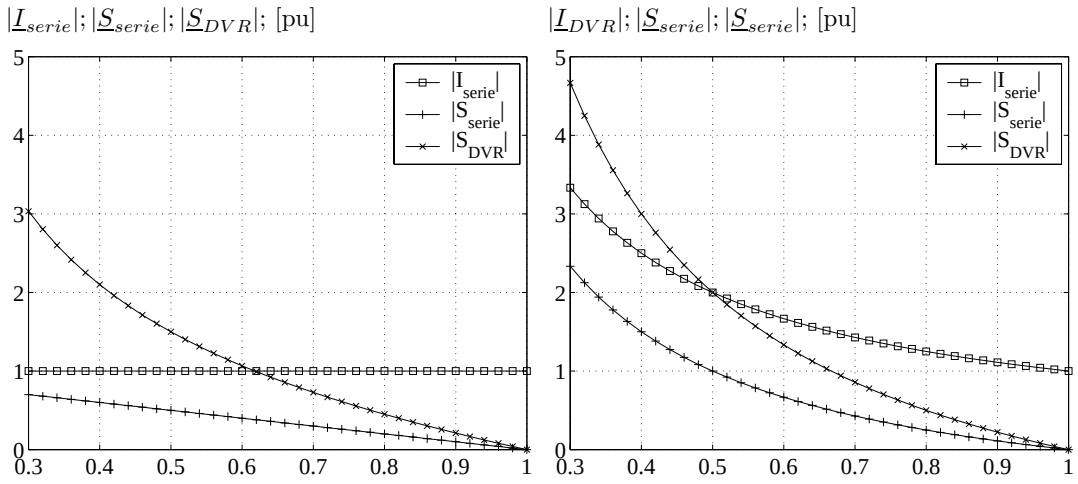


Figure 3.13: *Comparison of DVR topologies with power from the supply. The current requirements for the series converter ($|(\underline{I}_{serie})|$), power requirements for the series converter ($|\underline{I}_{serie}|$) and the total DVR power requirements ($|\underline{S}_{DVR}|$) versus voltage dip size in pu. a) supply side shunt converter and b) load side shunt converter.*

Table 3.3 illustrates the different topologies and a four level rating of each topology is done. Although the best topology cannot be ultimately stated, some main differences can be seen. In this comparison the system with a load side connected shunt converter is estimated to have the highest total points with general high performance followed with low cost and complexity. Still the negative grid effects and high rated series converter could disqualify the solution for certain applications.

The system with a constant DC-link voltages has been ranked as the second best topology with the highest number of pluses (+) with superior performance in deep voltage dips, but drawbacks regarding complexity, converter rating and overall cost are also important aspects.

The system with a variable DC-link is ranked number three with relative poor performance for severe and long duration dips. Some of the drawbacks can be accepted due to the simple topology and the converter rating.

The DVR topology, which have the highest number of minuses (-) and the least number of total points is the system with a supply side connected shunt converter. The uncontrollable DC-link voltage which is proportional to the dip voltage and if the dip is non-symmetrical the DVR will tend to draw a non-symmetrical current although the faulted phases will be less loaded. The topology is not found suitable for a DVR solution. If the passive shunt converter was substituted with an active converter some of the main drawbacks could be eliminated and the topology should then be re-evaluated.

	Stored Energy		No Stored Energy	
	Constant DC-link voltage	**Variable DC-link voltage**	**Supply side connected converter**	**Load side connected converter**
Long voltage dip duration	-	--	++	++
Deep voltage dips	++	-	--	+
Non-symmetrical voltage dips	++	++	--	+
DC-link voltage control	++	-	--	+
Size of energy storage	++	+		
Grid effects	+	+	--	-
Rating of charging/shunt converter	--	+	--	-
Rating of the series converter	+	+	+	--
System complexity	-	++	+	+
Cost Estimation	--	-	+	+
Control complexity	-	-	++	+
Sum (+)	10	8	6	8
Sum (-)	7	6	10	4
Sum (total)	3	2	-4	4

Table 3.3: *Comparison of the different DVR topologies with the gradings: very good(++), good(+), poor(-) and very poor (--).*

3.4 Protection of the DVR

Protection issues of series devices are very important and have been treated in [45] and [49]. The DVR must be robust against short circuits at the load side of the DVR and the loss of grid connection. Transients are not considered in the analysis. A single-phase DVR with a full bridge converter is illustrated in Fig. 3.14 in order to explain the protection issues.

3.4.1 Short circuit protection

A short circuit at the load side of the DVR can endanger the operation and damage the equipment of the DVR. During the short circuit a high current will be sourced to the fault and it has to flow in the series connected device. Two control methods can be considered:

- Passive control of the DVR; The short circuit currents are too high to be handled by the VSC and the protection philosophy is to bypass the DVR in or-

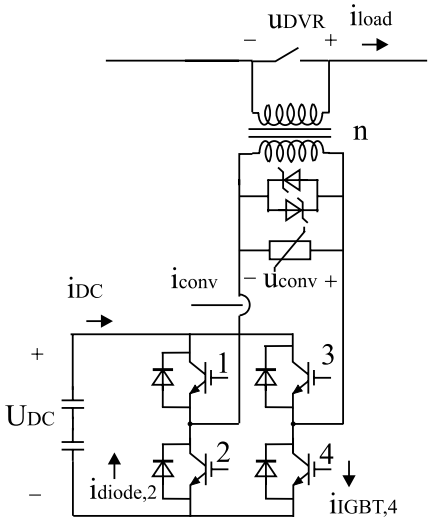


Figure 3.14: DVR with protection equipment illustrated for one phase.

der to avoid any equipment damage and interference with existing protection equipment.

- Active control of the DVR; The VSC are rated for the short circuit currents, and can be operated actively to clear the fault and reduce or increase the short circuit currents.

The passive control scheme is for the moment the most likely protection scheme for series connected power electronics. Using this philosophy, the VSC can be rated for relative low currents. For active control the VSC has to be rated to conduct short circuit currents and still to be able to inject voltages into the grid.

The protection of series connected devices is much more difficult than the protection of shunt devices and a down-stream short circuit can be critical and requires extra protection equipment.

During zero voltage injection the VSC conducts the load current and applying a zero state, the load current can flow in the diodes and the power switches. The full bridge converter has two zero state conditions for each phase with either the upper IGBT switches (1,3) turned on or the lower IGBT switches (2,4) turned on.

The power switches can be of the most known types IGBTs, GTOs or IGCTs and for the DVR used in this project the IGBTs are used. The IGBT has current limiting capabilities and during a short circuit of an IGBT the current is limited to approximately 5 - 10 times the rated current and the full voltage drop across the switch. During this process the power dissipation in the switch is very high and usually the switch must be turned off before 10 μs to be within its Safe Operating Area (SOA).

The short circuit level before and after the DVR has a main influence on the protection equipment used. Knowing the DVR and supply parameters the short

circuit current level can be estimated:

$$\underline{Z}_{DVR} = \frac{U_{DVR}^2}{S_{DVR}} \underline{u}_{DVR,Z} \tag{3.31}$$

$$I_{sc} = \frac{U_{load}}{\sqrt{3}(Z_{DVR} + Z_{supply})} \tag{3.32}$$

Assuming $u_{DVR} = 0.5$ pu, $s_{DVR} = 0.5$ pu, $Z_{supply} = 0$, $|\underline{u}_{DVR,Z}| = 0.10$ pu the short circuit current can with this very simple example be calculated to 20 times the rated current. Ideally, the converter should conduct the current until the protection equipment has cleared the fault, but it would require significantly more silicon to withstand 20 times the rated current for the required fault clearing time e.g. 60 ms - 1 s. Turning the power switches off makes only a current path through the diodes when the voltage across the DVR is larger than the DC-link voltage level. Therefore, turning off the power switches will lead to an uncontrolled charging of the DC-link capacitor. The uncontrolled charging can in some DVR design cause a destructive DC-voltage level, which will damage the power modules and the DC capacitors. The highest risk of damage will arise if the rated DC-link voltage is close to the maximum allowable DC-voltage and if the voltage injection value is low.

The protection issues for series devices are also analyzed in [49] and an integrated protection scheme with varistors, thyristors and mechanical bypass are proposed. Instead of just turning the power devices off, an alternative current path must be ensured to avoid interference with the existing protection equipment and the uncontrolled charging of the DC-link. In several DVR protection schemes thyristors are intended to take over the current for the VSC until a more robust and slower mechanically bypass is ensured. The methods to ensure a current path can be stated as:

- Voltage source converter; The converter can ensure a current path by applying a zero-state condition. High current capability increases the cost.
- Injection transformer; The transformer can be a part of the protection strategy. The ratio of the transformer indicates the potential voltage at the secondary side and the current limiting capability can be used effectively. Additionally, the saturation level of the transformer can be used to limit the current transfer to the secondary side. [49].
- Thyristors; Anti-parallel thyristors can react fast and would most likely be placed at the secondary side of the transformer to take advantage of the current limiting capability of the injection transformer.
- Mechanical bypass; The protection is relative slow, but robust, cheap and easy to control. The bypass can be placed both on the secondary and the primary side of the transformer. At the primary side all the DVR equipment is bypassed and a minimal voltage drop is caused by the DVR. Placing the mechanical bypass at the secondary side, the injection transformer is inserted in the short circuit current path and it can thereby reduce the potential short circuit current.

- Varistors; Varistors can be considered as a voltage dependent resistance and cannot ensure a continuous current path, but they can be used to detect and limit voltage spikes across the DVR. Varistors would must effectively be placed at the secondary side of the injection transformers.

Even by ensuring a current path at all time during a short circuit the DVR can interfere with the existing protection equipment. The short circuit level can be significantly reduced after the DVR and the short circuit current can be below the threshold value. At other locations the reduction of the short circuit level can be beneficial and wanted.

3.4.2 Loss of grid connection

In [43] the risk of damaging neighboring equipment in the case of a disconnection of the supply has been investigated. If the feeding supply voltage is low, the DVR has to stop injecting a voltage. A simplified diagram of this case is illustrated in Fig. 3.15 during line breaking the DVR will try to compensate the load voltage to pre-voltage level and the load current will be forced through the downstream load. A voltage and current reversal can be expected at the downstream load unless the DVR detects the primary supply breaking and goes into a bypass state. A number of measures have been proposed in [43], and one method is to stop injecting at very low supply voltage, which in some cases would lead to a bypass even though the supply line is still intact. The voltage across the downstream load is equal to the voltage:

$$\underline{U}_{supply} = -\underline{U}_{DVR}\frac{\underline{Z}_{load}}{\underline{Z}_{load} + \underline{Z}_{upstream}} \tag{3.33}$$

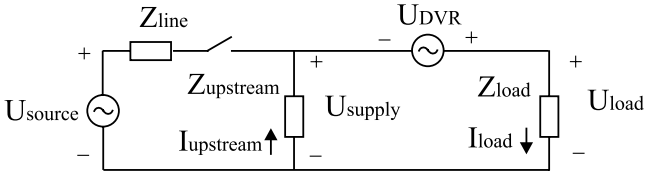


Figure 3.15: DVR with upstream load and breaker.

3.5 Summary and conclusion

The location of the DVR has been discussed, and the differences in placing the DVR at the medium voltage distribution system or at the low voltage distribution system. Thereafter DVR topologies have been discussed including the connection of converter with or without an injection transformer, converter topologies and how to obtain the active power necessary to compensate most voltage dips. Finally, the protection issues for a DVR have been treated. Some of the main conclusions are:

- The placement of a large DVR at the medium voltage level can simplify the DVR topology and minimize the losses and voltage drop across the DVR.
- A DVR topology using a injection transformer is expected to give certain benefits regarding the converter topology, the charging circuit and the protection of the DVR.
- Regarding the converter topology one of the first aspects is a possible requirement zero sequence voltage injection and the capability of the topology to inject zero sequence voltages. A high number of synthesized voltage levels can be beneficial in order to reduce the size of the line-filter.
- In a strong grid and with a rare intensity of severe voltage dips DVR topologies without any significant energy storage can be an interesting alternative. A shunt converter at the load side of the series converter can have a good performance, but at the expense of a high installed converter capacity.
- Protection of the DVR must be ensured during downstream short circuit and line breaking. A continuous current path is important to avoid uncontrolled charging of the DC-link.

At the basis of the discussion of the topologies for a dynamic voltage restorer the design aspects are treated.

Chapter 4

Design and specification of the dynamic voltage restorer

In this chapter some general design procedures for the dynamic voltage restorer are presented followed by a more specific design of the two prototype DVRs constructed in conjunction with the Ph.D. project. At the end of the chapter the main parameters for the control setup, for the LV and for the HV-DVR are presented.

4.1 Design parameters

The rating of the dynamic voltage restorer has been the topic in the papers [9] and [48]. A simplified model for the DVR is illustrated for one phase in Fig. 4.1.

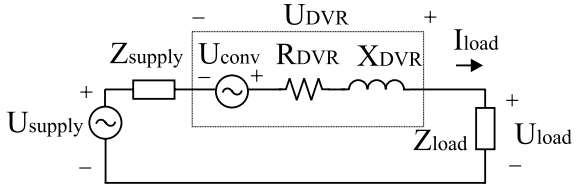


Figure 4.1: Single-phase simplified model for the DVR.

4.1.1 Voltage, current and energy rating

In the simplified model illustrated in Fig. 4.1 the DVR consists of a controllable voltage source and a fixed resistance, which is equivalent to the losses in the DVR and a fixed reactance, which is equivalent to the reactive elements in the DVR. The main design parameters for the DVR are the voltage injection capability, the current handling capability and the size of the energy storage. The voltage injection capability can be expressed as:

$$u_{DVR,\%} = \frac{U_{DVR}}{U_{supply,rated}} 100\,\% \tag{4.1}$$

The voltage injection capability should be chosen as low as necessary in order to reduce equipment cost and standby losses. Losses tend to increase if the voltage

rating of the DVR is increased assuming the current rating of the DVR current is fixed:

$$R_{DVR} \simeq \frac{U_{DVR}}{I_{DVR}} u_{DVR,R} \tag{4.2}$$

The losses in the DVR can be grouped into losses in the transformer, filter and the converter. The voltage injection is mostly fixed by the requirements to compensate symmetrical and non-symmetrical voltage dips and the next step is to size the current rating of the DVR. Because the DVR is a series connected device, the design of the current handling capability of the DVR depends on:

- In-rush phenomenon in the down-stream load, such as starting of large motors and magnetization of transformers.
- Non-linear loads, which may lead to higher peak currents.
- P(U) and Q(U) characteristics of the downstream loads; If the DVR is notable to compensate severe voltage dips, the load current may increase according to the resulting load voltages.
- Down stream short circuits; The protection issues are treated in Section 3.4, but the DVR should by able to survive a downstream short circuit and robustness to short circuits may increase the necessary current rating.
- Future load increase.
- Standby losses; Increasing the current rating of the DVR tends to decrease the standby losses in the system.
- Magnetization of the injection transformer; A fast magnetization of the injection transformers requires a high current, which must be supplied by the VSC.

If the current rating is sized too low, some of the above cases will result in current overload in the VSC and the DVR has to change to bypass mode, in which the DVR is not able to compensate voltage dips. The main parameter to size the current rating of the VSC is the peak current and the RMS current in the grid. The IGBTs have an overload current limit, which will influence the system during short circuit and an heavy loading conditions. The sizing of the current handling capability can be defined as:

$$i_{DVR,\%} = \frac{I_{DVR}}{I_{load,rated}} 100\,\% \tag{4.3}$$

To size voltage, current and energy rating, information about the voltage dip distribution and voltage dip frequency at the location of the inserted DVR is necessary. A one year pre-recording can be necessary to get statistically valid data. By these data it is possible to draw a diagram with the distribution curve of the number of voltage dips as a function of the voltage dip depth and voltage dip duration:

$$n_{dip}(U_{dip}, t_{dip}) \tag{4.4}$$

An example of this curve is given in Fig. 4.2 [47]. The classification can be complicated if phase jump, symmetry and non-ideal voltage dips are taken into account.

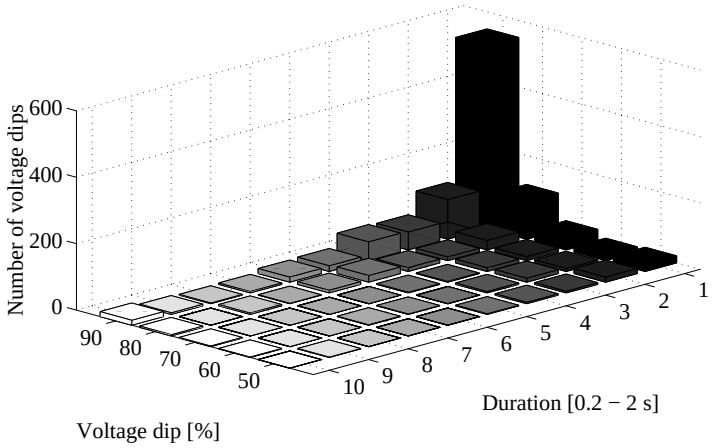


Figure 4.2: *Voltage dip matrix with number of dips as a function of voltage dip duration and voltage dip magnitude. [47]*

Information about the load is also necessary in the design procedure with the load sensitivity/tripping as a function of the dip voltage and voltage dip duration [11]. The CEBEMA curve in Fig. 1.1 is one graphical approach to the following function:

$$n_{trip}(U_{dip}, t_{dip}) \tag{4.5}$$

If a large mixed load is to be protected the tripping limit may vary and voltage dip symmetry and phase jump can influence the tripping curve. The optimization has to include cost functions of the losses associated with the voltage dips:

$$C_{losses}(U_{dip}, t_{dip}) \tag{4.6}$$

and a cost function for the DVR including the voltage, current, energy rating and standby losses:

$$C_{DVR}(U_{DVR}, I_{DVR}, E_{DVR}, P_{losses}) \tag{4.7}$$

In [18] it has been stated that the DVR cost is approximately 300 US$/kVA and it has a 5 % annual operating costs (% of total costs). The standby losses are very dependent on the voltage injection and current handling capabilities. Several factors can be included in the rating of a DVR optimized with respect to costs. Taking three DVR installations reported in [75], they have between 0.4 - 0.5 pu voltage injection capabilities and can maintain maximum voltage injection on all three phases for 14 - 30 cycles. Below 0.3 pu voltage injection the effort of inserting a small rated DVR

may be too large and above 0.5 pu the costs and standby losses may be favoring UPS solutions instead of DVR solutions.

The energy drain for a symmetrical voltage dip and a symmetrical load can be calculated to:

$$E_{DVR} = \sqrt{3}|1 - \underline{U}_{dip}||\underline{I}_{load}|cos(\phi_{load}) \cdot t_{dip} \tag{4.8}$$

when the DVR compensates a symmetrical voltage dip with no phase jump and the voltage injected is in-phase with the supply voltage.

4.2 Design of the DVR elements

The section includes the design of the two DVRs and the considerations taken in the design procedures.

4.2.1 Design of the converter

The converter is a voltage source converter, which is equipped with fully controllable switches. The most common three switch types in the considered power range is the IGBT, GTO and the IGCT. The IGBT switch is chosen for the DVR converters, because it is easy to control and suited for the actual power range. The IGBT is not necessarily the best switch, because the current limiting behaviour is not particularly wanted in a DVR application.

From the comparison of converter topologies in Section 3.3 the full bridge converter topology has been chosen for the DVR, originally because it is a versatile topology:

- Zero sequence voltages can be injected.
- Three voltage level can be synthesized and the effective switching frequency is the double of the actual device switching frequency. Thereby, the line-filter can be reduced.
- The DC-link is easy to control and charge.

The DVR topology is illustrated for one phase in Fig. 4.3 with a LC-filter and an injection transformer. Both the LV and HV-DVR are based on 1200 V IGBT modules and the rated DC-link voltage is 500-700 V. The rated DC-link voltage is set to 560 V for the LV-DVR, 600 V for the HV-DVR. From the above choices the injected voltage capability can be estimated. Using a carrier based sine modulation and defining the amplitude modulation m_a as:

$$m_a = \frac{\hat{u}_{conv}}{\hat{u}_{tri}} \tag{4.9}$$

$$\hat{u}_{tri} = U_{DC} \tag{4.10}$$

if the modulation index is below one the fundamental frequency component varies linearly with m_a. Above one the output voltage contains more harmonics and the fundamental component does not vary linearly with m_a [44]. The maximum amplitude with square-wave operation is:

$$U_{conv} = \frac{4U_{DC}}{\pi\sqrt{2}} \tag{4.11}$$

For the full bridge converter and the LV converter with 560 V DC the maximum fundamental RMS voltage is 504 V. Some modulation schemes have a higher utilization of the DC-link voltage which will be treated in Section 5.5. Operating in

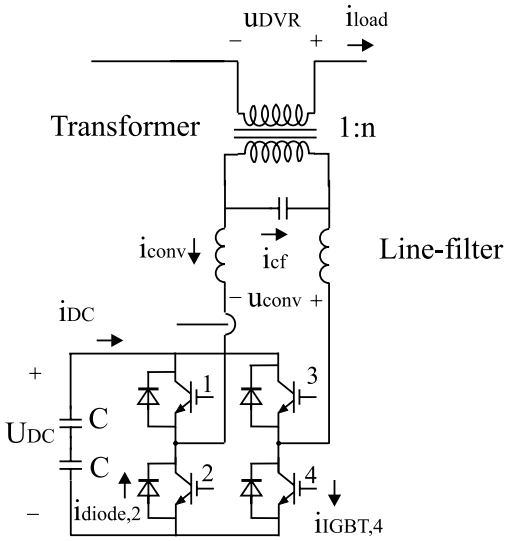


Figure 4.3: Single-phase diagram for the full bridge DVR.

the linear region with the modulation index below one the maximum RMS voltage is:

$$U_{conv} = \frac{U_{DC}}{\sqrt{2}} \quad if\ m_a = 1 \tag{4.12}$$

which in the above case is equal to 396 V in RMS phase voltage. The current through the converter is the sum of the ripple current generated by the switchings, the magnetization current of the transformer and the load current.

$$i_{VSC} = i_{Cf}(t) + i_{magnitization}(t) + ni_{load}(t) \tag{4.13}$$

Two switches are always conducting and during standby mode the RMS current can be equally shared between the upper and lower switches:

$$I_{diode} = I_{IGBT} = \frac{I_{conv}}{4} \tag{4.14}$$

The current sharing between the diodes and the active switches during voltage injection vary with the direction of the active power, circulation of reactive power and the modulation index. During transfer of active power to the DC-link the diodes conducts a larger part of the current. Exchange of pure reactive power gives ideally equal sharing between the IGBTs and the diodes. The worst case for the diodes are protecting a voltage dip at a maximum resistive load and injecting maximum voltage. Here the diodes conduct the major part of the load current and the worst case for the IGBTs are the protection of the same load from a maximum voltage swell.

In case of a short circuit in the downstream load and the bypass protection fails the DC-link can be uncontrollable charged by the short circuit current via the free

wheeling diodes. At worst case the DC-link is charged to the peak voltage of the maximum voltage across the DVR, the maximum voltage across the DVR is the supply voltage:

$$U_{DC,fault} = \sqrt{2}\frac{U_{supppply}}{n} \tag{4.15}$$

This uncontrolled voltage can be damaging for the system and in this DVR design the converter is designed to be able to handle a bypass fault without reaching a destructive DC-link voltage. This has been acquired by having a large voltage injection value 0.5 pu, which gives a poor utilization of the DVR converter hardware.

4.2.2 Design of the injection transformers

Galvanic isolation between the supply and the DVR converter is advantageous. Otherwise the DVR converters would have to float at the phase voltage potentials and it would require isolation to ground, a more complex converter topology and a more complex protection of the DVR from incoming transients.

Several types of transformers can be used for DVRs. Here it is chosen to operate with magnetic de-coupled single-phase transformers in an open star/open star configuration. The chosen transformer configuration can be used together with the full bridge topology and it can be used to generate zero sequence voltages.

Two concepts have been tested, which requires a different design of the DVR injection transformers. In the LV-DVR the VSC switches directly into the transformers and in the HV-DVR the VSC switches into a line-filter and the voltage applied to the transformer is filtered from most of the switching harmonics.

The ratio of the transformer can be sized according to the injection capability of the VSC and the wished injection level into the system. The ratio can be defined as:

$$n = \frac{U_{pri}}{U_{sec}} = \frac{U_{DVR}}{U_{conv}} \tag{4.16}$$

The ratio can be sized to have a high utilization of the converter, but protection concerns can also be necessary to include in the transformer decision/design.

Important aspects in the transformer design is the voltage drop across the transformer, which means the size of the leakage inductance and the copper resistance. The leakage inductance can in some cases be useful in the filtering of the switching harmonics from the VSC. The resistive losses are mostly unwanted, but can give some damping to oscillations in the line-filter. The summation of the resistive and reactive elements are also called the short circuit impedance of the transformer and it has a major influence of the short circuit current, which can be expected during a down-stream short circuit. Reactive and resistive components of the transformer

can be calculated to the primary side by:

$$X_{tra,pri} = \frac{U_{pri}^2}{S^2} u_{tra,X} \tag{4.17}$$

$$R_{tra,pri} = \frac{U_{pri}^2}{S^2} u_{tra,R} \tag{4.18}$$

$$\underline{Z}_{tra,pri} = R_{tra,pri} + jX_{tra,pri} \tag{4.19}$$

with $u_{tra,X}$ and $u_{tra,R}$ as the transformers pu reactive and resistive voltage drop. The $L_{tra,pri}/R_{tra,pri}$ can also have some influence on the obtainable bandwidth. During normal supply voltage condition, it is preferred not to inject a voltage by the DVR and a very low voltage drop across the transformer is wanted. During a voltage dip the DVR has to inject a voltage and the voltage drop of the transformer can be compensated by voltage injection.

During a downstream short circuit the mechanical and thermal stress of the injection transformer can be considerable and the worst case short circuit current can be calculated to:

$$\underline{I}_{tra,SC} = \frac{\underline{U}_{supply,max}}{\sqrt{3}\underline{Z}_{tra}} \tag{4.20}$$

In the equation the maximum supply voltage at the location is used and not the injected DVR voltage.

The transformer must be built by a ferro material in order to control the flux, leakage and reduce the size of the transformer. This introduce iron losses from hysteresis and eddy currents and non-linear magnetization currents. The saturation of ferro materials must also be considered and at which voltage level the transformer can be allowed to saturate. Applying a step change in the AC voltage the current to the transformer will mainly be decided by the phase of the AC voltage, the pre-flux level, the iron characteristic and the saturation level. The problems have not in detail been addressed in any litterature, but in [43] it has been proposed to chose the saturation level for series transformers at twice the level of typical shunt transformers, which will increase the cost, volume and weight significantly. The hysteresis and saturation effects can lead to high in-rush currents, which must be supplied by the DVR. The in-rush occurs, when it changes from zero voltage injection to high voltage injection. During steady state injection the magnetization current should also be supplied by the VSC.

Switching directly into the transformer requires the use of materials and design that keep the inductance high for high frequency components and preferable, a frequency independent inductance.

The transformer floats at the supply voltage level and the isolation level has to be accordingly high with uniform isolation. In an isolated medium voltage system the phase voltage can increase to the rated line voltage during a fault and the isolation level must be prepared for this situation.

Capacitive effects in the transformer have been considered. Capacitive coupling between the primary and secondary winding, primary winding capacitance and secondary winding capacitance are present. The values have been experimental measured on the LV transformer, to identify potential resonance problems. Applying a

converter to generate a sine wave voltage with a VSC could introduce a a small DC voltage, which then again could saturate the injection transformers. However, no problems have been encountered regarding resonance problems and DC saturation.

4.2.3 Design of the line-filter

Design of a line-filter for a DVR has been treated in [41]. The filter is inserted to damp the switching harmonics generated by the PWM control of VSC. The PWM control generates harmonics and if the modulation index are kept below one the switching harmonics are typically centered around the switching frequency and multiples of the switching frequency.

Consumer products have to keep certain standards before released to mass distribution. Regarding EMC three important areas are usually included [69]:

1. Emission of current harmonics of equal and non equal harmonics (2. - 40. harmonic). [64]

2. Conducted emission in the frequency region 150 kHz - 30 MHz.

3. Radiated emission in 30 MHz -1 GHz.

A supply connected PWM inverter, which is shunt connected and operated with 5 - 10 kHz switching frequency, emits currents in a wide frequency spectrum. A large part of the harmonics is injected in the spectrum without any limits 2 kHz - 150 kHz. Still it is considered important to damp the switching harmonics in order to be able to fulfill standards in conducted emission in the region 150 kHz - 30 MHz and radiated emission in the 30 MHz - 1 GHz.

In this design procedure it has not been chosen to design the filter to follow certain standards, because the DVR is difficult to classify. The DVR is not a consumer product and it is a series connected device to be placed in the distribution system. The DVR can thereby not be classified as a typical load. The filter design deals with guidelines to size the filter and the consequences for the DVR performance.

Ideally, the PWM converter only injects a fundamental component and the switching harmonics assuming that the converter is operated in the linear modulation region. A variety of factors can lead to the injection of non-characteristic harmonics. Some of the factors are:

- Non-linear effects in the converter caused by the non-linear voltage drop, turn-on, turn-off delay and deadtime.

- Quantification in the A/D conversion and the duty cycle generation.

- Aliasing in the A/D conversion.

- Omission of short duty cycles to reduce switching losses.

- Background harmonic distortion enters the control and leads to an injection of harmonics in the system.

- Non-linear control algorithms.
- Filter values and design.

The injected harmonic currents can be substantial, if it is a shunt connected PWM inverter operated up against a strong supply connection. Regarding the DVR, the non-fundamental DVR voltages will be injected in series with the supply and the load and the associated currents injected depend on the supply and load impedance. The load impedances are assumed to be relatively high, which then also count for the injected currents. The non fundamental harmonic voltage will still be injected and cause an increased total harmonic distortion of the load voltage.

The emission of noise from shunt devices is less complicated in comparison with series devices. In Fig. 4.4a the model for a shunt device is shown and by knowing the standard impedance of the supply the emission by the converter can be calculated. For a series connected device the emission of harmonics depends on the connected

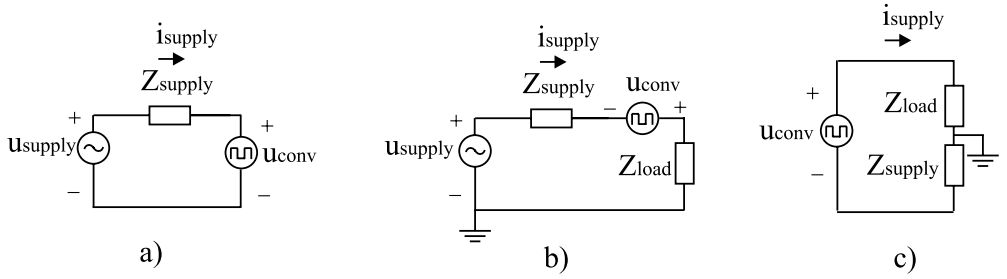


Figure 4.4: *Simple model for the emission from series and shunt converters. a) Shunt converter, b) series converter and c) redrawn circuit for the series converter with the supply voltage set to zero.*

load impedance and the supply impedance. Fig. 4.4b and 4.4c illustrates how the model for a single-phase series device can be redrawn. This voltage division between the supply and the load indicates that from the noise generated by the converter a part of it can be seen as load voltage distortion for downstream loads, and the other part is supply voltage distortion for upstream loads. Both aspects are important, the load voltage distortion is primarily considered to be an internal issue, because it concerns "own" and known loads, which also have the benefits from the inserted DVR. Upstream voltage distortion is a more external issue, which may disturb other loads and the upstream loads have no benefits from the inserted DVR.

Line-filters are included in most papers about the DVR THEY complicate the control. The most simple filter is to have an L-filter either from the leakage inductor in the injection transformer or from a special designed inductor. The damping is relatively low with this filter and often a filter capacitor is added after the converter inductance, here called a LC-filter, and for better damping an LCL-filter is used. The order of the filter can be further increased, but considerations are here kept at 1. - 3. order filters.

The model of the LCL-filter applied to a shunt VSC is illustrated in Fig. 4.5a. The impedance for the supply is very low and by superposition the supply can

be considered as a short circuit. The resonance frequency is decided by two filter inductors (L_{1f}, L_{2f}) and the filter capacitor (C_f). The supply inductor is included in the design for a small converter connected to a strong supply, $L_{2f} >> L_{supply}$ the influence of the supply inductance is minimal. The resonance frequency for the filter is equal to:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_{1f} + L_{2f} + L_{supply}}{L_{1f}(L_{2f} + L_{supply})C_f}} \tag{4.21}$$

For a series connected series converter the model is illustrated in Fig. 4.5b. The

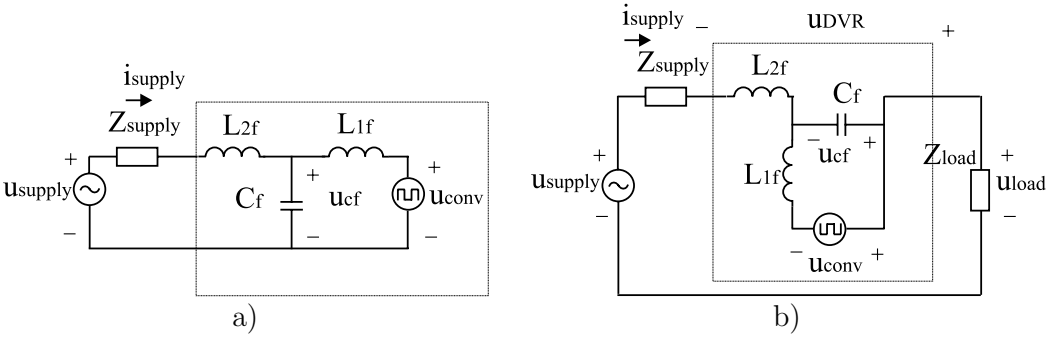


Figure 4.5: *LCL-filter. a) Applied for a shunt converter and b) applied for a series converter.*

supply inductance is still included in the model and also the connected downstream load. For a DVR the resonance frequency (f_{res}) varies with the actual connected load according to:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_{1f} + L_{2f} + L_{supply} + L_{load}}{L_{1f}(L_{2f} + L_{supply} + L_{load})C_f}} \tag{4.22}$$

in a DVR application it will very often be the case that $(L_{supply}+L_{load}+L_{2f}) >> L_{1f}$ and the resonance can be simplified to:

$$f_{res} \simeq \frac{1}{2\pi}\frac{1}{\sqrt{L_{1f}C_f}} \tag{4.23}$$

The design procedure for the line-filter could be as follows:

1. L_{1f} is the main parameter for the size of the ripple current flowing in the converter.

2. Sizing the filter capacitor with respect to the wanted resonance frequency and the absorbed reactive power during full voltage injection.

3. Sizing L_{2f} to the wanted damping, voltage drop and resonance frequency.

The frequency dependency of $L_{1f}(\omega)$,$L_{2f}(\omega)$ and $C_f(\omega)$ should be as low as possible in order to have a good damping of high frequency components and a predictable filter performance.

Inserting a line-filter has several effects on the system performance beside the damping of the switching harmonics. Considering an LCL-filter for a DVR application the insertion has the following potential problems:

- A voltage step increase in converter voltage can initiate the line-filter resonance frequency and this may lead to a distortion of the load voltage. The bandwidth of the injected voltage may have to be reduced to avoid high oscillations.
- The line-filter components introduce losses and voltage drop.
- A non-linear load can excite the filter resonance frequency and lead to a distorted load voltage.
- A potential risk of a harmonic voltage component in the supply will excite a resonance in the line-filter.

During voltage injection the conditions change because the DVR injects a voltage, and a high ripple current flows through the inductor closest to the converter. The voltage across the capacitor is large and the capacitor absorbs reactive power generated from the VSC and a main part of the ripple current components. The inductor closest to the supply also damps the harmonics injected and the voltages across the DVR are cleaned for a main part of the switching harmonics.

Filter for the LV-DVR The LV-DVR is switching directly into the injection transformer, filter capacitors are located at the primary side of the transformer and no additional inductors (L_{2f}) are added. The leakage inductance for the transformer can within an interval be controlled by the transformer design.

Filter for the HV-DVR The HV-DVR is equipped with air inductors for the inductors close to the converter, a LV capacitor bank and the inductor closest to supply is the leakage inductance from the injection transformers.

4.3 DVR parameters and system description

The common control hardware for the LV and HV-DVR is here presented. Followed by a more individual presentation of the measurement system and hardware parameters for the LV and HV-DVR.

In order to be able to evaluate and compare the parameters for the designed DVRs the DVR parameters have been listed with both real values and a pu values. The base values have been chosen to be the rated line voltage of the supply, rated frequency of the supply and rated three-phase power of the load:

$$S_{base1} = S_{load,rated},\ U_{base1} = U_{supply,rated},\ f_{base} = f_{supply,rated} \tag{4.24}$$

Base values on the secondary side (converter side) of the injection transformers are changed according to the voltage ratio of the injection transformers:

$$S_{base2} = S_{load,rated},\ U_{base2} = U_{supply,rated}/n,\ f_{base} = f_{supply,rated} \tag{4.25}$$

For the DC-side the voltage base is changed to the rated DC-link voltage and the power base is chosen to be the rated power multiplied with the pu voltage injection capability.

$$S_{DC,base} = S_{load,rated}\frac{u_{DVR,\%}}{100\,\%},\ U_{DC,base} = U_{DC,rated},\ f_{base2} = f_{supply,rated} \tag{4.26}$$

All the base values are listed in Table 4.1.

DVR	Location	$\mathbf{S_{base}}$ [kVA]	$\mathbf{U_{base}}$ [V]	$\mathbf{I_{base}}$ [A]	$\mathbf{Z_{base}}$ [Ω]
LV	Primary	20	400	28.8	8
	Secondary	20	800	14.4	32.0
	DC	10	565	17.7	31.9
HV	Primary	400	10.0 k	23.1	250
	Secondary	400	1.00 k	231	2.50
	DC	200	600	333	1.80

Table 4.1: *Base values for the LV- and HV-DVR at the primary side, secondary side and DC side.*

4.3.1 Control system

The basic control system is the same for the two designed DVRs and it is presented below. The main control equipment is a 32-bit, 33 MHz, floating-point Sharc DSP 21062 Digital Signal Processor (DSP) and a Siemens Micro Controller MCB80C167 (MC) [61]. The DSP is the main calculation unit and it calculates the duty cycles for each IGBT. The results from the DSP is then transferred to a Dual Port RAM unit (DPRAM), which is read by the MC and the MC generates via the COMPARE registers the actual PWM. The PWM signals are then transferred to the power converters by fiber optic.

The interface from the user to the DVR is via a Pentium PC and the DSP is located in a socket inside the PC. The analog signals are A/D converted with two eight channel AD7891 from Analog devices and read by the DSP once in each switching cycle. The control setup is illustrated in Fig. 4.6 and the main control parameters are listed in Table 4.2.

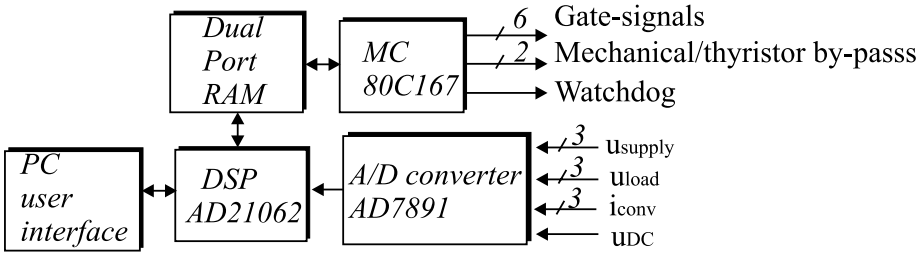


Figure 4.6: *The control setup and communication between the PC, DSP and the MC.*

Device	**Description**	**Abbreviation**	**Real value**
Compare unit:	Resolution time	$t_{resolution}$	400 ns
Gate driver:	Dead time in the converter	t_{dead}	3 μs
	Delay time	t_{delay}	2 μs
AD-converter:	Conversion time per channel	$t_{conversion}$	1.6 μs
	A/D accuracy		12 bit
Antialiasing filter:	Cross over frequency	f_{cross}	2.3 kHz
	Resistance	R_{af}	10 kΩ
	Capacitance	C_{af}	6.8 nF

Table 4.2: Control parameters for the LV and HV-DVR.

The PWM generation

The time values to change switch states are transferred from the DPRAM to the micro processor and the built-in Capture/Compare unit (CAP/COM) in the MC unit is used to generate the PWM signals. The counter is clocked every 400 ns, which gives the maximum resolution ($t_{resolution}$) and it gives quantification errors in requested pulse-width and the actual generated pulse width. The calculation of the duty-cycles in the DSP is illustrated in Fig. 4.7a. The time values t_1, t_2, t_3, t_4 are calculated for each phase in the DSP on the basis of the actual reference voltage and DC-link voltage. The time values are transferred to the MC and the MC generates the PWM signals to the power converters. Generation of the PWM signals in the MC is illustrated in Fig. 4.7b.

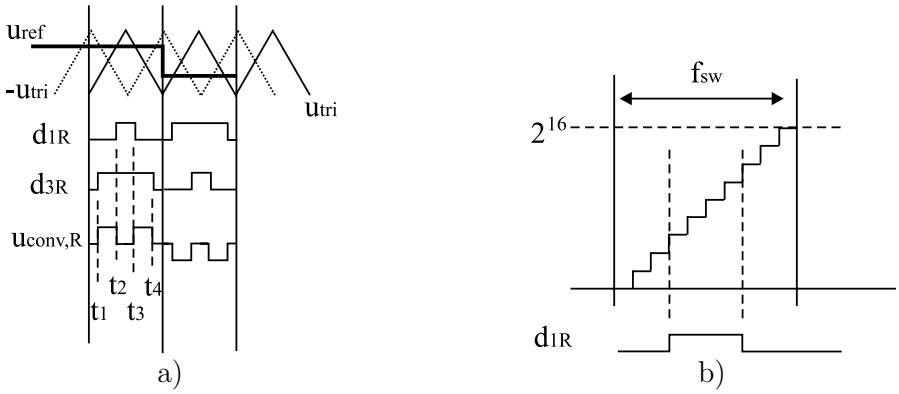


Figure 4.7: *a) The time values (t_1, t_2, t_3, t_4) are calculated in the DSP for each phase, d_{1R} and d_{3R} are the control signals for the phase R converter and $u_{conv,R}$ the resulting phase voltage. b) PWM generation in the Micro-controller.*

4.3.2 LV-DVR parameters

The LV-DVR has mainly been designed to be able to test the DVR hardware, and control strategies before scaling the DVR up to a high power unit which is used in the MV distribution system. The LV-DVR has also made it possible to compare high power versus low power DVRs and DVRs connected in the MV distribution system versus LV distribution systems. The LV-DVR has been scaled to be testable with a 30 kVA three-phase programmable power supply, which can generate arbitrarily waveforms.

The intended location for the LV-DVR is in a four wire LV-system with 400 V line voltage. The LV-DVR has been built on the basis of two two-level converters connected together via the DC-link illustrated in Fig. 4.8 and the main DVR parameters in table 4.3.

The DC-link can be charged with a passive six pulse diode bridge and the DC voltage can be controlled by an auxiliary three-phase 400 V AC supply, thereby the DC-link is approximately charged to the peak level of the line voltage $U_{DC} \simeq 560V$. The parameters for the DC-link is shown in table 4.4.

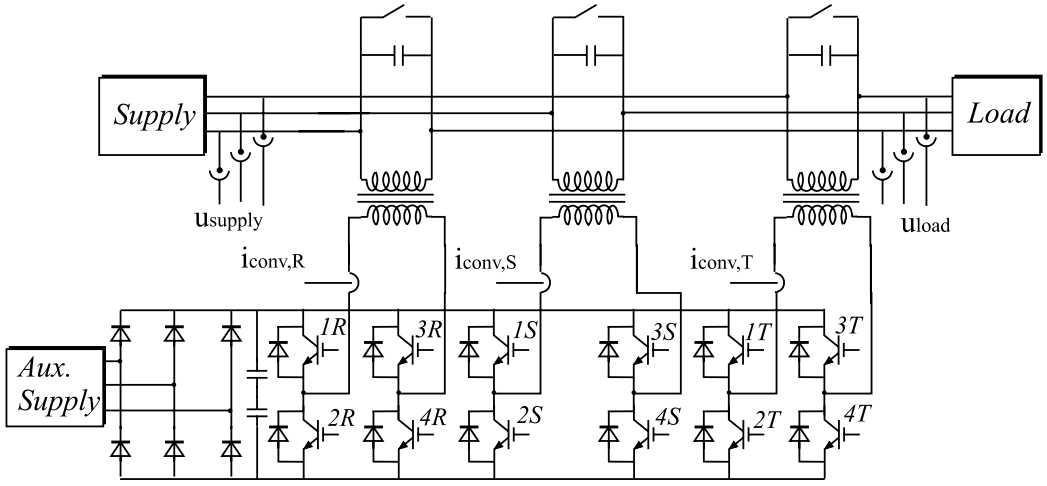


Figure 4.8: Power circuit for the LV-DVR.

The series transformers consist of three single phase transformers and the main parameters are listed in table 4.5.

Device	Description	Abbreviation	Real value	pu value
DVR	Total power	S_{DVR}	10 kVA	0.5
	Phase voltage	$U_{DVR}/\sqrt{3}$	115 V	
	Line voltage	U_{DVR}	200 V	0.5
	Current	I_{DVR}	28.8 A	1
Series	Total power	S_{conv}	10 kVA	0.5
converter	Phase voltage	$U_{conv}/\sqrt{3}$	230 V	
	Line voltage	U_{conv}	400 V	0.5
	Converter current	I_{conv}	14.5 A	1
Filter	Inductance (transformer)	L_{1f}	0.76 mH	0.030
	Capacitance	C_f	$20\mu F$	0.050
	Resonance	f_{res}	1290 Hz	25.9

Table 4.3: LV-DVR parameters.

Device	Description	Abbreviation	Real value	pu value
DC-link	Rated voltage	U_{DC}	565 V	1
	Voltage (supply)	$U_{DC,supply}$	651 V	1.15
	Capacitance	C_{DC}	2 mF	
	Maximum voltage	U_{max}	1200 V	2.12
	Energy storage(565 V)	$E_{storage}$	320 J	1.60
DC-charger	Power rating	$P_{charger}$	10 kVA	0.5

Table 4.4: DC-link parameters for the LV-DVR.

Description	Abbreviation	Real value	pu value
Rated power	S_{tra}	10 kVA	0.5
Primary voltage	U_{pri}	200 V	0.5
Secondary voltage	U_{sec}	400 V	0.5
primary current	I_{pri}	28.8 A	1
Secondary current	I_{sec}	14.4 A	1
Injection capability	U_{pri}/U_{rated}	0.5	
Transformer ratio	n	0.5	
Leakage inductance	L_{pri}	0.76 mH	0.06
Resistance	R_{pri}	120 mΩ	0.03
Mag. inductance (sec)	L_{mag}	314 mH	
Iron resistance (sec)	R_{fe}	359 Ω	
no load losses	$P_{no-load}$	265 W	0.004

Table 4.5: Transformer parameters for the LV-DVR.

The LV-measurement system measures phase voltages with respect to the neutral, first with a resistive voltage divider and then galvanic isolation have been ensured with an HPCPL-7800 isolation amplifier. The converter currents ($i_{conv,R}$, $i_{conv,S}$,$i_{conv,T}$) are measured with LEM current transducer, which ensures galvanic isolation and measurement of DC components. The parameters for the measurement system are given in Table 4.6.

Device	**Description**	**Abbreviation**	**Real value**
Measurement system:	Minimum AC voltage	U_{min}	-400 V
	Maximum AC voltage	U_{max}	+400 V
	Quantization voltage	U_{quant}	0.195 V
	Minimum AC current	I_{min}	-30 A
	Maximum AC voltage	I_{max}	+30
	Quantization current	U_{quant}	0.195 V
	Minimum DC voltage	U_{min}	500 V
	Maximum DC voltage	U_{max}	800 V
	Quantization voltage	U_{quant}	0.07 V

Table 4.6: Measurement parameters for the LV-DVR.

4.3.3 HV-DVR parameters

The intended location for the HV-DVR is in a three-wire 10 kV medium voltage system. The HV-DVR is based on the rating shown in Table 4.7 and the power circuit is illustrated in Fig. 4.9. The line-filter is kept on the LV-converter side to use existing components and reduce the complexity of the injection transformer. S2.1-3 are the mechanical bypass, F1.1-3 the converter fusses and F1.1-3 are the capacitor fusses.

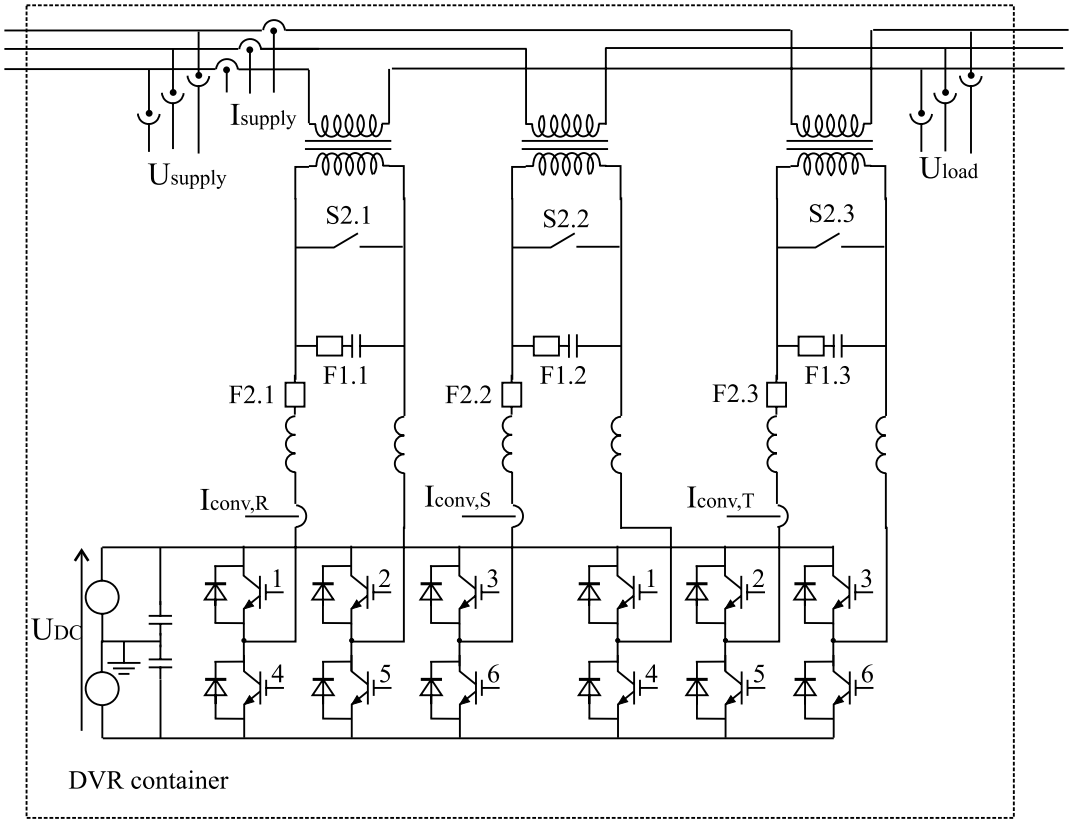


Figure 4.9: Power circuit for the HV-DVR.

Each phase consists of four paralleled IGBTs from Toshiba (MG150Q2YS51), which are N-channel 1200 V, 150 A modules. Saturation voltage is typically maximal 3.6 V. Each phase can approximately conduct 600 A continues DC current. Approximate values for the on-state voltage drop is 1 V and internal resistance 4.2 mΩ. [70].

The line-filter capacitors (illustrated in figure 4.10d) are built from 80 μF capacitors (Arcotronics MKP1.44/A, 280 V RMS). In order to be able to withstand 290 V and a potential over-voltage, two capacitors are series coupled and three units are coupled in parallel (2 X 3 capacitors per phase = 120 μF per phase and 560 V RMS voltage). The filter inductor for each phase are built from two air inductors

Device	Description	Abbreviation	Real value	pu value
DVR	Total Power	S_{DVR}	200 kVA	0.5
	Phase voltage	$U_{DVR}/\sqrt{3}$	2.9 kV	
	Line voltage	U_{DVR}	5. kV	0.5
	DVR current	I_{DVR}	23 A	1
Series	Total Power	S_{conv}	200 kVA	0.5
converter	Phase voltage	$U_{conv}/\sqrt{3}$	290 V	
	Line voltage	U_{conv}	500 V	0.5
	Converter current	I_{conv}	230 A	1
Filter	Inductance	L_{1f}	260μ H	0.03
	Capacitance	C_f	120μF	0.01
	Resonance	f_{res}	901 Hz	22

Table 4.7: DVR parameters for the HV-DVR.

(illustrated in figure 4.10c) of 120 μF each. Parameters for the DC-link is shown in Table 4.8. The DC-link is built from 48, 2200 μF, 500 V capacitors. 24 are paralleled equal to 52.8 mF, the two banks are series coupled with the midpoint grounded and the total capacitance is 26.4 mF and the maximum DC voltage is 1000 V. The converters and the DC-link is shown in in figure 4.10a. From the pu calculation it can be seen that the stored energy can be used for full power injection for 1.04 power cycles. The main data for the measurement system is shown in Table 4.10. The

Device	Description	Abbreviation	Real value	pu value
DC-link	Capacitance	C_{DC}	26 mF	
	Rated voltage	$U_{DC,rated}$	600 V	1.00
	Voltage (supply)	$U_{DC,supply}$	820 V	1.37
	Maximum voltage	U_{max}	1200 V	2.00
	Operating voltage	ΔU	200 - 600 V	0.33 - 1.00
	Energy storage(600 V)	$E_{storage}$	4680 J	1.17
	Energy storage(200 V)	$E_{storage}$	520 J	0.13
	Δ Energy	ΔE	4160 J	1.04
DC-charger	Power rating	$P_{charger}$	3 kW	0.015
	Voltage rating	$U_{charger}$	0 - 600 V	0 - 1.00

Table 4.8: DC-link parameters for the HV-DVR.

HV-measurement system measures phase voltages with respect to ground, first with a resistive voltage divider and 1:10000 then the signals are amplified and galvanic isolation have been ensured with an HPCPL-7800 isolation amplifiers.

The converter currents ($i_{conv,R}$, $i_{conv,S}$, $i_{conv,T}$) are measured with LEM current transducers, which ensures galvanic isolation and measurement of DC components. The parameters for the measurement system are given in Table 4.9.

The converter currents are measured and transformed to a voltage inside the

Device	Description	Abbreviation	Real value
Measurement system:	Minimum AC voltage	U_{min}	-15 kV
	Maximum AC voltage	U_{max}	+15 kV
	Quantization voltage	U_{quant}	7.3 V
	Minimum AC current	I_{min}	-500 A
	Maximum AC voltage	I_{max}	+500 A
	Quantization current	I_{quant}	0.24 A
	Minimum DC voltage	U_{min}	0 V
	Maximum DC voltage	U_{max}	1000 V
	Quantization voltage	U_{quant}	0.24 V

Table 4.9: Measurement parameters for the HV-DVR.

Device	Description/Technical data
HV voltage transducer	24 kV, Resistive voltage divider 1:10000
	ABB voltage sensor KEVA 24 A1
HV current transducer	3 - 30 - 300 A, LEM FLEX-2
DC-link voltage	Resistive voltage divider
LV current transducer	LEM current sensors

Table 4.10: Measurement system parameters for the HV-DVR.

converter rack and the currents are further filtered and transferred to the A/D-board. The measured currents are used for protection of the DVR and converter against over-load.

Three single phase transformers have been used, illustrated in figure 4.10b. Each having a rating of 67 kVA power rating and a 2.9/0.29 kV voltage ratio. The parameters for the HV transformers are shown in Table 4.11. The load can thereby be up to 400 kVA with 0.50 pu voltage injection.

Description	Abbreviation	Real value	pu value
Power	S_{tra}	67 kVA	
Primary voltage	U_{pri}	2.9 kV	
Secondary voltage	U_{sec}	290 V	
primary current	I_{pri}	23.1 A	
Secondary current	I_{sec}	231 A	
Injection ratio	U_{pri}/U_{rated}	0.5	
Ratio	n	10:1	
Leakage inductance	L_{sec}	201 μH	0.05
Resistance	R_{sec}	50 $m\Omega$	0.03
Mag. inductance (sec)	L_{mag}	314 mH	
Iron-loss resistance (sec)	R_{fe}	359	
No load losses	P_0	265 W	0.004

Table 4.11: Transformer parameters for the HV-DVR.

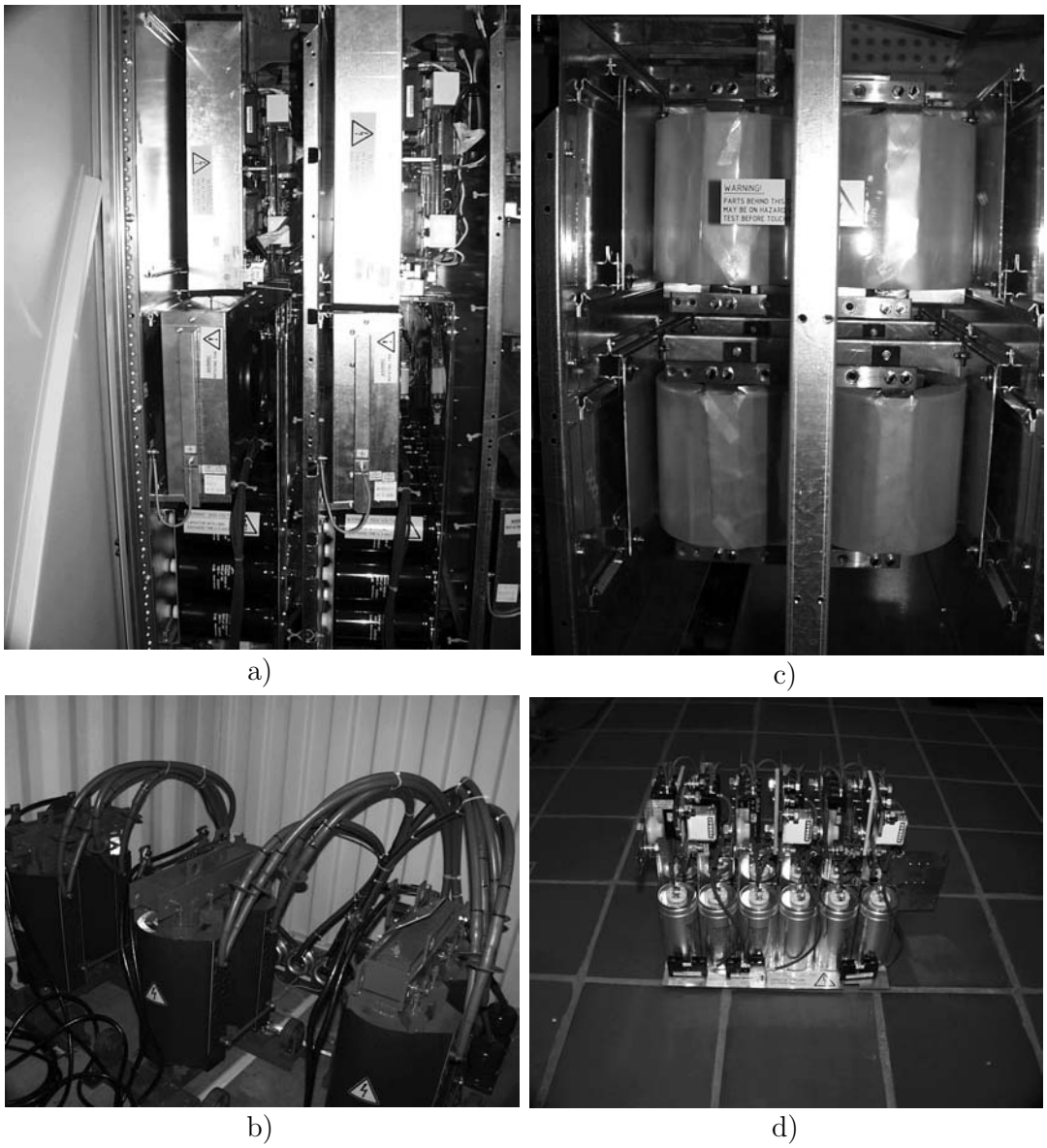


Figure 4.10: *The HV converter hardware.*
a) VSC and DC-link capacitors, b) the three single-phase injection transformers, c) line inductances and d) line capacitors.

4.4 Summary and conclusion

The design procedure for the DVR has been the topic for this chapter. This has included the voltage, current and energy rating of the DVR followed by considerations about single main elements in the DVR design.

- The voltage injection level should be kept low to keep standby losses and voltage drop across the DVR as low as possible. On the other hand a high voltage injection level can limit potential DC-link over-voltages and limit down-stream short circuit currents.
- The DVR current rating can be chosen high to decrease losses and avoid frequent DVR bypass conditions. A high current rating can be used to improve the load voltage control and improve the dynamic response of the DVR.
- The line-filter is critical regarding the damping of the switching harmonics and line-filter oscillations.
- A LV-DVR has been sized in order to protect a three-phase 20 kVA load from a 0.5 pu voltage dip in a four-wire 400 V system. The LV-DVR has a full rated passive shunt converter and can thereby compensate for infinitely long voltage dips.
- A HV-DVR has been sized in order to protect a three-phase 400 kVA load from a 0.5 pu voltage dip in a three-wire 10 kV system. The DVR is operated with a floating DC-link voltage and has a low AC/DC charging converter.

Finally, the specifications for the control system and the hardware parameters for the LV-DVR and HV-DVR have been presented.

Chapter 5

Control strategy for a dynamic voltage restorer

Control of dynamic voltage restorer is scarcely described in literature, but analogies with control of power converters for other applications can often be used. Control of FACTS is thoroughly described in [31] and further analogies can be drawn with the control of high power drives in [13]. Applications with series connected devices are particular close to a DVR and they are for instance treated in active filters by [2] and [25], and static voltage voltage controllers by [15], [16] and [17].

In this chapter the DVR control strategy is analyzed. First, the basic DVR control with the main DVR limitations and here after the control of a DVR during different characteristic symmetrical and non-symmetrical voltage dips. The influence of connecting different types of loads are discussed and how the control strategy is influenced by some different methods to feed active power to the DVR. Finally, the modulation strategy of a DVR is analyzed and the control for the DVR is designed.

5.1 Operation modes

The DVR can basically be operated in three different operation modes, which here are referred to as:

- Bypass mode; The DVR is bypassed mechanically or electronically, during high load currents and down-stream short circuits. In this mode the DVR cannot inject a voltage to improve the voltage quality.
- Standby mode; The supply voltages are at rated level and the DVR are ready to compensate for a voltage dip. During standby mode the DVR can have secondary tasks and operation modes:
  - Low loss mode; The DVR performs no switchings and the losses in the DVR are minimized to conduction losses.
  - Harmonic blocking mode and voltage balancing mode; The DVR improves the load voltage and compensate for a poor background voltage quality. The DVR has to perform switchings and it is expected to inject a relatively small voltage.

  - Capacitor emulation mode; The DVR is controlled to operate as an inserted series capacitor, thereby it can compensate for a large line inductance and for the inductance inserted in conjunction with the DVR.

- Active mode; A voltage dip has been detected and the DVR injects the missing voltage.

In the low loss mode the control of the DVR is optimized with respect to losses, which can be at locations with high quality supply voltages and at locations where the voltage drop caused by the DVR can be accepted. At locations with a poor background voltage quality, the losses in the DVR may have a secondary priority and the DVR can be operated actively to improve the voltage quality for the load.

5.1.1 DVR limitations

Before going into details about different control strategies it is important to address the DVR limitations, which may be closely linked to the control strategy. A DVR has limited capabilities and the DVR will most likely face a voltage dip outside the range of full compensation. Four important limitations for a DVR are:

- Voltage limit; The design of the DVR is limited in the injection capability to keep the cost down and to reduce the voltage drop across the device in standby operation.

- Current limit; The DVR has a limitation in current conduction capability to keep the cost down.

- Power limit; Power is stored in the DC-link, but the bulk power is often converted from the supply itself or from a larger DC storage. An additional converter is often used to maintain a constant DC-link voltage and the rating of the converter can introduce a power limit to the DVR.

- Energy limit; Energy is used to maintain the load voltage constant and the storage is normally sized as low as possible in order to reduce cost. Some dips will deplete the storage fast, and adequate control can reduce the risk of load tripping caused be insufficient energy storage.

All the limits should be taken into consideration in the control strategy. Fig. 5.1 illustrates a single-phase phasor diagram for one load case. The phasor of the pre-dip voltage is shown with a lagging load current and the voltage dip contains a negative phase jump with a reduced during-dip voltage. The voltage and power limits are indicated and the hatched region illustrates the region which the DVR can operate within. The pre-dip voltage cannot be maintained in the case illustrated in Fig. 5.1.

Other limitations

The voltage injected can with an ideal DVR be done instantly, but practical DVRs have a finite response-time and other factors may favor a smooth change from one

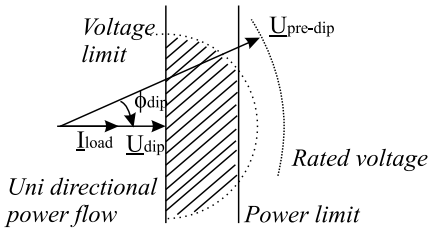


Figure 5.1: *A deep voltage dip with a phase jump. The hatched region indicates the region where the DVR can operate.*

operating point to another. For the DVR a slow change to the stationary operating point will reduce the risk of in-rush currents and saturation of the transformer. From a load point of view a fast change of the pre-dip voltage will make the voltage dip unseen. If a phase change is initiated to minimize the energy storage depletion a slow change to an adequate stationary operating point may prevent severe transients and in worst case load tripping.

Other factors are important for the control strategy, which include additional hardware constrains:

- Saturation; At high voltage injection levels the injection transformers can start to saturate, which degrades the generated load voltages and increases the currents handled by the series converter. [43]

- In-rush; At the beginning of a compensation the pre-flux level in the injection transformer can cause additional high in-rush currents.

- Bandwidth; A finite system bandwidth for the DVR complicates the compensation.

- line-filter impedance; The line-filter is necessary, but it can give unwanted voltage drop across the DVR and current oscillations in the filter components.

The limitations are very relevant to take into considerations, when the control strategies are discussed and evaluated.

5.2 Control strategy with different types of voltage dips

Control strategies for a dynamic voltage controller are analyzed with respect to different types of voltage dips. First, symmetrical voltage dips are considered followed by non-symmetrical cases.

5.2.1 Control strategy with symmetrical voltage dips

Different control strategies have been evaluated in order to control the DVR. The most commonly used method is to put the DVR voltage in phase with the supply voltage, regardless of the actual phase angle of the load current. An undisturbed load voltage requires this method, but it may lead to a fast drain of the energy storage unit. Energy optimized control has been adapted to save energy and fully utilize the energy storage capacity. This method is further described in [71].

Symmetrical voltage dip are ideally characterized by the dip duration, magnitude reduction and a phase jump. A control strategy for voltage dips with phase jump should be included in order to be able to compensate for this particular type of symmetrical voltage dip. [52] The DVR can be controlled by a number ways to improve certain parameters. It is first assumed, that the DVR is only active during the voltage dip.

1. Voltage quality optimized control: The voltages are always compensated to the pre-dip level, disregarding that this may be a operating point with high voltage injection and energy depletion.

2. Voltage amplitude optimized control: The injected voltages are controlled in a way, that minimizes the necessary injected voltages.

3. Energy optimized control: To fully utilize the energy storage, information about the load can be used to minimize the depletion of the energy storage.

The three discussed control methods are illustrated in Fig. 5.2.

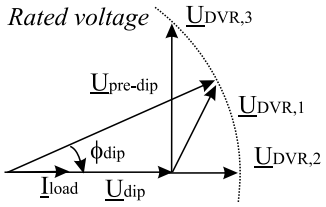


Figure 5.2: *Control strategies for a DVR compensating a voltage dip with a phase jump.* $\underline{U}_{DVR,1}$ *the voltage quality optimized control,* $\underline{U}_{DVR,2}$ *the voltage amplitude optimized control and* $\underline{U}_{DVR,3}$ *the energy optimized control.*

Common for all three methods are, that the load voltages are compensated to the rated load voltages:

$$|\underline{U}_{load}| = constant \tag{5.1}$$

$$\tag{5.2}$$

and the currents and power in steady state absorbed by the load are unchanged:

$$|\underline{I}_{load}| = constant,\ |\underline{P}_{load}| = constant,\ |\underline{Q}_{load}| = constant \tag{5.3}$$

The phase of the load voltages can be changed by the DVR, but with time the phase of the load currents will change until the same active and reactive power are absorbed by the load. The currents are equal for the supply, the DVR and the load and the amplitude of the current depends on the connected load. In a steady-state condition the load will absorb the same amount of power before and during the dip, if the voltage dip is fully compensated. The differences between the three methods are how much power, P_{DVR} and voltage, U_{DVR} the DVR has to inject into the system. Two factors for evaluating the different methods are the voltage dip depth, U_{dip} and the dip phase jump, ϕ_{dip}:

$$\underline{U}_{dip} = |\underline{U}_{dip}|\angle\phi_{dip} \tag{5.4}$$

Additionally, the load condition can be expressed by the absorbed apparent power, $\underline{S}_{load}$ and the load current, $\underline{I}_{load}$:

$$\underline{S}_{load} = P_{load} + jQ_{load} \tag{5.5}$$

$$\underline{I}_{load} = |\underline{I}_{load}|\angle\phi_{load} \tag{5.6}$$

Fig. 5.3 illustrates the active and reactive power flow in the system also investigated in [36]. The control strategy depends on the type of load connected and the load response to a change in the phase of the impressed voltage. Some loads are very sensitive to a voltage phase shift and a phase shift should be avoided in the control. Other types of loads are more tolerant to phase shifts and the main criteria is to ensure the rated voltage on all three phases.

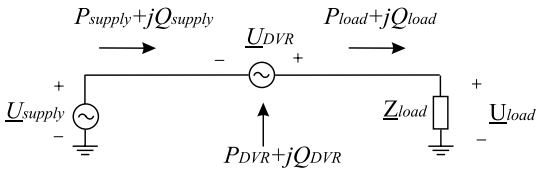


Figure 5.3: The flow of active and reactive power with a DVR inserted.

Voltage quality optimized control

Using the voltage quality optimization strategy the load voltages are always compensated to the pre-dip voltage amplitude and phase and the strategy gives undisturbed load voltages. In the case of a voltage dip without phase jump the method is equal to the voltage amplitude optimization. If a phase jump is present it can have a considerable impact on the power and voltage, which must be injected by the DVR

[43]. The power and voltage can be calculated to:

$$\underline{U}_{DVR} = 1 - \underline{U}_{dip} = 1 - |\underline{U}_{dip}|\angle\phi_{dip} \tag{5.7}$$

$$\tag{5.8}$$

$$|U_{DVR}| = \sqrt{(1 - U_{dip}cos(\phi_{dip}))^2 + (U_{dip}sin(\phi_{dip}))^2} \tag{5.9}$$

$$\phi_{DVR} = tan^{-1}\frac{-U_{dip}sin(\phi_{dip})}{1 - U_{dip}cos(\phi_{dip})} \tag{5.10}$$

$$P_{DVR} = \sqrt{3}|(\underline{U}_{DVR})||\underline{I}_{load}| \cdot cos(\phi_{load} + \phi_{DVR}) \tag{5.11}$$

A phase jump increases the amplitude of the voltage injection. The voltage quality optimized control is shown in Fig. 5.4 without phase jump ($\phi_{dip} = 0$) for three types of load ($PF_{load} = 0.5;0.75;1.0$).

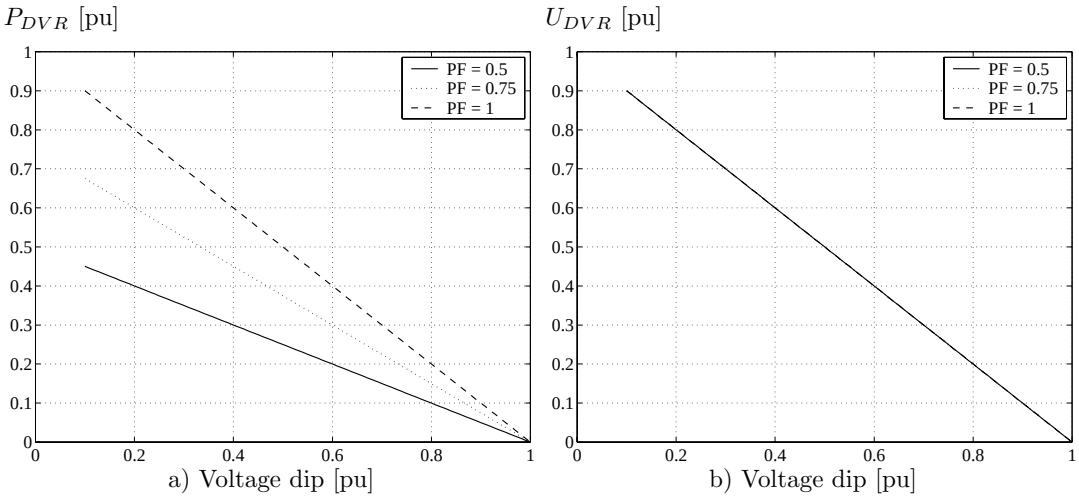


Figure 5.4: *Voltage quality optimized control of the DVR for three different power factors. a) Power injected by the DVR as a function of the voltage dip and b) voltage injected as a function of the voltage dip.*

The value of the injected power depends both on the load power factor and the phase jump. Fig. 5.5 illustrates the power and the voltages injected by the DVR with a 15 ° negative phase jump. The injected voltage is not influenced by the power factor, but the phase jump increases the necessary injection value in Fig. 5.5b For a 0.9 pu voltage dip the DVR has to inject 0.29 pu to have full compensation. The DVR has to absorb power if the load power factor is 0.5 or 0.75 and when the power factor is 1.0 the DVR still has to supply power to the load. Phase jump tends to increase the necessary voltage rating if the voltage quality optimization is used. Some aspects regarding phase jump are dealt with in [43].

Voltage amplitude optimized control

Voltage amplitude optimized control is a strategy, which gives a good utilization of the DVRs voltage rating during severe voltage dips with phase jump. The DVR

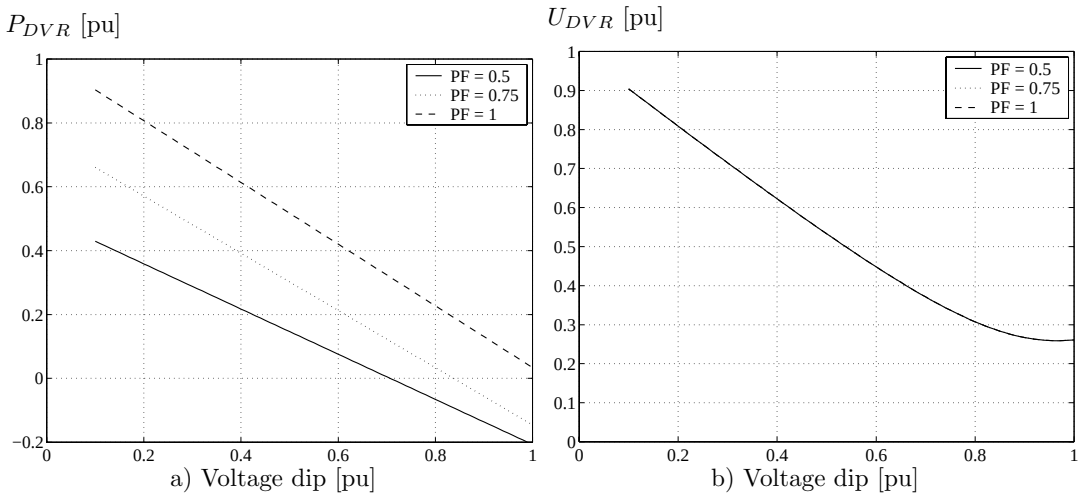


Figure 5.5: *Voltage quality optimization for three different power factors with ϕ_{dip} = (-15 °). a) Power injected by the DVR as a function of the voltage dip and b) voltage injected by the DVR as a function of the voltage dip.*

voltages are injected in phase with the supply voltage and the DVR voltage and power contribution can with this strategy be calculated to:

$$\underline{U}_{DVR} = |1 - |\underline{U}_{dip}||\angle\phi_{dip} \tag{5.12}$$

$$P_{DVR} = \sqrt{3}|\underline{U}_{DVR}||\underline{I}_{load}|cos(\phi_{load}) \tag{5.13}$$

$$P_{supply} = \sqrt{3}|\underline{U}_{dip}||\underline{I}_{load}|cos(\phi_{load}) \tag{5.14}$$

The power from the DVR increases with the severity of the voltage dip and the power contribution from the supply drops proportional to the voltage dip.

Energy optimized control

In the energy optimized control the DVR voltages are controlled according to a condition with low depletion of the energy storage. For a simple study case, with no supply impedance, the maximum power is taken from the supply, when the load current and supply voltage are in phase.

$$P_{supply} = \sqrt{3}|\underline{U}_{supply}||\underline{I}_{load}|cos(\phi_{load}) \tag{5.15}$$

The only way to maximize the power absorbed from the supply is to decrease the angle between the load current and supply voltage. The power factor of the load determines how much the power from the supply can be increased. The increase in active power ΔP can be calculated using:

$$\Delta P = P_{supply,max} - P_{supply,pre-dip} \tag{5.16}$$

$$\Delta P = \sqrt{3}|\underline{U}_{supply}||\underline{I}_{load}|(1 - cos(\phi_{load})) \tag{5.17}$$

If the load angle was low before the voltage the power from the supply can only be increased slightly and the power has to come from the DVR to compensate for the voltage dip. Energy optimized control has of course less interest in DVR topologies, which uses the power from the supply instead of stored energy.

The balance between active and reactive power is useful to evaluate the different strategies for a DVR. The equations for the active and the reactive power balance can be expressed as:

$$P_{DVR} = P_{supply} - P_{load} \tag{5.18}$$

$$Q_{DVR} = Q_{supply} - Q_{load} \tag{5.19}$$

Using energy optimized control the power from the DVR is controlled to a minimum value. Fig. 5.6a illustrates the active power the DVR should inject for three different load power factors using energy optimized control. For small voltage dips all the power is taken from the grid, until the DVR has to inject active power. The voltage, which has been injected using this method, is illustrated in Fig. 5.6b.

It can be seen from Fig. 5.6b, that during a 0.5 voltage dip it is necessary with a ($PF_{load} = 1$) to inject 0.5 pu-voltage, a ($PF_{load} = 0.75$) to inject 0.71 pu-voltage and a ($PF_{load} = 0.5$) to inject 0.87 pu-voltage. The power needed for this voltage dip is 0.5 pu, 0.25 pu, and 0 pu respectively. The energy optimized control gains mostly interest with low power factor loads and it requires a high voltage injection capability and loads, which are insensitive to phase shifts.

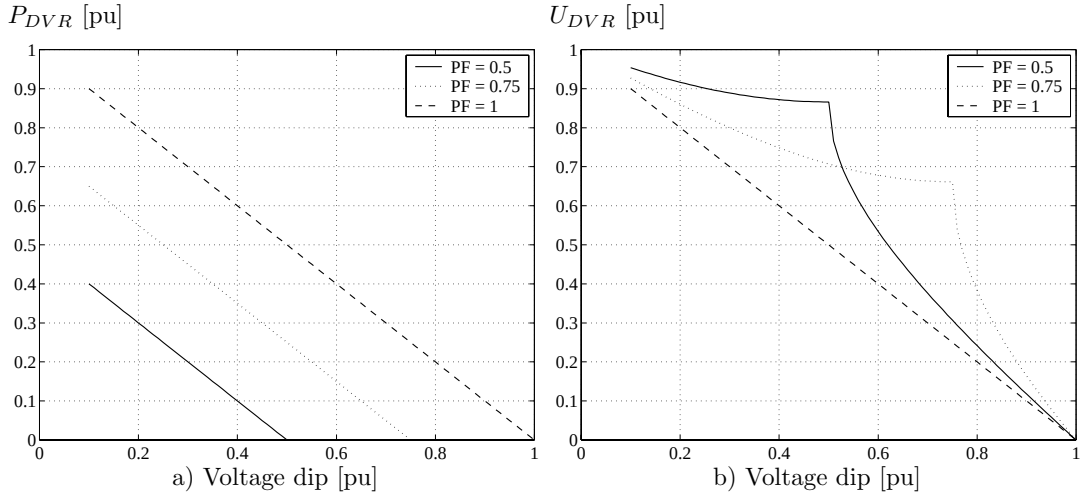


Figure 5.6: *Energy optimized control with three different power factors. a) Power injected by the DVR as a function of the voltage dip and b) Voltage injected by the DVR as a function of the voltage dip.*

Comparison of the control strategies

Three different control strategies have been discussed and the analysis has been concentrated to stationary and slow changing phasor analysis. Which of the methods to be preferred depends on several conditions such as the:

- Type of voltage dip; Depth, duration and phase jump etc.
- Type of load; Power factor and load behaviour to a phase change etc.
- Type of DVR; Energy source, power rating and voltage rating etc.

Fig. 5.7 illustrates a comparison with a DVR compensating a voltage dip with a $-15°$ phase jump protecting a 0.75 PF load. It can be seen, that for this type of load the voltage amplitude control requires the highest amount of active power, but the lowest required injected voltage. The voltage quality optimized method requires a high voltage injection capability. For severe voltage dips the energy optimized control requires the highest injection capability.

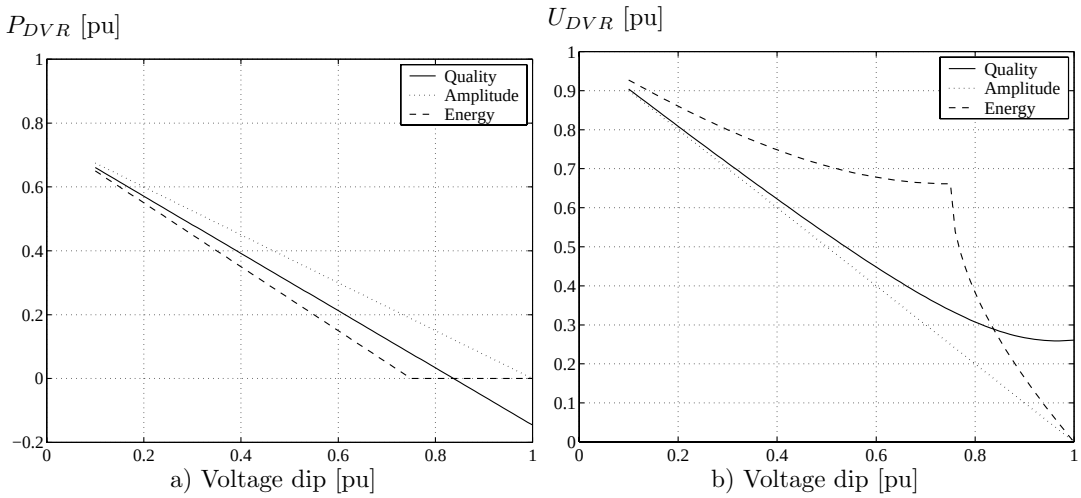


Figure 5.7: *Comparison of the three control strategies with PF_{load} = 0.75, ϕ_{dip} = -15 °. a) Power injected by the DVR as a function of the voltage dip and b) Voltage injected by the DVR as a function of the voltage dip.*

Different control methods can be used to compensate the symmetrical voltage dips. All methods could be applied for a DVR and used under different conditions. The voltage quality optimization can be used for light voltage dips and voltage amplitude optimized control for more severe dips with phase jump, where the full voltage rating is necessary.

Energy optimization has only an effect for certain load conditions and the control requires a relatively high voltage rating of the DVR, and introduces a large phase shift to the load even when the voltage dip is without phase jump.

5.2.2 Control strategy with non-symmetrical voltage dips

A very large distribution of voltage dips recorded in a EPRI survey [56] are non-symmetrical. 68 % resulted from single-phase faults, 19 % from two-phase faults and only 13 % from three-phase faults. Thereby, approximately 87 % of the voltage dips were non-symmetrical. The distribution of voltage dips can vary with the

system layout, the climate and the location. In Chapter 2 the characteristics of non-symmetrical voltage dips have been analyzed.

In the control it is important to distinguish between locations, in which the DVR should remove or ignore a sudden zero sequence voltage component from a voltage dip. The control and analysis of zero sequence components in DVR System have been treated in [19]. Removing the zero sequence component complicates the control and the zero sequence system should be measured. The DVR must be able to generate a zero sequence voltage and the control must be designed to handle a zero sequence component. The focus in this thesis is concentrated on control schemes to handle positive and negative sequence voltage components, because it is sufficient in most MV distribution levels. A DVR located in the MV distribution system with an inductor grounded system is a location in which zero sequence voltage components can appear, but not necessarily compensated, because all loads are delta connected. Leaving the zero sequence aspects the focus is how to compensate positive and negative sequence components.

The non-symmetry should be compensated to avoid tripping single-phase loads, two phase and three-phase loads. Therefore the DVR should compensate the positive sequence of the load voltage to rated value and suppress the negative sequence component in the supply voltage. Factors which can complicate the compensation of the negative sequence voltage include:

- The difficulties to synchronize with the positive sequence component in a supply voltage with the presence of a large negative sequence component.
- The detection of a non-symmetrical fault is more difficult and the injection can be delayed because of time delay in the detection of a non-symmetrical voltage dip.

Considering a symmetrical load the injection of a negative sequence voltage does not lead to a power drain of the energy storage only a pulsating power flowing to and from the DC-link storage.

5.3 Control strategy with different types of load

The control strategy can be adapted to the load to avoid load tripping, and to have a maximum utilization of the DVR equipment. The DVR can introduce a number of unwanted effects such as transients,harmonics, non-symmetrical load voltages and phase shifts. The load voltage quality can generally be controlled, but often it is a trade off between the different parameters and the load to protect may have a certain characteristic, which favor some particular control strategies. The parameters, which can be controlled are:

- Phase shifts; The DVR can in theory compensate voltage dips with phase jump, but some of the disadvantages can be high voltage injections and power drain from the energy storage. Loads, which could be sensitive to phase shifts are motors and loads synchronized to the supply, such as supply commutated

converters. Other loads may be robust to phase shifts, but it may lead to transients or in-rush currents in capacitors and transformers.

- Restoration voltage level; The load voltages do not necessarily need to be restored to rated voltage. If the load tripping voltage is 0.7 pu voltage the load voltages can be restored to 0.75 pu.
- Harmonics; The harmonics injected by the DVR can be controlled and filtered, but often at the expense of losses.
- Over-voltage/under-voltage; A fast response is necessary for some loads and often at the expense of generating transients.
- Transients; The DVR can lead to transients in the load voltages, especially in the transition phases in the beginning of a voltage dip and at the end of a voltage dip. Some loads may be sensitive to transients and the control should minimize the generation of transients.

Besides the characteristic above, the loads dependency of the voltage level have an impact on the stability of the control. The loads can be categorized according to:

- Constant power (P(U)= constant)
- Constant current (I(U)=constant)
- Constant impedance (Z(U)=constant)

The loads voltage dependency are particular important if the DVR is not able to restore the load voltages. Then the absorbed current or power will change according to the type of load connected. The different types of load must be handled by the DVR and a robust performance is important. If the load has a constant current or impedance behaviour it can be worthwhile to restore the load voltages to as low voltages as necessary. Thereby the load absorbs less power and the energy drain from the energy storage can be minimized. With a constant power load, the strategy does not give any benefits. Here, the current demanded by the load will increase and the risk of a current overload exists. With a constant power load it can even be considered to restore the load voltage to a higher voltage level to reduce the load current.

The loads, which could be protected by the DVR, are here grouped and potential problems are described:

- Time variable active/reactive power loads; Large load voltage variations if the voltage drop across the DVR is not compensated.
- Non-linear loads; A very large group of non-linear loads consists of single-phase and three-phase diode rectifies. Generally non-linear loads can lead to high load voltage distortion and initiating oscillations in the DVR line-filter.

- Loads with bidirectional power flow; Loads with reversed power flow require that the DVR storage can absorb power to be able to compensate for a voltage dip.
- Non-symmetrical loads; Can lead to non-symmetrical load voltages and power pulsations during compensation of symmetrical voltage dips.
- Electrical machines; Directly connected electrical machines can have high starting current and can be sensitive to voltage un-balance and phase shift. Electrical machines with a power electronic interface to the grid can have a completely different characteristic.
- Capacitive loads; PF correction capacitor banks could be located downstream and the load will oppose voltage variations.
- Inductive loads; Oppose fast changes in the load current.
- Resistive loads; time invariant currents, which will help to damp line-filter oscillations.
- Transformer loads; Phase shift sensitive and can have significant in-rush currents.
- Power electronic loads; The commutation of the converters is important for the DVR control strategy, non-linear loads often use line load voltages to commutate. Converters with thyristors have a control system, which is synchronized with the supply and firing turn-on signals are given to each switch, turn-off is handled by the supply voltages. Thyristor loads are expected to be sensitive to phase shifts and harmonics generated by the DVR or by the voltage dip. Passive diode converters are on the other hand considered to be very robust towards phase shifts, harmonics and voltage variations generated by the DVR.

5.4 DVR control

The section includes an analysis of the load voltage controllers, DC-link controllers and the synchronization and detection of voltage dips.

5.4.1 DVR load voltage controllers

Voltage control requires measurements and controllers to secure acceptable load voltages. The control must be robust to different disturbances from both the supply side and the load side. The disturbances could for example be non-symmetrical loads or non-symmetrical supply voltages. Various DVR voltage controllers have been tested and described in literature [33], [35] and [71]. The three main voltage controllers, which have been proposed are:

- Feedforward voltage controller

- Feedback voltage controller
- Multi variable controller

The feedforward voltage controller is the dominant DVR voltage control method, because of its simplicity and robustness. Feedforward control is used in several papers for instance in [33] and [35]. The principles of feedforward operation is illustrated in Fig. 5.8. The line above the variables indicate a three phase value represented as a space vector. From measurements of the supply voltages and the wanted load voltages the required injected DVR voltages can be calculated. Taking the actual converter currents into account the expected voltage drop across the line-filter can be calculated and the DVR reference voltages to the converter can be given.

In the feedback control, either the load voltages or the DVR voltages are measured and used in a feedback loop. The method has the potential of a fast and more correct response, but the tuning of the voltage controllers are complex and depends on the connected load. Fig. 5.9 illustrates the principles in the feedback control with the load voltages used as feedback signals. The converter currents are not necessarily used in the feedback control, because the voltage drop across the line filters are handled by the voltage controllers. The supply voltages are still measured to have a voltage dip detection and synchronization. Multi-variable control is used

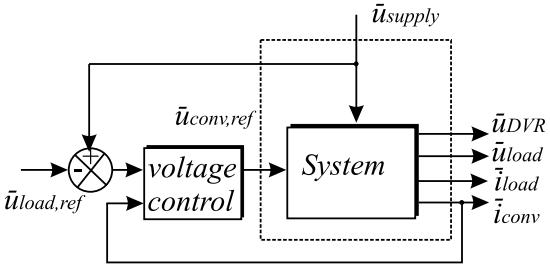


Figure 5.8: *Feedforward control of the load voltage in a DVR.*

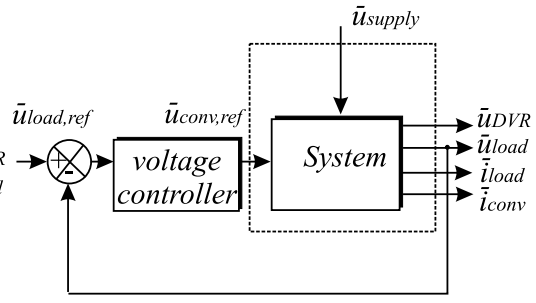


Figure 5.9: *Feedback control of the load voltage in a DVR.*

in [71] with an inner current loop to control the current in the filter capacitors and an outer voltage loop to control the DVR voltage. It is reported as a robust and fast control method.

Feedforward controllers

In feedforward control the reference parameter is the wanted load voltages, $u_{load,ref}$ and the error, $u_{supply,error}$ between actual supply voltage and reference load voltage must be injected by the DVR:

$$\overline{u}_{supply,error} = \overline{u}_{load,ref} - \overline{u}_{supply} \tag{5.20}$$

A voltage drop in the line-filter and the injection transformer can be expected and this voltage drop, u_{drop} can also to some extend be compensated with a feedforward control before the DVR voltage is injected by:

$$\overline{u}_{conv,ref} = \overline{u}_{supply,error} + \overline{u}_{drop} \tag{5.21}$$

Only the stationary 50 Hz voltage drop is expected to be compensated. Feedforward control has been tested both for the LV- and HV-DVR without compensation of the line-filter voltage drop.

Feedback controllers

One method in the feedback control is to set a reference for the load voltage, $u_{ref,load}$ and correct the error with a voltage controller:

$$\overline{u}_{load,error} = \overline{u}_{load,ref} - \overline{u}_{load} \tag{5.22}$$

$$\overline{u}_{conv,ref} = \overline{u}_{load,error} G_{controller} \tag{5.23}$$

With an infinite fast control and infinite DVR rating the load voltage would be an ideal voltage and non-ideal supply voltages would be out compensated. With the load voltage used as reference the controller tries to control the load voltage to a symmetrical and ideal voltage.

An alternative method sets the load voltage as reference $u_{load,ref}$, calculates the wanted DVR voltage on the basis of the actual supply voltage and any deviation is going to be injected by the DVR, $u_{DVR,ref}$. The method is depicted in Fig. 5.10. A voltage controller handles any error between actual DVR voltage, u_{DVR} and the reference DVR voltage:

$$\overline{u}_{DVR,ref} = -\overline{u}_{load,ref} + \overline{u}_{supply} \tag{5.24}$$

$$\overline{u}_{DVR,error} = \overline{u}_{DVR,ref} - \overline{u}_{DVR} \tag{5.25}$$

$$\overline{u}_{conv,ref} = \overline{u}_{DVR,error} \cdot G_{controller} \tag{5.26}$$

The method gives a better opportunity to distinguish between how much the DVR injects, and sets up the limits for the voltage injection according to the DVR hardware. A fast control can be obtained with feedback control, but the controller must be well designed in order to obtain a stable system.

The performance of the closed loop control depends on the type of controller used. The controller has to be able to stabilize the load voltage, hence stabilize the positive voltage component and damp the inverse voltage component.

Comparison of the feedback and feedforward control

In Table 5.1 some of the main differences between the feedback and the feedforward control are listed. From Table 5.1 it can be seen that feedback control requires more concern in the controller design, but it has the potential of a superior performance. Adding other tasks to the DVR control e.g. harmonic blocking or compensation of the harmonic voltage drop caused by nonlinear loads also require feedback control.

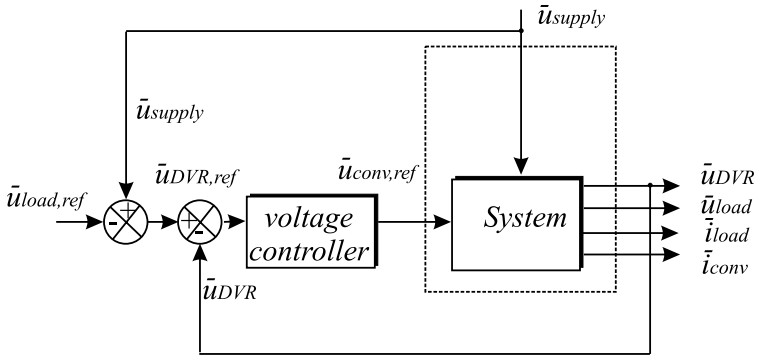


Figure 5.10: *Modified feedback control, where the DVR voltages are calculated and used in a feedback control.*

	Feedforward control	**Feedback control**
Voltage sensors	3(6)	6
Response time	-Fast, depends on the system.	-Medium, controllable via the controller.
Stationary error	-Can be low with voltage drop compensation.	-Can be eliminated.
Transient over shoot	-Difficult to control.	-Controllable.
Stability	-Good.	-Instability risk.
Compensation of DVR generated harmonics	-Difficult to control.	-Can be reduced.
Switching harmonics	-Do not enter the control.	-Enter the control.
Compensation of background harmonics	-Almost impossible.	-Possible.
Compensation of non symmetrical faults	-Slow, possible.	-Good.
Load voltage distortion at non-linear loads	-High.	-Can be reduced.

Table 5.1: Comparison of feedforward and feedback control.

Stationary and rotating reference frames

From Fig. 5.8 an Fig. 5.9 the basic control methods can be implemented in a number of ways. Each phase could be controlled individually with RMS calculation of each supply voltage and an injection of the missing voltage. (5.27) illustrates an

example of the calculation of the RMS voltage:

$$U_{RMS} = \sqrt{\frac{1}{T}\int_{t_1}^{t_2} u(t)^2 dt} \tag{5.27}$$

In order to have a tracking of the 50 Hz component, the difference between t_1 and t_2 must at least be 10 ms, and a slow response-time above 5 ms can be expected. Beside the RMS value the phase angle of each voltage must be estimated from for instance detection of the zero crossing.

Discrete Fourie Transformation (DFT) can also be used to detect the fundamental 50 Hz component and the associated phase angle. The method is also slow and requires a large amount of data processing. (5.28) illustrates the DFT method.

$$X(m) = \sum_{n=0}^{N-1} x(n) e^{j2\pi mn/N}, 0 \leq n \leq (N-1) \tag{5.28}$$

N is the size of the data array and a calculation of one element requires (N-1) complex multiplications and (N-1) complex additions. Using DFT is time consuming and difficult to implement in real time control.

A high bandwidth is required to protect very sensitive loads, and therefore only instantaneous compensation and detection methods of voltage dips are further considered. The control of the fundamental voltages is for all the described methods done in the time domain. The frequency domain can in some cases be used for harmonic blocking, which could be a secondary task for the DVR.

The voltage control is often implemented in different reference frames. The objective by using another reference system is to simplify the control or improve the performance. The typically used reference frames are:

- Stationary reference frames
  - Three-phase system (RST)
  - Space vector system ($\alpha\beta 0$)
- Rotating reference frames
  - Synchronous rotating system(dq0)
  - Inverse rotating system (-dq0)

In the stationary RST reference frames the current and voltages are sinusoidal quantities. A coordinate transformation of the RST-system to a space vector representation can often be advantageous. The transformation is:

$$\overline{u}(t) = \frac{2}{3}(u_R(t) + u_S(t)e^{j\frac{2\pi}{3}} + u_T(t)e^{j\frac{4\pi}{3}}) = u_\alpha(t) + ju_\beta(t) \tag{5.29}$$

Rewritten to a matrix representation, the matrix can be written as:

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} u_R \\ u_S \\ u_T \end{bmatrix} \tag{5.30}$$

Zero sequence values are eliminated and with symmetrical phase voltages the resulting space vector rotates with a constant angular velocity and it has a constant magnitude. Transformation to a rotating system can often lead to further simplifications and improvements of the control system. The transformation to a rotating dq-frame is shown in:

$$\overline{u}_{dq}(t) = u_d(t) + ju_q(t) = (u_\alpha(t) + ju_\beta(t))e^{-j\theta} \tag{5.31}$$

The transformation matrix can here be written as:

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} \tag{5.32}$$

The control principle in the rotating dq reference frame is illustrated in Fig. 5.11. The Phase Locked Loop (PLL) synchronizes to the positive sequence component in the supply voltages, and with symmetrical voltages $u_{supply,d}$ is a DC value and equal to the peak value of the phase voltages and $u_{supply,q}$ is zero.

Setting a DC-value for the d-reference $u_{load,ref,d}$ the DVR converter is set to generate a voltage in-phase with the supply voltage and the q-reference component $u_{load,ref,q}$ indicates a voltage perpendicular to the supply voltage. Setting the q-reference to zero the DVR only injects a voltage in-phase with the supply, which is an effective way to increase or decrease the load voltage. The dq-reference values are then transformed back to the rotating reference frame with the transformations-angle θ_{PLL} and thereafter to the reference phase values $u_{conv,ref,R}$, $u_{conv,ref,S}$ and $u_{conv,ref,T}$.

In the control of dynamic voltage restorer both stationary and rotating control have been tested in [33] and only very small differences have been registered in the performance. Generally, the use of a rotating dq-frame has the widest acceptance.

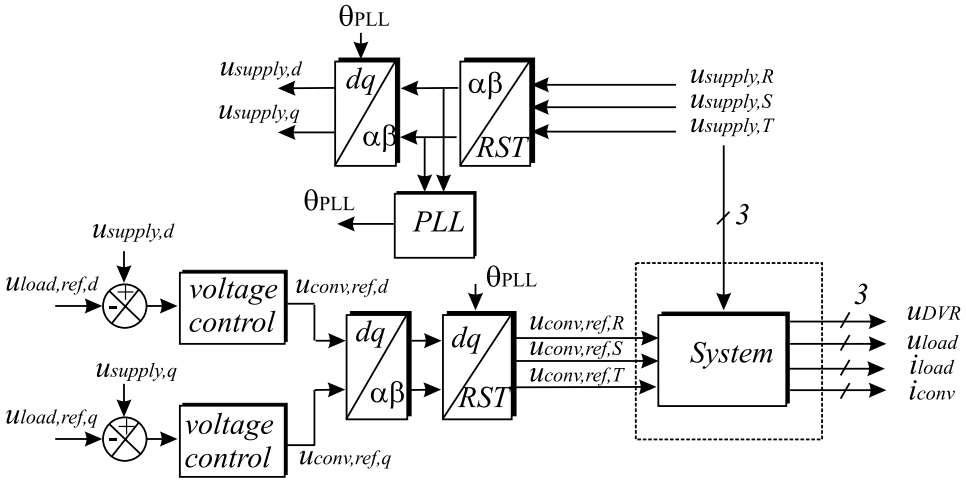


Figure 5.11: Feedforward control in the rotating reference frame.

Load voltage controllers to control the non-symmetry Compensation of the negative sequence component is in the most cases wanted and the dq-reference frame is not always a good reference frame to handle negative sequence components.

The negative sequence components appear as 100 Hz component in the dq-frame and if the DVR control system is only equipped with a d- and a q-controller the controller will damp the 100 Hz component according to the bandwidth of the used controller.

A method proposed in [58] and [59] uses the transformation to a negative dq-frame (dq-)-system. Thereby the negative sequence system appears as DC-values. (5.33) shows the transformation:

$$\overline{u}_{(dq-)} = \overline{u}_{\alpha\beta}(t)e^{j\theta} \tag{5.33}$$

The (dq-)-frame still contains the positive sequence component and the DC-component from the negative sequence. The negative sequence component can be extracted by calculating a mean value of a 10 ms moving window. Using a window size of 10 ms, the positive sequence components equals zero in mean value. The mean value in the (dq-)-system, must be calculated both for the d- and q-component, according to:

$$u_{(d-),mean}(t) = \frac{1}{T}\int_{t-T}^{t} u_{(d-)}(t)dt \tag{5.34}$$

$$u_{(q-),mean}(t) = \frac{1}{T}\int_{t-T}^{t} u_{(q-)}(t)dt \tag{5.35}$$

Calculation of the mean value in a DSP requires storing of data. In the case of a sampling frequency equal to 5 kHz an array of 50 elements must be stored:

$$n_{data} = f_{sw} \cdot 10\,ms = 50 \tag{5.36}$$

Practical calculations of the mean value can be done by adding the new value, u(n) and subtracting the oldest value u(n-50) to a sum, u_{sum}. Thereafter the mean value can be calculated:

$$u_{sum}(n) = u_{sum} + u(n) - u(n-50) \tag{5.37}$$

$$u_{mean}(n) = \frac{1}{T}u_{sum} \tag{5.38}$$

Instead of mean value the DC-value may be extracted by filtering technics, which for low order filters require less storage of data. For higher order of filters the calculation can be larger than the mean value calculation.

The extracted result of the negative sequence component can be used for reducing non-symmetry in the load voltage. Here both feedback and feedforward control of the negative sequence component can be used. The reference value of the negative sequence component, $\overline{u}_{(dq-),ref}$ is most likely set to zero in order to have symmetrical load voltages.

The compensation of the negative component with a dedicated control setup is much slower compared with the positive sequence controller. The time constant

of a feedforward control is in the order 5 - 10 ms before the DVR effectively can compensate for the non-symmetrical voltage.

For both feedforward and feedback methods this (dq-)-transformation appear to be the most promising method to separately control positive and negative sequence components.

5.4.2 DC-link voltage controllers

So far the control of the AC voltages across the DVR has been analyzed. In this section different methods to control the DC-link voltage are further described.

The DC-link voltage can to some degree be controlled by the series DVR converter. In [80] the DVR converter is used to charge the DC-link and the attached batteries, but often the DC voltage is controlled by an externally DC-link charger. Some DVR system topologies give the opportunity to control the DC-link voltage and other topologies have are relative uncontrollable DC-link voltage. The DC-link voltage can with some DVR hardware be chosen to be kept constant at all times. With a constant DC-link voltage the generated DVR voltage can always be at maximum. Other concerns may lead to controllable variations in the DC-link voltage. Losses are lower with a small DC-link voltage and during a voltage dip the rating of the DC-link charger may give limitations in the ability to maintain a constant DC-link voltage.

The two main topologies, which are capable of maintaining a constant DC-voltage are a DVR with an active shunt converter (AC/DC converter) or a topology with a separate energy DC-storage and a DC-link (DC/DC converter). An other more simple charger could be a diode charger connected to the supply side or to the load side of the series converter and the DC-link voltage depends on the supply or the load voltages.

With the series converter to control the DC-link voltage a voltage drop across the DVR has to be controlled to take power from the supply to charge the DC-link voltage. The load voltage is a summation of the supply and the DVR voltage:

$$\underline{U}_{load} = \underline{U}_{supply} + \underline{U}_{DVR} \tag{5.39}$$

The DVR voltage is equal to the generated converter voltage (U_{conv}) subtracted line-filter voltage drop.

$$\underline{U}_{DVR} = \underline{U}_{conv} - \underline{U}_{line-filter} \tag{5.40}$$

To be able to charge the DC-link the injected converter voltage must include a charging voltage drop, which corresponds to a resistive voltage drop across the DVR. In order to control the load voltages to rated values the DVR can circulate reactive power. The ability to take active power from the grid and still maintain a rated load voltage depends on the grid strength, the supply voltage level, resistive and inductive voltage drop caused by the line-filter and finally the apparent power absorbed by the load,

$$\underline{U}_{load} = \underline{U}_{supply} + \underline{U}_{conv} - (\underline{Z}_{line-filter})\sqrt{3}\underline{I}_{load} \tag{5.41}$$

A current has to flow to the load in order to be able to charge the DC-link and the charging voltage is always in-phase with the load current. During low load currents the charging voltage has to be increased to ensure a fast charging. In this condition the voltage drop across the line-filter, supply line etc. are also low and a higher charging voltage can be accepted.

5.4.3 Synchronization with the supply

Synchronization to the supply voltages is essential in order to control the DVR and during a dip the pre-dip conditions should somehow be registered to maintain undisturbed load voltages. Synchronization methods are used in many other applications for FACTS and active converters operating at the grid. A phase locked loop (PLL) circuit to track and filter the fundamental component is the dominating method. In [71] two other methods have been tested, which are a Kalman filter and a Discrete Fourier Transformation (DFT).

A significant difference between DVRs and other applications is the PLL′s response during a phase jump. Other applications have to detect the jump and change according to the new supply voltage. The DVR has to be able to synchronize to the pre-dip situation and inject the missing voltage. A so called freezing to the pre-dip conditions for a DVR has been described in [32]. The operation and circuit for a PLL circuit has been further described in [38]. The tuning, response and robustness to background voltage quality problems have been further described in [20] and [62]. A relative slow PLL has been chosen for the DVR. Thereby the influence from harmonics, non-symmetrical voltages etc. remains low. The detection circuit freezes the PLL in the case of a voltage dip. Fig. 5.12 illustrates the discrete PLL used to synchronize the DVR.

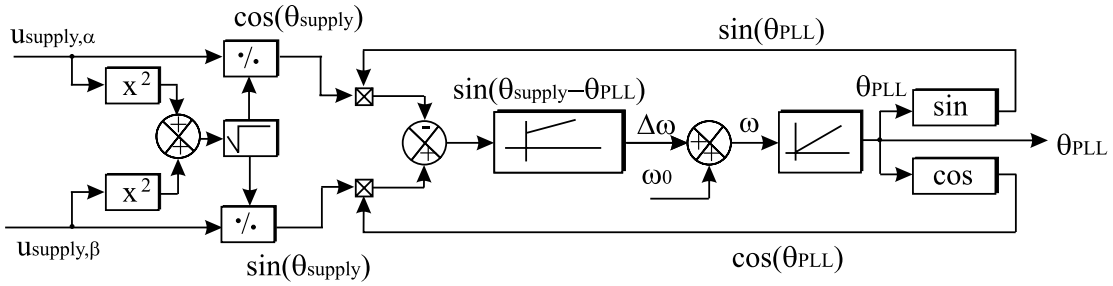


Figure 5.12: Phase locked loop to synchronize the DVR to the supply voltages.

The PLL locks to the supply angle with a preferable low phase delay from the input to the output, damp the background harmonics, non-symmetrical voltages etc. The angle between the supply and PLL output, which should be minimized can be described as,

$$\Delta\theta = \theta_{supply} - \theta_{PLL} \tag{5.42}$$

Instead of minimizing $\Delta\theta$, $\sin(\Delta\theta)$ is controlled with a PI controller. The trigonometric function for sin $\Delta\theta$ can be stated as:

$$sin(\theta_{supply} - \theta_{PLL}) = -sin(\theta_{supply})cos(\theta_{supply}) + sin(\theta_{PLL})cos(\theta_{supply}) \quad (5.43)$$

The angle θ_{supply} of the supply is found according to:

$$sin(\theta_{supply}) = \frac{u_\beta}{\sqrt{u_\beta^2 + u_\alpha^2}} \quad (5.44)$$

$$cos(\theta_{supply}) = \frac{u_\alpha}{\sqrt{u_\beta^2 + u_\alpha^2}} \quad (5.45)$$

The angle of the PLL is found through an integration of the rated angular velocity (ω_0) and the velocity difference between the the supply and PLL ($\Delta\omega$):

$$\theta_{PLL} = \int_0^\infty (\omega_0 + \Delta\omega)dt \quad (5.46)$$

The PLL circuit is transformed to the z-plane and is implemented in the DSP controller. The integrators in the PI controller have been supported with anti-windup and the PLL angle (θ_{PLL}) is initialized before overrun.

Precautions at phase jumps must be taken to avoid wrong compensation during voltage dip with phase jumps. If the PLL is fast the DVR will not be able to see the phase jump and it will only compensate for the missing magnitude. Using a slow PLL the velocity of the PLL will hardly change and it will be seen as a suddenly q-component in the supply voltage and the DVR can be controlled to compensate for the phase jump. A very slow PLL may give synchronization problems at start up, at frequency variations and during non-ideal phase jumps.

The transfer function for the PLL is highly non-linear due to the trigonometric functions and multiplications. Therefore, an analytic analysis and design of the PLL is troublesome. A tuning of the PLL is in this thesis primarily based on simulations.

5.4.4 Voltage dip detection

An essential part of the control of a DVR is the detection circuit. A voltage dip must be detected fast and corrected with a minimum of false operations. The detection circuit operates the DVR from standby to active mode and vice versa. Parameters for the detection circuit are:

- Robust operation with the presence of background voltage quality problems.
- Fast voltage dip detection and transition to active operation to minimize load under voltages.
- Detection of a restored supply voltage and transition from active to standby operation and a minimization of load over-voltages.

These are the main parameters to the detection circuit. Methods to achieve a fast detection is to use instantaneously measurements instead of RMS based calculations. The measurements of the supply voltage gives the instantaneously voltage and the transformation of the supply voltages to a rotating or a stationary reference can in some cases be advantageously. Three voltage dip detection methods are here presented:

1. Magnitude of the space vector in $\alpha\beta$-reference

$$| \overline{u}_{supppply,\alpha\beta} | = \sqrt{u^2_{supply,\alpha} + u^2_{supply,\beta}} \tag{5.47}$$

$$| \overline{u}_{supply,\alpha\beta} | < u_{threshold} \tag{5.48}$$

2. Length of the d-component and q-component in the dq-reference frame comparing each values with threshold values.

$$u_{supply,d} < +u_{threshold} \tag{5.49}$$

$$-u_{threshold} > u_{supply,q} > +u_{threshold} \tag{5.50}$$

3. Length of the error vector comparing with a threshold value.

$$| \overline{u}_{error,dq} | = \sqrt{(u_{ref,d} - u_{supply,d})^2 + (u_{ref,q} - u_{supply,q})^2} \tag{5.51}$$

$$| \overline{u}_{error,dq} | > u_{threshold} \tag{5.52}$$

The detection circuit depends on the DVR hardware and control strategy. E.g. the zero sequence components and phase jump are going to be detected and compensated.

All the three methods can detect a large symmetrical voltage dip without any phase jump. A non-symmetrical voltage dip on the other hand can give some problems in the detection. The voltage dip can often give the appearance that the supply voltages are restored. Fig. 5.13a illustrates a very typically single-phase fault on a higher voltage level. The dashed line indicates the non-faulted voltages and the solid line the faulted voltages. At t = 10 ms the instantaneous values are equal in the faulted and the non-faulted case even though the fault still persist.

Fig. 5.13b-d illustrates how the the three different methods detects this type of fault. At t = 11.7 ms the d-component has reduced to 90 % of the rated value in Fig. 5.13c and the the error in Fig. 5.13d is above 10 %.

The case illustrates that the detection of a small non-symmetrical voltage dip can be delayed and the delay depends on the time the fault occur and once the voltage is detected below a certain threshold value the DVR has to continue to be active even though the voltage seems to be restored. All the methods are equally effective in the detection of this type of non-symmetrical fault.

If the voltage dip contains a phase jump method 1 will only detect the voltage reduction, but not the phase jump. In the methods 2 and 3 a phase jump will lead to a reduction in both the d- and q-component. Detection method number 3 is chosen,

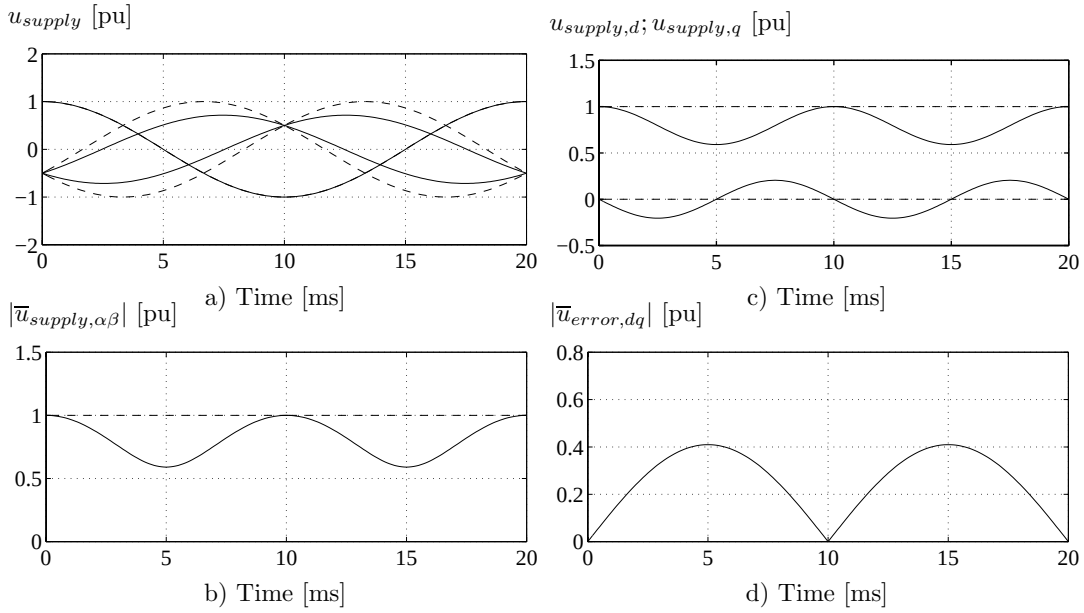


Figure 5.13: *Detection of a non-symmetrical voltage dip. a) RST-system with the faulted and non-faulted voltages (dashed), b) method 1 amplitude of the space vector, c) method 2 evaluation of the d- and q-component and d) method 3, the magnitude of the error vector.*

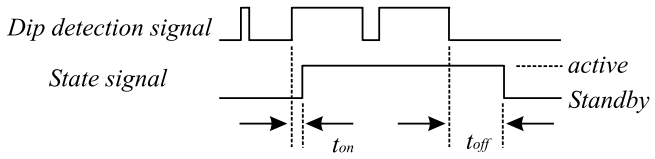


Figure 5.14: *The operation principle of the detection circuit with short pulse prevention and turn-on and turn-off delay.*

because it gives the ability to detect phase jump and only one parameter has to be compared.

It is undesirable if the converter often changes state from active to standby mode. During a state change the DVR can cause oscillations, generate harmonics and distorte the load voltages. To avoid frequent shifts from active to standby mode a kind of hysteresis control is embedded. Two digital filters have been used, the first is a low-pass filter with a high bandwidth (1 kHz), which ensures that the DVR very fast goes into active mode and a slow low-pass filter (50 Hz), which takes the DVR slowly back to standby mode. The result is that very short transients are not detected as a voltage dip and once the DVR is set in active mode, a certain time without any under-voltage must pass before the DVR is taken from active to standby mode. Fig. 5.14 illustrates the principle operation of the detection circuit.

5.5 Modulation strategy

The section gives a small presentation of some relevant modulation strategies for a DVR and focus is put on a modulation strategy for the chosen full bridge DVR power topology.

Generally, modulation strategies for power converters have lead to numerous methods. The primary goals are to minimize losses, generation of harmonics and calculation requirements. Three fundamental methods are generally considered controlling the modulation of converters, which are:

- Pulse width modulation (PWM)
- Square wave modulation
- Pulse amplitude modulation (PAM)

The PWM modulation of a DVR converters is considered to be the best choice, because a DVR requires a fast response and a small generation of harmonics.

A variety of PWM schemes exist for different converters and applications. A survey for PWM methods is given in [13]. Special considerations are relevant regarding PWM schemes for DVRs. Similarities can be seen between active shunt converters and the series connected DVR.

Traditionally PWM methods are divided into open and closed loop PWM [13]. Current is typically feedback in closed loop PWM and in the control of a DVR current loops are often avoided. Focus is thereby concentrated to open loop PWM methods, which are often categorized by the use of carrier functions. Some relevant PWM methods for full bridge converters are:

- Carrier based PWM
  - Sub-oscillation modulation
  - Space vector modulation
  - Harmonic elimination modulation
  - Optimized modulation
- Carrierless PWM
  - Random PWM

Carrier based sub-oscillation modulation is the method reported for a DVR in [32]. The carrier based sinus modulation for a full bridge converter is illustrated in Fig. 5.15a with a unipolar switching scheme. The phase values are compared with two triangular carrier functions and the result is the control signals for the six upper switches in the three full bridges.

The space vector modulation have been used in [81] and the space vector modulation is illustrated for a full bridge converter in Fig. 5.15b [12]. The large crosses æ+æ indicate the possible vectors in the space vector plane and the æ(xxx)æ indicate

the switching conditions to achieve the actual vector. For instance the (+0-) condition indicates that the first full bridge is controlled to generate a positive voltage, the second full bridge a zero voltage and the third full bridge a negative voltage. The circle indicates a possible path for a space vector to generate a symmetrical DVR voltage.

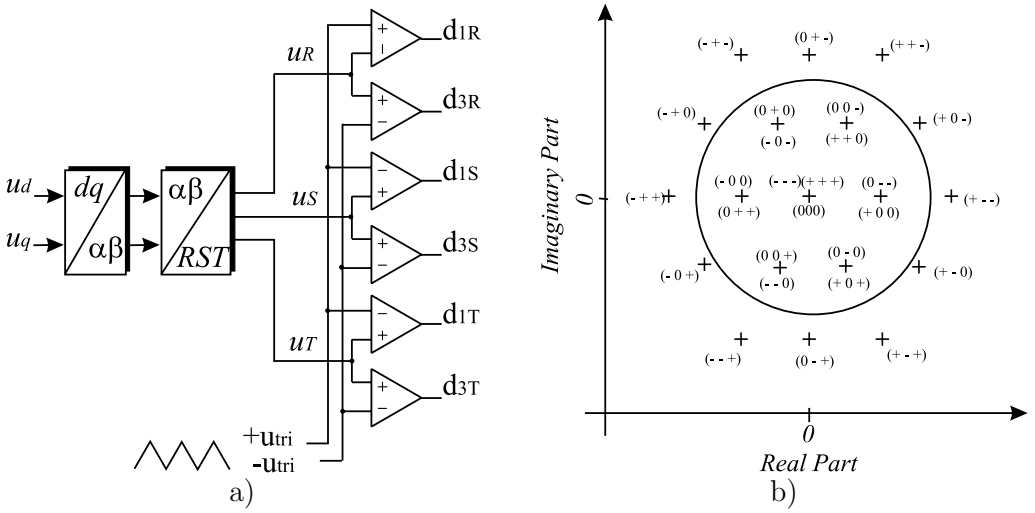


Figure 5.15: *Modulation methods. a) Carrier based sinus modulation with a unipolar switching scheme for the full bridge converter and b) space vector modulation for the full bridge converter. (0) indicates a zero voltage, (+) a positive voltage and (-) a negative voltage.*

In the optimized methods a weight function of the harmonic components may be minimized numerically to lower the total harmonic distortion [12].

Using carrierless PWM the switching harmonics can be spread out and a smaller filter can be used to be below emission standards. Having the risk of initiating resonance frequencies is larger with this method and therefore not selected.

Several modulation methods generate zero sequence voltages to utilize the DC-link voltage better. For instance by adding a third harmonic in the reference to the carrier based sinus modulation and also the space vector modulation can generate zero sequence components. In the chosen topology with single-phase transformers and full bridge converters the zero sequence system would be transferred to the primary side, and for the LV-DVR it would influence the neutral to phase voltages. In the HV-DVR the injection of a zero sequence components would not be transferred to the LV loads, because of the delta/wye 10/0.4 kV transformers. Still the injection of zero sequence components is omitted since it could interfere with the ground fault detection in a high impedance grounded system. Discontinuous PWM methods also inject zero sequence components and will not be further considered [12].

Changing the converter hardware and the DVR coupling to the supply with the injection transformers can change focus of the modulation strategy, and with an open star/delta injection transformer the zero sequence can be manipulated freely. However this is not done in this thesis.

5.6 Design of the DVR control

The controllers for the DVR are here designed on the basis on the available hardware. The main control parameters for the LV- and HV-DVR are presented.

5.6.1 Design of the AC voltage controllers

Different DVR voltage controllers have been tested by simulations, and tested both on the LV- and HV-DVR.

Simplifying the system gives a good indication of the very important control aspects of a DVR. The DVR, in a single-phase diagram, is illustrated in Fig. 5.16. The supply voltage is by superposition set to zero and the supply impedance is usually very low and here also set to zero. The converter (U_{conv}) is assumed ideal and the DVR is drawn with an LCL line-filter with no losses in the line-filter. Additionally, the load is assumed linear and resistive (R_{load}).

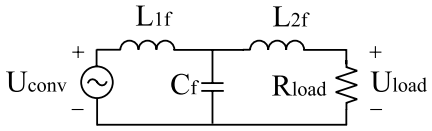


Figure 5.16: *The simplified DVR diagram with the main components.*

For a DVR system with only a L line-filter the transfer function can be simplified to:

$$G_{system}(s) = \frac{1}{1 + \frac{L_{1f}}{R_{load}} s} \tag{5.53}$$

The function is a first order system and the filter inductor value is fixed, but the load can change and thereby the time constant of the system. Adding a capacitor to the line-filter (LC-filter), a second order system appears with the following transfer function:

$$G_{system}(s) = \frac{1}{1 + \frac{L_{1f}}{R_{load}} s + L_{1f} C_f s^2} \tag{5.54}$$

In this case the resonance frequency is set by the filter and the damping is inverse proportional to the resistive load. The LV-DVR (5.54) is close to the actual transfer function.

The HV-DVR has a filter inductance on the LV-side(L_{1f}) and a filter inductance from the step-up transformer(L_{2f}). The filter is an LCL-filter and the transfer function can now be extended to:

$$G_{system}(s) = \frac{1}{1 + \frac{L_{1f}+L_{2f}}{R_{load}} s + C_f L_{1f} s^2 + \frac{L_{1f} L_{2f} C_f}{R_{load}} s^3} \tag{5.55}$$

Such a system has three left side poles, two poles are complex close to the real y-axis and a real pole on the x-axis. The step response of the system changes according to

the load. The step response of the open loop transfer function is illustrated in Fig. 5.18a for three different load conditions.

In order to be able to design a closed loop controller other aspects have to be included. The control hardware has one sample delay from the beginning of the measurement to the change of the switchings. In z-domain the delay can be included as:

$$G_{delay}(z) = z^{-1} \tag{5.56}$$

In front of the A/D conversion an anti-aliasing filter is placed and the filter model is included in the system analysis:

$$G_{af}(s) = \frac{1}{1 + R_{af}C_{af}s} \tag{5.57}$$

The closed loop controller is chosen relatively slow and the main purpose with the closed loop control is to achieve compensation of the fundamental symmetrical voltage. The transfer function for the system is in the RST system and the PI-controller is kept in the rotating system to simplify the controller design. The PI-controller model in z-domain is:

$$G_{controller}(z) = K_p + \frac{K_i}{z - 1} \tag{5.58}$$

The PI controllers are equipped with anti windup and the simplified system diagram is illustrated in Fig. 5.17.

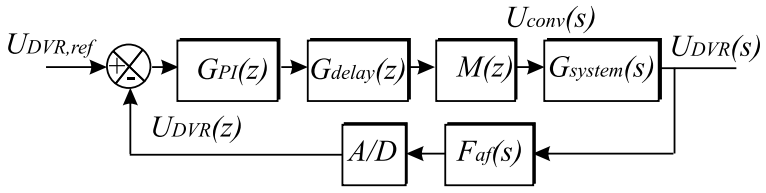


Figure 5.17: *The simplified block diagram of the DVR.*

Simulations are performed to verify the designed controller and the values are K_p = 0.0125, K_i = 0.01. The approximate rise time is 15 ms with very little overshoot even for light loads. The closed loop response with the load parameter variation (R_{load} = 1 pu, 4 pu, 9 pu) is simulated and shown in Fig. 5.18b.

5.6.2 Design of the synchronization controller

An exact response-time is not essential but an over-damped response is seeked to avoid oscillations and overshoot in the operating range. The PLL is constructed only to detect one rotational direction. The goal is to construct the PLL to synchronize with the positive sequence system in the measured supply voltage, suppress harmonics and negative sequence components. The parameters for the PLL are shown in Table 5.2.

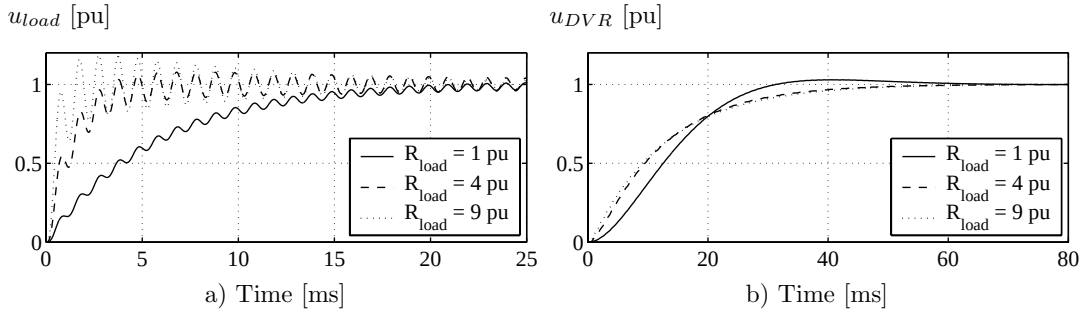


Figure 5.18: *a) Open loop step response for the HV-DVR with a LCL-filter and variation of the resistive load. b) Closed loop step response for the HV-DVR with a LCL-filter and variation of the resistive load.*

5.6.3 Design of the saturation controller

During the testing of the HV-DVR the series transformers were often driven into saturation, which lead to an over-current in the converter module. To overcome this problem and to maintain high utilization of the injection transformers and a high bandwidth of the DVR control saturation controllers were developed.

The controller is designed to limit the converter reference voltages ($u_{conv,ref}$) when the converter currents are above twice the rated converter current. The injected converter voltage is limited to zero until the reference voltage has reversed. The saturation control is illustrated in Fig. 5.19.

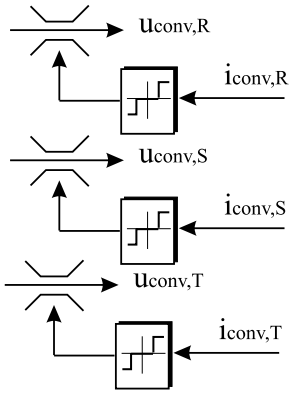


Figure 5.19: *Saturation control of the injection transformers on the basis of the individual phase currents.*

5.6.4 Design of the modulation

Unipolar sinusoidal modulation has been implemented. For each phase four timer values are calculated for the compare unit in the Micro Controller. The four timer values are calculated on the basis of a triangular voltage source u_{tri} and the inverse triangular voltage source $-u_{tri}$. Two triangular sources are compared with the reference voltage $u_{ref}(t)$ and the four timer values can be calculated. Fig. 4.7 page 59 illustrates the modulation principle for one phase and the same is done for the other phases.

Parameter	**Abbreviation**	**LV-DVR**	**HV-DVR**
PLL	Proportional gain, K_p	25	25
	Integration time, T_i	10 ms	10 ms
Control method		Feedforward	Feedforward/feedback
	Proportional gain, K_p	-	0.0125
	Integration time, T_i	-	33 ms
	f_{sw}	5 kHz	3 kHz
	I_{sat}		500 A
Reference voltage	$u_{ref,d}$	325 V (1.0 pu)	8100 V (1.0 pu)
DC-link	$U_{DC,ref}$	560 V	600 V

Table 5.2: Main control values for the LV- and HV-DVR.

5.7 Summary and conclusion

The chapter deals with the overall control strategy for a DVR, and some of the main subjects and conclusions have been:

- The main purpose of a DVR is the control of the fundamental voltage, but the possibility to add other tasks to the DVR exists. DVR limitations have been discussed, which could influence the control strategy. Different operation modes have been described for a DVR including standby mode, active mode and bypass mode, which have been incorporated in the control.

- Different control strategies have been treated, such as voltage quality optimized control, voltage amplitude optimized control and energy optimized control. The control methods have been discussed with respect to voltage quality, voltage injection, power drain of the energy storage and how it may the influence the connected load.

- In Section 5.3 the control strategy has been treated with focus on the type of load to protect and how it could affect the voltage drop across the DVR, the load voltage quality and the risk of load tripping.

- The AC load voltage controllers have been discussed in Section 5.6, whether to have feedforward and/or feedback control of the load voltages and which reference frames could be used. Control with instantaneous values in a rotating dq-reference frame is used, which to some degree is sufficient to control positive and negative sequence components and the zero sequence components is removed with this type of control. The control of the DC-link voltage has been discussed and an external DC-link charger is used to simplify the control of the series converter, and avoid increased voltage drop across the DVR.

- The detection of a symmetrical and non-symmetrical voltage dips has been dealt with in Section 5.4. Three methods to detect a voltage dip have been discussed and one method have been chosen for the further control.

- A carrier based modulation strategy for the DVR has been chosen on the basis of some possible modulation methods.

- The last section includes a presentation of the designed control system for the LV and HV-DVR with some of the main differences in the control of the two DVRs.

Chapter 6

Simulation of a DVR system

The chapter includes modelling of the DVR system components to be able to simulate the performance of the LV- and HV-DVR. The models have been implemented in Saber and simulations are shown from both the LV- and HV-DVR. Simulations are compared with measurements from the LV- and HV-DVR to verify the models of the DVRs.

6.1 Modelling of the system components

The system is modelled and the models have been implemented in Saber and used for simulation of the DVR. The model and simulations have been used to:

- Gain general understanding of the DVR working principles and protection issues.
- Test different DVR designs including the converter, transformer, line-filter.
- Design the DVR controllers including bandwidth and dynamic response estimations.
- Test different types of voltage dips and different load conditions.
- Preparation of the high voltage - high power tests of the HV-DVR.

The modelling have been kept relatively simple to keep simulation time low. The system is reduced to three main elements, which is a simplified model of the supply, the DVR and the load.

6.1.1 Modelling of the supply and the voltage dips

The supply is modelled as three ideal phase voltages with a supply impedance. Two methods have been used to generate voltage dips, which are:

- The magnitude of the supply voltages are changed according to wanted voltage dip. The voltage dip in the simulations can be defined by its content of positive sequence system, content of negative sequence and the phase jump. The method is easy to simulate and it gives very ideal voltage dips. This is the only method used for simulations of the LV-DVR.

- An actual short circuit is generated, and thereby the voltage dip will arise according to the impedance conditions. The method is illustrated for the HV-DVR in Fig. 6.2. The short circuit currents are measured, and the short circuit is cleared during zero current crossing. The short circuits in this Fig. can be both generated at the LV-side of the transformer and at the same voltage level as the DVR.

The LV-DVR is tested with a programmable three-phase 400 V supply, which have a supply impedance of ($Z_{supply} = 0.04\ \Omega$). The simulation setup for the LV-DVR is illustrated in Fig. 6.1.

The simulation of the HV-DVR has been performed with the parameters, which are expected at the test location for the HV-DVR. For the simulation of the HV-DVR a three-phase supply is inserted at the 10 kV level, and included in the supply impedance (Z_{supply}). The inserted supply impedance include impedance from the 10 kV feeding point to an infinite busbar and impedance from the 10 kV over-head wires and cables from the 10 kV feeding point to the connection point of the DVR.

A high ground resistance has been inserted to simulate the DVR in a high impedance grounded system.

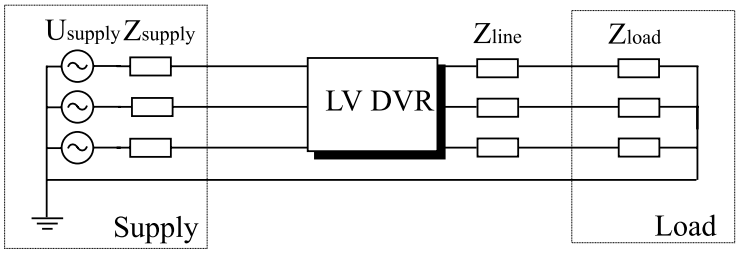


Figure 6.1: *LV-DVR with a three-phase supply. The neutral is connected to the LV-load, which is star connected.*

6.1.2 Modelling of the dynamic voltage restorer

The model of the dynamic voltage restorer can in some cases be simplified to controllable sinusoidal voltage sources, but for a more precise model the Pulse Width Modulator and line-filter should be included. The model should give an idea about the possible bandwidth of the DVR and the injection of harmonics by the switching voltage source converter. Finally, the model is used for the design process.

Modelling of the injection transformer

Two types of injection transformers have been used for the two DVR prototypes. The LV-DVR transformer has a voltage ratio of 115/230 V, and the HV-DVR transformer has a voltage ratio of 2900/290 V. The winding to the supply side is always designated as the primary-side and the winding to converter side is designated the

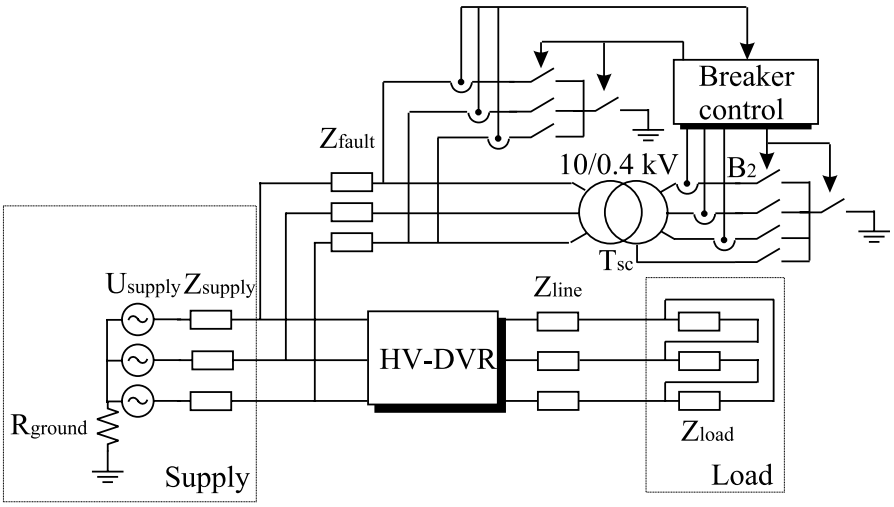


Figure 6.2: *HV-DVR with a three-phase supply, breakers at the HV- and LV-side to initiate short circuits and a delta connected load.*

secondary-side. The two transformers are modelled equally despite that the converter switches directly into the LV-DVR transformer. In the HV-DVR transformer the PWM voltages are filtered before they are applied to the transformer.

Included in the transformer models have only been resistance to model copper losses (R_{tra}), inductance to model leakage flux (L_{tra}) and the transformer ratio (n).

The series transformers have been designed very close to traditional shunt transformers, which means at rated voltage the transformer is very close to saturation. The non-linear effects caused by the magnetization is not included in the model. A natural extension of the model would be to include the hysteresis, pre-magnetization level and saturation curve of each transformer.

Modelling of the line-filter

The line-filter is modelled with ideal filter components, though both the filter capacitor and filter inductor is expected to vary with the frequency. The line inductor for the HV-DVR is modelled with inductance (L_{1f}) and expected resistance (R_{1f}) and the filter capacitor is modelled as a pure capacitance (C_f) according to:

$$u_{1f}(t) = L_{1f}\frac{di(t)}{dt} + R_{1f} \tag{6.1}$$

$$i_{cf}(t) = C_f\frac{du_{cf}(t)}{dt} \tag{6.2}$$

The HV-DVR filter inductor is an air inductor, but still the winding to winding capacitance may give a different transfer function for high frequency components.

Modelling of the VSC

The series converters basic parts are the gate driver and the power unit. The power circuits for the LV- and HV-DVR are illustrated in Fig. 4.8 page 60 and Fig. 4.9 page 63, respectively.

Power unit For each phase a full bridge converter with four IGBTs and four free-wheeling conducting diodes are used. The IGBTs are modelled as an ideal switch in series with a diode. The switch has a 500 ns turn-on and turn-off time and the diode is modelled with a bias voltage drop (U_{bias}) and a series resistor (R_{on}). The free-wheeling diodes are also modelled with a bias voltage drop and a series resistor, according to:

$$u_{on}(t) = U_{bias} + R_{on} i(t) \tag{6.3}$$

Each switch has in parallel with the switch a 100 pF capacitor and a 100 kΩ resistor to improve the convergence and make the switching transitions more smooth. The used on-state parameters for the IGBTs and diodes are listed in Table 6.1.

Description	Abbreviation	Real value	LV-DVR	HV-DVR
IGBT:	On state resistance	R_{on}	14 mΩ	3.5 mΩ
	Bias voltage	U_{bias}	1.5 V	1.0 V
Diode:	On state resistance	R_{on}	12 mΩ	2.3 mΩ
	Bias voltage	U_{bias}	1.1 V	1.0 V

Table 6.1: LV- and HV-DVR switch parameters.

Gate unit From the micro-controller one signal for each half bridge is the input signals for the gate unit. In the gate unit the turn-off and turn-on signals for each IGBT are generated. Shoot through is avoided with implementation of a dead-time ($t_{dead} = 2.3\ \mu s$), which can be adjusted in the gate unit.

Modelling of the measurement system The measurement system is modelled with infinite bandwidth, but the anti-aliasing have been included and the measured signals are transferred to sampled variables. The A/D-conversion has been modelled with 12-bit quantifications. Anti-aliasing filters are placed at the input and these filters lead to a phase shift and damping of the analog input signals. The parameters for the measurement system are listed in Table 4.6 page 62 and Table 4.9 page 65.

Control system

The control algorithms are modelled exactly as they are executed in the DSP controller. Sampled parameters are used one sample later, because of the structure of

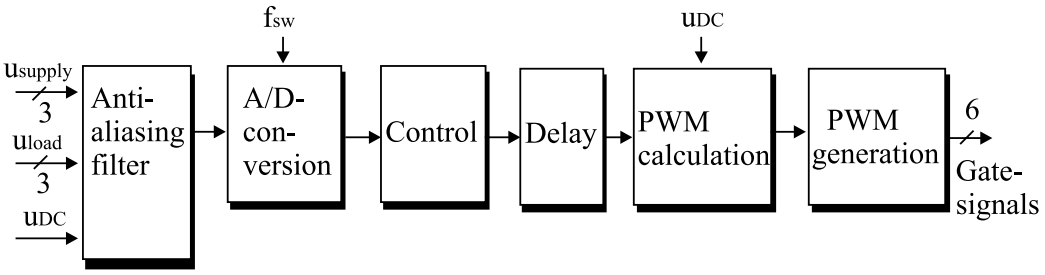


Figure 6.3: *Model of the control system. Seven voltages are after filtering sampled and used for the control. The hardware system has one sample delay and after the calculation and generation of the PWM signals six gate signals are transferred to the gate units.*

the DSP/MC system. In a high tuned dynamic system this can influence the response and the delays are added in the model of the control system. The principles in the control structure is illustrated in Fig. 6.3

Calculations of the duty cycle values are kept in floating point values and transferred to compare units. This is a deviation from the the real system, in which 16 bit integer values a transferred to the MC. The values are compared with an analog triangular carrier signal, which also deviates from the MC′s discrete carrier signal clocked with 2.5 MHz. A more correct model for the MC have been developed, but abandoned because of a large increase in the simulation time.

LV-control Feedforward control is primarily used in the LV-DVR control. The switching and sampling frequency is 5 kHz. The LV-control is further described in Section 7.1 page 119.

HV-control The control is implemented with feedforward and feedback control. The switching and sampling frequency is 3 kHz and the HV-control is described in Section 8.1 page 139.

6.1.3 Modelling of the load

The load is also modelled relatively simple with concentrated parameters.

LV-loads The loads to the LV load are connected in star with the star-point connected to neutral.

HV-loads For the simulation of the HV-DVR all loads are calculated to the 10 kV side. The impedance of the MV cables from the DVR to the 10/0.4 kV transformer and the short circuit impedance of the 10/0.4 kV transformer are modelled as one line impedance ($\underline{Z}_{line}$). Connected LV-loads are calculated to the HV-side

of the distribution transformer and connected in delta to take the Dy transformer connection into account.

Different loads have been tested to identify potential problems with the insertion of a DVR. The loads which have been modelled are linear loads and primarily resistive and inductive loads. Non-linear loads have been modelled with 6 pulse diode rectifier loads with either a large DC-capacitor or a large DC-inductor in the DC-link.

6.2 Simulation and verification of the system models

In this section the implemented system model is verified with measurements to ensure, that the DVR is acceptable modelled and that the model implemented in *Saber*® can be used to an extensive study of the DVR behaviour. First some simulations and measurements are presented for the LV-DVR, and thereafter for the HV-DVR with the main focus is put on the HV-DVR.

6.2.1 Simulation of the LV-DVR

The voltage dips are generated by changing the supply voltages. The DVR is simulated with an infinite energy storage and a 0.7 pu symmetrical voltage dip with a 15° negative phase jump. The DVR is loaded with a 5 kW resistive load and the voltage dip takes place at t = 50 ms and is cleared at t = 150 ms. Fig. 6.4 illustrates the simulated response of the LV-DVR.

Fig. 6.4.f - j show the initial response of the voltage dip with a very ideal step change of the supply voltages. After the dip has been detected by the DVR, it switches from standby operation to active voltage injection and the line-filter oscillations can be seen in Fig. 6.4g. The control is implemented in the dq-rotating reference frame and the phase jump can be seen by the change in the q-component of the supply voltage in Fig. 6.4d and Fig. 6.4i. Both the change in d- and q-component are compensated and the dq-components in the load voltages are restored to $u_{load,d}$ = 325 V and $u_{load,q}$ = 0 V, respectively, which can be seen in Fig. 6.4e, and Fig. 6.4j.

6.2.2 Verification of the LV-DVR model

A verification of the model is limited to certain operating points within normal operating conditions.

Comparison of the simulated and measured response

To ensure that the model is valid, simulations and measurements have been compared for certain operating conditions. Fig. 6.5a - f illustrates the measurement of a 0.70 pu voltage dip with the test conditions given in Table 6.2.

Parameter	Description	Abbreviation	Real value	pu value
Supply:	Voltage	U_{supply}	400 V	1 pu
	Impedance	$\underline{Z}_{supply}$	j0.04 Ω	
Voltage dip:	Depth	$\lvert\underline{U}_{dip}\rvert$	160 V	0.7 pu
	Duration	t_{dip}	100 ms	5 pu
	Phase jump	ϕ_{dip}	0 °	
DVR:	DC-link voltage	U_{DC}	500 V	
	Switching frequency	f_{sw}	5 kHz	100 pu
Load:	Apparent power	$\underline{S}_{load}$	2 kW	0.1 pu
	Impedance	$\underline{Z}_{load}$	(80 + j0) Ω	0.1 pu

Table 6.2: Test conditions for the verification of the LV-DVR model.

The DVR has been simulated under the same conditions, and the two cases have been compared. A zoomed view of the measured response is illustrated in Fig. 6.5c - e, and the simulated response in Fig. 6.5f - h. Both reveal a low-damped oscillation from measurement of the approximate period of the oscillation, and the frequency can be calculated to 1250 Hz. The resonance frequency from the leakage inductance of the transformer and the capacitor in the line-filter can be calculated to 1290 Hz, which explains the origin of the oscillation. The oscillations are weakly damped, because the load is a light resistive load, with a larger load the damping is improved. The oscillations depend also on the phase of the voltage.

A new voltage dip have been applied at a different angle of the supply and the DVR voltage have only small oscillations. Fig. 6.6a illustrates the measured DVR voltage from t = 0 - 200 ms and a zoomed view from t = 50 - 80 ms of measured the DVR voltage, the measured load current and the measured converter current are illustrated in Fig. 6.6b, Fig. 6.6f and Fig 6.6g.

In Fig. 6.6c-e the measurements are illustrated from 56 - 61 ms and the simulation results in Fig. 6.6h - j. A difference between the simulations and measurements can be seen in the ripple current of the converter, which indicates some deviations in the transformers leakage flux or DC-link voltage between the actual and simulated system. The simulations and measurements are considered to show generally good agreement.

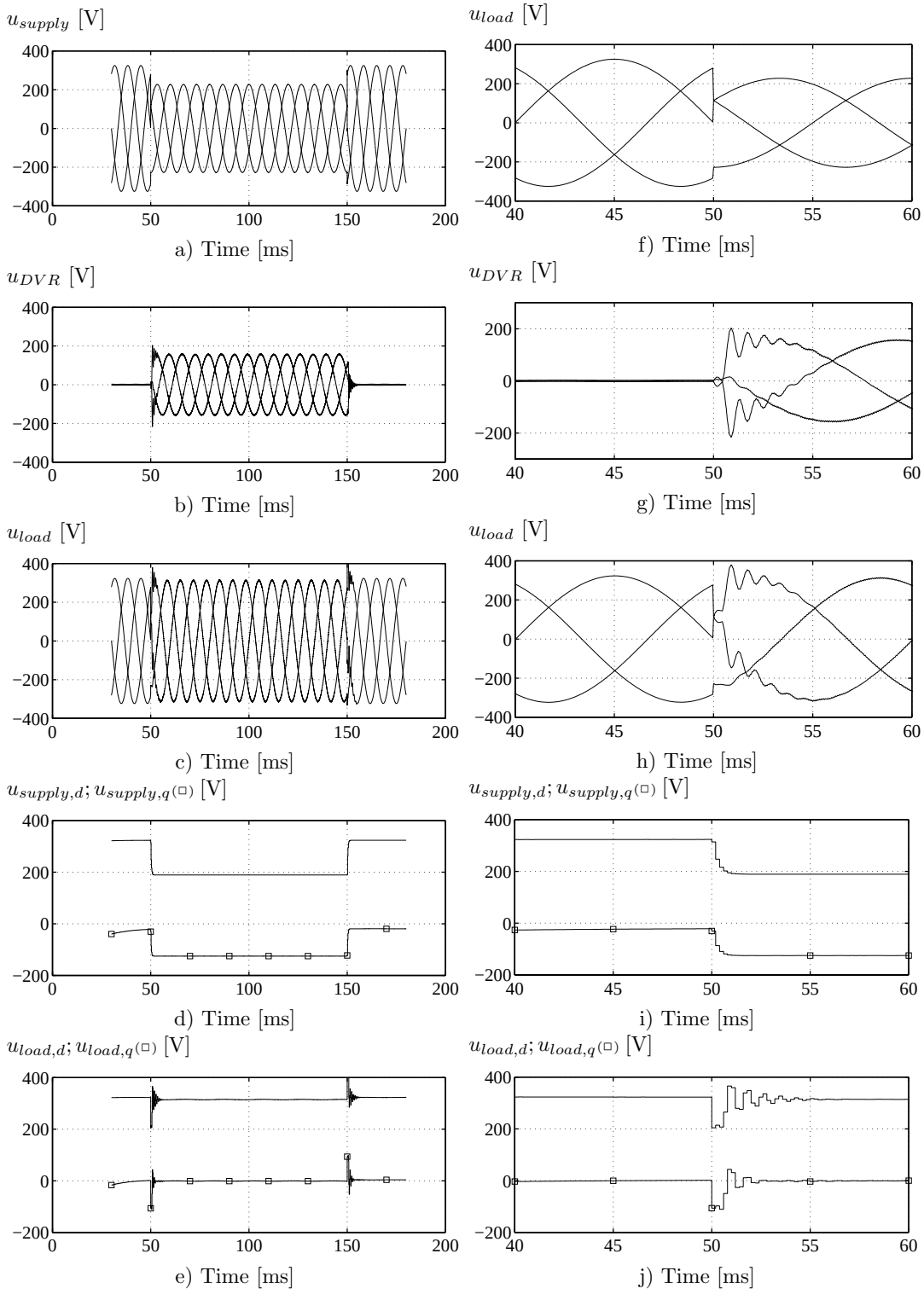


Figure 6.4: *Simulated LV-DVR response during a 0.70 pu symmetrical voltage dip. a) - e) has the time range 0 - 200 ms and f) - j) the time range 40 - 60 ms. a) supply voltages, b) DVR voltages, c) load voltages, d) dq-components of the supply voltages, e) dq-components of the load voltages, f) supply voltages, g) DVR voltages, h) load voltages, i) dq-components of the supply voltages and j) dq-components of the load voltages.*

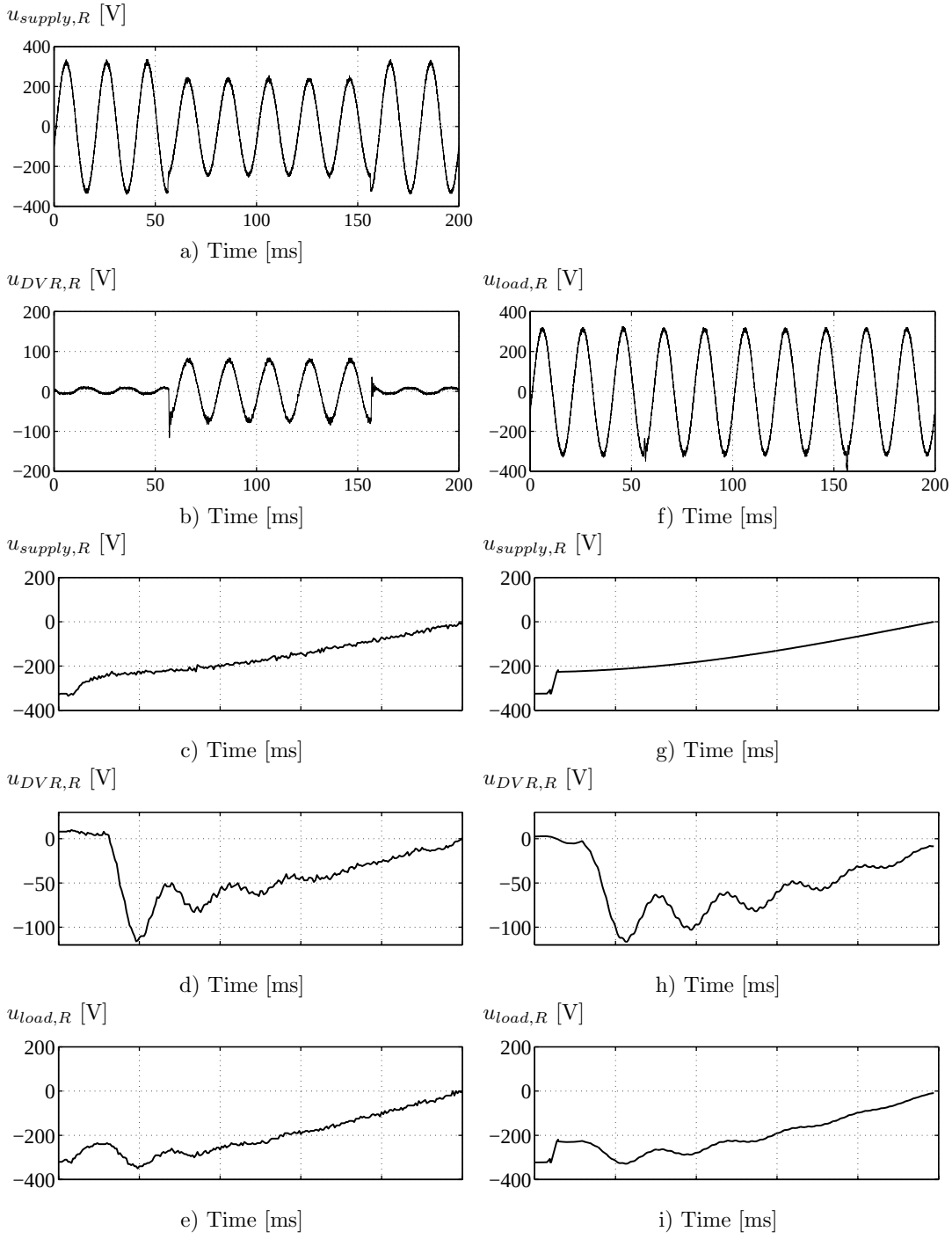


Figure 6.5: *Measured and simulated response during a 0.7 pu voltage dip. a) measured supply voltage 0 - 200 ms, b) measured DVR voltage 0 - 200 ms, c) measured load voltage, d) measured supply voltage, e) measured DVR voltage, f) measured load voltage 0 - 200 ms, g) simulated supply voltage, h) simulated DVR voltage and i) simulated load voltage.*

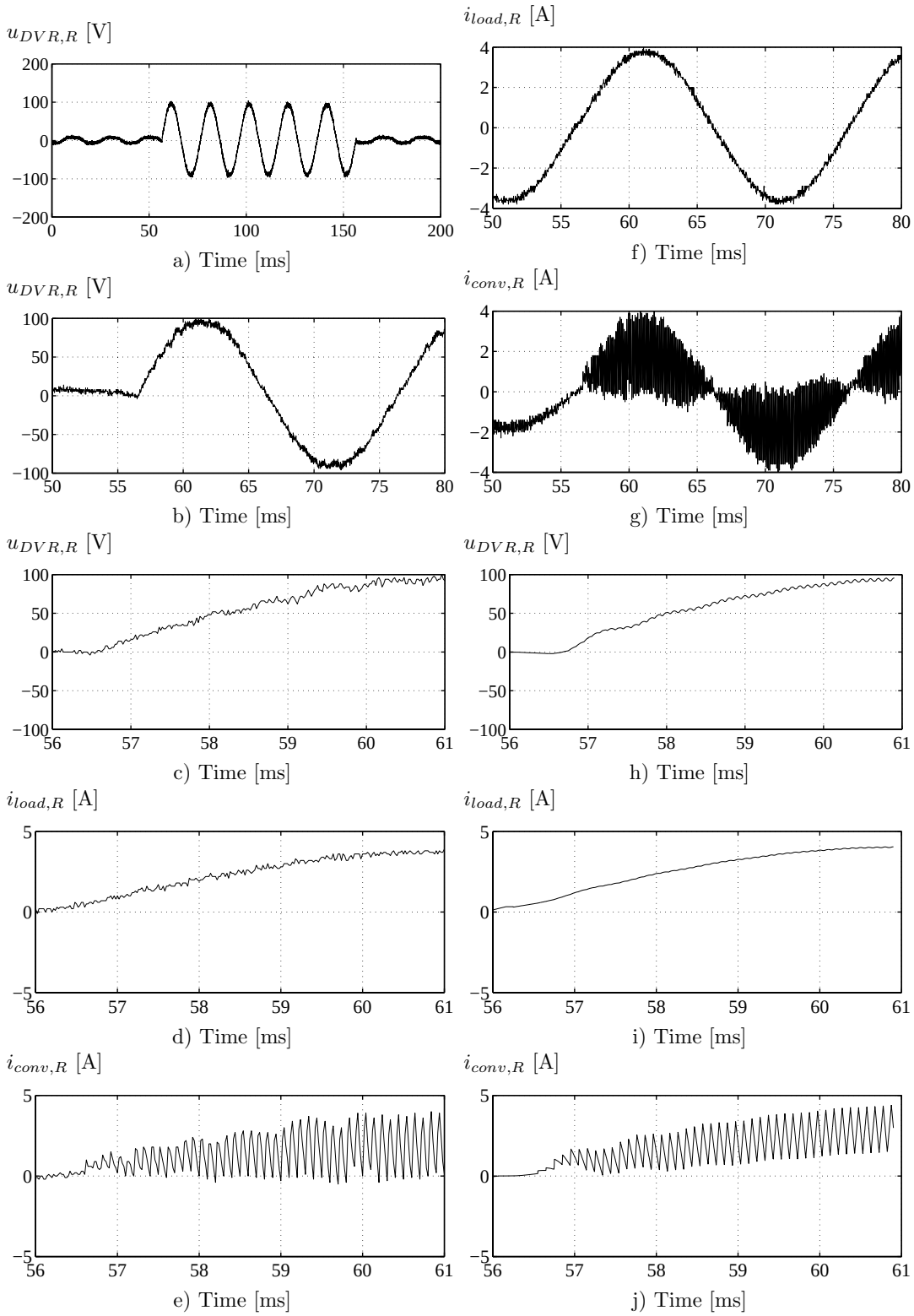


Figure 6.6: *Measured and simulated response during a 0.7 pu voltage dip. a) measured DVR voltage 0 - 200 ms, b) measured DVR voltage 50 - 80 ms, c) measured DVR voltage 56 - 61 ms, d) measured load current 56 - 61 ms, e) measured converter current 56 - 61 ms, f) measured load current 50 - 80 ms, g) measured converter current 50 - 80 ms, h) simulated DVR voltage 56 - 61 ms, i) simulated load current 56 - 61 ms and j) simulated converter current 56 - 61 ms.*

6.2.3 Simulation of the HV-DVR

Several simulations have been performed of the HV-DVR, here it is chosen to include simulations of a rated voltage dip. First letting the DVR protect a rated resistive load and then with a light resistive load. In the verification of the models of the HV-DVR simulations of a symmetrical and a non-symmetrical voltage dips are included, which both are comparable with measurements later performed. The power circuit for the HV DVR can be seen in Fig. 4.9 page 63 and the control setup is illustrated in Fig. 8.1 page 140.

Simulation of a rated voltage dip at rated load

The voltage dip is generated by reducing the voltages of the supply to 0.5 pu for 100 ms, thereby the voltage dip is 0.5 pu without any phase jump. The DVR response can be seen in Fig. 6.7 from 0 - 200 ms in Fig. 6.7a - e. A zoomed view of the response from 40 - 60 ms is illustrated in 6.7f - j. The load is 1 pu (400 kW) equal to three 750 Ω resistors connected in delta.

A small dip can be seen at the load side of the DVR in the beginning of the voltage dip and a small over-voltage at the end of the voltage dip. During standby operation approximately 360 V RMS voltage drop can be calculated across the DVR, which is equivalent to 6.2 % of the rated voltage. The converter currents are illustrated in Fig. 6.7d with the ripple content and the current oscillation between the filter capacitor and the converter, which generate the oscillations at the load voltages.

The dq-values are illustrated in Fig. 6.7e and the positive sequence components appear as DC-values. The line-filter oscillations can easily be seen in Fig. 6.7g at the injected DVR voltages, but they are relative highly damped, because of the high resistive load.

Simulation of a rated voltage dip at light load

The load is now set to 1/100 of the rated load with all other parameters equal to the previous simulation example and the DVR response is illustrated in Fig. 6.8. The light load gives a poor damping of the line-filter oscillations in the transition phases, which for instance can be seen at the injected DVR voltages in Fig. 6.8b and Fig. 6.8g. The voltage drop across the DVR is close to zero, because of the low load currents.

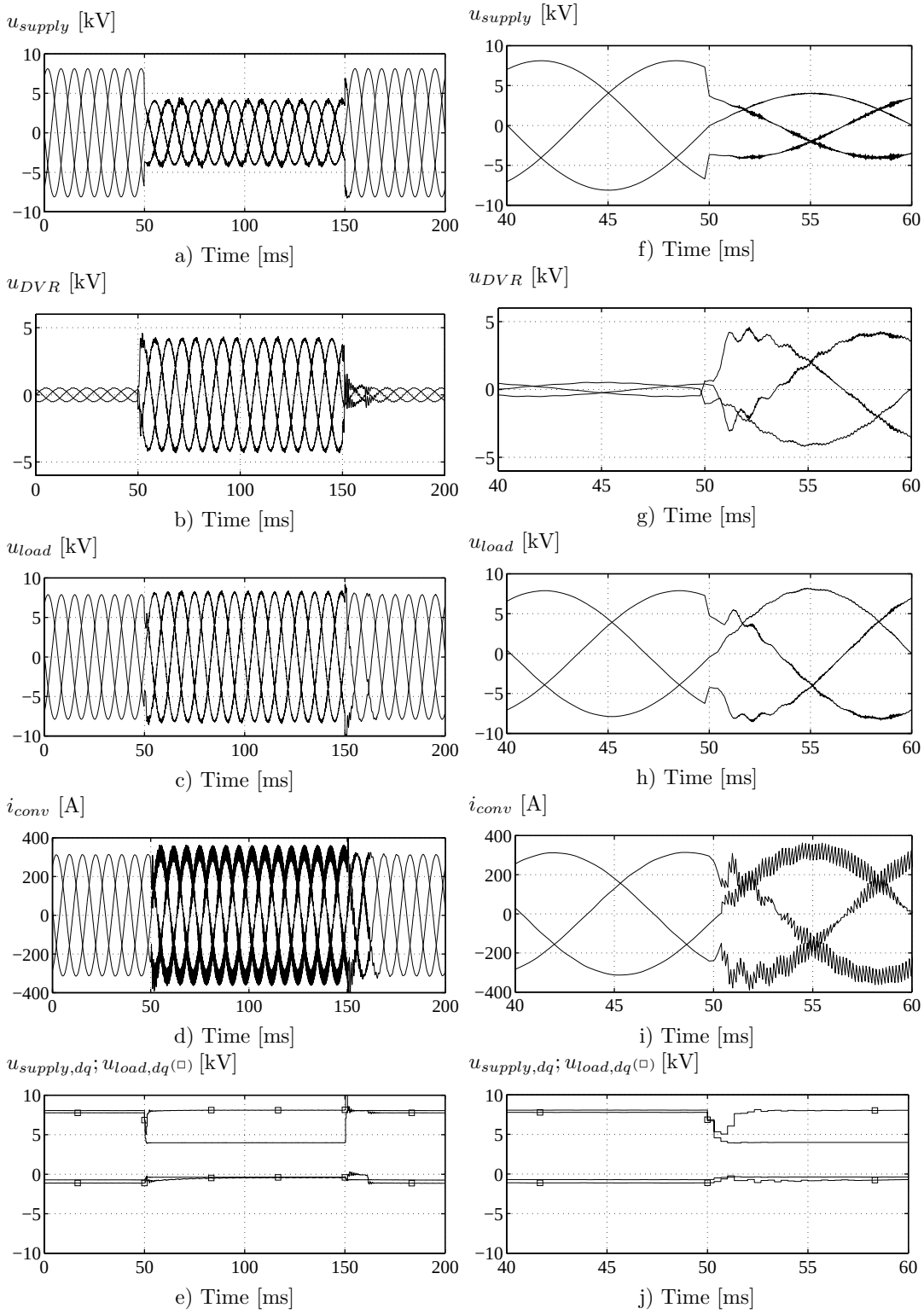


Figure 6.7: *Simulated 0.50 pu symmetrical voltage dip with 1 pu load. a) - e) 0 - 200 ms and f) - j) 40 - 60 ms. a) Supply voltages, b) DVR voltages, c) load voltages, d) converter currents, e) dq-supply and dq-load voltages, f) supply voltages, g) DVR voltages, h) load voltages, i) converter currents and j) dq-supply and dq-load voltages.*

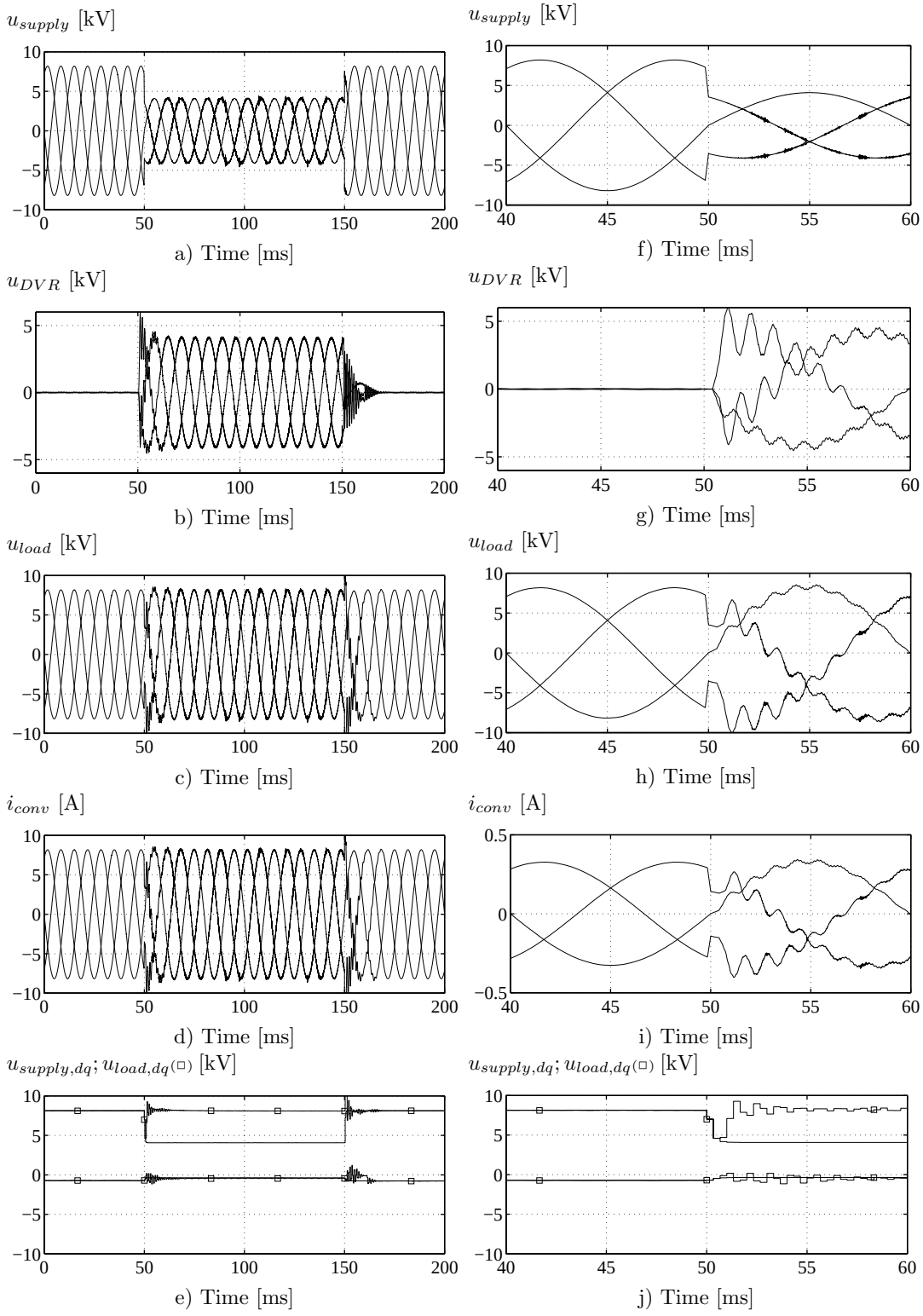


Figure 6.8: *Simulated 0.5 pu symmetrical voltage dip with 0.01 pu load. a) - e) 0 - 200 ms and f) - j) 40 - 60 ms. a) Supply voltages, b) DVR voltages, c) load voltages, d) converter currents, e) dq-supply and dq-load voltages, f) Supply voltages, g) DVR voltages, h) load voltages, i) converter currents and j) dq-supply and dq-load voltages.*

6.2.4 Verification of the HV-DVR model

Two conditions are simulated with all the parameters very close to the actual test conditions later performed with the HV-DVR. A fault have been generated at the low voltage side of the transformer (T_{sc}) with breaker (B_2) in Fig. 6.2 page 101. Some of the main test conditions are stated in Table 6.3.

Component	Description	Abbreviation	Real value	pu value
Supply:	Voltage	U_{supply}	10 kV	1 pu
	Impedance	$\underline{Z}_{supply}$	(2.6 + j 1.9) Ω	
Fault:	Impedance	$\underline{Z}_{fault}$	7.5 Ω	
Voltage dip:	Depth	U_{dip}	7.4 kV	0.74 pu
	Duration	t_{dip}	100 ms	5 pu
	Phase jump	ϕ_{jump}	-12 °	
DVR:	DC-link voltage	U_{DC}	600 V	
	switch frequency	f_{sw}	3.0 kHz	60 pu
Load:	Apparent Power	$\underline{S}_{load}$	45 kW	0.11 pu
	Impedance	$\underline{Z}_{load}$	6670 Ω	

Table 6.3: Test conditions for the verification of the HV-models.

Comparison of a simulated and measured symmetrical voltage dip

The supply voltages in front of the DVR and the dip can be measured to 0.74 pu. The simulated response can be seen in Fig. 6.9 and can be compared with the measured response in Fig. 8.14 page 155.

The symmetrical fault is generated at t = 50 ms, and at t = 150 ms a command to clear the fault is given, when each phase reaches a zero crossing the switch in the actual phase is cleared. Fig. 6.9a illustrates the short circuit currents, Fig. 6.9b the supply voltages in-front of the DVR, Fig. 6.9c the injected DVR voltages, Fig. 6.9d the resulting load voltages and Fig. 6.9e the load currents.

In the initial phase of the voltage dip, the simulated response is very close to the actual measured response. The clearing of the fault current generates a voltage spike at the simulated supply voltages, which cannot be found on the measurements. In the measurements the return of the supply voltages takes place more smoothly and thereby it is easier for the DVR to control the load voltage. Oscillations at the supply voltages cannot be found on the simulations, which is because of the simple model of the supply and the short circuit path. The simulated line-filter oscillations on the DVR voltages and load voltages are very close to the actual measured oscillations.

Fig. 6.9f illustrates a zoomed view of the transition phase from standby mode to active mode for one phase voltage and Fig. 6.9g is a further zoom of transition. Fig. 6.9h shows the return of the supply voltage and Fig. 6.9i a further zoom. Fig. 6.9i shows the transition from active mode to standby mode.

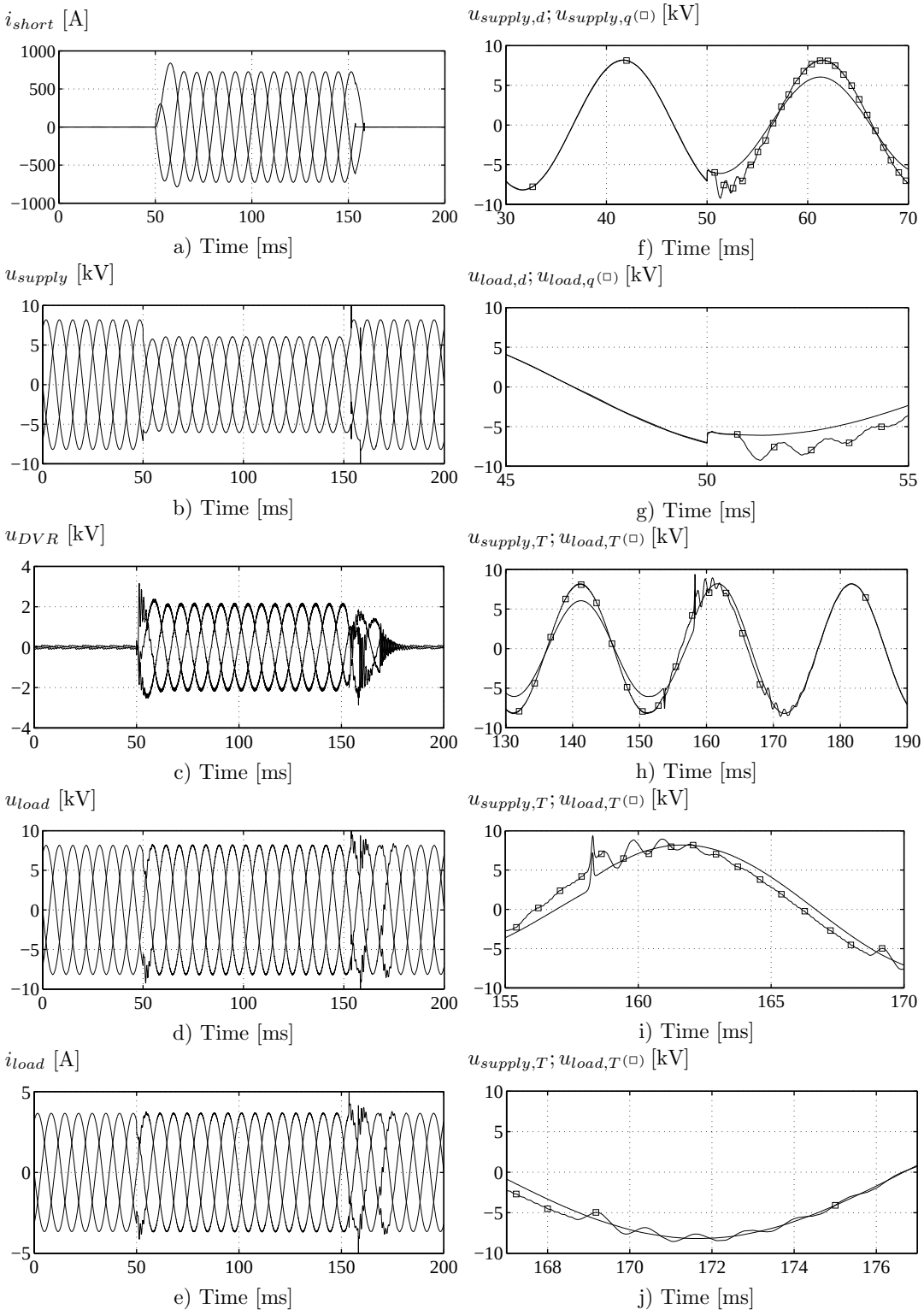


Figure 6.9: *Simulated 0.74 symmetrical voltage dip protecting a 45 kW load. a) Short circuit currents, b) supply voltages, c) DVR voltages, d) load voltages, e) load currents, f) transition from standby to active mode, g) zoomed view of the start transition, h) transition from active mode to standby mode, i) zoomed view of the return of the supply voltage and j) transition from active to standby mode.*

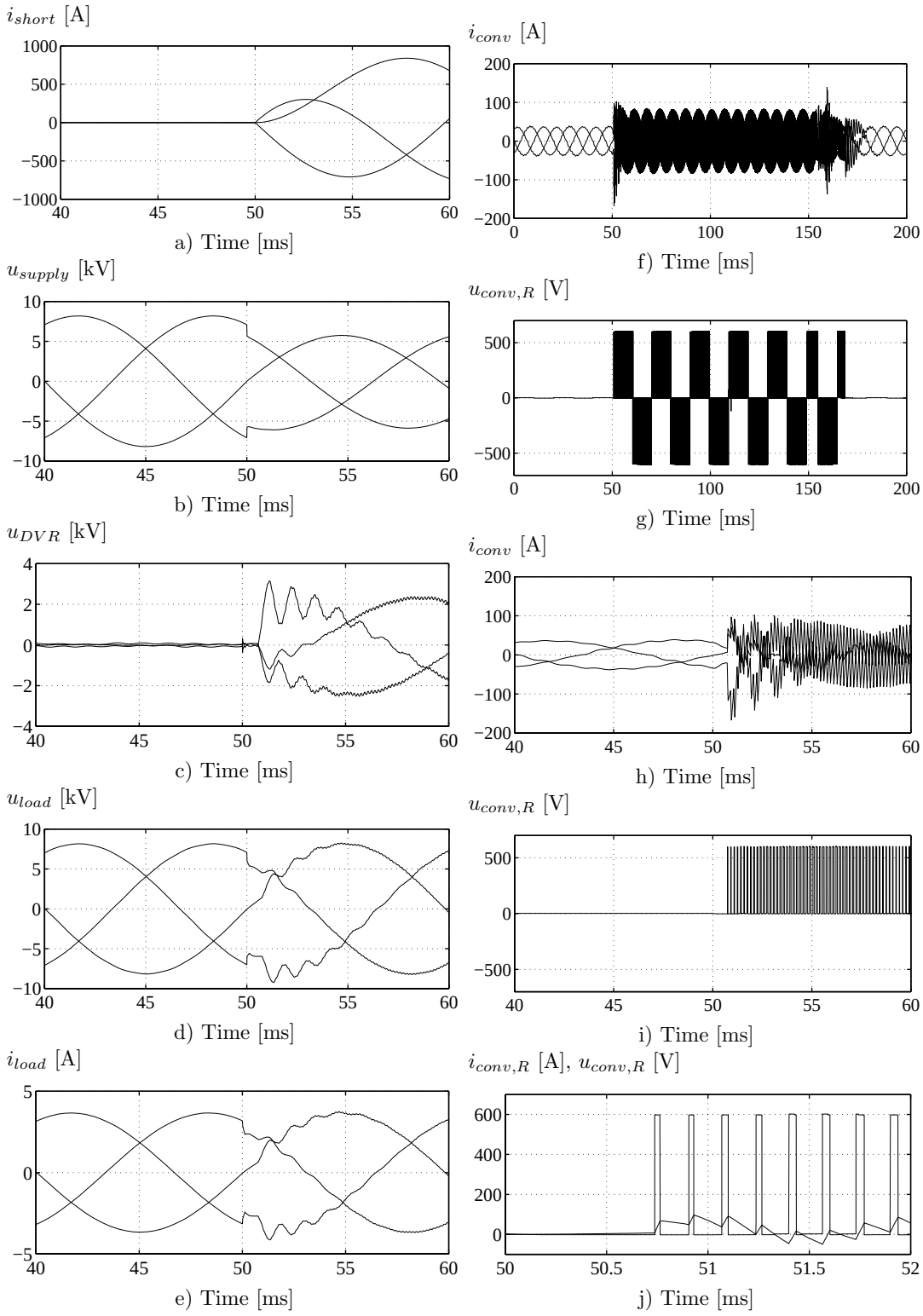


Figure 6.10: *Simulated 0.74 pu voltage dip protecting a 45 kW load. a) short circuit currents, b) supply voltages, c) DVR voltages, d) load voltages, e) load currents, f) converter currents, g) converter R voltage, h) zoomed converter currents, i) zoomed converter R voltage and j) converter R current and converter R voltage*

Fig. 6.10a - e illustrate a zoomed view of the initial phase of the voltages dip from 40 - 60 ms. Fig. 6.10e illustrates the converter currents with a very high ripple content, because of the relatively light load.

In Fig. 6.10f the uni-polar pulse width modulated converter voltage can be seen, and the three voltage levels possible to generate. The DVR performs no switchings in standby mode to minimize losses. In Fig. 6.10j the converter voltage and current for phase R is further zoomed, and the ripple content in the current can be seen.

Comparison of a simulated and measured non-symmetrical voltage dip

The fault is generated by connecting one phase to neutral at the low voltage side of the transformer (T_{sc}) in Fig. 6.2 page 101. The simulated DVR response is illustrated in Fig. 6.11 and the load is 0.19 pu (75 kW). The associated measured response can be seen in Fig. 8.16 page 158 and Fig. 8.20 page 164.

The short circuit current in Fig. 8.20a flows only in two phases and the supply voltages in Fig. 8.20b are reduced in two phases, and because of the phase jump the two affected voltages are not equally reduced. The DVR compensates the voltage dip by voltage injections in Fig. 8.20c, and the load voltages in Fig. 8.20d are partly compensated. A non-symmetrical component in the load voltages in Fig. 8.20d and in the load currents in Fig. 8.20e can still be identified.

The simulated dq-values of the supply voltages are shown in Fig. 8.20f in which the 100 Hz component from the negative sequence component can be seen. The injected dq-DVR voltage and the associated load voltages are illustrated in Fig. 8.20g - h and the dq-DVR reference voltage in Fig. 8.20i. In Fig. 8.20j the actual converter currents are illustrated.

The simulated response is very close to the measured response in Fig. 8.16 page 158 and Fig. 8.20 page 164. In the measured case the supply voltages have a noticeable content of 5. and 7. harmonic content. It can be difficult to compare the injected DVR voltages, because the measured voltages have a large quantification noise. Generally a good agreement can be found between simulations and measurements.

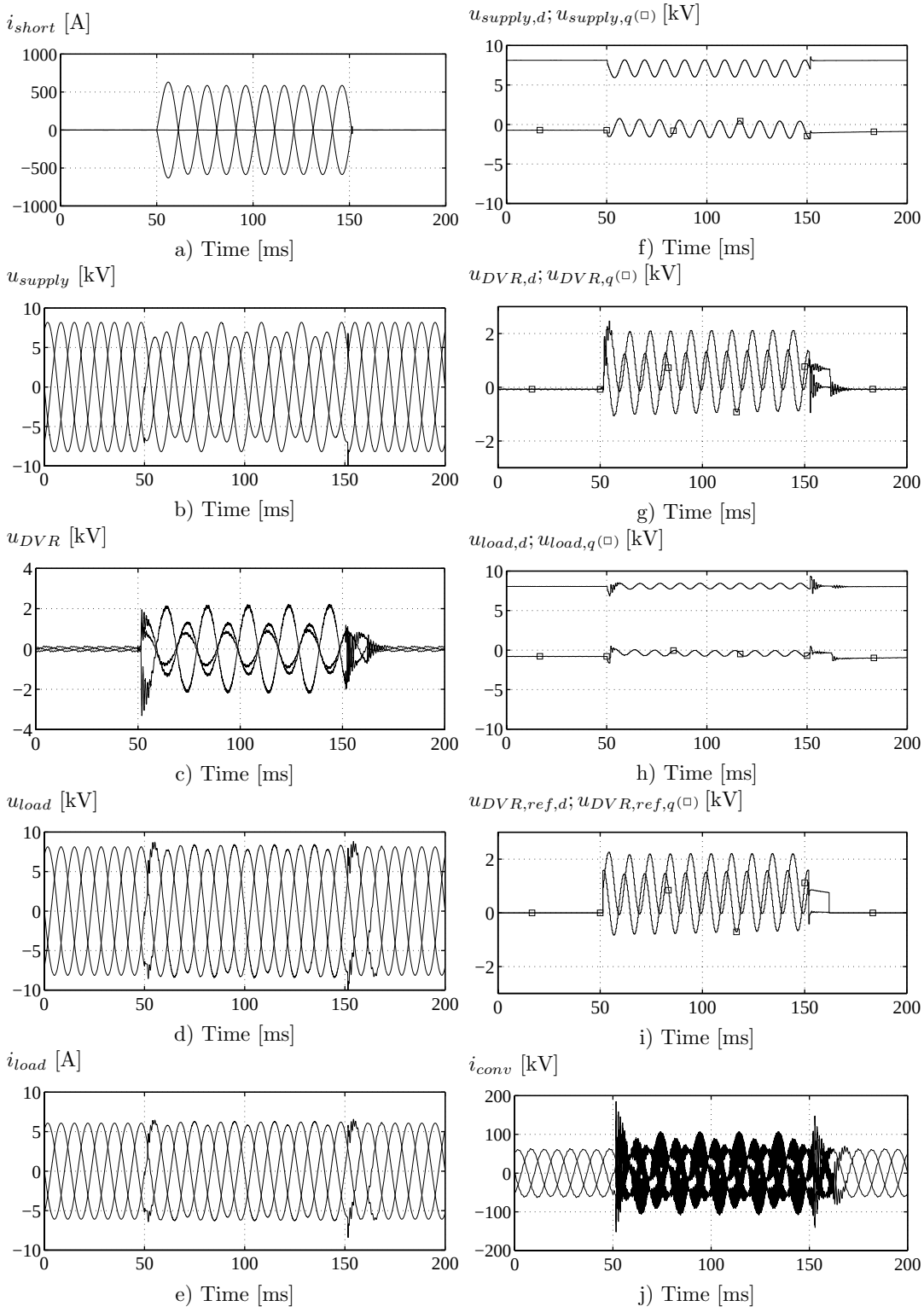


Figure 6.11: *Simulated 0.75 pu non-symmetrical voltage dip with a 75 kW load. a) Short circuit currents, b) supply voltages, c) DVR voltages, d) load voltages, e) load currents, f) dq-supply voltages, g) dq-DVR voltages, h) dq-load voltages, i) dq-DVR reference voltages and j) converter currents*

6.3 Summary and conclusion

The chapter explains how the supply, DVR and load have been modelled for simulation. Included in the chapter is simulations from the LV-DVR and a comparison between measurements and simulations. Finally, simulations of the HV-DVR are presented, which include simulations of different load conditions, and in the comparison between measurements symmetrical and non-symmetrical voltage dips are simulated.

- The model of the supply and the generation of voltage dips is explained, which gives simplified and ideal voltage dips. For the HV-DVR a pure change in amplitude is not sufficient, because the fault generated at the test site also include a phase jump.
- The DVRs are implemented with ideal injection transformers without saturation and shunt impedances. The main filter components have been included, and the VSC is pulse width modulated and the control is implemented in discrete time domain very close to the actual control of the two DVRs.
- The load is implemented very simple with expected cable impedances to the load, an ideal distribution transformer and linear and non-linear loads.
- For small voltage dips the measurements are close to the simulated response, but for more severe dips, in-rush and saturation effects in the injection transformers will lead to large deviations between simulations and measurements.

Chapter 7

Control and testing of the LV-DVR

In this chapter the control strategy and performance for the LV-DVR is verified with measurements on the LV-DVR. The LV-DVR is mainly used to get experience with the DVR hardware and control.

7.1 Control of the LV-DVR

Different control methods have been implemented in the LV-DVR. The main control method is the feedforward/open loop control as illustrated in Fig. 7.1. The DVR operates normally in standby mode, and when a voltage dip is detected it changes to active mode. The DC-link is fed from a three-phase auxiliary supply with a six pulse passive diode rectifier. The hardware parameters are listed in Section 4.3.2 page 60, and the power circuit is illustrated in Fig. 4.8 page 60.

The DVR measures the three supply voltages and transform the voltages to the $\alpha\beta$-system. The PLL uses the $\alpha\beta$-supply voltages and generates the filtered PLL angle. The angle of the PLL (θ_{PLL}) is used in the transformation to the rotating dq-system. The DVR controls the load voltages to be in-phase with the supply voltages by setting the d-reference voltage to 325 V and the q-reference voltage to zero. The error between the actual supply voltages and the wanted load voltages is calculated and is feedforward to the DVR and the PWM signals to the three full bridges is generated. During normal supply voltages the DVR is in standby mode, and the DVR-reference voltages are set to zero.

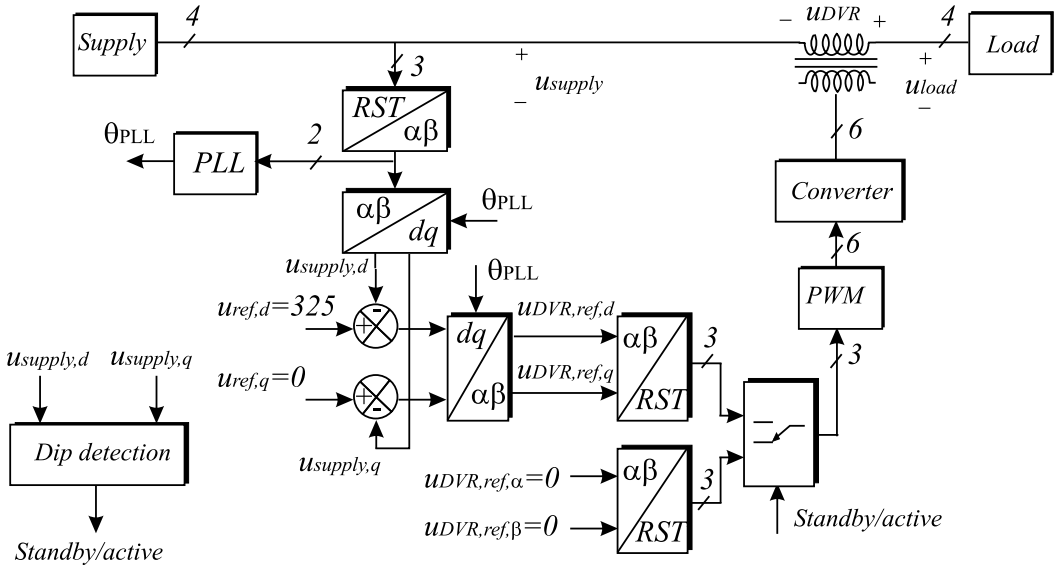


Figure 7.1: feedforward/Open loop control of the LV-DVR.

7.2 Testing of the LV-DVR

The tests presented can be grouped into the following categories:

- Stationary conditions under different load conditions; The primary test results are from the protection of non-linear loads.
- Symmetrical voltage dips; Response analysis and control considerations are presented.
- Symmetrical voltage dips with phase jump; Two control methods are presented and tested with simulations and measurements.
- Non-symmetrical voltage dips; Characteristics of non-symmetrical voltage dips are tested with voltage dips containing both positive and negative sequence systems.
- Different system topologies for active power access during voltage dips; Four topologies have been analyzed in Section 3.3.3 and the test results are presented on the LV-DVR.

The supply in all the tests have been a three-phase programmable 3 X 10 kVA power supply, and the test setup for testing symmetrical voltage dip is illustrated in Fig. 7.2. Pictures from the hardware are shown in Fig. 7.3

The LV-DVR is protected with mechanical bypass breakers and the transformer is a 115/230 V transformer. At a short circuit at the down-stream side of the DVR, the converter is turned off due to over-current, and the full supply voltage

will be across the DVR. The RMS value of the voltage at the secondary side can be 460 V, and the DC-link will be charged to approximately 650 V, which is well below the 1200 V breakdown voltage of the IGBTs and below the 760 V maximum capacitor voltage. The converter can withstand this potential condition, but the series transformer will be put into deep saturation, and both the line-filter and the transformer will be overloaded and overheated if the bypass switches are not activated.

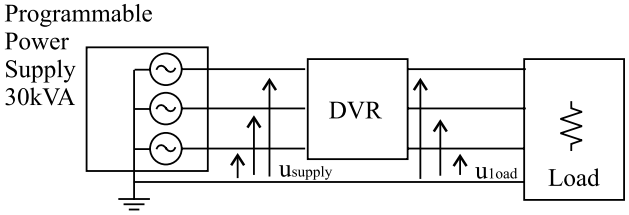


Figure 7.2: Test setup for DVR-operation at a symmetrical voltage dip.

a) b)

Figure 7.3: *The LV-DVR hardware. a) The test setup with the power supply at the left, the converters in the upper right corner and the injection transformer and line-filter in the lower right corner. b) A zoomed view of one single-phase 3.3 kVA injection transformer.*

7.2.1 Testing stationary conditions

The DVR has been tested under different load conditions in order to investigate the performance and potential problems concerning the DVR.

Linear load

Different types of linear loads have been applied without noticing any problems during stationary conditions. Only the voltage drop across the DVR varies with the load current. The loads which have been tested are inductive/resistive loads, capacitive/resistive loads and non-symmetrical linear loads.

Non-linear load

Inserting a DVR increases the supply impedance seen by the load, and a non-linear load will lead to a more distorted load voltage. To verify the performance at a non-linear load a test has been performed, both with passive diode bridges, in the two following configurations.

1. Voltage Source Converter (VSC); Six pulse diode bride with $U_{DC} \simeq constant$ and a capacitor in the DC-link. Illustrated in Fig. 7.4a.

2. Current Source Converter (CSC): Six pulse diode bridge with an inductor and a resistor in the DC-link. $I_{DC} \simeq constant$. Illustrated in Fig. 7.4b.

They are very different in behaviour regarding power as a function of voltage and current waveform.

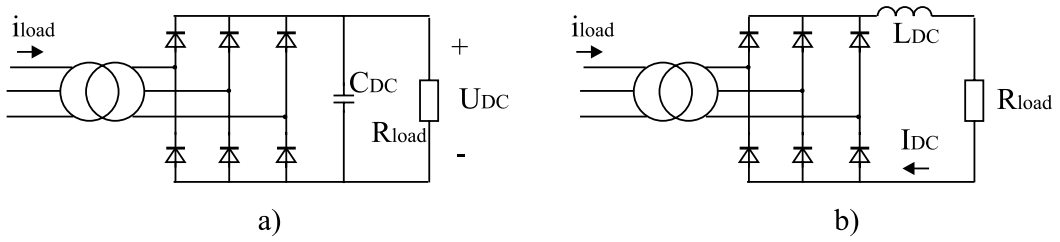


Figure 7.4: Non-linear loads a) VSC load and b) CSC load.

Voltage source converter load This converter type is very load voltage dependent and behaves like a VSC converter. In this test the DC-link absorbs approximately 5 kW. A delta/star transformer is put in-front of the diode bridge to bring the current distortion down to more realistic values. The load current includes the inductive current from the magnetization of the load transformer.

Fig. 7.5a illustrates the measured supply voltage, in Fig. 7.5b the measured DVR voltage and in Fig. 7.5c the resulting load voltage. In Fig. 7.5d - e the converter current and the load current are shown, respectively. Applying a very non-linear load initiates a resonance between the filter capacitor and the leakage inductance of the injection transformer. A step-change in the load current initiates an oscillation in the converter with a low damping as it can be seen in Fig. 7.5d.

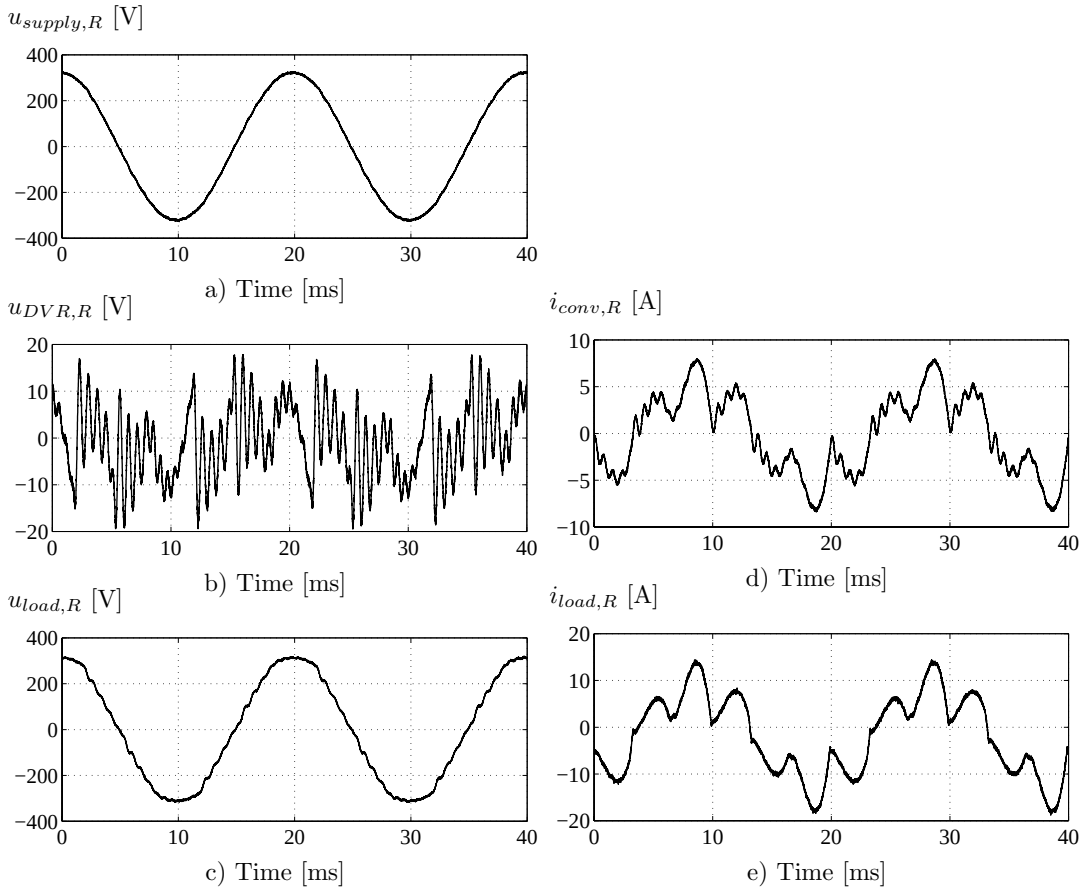


Figure 7.5: *Testing stationary conditions sourcing a passive VSC load. a) Supply voltage, b) DVR voltage, c) load voltage, d) DVR current and e) load current.*

If the load is not purely non-linear, but also has a resistive part, the damping in the system can be improved significantly. Fig. 7.6 illustrates the case with 5 kW non-linear load and 5 kW linear resistive load. Thereby, the resonance in the line-filter is significantly damped, which is most visible in the converter current shown in Fig. 7.6d.

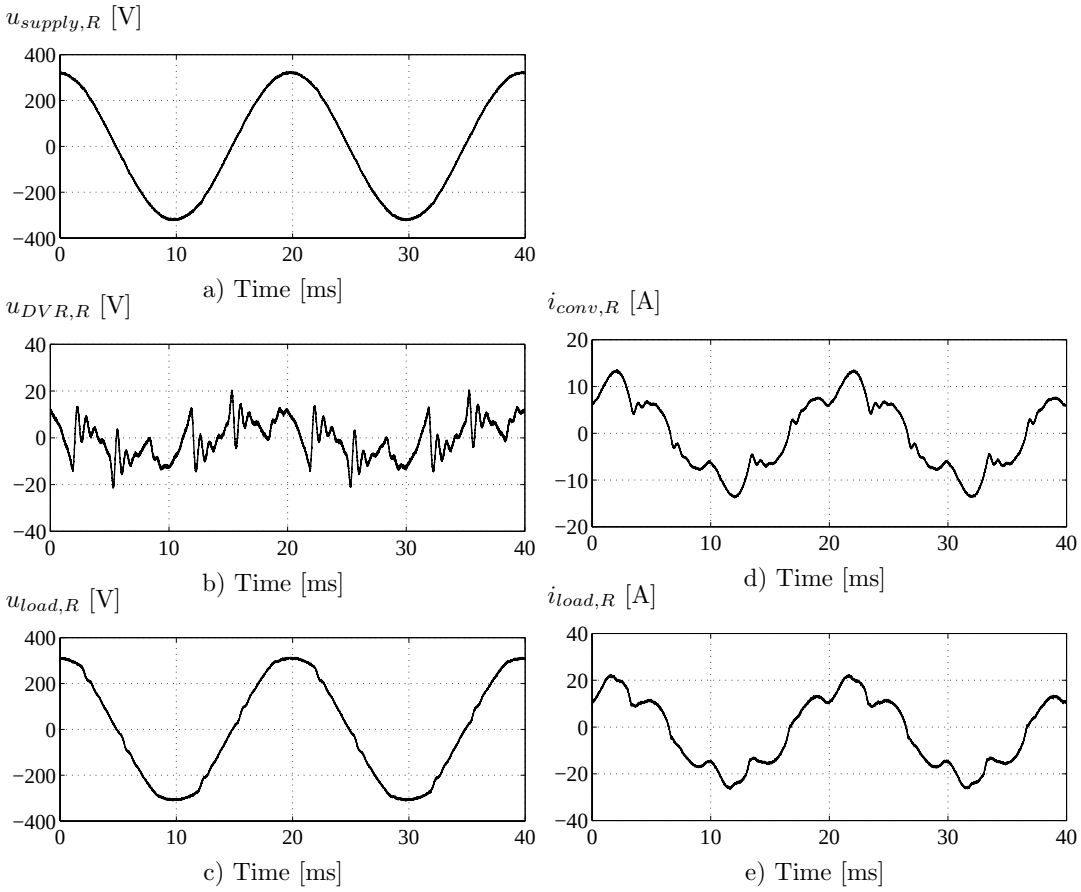


Figure 7.6: *Testing stationary conditions sourcing a passive VSC and resistive load. a) Supply voltage, b) DVR voltage, c) load voltage, d) DVR current and e) load current.*

Current source converter load The problems with non-linear load are even more clear using a current source converter load. The supply voltage, DVR voltage, load voltage, DVR current and load current are illustrated in 7.7. The step changes in the load currents are more clear (see Fig. 7.7e) and the damping can easily be seen.

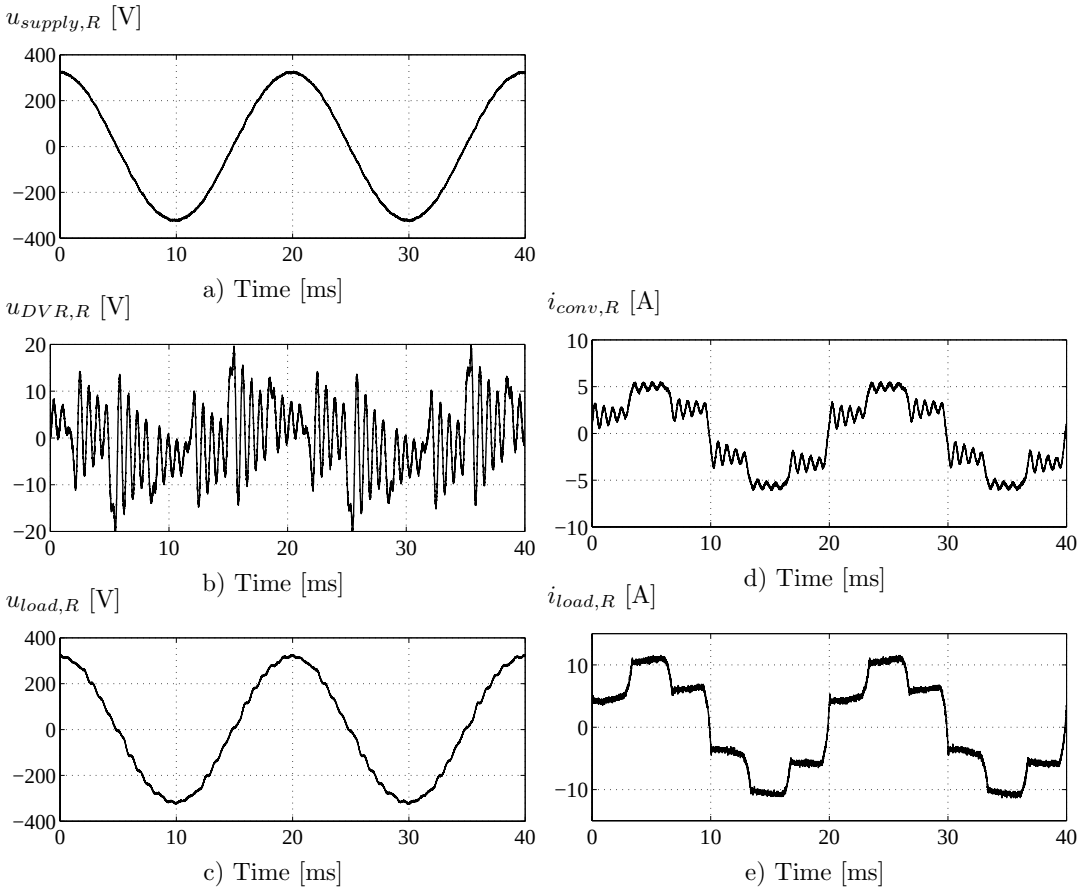


Figure 7.7: *Testing stationary conditions sourcing a passive CSI load. a) Supply voltage, b) DVR voltage, c) load voltage, d) DVR current and e) load current.*

It is relatively difficult to damp these oscillations with the used control strategy, because the oscillations can not be seen without using the load voltages in the control. Methods to reduce the oscillations are:

- Increasing the damping by adding more resistance in the oscillation circuit, which has the disadvantage of increasing the losses in the system.
- Putting restrictions on the load composition and THD_I.
- Closed loop control with an active damping of oscillations.

7.2.2 Testing dynamic conditions

The dynamic conditions include the testing of symmetrical voltage dips with and without phase jump and non-symmetrical voltage dips.

Testing symmetrical voltage dips

Compensating a symmetrical voltage dip with no phase jump is from a control point of view the easiest voltage dip to compensate. A symmetrical dip is easy to detect in the dq-reference system by detecting a reduction in the d-component.

A symmetrical voltage dip has been initiated and the supply voltage, DVR voltage, load voltage and converter currents can be seen in Fig. 7.8.

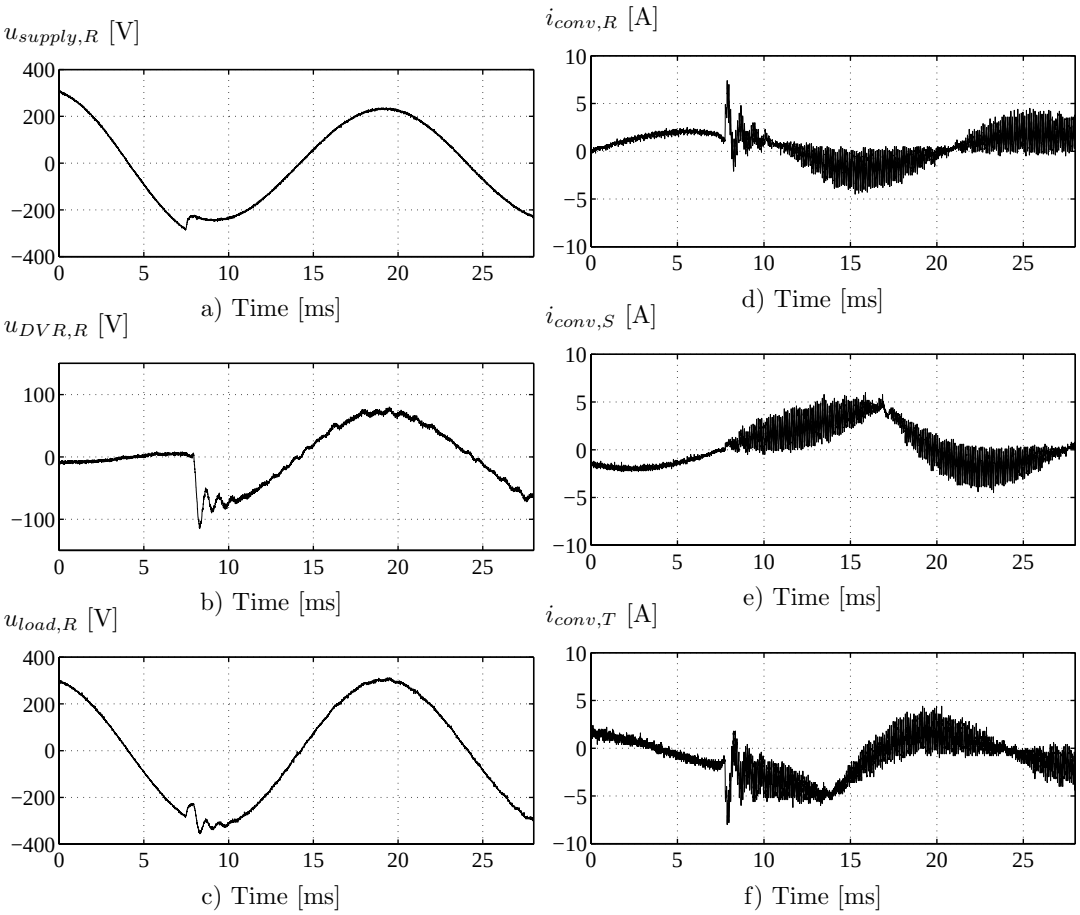


Figure 7.8: *Testing the LV-DVR response during a symmetrical voltage. a) Supply voltage, b) DVR voltage, c) load voltage, d) converter R current, e) converter S current and f) converter T current.*

To be able to estimate the performance and response-time the supply and load voltages are plotted in Fig. 7.9a. In the zoomed view in Fig. 7.9b it can be seen, that at t = 7.5 ms the supply voltage starts to decrease, 0.5 ms later a response from

the DVR can be seen, and another 0.2 s before the pre-dip supply voltage level has been reached. The load voltage contains some low-damped oscillations, especially in the first phase after the voltage dip.

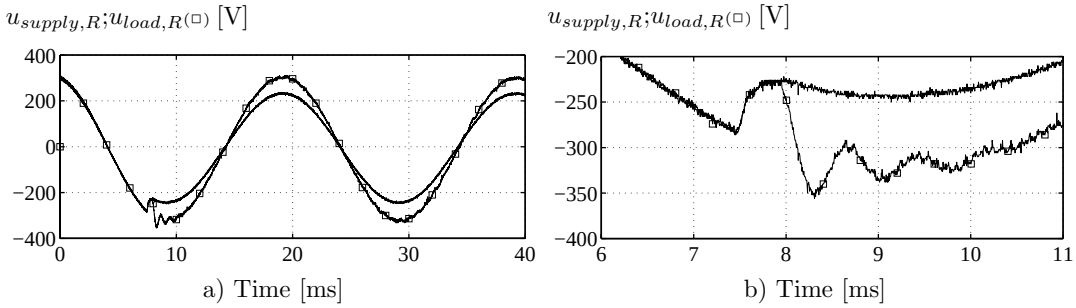


Figure 7.9: *Testing a symmetrical voltage dip illustrated with phase R supply voltage and phase R load voltage. a) 0 - 40 ms and b) zoomed view 6 - 11 ms.*

If the load currents are symmetrical and only slowly time varying the compensation of the voltage drop across the DVR can be compensated with feedforward control. [58]

A performance criteria for the DVR is the bandwidth/reponse time of the system, and in the open loop approach the response-time can be seen from the above measurement and be approximately calculated from known system parameters. The response-time of the open loop scheme depends on hardware and software components. For the hardware several issues are of relevance eg. the cross over frequency of the anti-aliasing filter (f_{af}), the switching frequency (f_{sw}) and the sampling frequency ($f_{sampling}$), delay in the control($t_{d,cont}$), the filter resonance frequency (f_{res}) and the impedance of the load ($\underline{Z}_{load}$).

A high injection value increases the risk of saturation of the DVR transformer and the in-rush current, which is handled by the DVR converter can be high. If the load currents are well below the rated current, the transformer can be brought into a deeper saturation and thereby increase the injected voltage on the cost of higher losses and magnetization current. Above a certain voltage dip depth the voltage rating of the DVR is not sufficient and the DVR can inject maximum voltage. The maximum voltage values are set individually for the d- and q-component. If the voltage dip is followed by a large phase jump the voltage dip is primarily detected from the q-component of the voltage. All other dips are mainly detected through a change in the measured d-component of the voltage.

Testing symmetrical voltage dips with phase jump

A voltage dip with a phase jump complicates the compensation. Different control strategies have been treated in Section 5.2.1 and here simulations and measurements have been performed to test two different control strategies during a phase jump. The first method freezes to the pre-dip angle as indicated in Fig. 7.10 and the other method uses the PLL angle, which changes as the PLL starts to track a new angle of

the supply. The synchronization circuit in Fig. 7.10 is further described in Section 5.4.3.

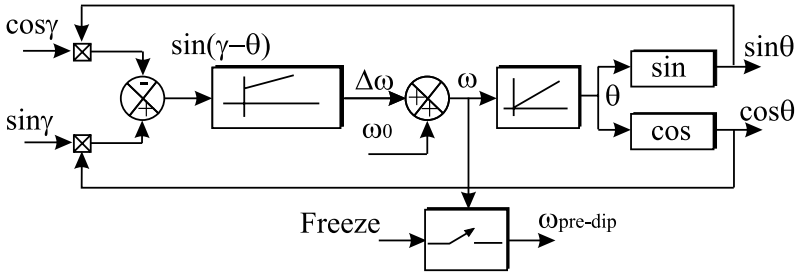


Figure 7.10: *PLL circuit with a freezing function to capture the pre-dip angular velocity and angle.*

The programmable power supply can generate arbitrary angles of the phase jump and has been used in the generation of voltage dips. A symmetrical 0.70 pu voltage dip with 15° negative phase jump and a duration of 80 ms is initiated and the response with the freezing control method is illustrated in Fig. 7.11. The graphs in 7.11a - c are measured by an oscilloscope and the graphs at Fig. 7.11d - f are measured by the DSP. Fig. 7.11d illustrates the angular difference between the freeezed angle and the actual supply angle. The freezed angular velocity is used for the transformations and the d- and q-supply voltage component can be seen in Fig. 7.11e - f. A q-voltage is here injected and at the load side the phase jump remains almost unnoticed. It can be concluded that the method can be used to protect the load from a phase jump.

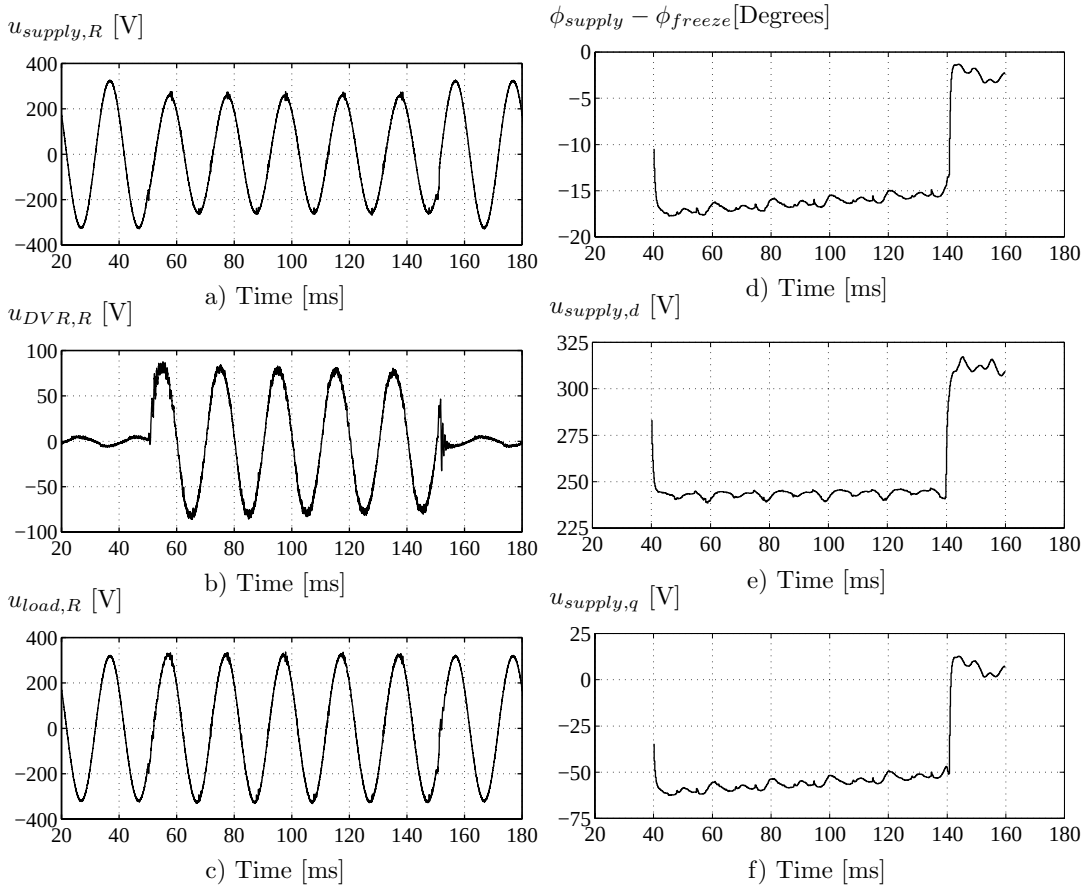


Figure 7.11: *Compensating symmetrical voltages dips with a phase jump using the freezing method. a) Supply voltage, b) DVR voltage, c) load voltage, d) angle between supply and PLL, e) d-component of the supply voltage and f) q-component of the supply voltage.*

The other method which is used to compensate voltage dips is referred to as an in-phase method and the method is shown in Fig. 7.12. The angle used for the transformations is the PLL angle and when the phase jump is initiated the PLL starts to track the new supply angle. The PLL is here rather fast with a rise time of approximately 20 ms, therefore after 20 ms the DVR injects voltages in-phase with the supply voltages. The load will experience a smooth phase change stretched over 20 ms. When the supply voltage returns, the load will experience the phase change again.

Some loads are sensitive to phase changes, and therefore the freezing method is considered to be the best method as explained in Section 5.2.1. The freezing method requires a higher voltage injection capability of the DVR, because the length of injected vector is larger with this method. The in-phase method can be applied when the loads connected are robust towards a phase-shift in the impressed load voltages. The time to smooth the phase shift can be controlled by altering the controller in the PLL circuit. Choosing a very slow PLL the response from the two methods can be very alike.

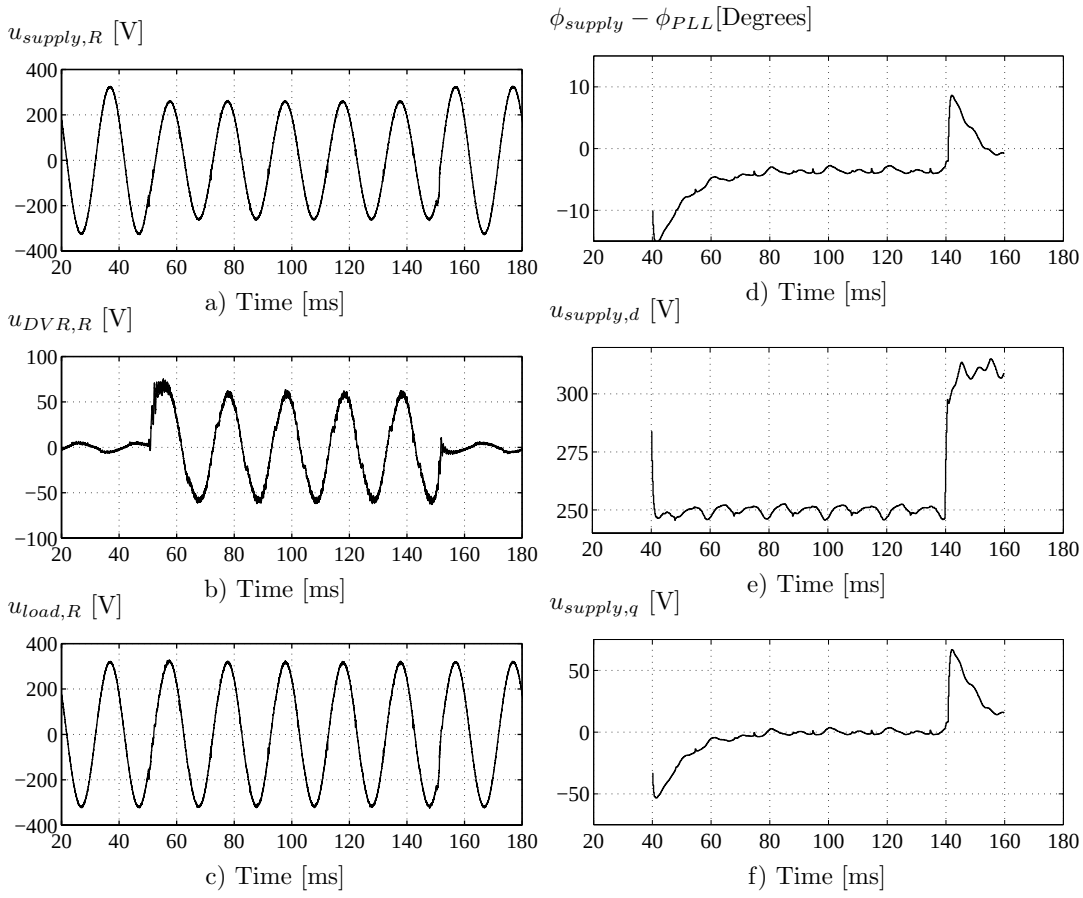


Figure 7.12: *Compensating a symmetrical voltage dip with a phase jump using the in-phase method. a) Supply voltage, b) DVR voltage, c) load voltage, d) angle between supply and PLL, e) d-component of the supply voltage and f) q-component of the supply voltage.*

Testing non-symmetrical voltage dips

Non-symmetrical voltage dips are more difficult to detect, and one of the reasons is the synchronization to the supply voltages. Non-symmetrical dips have been tested with the LV-DVR. Because of limitations in the hardware the DVR has only been loaded with 5 kW in this case.

The faults are typically expected to occur on a higher voltage level with a Dy transformer between the fault and the DVR. The test circuit for the non-symmetrical voltage dips is illustrated in Fig. 7.13. The Dy transformer does not transfer the zero sequence component, and line values are transformed to phase values.

If the fault occurs on the same level as the DVR, the character of the voltage dips changes and it can include zero sequence voltage components. The control strategy here is only developed for positive and negative sequence components.

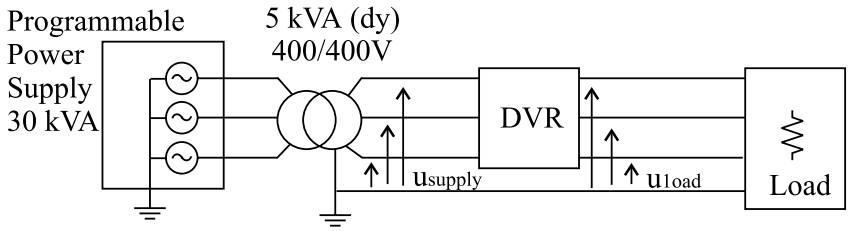


Figure 7.13: Test setup for non-symmetrical voltage dip using a dy transformer.

In the case of a single-phase fault, a reduction and a phase shift in two phases can be detected at the LV-side. During the fault two phase voltage makes a phase shift ideally to $0.76 \angle 131°$ and $0.76 \angle -131°$. To generate the voltage dip one phase of the power supply is reduced to 50 %. Even though two phases jump in phase, the space vector only reduces in size with no phase jump. The negative sequence component introduces a 100 Hz component in the dq-system, which can be seen in Fig. 7.14a with the dq-voltages measured by the DSP. The dq-reference voltage for the DVR contains also the 100 Hz component to inject a negative sequence component (see Fig. 7.14b) and the DVR reference voltages in the RST system is shown in Fig. 7.14c. Two of the reference phase voltages are phase displaced with 180°, which is required to bring the load voltages to pre-dip values. The actual DVR voltages are measured by an oscilloscope and illustrated in Fig. 7.14d. Compensating non-symmetrical faults is thereby possible with the open loop control strategy.

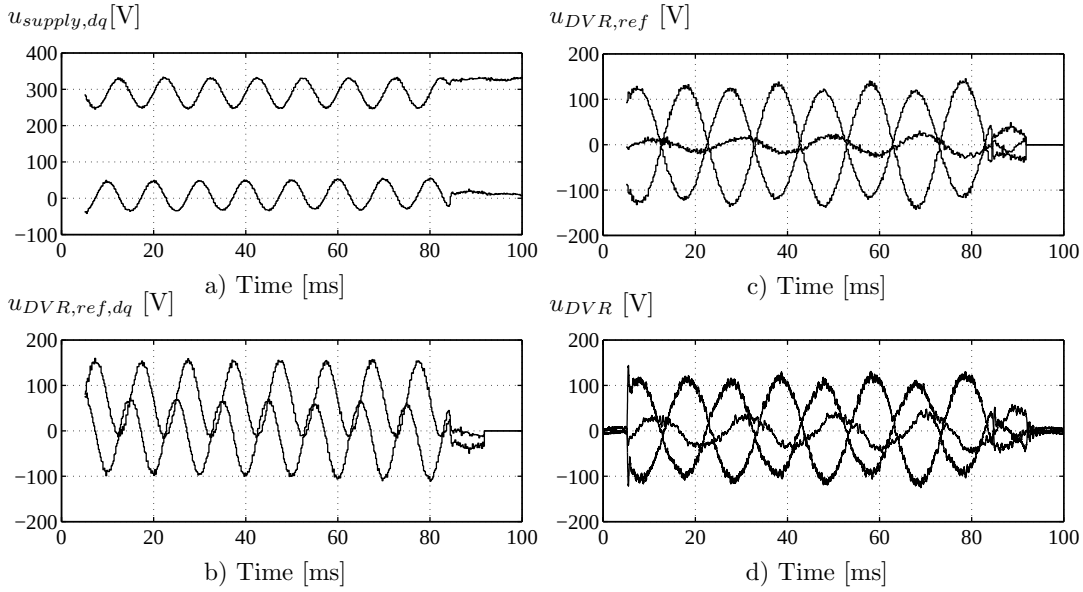


Figure 7.14: *Compensating of a non-symmetrical voltage dip. a) - c) are measured by the DSP and d) is measured by an oscilloscope. a) dq-supply voltage, b) dq-DVR reference voltage, c) DVR reference voltages and d) measured DVR voltages.*

7.3 Testing different system topologies

Four different topologies for DVRs have been tested, which all have been described and investigated in Section 3.3.3 page 31. It includes two topologies with stored energy and two topologies with power from the remaining supply voltage.

Different types of voltage dips have been applied. Here the functionality and performance is illustrated for a 0.78 pu symmetrical voltage dip without phase jump and a 5 kW resistive load.

7.3.1 Topologies with stored energy

In this case all power is stored before the voltage dip and a very small scale converter is used to re-charge the energy storage. Two basic methods have been tested, which is the constant DC-link voltage (shown in Fig. 3.8 page 33) and the variable DC-link voltage (shown in Fig. 3.9 page 33). Topologies with stored energy do not increase the current drawn from the supply, and the power taken from the grid is reduced according to the voltage dip size.

Constant DC-link voltage

In this test an undisturbed auxiliary supply charges the DC-link to be almost constant during the test. Fig. 7.15 illustrates the measured response. The supply

voltage drops and the DVR injects the missing voltage and restores the voltage. During the compensation the supply and the load current are almost unchanged, and the DC-link voltage is almost constant. The DVR performance is acceptable with a very low distortion of the load voltages and a almost unchanged current draw from the supply.

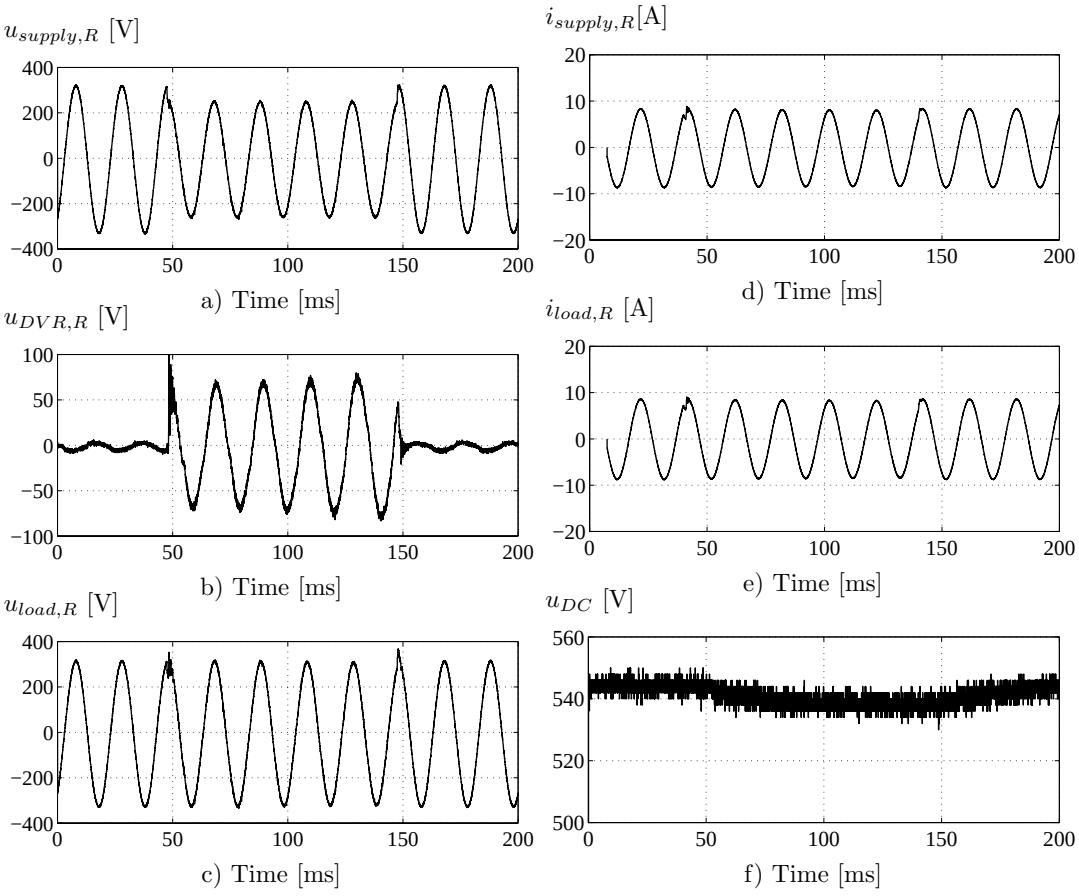


Figure 7.15: *Testing a DVR topology with stored energy and a constant DC-link voltage. a) Supply voltage, b) DVR voltage, c) load voltage, d) supply current, e) load current and f) DC-link voltage.*

Variable DC-link voltage

Variable DC-link voltage offers benefits in simplicity and performance. It requires an energy storage, but the rating of associated converters are very low. The voltage injection capacity depends on the actual state of the DC-link voltage, and energy saving control strategies are important in order to fully utilize the energy storage system. Over modulation control have not been included in the control and below 400 V the DVR is bypassed in order to avoid initiating the DC-link voltage protection.

A voltage dip has been applied and the measured response is illustrated in Fig. 7.16. The DVR restores the load voltage and the DC-link voltage is reduced until the supply voltage returns.

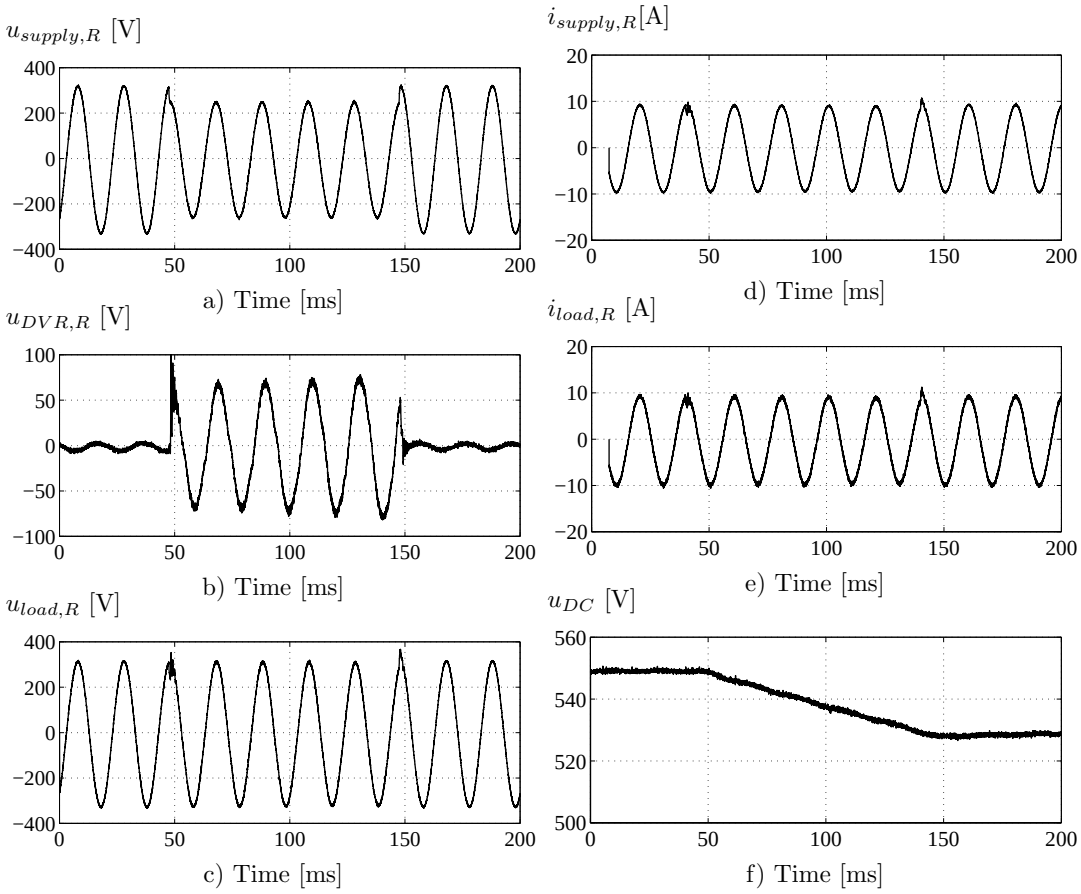


Figure 7.16: *Testing a DVR topology with stored energy and a variable DC-link voltage. a) Supply voltage, b) DVR voltage, c) load voltage during, d) supply current, e) load current and f) DC-link voltage.*

7.3.2 Topologies with power from the supply

Taking power from the remaining grid voltage has the disadvantages of an increase in the supply current, but the energy storage can be avoided. Taking power from the grid may disturb the neighboring loads, because the DVR protects its downstream loads by taken more current from the supply, which may lead to a more severe voltage dip for upstream loads.

Topologies for DVR using the grid can generally be characterized with the location of the shunt converter e.g. at the supply side of the DVR (Fig. 3.10 page 34) or at the load side of the DVR (Fig. 3.11 page 35). Additionally, the shunt converter can be an active or a passive type. In this thesis only passive six pulse diode rectifiers are used as shunt converters.

Supply side connected passive shunt converter

A supply side connected passive shunt converter has the benefits of a very simple topology with low energy storage requirements, the response to a symmetrical voltage dip has been tested on the LV-prototype.

Fig. 7.17 illustrates the supply voltage, the DVR voltage, the load voltage, the supply current, the shunt current and the DC-link voltage. The DC-link is charged to normal DC-link voltage. At t = 10 ms a voltage dip appears, and power is supplied from the DC-link until the DC-link voltage is below $\sqrt{2}U_{supply}$ in this case at t = 48 ms. From this point the active power supplied to the load comes partly from the energy storage and the supply until (approximately 58 ms) the DC-link voltage has stabilized to a voltage, dependent on the dip depth and the power drawn by the load. All the power is at this point supplied from the supply, transferred via the shunt converter to the DC-link. When the supply voltage returns (t = 60 ms) to pre-dip level a large in-rush current can be detected and the DC-link is charged to the pre-dip voltage level.

The supply side connected shunt converter is a topology with very low energy storage requirements and the possibility to supply an undisturbed load voltage. The shunt current is, on the other hand, very uncontrollable at non-symmetrical voltage dip, and the current drawn by the shunt converter will be very uneven distributed between the phases. The DC-link level is fully dependent of the voltage dip depth. Severe voltage dips require a high voltage injection, but the DC-voltage can in such a case be expected to be low.

Load side connected passive converter

A DVR with a load side connected passive converter can to some extend keep the DC-link voltage high, because the load voltage is controlled by the DVR itself. The disadvantage is the currents handled by the series converter during a voltage dip significantly increase, and the load voltages tend to be more distorted, because of the non-linear current drawn by the shunt converter.

Fig. 7.18 illustrates the measured response of a DVR with a load side connected shunt converter. The shunt converter draws a steady state current before the dip to ensure full DC-link voltage. In the beginning of the voltage dip, the shunt currents are zero, because the load voltages are compensated to a slightly lower voltage and the active power is taken from the DC-link. As the DC-link is drained for energy, the shunt currents are steadily increased and the currents are stabilized to a point, where all power is taken from the supply. At the time the load voltage is restored, a high shunt current can be detected as a response to a higher load voltage and the DC-link is charged back to the pre-dip voltage. The non-linear current drawn by the shunt converter can be seen at the voltage across the DVR and a slightly more distorted load voltage can also be seen.

A DVR with this system topology, seems to be a very effective solution to keep the DC-link almost constant. In the case of non-symmetrical voltage dip the currents taken from the supply are still taken equally from each phase.

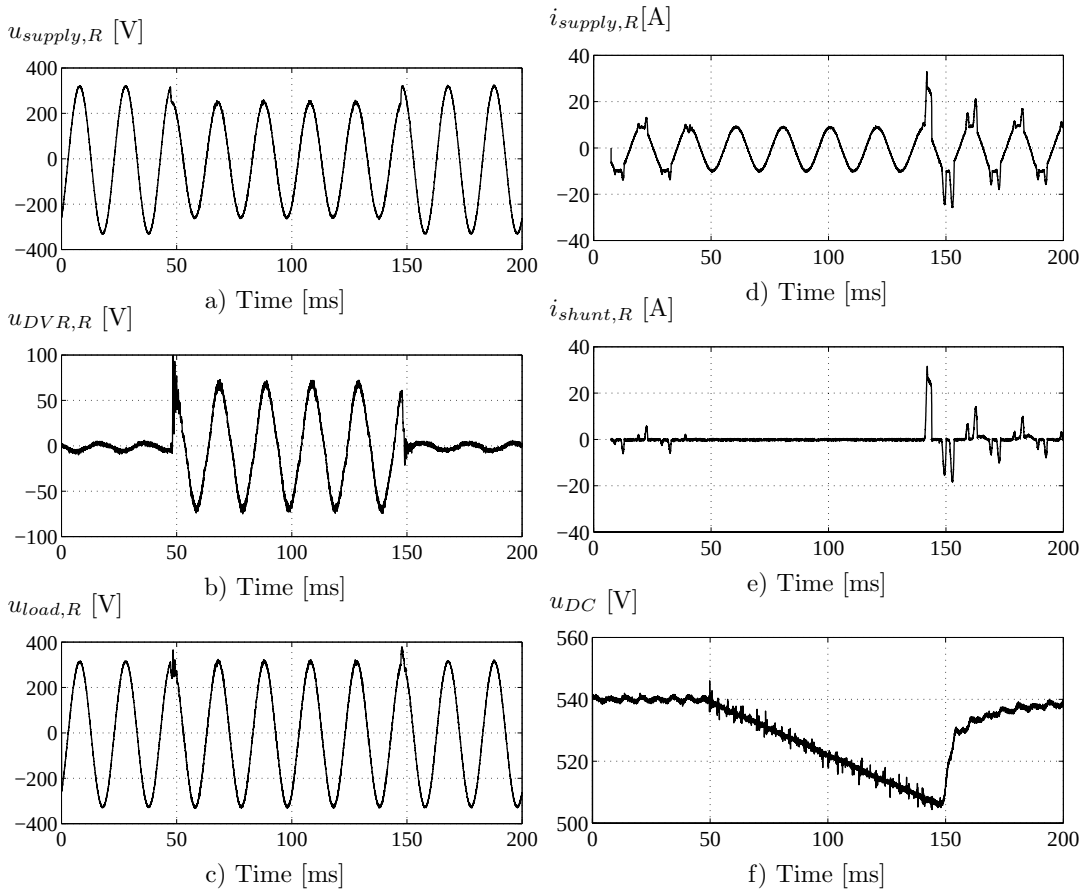


Figure 7.17: *Testing a DVR topology with power from the supply and a supply side connected passive shunt converter. a) Supply voltage, b) DVR voltage, c) load voltage, d) supply current, e) shunt current and f) DC-link voltage.*

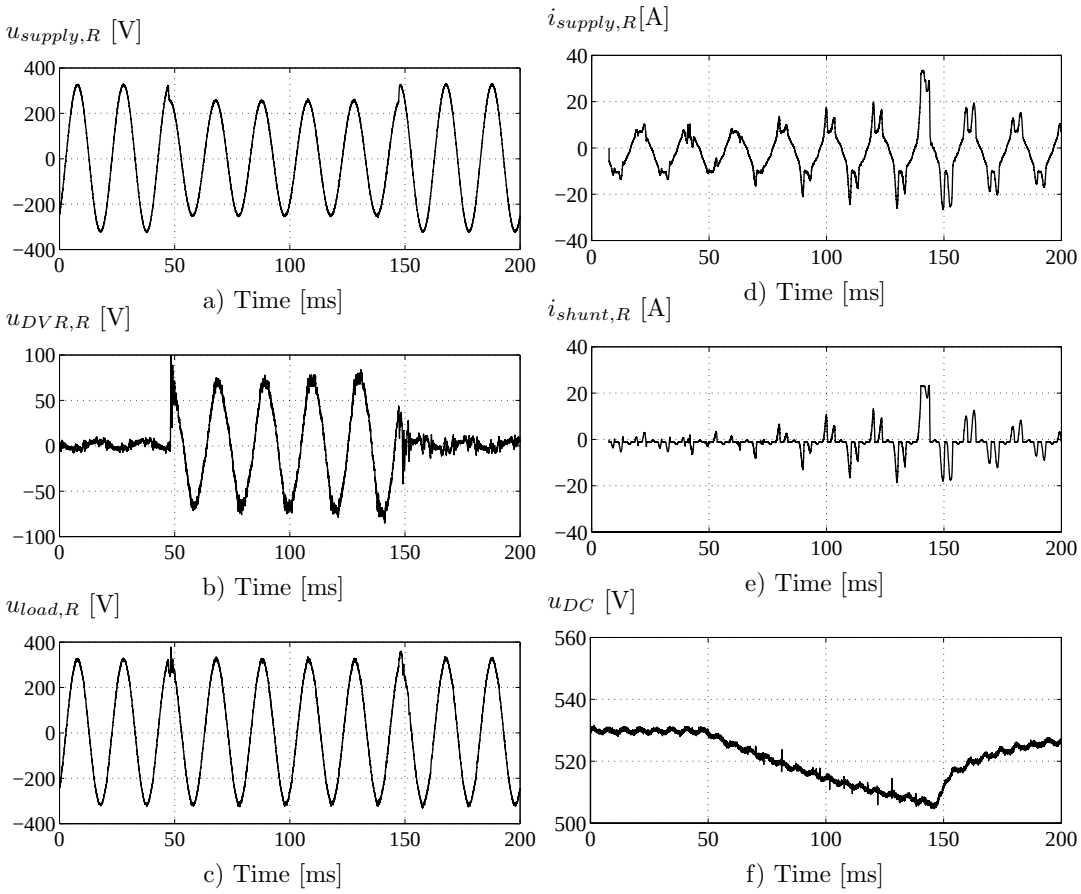


Figure 7.18: *Testing a DVR topology with power from the supply and a load side connected passive shunt converter. a) Supply voltage, b) DVR voltage, c) load voltage, d) supply current, e) shunt current and f) DC-link voltage.*

7.4 Summary and conclusion

The chapter shows some of the measured and simulated results from the first prototype DVR. Tests have been performed, which verifies a number of important issues for the control of a DVR:

- Non-linear loads can be protected by the DVR, but the load voltage distortion increases significantly because of the voltage drop across the DVR and oscillations in the line-filter. Especially high distorted load currents in combination with a low resistive load tend to initiate oscillations between the series transformer and the filter capacitor.
- Symmetrical voltage dips can be handled by the control method, and two control methods have been developed and tested in order to be able to compensate voltage dips with phase jump. Different linear loads are handled without problems by the DVR, light resistive loads tend to give a poor damping of the oscillations in the transition phases.
- Non-symmetrical voltage dips with a negative sequence voltage component can be handled by the DVR and the implemented control method. Control of the zero sequence components have not been implemented.
- An investigation of the performance of different system topologies for DVRs have been performed. It has been limited to include four topologies of methods to source power to the DC-link.

Chapter 8

Control and testing of the HV-DVR

The chapter explains more specifically how the HV-DVR is controlled and the testing of the HV-DVR is performed. First the test results from the testing at Aalborg University with high voltage - low power are presented followed up by the high voltage - high power test at DEFU′s test facilities at Kyndby.

8.1 Control of the HV-DVR

The parameters for the HV-DVR are presented in Section 4.3.3 page 63 and the hardware is illustrated in Fig. 4.9 page 63. The HV-DVR is controlled by a feedback controller in a rotating dq-reference frame. Fig. 8.1 illustrates the control method used to control the HV-DVR. Feedforward is used in order to have better compensation of non-symmetrical voltage dips and a fast clearance of the injected voltage at the return of the supply voltages. The voltages are restored to 1 pu, because the voltage dips, which are possible to generate at the test site are not below 0.75 pu, and the restoration to 1 pu gives the best possibility to verify the DVR′s injection and operation capabilities.

To reduce the in-rush currents into the injection transformers and the risk of deep saturation of the transformers the d-reference supply voltage is controlled according to the depth of the voltage dip, which gives a deliberately slower response with a lower risk of high oscillations and saturation. In-rush saturation can still occur in the DVR transformer at high injection values. In order to control the in-rush current, the converter currents are monitored and above twice the rated current. The converter reference voltages are on a per phase base changed to zero and not applied until a reversed reference voltage is given. This method can give some distortion of the load voltages. The voltage dips are detected at the first crossing of the 0.85 pu of the space vector magnitude. In the following 1.7 ms the start d-reference voltage is set and a first order digital filter changes the d-reference to 1 pu voltage. The time constant of the digital filter is chosen to be 20 ms.

Synchronization to the supply and the modulation method are equal to the methods implemented for the LV-DVR described in Section 5.4.3 and Section 5.6.4, respectively.

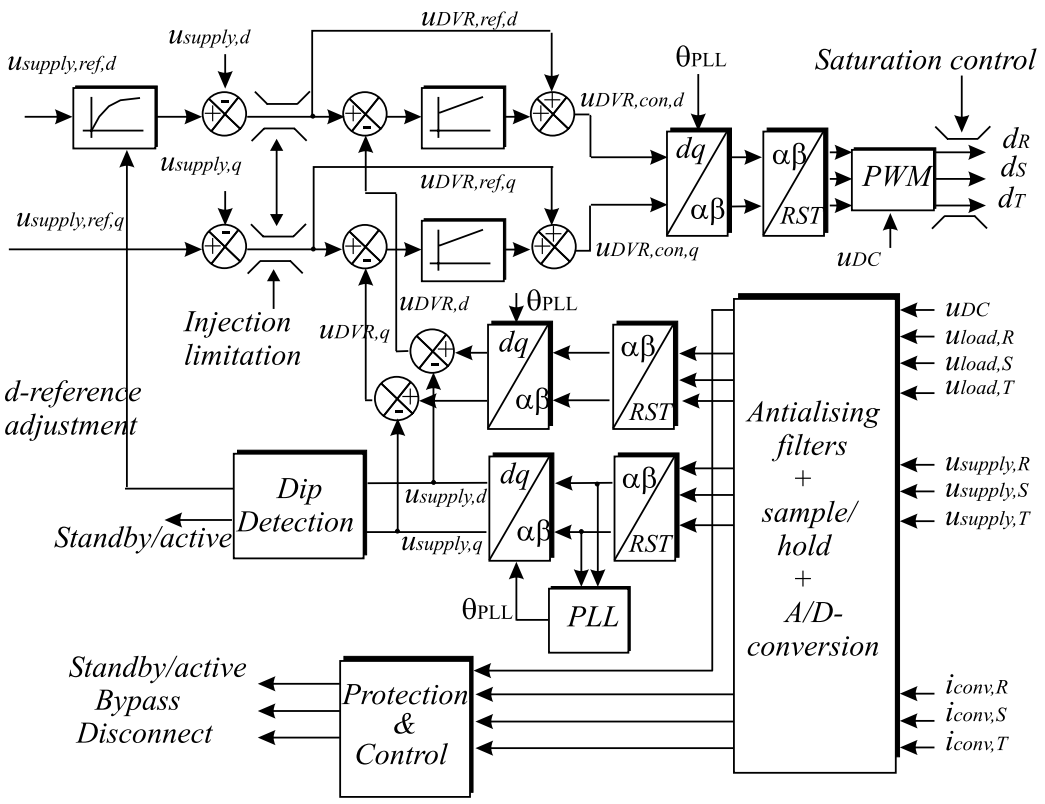


Figure 8.1: Control strategy for the HV-DVR in a rotating dq-reference frame.

DC-link voltage control

Regarding the DC-link voltage, the charging is achieved with two DC-voltage supplies instead of the passive diode bridge used for the first prototype. The voltage is held high in the pre-dip condition, and during the voltage dip the DC-link voltage is reduced, and below 200 V the DVR is switched to standby mode and the power supplies will automatically re-charge the DC-link. The power rating of the charging power supplies are 300 V/5A each. Thereby the DC-link can be charged to 600 V with a 3 kW power rating, which is less than 1 % of the rated load to protect. The two power supplies are unidirectional and cannot absorb power. The DC-link voltage is mostly set to 2 X 300 V to have maximum energy stored in the DC-link.

Protection of the HV-DVR

The HV-DVR is protected differently than the LV-DVR by having a mechanic bypass breaker on the secondary side of the transformer, and it is made in this way in order to utilize an existing LV-breaker.

The HV-DVR is not sufficiently short circuit protected, but the design of the DVR has made it likely, that it can survive a short circuit close to the DVR at the load side.

8.2 High voltage/low power test - Aalborg University test site

The control of the HV-DVR is first verified through high voltage - low power tests at Aalborg University. The test setup and how to generate voltage dips are first described followed by different test results.

8.2.1 Test site and generation of voltage dips

Extensive testing have been done in the laboratory in order to find the best control method and verify the operation of the HV-DVR under different load conditions. The HV-DVR has been tested with the test setup illustrated in Fig. 8.2. The

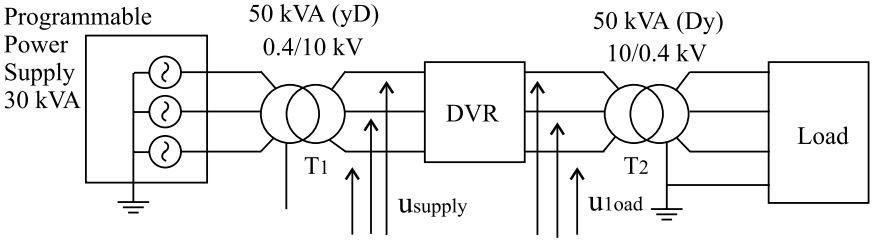


Figure 8.2: *Test setup of the HV-DVR at Aalborg University high voltage laboratory.*

supply is a 30 kVA three phase 400 V programmable power supply with the neutral connected to ground. A 50 kVA 0.4/10 kV distribution transformer (yD) steps up the voltage to 10 kV line voltage. In a real system the power would come from a higher voltage level and could be stepped down by a 50/10 kV Yy transformer. The DVR is connected at the 10 kV level and the load is a 50 kVA 10/0.4 kV (Dy) distribution transformer, which steps down the voltage to a 400 V line voltage. A low rated load can be connected at the LV side and a large part of the power rating of the supply is used to magnetize the two distribution transformers. The setup is still very useful to test the dynamic behaviour of the DVR and the performance during different voltage dips. Fig. 8.3 shows two pictures of the test setup for the HV-DVR at Aalborg University.

The characteristics for all the tests at Aalborg University are that:

- The supply voltages are ideal supply voltages and the voltage dips are programmed to be ideal voltage dips.
- The short circuit impedance at the connection point of the DVR is very high, because of the limited current capabilities of the power supply and the low rating of the step-up transformer.
- The load is very light, consisting of a small distribution transformer and a small resistive load.

a) b)

Figure 8.3: *The Aalborg University test site for the HV-DVR. a) Side view of the DVR container with the step-up and step-down transformers. b) Front view of the DVR with the DC-supply and measurement system to the left, the PC and DSP to the right and in the back the converter rack with the DC-circuit and line-filters.*

The ideal conditions can be beneficial to evaluate the DVR performance at well defined voltage dips, but the conditions are relatively far from real site conditions.

8.2.2 Testing symmetrical voltage dips

Severe voltage dips are possible to test with the setup and during a severe voltage dip the in-rush currents to the injection transformers can be high. A symmetrical voltage dip is generated by the programmable power supply, and the DVR response measured by the DSP controller can be seen in Fig. 8.4. In this case no pre-triggering is initiated and the voltage dip is 0.67 pu with a duration of 100 ms. The load is very light resistive of approximately 3 kW, which is equal to 0.0075 pu of the rated load.

The 0.67 pu voltage dip is well compensated with a fast initial response with the DVR almost instantly injecting 600 V RMS as it can be seen in Fig. 8.4b and a slower compensation to fully restorer the load voltages.

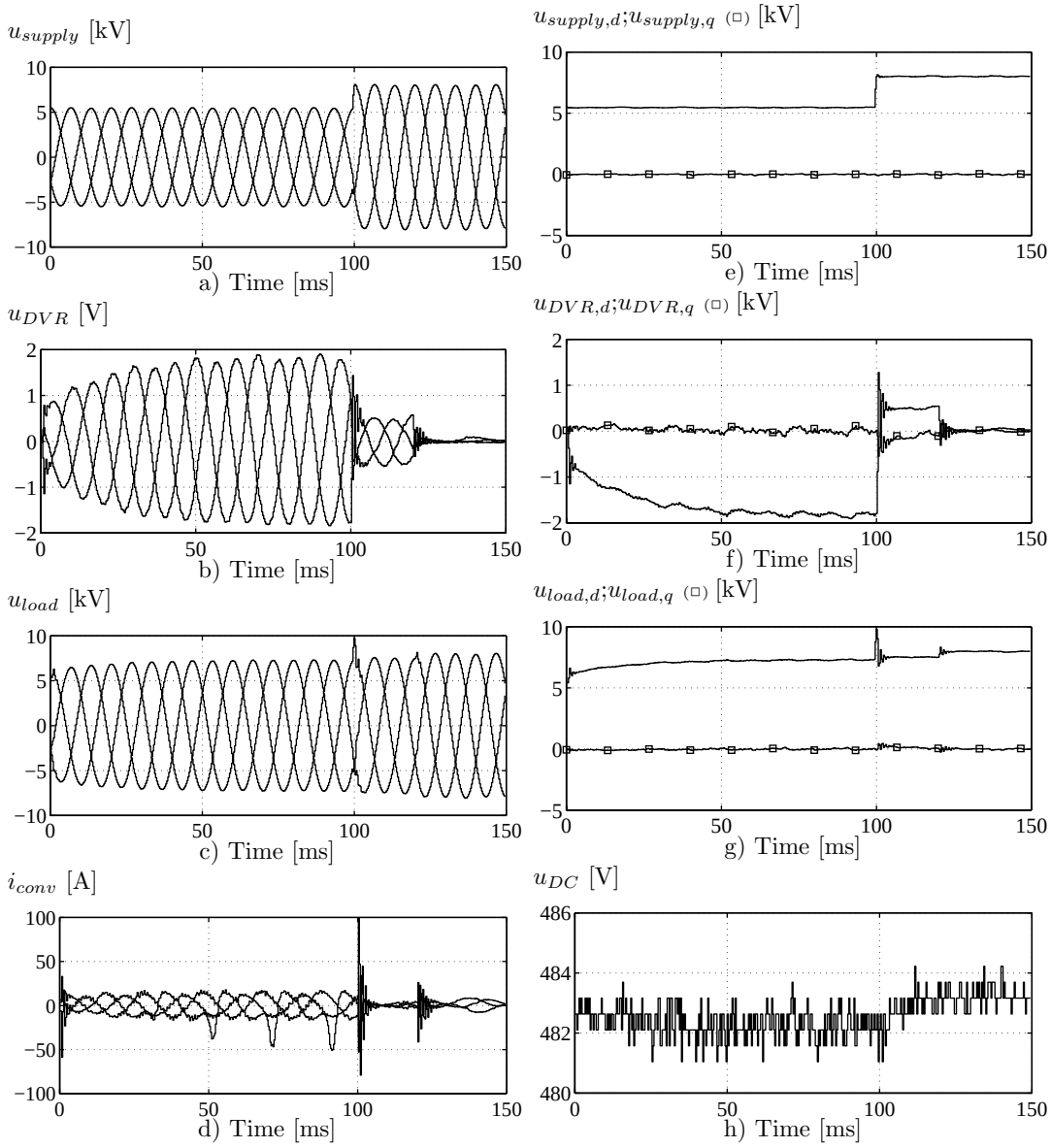


Figure 8.4: *A symmetrical voltage dip response measured by the DSP controller in the Aalborg University laboratory. a) Supply voltages, b) DVR voltages, c) load voltages, d) converter currents, e) dq-supply voltages, f) dq-DVR voltages, g) dq-load voltages and h) DC-link voltage.*

An FFT analysis (0 - 1500 Hz) of the response of the load and supply voltage in the period (75 - 95 ms) indicates only 0.6 % voltage THD of the supply voltage and 0.35 % non-symmetry. The load voltages also only contain 0.5 % voltage THD and 0.6 % non-symmetry.

Fig. 8.5 illustrates another compensation with high distortion of the supply voltages, caused by a current limit in the programmable power supply. The load voltages are distorted, because of the distorted supply voltages and the injected

DVR voltages. In this case an active limitation of the in-rush current to the injection transformers gives distortion of the load voltages. E.g. at t = 25 ms in Fig. 8.5b one of the converter phase voltages is set to zero to limit the in-rush current. The operation distorts the load voltage, but presumably a majority of loads would be rather insensitive to this control method. Other methods to avoid distortion of the load voltages are to increase the rated dynamic current limit of the converter, increase the saturation level of the injection transformers or decrease the bandwidth of the control. The distortion of the supply voltages in Fig. 8.5a illustrates some of the difficulties of testing the HV-DVR at high voltage and low power.

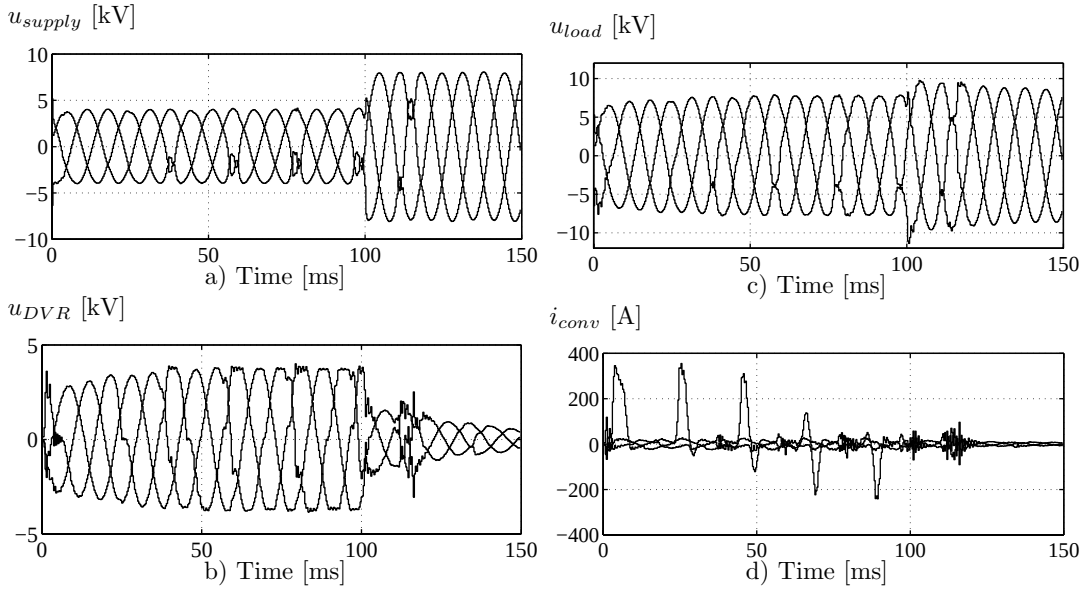


Figure 8.5: *Symmetrical voltage dip response measured by the DSP controller in the Aalborg University test laboratory. a) Supply voltages, b) DVR voltages, c) load voltages and d) converter currents.*

8.2.3 Testing non-symmetrical voltage dips

Testing of a non-symmetrical voltage dip is illustrated in Fig. 8.6. The voltage dip is generated by reducing one supply voltage to zero, and at the MV-level the voltage dip is controlled by a change in magnitude and angle of two phases. The non-symmetry of the supply is 34 %, and the positive sequence component is reduced to 0.73 pu. The load voltages are not fully restored and voltage harmonics are injected by the DVR. By analysis the non-symmetry is decreased to 6 % and the positive sequence voltage dip is reduced to 0.89 pu with a set point of 0.9 pu. A harmonic analysis of the load voltages reveals an increase in the third harmonic positive sequence component from zero to 3.0 % of the fundamental positive sequence load voltage. The component is unwanted and will be transferred to the LV load. The component originates from the control in a rotating dq-control and an insufficient tuning of the PLL circuit.

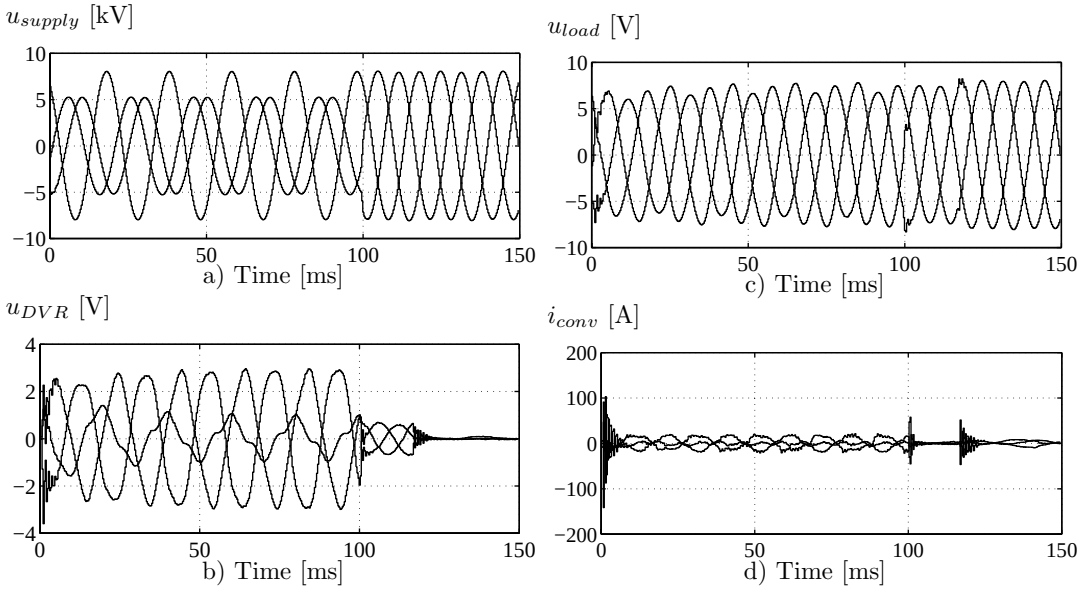


Figure 8.6: *Non-symmetrical voltage dip response measured by the DSP controller in the Aalborg University test laboratory. a) Supply voltages, b) DVR voltages, c) load voltages and d) converter currents.*

A method to reduce the oscillation at the beginning of a voltage dip is to operate the DVR continuously in active compensation mode and the load voltages are controlled to symmetrical voltages. At high supply voltages the power is sourced into the DC-link, which is a problem with the uni-directional DC-link charger and the reference voltage has to be adjusted to keep the DC-link voltage constant. At low supply voltages the DVR may inject a large amount of power, which likely will be above the 3 kW of DC supplies and the DC-link voltage will decay. To avoid these problems with active power, the injected voltage is zero and below a certain threshold value the DVR enters into active compensation mode.

8.3 High voltage/high power test - the Kyndby test site

A number of tests have been performed at DEFU′s test laboratory at Kyndby. At the test facility it is possible to insert the DVR in a medium voltage (10 kV) distribution system. The distribution system is realistic and consists of several options to connect to the grid. It is possible at the test site to test the DVR at high voltage and protecting a relatively high rated load. The test site is first described followed be the methods used to generate voltage dips. Finally, test results from stationary and dynamic tests of the HV-DVR are presented.

8.3.1 Test site and generation of voltage dips

The Kyndby test site

The distribution system is fed from a 132/50 kVA 70 MVA transformer. The test site has its own 50/10 kV 12/15 MVA transformer and a 10/0.4 kV distribution grid. The DVR is connected to a 10 kV distribution system after a 40 A HV fuse in a sub station feeding one 400 kVA 10.5/0.4 kV transformer. The distribution transformer can be loaded with 125 A and the maximum loading available is 11 x 9 kW.

A schematic drawing and location of the DVR is illustrated in Fig. 8.7. The voltage dips are generated by controlled short circuits at the LV-side of a the distribution transformer T_{sc}. The breaker B_2 is a low voltage controllable breaker (Sace Novomax), which primary task is to connect and clear a short circuit on the LV-side. The B_1 breaker is connected at the high voltage side and its primary tasks are to magnetize the transformer and function as a backup breaker, and to clear any faults in the shorting transformer (T_{sc}) or any misbehavior by the LV-breaker.

The data acquisition system is illustrated in Fig. 8.8. Four 4-channel oscilloscopes (8 bit Tektronix TDS3000) are triggered by a common trigger signal generated by the short circuit control. The oscilloscopes record the three load HV currents (i_{load}), the three HV load voltages (u_{load}), the three HV supply voltages (u_{supply}) and the three radial currents of the 10 kV radial (i_{radial}). The radial currents are the sum of all the currents, and it includes the load currents, short circuit currents, magnetization and charging currents. All measured load and supply voltages with the oscilloscopes are recorded with an 8 bit oscilloscope and the quantification steps are 97 V.

Data is also collected by the DSP, and the DSP receives 10 channel inputs from the A/D converter. If the DSP detects a voltage dip, 16 variables are stored with the pre-dip values and the length of the DSP data sets are 450 samples. The load and supply voltages are measured and stored both by oscilloscopes and the DSP controller.

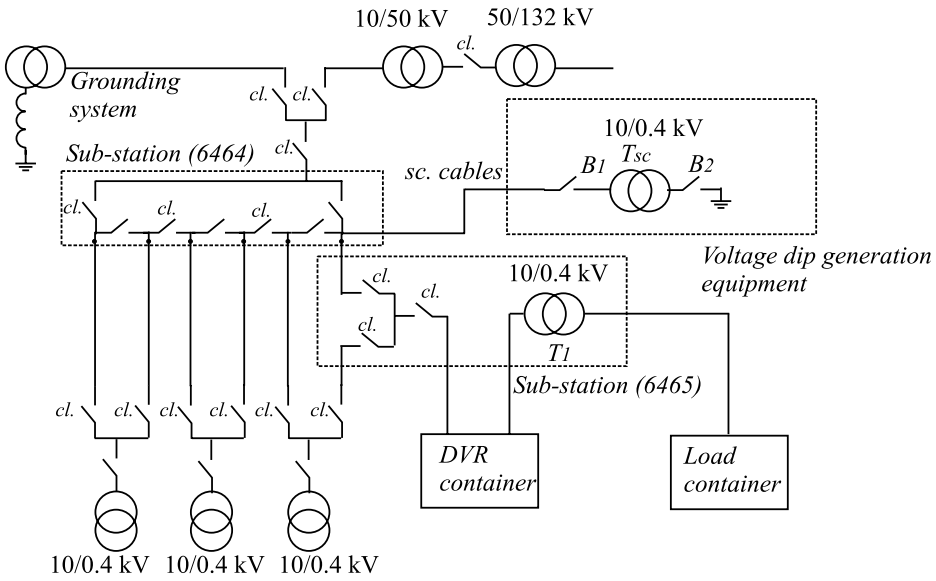


Figure 8.7: *Schematic diagram of the Kyndby test site. The DVR is connected to the 6465 sub-station and three short circuit cables are connected in the 6464 station to the voltage dip generation equipment. The breaker status during the tests are indicated with cl. for closed.*

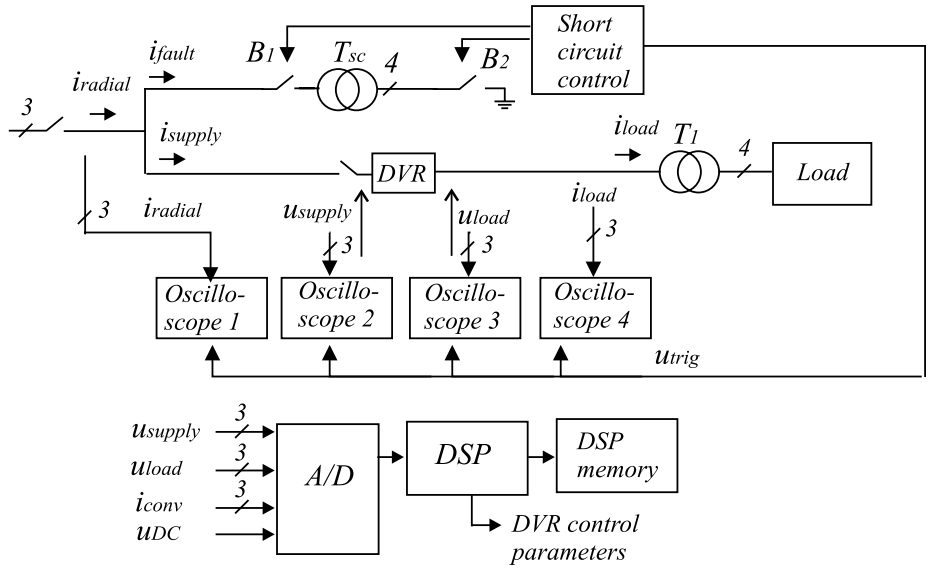
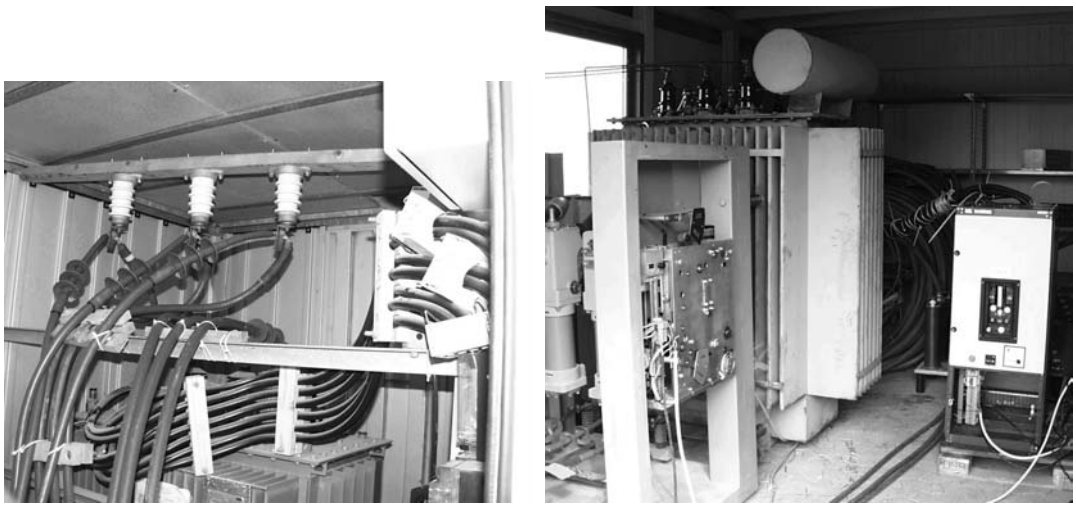


Figure 8.8: *The acquisition system used during the tests with four oscilloscopes with common triggering and furthermore data is collected by the DSP controller.*

In Fig. 8.9a the Kyndby test site is illustrated and in Fig. 8.9b the sub-station with the DVR container in the back. The connection of the DVR and the short circuit equipment are pictured in Fig. 8.10

a) b)

Figure 8.9: *The Kyndby test site. a) DEFU's test site and b) The connection of the DVR close to the 6465 sub-station with 6 HV cables from the DVR to the sub-station.*



a) b)

Figure 8.10: *The Kyndby test site. a) The connection of the DVR in the 6465 sub-station. Below the 400 kVA distribution transformer (T_1) can be seen and b) The HV breaker (B_1) to the left, the shorting transformer (T_{sc}) and the LV-breaker (B_2) to the right.*

Generation of voltage dips

The generation of a voltage dip in a strong 10 kV radial is not trivial and requires a triggering of a short circuit in the grid followed by a clearing of the fault. The maximum voltage dip is generated by connecting the sensitive load at the weakest point at the test site and generate the fault close to the connected DVR. The expected voltage dip was estimated by:

$$\underline{U}_{dip} = \underline{U}_{supply}\frac{\underline{Z}_{fault}}{\underline{Z}_{fault}+\underline{Z}_{supply}} = \underline{U}_{supply}\frac{\underline{Z}_{sc.-transformer}}{\underline{Z}_{sc.-transformer}+\underline{Z}_{supply}} \tag{8.1}$$

The simplified circuit and vector diagram for (8.1) are illustrated in Fig. 2.1 and Fig 2.2 page 12. The impedance after the 50/10 kV transformer to an infinite busbar can be estimated to:

$$\underline{Z}_{inf} = (0 + j0.41)\,\Omega \tag{8.2}$$

The supply impedance $\underline{Z}_{supply}$ can be altered by connecting or disconnecting existing MV cables or overhead wires in the distribution grid. Z_{supply} is was chosen as large as possible in order to be able to generate a significant voltage dip. The maximum supply impedance was calculated to:

$$\underline{Z}_{cable+line} = (2.59 + j1.50)\,\Omega \tag{8.3}$$

$$\underline{Z}_{supply} = \underline{Z}_{inf} + \underline{Z}_{cable+line} = (2.59 + j1.91)\,\Omega \tag{8.4}$$

The impedance of the shorting transformer (T_{sc}) is the short circuit impedance, which consists of the resistive part and the leakage inductive part. Using ordinary distribution transformers the inductive and resistive parts depends on the size of the transformer and the method to change the shorting transformer impedance $Z_{sc.-transformer}$ is to change the power rating of the transformer. A 630 kVA and a 600 kVA transformer were at disposal and the impedance of the transformer can be calculated to:

$$Z_{sc.-transformer} \simeq \frac{U^2_{sc.-transformer}}{S_{sc.-transformer}}(u_r + ju_x) \tag{8.5}$$

$$Z_{sc.-transformer} = \frac{(10\,kV)^2}{630\,kVA}(0.01 + j0.047)\Omega = (1.59 + j7.47)\,\Omega \tag{8.6}$$

Thereby the maximum voltage dip can be estimated to:

$$\underline{U}_{dip} = 10kV\frac{(1.59 + j7.47)\Omega}{(2.59 + j1.91 + 1.59 + j7.47)\Omega} = 7.4\,kV\angle -12^\circ \tag{8.7}$$

$$\underline{u}_{dip} = 0.74\,pu\angle -12^\circ \tag{8.8}$$

The phase jump may be different compared to a voltage dip originated from a HV transmission fault. A primary concern for all the equipment in the fault current path is the short circuit current flowing into the fault. Here the thermal and dynamic stress on the equipment must be within acceptable limits and the ability to clear

the fault must be ensured sufficiently. The symmetrical short circuit current can be estimated to:

$$\underline{I}_{k,(3)} = \frac{\underline{E}}{\sqrt{3}(\underline{Z}_{sc.-transformer} + \underline{Z}_{supply})} \tag{8.9}$$

$$\underline{I}_{k,(3)} = \frac{10kV}{\sqrt{3}(4.18 + j9.37)\ \Omega} = 563\ A\angle -66^{\circ} \tag{8.10}$$

The impedance inserted by the shorting transformer (T_{sc}) is here a main parameter to the size of the short circuit current.

A voltage dip generated by the LV-breaker (B_2) is illustrated in Fig. 8.11 and the DVR is during the test in mechanical bypass mode. In the initial phase of the voltage dip, oscillations can be seen. The oscillations takes place at the return of the supply voltages. The frequency of the oscillation is approximately 1850 Hz, which originates from a natural frequency in the system. The oscillations in the supply voltages will also be present when the DVR is inserted and will to some extent influence the control of the DVR.

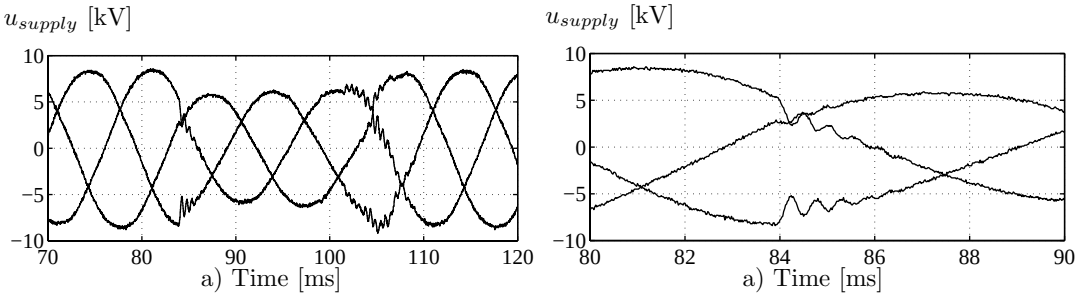


Figure 8.11: *A measured symmetrical voltage dip done by connecting and disconnecting the LV-breaker. a) Measured supply voltages in front of the DVR from 70 - 120 ms and b) zoomed view of the supply voltages from 80 - 90 ms.*

Another symmetrical short circuit is generated and the currents in the 10 kV radial are illustrated in Fig. 8.12 in which the short circuit currents are dominating. It can be seen that after the DC component in the currents are fading out, the short circuit currents are constant and almost equal in amplitude. The stationary short circuit currents are approximately by 495 A RMS at the 10 kV side and 12.3 kA at the 400 V side. After approximately 110 ms a command is given to the LV-breaker to clear the fault. During the process of clearing the fault large arcs are generated (> 0.5 m) and extinguished. The fault currents decays and they are forced to zero. After the fault is cleared, in-rush currents to the 10/0.4 kV distribution transformers (T_{sc}) can be seen.

The resulting supply voltage in front of the DVR can be seen in Fig. 8.12b. Before the fault, the synchronous line voltage is measured to 10.3 kV during the dip the voltages drop to a synchronous line voltage of 7.6 kV, which is equivalent to a 0.74 voltage dip. This is currently the maximum voltage dip possible at the test

site. The length of the voltage dip can be controlled from 30 ms - 150 ms. Below 30 ms the breaker cannot react and above 100 ms the site protection will interact with the test.

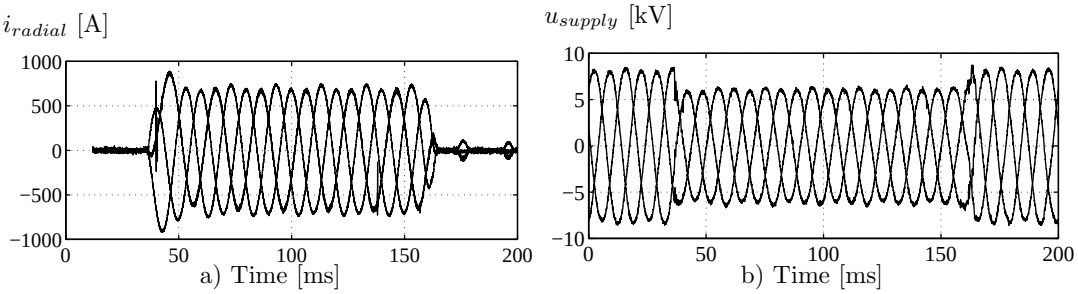


Figure 8.12: *The generation of a voltage dip and a measured symmetrical voltage dip. a) Radial currents and b) supply voltages.*

8.3.2 Testing stationary performance

First, the stationary performance have been monitored and the DVR is conducting the load current in a so called standby mode without injecting any voltages. The standby mode is compared with the bypass mode in which the load current flows through the mechanical bypass breaker. In the bypassed mode the injection transformers are still connected, mainly because the bypass switch is at the secondary low voltage side. Three stationary conditions have been monitored, which are:

1. Light load (9 kW resistive load)
2. Heavy load (99 kW resistive load)
3. Nonlinear load (A frequency converter is feeding an induction motor, which by the shaft is loaded with a PM synchronous generator and the generator is finally loaded with 45 kW resistive resistive load. The converter has a 6 pulse diode bridge in the rectifier stage.)

Only load condition three is shown with time domain plots. Fig. 8.13a - d illustrates the DVR in mechanical bypass with the series transformer still connected and in Fig. 8.13e - h in the standby mode with current flowing through the DVR converter. The voltage drop increases in standby mode because of the extra voltage drop in the LV-cables and the DVR semiconductors. The DVR voltages in Fig. 8.13b and 8.13f are calculated by subtracting the supply voltages from the load voltages and therefore the quantification noise is significant.

The supply voltage, the load voltage and the load current in Fig. 8.13 have been FFT analyzed. The positive sequence component, the negative sequence component and the THD have been calculated for the case with non-linear load. The results are listed in Table 8.1. The fundamental voltage drop across the DVR for this small load is 0.8 % in the standby mode and 0.5 % in bypass mode. The load voltage is

Parameter	**Abbreviation**	**DVR bypassed**	**DVR standby**
Supply voltage	U_1/U_{rated}	1.023 pu	1.023 pu
	$(U_2/U_1)100\,\%$	0.36 %	0.34 %
	$U_{THD,R}$	1.79 %	1.95 %
Load voltage	U_1/U_{rated}	1.018 pu	1.015 pu
	$(U_2/U_1)100\,\%$	0.27 %	0.16 %
	$U_{THD,R}$	2.07 %	2.94 %
Load current	I_1	1.89 A	1.91 A
	$(I_2/I_1)100\,\%$	5.4 %	3.02 %
	$I_{THD,R}$	61.4 %	55.0 %

Table 8.1: *Measurements with non-linear load in standby and bypassed mode. The subscript 1 indicates a positive sequence value and the subscript 2 indicates a negative sequence value.*

decreased, when the DVR is in standby and the voltage THD is increased. The load

current is less distorted when the DVR is inserted, because of the increased supply impedance. Generally the stationary performance seems acceptable and the shown influence from the DVR was expected.

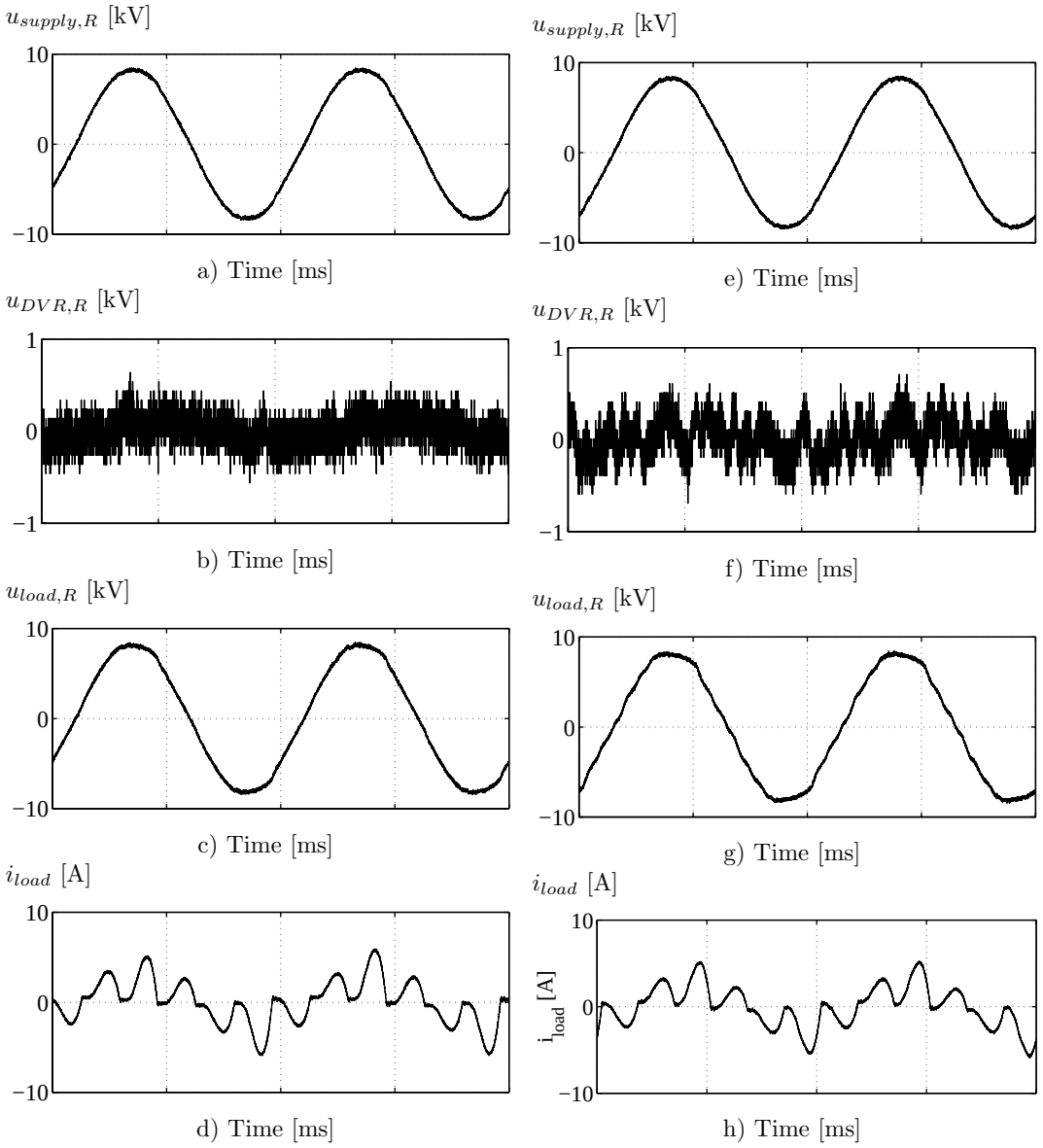


Figure 8.13: *Stationary measurements in the mechanical bypass mode a) - d) and in the standby mode e) - h). a) Supply voltage, b) DVR voltage, c) load voltage, d) load current, e) supply voltage, f) DVR voltage, g) load voltage and h) load current.*

8.3.3 Testing dynamic performance

Testing the dynamic performance of the DVR is carried out by generating voltage dips and record the DVR response. Symmetrical and non-symmetrical voltage dips have been tested under different load conditions.

Symmetrical voltage dip

A symmetrical short circuit with the neutral has been applied leading to a 0.74 pu and 130 ms voltage dip. The DVR response is illustrated in Fig. 8.14. The DVR protects a load consisting of the 400 kVA distribution transformer and a 45 kW resistive load.

Fig. 8.14a illustrates the currents of the 10 kV radial and Fig. 8.14b the supply voltages in front of the DVR, Fig. 8.14c the injected DVR voltages, Fig. 8.14d the restored load voltages and Fig. 8.14e the load currents measured at the HV-side. From these collected data, the voltage dip seems to be very effectively compensated at the load side. A zoomed view of the transition phase from standby to active mode is illustrated in Fig. 8.14f to be able to verify the dynamic performance and response-time of the DVR system. For clarity it only includes the supply and the load voltage for phase T from 20 - 60 ms. The voltages are almost equal before 37 ms and after the voltage dip the injected voltage can easily be seen. A further zoom of the transition phase is illustrated in Fig. 8.14g from 34 - 44 ms. An oscillation of the supply voltage is identified, which is transferred to the load voltage. The voltage dip is initiated at 36.5 ms and at 37.5 ms the load voltage starts to deviate from the supply voltage and at 37.7 ms the load voltage is restored, but with a low-damped second order oscillation and the response-time seems to be below 1.5 ms.

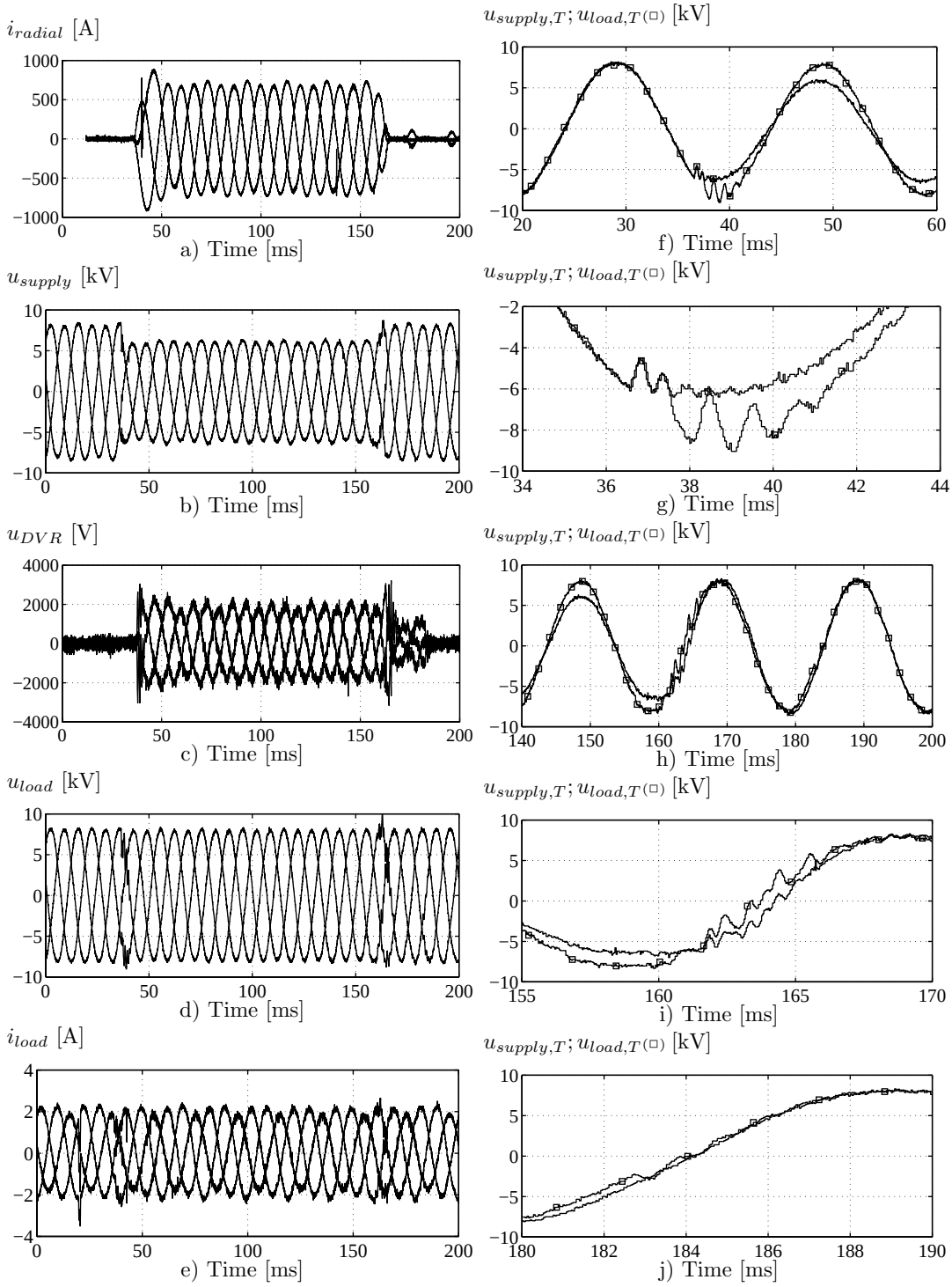


Figure 8.14: *Measured 0.74 pu symmetrical voltage dip. a) Radial currents (load current + short circuit current), b) supply voltages, c) injected DVR voltages, d) load voltages, e) load currents, f) transition from standby to active mode, g) zoomed view of the start transition, h) transition from active mode to standby mode, i) zoomed view of the return of the supply voltage, j) zoomed view of the transition from active to standby mode.*

The return of the supply voltage is illustrated in Fig. 8.14h in the period 140 - 200 ms and a zoomed view in Fig. 8.14i in the period 155 -170 ms. Oscillations occur both from the supply voltage and from the injected DVR voltage. In phase T no over-voltage is generated. The DVR is still in active mode and it is changing from active mode to standby mode at t = 182.5 ms, which is illustrated in Fig. 8.14j.

From the time domain plots in Fig. 8.14 the DVR response seems acceptable. A more thorough analysis has been performed in the frequency domain with an FFT analysis. The dip load voltage and supply voltage have been FFT analyzed in the time period 68 - 88 ms. The phase R voltage in percentage is illustrated in Fig. 8.15a and a zoomed view in 8.15b with the lower harmonics. The phase R voltage is restored to 98 % and the largest harmonic voltage component is the fifth harmonic with approximately 1 % content. The DVR seems to inject 0.5 % 100 Hz and 150 Hz components. The THD of the supply voltage and the load voltages are still only 2.6 % and 2.3 %, respectively, which is fully acceptable.

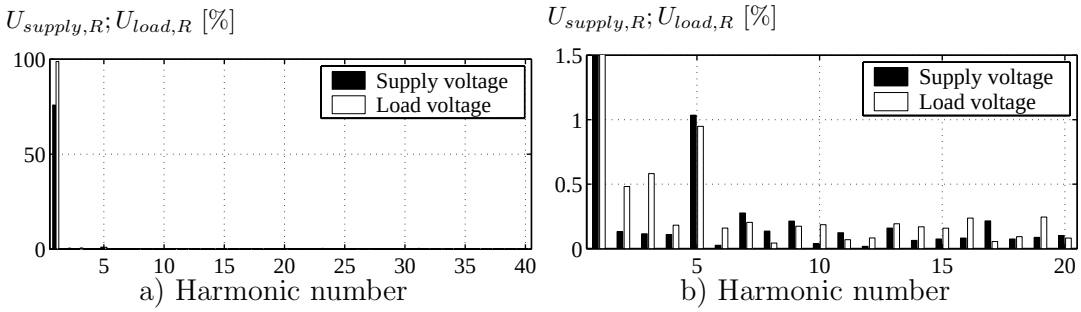


Figure 8.15: *FFT analysis of the during dip phase R RMS voltage in percentage of the rated supply voltage. a) 1. - 40. harmonic and b) Zoomed view of the lower harmonics 1. - 20. harmonic*

By analysis it can be calculated that the non-symmetry of the supply and load is 0.3 % and 1.0 %, respectively. The voltage dip can be characterized to 0.74 pu at the supply side and 0.98 pu at the load side. The DVR response is characterized as a very successfully voltage dip compensation.

Non-symmetrical voltage dips

Several non-symmetrical voltage dips have been tested. Two non-symmetrical voltage dips are here presented, which is a two-phase short circuit without neutral and a single-phase to neutral fault.

Two-phase fault A two-phase fault without ground has been applied, and the measured response is illustrated in Fig. 8.16. Fig. 8.16a illustrates the currents in the radial, Fig. 8.16b the supply voltages in front of the DVR, Fig. 8.16c the injected DVR voltages, Fig. 8.16d the load voltages and Fig. 8.16e the load currents.

The test developed to become a very interesting test, because at the time t = 100 ms an internal fault occurred in the shorting transformer, which by analysis is identified as a ground fault in the transformer. The 10 kV distribution network is inductor grounded and the stationary short circuit current to ground is very low. The DVR is controlled to only inject positive and negative sequence components, and thereby the DVR continues to compensate and protect the load from the voltage dip.

Phase T is chosen for a further study, and Fig. 8.16f illustrates the supply and load voltage drawn in the same plot from 0 - 200 ms. A zoomed view of the same plot from 50 - 90 ms is illustrated in Fig. 8.16g, which shows the transition phase from standby mode to active mode. Oscillations appear in the supply voltage and after a short time the DVR injects a voltage in phase T. The transition is further zoomed in Fig. 8.16h from 60 - 70 ms and oscillations in the supply voltage can be seen, which are transferred to the load side and approximately 2 ms after a reduction in the supply voltage the load voltage is compensated back to the rated supply voltage with oscillations in the DVR line-filter.

The ground fault at approximately t = 100 ms is illustrated for phase T in Fig. 8.16i from 96 - 110 ms. The ground initiated oscillations in the supply voltage and oscillations in the injected DVR voltage. Fig. 8.16j illustrates the return of the supply voltage, which also initiates oscillations.

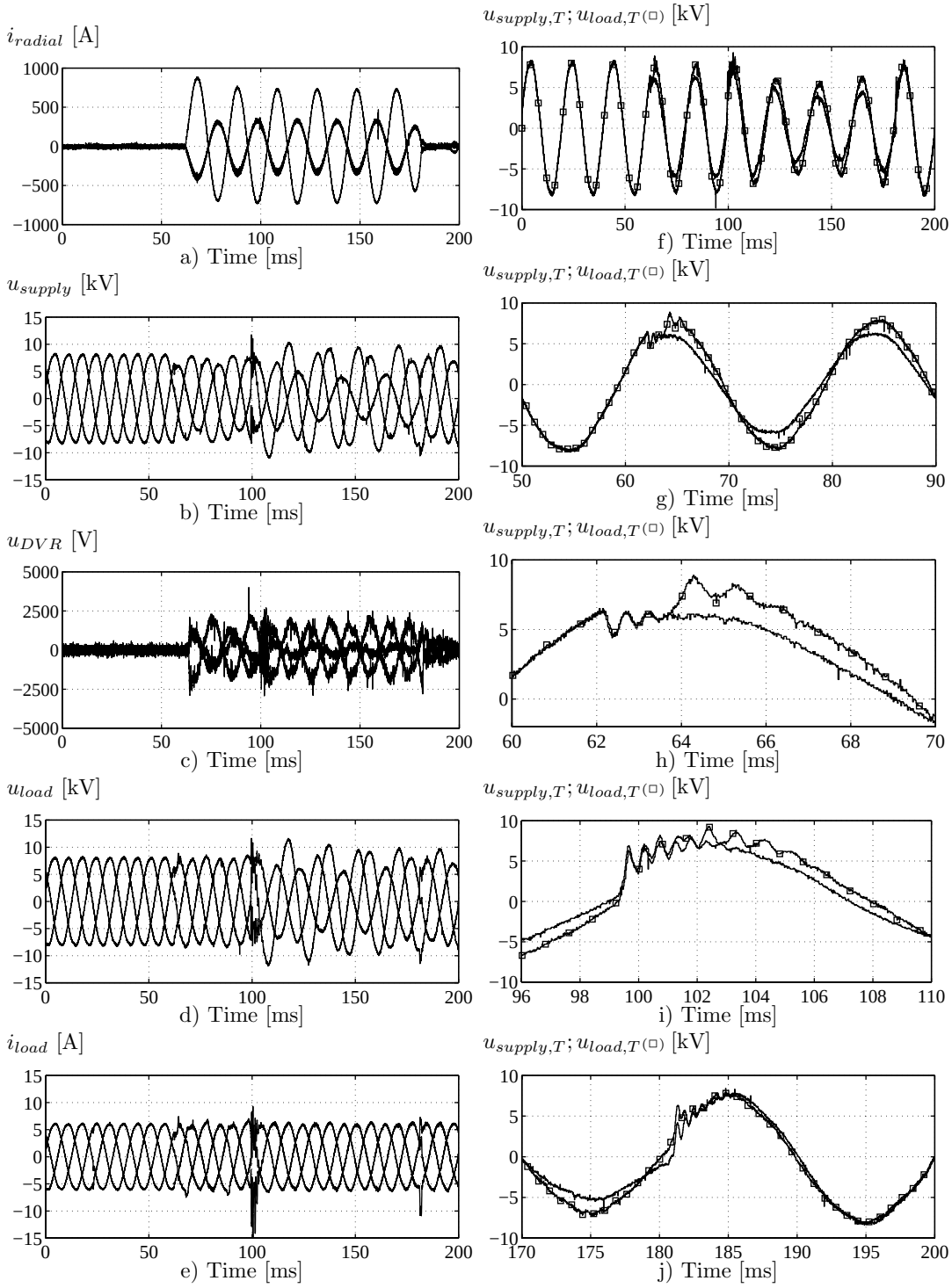


Figure 8.16: *Non-symmetrical voltage dip with a two-phase fault. a) Supply currents (load current + short circuit current), b) supply voltages, c) injected DVR voltages, d) load voltages, e) load currents, f) supply voltage and load voltage for phase T, g) transition from standby to active mode, h) zoomed view of the start transition, i) oscillation during the ground fault and j) transition from active mode to standby mode*

In the first phase of the voltage dip before the ground fault an FFT is made of the supply and load voltage in the period 75 - 95 ms (illustrated in Fig. 8.17a and 8.17b) and an FFT after the ground fault for the time period 135 - 155 ms (illustrated in Fig. 8.17f and 8.17g). Fig. 8.17c - e illustrate the positive, negative and zero sequence component before the ground fault and Fig. 8.17h - j after the ground fault. To generate the symmetrical components each phase value has been decomposed into harmonics, and all the phase components have been transformed to symmetrical components.

An analysis of the synchronous component in Fig. 8.17c and Fig. 8.17h illustrate an unchanged synchronous component before and after the ground fault. The synchronous component of the supply voltages are 0.88 pu, and the DVR restores the synchronous component of the load voltage to 0.98, which is fully acceptable.

The negative sequence components in Fig. 8.17d and Fig. 8.17i are also relatively unchanged before and after the ground fault, and the symmetry is reduced from 15 % to 4 % because of the DVR.

The zero sequence component in Fig. 8.17e and Fig. 8.17j increases from zero percent to approximately 30 % of the rated phase voltage. The ground fault in the transformer contains some fault impedance, otherwise the zero sequence component would be close to 100 %. The zero sequence component is not transferred to the LV loads, because of the delta/star distribution transformers.

By the analysis it can be seen that the DVR only injects positive and negative sequence components, and the zero sequence system is unchanged as expected. The voltage THD of phase R is at the supply side 3.7 % and 4.0 % at the load side. The visual and analytic results indicate an almost acceptable performance. Only a better performance in the reduction of the negative sequence component could be wanted.

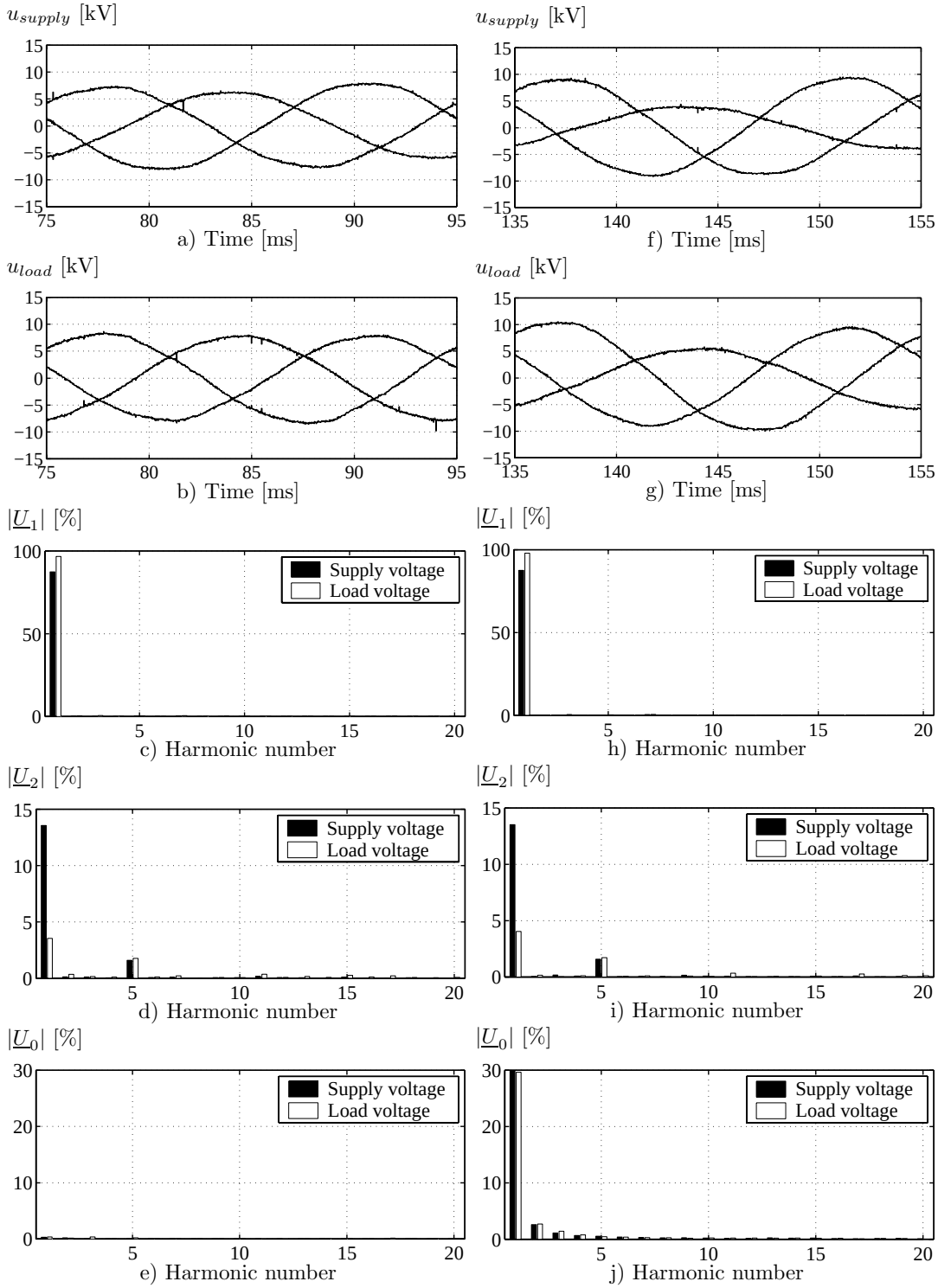


Figure 8.17: *FFT analysis of the during dip supply and load voltages before the ground fault (75 - 95 ms) a) - e) and after the ground fault (135 - 155 ms) f) - j).*
a) Supply voltages, b) load voltages, c) positive sequence, d) negative sequence, e) zero sequence, f) supply voltages, g) load voltage, h) positive sequence, i) negative sequence and j) zero sequence.

Single-phase fault A single-phase fault have been applied at the LV-side and Fig. 8.19 shows the system response. The load is a 99 kW resistive load.

Fig. 8.19a - e have been collected with oscilloscopes at 50 kS/s and it illustrates the radial currents in Fig. 8.19a, the supply voltages in Fig. 8.19b, the DVR voltages in Fig. 8.19c, the load voltages in Fig. 8.19d and the load currents in Fig. 8.19e.

Fig. 8.19f-j are collected by the DSP at a sample rate equal to the switching frequency, which is 3 kS/s. Notice the different time scales, because the DSP is triggered by the measured voltage dip and the oscilloscopes are triggered by the short circuit equipment. In Fig. 8.19f the decaying DC-link voltage is illustrated, which is drained during the compensation. Fig. 8.19g illustrates the measured supply voltages, in Fig. 8.19h the DVR voltages, in Fig. 8.19i the load voltages and in Fig. 8.19j the converter currents.

The load voltages and the supply voltages measured by the DSP have been FFT-decomposed and the result is shown in Fig. 8.18. An analysis of the single-phase fault indicate the synchronous component is increased from 0.92 pu to 0.98 pu. The negative sequence is reduced from 10 % to 2.7 % and the voltage THD of phase R is decreased from 2.8 % to 2.6 %.

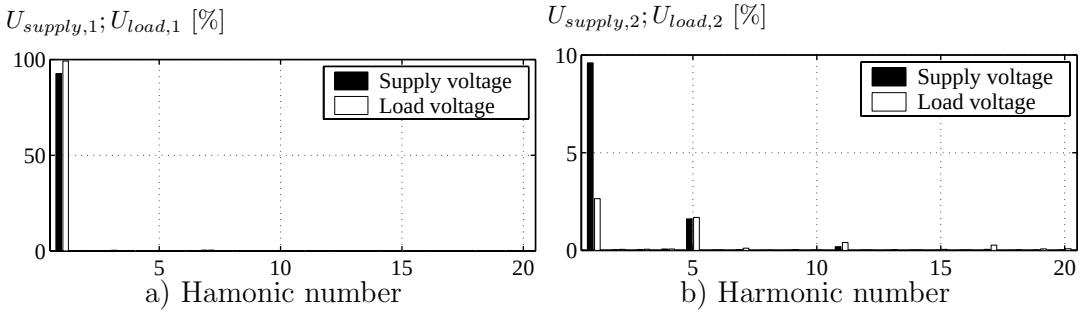


Figure 8.18: *FFT analysis of the during dip load voltages and supply voltages measured by the DSP during a single-phase fault. a) Positive sequence system and b) negative sequence system.*

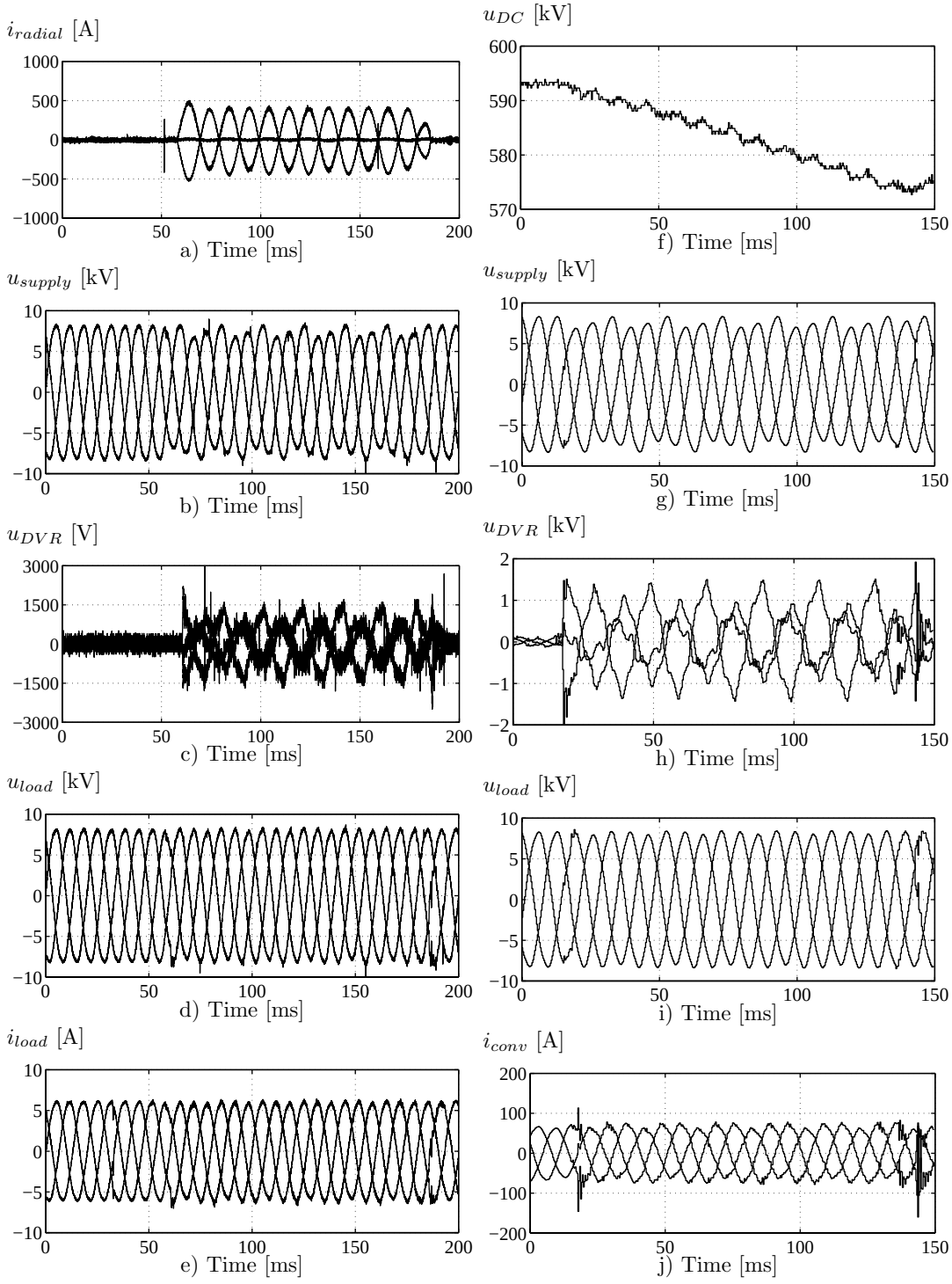


Figure 8.19: *Non-symmetrical voltage dip with a single-phase fault. a) - e) measured by the oscilloscopes and f) - j) by the DSP.*
a) Radial currents (load current + short circuit current), b) supply voltages, c) injected DVR voltages, d) load voltages, e) load currents, f) DC-link voltage, g) supply voltages, DVR voltages, i) load voltages and j) converter currents.

The control of the DVR is implemented in a rotating dq-reference frame and in Fig. 8.20 some of the main DVR control parameters are illustrated. In Fig. 8.20a the dq-supply voltages, in Fig. 8.20b the dq-DVR voltages, in Fig. 8.20c the dq-load voltages and in Fig. 8.20d the dq-reference DVR voltages. The voltage measurements contain a 300 Hz component, which originates from the 5. and 7. harmonic background distortion of the supply voltages.

Fig. 8.20e illustrates a zoomed view from 0 - 60 ms and Fig. 8.20f 0 - 30 ms of the supply and load voltages. The injection by the DVR stabilizes the load voltage and restores the DC-value from the positive sequence voltage component and dampens the 100 Hz component originating from the negative sequence component. The DVR does not manage to damp the 300 Hz component significantly.

The ability to track a reference voltage is illustrated in Fig. 8.20g and 8.20h. Fig. 8.20g illustrates the d-DVR reference voltage and actual d-DVR voltage and Fig. 8.20h is the q-reference voltage with actual q-DVR voltage.

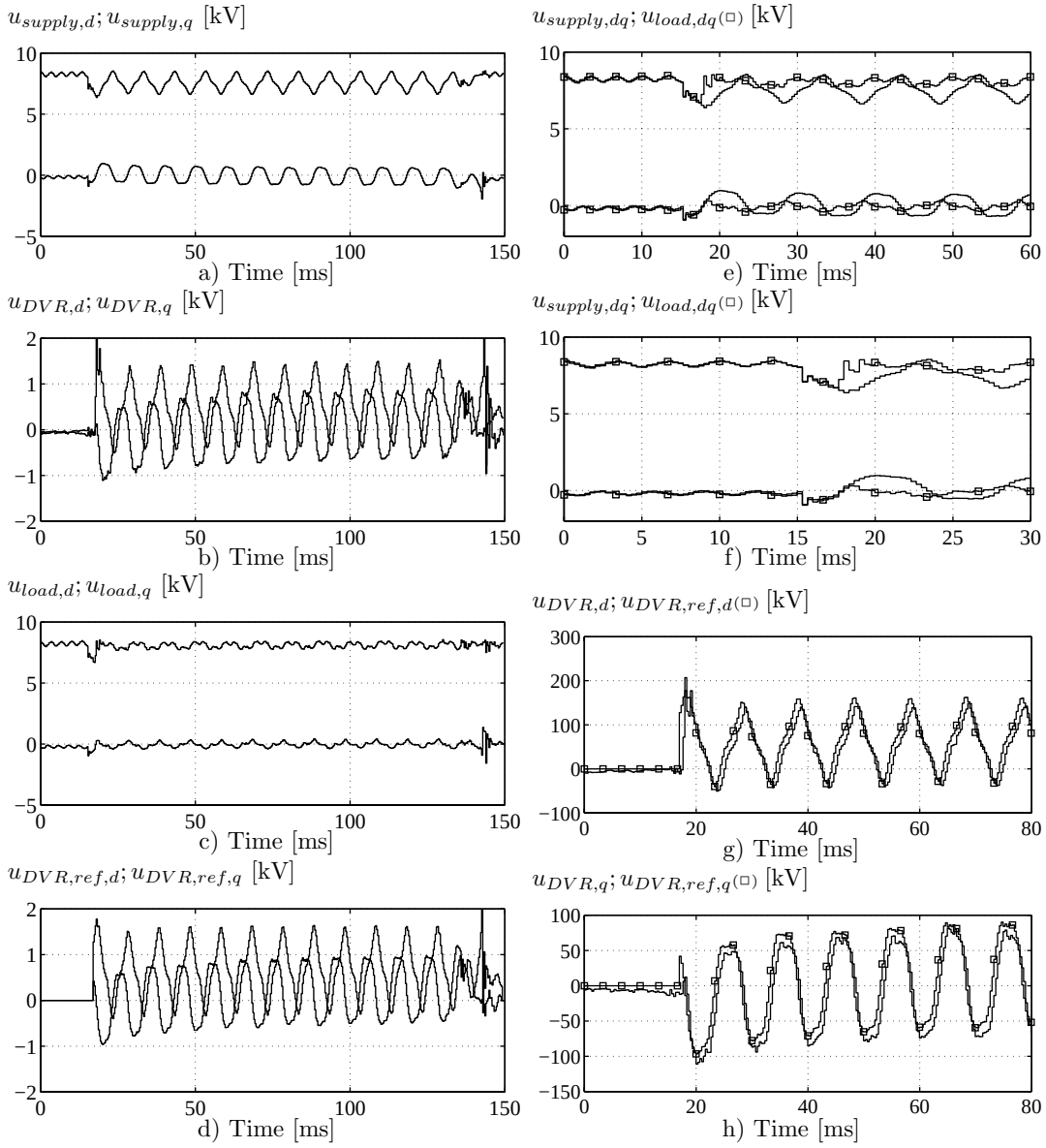


Figure 8.20: *Non-symmetrical voltage dip with a single-phase fault measured by the DSP controller in the dq-reference frame. a) supply voltages, b) DVR voltages, c) load voltages, d) reference voltages, e) supply and load voltages, f) zoom of supply and load voltages, g) d-component of the DVR reference and actual DVR voltage and h) q-component of the DVR reference and actual DVR voltage.*

Applying different loads

Different load conditions have been tested. Problems have again been encountered, when the DVR protects a non-linear load and the test results have been included.

Non-linear load The protection of a non-linear load during a voltage dip has been tested. The non-linear is a 45 kVA frequency converter described in Section 8.3.2, and the test results can be seen in Fig. 8.22. An analysis of the single-phase fault indicates that the synchronous component is increased from 0.92 pu in the supply voltages to 0.98 pu in the load voltages. The negative sequence is reduced from 10 % to 2.3 % and the voltage THD of phase R is increased from 3.3 % to 6.9 %.

A zoomed view of the response from 100 - 140 ms is illustrated in Fig. 8.22f - i, and these indicate some of the difficulties compensating a highly non-linear load. A non-linear load with a heavy current distortion initiates oscillations in the DVR filter and the load voltages are hence distorted. An FFT analysis of one phase voltage is illustrated in Fig. 8.21 during the fault in the time period 100 - 120 ms. The compensation has succeeded, but most harmonics have been amplified. The 21. and 23. harmonic have been heavily amplified, because the resonance frequency is close to this frequency. The third harmonic is also amplified, because the load voltages are less symmetrical and the harmonics multiplied by three will not be cancelled by each other.

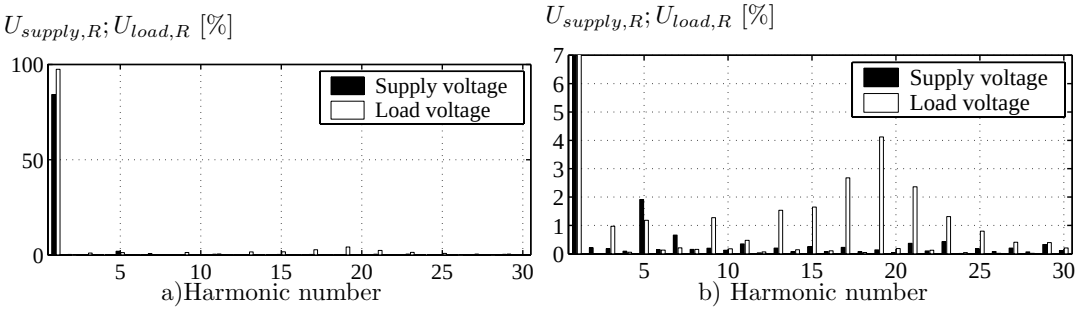


Figure 8.21: *FFT analysis of the phase R supply voltage and the phase R load voltage (100 - 120 ms). a) Phase R voltages and b) A zoomed view of the phase R voltages.*

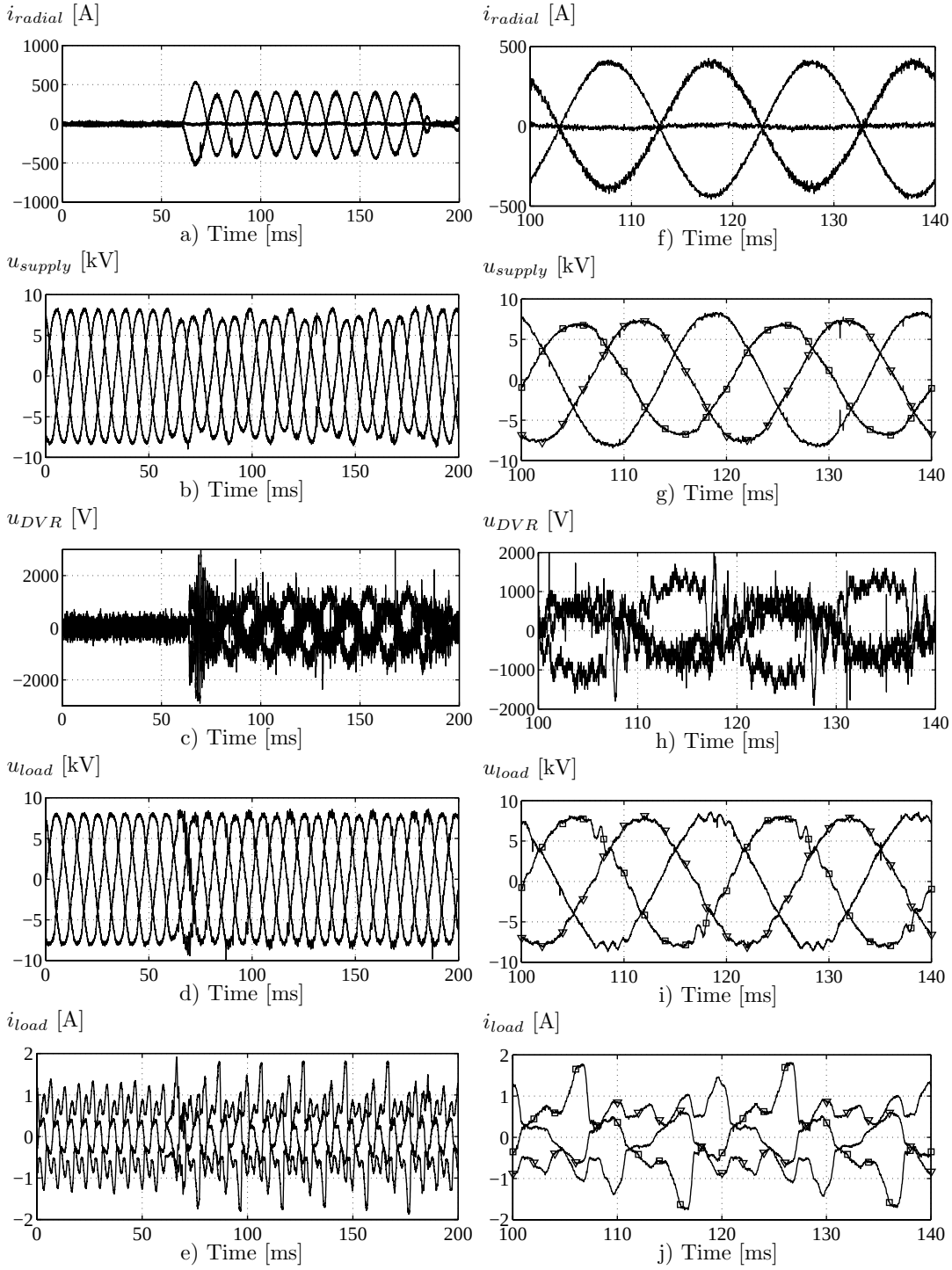


Figure 8.22: *Measured response during a non-symmetrical voltage dip with a single-phase short circuit protecting a non-linear load. a) - e) 0 - 200 ms and f) - j) zoomed view 100 - 140 ms.*
a) Radial currents (load current + short circuit current), b) supply voltages, c) injected DVR voltages, d) load voltages, e) load currents, f) radial currents, g) supply voltages, h) DVR voltages i) load voltages and j) load currents.

Testing the protection of the HV-DVR

The protection of the HV-DVR is not tested, but one faulted compensation is included to illustrate, what happen if the VSC in the DVR is turned off without ensuring a continuous current path. Fig. 8.23 illustrates an unsuccessfully compensation with a symmetrical three-phase fault.

A severe oscillation takes place in one of the injected DVR voltages, and the VSC was turned off due to over-current and a command to the bypass breaker was given. The oscillations stops, but the voltages across the DVR build up and are very non-linear, because of saturation in the injection transformers. At 136 ms the bypass breaker ensures a current path and the voltage across the DVR is close to zero. The DC-link is not charged to a higher voltage level, because the supply voltages are reduced due to the voltage dip and would only charge the DC-link to approximately 570 V. If the supply voltages were at rated voltage levels the DC-link could be charged to approximately 820 V, because $U_{DC} \simeq \sqrt{2} \cdot 10/\sqrt{3}$ kV.

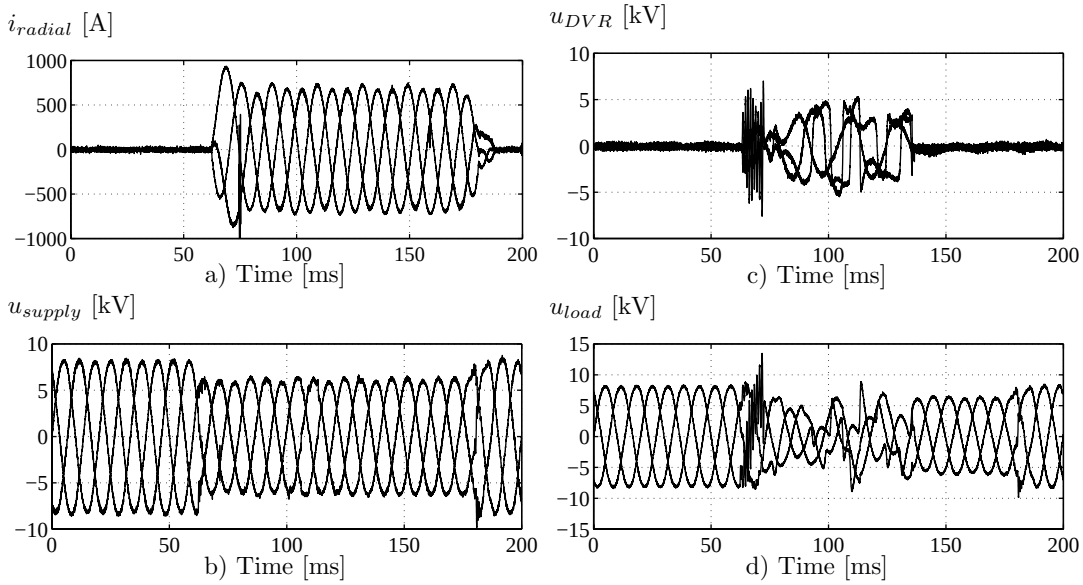


Figure 8.23: *Symmetrical voltage dip with an unsuccessful compensation recorded by the oscilloscopes. a) radial currents (load current + short circuit current), b) supply voltages, c) injected DVR voltages and d) load voltages.*

8.4 Summary and conclusion

The designed HV-DVR has been verified both with low power and high power tests.

- The high voltage - low power tests at Aalborg University indicated the dynamics and the control of the DVR at more severe voltage dips. Occasionally the rating of the programmable power supply limited the test possibilities and did not give a realistic view of the DVR performance during voltage dip compensation.

- The high voltage - high power tests at DEFU′s test facilities at Kyndby gave a very close picture of a real site application for the developed DVR. The method to generate voltage dip is partly realistic, which indicates a LV fault at the same 10 kV feeder as the sensitive load. It has not been possible to test for voltage dips, which originates from faults on the MV or HV levels.

- During the compensation of symmetrical voltage dips the performance of the DVR is very good with the exception of oscillations at the beginning and at the end of the voltage dip. The oscillations can be reduced by decreasing the bandwidth, which may lead to a larger voltage dip for the load to protect and a larger voltage surge, when the supply voltages are restored. The oscillations depend on the load to protect and at high rated loads the oscillations are less pronounced.

- Compensation of non-symmetrical voltage dips have been succeeded, and with the present control strategy the DVR damps the negative sequence component in the load voltage to less than 1/4 of the non-symmetrical content in the voltage dip. The positive sequence component is well compensated during non-symmetrical voltage dips.

- During the compensating of highly non-linear loads the DVR tends to distort the load voltages. The distortion of the load voltages takes place, because the DVR increases the impedance seen by the load and the non-linear currents initiate oscillations in the line-filter of the DVR. In one test the voltage THD was close to 7 % at the load side. As a consequence improvements in the DVR or in the control must be implemented in order to be able to compensate very non-linear loads. An active damping of the DVR′s oscillation frequency and the large harmonic voltage drop across the DVR could be applied to keep the voltage THD below e.g. 5 %.

- The control strategy does not give a significantly damping of background voltage harmonics and during voltage injection the DVR generate additional harmonics.

The performance of the DVR could be improved, but the control and DVR setup makes a great difference in the protection of sensitive loads against symmetrical and non-symmetrical voltage dips. The performance varies with the character of the load to protect.

Chapter 9

Conclusion

New power electronic solutions have gained increased interest to solve well known power quality problems. Voltage dips have been reported as a major power quality problem and a series connected converter, like the DVR, is considered to be an effective and cost-effective solution to mitigate voltage dips.

To gain a better understanding of voltage dip compensation with a dynamic voltage restorer in the distribution grid a number of aspects regarding the dynamic voltage restorer have been analyzed and tested in this thesis. The investigations range from the location and design of a DVR to a practical implementation and testing of a DVR located in a medium voltage 10 kV grid.

9.1 Summary of the thesis

This thesis is focused on one type of custom power device, which is referred to as a dynamic voltage restorer (DVR). The main characteristics of the device are that it is series connected to the supply, and it has the ability to inject a rather large voltage into the grid to compensate for voltage dips.

Power electronic controllers for voltage dip mitigation have been discussed and it is concluded that the series connected device is an effective apparatus to compensate voltage dips. To establish a basis for the design and control of a dynamic voltage restorer, the most relevant power quality issues for a DVR have been described with focus on the characteristics of voltage dips.

The basic elements in a DVR have been described in Chapter 2, and it is discussed where in the distribution grid a DVR should be located. It could be a high power rated DVR located at the medium voltage level for protecting a large load from voltage dips or it could be placed in the low voltage distribution grid and protect a single low power rated load.

The DVR is equipped with a hard switching voltage source converter (VSC), and two different methods have been considered to be able to inject a voltage in series with the supply voltage. Today, the used method is to connect the VSC via an injection transformer, which ensures an galvanic isolation and simplifies the converter topology. An alternative method is to connect the VSC without the injection transformer directly to the grid and have the converter float at the potentials of the supply voltages. Avoiding the transformer requires a more complex VSC hardware, but the performance is expected to be improved.

Regarding the converter topology for a DVR some of the main parameters have been specified and four different topologies have been compared. They include a half bridge converter topology with a yy transformer, a half bridge converter topology with a dy transformer, a full bridge converter topology with a yy transformer and a half bridge three level converter topology with a dy transformer. Based on the analyses the full bridge topology was chosen for its versatility, the three level voltage generation and the high effective switching frequency.

Different DVR system topologies have been purposed and theoretically investigated regarding methods to have active power access during voltage dips. It includes either an energy storage system or power taking from the grid. Two of the topologies uses stored energy operating with a constant DC-link voltage and a variable DC-link voltage, respectively. The two other topologies use the remaining supply voltages. In order to ensure active power to the series voltage injection, the DVR increases the supply currents with a shunt converter. It can either be placed at the supply side of the series converter or at the load side of the series converter. The four topologies have been compared on a number of parameters with strengths and weaknesses. It was concluded that the DVR with a passive shunt converter at the load side of the series converter was the "best" choice, despite a higher total rating of the converters. The second "best" topology is considered to be the DVR with stored energy and a constant DC-link voltage.

The protection of the DVR is extremely relevant for series connected devices in the grid. A short circuit at the load side of the DVR can lead to high short circuit currents, and if a current path is not ensured it may lead to an over-voltage in the system and an uncontrolled charging of the DC-link, which may damage the DVR. Breaking of the supply lines should also be detected in order not to disturb neighboring upstream loads.

The design parameters for a DVR have been discussed in Chapter 4 and a general design procedure has been described regarding the voltage, current and energy rating of the DVR. The design of the individual DVR elements has been discussed, but only a few parts of the DVR hardware equipment have actually been constructed by design, because existing VSC equipment have been used and only the injection transformers have been chosen by real design.

A three-phase 10 kVA low voltage DVR (LV-DVR) rated to protect a 20 kVA load from a 0.5 pu voltage dip has been designed and constructed, including the measurement system and control equipment to the DVR. The system has been used to gain experience with the DVR and test different voltage dips, load conditions and control strategies. From the experiences gained with the LV-DVR a high voltage DVR (HV-DVR) has been build to be inserted in a medium voltage 10 kV distribution system and the DVR has a power rating of 200 kVA and is rated to protect a 400 kVA load from a 0.5 pu voltage dip.

Control strategies for a DVR have been treated in Chapter 5. Three operation modes have been incorporated in the control, which include a bypass mode during converter over-current conditions, a standby mode during normal supply voltage conditions and an active mode during under-voltage/voltage dip compensation. The control strategy has also been discussed regarding methods to reduce the power

drained from the energy storage, the voltage quality and the DVR limitations.

On the basis of the control strategy analysis of a more specific control of the DVR has been considered concerning feedback or feedforward control of the three load voltages. It is found adequate to control the DVR in a rotating dq-reference frame. The control of the DC-link voltage can be handled differently and it is chosen to let an external converter control the DC-link voltage. A phase locked loop (PLL) is used to synchronize with the supply voltages and new voltage dip detection methods are described. Different modulation strategies have been presented, and a carrier based uni-polar switching scheme has been chosen for the full bridge converter topology.

In Chapter 6 the simulation of a DVR have been presented. First, a modelling of the system components have been done and implemented in the circuit simulation program Saber. Simulations have been widely used in the design, as well as the testing of different control methods and protection strategies. The models have been sufficient to evaluate the DVR performance regarding bandwidth, ability to reduce negative sequence components, prediction of load voltage distortion, performance during different load conditions and the line-filter oscillations. Saturation effects in the injection transformers have not been included, therefore large deviations can be found if the transformers are close to saturate. Simulation results are compared with measurements on the LV-DVR and HV-DVR to examine the validity of the models.

Chapter 7 contains a description of the LV-DVR control and some of the main test results performed with the LV-DVR. Stationary tests with linear and non-linear loads have been performed to identify how the insertion of a DVR influence the load. Increased distortion during non-linear load has been encountered caused by oscillations in the line-filter of the DVR. Dynamic test with symmetrical voltage dips indicated a fast dynamic performance and a response-time below 1 ms. With the programmable power supply it has been possible to test the DVR performance during a symmetrical voltage dip with a phase jump. Two control methods have been implemented and tested. The first method restores the load voltages and thereby avoids to impress a phase jump at the load. The second method smoothes away the phase jump and with time the DVR injects voltages in-phase with the supply voltages. The four analyzed system topologies have been tested experimental with the LV-DVR, which were compared theoretically in Chapter 3.

In Chapter 8 the HV-DVR control and testing are described. The first tests after the construction have been carried out at the high voltage test laboratory at Aalborg University. The test facilities gave the opportunity to make the basic tests at high voltage, but with low rated loads. After the tests in Aalborg the DVR was shipped to DEFU′s test facility at Kyndby in Sealand.

The generation of the voltage dips were generated by initiating a controlled short circuit at the low voltage side of a 630 kVA 10/0.4 kV transformer. The short circuit currents were measured to approximately 495 A at the high voltage side, which is equal to 12.3 kA at the low voltage side. A voltage dip at the high voltage side of 0.74 pu was achieved.

Stationary tests with different load conditions have been performed to verify the

operation of DVR, when the DVR was connected in a realistic grid location with a high load and a high short circuit level. No problems were encountered during the stationary tests.

The dynamic performance was first tested with a three-phase symmetrical short circuit and the DVR succeeded to protect the load from a 100 ms and 0.74 pu voltage dip. Some oscillations were generated by the DVR in the transition phases from standby mode to active mode, at the return of the supply voltages and during the transition from active mode to standby mode. A zoom of the DVR response indicated a response-time below 2 ms for the DVR to restore the load voltages and an THD analysis of the supply and load voltages indicated a small drop in the distortion of the load voltages.

Different non-symmetrical faults were also initiated to test the DVR performance during a non-symmetrical voltage dip. A two-phase fault was applied and the DVR succeeded to restore the voltage dip and by analysis the non-symmetry in the supply voltage was approximately 14 % and reduced to approximately 4 % at the load by the DVR. During the short circuit a ground fault was generated internally in the short circuited transformer and despite of a ground fault at the MV-level the DVR continued to inject positive and negative sequence components to protect the load from the still existing voltage dip. A voltage dip generated by a single-phase short circuit was also handled by the DVR and the negative sequence was reduced from 10 % in the supply voltages to 3 % in the load voltages. Protecting a non-linear load from a voltage dip was succeeded, but line-filter oscillations were identified during the active compensation and the voltage THD was measured to approximately 7 %.

One example of an unsuccessfully compensation was included to illustrate how the voltage across the DVR can increase significantly if the VSC current paths are interrupted. The DVR was only protected with a slow mechanical breaker and from the time the VSC was turned off until the mechanical bypass ensured a current path 60 ms elapsed. During this process the voltage across the DVR rose, but because of the DVR design the DC-link voltage remained unchanged.

9.2 Conclusion and new aspects

By the results presented in this thesis it is believed that all objectives of the research project have been fulfilled. The main conclusions and new contributions are identified as:

- The protection of series connected power electronics to the grid is a main disadvantage for DVRs. The protection issues have been analyzed and verified through simulations and experiences gained during the tests. A DVR with a high voltage injection ratio is easier to protect, because it limits potential short circuit currents and over-voltages in the DC-link.

- Regarding the system topology for a DVR four topologies have been compared through analysis and testing. It includes two topologies with stored energy and two methods, which uses the remaining supply voltages and increase the supply current to restorer the load voltages. The analysis, test and comparison of system topologies for DVRs have not previously been reported.

- Focus has been kept at one control strategy, which here is referred to as a voltage quality optimized control. The DVR restores the load voltages to the pre-voltage levels The load voltages are not phase shifted in order to reduce the power drain or because the voltage dip contains a phase jump.

- The control methods to compensate a phase jump is previously described. But in the thesis a method have been implemented and verified through simulations and measurements on voltage dips containing phase jumps. Two control methods have been presented, and the preferred solution completely compensates the phase jump and it avoids to impress a phase shift on the loads.

- A new voltage control method of the DVR has been proposed with a combination of feedforward and feedback control. The advantages are a fast control response combined with zero steady state error in the load voltages independent of the load current conditions.

- A new fast detection method of a voltage dip has been proposed, which can detect symmetrical, non-symmetrical voltage dips and voltage dips including a phase jump.

- Different DVR load conditions have not been reported in the previous literature, and the different response during light and heavy load conditions are identified. Problems have been identified regarding protection of non-linear loads. The oscillations in the line-filter can increase the voltage THD at the load side. Solutions have been proposed to reduce the line-filter oscillations.

- A new control strategy to avoid large in-rush currents to the injection transformers has been developed, implemented and tested. It gives the opportunity to reduce the iron in the injection transformers and maintain a high bandwidth, but at the expense of a higher distortion of the load voltages.

- The HV-DVR is designed as a series converter with a variable DC-link voltage, which is a very simple topology and the topology have not been reported used. The power circuit is simple and have only a 0.02 pu charging converter.
- The high-voltage/high-power tests of the DVR are unique and not previously reported in the literature. The generation of controlled short circuits is an efficient way to generate significant voltage dips in a 10 kV grid.
- The designed HV-DVR gave a good protection of the load against voltage dips. Symmetrical voltage dips are compensated with a response-time of less than 2 ms. Non-symmetrical voltage components in the voltage dips are reduced to approximately 1/4 at the load voltage side. The THD at the load voltage side is not significantly increased during the compensation of linear loads. The protection of non-linear loads initiates oscillations in the DVR line-filter and combined with the harmonic voltage drop across the DVR the THD of the load voltages are relatively high.

9.3 Future work

Several topics, worthwhile a more in-dept study, have not been pursued in this thesis. Interesting topics for the future research in DVRs include:

- Verification of the HV-DVR performance at a location with different types of voltage dips originated from faults at the transmission level and distribution level.
- Further investigation of DVR topologies including the direct connected DVR.
- Testing a number of different loads, such as thyristor loads, motor loads, active rectifier loads to verify the robustness of the loads to protect from voltage dips.
- Thoroughly design of the line-filter, to have an optimum damping of the switching harmonics generated by the VSC and to avoid the oscillations at non-linear load. Furthermore, oscillations at the beginning and at the end of the voltage dip are expected to be reduced by an appropriate filter design.
- Electrical noise emission from the VSC to neighboring upstream loads and downstream loads.
- Investigation of robustness towards transients and lightning over-voltages.
- Development of an integrated protection scheme for the DVR and actual testing of the protection at severe fault conditions. Investigation of interference with existing short circuit protection equipment.
- Improvements of the performance towards a reduction of the negative sequence component.
- Control improvements to reduce the line-filter oscillations, increase the bandwidth and reduce load over-voltages.
- Mapping of the power losses in the DVR and voltage drop caused by the DVR.
- Cost calculations compared to the value of the improved voltage quality.

9.4 The future use of DVRs

A series connected voltage controller like the DVR is expected to experience an increased attention in the future, because it can be an effective and relative inexpensive solution to stabilize the voltage compared to high power rated UPS systems.

The main obstacles for the series controller is the standby losses and the protection of the series equipment during faults. As power electronics continuously are improving, the losses by the insertion of series voltage regulator might be reduced as the ability to handle high currents during short circuits.

Series voltage controllers upto 0.20 pu voltage injection might have a greater potential than controllers up to 0.5 pu. The losses and equipment cost will be lower and the utilization of the equipment is expected to be higher.

A factor, which decreases the potential use of series voltage controllers is that voltage sensitive equipment in the future will be made more robust and tolerant towards voltage dips. This can be achieved by voltage tolerant power electronic controllers in the rectifier stage, increased energy storage inside the equipment and intelligent control of voltage variations by the equipment.

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Chapter A

Published Papers

ANALYSIS OF TOPOLOGIES FOR DYNAMIC VOLTAGE RESTORER

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Abstract

Voltage dips are generally recognized as a significant power quality problem, which causes damage to a variety of sensitive consumers. Different approaches exist to limit the costs caused by voltage dips and one interesting approach, which is considered here is to use voltage sourced converters connected in series with the supply system. This type of devices is often termed a Dynamic Voltage Restorer (DVR). The location of the considered DVR is at a feeder in the distribution system, which gives the electric utilities the possibility to deliver and offer an improved power quality to a certain group of customers. In this paper different topologies for a DVR are analyzed and described. This includes the location of the device, the type of converter to be used and the energy storage and flow of active power for different topologies. One topology for a DVR is further described and the DVR's ability to compensate for voltage dips are verified with experimental tests. The experimental DVR is rated to give full protection to a 20 kVA load from voltage dips up to 50 %. A control strategy for the DVR is shortly discussed and finally the DVR prototype is described and used to verify the operation principle of a DVR.

Keywords— **Dynamic Voltage Restorer, DVR, Voltage Source Converters, Voltage Dips, Voltage Quality, Custom Power Systems.**

I. Introduction

Power Quality is a topic gaining increasing interest caused by different trends. Automated production plants and other industries require a high power quality to ensure an effective and uniform production. The integration of renewable energy systems and decentralized production plants complicate also the delivery of a uniform power quality to the customers. Finally, the deregulation of the electrical sector has lead to the possibility to differentiate the power quality and therefore deliver value added power to certain customers. The power converters available today are relative new and they are a power full tool to customize the power and deliver the Power Quality asked for.
General power quality issues have been treated in [2] and the origin and character of voltage dips have been studied intensively in [1]. Dynamic Voltage Restorer have been treated in several papers, commercial use is still rather seldom, but tests have been reported in [4], [6] and [3]. Different topologies for DVR's have been used, but the topology aspect have not been treated separately. The topology is highly relevant to achieve a good overall performance and some considerations are particular important for a DVR application. In this paper some major topology constraints are treated. First the location of a DVR is shortly discussed, followed by converter type considerations and finally how power can be sourced to the DVR during a voltage dip. In the last section experimental test are presented followed up with a conclusion.

II. Topologies for a DVR

The basic elements in a dynamic voltage restorer is illustrated in figure 1, with a DVR in series with the supply and load.

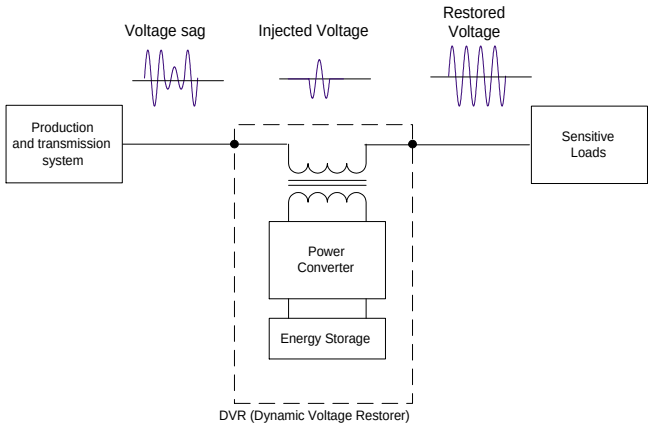

Fig. 1. Series connected dynamic Voltage Restorer

A. Location of a DVR

The intention is only to protect one consumer or a group of consumers with value added power. Applying a DVR in the medium or low voltage distribution system would often be possible and a radial grid structure is the only type of system considered here. In Europe three wire systems are common in the medium voltage systems, as illustrated in figure 2.b and four wire in low voltage systems (figure 2.a). In both systems the main purpose is to inject a synchronous voltages during symmetrical faults and in some cases inject an inverse voltage component during non symmetrical faults.

A main difference between a Low Voltage (LV) connection and a Medium Voltage (MV) connection is the flow of zero sequence currents and the generation of zero sequence voltages. In the four wire system the DVR must secure a low impedance for zero sequence currents and the zero sequence must either flow in the power converter or in a delta winding of the injection transformer.

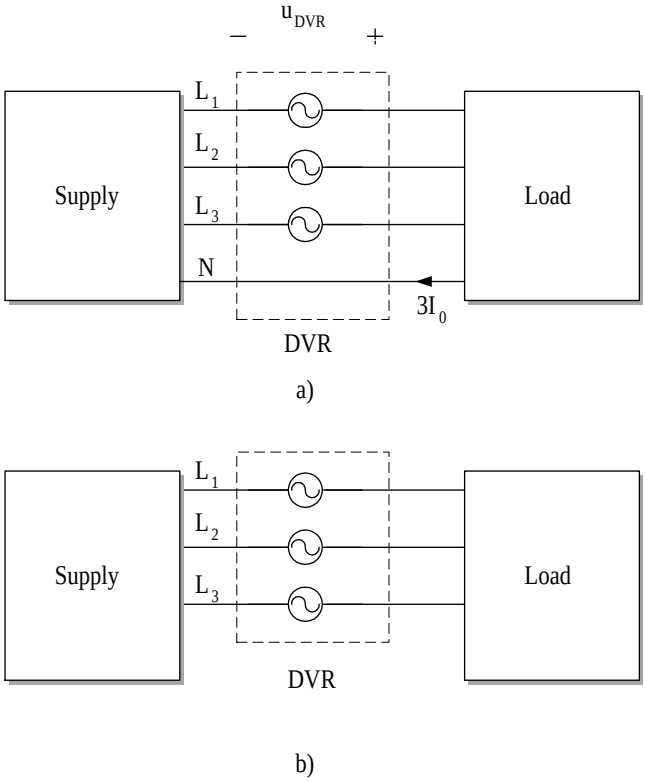

Fig. 2. Two typical locations of a DVR, a) Low voltage four wire system. b) Medium voltage three wire system.

B. Converter Type

Pulse width modulated Voltage Sourced Converters (VSC) are the commonly used converters for this type of application and it is the only type considered here. Applying a VSC to compensate for a missing voltage requires a boost inductance (L) and a line filter to damp the generated switching harmonics, as shown in figure 3.

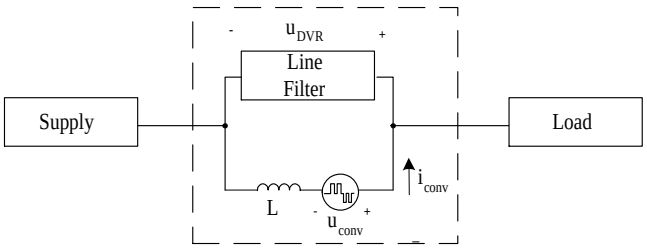

Fig. 3. DVR VSC converter with line filter

The boost inductance reduces the ripple current in the converter and hence the necessary line filtering. Shunt connected VSC have typically 10 - 20 % boost inductance to reduce the current ripple generation. For a DVR, this size would give a considerably voltage drop across the DVR, if the converter voltage is zero for instance during standby operation.
Additionally losses should be minimized, because the DVR conducts the load current continuously and a fast response is important to avoid a deterioration of the load voltage. The critical factors, when choosing a converter for a DVR application are:

- Switching frequency.
  – Generation of switching harmonics.
  – Ripple current in the converter.
  – Power losses caused by the switching and conduction.
- Dynamic response.
- DVR impedance.

The different factors interact and an optimum may depend on the site specifications. Generally, a small boost inductance is important to minimize the total DVR impedance, thereby the voltage drop across the DVR. Nevertheless, the converter needs an inductance to reduce the current ripple in the converter. High switching frequencies above 5 kHz are unwanted for high power applications. Choosing a more complicated converter topology can help achieve a low DVR impedance, low current ripple and low switching frequency, but the penalty is higher cost and complexity. As an example using a three level converter (figure 4.b) instead of a two level (figure 4.a) converter can with the same current ripple and switching frequency operate with a lower boost inductance. Several multilevel topologies exist, which are further described in [5].

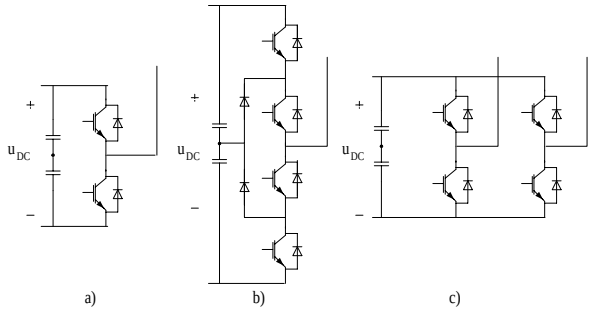

Fig. 4. Different types of series converters for a DVR, a) two level (half bridge)), b) three level (half bridge), c) three level. (full bridge)

In general useful topologies are those where active power easily can be transferred from a simple DC voltage circuit to the DVR converter. A full bridge converter as illustrated in figure 4.c is also a good choice for DVR converters, by unipolar switching the first switching harmonics appear at twice the switching frequency. An advantage of this topology is that with a given switch (U_{max},I_{max}) the rating can be doubled compared with a the two level topology.

C. Energy Source

Compensating effective for large voltage reductions requires active power, either from a storage system, the grid itself or from an auxiliary supply. The solutions can be summarized to:

- Energy storage (figure 5.a)
- Auxiliary supply (figure 5.b)
- Line connected shunt converter
  – Front connected (figure 5.c)
  – Back connected (figure 5.d)

The different solutions are illustrated in figure 5.

Operating with an energy storage gives limitations in the performance to compensate for long duration dips and a large energy storage is still rather costly, therefore most of the proposed DVR solutions have

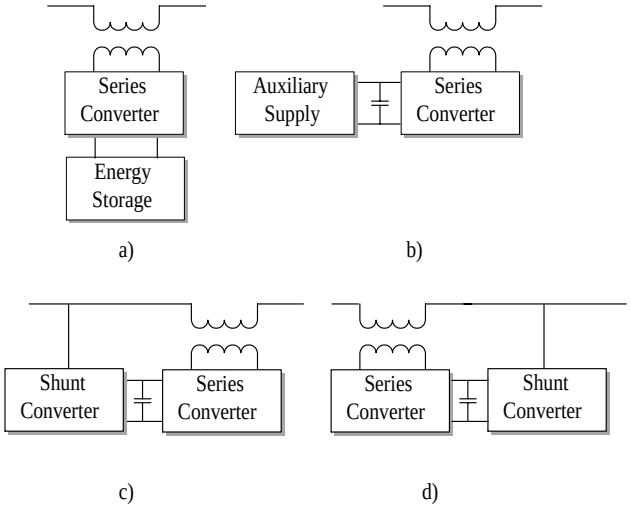

Fig. 5. Different types of connections to source power to the DVR. a) Energy storage, b) auxiliary supply, c) front connected shunt converter and d) back connected shunt converter

been realized with a shunt converter from the line itself or an auxiliary supply. In [7] the front connected shunt converter have been proposed and the main advantage with this solution is that the shunt converter has a restored "clean" voltage to enable a stable charging to the the common DC link. A drawback with the back connected shunt converter is the requirement of a higher current rating of the series converter.

The current rating of the DVR is critical. It should be scaled according to the existing load and a future load increase. If the load consists of large loads with transient currents, the DVR must be rated to handle these higher currents or somehow bypass the current. During a voltage dip, the voltage applied to the transformer changes abruptly and the transformer is magnetized according to the dip size. A transient DC-current can be detected and saturation effects in the transformer can even increase the inrush current. The DVR converter has to supply the inrush current and must be rated to supply this current.

III. Experimental Results

A small scale prototype DVR has been implemented for verification of the DVR operation principles. The system and control setup are briefly described and obtained results are shown.

A. System Description

One type of DVR is chosen for further analysis and the main purpose is to illustrate the operation of one DVR topology.

The prototype is rated to protect a 20 kVA load from a 50 % voltage dip. The converter switches directly into the transformer, which gives a good utilization in the leakage inductance of the transformer. Additionally, it minimizes the voltage drop across the DVR during standby operation.

The converter is based on three full-bridge Voltage Source Converters with a common DC-link as shown in figure 4.c. The power is fed into the DC-link by an auxiliary AC Supply and rectified in a passive diode bridge. Each injection transformer for the DVR are magnetically decoupled to have maximum test possibilities.

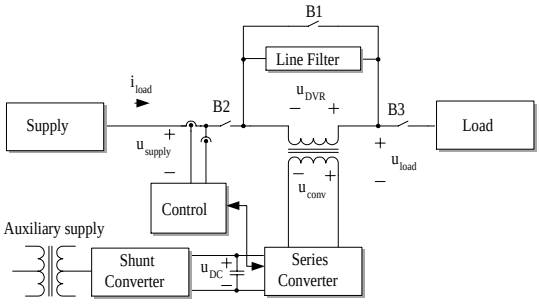

Fig. 6. Prototype DVR in the laboratory.

B. Control System

A control system is implemented in software for control and protection of the DVR. The DVR is controlled in four different operating states, which are:

- Active; the DVR generates a voltage to compensate for a voltage dip.
- Standby; normal voltage within certain margins are detected and the DVR voltage is zero and controlled to minimize switching losses
- Bypassed; the current is to high for the DVR converter to conduct and an alternative current path has been secured until the current has decreased to a level, which can be handled by the DVR. Voltage dips can not be compensated in this operating state.
- Disconnected; the DVR is fully disconnected for instance during service.

Other operating states could be added, for instance:

- Standby with voltage drop compensation
- Flicker reduction mode
- Background harmonic blocking mode

These additional tasks for a DVR could be attractive in certain cases.
To detect a voltage dip, the voltage is continuously measured and a Phase Locked Loop is implemented to detect the phase and angular position of the three phased supply voltage. The control structure for these tests are relative simple and illustrated in figure 7.

A voltage dip is detected, measuring the supply space voltage vector according to:

$$\underline{u}_{supply} = u_R + u_S e^{j\frac{2\pi}{3}} + u_T e^{j\frac{4\pi}{3}} = u_a + ju_b \quad (1)$$

A rotating dq-frame is used to control the amplitude of the DVR, as shown in:

$$u_d + ju_q = (u_a + ju_b)e^{-j\phi} \quad (2)$$

If the magnitude of the d-component differs from nominal supply voltage - 10 %, the DVR generates a

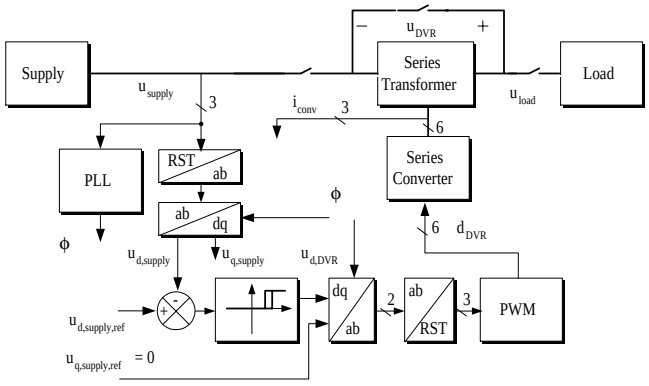

Fig. 7. Control system to compensate for voltage dips implemented in the DVR.

voltage to compensate for the missing voltage. Voltage surges are not compensated, basically because the used DC-charger only operates in one quadrant. An open loop control may not give optimal performance regarding the dynamics and steady state errors can occur. On the other side, the control is stable and simple for a first control approach. Phase jumps in the supply voltage are not compensated with this type of control.

C. Measured Performance

The performance during a 40 % voltage dip is recorded and illustrated in figure 8. The voltage dip is symmetrical, without phase jump and the RMS phase voltage drops from 230 V to 160 V. The duration of the voltage dip is 100 ms or five 50 Hz cycles and the load is a light resistive load ($R_{load} = 80\ \Omega$, $P_{load} = 2$ kW).

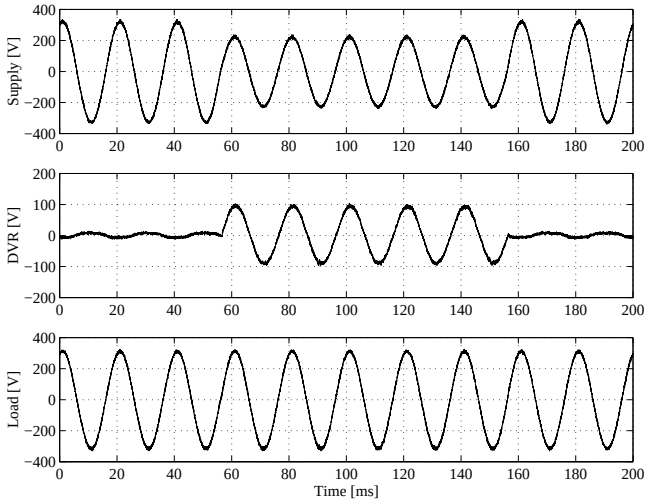

Fig. 8. Measured response during a 40 % voltage dip from 230 V to 160 V phase voltages. a) Supply voltage, b) DVR voltage and c) load voltage.

The associated converter current and load current are illustrated in figure 9.

D. System Evaluation

The performance during a symmetrical voltage dip is relative good. The response is fast, but with some overshoot, which could be reduced with a closed loop control.

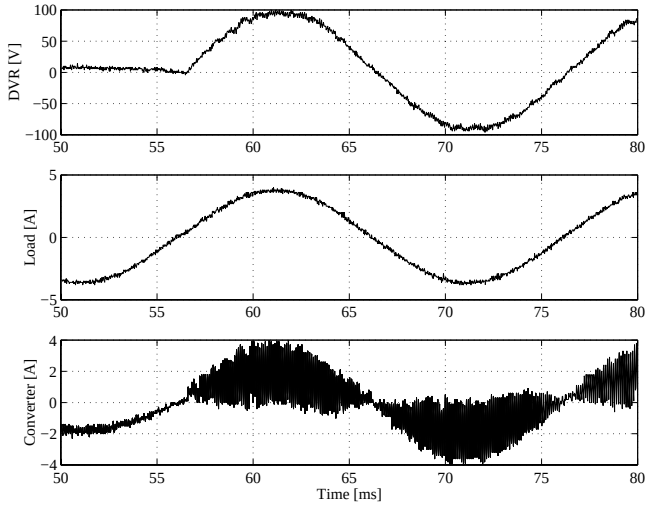

Fig. 9. Measured response during a 40 % voltage dip from 230 V to 160 V phase voltages. a) DVR voltage, b) load current and c) converter current.

IV. Conclusion

The DVR is generally considered as an effective device to compensate sensitive loads from externally disturbances. Voltage dip is a significant disturbance, which may lead to tripping and high cost to sensitive customers. In this paper topologies for a dynamic Voltage Restorer are discussed. A prototype has been build to verify the operation of the full bridge topology with auxiliary supply to feed power to the DC-link. Good results and performance have been achieved with the control and hardware. More tests and analytically work of different topologies could mature and improve the knowledge of the DVR technology.

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Control Strategies for Dynamic Voltage Restorer Compensating Voltage Sags with Phase Jump

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Abstract— **Voltage sags are an important power quality problem and the dynamic voltage restorer is known as an effective device to mitigate voltage sags. In this paper different control strategies for dynamic voltage restorer are analyzed with emphasis put on the compensation of voltage sags with phase jump. Voltage sags accompanied by a phase jump are in some cases more likely to trip loads and a satisfactory voltage compensation are more difficult to achieve. Different control methods to compensate voltage sags with phase jump are here proposed and compared. Two promising control methods are tested with simulations carried out in Saber and finally tested on a 10 kVA rated Dynamic Voltage Restorer in the laboratory. Both methods can be used to reduce load voltage disturbances caused by voltage sags with phase jump. One method completely compensates the phase jump, which is the best solution for very sensitive loads. The second method does only partly compensate the phase jump, but it is expected to have a better performance in compensating a broader range of voltage sags.**

I. Introduction

Significant deviations from the nominal voltage are a problem for sensitive consumers in the grid system. Interruptions are generally considered to be the worst case with the load disconnected from the supply. The number of interruptions, though expensive, can be minimized with parallel feeders and are less likely to occur with the transition from overhead lines to cables in the LV and MV distribution system.

Voltage Sags are characterized by a reduction in voltage, but the load is still connected to the supply. Sags are in most cases considered less critical compared to interruptions, but they typically occur more frequently. Voltage sags have in several cases been reported as a threat to sensitive equipment and have resulted in shutdowns, loss of production and a hence a major cost burden. The theory of voltage sags and interruptions is thoroughly described in [1].

Sags are so far almost impossible to avoid, because of the finite clearing time of the faults causing the voltage sags and the wide propagation of sags from the transmission and distribution system to the low voltage loads. Equipment can be made more tolerant of sags either via more intelligent control of the equipment or by storing more energy in each equipment. Instead of modifying each component in for instance a factory to be very tolerant to voltage sags, a better solution might be to install one dynamic voltage restorer to mitigate voltage sags. A DVR can eliminate most sags and minimize the risk of load tripping at very deep sags.

The control of a DVR is not straight-forward because of the requirements of fast response, large variation in the type of sags to be compensated and variation in the type of connected load. The DVR must also be able to distinguish between background power quality problems and the voltage sags to be compensated. Sags are often non-symmetrical and accompanied by a phase jump. Control strategies for DVR's have been addressed in [3] and [7]. In [5] the problems with phase jump have been reported but no control methods have been proposed. This paper shortly describes voltage sags with a phase jump and illustrate different control strategies for a DVR and some DVR limitations, which should be included in the control strategy. Two control methods are proposed with the ability to protect the load from a sudden phase shift caused by a voltage sag with phase jump. Finally, the major parts in the experimental setup are described with the DVR hardware and control system used. Simulations and measurements illustrate how symmetrical voltage sags with phase jump successfully can be compensated.

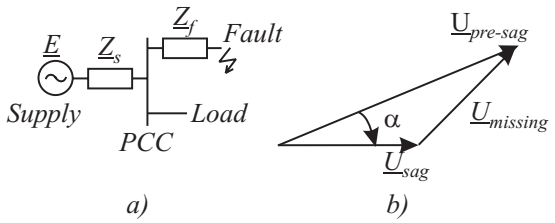

Fig. 1. Voltage sag with phase jump. a) Simplified circuit to calculate the voltage reduction and phase jump. b) Vector diagram of voltage sag with the used definition of pre-sag voltage, sag voltage and missing voltage.

II. Voltage sags with phase jump

Voltage sags are caused by a short circuit current flowing into a fault, which is shown in Fig. 1a. Magnitude and phase of the voltage, $\underline{U}_{sag}$ during the sag, at the Point of Common Coupling(PCC), are determined by the fault and source impedances, using the following simplified equation:

$$\underline{U}_{sag} = \underline{E}\frac{\underline{Z}_f}{\underline{Z}_f + \underline{Z}_s} \tag{1}$$

A fault current somewhere in the grid can lead to a reduced magnitude and, in some cases, a phase jump of the voltage at the point of common coupling. Fig. 1b. defines the used definitions of the voltage at the PCC. $\underline{U}_{sag}$ is the voltage during the sag and α is the phase jump at PCC.

The Dynamic voltage restorer injects a voltage in series with the supply to compensate for voltage sags. The principle operation of a DVR is illustrated in Fig. 2.

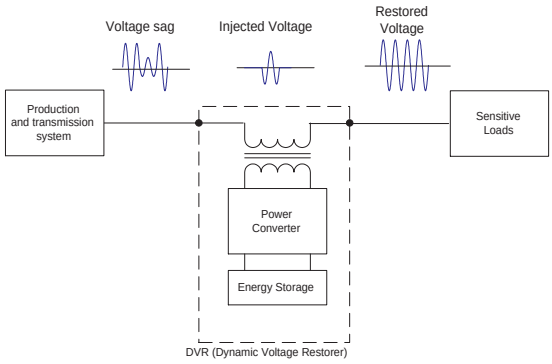

Fig. 2. Principle operation of the Dynamic Voltage Restorer.

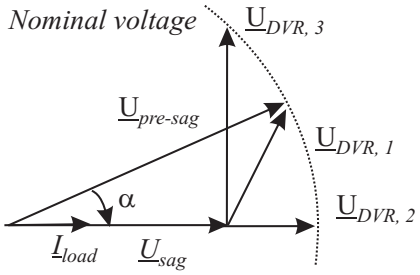

Fig. 3. Control strategies for the DVR. $\underline{U}_{DVR,1}$ the pre-sag compensation, $\underline{U}_{DVR,2}$ the in-phase compensation and $\underline{U}_{DVR,3}$ the energy optimal control

III. Control strategy

The possibility of compensation of voltage sags can be limited by a number of factors including finite DVR power rating, different load conditions, background power quality problems and different types of sags. If the DVR should be a successful device, the control may be able to handle most sags and the performance must be maximized according to the equipment inserted. Otherwise, the DVR may not be able to avoid load tripping and even cause additional disturbances to the load.

A control strategy for voltage sags with phase jump should be included, to be able to compensate this particular type of sag. The control strategy can depend on the type of load connected. Some loads are very sensitive to phase jump and the load should be protected from them. Other type of loads are more tolerant to phase jump and the main task is to maintain the nominal voltage on all three phases. Three basic control strategies for a DVR can be stated as:

- Method 1: Pre-sag compensation; The supply voltage is continuously tracked and the load voltage is compensated to the pre-sag condition. The method gives a nearly undisturbed load voltage, but can often exhaust the rating of the DVR.
- Method 2: In-phase compensation; The generated DVR voltage is always in phase with the measured supply voltage regardless of the load current and the pre-sag voltage.
- Method 3: Energy optimal compensation; To fully utilize the energy storage, information about the load current is used to minimize the depletion of the energy storage.

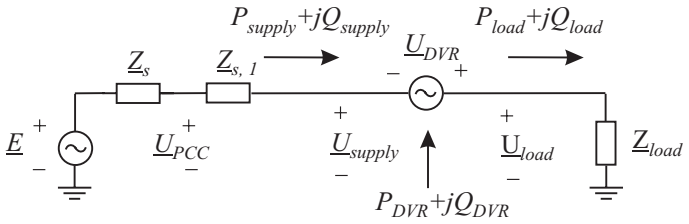

Fig. 4. The flow of active and reactive power with a DVR inserted.

The discussed three methods are illustrated in Fig. 3 and by studying Fig. 3 it appears like the energy storage can be reduced applying the DVR voltage perpendicular to the load current, but the current will change phase according to the new load voltage applied to it and energy will be drawn from the DVR. Fig. 4 illustrates how the power flows in the system. The voltage generated which is perpendicular to the load current can be used to bring the current in-phase with the supply voltage or make the DVR and load appear as a capacitive load. A capacitive load current tends to raise the supply voltage $\underline{U}_{supply}$ and by raising the supply voltage more power can be taken from the grid and hence saved from the energy storage.

Before selecting a control method to be used further issues have to be addressed, which are closely linked to the chosen control strategy. A DVR has limited capabilities and the DVR will most likely face a sag outside the range of full compensation. Three important limitations for a DVR are:

- Voltage limit; The design of the DVR is limited in the injection capability to keep the cost down and reduce the voltage drop across the device in normal operation.
- Power limit; Power is stored in the DC-link, but the bulk power is often converted from the supply itself or from a larger DC storage. An additional converter is used to maintain a constant DC-link voltage and the rating of the converter introduces a power limit to the DVR.
- Energy limit; Energy is used to maintain the load voltage fixed and it is normally sized as low as possible in order to reduce cost. Some sags will deplete the storage fast and the control can reduce the risk of load tripping caused be insufficient energy storage.

All the limits should be included in the control to fully utilize the investment of a DVR. Fig. 5 illustrates a single phase phasor diagram for one load case. The phasor of the pre-sag voltage is shown with a lagging load current. The phase jump is negative with a reduced during-sag voltage.

The voltage and power limits are indicated and the hatched region illustrates the region within the DVR can operate. The pre-sag voltage cannot be maintained in the case illustrated in Fig. 5. In-phase control to nominal voltage is also not obtainable if the current phasor stays, because of the power limit.

A phase jump could be initiated by certain voltage sags with phase jump, or by the DVR itself to reduce the power drain or maximize the load voltage at severe sags. In both cases a phase jump may be undesirable for the load and may initiate transient currents in capacitors, transformers, motors etc. The operation of line commutated converters

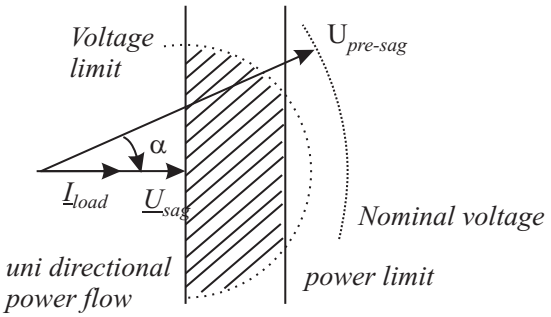

Fig. 5. A deep voltage sag with a phase jump. The hatched region indicates the region the DVR can operate.

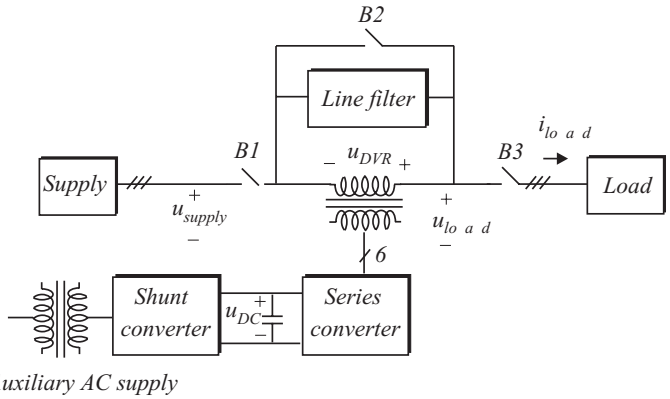

Fig. 6. Prototype DVR in the laboratory including a three phase supply and load

may also be disturbed by a sudden change in the phasor of the load voltage. Because of the potential problems with a phase shift at the load, the control of a DVR is tested, emphasis is put on the voltage sags with phase jump and how to avoid the phase shift to propagate to the load.

Two methods are tested, which could protect phase shift sensitive loads from phase jumps. They are here characterized as:

- In-phase compensation with a smooth compensation of the phase jump.
- Pre-sag compensation.

The first method continually tracks the supply voltage and information about the pre-sag condition is initially used, but it changes slowly to inject a voltage in phase with the new supply voltage. The second method uses the pre-sag condition and in the ideal case the load voltage is undisturbed by the voltage sag.

IV. DVR test system

To test and verify the control of the DVR a prototype has been built in the laboratory.

A. Hardware

In the laboratory the DVR converter is based on three full-bridge Voltage Source Converters with a common DC-link. Fig. 6 illustrates the DVR setup.

The power needed, when injecting a voltage in phase with the load current is usually taken from an energy storage or from the grid itself. The different topologies for DVR's are treated in [6]. In this setup the DVR is powered by an auxiliary AC Supply and the AC is rectified by a passive diode bridge and fed in to the DC-link. The setup correspond to a system with energy storage and a constant DC-link voltage. During a voltage sag the DC-link voltage is only slightly reduced because of the active power drawn by the series converter.

Each injection transformer for the DVR are magnetically decoupled in order to have the maximum test possibilities. To minimize the voltage drop across the DVR and to take the full advantage of the leakage inductance in the transformer, the converter switches directly into the transformer also used in [2]. The line filter sinks the main part of the switching harmonics.

Calculations for the control is carried out in a Digital Signal Processor (DSP) and the switchings are performed by a Micro Controller (MC). The main hardware parameters for the DVR are listed in Table I.

TABLE I
Main system parameters for the experimental DVR setup.

Description	Rated value	Per unit value
Load rating	20 kVA	1 pu
DVR rating	10 kVA	0.5 pu
Load voltage	230 V	1 pu
DVR voltage	0 - 115 V	0 - 0.5 pu
DC-link voltage	560 V	
Supply frequency	50 Hz	1 pu
Switching frequency	5 kHz	100 pu

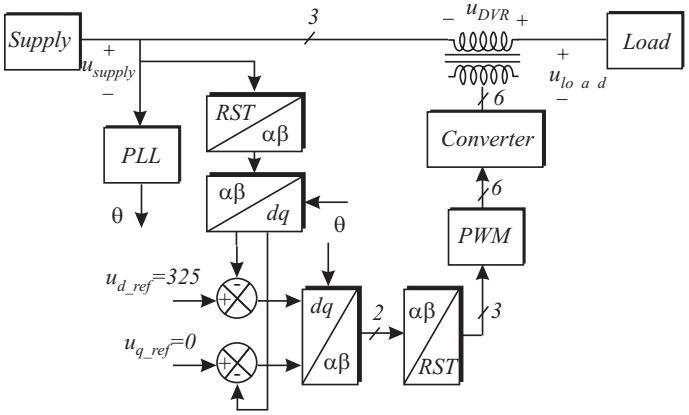

Fig. 7. DVR control in the rotating dq-reference frame.

B. Control Method

The two main control methods applied to DVR's are the open loop control and the closed loop control [7]. Closed loop control have the potential of the best performance, but changes in the load leads to a varying system model and the voltage controller must be designed with caution. Open loop load voltage control is often used and combined with feed forward compensation of the voltage drop caused by the line filter and the injection transformer. In this paper open loop control is used and Fig. 7 illustrates the control used.

Space vector control has been applied to the DVR,

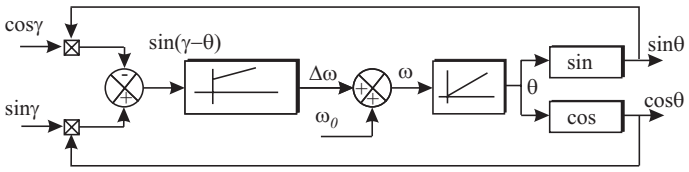

Fig. 8. Phase locked loop(PLL) to synchronize the DVR to the supply voltage.

hence the RST voltages have been transformed in to a space vector representation:

$$\underline{u}_{\alpha\beta} = u_R + u_S e^{j\frac{2\pi}{3}} + u_T e^{j\frac{4\pi}{3}} = u_\alpha + j u_\beta \qquad (2)$$

The space vector are transformed in to a rotating dq-reference frame according to 3:

$$u_d + j u_q = (u_\alpha + j u_\beta) e^{-j\theta} \qquad (3)$$

A voltage sag is detected by measuring the error between the dq-voltage of the supply and the reference values:

$$|u_{error,dq}| = \sqrt{(u_{ref,d} - u_{supply,d})^2 + (u_{ref,q} - u_{supply,q})^2} \qquad (4)$$

The d-reference component is set to rated voltage and the q-reference component is set to zero.

C. Synchronization

The synchronization of the DVR to the supply is shown in Fig. 8, which is further described in [4]. The angle γ indicates the instantaneous angle of the supply space voltage and θ is the angle of the PLL. The PLL tracks the positive sequence component of the supply voltage and the PLL angle is used for transformation to the dq-system. The angle θ is filtered from most harmonics, non-symmetry and transients from the supply voltages. The PLL above is processed in the DSP with the same sampling time as the switching frequency.

V. Simulations

The control system, converter, supply and load are modelled and written for implementation in Saber to test the different control strategies for the DVR. Fig. 9 illustrates the supply voltage with a 70 % voltage sag and a 30° negative phase jump. The sag is symmetrical with a duration of 100 ms. At time, t = 40 ms the voltage sag is initiated and the supply voltage is restored 100 ms later. At time t = 140 ms the supply voltage jumps back to the pre-sag condition, which correspond to a positive phase jump.

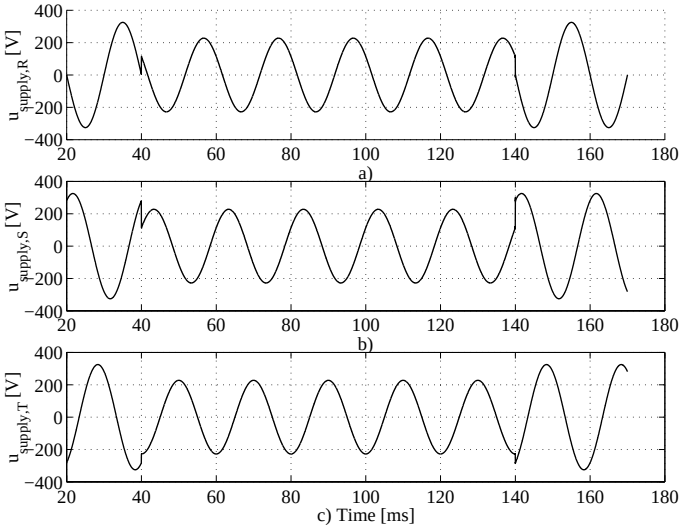

Fig. 9. The associated supply voltages during a voltage sag with a phase jump. a) Supply voltage phase R, b) supply voltage phase S and c) supply voltage phase T.

A. In-phase compensation with smooth compensation of the phase jump

A PLL with a response time of approximately 10 ms is used for this method Fig. 10a. illustrates how the PLL is able to track the fundamental component during a 70 % voltage sag with a 30° negative phase jump. The PLL has a fast response time and it starts tracking the new angle of the supply. The associated dq-voltages of the supply is shown in Fig. 10b. and c. A reduction in the d- and q-component can initially be seen and the missing voltage must be injected to avoid disturbing the load. In case of a symmetrical voltage sag without a phase jump the supply would only have a reduction in the d-component.

The $u_{ref,q}$ is set to zero (0 V) and the $u_{ref,d}$ is set to nominal voltage (325 V) and the effect is a smooth compensation of the phase jump from instantaneous wave compensation to in-phase compensation. In Fig. 11 the generated load voltages are shown. With this method the DVR is also injecting a voltage after the supply voltage is restored, because the positive phase jump, that occurs when the supply voltage is restored, is smoothed by the DVR.

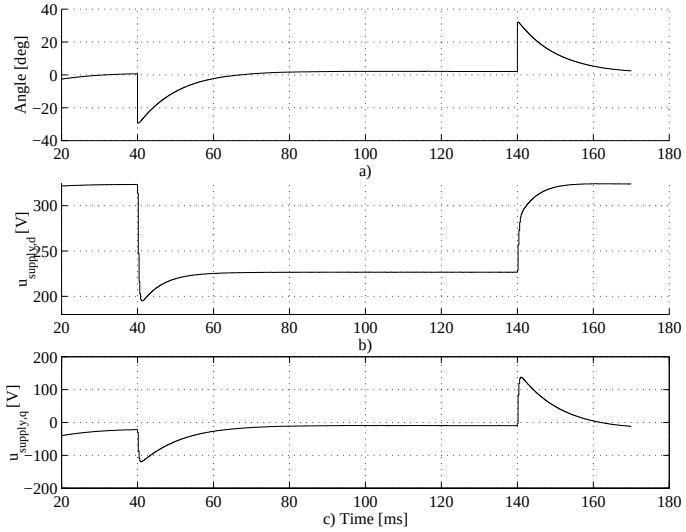

Fig. 10. Simulation of a 70% voltage sag with in-phase compensation a) Angle between the supply and the PLL. ($\gamma - \theta$), b) d-supply voltage and c) q-supply voltage

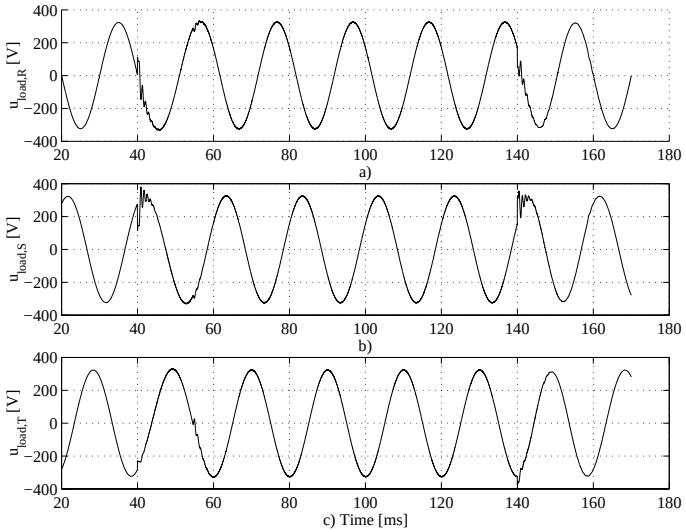

Fig. 11. The associated load voltages for each phase during a voltage sag with a phase jump.

B. Pre-sag compensation

To have pre-sag compensation the angular velocity of the pre-sag voltage is used during the sag and the PLL output is used again, when the sag is over. Fig. 12a. illustrate again the angle between the supply voltage and the used transformation angle. Both the dq-component of the supply voltage (Fig. 12b. and c. are reduced and the DVR injects d-component up to 325 V and q-component up to 0 V. The load voltage in Fig. 13 seems almost undisturbed and the phase jump remain unseen by the load.

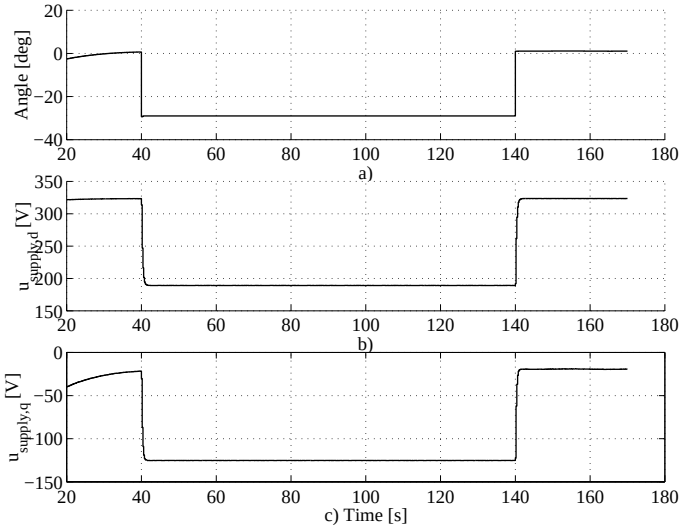

Fig. 12. Simulation of a 70% voltage sag with pre-sag compensation a) Angle between the supply and the PLL ($\gamma - \theta$), b) d-supply voltage and c) q-supply voltage.

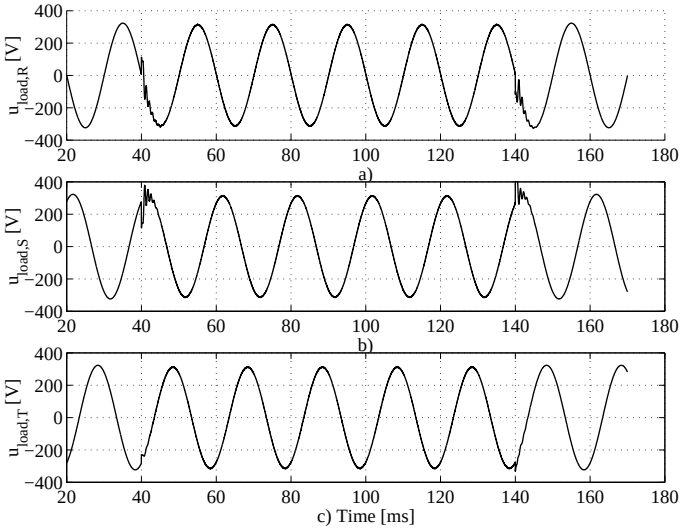

Fig. 13. The associated load voltages for each phase during a voltage sag with a phase jump.

VI. Experimental results

The two methods have been tested on an experimental setup, the DVR system has been described under test system and the test conditions is in both cases a voltage sag down to 80 % with a 15° negative phase jump. The stationary values for the two control methods are:

$$\underline{U}_{pre-sag} = \underline{U}_{supply} - \underline{U}_{sag} = 1\angle 15^\circ - 0.8 = 0.31\angle 57^\circ \quad (5)$$

$$\underline{U}_{in-phase} = \underline{U}_{supply} - \underline{U}_{sag} = 1\angle 0^\circ - 0.8 = 0.2\angle 0^\circ \quad (6)$$

This means the pre-sag compensation require a 50 % higher rated DVR compared with the in-phase compensation method.

The load applied for these tests is a symmetrical star connected load with resistors (16 Ω) paralleled with inductors (168 mH). The load conditions are approximate 11 kVA with a power factor of 0.96, hence the load current is lagging the load voltage by 17°.

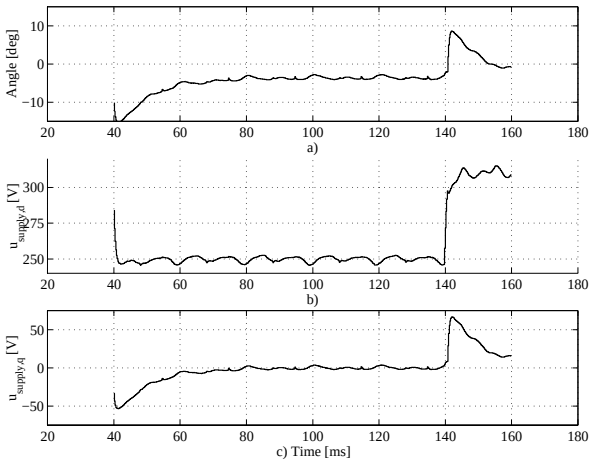

Fig. 14. Measurement of a 80% voltage sag with in-phase compensation a) Angle between the supply and the PLL. ($\gamma - \theta$), b) d-supply voltage and c) q-supply voltage

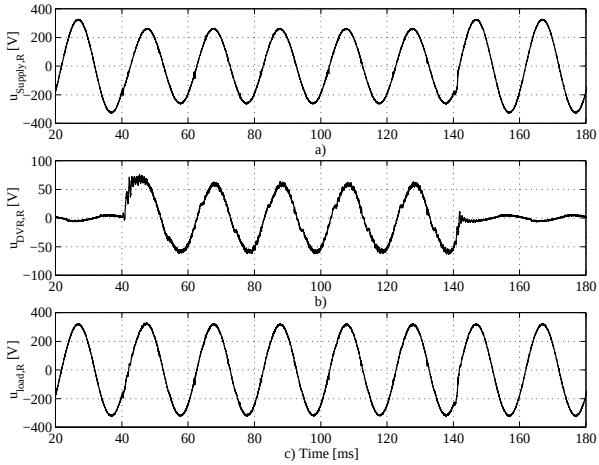

Fig. 15. Measured response during a 80 % voltage sag from 230 V to 184 V with in-phase compensation. a) Supply voltage phase R, b) DVR voltage phase R and c) load voltage phase R.

A. *In-phase compensation with smooth compensation of the phase jump*

The in-phase compensation with smooth compensation of the phase jump avoid a large phase jump seen by the load, but within a certain time the PLL synchronize with the new supply frequency and generate a voltage in phase with the supply voltage. Applying the smoothing method the DVR still require a high rating. Fig. 14a. illustrate the measured angular difference between the PLL angle and the actual supply angle. The deviation disappear fast with a time constant of approximate 10 ms. In 14b. and c. the associated d- and q-voltages for the supply voltage can be seen. The parameters in Fig. 14 have been recorded by the DSP at 5 kHz sampling frequency with no pre-triggering.

The DVR response and performance for one phase can be seen in Fig. 15, which illustrate the supply voltage with the phase jump, the injected DVR voltage and the resulting load voltage. The parameters have here been measured with an oscilloscope at 50 kHz sampling frequency. From the zoomed view of the the initial response in Fig. 16 the phase jump can be seen and how the DVR in time starts to inject a voltage in-phase with the new supply voltage. The phase of the load voltage is with this method changed two times at the beginning of the sag and at the end of the sag. These phase shifts can still disturb the load and induce a transient current according to the new phase of the load voltage.

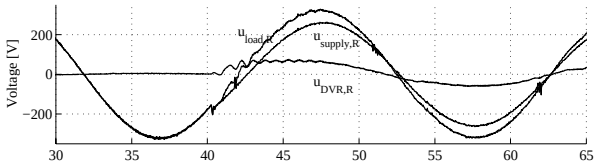

Fig. 16. Zoomed view of the measured response during a 80 % voltage sag from 230 V to 184 V. The Supply voltage drops, the DVR voltage goes from a low standby voltage drop to an injection value and the load voltage is almost maintained constant.

B. *Pre-sag Compensation*

The pre-sag condition is here locked and the load is compensated for the phase jump. Fig. 17 illustrate the measured angle difference and the associated dq-voltages for the supply. In the RST reference frame the response is shown in Fig. 18 with the supply voltage, DVR voltage and the load voltage.

A zoomed view of the initial response of a voltage sag is illustrated in Fig. 19, which clarify that the original phase of the supply voltage is maintained by the DVR.

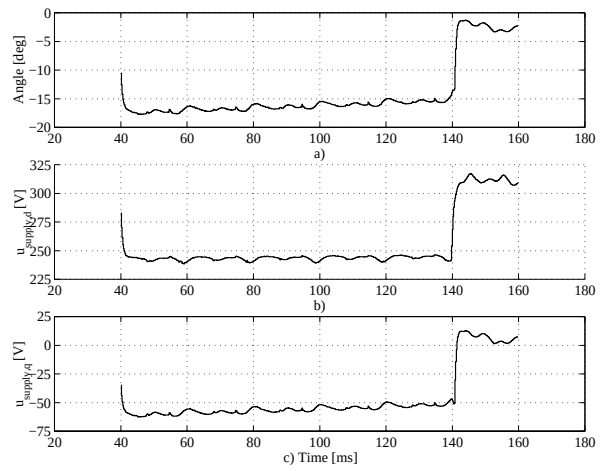

Fig. 17. Measured response during a 80 % voltage sag from 230 V to 184 V with pre-sag compensation a) Angle between supply and the PLL. ($\gamma - \theta$), b) d-supply voltage and c) q-supply voltage

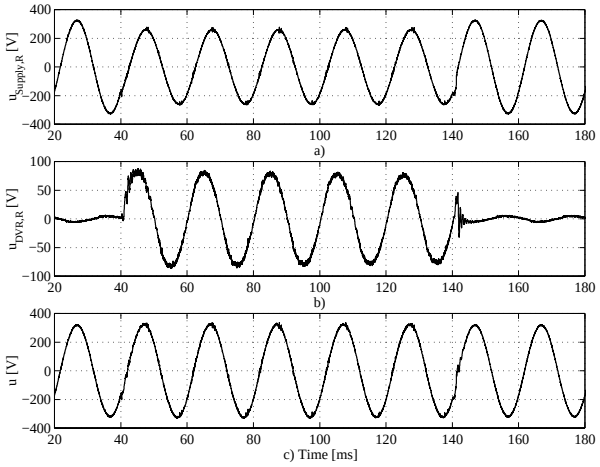

Fig. 18. Measured response during a 80 % voltage sag from 230 V to 184 V. with pre-sag compensation a) Supply voltage phase R, b) DVR voltage phase R and c) load voltage phase R

The method gives minimum disturbances to the load and no transient currents will be initiated if the pre-sag phase and voltage are maintained. Freezing to the pre-sag condition can be difficult, when the duration of the voltage sag are long. In this case small deviations between actual supply angular velocity and pre-sag angular velocity can give a degraded performance.

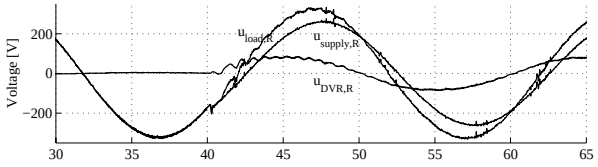

Fig. 19. Zoomed view of the measured response during a 80 % voltage sag from 230 V to 184 V. The Supply voltage drops, the DVR voltage goes from a low standby voltage drop to an injection value and the load voltage is almost maintained constant.

VII. Conclusion

The DVR could be a important device in the future to protect sensitive loads from voltage sags. Often voltage dips are accompanied with phase jumps, which challenges the DVR rating and the control of a DVR. A good compensation of voltage sags with phase jump is essential to protect very sensitive loads.

The control of a dynamic voltage have been analyzed and it is stated that that to protect sensitive loads it is pursued to preserve a load voltage without sudden phase shift.

Two methods have been proposed to compensate a voltage sag with a phase jump. The first method called "in-phase compensation" smoothes the phase jump and after approximately 10 ms generates an in-phase voltage with the during-sag voltage. The second method called "pre-sag compensation" compensate for the phase jump and protects thereby fully the load from the phase jump. Simulations indicate that the methods are feasible and experiments with a 10 kVA rated DVR verifies, that both methods are applicable in the control of a dynamic voltage restorer.

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Comparison of System topologies for Dynamic Voltage Restorers

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Abstract— **In this paper system different topologies for dynamic voltage restorers are analyzed with the emphasis put on methods to acquire the necessary energy during a voltage sag.**

Four different system topologies are analyzed and tested. Two, which can be realized with insignificant energy storage and the energy is taken from the grid and two topologies, which are based on stored energy are compared.

Experimental tests on a 10 kVA rated Dynamic Voltage Restorer shows that the no-energy storage concept is feasible, but an improved performance can for certain voltage sags, be achieved with stored energy. In the comparison the no-storage topology with a passive shunt converter at the load side is ranked highest followed by an energy storage topology with constant DC-link voltage.

I. Introduction

Voltage sags in the grid are almost impossible to avoid, because of the finite clearing time of the faults causing the voltage sags and the wide propagation of sags from the transmission and distribution system to the low voltage loads. The theory of voltage sags and interruptions is thoroughly described in [1]. Equipment can be made more tolerant to sags either via more intelligent control of the equipment or by storing more energy in each equipment. Instead of modifying each component in a plant to be very tolerant to voltage sags, a better solution might be to install one dynamic voltage restorer (DVR) to mitigate voltage sags. A DVR can eliminate most sags and minimize the risk of load tripping at very deep sags. The main drawbacks of inserting a DVR is the standby losses and the equipment costs.

So far the main focus in literature have been on the compensation of sags, non-symmetrical sags, sags with phase jumps [4], [6] and the control of DVR's reported in [8] and [3]. Topologies for dynamic voltage restorer have been treated theoretically in [5]. This paper investigates and compares basic system topologies for DVR's followed up with extensive tests in the laboratory. System topologies for DVR's are very relevant for cost, complexity and performance and a comparison of the different concepts will be performed.

II. Voltage sags

Voltage sags are caused by a short circuit current flowing into a fault, which is shown in Fig. 1. Magnitude and phase of the voltage, $\underline{U}_{sag}$ during the sag, at the Point of Common Coupling(PCC), are determined by the fault and source impedances, using the following simplified equation:

[0]Acknowledgement to the electric distribution companies in Denmark, Elfor and Sjaellandssamarbejdet for sponsoring the research in power quality and equipment for power quality enhancement.

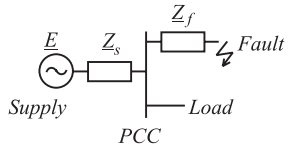

Fig. 1. The origin of voltage sags.

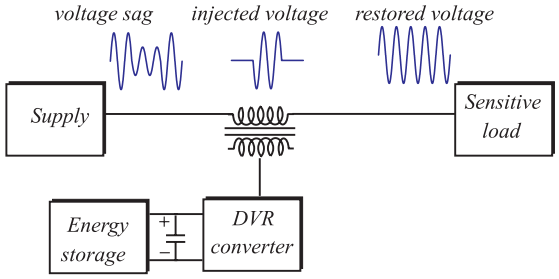

Fig. 2. Principle operation of the Dynamic Voltage Restorer.

$$\underline{U}_{sag} = \underline{E}\frac{\underline{Z}_f}{\underline{Z}_f + \underline{Z}_s}. \quad (1)$$

Voltage sags are for a symmetrical sag characterized by the remaining voltage, U_{sag}. The missing voltage is the voltage, which should be generated by the DVR for an un-disturbed load voltage, the sag duration, t_{sag} varies from location but are generally linked to the protection system used in the grid system. The remaining voltage is characterized by:

$$\underline{U}_{sag} = \underline{U}_{pre-sag} - \underline{U}_{missing}. \quad (2)$$

The Dynamic voltage restorer injects a voltage in series with the supply to compensate for voltage sags. The principle operation of a DVR is illustrated in Fig. 2.

For a DVR the depth and duration of the voltage sags are important for the DVR rating and system topology.

III. System topologies for Dynamic Voltage Restorer

In the basic concept of a DVR the voltage output is always controlled to the rated value. All the concepts, which are considered here are three-phase systems and in the analysis of the rating requirements only the active power flow is considered. It is assumed the load is a high power factor load, only active power is absorbed by the passive converter and the DVR injects only a voltage in-phase with the supply voltage.

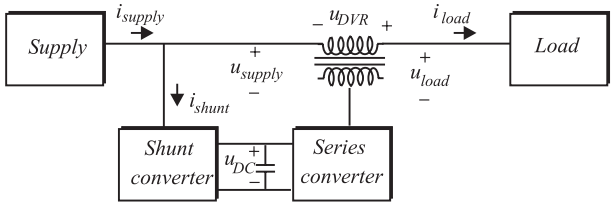

Fig. 3. Dynamic Voltage Restorer with no energy storage and supply side connected converter (System 1).

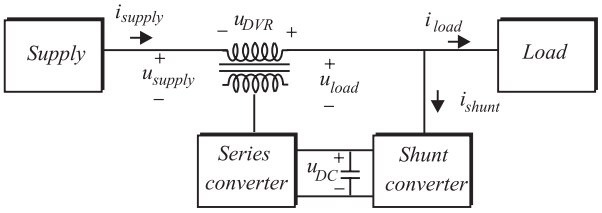

Fig. 4. Dynamic Voltage Restorer with no energy storage and load side connected shunt converter (System 2).

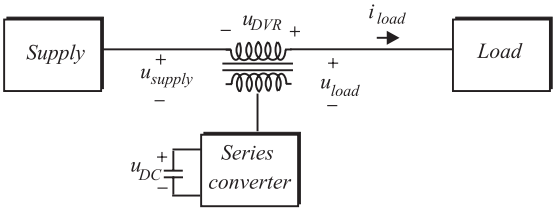

Fig. 5. Dynamic Voltage Restorer with energy storage and with variable DC-link voltage (System 3).

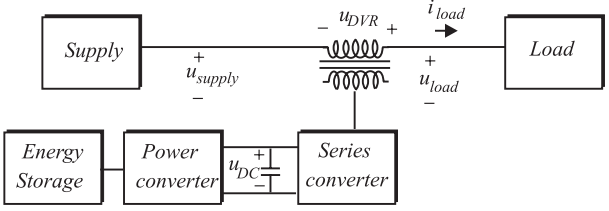

Fig. 6. Dynamic Voltage Restorer with energy storage and with constant DC-link voltage (System 4).

The efforts in this paper are focused on loads absorbing power and the compensation of voltage sags. Four different DVR system topologies for Dynamic Voltage Restorer are considered:

- **Topologies with no energy storage**

System 1. Energy is taken from the existing supply with a passive shunt converter connected to the supply side (Fig. 3).

System 2. Energy is taken from the existing supply with a passive shunt converter connected to the load side (Fig. 4). Reported in [9].

- **Topologies with energy storage**

System 3. Stored energy in the DC-link and a variable DC-link voltage (Fig. 5).

System 4. Arbitrary kind of energy storage with a controllable DC-link, which can be held constant (Fig. 6). Reported in [7].

The topologies varies in performance, complexity, cost and control which are further analyzed.

A. DVR Topologies with no energy storage

The no energy storage topologies are utilizing the fact, that during a voltage sag a significant part of the supply voltage often still remains. If the DVR is connected to a strong grid the necessary power to the load can be ensured by increasing the supply current by a shunt converter and inject the missing voltage with the series converter.

A passive shunt converter is used because only unidirectional power flow is assumed necessary. Two basic topologies can be used, which here are categorized according to the location of the shunt converter.

A.1 Supply side connected shunt converter

The supply side connected converter as shown in Fig. 3 has an uncontrollable DC-link voltage and the passive converter will charge the DC-link capacitor to the actual state of the supply voltage. The DC link voltage is approximately equal to the peak phase-phase value of the supply voltage. At voltage sags the DC-link voltage drops proportionally to the during sag voltage, according to

$$U_{DC} \simeq \sqrt{6} \cdot U_{supply} \simeq \sqrt{6} \cdot U_{sag}. \tag{3}$$

where U_{DC} and U_{supply} are the DC-link voltage and supply voltage respectively. The active power consumed by the load is constant before and during the sag. The power and current handled by the converters can be approximated to:

$$P_{shunt} = P_{serie} \simeq 3(1 - U_{sag}/U_{rated})I_{load}, \tag{4}$$

$$I_{serie} = I_{load}, \tag{5}$$

$$I_{shunt} \simeq \frac{1 - U_{sag}/U_{rated}}{U_{sag}/U_{rated}} I_{load}. \tag{6}$$

P_{shunt} and P_{serie} are the three-phase power handled by the shunt and series converter respectively. U_{sag} is the during sag phase voltage, U_{rated} is the rated supply voltage and I_{load} is the rated load current.

The power handled by the shunt converter is proportional to the missing voltage and at severe sags the current drawn by the shunt converter rises significantly. E.g. if only 30 % is left of the supply voltage at rated load the current through the series converter is 100 % and 233 % through the shunt converter.

A.2 Load side connected shunt converter

At a load side connected shunt converter, as shown in Fig. 4, the voltage to the shunt converter can be

controlled within certain limits of the series converter. The DC-link voltage can be held almost constant by injecting sufficient voltage (U_{DVR}).

$$U_{DC} \simeq \sqrt{6} \cdot U_{load} \simeq \sqrt{6} \cdot (U_{sag} + U_{DVR}) \tag{7}$$

The main drawback is a high current through the series converter. E.g. in the case of a 30 % voltage sag at rated load the current through the series converter is 333 % and 233 % through the shunt converter.

$$P_{shunt} = P_{serie} \simeq \frac{1 - U_{sag}/U_{rated}}{U_{sag}/U_{rated}} P_{load}, \tag{8}$$

$$I_{serie} = I_{supply} \simeq \frac{P_{load}}{3U_{sag}}, \tag{9}$$

$$I_{shunt} \simeq \frac{1 - U_{sag}/U_{rated}}{U_{sag}/U_{rated}} I_{load}. \tag{10}$$

where P_{load} is the rated power of the load. Another interesting point is the distorted current drawn by the passive shunt converter, which also can degrade the quality of the load voltage.

B. Topologies with energy storage

Storing electrical energy is expensive, but for certain voltage sags the performance of the DVR can be improved and the strain on the grid connection is lower. Two methods are here considered and in both methods the current flowing from the grid is unchanged during a voltage sag.

B.1 Variable DC-link voltage

Storing energy in DC-link capacitors as shown in Fig. 5 is a well suited solution for DVR's. A simple topology can be operated with a variable DC-link voltage. The stored energy, $E_{storage}$ is proportional to the square of the DC-link voltage, U_{DC}.

$$E_{storage} = \frac{1}{2} C_{DC} U_{DC}^2 \tag{11}$$

The voltage decays exponentially during a voltage sag compensation and as the DC-link voltage decays the ability to compensate severe sags deteriorates.

$$P_{serie} \simeq (1 - U_{sag}/U_{rated}) P_{load} \tag{12}$$

The variable DC-link voltage solution has a relative simple power topology and can be re-charged by the series converter or with a low rated auxiliary charging converter. At variable DC-link voltage the energy storage is difficult to use efficient and at severe sags a large fraction of the energy storage is not used.

B.2 Constant DC-link voltage

A method to fully utilize the energy storage or use other types of storage methods e.g. Super Magnetic Energy Storage (SMES), batteries or super capacitors, is to add a highly rated energy conversion converter to the DVR system. The energy is then transferred from a large storage to a small rated DC-link. The DC voltage is held almost constant and the rating of the converters can be calculated to

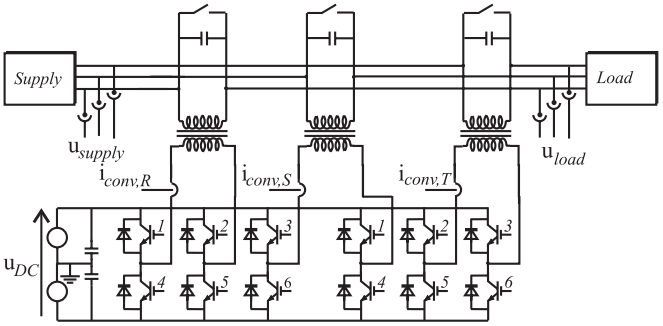

Fig. 7. Power circuit for the DVR in the laboratory.

$$U_{DC} \simeq constant \tag{13}$$

$$P_{power\ converter} = P_{serie} \tag{14}$$

$$P_{serie} \simeq (1 - U_{sag}/U_{rated}) P_{load} \tag{15}$$

The performance is improved compared to the variable DC-link solution, but the equipment costs are higher.

IV. DVR test system

To test and verify the control of the four different DVR's a 10 kVA prototype has been built in the laboratory.

A. Hardware

The DVR converter is based on three full-bridge Voltage Source Converters with a common DC-link. Three single phase transformers ensures galvanic isolation and step down the voltage to 115 V. A filter is located at the line side to filter out the switching harmonics generated by the converter. Fig. 7 illustrate the power circuit for the DVR.

Calculations for the control is carried out in a DSP, ADSP21062 and the switchings are performed by a Micro Controller, SAB80C167. The main hardware parameters for the DVR are listed in Table I. The supply is a fully programmable three phase, 30 kVA AC power supply, where supply sags can be tested. The basic components are shown in Fig. 8.

B. Control Method

Two control methods are generally applied to DVR's, which are the open loop control [2] and closed loop control [8]. Closed loop control have been used for the following tests in a rotating dq-reference frame. Fig. 9 illustrate the control setup. The DVR is synchronized to the supply with an PLL and from the basis of a supply reference voltage ($u_{supply,dq,ref}$) and the actual state of the supply voltage ($u_{supply,dq}$) reference signals for the DVR are calculated ($u_{DVR,dq,ref}$). The error between the DVR reference voltage ($u_{DVR,dq,ref}$) and the

Fig. 8. Prototype DVR in the laboratory. At the left side the programmable supply rack is located (2.5m high), on the wall the power electronic DVR is mounted and below the DVR injection transformers can be seen.

TABLE I
MAIN SYSTEM PARAMETERS IN THE DVR SETUP.

description	absolute value	per unit
load rating	20 kVA	1 pu
DVR rating	10 kVA	0.5 pu
load voltage	230 V	1 pu
DVR voltage	0 - 115 V	0 - 0.50 pu
DC-link voltage	560 V	
supply frequency	50 Hz	1 pu
switching frequency	5 kHz	100 pu

actual DVR voltage($u_{DVR,dq}$) are reduced by two PI-controllers. The controllers generate the dq-control signals to the DVR, which are transformed to three-phase values and the control values are PWM modulated according to an uni-polar switching scheme and the actual state of the DC-link voltage (u_{DC}).

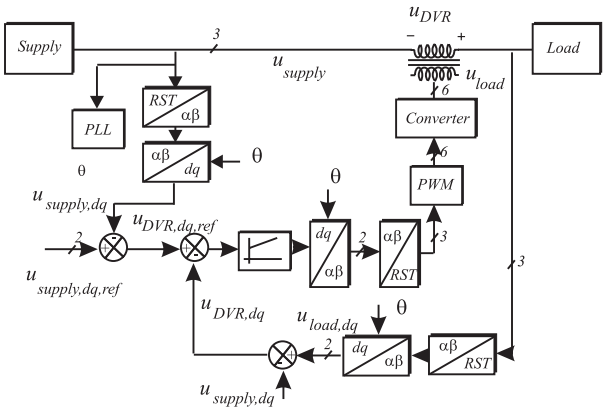

Fig. 9. DVR closed loop control in the rotating dq-reference frame.

V. Experimental results

The four described topologies have been tested and here the time domain results are shown for one type of voltage sag. A 6.6 kVA resistive load is used as load and a 70% symmetrical voltage sag, without any phase jump and the duration of 100 ms has been initiated.

A. No-stored Energy

The performance of the DVR topologies with no energy storage is first tested.

A.1 Supply side connected shunt converter (System 1)

The voltage sag have been applied and the response can be seen at Fig. 10 and Fig. 11. The DC-link is precharged proportionally to the rated voltage supply and in the first period after the sag, the power is solely taken from the DC-link capacitor. At a 70 % voltage sag the DC-link voltage will also drop to approximately 70 % and the shunt converter will begin to absorb the power necessary to inject in series to stabilize the load voltage. In Fig. 10c the DC-link is not fully stabilized and as the sag is cleared a uncontrolled re-charge is initiated. The supply voltage, injected DVR voltage and the load voltage can be seen in Fig. 11 for one phase.

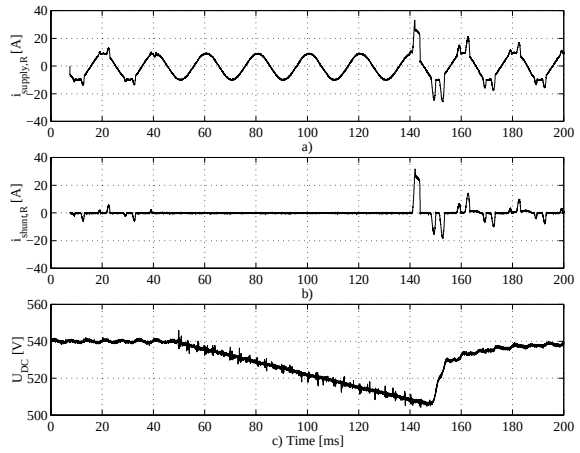

Fig. 10. Measured performance for the supply side connected converter (System 1). a) supply current, b) shunt current and c) DC-link voltage.

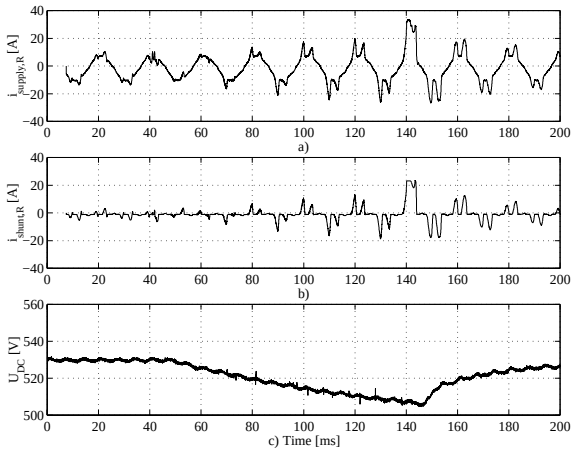

Fig. 12. Measured performance for the load side connected converter (System 2). a) supply current, b) shunt current and c) DC-link voltage.

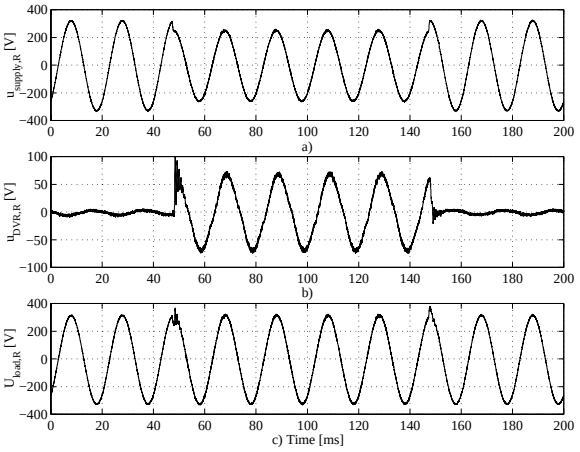

Fig. 11. Measured performance for the supply side connected converter (System 1). a) Supply voltage, b) DVR voltage and c) Load voltage.

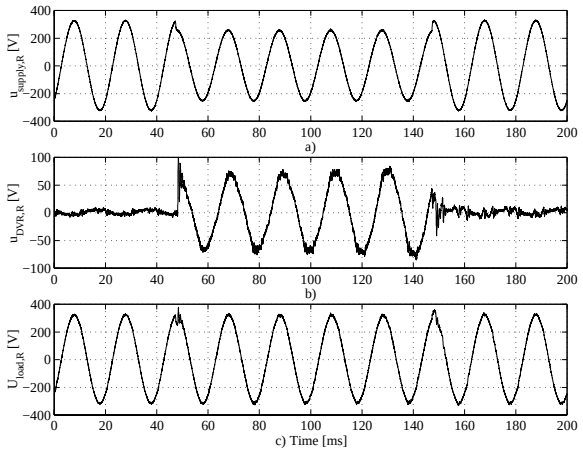

Fig. 13. Measured performance for the load side connected converter (System 2). a) Supply voltage, b) DVR voltage and c) Load voltage.

A.2 Load side connected shunt converter (System 2)

The voltage sag have been applied and the response can be seen in Fig. 12 and Fig. 13. The current flow from the supply and the shunt converter increases Fig. 12a and 12b respectively as the power is drained out of the DC-link. In case of a long sag duration the DC-link stabilizes at a relative high voltage. The supply and shunt converter currents are highly distorted by the non-linear shunt converter. The supply voltage, injected DVR voltage and the load voltage can be seen in Fig. 13 for one phase. The injected voltage in Fig. 13b has a higher harmonic content compared with the previous solution, because the non-linear shunt converter leads to a more distorted load voltage.

B. Stored energy

The concepts with stored energy put less strain on the supply, because they do not increase the absorbed power during a voltage sag.

B.1 Variable DC-link voltage (System 3)

A variable DC-link voltage is used in this method, the main reason is to keep the system cost low. The DC-link can either be charged from the supply with a small rated charging converter or by the series converter itself. The voltage sag have been applied and the response can be seen in Fig. 14. The DC-link voltage decays as power is taken out of the DC-link, the series converter is operated with an increasing modulation index and if the DC-link voltage continues to decrease the load voltage cannot

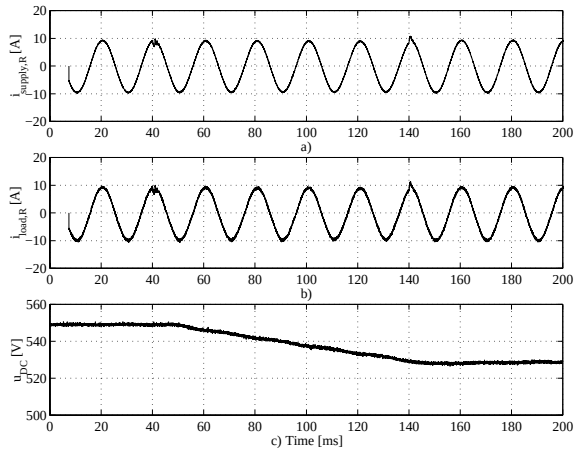

Fig. 14. Measured performance for the variable DC voltage DVR (System 3). a) supply current, b) load current and c) DC-link voltage.

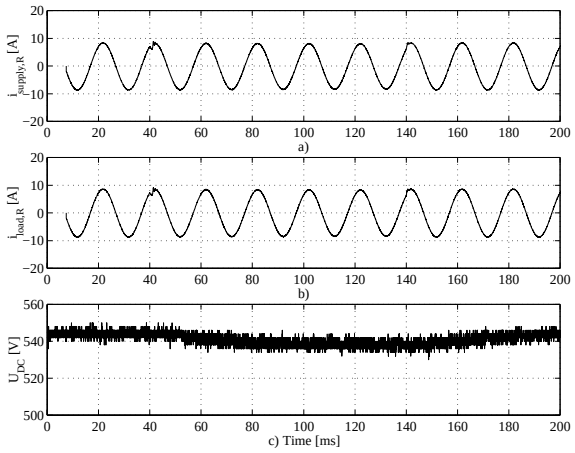

Fig. 16. Measured performance for the constant DC voltage DVR (System 4). a) supply current, b) load current and c) DC-link voltage.

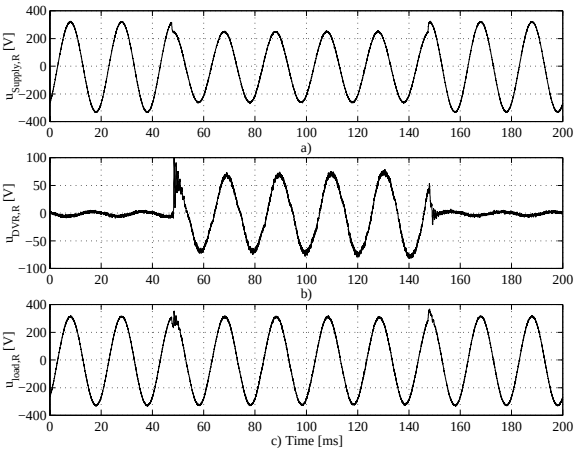

Fig. 15. Measured performance for the variable DC DVR (System 3). a) Supply voltage, b) DVR voltage and c) Load voltage.

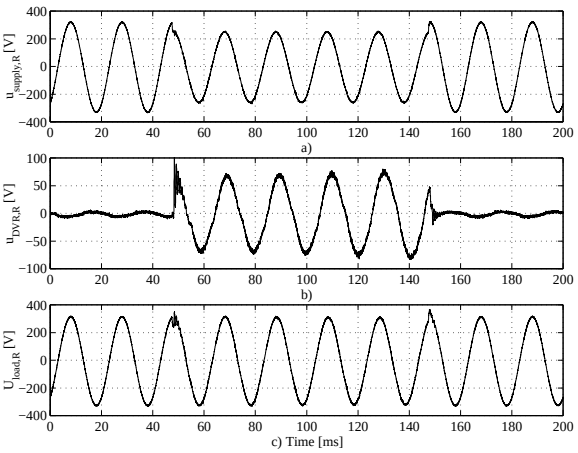

Fig. 17. Measured performance for the constant DC DVR (System 4). a) Supply voltage, b) DVR voltage and c) Load voltage.

be fully restored. The supply voltage, injected DVR voltage and the load voltage can be seen in Fig. 15 for one phase.

B.2 Constant DC-link voltage (System 4)

Experimentally the constant DC-link voltage is maintained with a passive converter and fed from an auxiliary supply. Using this method the DC-voltage is almost constant. The voltage sag have been applied and the response can be seen at Fig. 16. The current from the supply and through the series converter is close to unchanged. The associated supply voltage, injected DVR voltage and the load voltage can be seen in Fig. 17 for one phase.

VI. Comparison

From system analysis and experimental results the four system topologies are compared. Each topology is rated by its expected performance for some main parameters. The results are listed in Table II with the grades (++ very good), (+ good) (- poor) and (-- very poor).

Although the best topology cannot be ultimately stated some main differences can be seen from Table II.

In this comparison System 2 is estimated to have the highest total points with general high performance followed with low cost and complexity. Still the negative grid effects and high rated series converter could disqualify the solution for certain applications.

System 4 has been ranked as second best topology with the highest number of (+) with superior perfor-

TABLE II

Comparison of the different DVR topologies with the grading: very good(++), good(+), poor(-) and very poor (--).

(1) - Supply side connected shunt converter,

(2) - Load side connected shunt converter,

(3) - Variable DC-link voltage,

(4) - Constant DC-link voltage.

	(1)	(2)	(3)	(4)
Long voltage sag duration	++	++	--	-
Deep voltage sags	--	+	-	++
Non-symmetrical voltage sags	--	+	++	++
DC-link voltage control	--	+	-	++
Size of energy storage			+	++
Grid effects	--	-	+	+
Rating of charging/shunt converter	--	-	+	--
Rating of the series converter	+	--	+	+
System complexity	+	+	++	-
Cost Estimation	+	+	-	--
Control complexity	++	+	-	-
Sum (+)	6	8	8	10
sum (-)	10	4	6	7
sum (total)	-4	4	2	3

mance in deep voltage sags, but drawbacks regarding complexity, converter rating and overall cost.

System 3 is ranked number three with relative poor performance for severe and long duration sags, some of the drawbacks are leveled out by the simple topology and converter rating.

The DVR topology, which have the highest number of (-) and least number of total points is System 1. The uncontrollable DC-link voltage which is proportionally to the sag voltage and if the sag is non symmetrical the DVR will tend to draw a non-symmetrical current although the faulted phases will be less loaded. The topology is not found suitable for a DVR solution. If the passive shunt converter was substituted with an active converter some of the main drawbacks could be eliminated and the topology should then be re-evaluated.

VII. Conclusion

Four topologies for DVR's have been investigated and experimentally tested. Each method varies in complexity, performance and cost.

In the comparison of the different system topologies for Dynamic Voltage Restorer the no energy storage topology with a load side connected passive converter (System 2) is evaluated highest, followed by the stored energy concept with constant DC-link voltage (System 4). Third is the stored energy with variable DC-link voltage (System 3) and the poorest performance is estimated for the no energy storage topology with a supply side connected passive converter (System 1).

The experiments indicate some of the main differences, but further parameters could be included e.g. performance at non-symmetrical sags, general stability and the differences in the control structure. Further topologies could also be included e.g. active shunt rectifiers.

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