Design and Control of an Inverter for Photovoltaic Applications

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Design and Control of an Inverter for Photovoltaic Applications

by

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He is currently employed as application-engineer at the Danish company PowerLynx A/S, where he works in the field of grid-connected photovoltaic.

Mr. Kjær is a member of the Society of Danish Engineers (IDA), and the Institute of Electrical and Electronics Engineers (IEEE).

Preface

This thesis is submitted to the Faculty of Engineering and Science at Aalborg University (AAU) in partial fulfillment of the requirements for the Ph.D. (doctor of philosophy) degree in Electrical Engineering.

The 'Solcelle Inverter' project, from which this thesis is a spin off, was started in 2001 as a co-operation between (in alphabetical order) Danfoss A/S, Institute of Energy Technology (IET) - Aalborg University, Risø VEA, and Teknologisk Institut, with financial support from Elkraft System under grant number: 91.063 (FU 1303).

The thesis has been followed by Professor, Ph.D., Frede Blaabjerg (IET), Associate Professor John K. Pedersen (IET), Theiss Stenstrøm (Danfoss A/S), Bo Holst (Danfoss A/S), Ph.D. Uffe Borup (former Danfoss A/S, now PowerLynx A/S), Henrik Bindner (Risø VEA), Ivan Katic (Teknologisk Institut), and Søren Poulsen (Teknologisk Institut).

The purchase of components for the construction of the prototype inverter was made possible thanks to engineer-samples from Evox-Rifa, Fairchild Semiconductors, Unitrode / Texas Instruments, Maxim Semiconductors, ON Semiconductors, and EPCOS.

At Aalborg University I would like to thanks Walter Neumayr for his expertise during the manufacturing of the prototype. Also thanks to Gert K. Andersen, Michael M. Bech, Stig Munk-Nielsen, and Remus Teodorescu for their time to discuss various technical problems.

This thesis is structured in 8 chapters, a literature reference, and 8 appendices. References to literature, figures and equations is done by the following principle:

Literature	[L]	where L is the literature number in the reference list.
Figures	C.F	where C indicates the chapter or appendix, and F indicates the figure number in the actual chapter or appendix.
Equations	(C.E)	where C indicates the chapter or appendix, and E indicates the equation number in the actual chapter or appendix.

Upper case letters, e.g. I_d, denotes Root Mean Square (RMS) values. Lower case letters, e.g. i_d, distinguishes instantaneous values. Furthermore, peak values are denoted with a hat, e.g. $\hat{I}_d$, values averaged over time are denoted with brackets, e.g. $\langle I_d \rangle$, and finally, small-signal values are denoted with a tilde, e.g. $\tilde{\imath}_d$.

Aalborg University, December 2004

Søren Bækhøj Kjær

Abstract

The energy demand in the world is steadily increasing and new types of energy sources must be found in order to cover the future demands, since the conventional sources are about to be emptied.

One type of renewable energy source is the photovoltaic (PV) cell, which converts sunlight to electrical current, without any form for mechanical or thermal interlink. PV cells are usually connected together to make PV modules, consisting of 72 PV cells, which generates a DC voltage between 23 Volt to 45 Volt and a typical maximum power of 160 Watt, depending on temperature and solar irradiation.

The electrical infrastructure around the world is based on AC voltage, with a few exceptions, with a voltage of 120 Volt or 230 Volt in the distribution grid. PV modules can therefore not be connected directly to the grid, but must be connected through an inverter. The two main tasks for the inverter are to load the PV module optimal, in order to harvest the most energy, and to inject a sinusoidal current into the grid.

The price for a PV module is in the very moment high compared with other sources. The lowest price for a PV module, inclusive inverter, cables and installation, is approximately 30 DKK[!] per Watt (app. 4.0 € per Watt), or about 5000 DKK (app. 670 € per system) for a standard PV module and inverter with a nominal power of 160 Watt. This corresponds to a production-price of 0.24 € per kWh over a time period of 25 years, which cannot yet compete with other energy sources. However, it might be profitable for domestic use, since in does not have to take duty, tax, and wage for regular cleaning of the PV module, etc, into consideration.

One method, among many, to PV power more competitive is by developing inexpensive and reliable inverters. The aim of this thesis is therefore to develop new and cheap concepts for converting electrical energy, from the PV module to the grid. Research has therefore been done in the field of inverter technologies, which is used to interface a single PV module to the grid. The inverter is developed with focus on low cost, high reliability and mass-production.

The project contains an analysis of the PV module, a specification based on the analysis and national & international standards, and a state-of-the-art analysis of different inverter topologies. Two new topologies are discovered, and a topology is selected for further design. The inverter, with belonging auxiliary circuits, is designed and a prototype is build. The prototype is tested at the test facilities of Teknologisk Institut. The project has resulted in an inverter, which can be mass-produced within a short time.

[!] 1 € is approximate 7.50 DKK (January 2005)

Dansk Resumé

Verdens energibehov er stødt stigende og nye energityper skal derfor findes for at dække fremtidens efterspørgsel, da de konventionelle kilder er ved at rinde ud.

En type af vedvarende energikilde er solcellen, der omsætter sollys til elektrisk strøm, uden nogen form for mekanisk eller termisk mellemled. Solceller sammensættes som reglen til solcellemoduler bestående af 72 solceller, der frembringer en jævnspænding mellem 23 Volt til 45 Volt og en typisk maksimum effekt på 160 Watt, alt efter temperatur og solintensitet.

Den elektriske infrastruktur rundt omkring i verden er baseret på vekselstrøm, med få undtagelser, med en spænding på 120 Volt eller 230 Volt i distributionsnettet (nettet). Solcellemoduler kan derfor ikke direkte tilsluttes til nettet, men skal tilsluttes gennem en inverter. Inverterens to hovedopgaver er at laste solcellemodulet optimalt så der høstes mest energi, samt at injicere en sinusformet strøm i nettet.

Prisen på solcellemoduler er i øjeblikket høj sammenlignet med andre kilder. Den laveste pris for et solcellemodul, inklusiv inverter, kabel og installation, er ca. 30 DKK per Watt (ca. 4.0 € per Watt), eller omkring 5000 DKK (ca. 670 € per system) for et almindeligt solcellemodul med inverter, med en nominel effekt på 160 Watt. Dette svarer til en produktionspris på 1.80 DKK per kWh over en periode på 25 år, hvilket endnu ikke kan konkurrerer med andre energityper. Til hjemlig anvendelse kan det godt løbe rundt, da der ikke skal tages højde for afgifter, skatter, samt arbejdsløn til jævnlig rengøring af solcellemodulet, mm.

En af måderne, blandt mange, at gøre denne energikilde mere konkurrencedygtig, er ved at udvikle prisbillige og pålidelige invertere. Formålet med denne afhandling er således at udvikle nye og billige koncepter til konvertering af elektrisk energi fra solceller til nettet. Der er blevet forsket i udviklingen af en inverter-teknologi, der skal anvendes direkte til det enkelte solcellemodul. Inverter er udviklet med fokus på low-cost, høj pålidelighed samt masseproduktion.

Projektet indeholder en analyse af solcellemodulet elektriske virkemåde, en kravspecifikation baseret på analysen og nationale samt internationale standarder, samt en state-of-the-art analyse af forskellige inverter topologier. To nye topologier er fundet, og en topologi er udvalgt til endelig dimensionering. Inverteren med tilhørende hjælpekredsløb er designet og en prototype er bygget. Prototypen er blevet testet som demonstrator ved Teknologisk Instituts' testfaciliteter. Projektet har resulteret i en inverter, som inden for en kort tidshorisont kan masseproduceres.

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Chapter 1

Introduction

This chapter introduces the 'direct current' to 'alternating current' (DC-AC) inverter concepts for photovoltaic (PV) applications. The PV module in Figure 1.1 is capable of generating electric DC power, when exposed to sunlight. The interest in this thesis is especially on inverters where the load is the low-voltage AC public utility network (through out this thesis: the grid), and the source is a single PV module. This chapter answers the following important questions:

- Why are inverters for PV modules of interest?
- What is the background on previous solutions?
- What is the background on potential solutions?
- What is attempted in the present research project?
- What will be presented in this thesis?

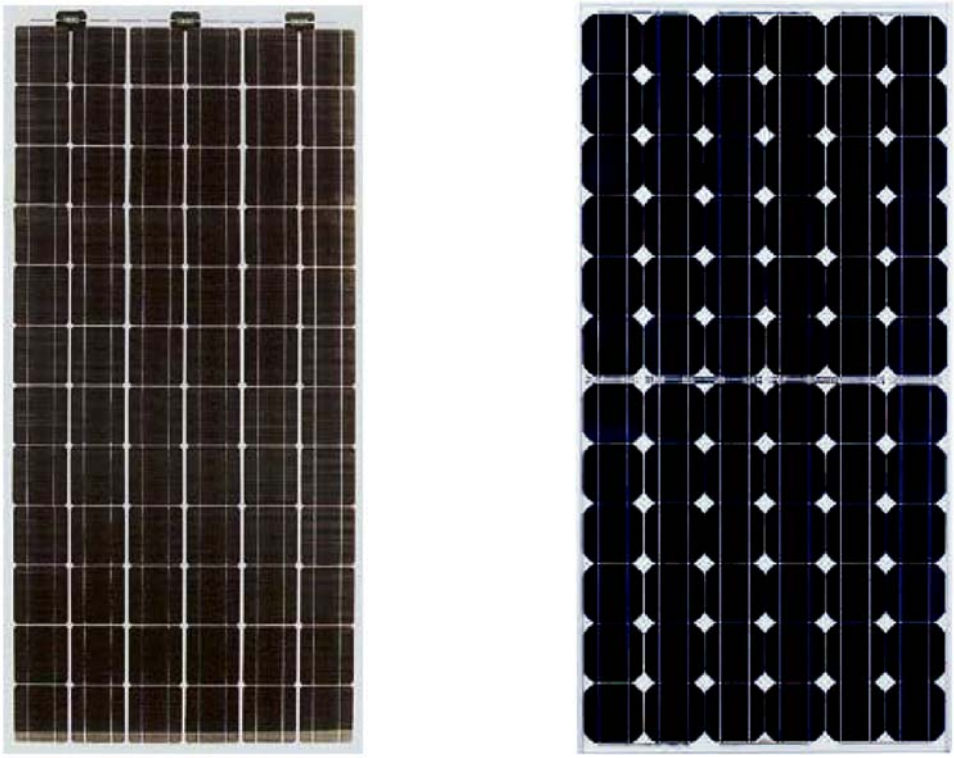

Figure 1.1. Photograph of two mono-crystalline 72 cells photovoltaic (PV) modules.

1.1 Background and Motivation

Power generated by PV modules[1] and injected into the grid is gaining more and more visibility in the area of PV applications, cf. Figure 1.2. This is mainly because the global energy demand is steadily increasing. Not many PV systems have so far been put into the grid, cf. Figure 1.3. This is due to a relatively high cost, compared with the more traditional energy sources, such as oil, gas, nuclear, hydro, wind, etc.

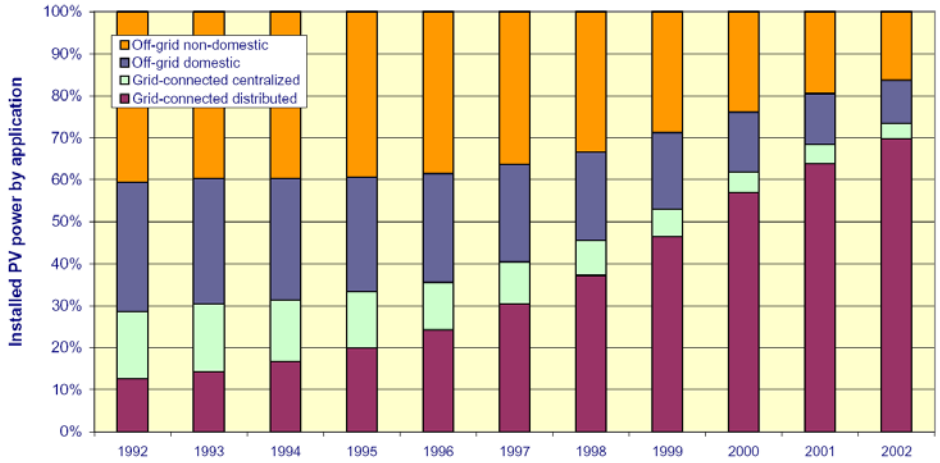

Figure 1.2. Percentage of PV power by application in the International Energy Agency (IEA) reporting countries [1].

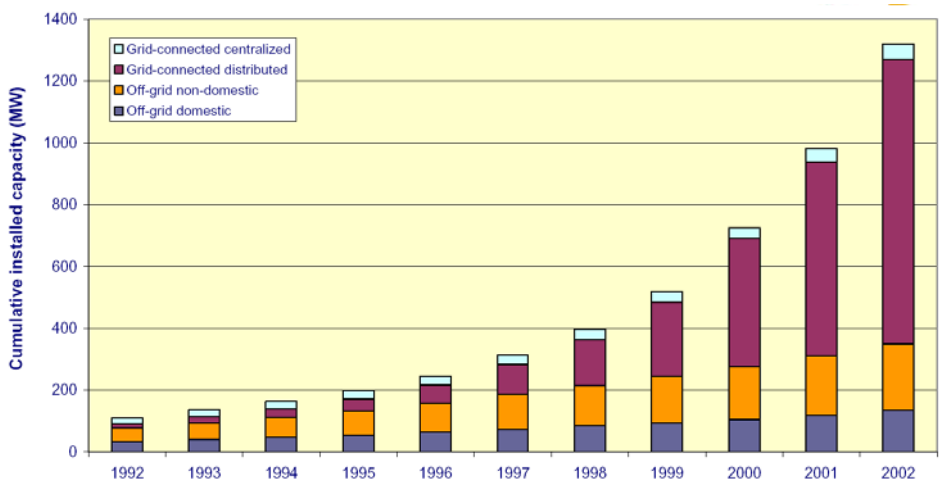

Figure 1.3. Cumulative installed PV power by application area in the reporting countries [1].

The PV modules was in the past the major contributor to the cost of the systems, cf. Figure 1.4. A downward tendency is now seen in the price of the modules, due to a massive increase in production capacity, cf. Figure 1.5. The cost of the inverters is for the same reason becoming more visibly in the total.

[1] The photovoltaic module is described in chapter 2, and is therefore not explained in dept in this chapter.

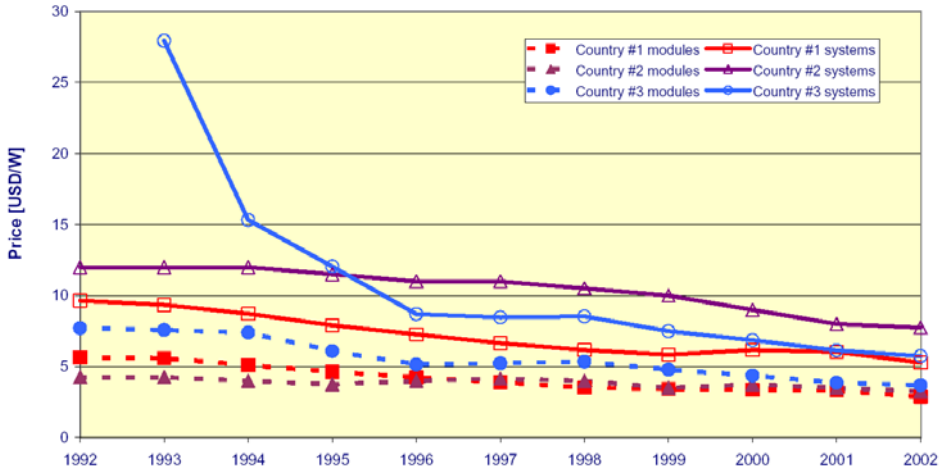

Figure 1.4. PV system and module price trends in selected reporting countries [1].

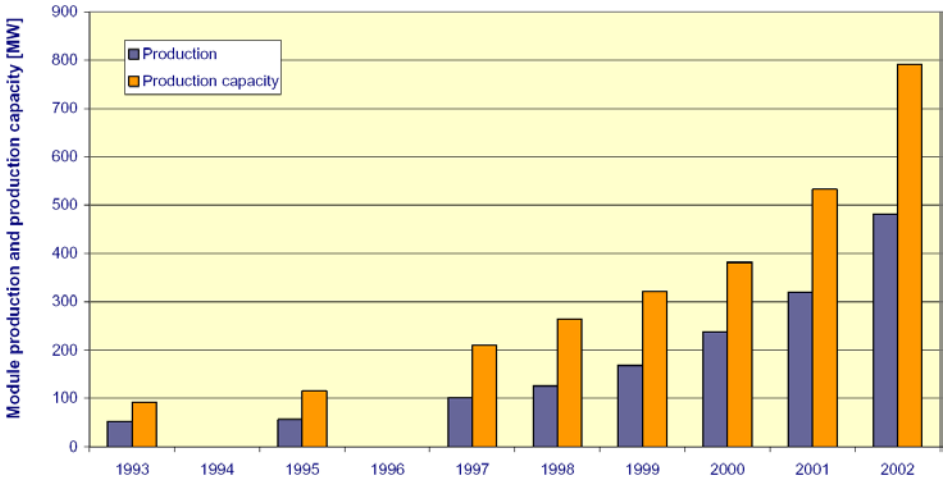

Figure 1.5. PV module production and module production capacity between 1993 and 2002 [1].

The four figures can shortly be summarized as:

- Installed grid-connected PV power, in International Energy Agency (IEA) countries: 980 MW in year 2002, which is an increase of 46% compared to year 2001,
- PV module production capacity was 790 MW/year in 2002, an increase of 49% compared to year 2001,
- The price per Watt in 1996 is app. 8.8 USD, where 50% of the cost is used to PV modules. In 2002, the price is app. 5.5 USD, where 60% of the cost is used to the PV modules.
- The price in Europe is approximately 6.2 USD per installed Watt, in year 2002, including inverter, hardware and workmanship. The Danish SOL1000 program has included a reduction, thus the Danish price is approximate 4.3 USD per installed Watt (1.80 DKK per kWh, expected lifetime 25 year).

A PV module does not contain any moving parts. A long lifetime is therefore guaranteed, without almost any tear-and-wear and maintenance. For example, BP SOLAR gives the following warranties: 25-year on 80% power-output, 12-year on 90% power-output, and 5 years on materials and workmanship [2].

It is also worth noting that the countries with the fastest going development and application of grid-connected PV modules are Germany, Japan and the Netherlands.

Finally, the energy captured by the PV module is environment friendly, renewable, inexhaustible or as an advertising expert would argue:

The SUN - Your source of natural light and energy for over 5 billion years!

Try it today, free while supplies last...

1.2 Inverters for Photovoltaic Applications

The power electronic interface for PV-grid systems has two main tasks:

- To amplify and invert the generated DC power into a suitable AC current for the grid. A standard PV module generates approximately 100 W to 150 W at a voltage around 23 V to 38 V, whereas the grid mostly requires 110V at 60 Hz or 230 V at 50 Hz.
- To control the PV module so as to track the Maximum Power Point (MPP) for maximizing the energy capture.

Both tasks must be made at the highest possible efficiency, over a wide power range, due to the morning-noon-evening and winter-summer variations. The MPP is tracked by means of a MPP Tracker (MPPT) device.

The power injected into a single-phase grid follows a sinusoidal waveform raised to the second power, if the voltage and the current are in phase and with no harmonics (the power injected into a three-phase grid is constant). The PV module cannot be operated at the MPP if this alternating power is not decoupled by means of an energy buffer, as will be seen later on in chapter 2.

Finally, the current injected into the grid must obey the regulations, such as the EN61000-3-2 [3] and the IEEE std. 1547 [4], which state the maximum allowable amount of injected current harmonics. Besides these regulations, inverters intended for grid operation must also include a device for determining the state of islanding operation, which is not allowed due to personnel safety [5].

1.2.1 The Past

The past technology, illustrated in Figure 1.6-a, was based on centralized inverters, which interfaced a large number of modules to the grid [6]. The PV modules were divided into series connections (called a string), each generating a sufficient high voltage to avoid further amplification. These series-connections were then connected in parallel, through string-diodes, in order to reach high power-levels.

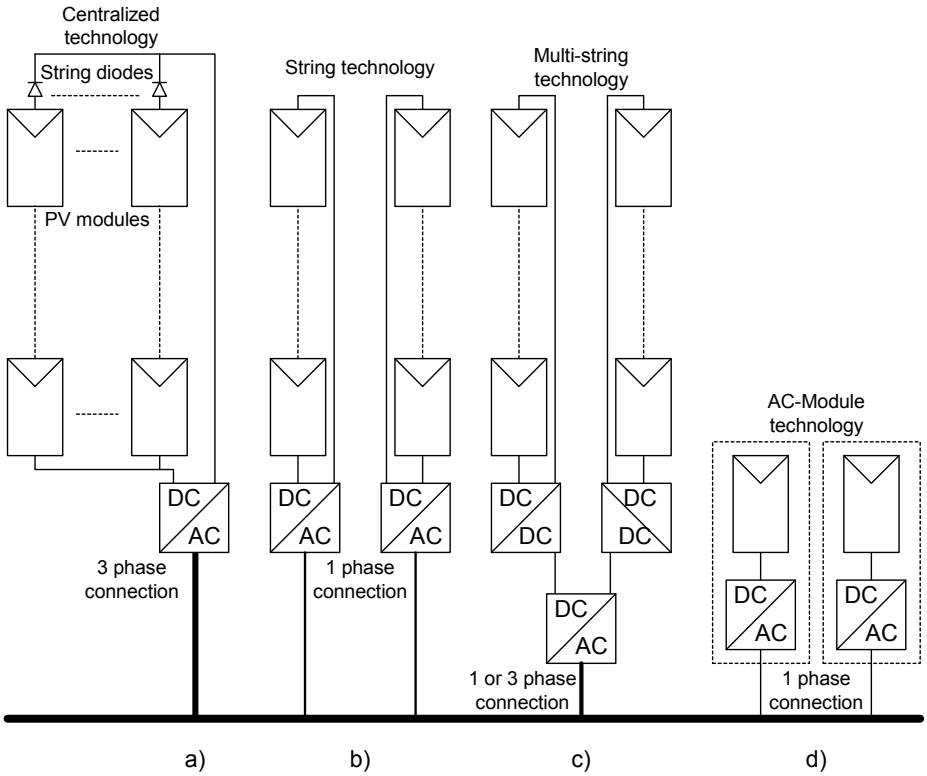

Figure 1.6. Photovoltaic system technologies. A) Past centralized technology, b) Present string technology, c) Present multi-string technology, d) Latest AC-Module technology.

This results in some limitation, such as: high voltage DC cables between the PV modules and the inverter, power losses due to a centralized MPPT, mismatch losses between the modules, losses in the string diodes, risk of hotspots in the PV modules during partial shadow, and individual design for each installation. Thus, a non-flexible design is achieved, and the benefits of mass-production cannot be reached.

1.2.2 The Present

The string inverter, shown in Figure 1.6-b, is a reduced version of the centralized inverter, where a single string of PV modules is connected to the inverter [7]. The input voltage may be high enough to avoid voltage amplification. This requires roughly 15 modules in series for European systems. The total open-circuit voltage for 15 PV modules may reach as much as 700 V, which calls for 900 V MOSFETs/IGBTs in order to allow for a 75% voltage de-rating of the semiconductors. The normal operating voltage is however as low as 375 V to 525 V.

There are no losses associated with string-diodes and a separate MPPT can be applied for each string. This is assumed to increase the overall efficiency, when compared to the centralized inverter.

1.2.3 The Future

The multi-string inverter, depicted in Figure 1.6-c, is a further development of the string-inverter, where several strings are interfaced with their own DC-DC converter to a common DC-AC inverter [7], [8], [9]. This is beneficial, compared with the centralized system, since every string can be controlled individual. Thus, the operator may start his/her own PV power plant with a few modules. Further enlargements are easily done because a new string can be plugged into the existing platform. A flexible design with high efficiency is hereby achieved.

The AC-module in Figure 1.6-d is a reduction of the string inverter, where each PV module has its own integrated power electronic interface to the utility [10], [11]. The power loss of the system is reduced due to removing the mismatch between the modules, but the constant losses in the inverter may be the same as for the string inverter. Also the AC-module concept supports optimal operation of each module, which leads to an overall optimal performance. Moreover, it has the possibility to be used as a plug-in device by individuals without specialized knowledge.

The definition of the AC-module is given as [3]:

"An AC-module is an electrical product and is the combination of a single module and a single power electronic inverter that converts light into electrical alternating (AC) power when it is connected in parallel to the network. The inverter is mounted on the rear side of the module or is mounted on the support structure and connected to the module with a single point to point DC-cable. Protection functions for the AC side (e.g. voltage and frequency) are integrated in the electronic control of the inverter."

Table 1.1 compares the performance among seven commercial AC-module inverters. The evaluation shows that all inverters show excellent grid performance in terms of a high power factor. Another important issue is the capability to convert the low irradiation power into electric power. Table 1.1 also shows that the start-up power is located in the span from 0.15 W to 2.5 W. The power consumption during nighttime is also very low. These entries together with high efficiencies and high power density indicate a high level of knowledge about the design giving parameters.

Finally, the single cell converter system is the case where one large PV cell is connected to a DC-AC converter [12], [13]. This is beneficial for the thin-film types of PV cells, including the photo electro chemical cells [14], which can be made arbitrary large by an inexpensive "roll on – roll off" process. The main difficulty in realizing such an inverter is that the input power may reach 100 Watt per square meter cell at 1 Volt (or less) across the terminals!

Table 1.1. Performance comparison for commercial AC-module inverters. HF = high frequency and LF = low frequency transformer or power stage. Sources: www.dorfmueller-solaranlagen.de, www.dde.nl, www.mastervolt.com, www.nkf.nl, www.solar.philips.com, and www.ascensiontech.com.

Vendor	DORF-MÜLLER	EXENDIS	MASTER-VOLT	NKF	PHILIPS	MASTER-VOLT	ASCEN-SION-TECH
Type	DMI 150/35	GRIDFIT 250	SOLADIN 120	OK4E	PSI300	SUN-MASTER 130S	SUNSINE 300
Country and year	D1995	NL2002	NL2001	NL1997	NL2004	NL1998	US2000
Nominal PV-power [W]	100	250	90	100	375	110	300
MPP voltage [V]	28-50	27-50	24-40	24-50	45-135	24-40	36-75
Power decoupling	@ PV	@ PV	@ PV	@ PV	?	?	@ PV
Number of stages	HF	HF+LF	HF+LF	2*HF	?	2*HF+?	HF+LF
Transformer	LF	HF	HF	HF	NON	HF	LF
Mass [kg]	2.80	1.50	0.28	0.63	1.50	0.55	~ 50!
Power density [W/cm^3]	0.06	0.17	0.15	0.30	0.12	0.09	0.10
Start-up power [W]	2.5	0.5	0.4	0.15	2.0	0.95	-
Stand-by power [W]	0	0.008	0.05	0.003	0.1	0.08	0.3
EU (E) or max (M) efficiency [%]	89M	90E	91E	91E	93M	92M	90E
Power factor [ ]	>0.99	>0.99	0.99	>0.99	>0.95	0.99	>0.95

According to the definition of the European efficiency [15], the individual efficiencies, at 5%, 10%, 20%, 30%, 50% and 100% of nominal power, are weighted and summed up according to:

$$\eta_{EU} = 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} + 0.10 \cdot \eta_{30\%} + 0.48 \cdot \eta_{50\%} + 0.20 \cdot \eta_{100\%} \qquad (1.1)$$

This is done in order to make a fair comparison of the inverters, under partial load conditions.

1.3 Aims of the Project

1.3.1 Objectives

The main objective for this research project is to develop an inverter for AC module applications. The target is to develop new and cost-effective solutions for injection of electrical power, generated by PV modules, into the grid. The project must result in an inverter for use with a single PV module, approximately from 120 W to 160 W.

The inverter should be made with low-cost, high reliability, and mass-production in mind. The project will end up with an inverter, which can be mass-produced within short time.

1.3.2 Limitations

Focus is put on the power electronic circuits, and not the auxiliary circuits, like switch mode power supply, measuring and protection circuits, and the microcontroller. On the other hand, the auxiliary circuits are all designed and included, in order to make operational prototypes. However, they are not optimized neither in respect to low power consumption nor cost.

1.4 Outline of the Thesis

Chapter 2 – The chapter gives a historical overview of the photovoltaic device. This is followed up by an explanation of it principles of operation. This leads into the electrical and thermal models for the PV cell and module. Finally, the behavior of the PV cell and PV module, during different operating point, are explored.

Chapter 3 – The specifications for the PV module to inverter, and inverter to grid interfaces are given in this chapter. Some specifications regarding safety and compliances are also discussed.

Chapter 4 – The photovoltaic inverter topology overview gives an introduction to different system layouts, and different topologies within the single- and dual-stage DC-AC inverter families. The chapter also includes an estimation of power losses and cost for each topology. The estimations are used to select the final topology.

Chapter 5 – The design of the power-electronic circuits is presented in this chapter. This includes both the DC-DC converter and the DC-AC inverter.

Chapter 6 – The design of the controllers included in the PV inverter is documented in this chapter. They are the Maximum Power Point Tracker, control of PV current, control of intermediate voltage, and control of grid current.

Chapter 7 – The PV inverter is tested, and verified. The tests include the efficiency of the MPPT algorithm (ability to track the MPP), energy efficiency (from PV terminals to grid terminals), and grid performance.

Chapter 8 – Finally, a conclusion on the obtained results is presented. This also includes the novelties within the work, and suggestions for future work.

List of References

Eight appendices, from appendix A to appendix H

Chapter 2

The Photovoltaic Module

The photovoltaic (PV) module is presented in this chapter. The typical PV module is made up around 36 or 72 PV cells in series. The PV cell is basically a large PN junction, which produces electrical DC power, when exposed to sunlight.

2.1 Historical Review, Forecast and Types of PV Cells

The following is based on [1], [16], [17], [18], [19], [20], [21] and [22], where more information also is available.

Edmond Becquerel discovers the photovoltaic-effect in 1839, during an experiment with wet-cell batteries. Willoughby Smith discovered the photoconductivity of selenium in 1873, and three years later in 1876, William Adams and Richard Day discovers the photovoltaic effect in solid selenium. Thus, the road was made ready for the 'modern' PV cell in Figure 2.1 to appear.

Figure 2.1. A modern mono-crystalline silicon PV cell, with a multiple of thin fingers for collecting the free electrons, and two thick bus bars for interconnection.

The modern PV cell, based on the same physical layout as today PV cells, is invented in 1883 by Charles Fritts. The cell was made from a thin disk (wafer) of selenium covered with very thin, semi-transparent, gold-wires. The gold-wires were used to collect the free electrons, generated by the PV effect. The light-to-electrival power efficiency was between 1% and 2%.

The first semiconductor-based transistor was successfully tested on December 24th in 1947 at Bell Labs (discovered by Bardeen, Brattain and Shockley). The first PN junction made from single-crystal grown germanium is made in ‘50 and by silicon in ‘52 (the single-crystal grow technique was developed in 1918 by Czochralski). A few years later, in ‘54, the first silicon PV cell is announced by Chapin, Fuller and Pearson, the efficiency is reported to 4.5% and was raised to 6% within a few months.

The first commercial PV product is launched in ‘55. The price was however very high (1500 USD per watt!), so the first successful demonstration was the Vanguard I satellite in ‘59. Its power systems delivered less than one Watt to the onboard radio. The efficiency is raised to 8%, 9%, 10% and 14% in the years ‘57 to ‘60, all by Hoffman Electronics.

The 60’s is the decade where the PV technology breaks through, and becomes the main power source for many satellites, e.g. the Telstar by Bell Telephone Laboratories is launched with 14 Watt PV cells in ‘62. NASA launches the Nimbus spacecraft equipped with 470 Watt PV array in ’64, and the Orbiting Astronomical Observatory with 1 kW PV array in ’66.

The 70’s is where the price is reduced the most, from 100 USD per watt to 20 USD per watt. This leads to more terrestrial applications, such as lights and horns on offshore oilrigs, lighthouses, and railroad crossings. The first dedicated laboratory for PV is founded in ‘72, at the university of Delaware. One of the first homes completely powered by PV, is build in ‘73 by university of Delaware and surplus electricity is sold to the grid.

The 80’s is where everything accelerates. ARCO solar produces more than 1 MW PV cells in ‘80, being the first in the world. The first megawatt-scale PV plant is made in ‘82 in California, and in ’83 a 6 MW plant is inaugurate, also in California. The worldwide production of PV cells exceeds 21 MW in ’83 and the first silicon PV cell with an efficiency of 20% is developed in ’85.

The 90’s is devoted to the ‘roof-top’ programs, e.g. the Danish SOLBYEN (60 kW), SOL 300 (750 kW), and SOL 1000 (≈1 MW), the 100 000 roof program (≈ 100 MW) in Germany, the Million Solar Roofs in the US, and many more. Besides these programs, the efficiency of CdTe thin film PV cells are raised to 15.9% in ’92, and the gallium indium phosphide and gallium arsenide PV cells reaches 30% efficiency in ’94.

Increasing efficiencies, new technologies and price reduction in materials and production will lead to a future, where PV power will be price competitive with conventional power sources, such as oil, coal, natural gas, etc. A price reduction of 50% is possible over the next seven years [23].

Table 2.1. Status of the most common PV technologies. The efficiency survey covers the typical and maximum efficiency for commercial available PV modules, and maximum recorded laboratory efficiencies in year 2002. The PV module production in IEA countries is also given for year 2002.

	Silicon			Thin film	
Efficiency:	Mono crystalline	Multi crystalline	Thin film amorphous	CIS	CdTe
Typical	12% - 15%	11% - 14%	5% - 7%	-	-
Maximum	22.7%	15.3%	-	10.5%	12.1%
Laboratory	24.7%	19.8%	12.7%	16.0%	18.2%
Production in 2002 (IEA)	161 MW	244 MW	20 MW	Total 37 MW	

Table 2.1 reveals that the most efficient technology is the mono-crystalline silicon PV cell. This is due to a low rate of re-combination of holes and electrons, within the PN junction. The mono-crystalline PV cells are also more costly when compared to the multi-crystalline PV cells. This is due to the manufacture process of the mono-crystalline silicon, which are rather expensive.

Table 2.2. Typical data for some PV modules, at Standard Test Condition (STC)[2]. This is only a short list. More information can be found oh the manufactures homepages. See [24] for a comprehensive list (more than 60) of manufactures.

Technology and module type	Mono crystal-line BP4160	Multi crystal-line BP3160	CIS ST40	CdTe FS55
Nominal power at MPP	160 W	160 W	40 W	55 W
Voltage at MPP - U_{MPP}	35.4 V	35.1 V	16.6 V	60 V
Current at MPP - I_{MPP}	4.52 A	4.55 A	2.41 A	0.92 A
Short circuit current - I_{SC}	4.9 A	4.8 A	2.68 A	1.09 A
Open circuit voltage - U_{OC}	44.2 V	44.2 V	23.3 V	88 V
Temperature coefficient of short circuit current	0.065 %/K (3.19 mA/K)	0.065 %/K (3.12 mA/K)	0.013 %/K (0.35 mA/K)	0.04 %/K (0.44 mA/K)
Temperature coefficient of voltage	-0.45 %/K (-160 mV/K)	-0.46 %/K (-160 mV/K)	-0.60 %/K (-100 mV/K)	-0.22 %/K (-130 mV/K)
Temperature coefficient of power	-0.5 %/K (-0.80 W/K)	-0.5 %/K (-0.80 W/K)	-0.6 %/K (-0.24 W/K)	-0.25 %/K (-0.14 W/K)
Nominal Operating Cell Temperature	47 °C	47 °C	47 °C	45 °C
Area of PV cells (not entire module)	1.12 m^2	1.18 m^2	0.36 m^2	0.72 m^2
Estimated efficiency, based on area and STC	14.3%	13.6%	11.1%	7.6%
Number of cells in series	72	72	36	(guess: 118)
Diode quality factor	1.86			5.15
Reverse saturation current	13.0 μA			3.90 mA

[2] Standard Test Condition (STC) is defined as 25 °C cell temperature, 1000 W/m^2 sunlight intensity, and an air mass 1.5 solar spectral content

Table 2.2 shows the parameters for 4 typical PV modules (based on four different technologies). The largest difference between the technologies is the temperature coefficients, which is largest for the silicon-based and lowest for the CdTe-based PV modules. Besides this, and without knowing the number of cells in the CIS and CdTe modules, the voltage generated across the CdTe cells are higher than the voltage over the silicon cells.

2.2 Operation of the PV Cell

A PV cell is basically a large silicon PN junction (diode), cf. Figure 2.2. The incoming of a photon makes the current flow: the PN junction has become a PV cell.

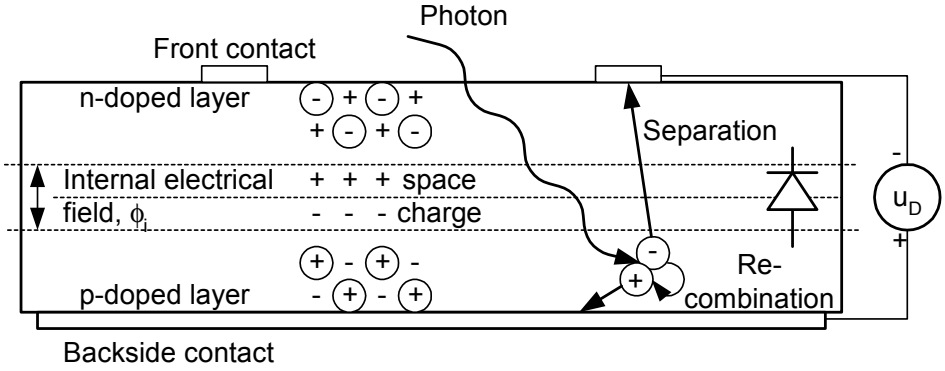

Figure 2.2. Cross section of an abrupt PN junction [25] (including integrated diode) and processes occurring in an irradiated PV cell [26].

The silicon atom contains four electrons in the outer shell. The electrons are a part of the electron pairs binding with four other silicon atoms. By doping the silicon with boron (p-doped), which has only three electrons in the outer shell, the silicon becomes electron deficit. Thus, a 'hole' is present in the silicon lattice, and positive charges may move around in the lattice. When doped with phosphorus (n-doped), which have five electrons in the outer shell, the silicon becomes electron saturated. These extra electrons are also free to move around in the lattice.

The PN junction, where the two alloys meets allows free electrons in the n-doped layer to move into the holes in the p-doped layer. An internal field is being build and the electrons can no longer force the junction, thus the layers have reached equilibrium. The amplitude of the built-in potential is [27]:

$$\phi_i = \frac{k \cdot T_{cell}}{q} \cdot \ln\left(\frac{N_a \cdot N_d}{{n_i}^2}\right), \tag{2.1}$$

where N_a and N_d is the acceptor and donor doping densities respectively, and n_i is the intrinsic carrier density, which do not contain boron or phosphorus. The constant k is Boltzmanns ($13.8 \cdot 10^{-24}$ J/K), q is the electron charge ($160 \cdot 10^{-21}$ C), and T_{cell} is the absolute cell temperature.

An incoming photon may ‘knock’ off a carrier from the p-layer, which leaves a free hole, and the carrier is moving around in the p-layer. If the carrier reaches the PN junction before recombination, the internal field causes it to move into the n-layer. On the other hand, the carrier may be a victim of recombination before it can reach the junction, thus it will not assist the current generation. Recombination is caused by irregularities in the lattice, impurities in the material, or simply coincidence! Once the electron has forced the PN junction, is has two possible return paths. The electron can either pass through the PN junction (which then works as a diode) or it can pass through an auxiliary circuit, the load.

The minimum energy required to release a carrier from the p-layer are in the span E_{gap} = 0.2 to 3.7 eV [25], which varies along with material, temperature, quantity of doping and layout of the PN junction. The empirical formula in (2.2) describes the band gap energy [27]:

$$E_{gap} = E_{gap(0)} - \frac{\alpha \cdot T_{cell}^{\ 2}}{\beta + T_{cell}}, \tag{2.2}$$

where $E_{gap(0)}$ is the band gap energy at 0 K, α and β are some constants, the values are given in Table 2.3.

Table 2.3 Parameters describing the band gab energy as function of temperature.

	Germanium	Silicon	Ga As	CIS	CdTe
Egap (0) [eV]	0.74	1.17	1.52	-	-
α [meV/K]	0.48	0.47	0.54	-	-
β [K]	235	636	204	-	-
Egap at 25 °C [ev]	0.67	1.11	1.40	1.01	1.44

The energy of an incoming photon is:

$$E_{photon} = h \cdot f = \frac{h \cdot c}{\lambda}, \tag{2.3}$$

where h is the Planck constant ($h = 66.3 \cdot 10^{-33}$ J·s = $4.14 \cdot 10^{-15}$ eV·s, 1 eV = $160 \cdot 10^{-21}$ J), f is the frequency of the incoming photon, c is the speed of light ($c = 300 \cdot 10^{6}$ m/s), and λ is the wavelength (80% of the suns spectrum is between 400 nm to 1500 nm). The energy-span for a ‘normal’ photon is therefore in the span from 0.83 eV to 3.10 eV. The requirement for excitation of an electron, into the n-doped layer, is that the energy of the incoming photon is larger than the energy needed for the electron to overcome the PN junction.

Because some of the photons have energy lower than the required, these do not assist the carrier generation. Thus, the energy associated with these photons is transformed into heat. The photons that have energy larger than required, are the current generating ones. The scenarios are summarized below.

1) The photon is reflected at the surface,
2) The photon passes through the PV cell,
3) $E_{photon} < E_{gap} \Rightarrow$ The photon is transformed into heat,
4) $E_{photon} = E_{gap} \Rightarrow$ A free carrier is generated,
5) $E_{photon} > E_{gap} \Rightarrow$ Free carrier + heat.

2.3 Model of the PV Cell

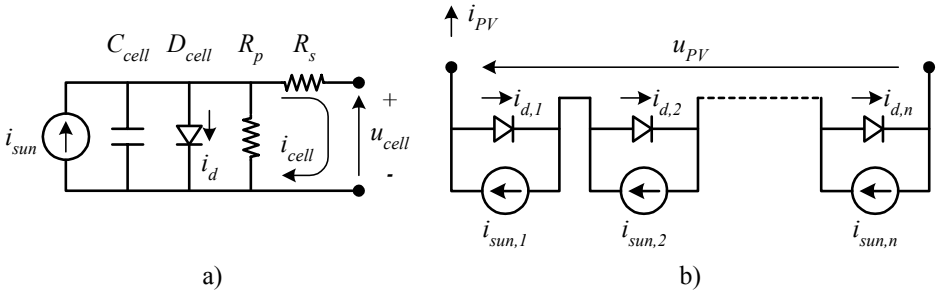

Figure 2.3. Electrical model of a PV cell (a), and of a PV module made up around n cells (b).

An electrical model of the PV cell is shown in Figure 2.3-a. The PV module is composed of n of these cells in series, as shown in Figure 2.3-b, in order to reach a high voltage at the terminals. The connection of PV cells in series is named a string.

From Figure 2.3-b and the theory of superposition, it becomes clear that the current generated by the PV module is determined by the lowest i_{sun}, this is the principle of the weakest link. Thus, care must be taken when selecting the PV cells for a PV module, so that the cells are equal.

2.3.1 Light Dependent Current Source

The current source in Figure 2.3, i_{sun}, is proportional to the amount of irradiation, and linear with respect to the PV cell temperature. According to (2.2), an increase in temperature involves a decrease in band gap energy, which result in more current generated by the incoming photons. The current is given as [28]:

$$i_{sun} = \left(i_{sun,STC} + k_{temp} \cdot \left(T_{cell} - T_{cell,STC}\right)\right) \cdot \frac{P_{sun}}{P_{sun,STC}}, \tag{2.4}$$

where i_{sun} and $i_{sun,STC}$ is the short circuit current at the given working point and STC, respectively. The constant k_{temp} is the temperature coefficient of i_{sun}. T_{cell} and $T_{cell,STC}$ are the actual and STC cell temperatures, respectively. Finally P_{sun} and $P_{sun,STC}$ are the irradiations at the present operating point and at STC, respectively.

2.3.2 Diode

The current through the diode, i_d, is described by the well-known diode-equation:

$$i_d = i_{rs} \cdot \left(\exp\left(\frac{q \cdot u_d}{k \cdot A \cdot T_{cell}} \right) - 1 \right), \tag{2.5}$$

where i_{rs} is the reserve saturation current, A is the diode quality factor (normal defined between 1 to 5), and u_d is the voltage across the diode. The reverse saturation current increases with temperature. This must be included in order to make a precise model of thermal effects. The reverse saturation current can be modeled as:

$$i_{rs} = i_{rs,STC} \cdot \left(\frac{T_{cell}}{T_{STC}} \right)^3 \cdot \underbrace{\exp\left(\frac{E_{gap}(\cdot q)}{k \cdot A} \cdot \left(\frac{1}{T_{STC}} - \frac{1}{T_{cell}} \right) \right)}_{Arrhenius}, \tag{2.6}$$

where $i_{rs,STC}$ is the reverse saturation current at STC [28]. Please note that the equation given in [28] and many others references includes q (the electron charge) in the Arrhenius part of (2.6), shown by (·q). This is done to convert the gap energy from electron volts (eV) to Joules (J).

2.3.3 Resistances

The two resistors included in the model, R_s, and R_p, describe the power losses due to resistance in the current-collecting bus-bars, fingers and connections between modules and the inverter, the purity of the semiconductor material and the regularity of the semiconductor lattice. The parallel resistance is high; it does therefore not have much influence on the PV cell characteristic. The size of the series resistance is measured in [29] and [30] to approximately 1 Ω for a 72 cells module, which corresponds to 14 mΩ per cell. The power loss per cell is therefore computed to: $(4.52\ A)^2 \cdot 14\ m\Omega = 0.28$ W per cell, or 20 W for the entire module (the value of the current is from Table 2.2).

The small-signal impedance per PN junction is computed from (2.5) and (2.10) as $- du_{PV} / di_{PV}$, neglecting resistive, inductive and capacitive elements:

$$R_{PN} = -\frac{du_{PV}}{di_{PV}} = \frac{k \cdot A \cdot T_{cell}}{q \cdot (I_d + i_{rs})} = \frac{k \cdot A \cdot T_{cell}}{q \cdot ((i_{sun} - i_{cell}) + i_{rs})} \approx \frac{k \cdot A \cdot T_{cell}}{q \cdot (i_{sun} - i_{cell})}, \tag{2.7}$$

which is the same as U_{MPP} / I_{MPP} at the maximum power point.

2.3.4 Capacitance

The two layers of the PN junction form a capacitor. If the layers are regarded as being a plate capacitor without end-effects, the capacitance can be stated as:

$$C_{cell} = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A_{disc}}{d}, \tag{2.8}$$

where ε_0 is the permittivity (dielectric constant) of free space ($8.85 \cdot 10^{-12}$ F/m), ε_r is the relative permittivity of the semiconductor material (11.7 for silicon), A_{disc} is the area of the discs and d is the distance between the two discs. The area of the discs is easily measured with a ruler, but the distance between the two plates is more difficult to measure! The distance depends on the applied voltage, doping, and temperature. However, the junction capacitance can be estimated as [27]:

$$C_{cell} = A_{disc} \cdot \sqrt{\frac{1}{2} \cdot \frac{q \cdot \varepsilon_0 \cdot \varepsilon_r}{\phi_i - u_d} \cdot \frac{N_a \cdot N_d}{N_a + N_d}}. \tag{2.9}$$

Assuming a cell temperature of 300 K, $N_a = 10^{18}$ cm^{-3}, $N_d = 10^{16}$ cm^{-3}, $n_i = 10^{10}$ cm^{-3}, the amplitude of the internal field is given by (2.1) to 0.833 V. If the PV cell is operated at MPP, around 0.492 V, and the size of the PV cell is 6" in diameter (standard silicon wafer size), the junction capacitance equals 9.0 µF per cell, and 9.0 µF / 72 = 125 nF per module.

2.3.5 Electrical Circuit

The final model of the PV cell can then be established. The current through the terminals of the PV cell is given by (2.10), assuming infinite parallel resistance. The voltage across the PN junction is given by (2.11) and finally the power generated by the PV cell is given in (2.12).

$$i_{cell} = i_{sun} - i_d, \tag{2.10}$$

$$u_d = u_{cell} + R_s \cdot i_{cell}, \tag{2.11}$$

$$p_{cell} = u_{cell} \cdot i_{cell}. \tag{2.12}$$

The following procedure is advised to find the parameters describing the steady state operation of a PV cell (neglecting resistances). Obtain the following parameters from the datasheet or measurements, see also Table 2.2: nominal power at MPP, voltages and currents at MPP and open/short circuit conditions, and the temperature coefficient for the short circuit current. The number of cells in series and parallel are also of interest in order to determine the properties per cell (normally 36 or 72 cell in series, and only one string per PV module) and the used semiconductor material (determines the band gap energy).

The STC reverse saturation current and diode quality factor can then be extracted from (2.5) and (2.10), assuming no series resistance, as:

$$\begin{bmatrix} \ln\left(i_{rs,STC}\right) \\ \left(\frac{q}{k \cdot A \cdot T_{cell}}\right) \end{bmatrix} = \begin{bmatrix} 1 & U_{MPP} \\ 1 & U_{OC} \end{bmatrix}^{-1} \cdot \begin{bmatrix} \ln\left(I_{SC} - I_{MPP}\right) \\ \ln\left(I_{SC}\right) \end{bmatrix} \tag{2.13}$$

where I_{SC} is the short-circuit current, U_{OC} is the open-circuit voltage, both recorded at STC.

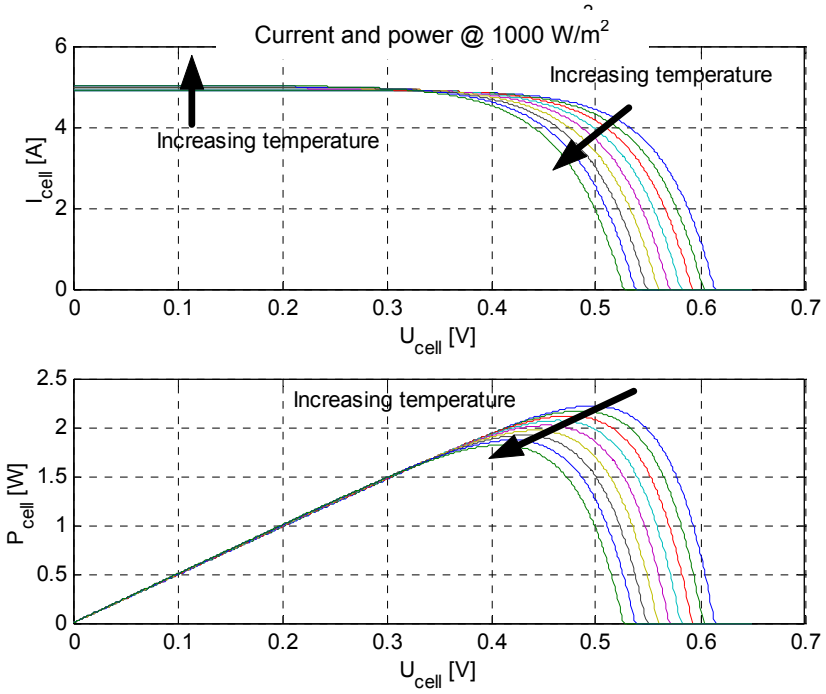

Figure 2.4. Computed current and power characteristic for the BP4160 module, at fixed irradiation and different cell temperatures (from 25 ℃ to 65 ℃ in steps of 5 ℃).

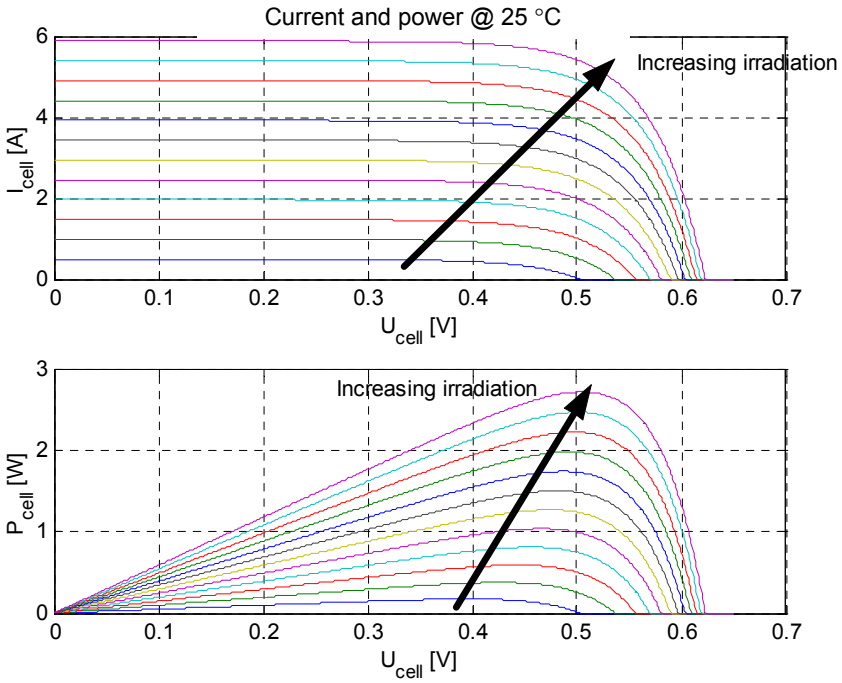

Figure 2.5. Computed current and power characteristic for the BP4160 module, at fixed cell temperature and different irradiations (from 100 W/m^2 to 1200 W/m^2 in steps of 100 W/m^2).

Thus, the parameters for the BP4160 module are: diode quality factor A = 1.86, and reverse saturation current $I_{RS,STC}$ = 13.0 μA. The model predicts an open circuit and MPP voltages of 44.2 V and 35.8 V, respectively, and a MPP power of 160.1 W which are very close to the values given in Table 2.2, thus the achieved values are accepted.

Two plots are given in Figure 2.4 and Figure 2.5, showing the computed results when using the models given in equations (2.4) to (2.6), and (2.10) to (2.13).

2.3.6 Thermal Modeling

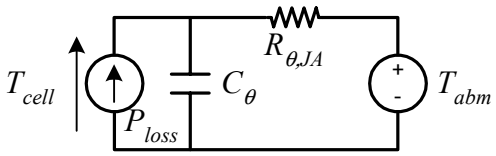

Figure 2.6. Simplified thermal model of a PV module.

A simple thermal model of the PV cell is shown in Figure 2.6. The cell temperature can be modeled as:

$$T_{cell,Ploss} = P_{loss} \cdot \frac{R_{\theta,JA}}{s \cdot R_{\theta,JA} \cdot C_\theta + 1}, \tag{2.14}$$

$$T_{cell,Tabm} = T_{abm} \cdot \frac{1}{s \cdot R_{\theta,JA} \cdot C_\theta + 1}, \tag{2.15}$$

$$T_{cell} = T_{cell,Ploss} + T_{cell,Tabm}, \tag{2.16}$$

$$T_{cell} = \frac{P_{loss} \cdot R_{\theta,JA} + T_{abm}}{s \cdot R_{\theta,JA} \cdot C_\theta + 1}, \tag{2.17}$$

where P_{loss} is the heat generating power, $R_{\theta,JA}$ is the thermal resistance from the junction to the ambient, C_θ is the thermal capacitance, T_{abm} is the ambient temperature, and s is the Laplace operator. The steady state version of equation (2.17) dictates that the cell temperature is equal to the ambient temperature plus an amount from the 'lost' power and thermal resistance. The heat generating power is equal to

$$P_{loss} = P_{sun} - P_{PV}, \tag{2.18}$$

where P_{PV} is the power generated by the PV module. Thus, the size of the thermal resistance can then be estimated by the Nominal Operating Cell Temperature (NOCT[3]) conditions as

$$R_{\theta,JA} \approx \frac{T_{cell,NOCT} - T_{abm,NOCT}}{P_{sun,NOCT}}. \tag{2.19}$$

[3] NOCT – Nominal Operating Cell Temperature is defined as the equilibrium cell junction temperature corresponding to an open-circuited module operating in a reference environment of 800 W/m^2 irradiance, 20 °C ambient air temperature with a 1 m/s wind across the module from side to side.

Applying the data for the BP 4160 module from Table 2.2, the thermal resistance is estimated to (47 °C – 20 °C) / 800 W = 0.034 K/W. The BP 4160 PV module is laminated with glass and Ethylene Vinyl Acetate - EVA. The computed/predicted thermal resistance for a glass and Tedlar laminated PV module is 0.029 K/W in [31]. The prediction is based on the conduction and convection heat transfer theory of the PV module, together with ambient- and sky-temperatures and wind speed. The two values are rather close to each other, thus the applied model is assumed valid.

The size of the thermal capacitance, C_θ, is unknown. It can be estimated when knowing which materials are used to form the PV module and their physical properties and dimensions. A rough estimation predicts a thermal time-constant of approximately 5 minutes. The size of the thermal capacitance can then be estimated to 300 s / 0.034 K/W ≈ 10 000 W·s/K.

2.4 Behavior of the PV Module

2.4.1 Partial Shadow

As seen in Figure 2.3-b, the PV module applies to the weakest-link principle. What Figure 2.3 does not show is the avalanche breakdown phenomenon of the PV cell.

The avalanche current can be calculated as

$$i_{d,avalanche} = -I_{rs,r} \cdot \left(\exp\left(q \cdot \frac{u_{d,avalanche} - u_d}{k \cdot A \cdot T_{cell}} \right) - 1 \right) \tag{2.20}$$

where $I_{rs,r}$ is the reverse-bias saturation-current [32]. Another approach is given in [33]. Hence, if one of the PV cells in Figure 2.3-b is shadowed, then it will be reversed biased and an avalanche current will start to flow, if the reverse voltage is high enough. This does not damage the PV cell, but it starts to dissipate power, being a load! If the PV module output current remains constant, the temperature of the shadowed cell may increase beyond the melting point of the laminate. The current should therefore be decreased in order to lower the risk of de-lamination [34]. The temperature can actually reach as much as 170 °C, which is very close to the damaging temperature of silicon.

A solution is to include bypass-diodes in the PV module. Normally, one diode is used to bypass 20 to 40 PV cells. These bypass diodes are implemented with discrete components in the junction box, on the rear side of the PV module. A better, and still more expensive, solution would be to bypass each PV cell with a separate diode [34]. This diode could be implemented in the same silicon wafer as the PV cell. Next are three cases shown, where the PV modules are partially shaded.

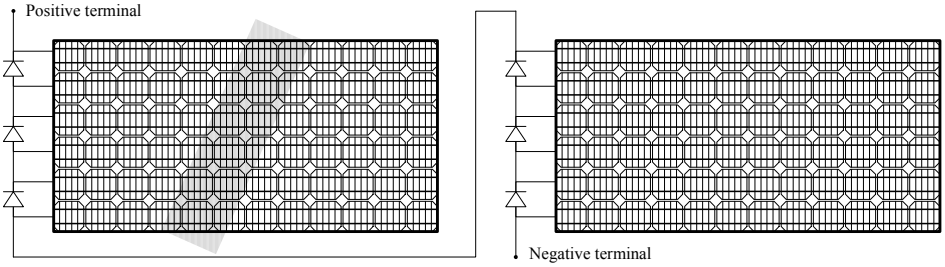

*Figure 2.7. Model of two 6*12 = 72-cell PV modules, each with three bypass-diodes mounted in the junction box, and partial shadow covering part of the first PV module.*

All calculations are made in PSPICE, using the established models in Figure 2.3, equations (2.4) to (2.6), and (2.10) to (2.13), and Figure 2.7. The shadow covering the PV module is assumed being a lamppost, rod or similar. Thus, the shadowing of Figure 2.7 is applied, that is:

The surface of one cell in each row (only for one PV module, 6 PV cells) is fully shadowed, where the intensity of the shadow is between 0 and 1. Zero is the case where all the light is passed through the rod –the rod is removed! A shadow-factor between 0 and 1 is the case where the rod is semi-transparent (a typical value is 0.7, measured with a pyranometer), and a shadow-factor equal to 1 for complete shadow (zero light) behind the rod. One quarter of the surfaces of the two neighbour cells is also covered with shadow, in total 12 PV cells.

Thus, the short circuit current for each type of shadow are given as

$$S = 1 - \frac{Irradiation_{behind}}{Irradiation_{before}} \tag{2.21}$$

$$i_{sun,noshadow} = I_{sun}, \tag{2.22}$$

$$i_{sun,25\%shadow} = I_{sun} \cdot (1 - 0.25 \cdot S), \tag{2.23}$$

$$i_{sun,100\%shadow} = I_{sun} \cdot (1 - S), \tag{2.24}$$

where S is the amount of shadow. The breakdown voltage in (2.20) is assumed equal to –20 V pr PV cell [35].

The results are tabulated in Table 2.4 for all three combinations, and the voltage-power characteristics are further depicted in Figure 2.8 for the 1 diode per cell approach. Table 2.4 shows that even a small reduction of incoming irradiation results in a huge reduction on the available power at the MPP. The reduction in power generation is only apparent, since the non-shadowed cells still generates full power, but the power is consumed in the shadowed PV cells.

Table 2.4. Results from the PSPICE simulations. The power tabulated, is the available power at MPP when one of the two PV modules is partial shadowed.

Scheme \ Shadow	0%	20%	40%	60%	80%	100%
Amount of incoming light	100%	98.8%	97.5%	96.3%	95.0%	93.8%
No diodes	320 W	294 W	231 W	157 W	77 W	0 W
1 diode pr 24 cell, as Fig. 2.7.	320 W	294 W	231 W	157 W	144 W	142 W
1 diode pr cell	320 W	294 W	275 W	265 W	254 W	240 W

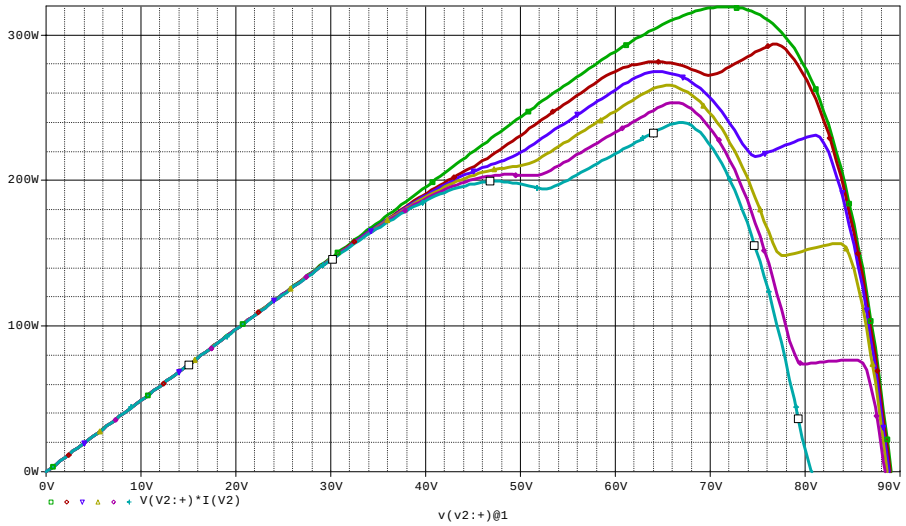

Figure 2.8. Power versus voltage plot for the cases where each PV cell is bypassed with a diode. Note the regularity of the non-shaded curves, compared to the shadowed ones.

For example, in the case of 80% shadow of the cells, the total generated electrical power is equal to 304 W. When no bypass-diodes is applied the 18 shadowed cells start to consume 227 W of the generated power, thus only 77 W is available at the terminals. When one diode is applied for each 24 PV cells, the available power increases to 144 W, thus 160 W is lost in the shaded cells. Finally, when the 1 diode per cell scheme is applied, 'only' 64 W is wasted into heat.

Another problem regarding partial shadow is the irregularity of the power curves in Figure 2.8. Some MPPT algorithms use a 'perturb and observe' approach, starting from no-load, see chapter 6. Thus, they might end up finding a local and not the global MPP, leading to a further reduction in generated power. Other types of MPPT algorithms use the derivative of the generated power when changing the voltage. The derivative is equal to zero at the MPP. Once again, these algorithms may fail due to the presence of several zeros in the derivative! This will be treated later on in the chapter 6.

2.4.2 Ripple in Voltage and Current

The PV cell, and module, is hypersensitive to ripple in the output current and voltage. The ripple does not damage the PV cell, but it reduces the available power dramatically, see Figure 2.9.

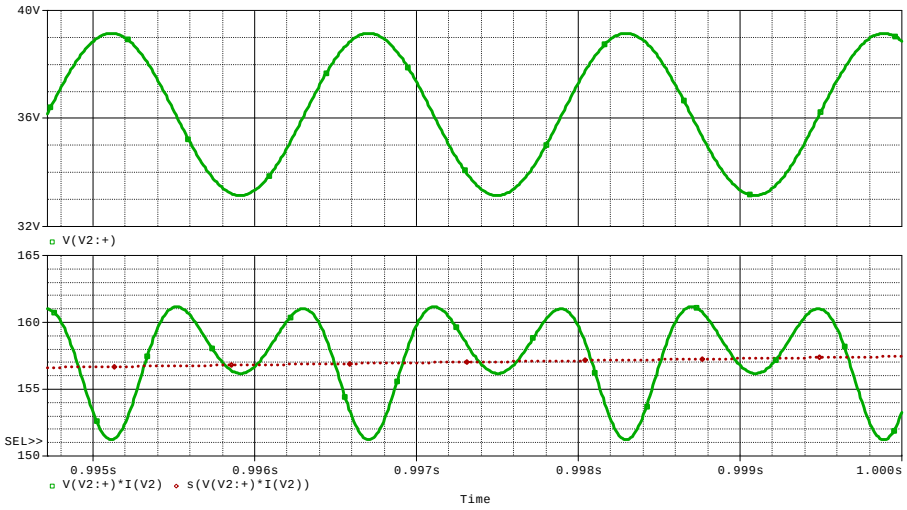

Figure 2.9. PSPICE simulation of the BP4160 module exposed to 3 V ripple. The upper plot shows the terminal voltage, which varies around the MPP voltage, with 3.0 V. The lower plot shows the corresponding instantaneous power (the full line), and the averaged power (the dotted line).

The current generated by the PV module is in the next approximated by a second order Taylor polynomial. The approximation is applied, in order to get around the integral of exp(sin(ω·t)), when combining equations (2.5), (2.10)-(2.12), (2.25), and(2.26).

Assuming that the PV module is operated around the MPP. The PV voltage and current can then be stated as:

$$u_{PV} = U_{MPP} + \tilde{u}, \tag{2.25}$$

$$\tilde{u} = \hat{u} \cdot \sin(\omega \cdot t), \tag{2.26}$$

$$i_{PV} = \alpha \cdot u_{PV}^{\,2} + \beta \cdot u_{PV} + \gamma, \tag{2.27}$$

$$i_{PV} = I_{MPP} + \tilde{i}. \tag{2.28}$$

where α, β and γ are the parameters describing the second order Taylor approximation, and ω is the angular frequency of the ripple (equal to two times the grid frequency for most single stage inverters). The power generated by the PV module is given as the product between voltage and current:

$$p_{PV} = u_{PV} \cdot i_{PV}, \tag{2.29}$$

$$p_{PV} = \left(U_{MPP} + \tilde{u}\right) \cdot \left(I_{MPP} + \tilde{i}\right), \tag{2.30}$$

$$p_{PV} = \left(U_{MPP} + \tilde{u}\right) \cdot \left(\alpha \cdot \left(U_{MPP} + \tilde{u}\right)^2 + \beta \cdot \left(U_{MPP} + \tilde{u}\right) + \gamma\right), \tag{2.31}$$

$$p_{PV} = \left(U_{MPP} + \hat{u} \cdot \sin(\omega \cdot t)\right) \cdot \left(\alpha \cdot \left(U_{MPP} + \hat{u} \cdot \sin(\omega \cdot t)\right)^2 + \beta \cdot \left(U_{MPP} + \hat{u} \cdot \sin(\omega \cdot t)\right) + \gamma\right) \tag{2.32}$$

Equation (2.32) is averaged over one fundamental period, i.e. T = 2π / ω, in order to find the average power generated by the PV module.

$$P_{PV} = \frac{\omega}{2\pi} \int_0^{2\pi/\omega} p_{PV}\, dt, \tag{2.33}$$

$$P_{PV} = P_{MPP} + \frac{(3 \cdot U_{MPP} \cdot \alpha + \beta) \cdot \hat{u}^2}{2}. \tag{2.34}$$

The PV utilization ratio, k_{PV}, is defined as the average generated power divided with the power available at the MPP:

$$k_{PV} = \frac{P_{MPP} + \frac{(3 \cdot U_{MPP} \cdot \alpha + \beta) \cdot \hat{u}^2}{2}}{P_{MPP}}, \tag{2.35}$$

$$k_{PV} = 1 + \frac{3 \cdot U_{MPP} \cdot \alpha + \beta}{2 \cdot P_{MPP}} \cdot \hat{u}^2. \tag{2.36}$$

Finally, the maximum allowable ripple voltage (amplitude, see (2.26)) in order to obtain a utilization ratio of k_{PV} equals:

$$\hat{u} = \sqrt{\frac{(k_{PV} - 1) \cdot 2 \cdot P_{MPP}}{3 \cdot \alpha \cdot U_{MPP} + \beta}} \tag{2.37}$$

Since (2.37) is developed on the basis of a Taylor approximation, attention should be given on the size of û (or k_{PV}). The utilization ratio should not be lower then 0.98, in order to keep the prediction error low. More important is that a low utilization is non-desirable, while it decreases the overall yield.

The parameters describing the second order Taylor approximation is easily derived from (2.5) and (2.10), assuming negligible resistances:

$$\alpha = \frac{1}{2} \cdot \frac{d^2 I_{MPP}}{d U_{MPP}^2}, \tag{2.38}$$

$$\beta = \frac{d I_{MPP}}{d U_{MPP}} - 2 \cdot \frac{1}{2} \cdot \frac{d^2 I_{MPP}}{d U_{MPP}^2} \cdot U_{MPP}, \tag{2.39}$$

$$\gamma = \frac{1}{2} \cdot \frac{d^2 I_{MPP}}{d U_{MPP}^2} \cdot U_{MPP}^2 - \frac{d I_{MPP}}{d U_{MPP}} \cdot U_{MPP} + I_{MPP}, \tag{2.40}$$

$$I_{MPP}(U_{MPP}) = i_{sun} - i_{rs} \cdot \left(\exp\left(\frac{q \cdot U_{MPP}}{k \cdot A \cdot T \cdot n} \right) - 1 \right), \tag{2.41}$$

$$\frac{d I_{MPP}}{d U_{MPP}} = -i_{rs} \cdot \frac{q}{k \cdot A \cdot T \cdot n} \cdot \exp\left(\frac{q \cdot U_{MPP}}{k \cdot A \cdot T \cdot n} \right), \tag{2.42}$$

$$\frac{1}{2} \cdot \frac{d^2 I_{MPP}}{d U_{MPP}^2} = -i_{rs} \cdot \frac{1}{2} \cdot \left(\frac{q}{k \cdot A \cdot T \cdot n} \right)^2 \cdot \exp\left(\frac{q \cdot U_{MPP}}{k \cdot A \cdot T \cdot n} \right). \tag{2.43}$$

where n is the number of PV cells in series.

Table 2.5. Amount of allowable ripple in PV module voltage as a function of permitted power reduction, for two different PV modules (technologies). Parameters for BP4160 mono crystalline: α = -0.0161, β = 1.0276, and γ = -11.7038. Parameters for FS55 CdTe: α = -0.00037, β = 0.0330, and γ = 0.2704.

Specified k_{PV}	0.980	0.985	0.990	0.995	0.999
û for mono-crystalline module (BP4160)	3.00 V	2.60 V	2.12 V	1.50 V	0.67 V
Relative to U_{MPP} (BP4160)	8.5%	7.3%	6.0%	4.2%	1.9%
Value of k_{PV}, simulated in PSPICE (BP4160)	0.977	0.983	0.989	0.994	0.999
û for CdTe module (FS55)	7.70 V	6.66 V	5.44 V	3.85 V	1.72 V
Relative to U_{MPP} (FS55)	12.2%	10.6%	8.7%	6.1%	2.7%
Value of k_{PV}, simulated in PSPICE (FS55)	0.977	0.983	0.989	0.994	0.999

The results in Table 2.5 shows that the BP4160 module may be exposed to a ripple of 6.0% of the MPP voltage, whereas the FS55 may be exposed to 8.7% of the MPP voltage, and still obtain a utilization ratio of 0.99. The difference in allowed ripple is due to the 'square ness' of their power characteristics. The power characteristic for the mono-crystalline module is rather sharp at the MPP, cf. Figure 2.10, whereas for the CdTe module the bend is softer, cf. Figure 2.11.

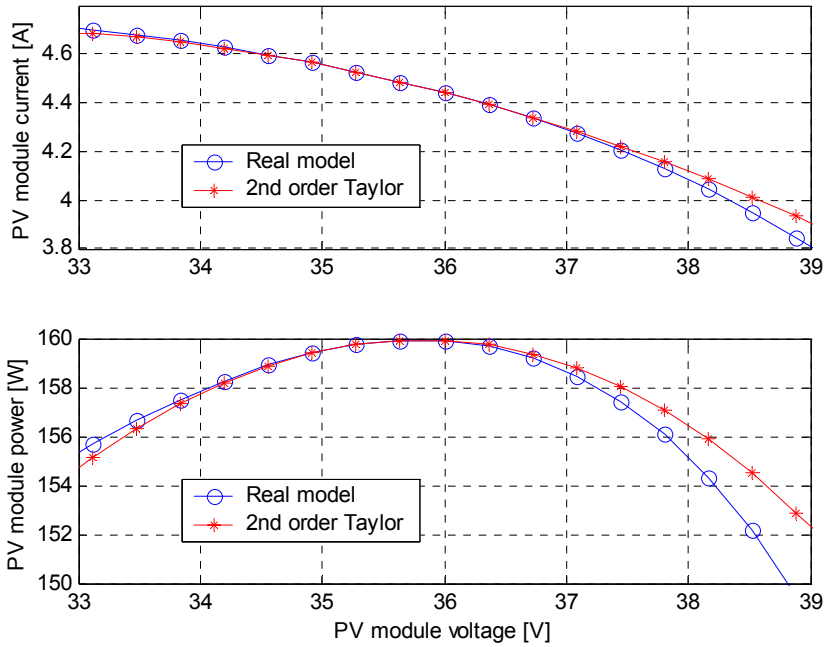

Figure 2.10. Taylor approximation for the BP4160 module. The upper plot shows the real model and the second order Taylor approximation of the PV current, around the MPP. The lower plot shows the corresponding power. Both plots show good agreements between the real model and the second order Taylor approximation.

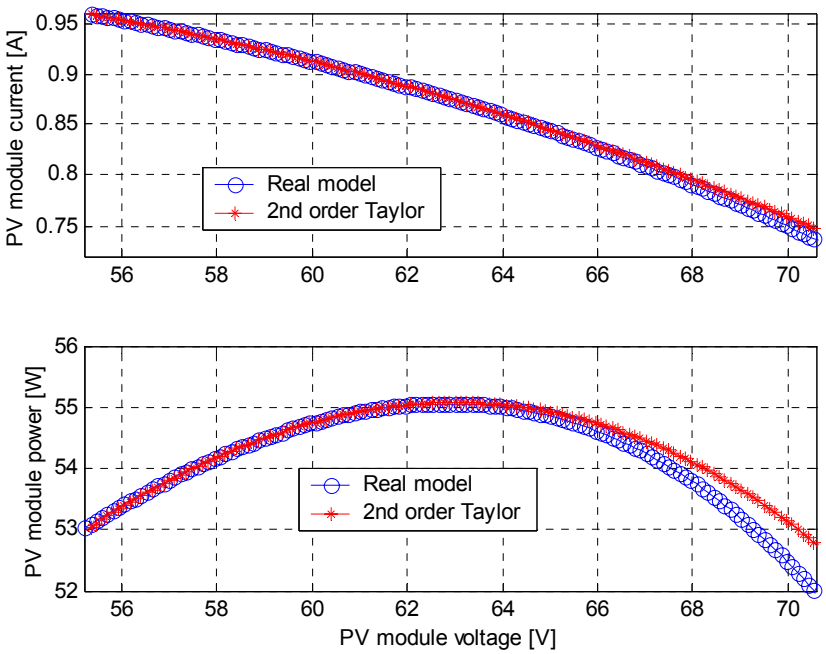

Figure 2.11. Taylor approximation for the FS55 module. The upper plot shows the real model and the second order Taylor approximation of the PV current, around the MPP. The lower plot shows the corresponding power. Both plots show good agreements between the real model and the second order Taylor approximation.

2.4.3 Decoupling Capacitor - C_{PV}

The utilization ratio of the PV module is lowered by the ripple at its terminals, as seen in the previous section. This must be avoided, either with an energy storing capacitor embedded somewhere in the inverter, or by adding a capacitor in parallel with the PV module, C_{PV}. The latter choice is now investigated.

Assuming that the PV module is operated at the MPP, that the voltage across the decoupling capacitor is constant, and that the power into the inverter follows a sinusoidal raised to the second power. The current through the capacitor is then given as:

$$i_{CPV} = I_{MPP} \cdot \left(1 - 2 \cdot \sin^2(\omega \cdot t)\right), \tag{2.44}$$

where ω is the angular frequency of the grid. The voltage across the PV module and the capacitor can be found as $1/C \cdot \int i_C \, dt$:

$$\tilde{u}_C = U_{MPP} + \tilde{u} = U_{MPP} + \frac{I_{MPP}}{C_{PV}} \cdot \int 1 - 2 \cdot \sin^2(\omega \cdot t)\, dt = U_{MPP} + \hat{u} \cdot \sin(2 \cdot \omega \cdot t). \tag{2.45}$$

It can be shown that the voltage reaches maximum at time $\omega \cdot t = \pi/4$. Substituting this into (2.45) yields the amplitude of the small-signal PV module voltage:

$$\hat{u} = \frac{I_{MPP}}{2 \cdot C_{PV} \cdot \omega} = \frac{P_{MPP}}{2 \cdot C_{PV} \cdot \omega \cdot U_{MPP}}. \tag{2.46}$$

The MPP power and voltage is assumed known for the PV module, and the maximum allowable voltage ripple is given by (2.37). Thus, combining (2.37) and (2.46), and solving for the capacitor yields:

$$C_{PV} \geq \frac{P_{MPP}}{2 \cdot \omega \cdot U_{MPP} \cdot \sqrt{\frac{(k_{PV} - 1) \cdot 2 \cdot P_{MPP}}{3 \cdot \alpha \cdot U_{MPP} + \beta}}}. \tag{2.47}$$

Table 2.6. Calculation of the European utilization ratio. The coefficients describing the second order polynomial are calculated for a Shell Ultra175 PV module, operating a six different points, with a de-coupling capacitor of 2. 2 mF.

Irradiation	5%	10%	20%	30%	50%	100%
Meteorological conditions	60 W/m^2 10 °C	120 W/m^2 12 °C	240 W/m^2 15 °C	360 W/m^2 18 °C	600 W/m^2 24 °C	1200 W/m^2 40 °C
Cell temperature	12 °C	16 °C	23 °C	30 °C	43 °C	78 °C
MPP power [W]	8.2 W	17.5 W	36.3 W	54.9 W	89.9 W	160.3 W
MPP voltage [V]	28.6 V	30.1 V	31.2 V	31.5 V	31.0 V	28.1 V
α	-0.0013	-0.0021	-0.0050	-0.0074	-0.0115	-0.0224
β	+0.0637	+0.1137	+0.2737	+0.4118	+0.6207	+1.0611
K_{PV}	0.9999	0.9996	0.9981	0.9958	0.9890	0.9560
EU weight	0.03	0.06	0.13	0.10	0.48	0.20

Applying a capacitor of 2.2 mF yields a European utilization ratio of 0.985, according to equation (1.1) and appendix A, cf. Table 2.6. This corresponds to an amplitude of 4.1 V at 1200 W/m^2 of irradiation.

2.5 Summary

The PV cell was introduced in this chapter with a short review of its history and types of technologies. This revealed that the most popular type of technology is the multi-crystalline silicon based PV cell, with globally 244 MW produced PV modules in 2002. The mode of operation was also presented.

A mathematical model for the PV cell was presented, based on the physical structure of the PV cell, which actually is a large PN junction (diode). The model is used to predict the amount of current generated by the light-controlled current-source under different irradiations and temperatures, based on numbers from the datasheet. The diode in the PN junction is also included in the model. A simple thermal model for the PV module is developed, based on Nominal Operating Cell Temperature (NOCT) conditions. Thus, it becomes possible to estimate the voltage-current characteristic at different irradiations and temperatures for a wide range of PV modules.

Based on the developed model, two phenomena where investigated, partial shadow and ripple at the PV module terminals. The partial shadow is also treated in many papers. The case of partial shadow is included in the chapter in order to show the problems associated with it. Thus, even a small amount of partial shadow may result in severe power losses, and the risk of de-lamination, and a very irregularly voltage-power characteristic. The irregularly characteristic is a problem for most Maximum Power Point Trackers (MPPT). This is regarded as a problem, which must be dealt with.

Finally, the sensitivity to ripple in voltage and current at the terminals of the PV module were considered. Such work has not yet been seen in the literature. The theory was established and verified with PSPICE simulations. The theory predicts a power loss of 1%, i.e. a utilization ratio of 99% when the amplitude of the ripple voltage is equal to 6% of the maximum power point voltage, and a loss of 2% when the voltage equals 8.5%.

These results are used to specify the demands for the module-inverter interface.

Chapter 3

Specifications & Demands

An inverter used in grid connected PV systems must satisfy some specifications, cf. Figure 3.1, which are given by national and international standards. The specifications for the PV module to the inverter, and the inverter to the grid interfaces are presented in this chapter. To cover a wide range of the potential market, different international standards will be presented. A specification for the tests that must be performed on the inverter is reviewed.

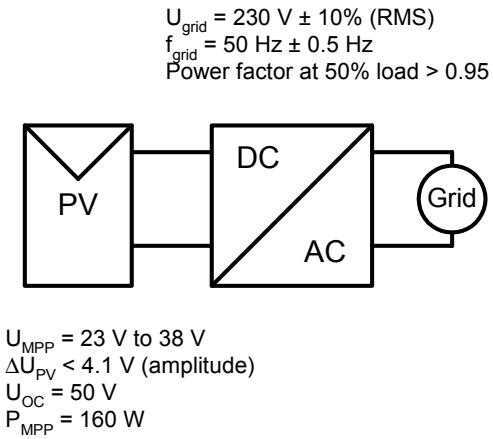

Figure 3.1. Figure of the inverter with PV module, and connected with the grid. The numbers given are a summary of the specifications.

3.1 General

3.1.1 Ambient Temperature

The ambient temperature, together with additional temperature increase inside the inverter, sets the rating for the selected components. As seen in appendix A, the PV cell temperature can reach 78 °C on a sunny day (irradiance: 1200 W/m^2 and ambient temperature: 40 °C). Thus, if the inverter is to be mounted on the rear side of the PV module, it has to withstand a temperature of almost 80 °C. If mounted on the support structure, the temperature will reach 40 °C, and probably 30 °C if mounted indoor.

3.1.2 Operational Lifetime and Reliability

The inverter should be maintenance-free during the AC-Module's lifetime. This is desirable while the AC-Module is intended to be a 'plug and play' device, which can be operated by persons without specialized training. The inverter lifetime is then directly specified according to the lifetime of the included PV module. For example, BP SOLAR gives a 25-year warranty on 80% power-output, cf. chapter 1.

3.1.3 Galvanic Isolation

Australia, Italy, Japan, Switzerland, England, and the United States of America require a transformer between the inverter and the grid if a DC monitoring device not is included. Denmark demands an HPFI-relay (High-sensitive, Pulsing direct current, earth Fault circuit breaker), if the transformer is omitted [37]. Germany, the Netherlands, and Portugal do not require a transformer at all [3].

Regarding personal safety, most PV modules belong to the class II equipment safety-class (reinforced or double isolation, symbolized with a ▣). Thus, they must not be grounded! According to section 3.3.9, system ground is required in some countries if the open circuit PV module exceeds 50 V. System ground is not required for the developed inverter, since the inverter is designed to maximum 50 V open circuit voltage, c.f. section 3.2.3. Thus, galvanic isolation is not required between the PV module and the grid, when personal safety is the issue.

3.2 Photovoltaic Module – Inverter Interface

A survey of 35 mono- and multi-crystalline silicon, 72-cells, PV modules is conducted in appendix A. The survey is used to set up the specifications for the PV module interface.

3.2.1 Nominal Power

The maximum power generated by the investigated PV modules is 189 W at an irradiation of 1200 W/m^2, and an ambient temperature of 25 °C. This operating point is however very seldom reached. The nominal power for the inverter is therefore selected to 189 W / 1.2 ≈ 160 W, with the capability of operating at 120% power during short time.

3.2.2 Starting Power

The inverter should be able to invert even small amounts of DC power into AC power. In other words, the inverter must be able to operate at very low irradiation. The European efficiency, presented in chapter 1, is the weighted average of efficiencies down to 5%. Thus, the inverter should be able to operate at 5% or less of the nominal power, which is 8 W.

3.2.3 Maximum Open-Circuit Voltage[4]

The worst-case open-circuit voltage across the investigated PV modules is estimated to 45 V at 1200 W/m^2, and a cell temperature of 25 °C. Thus, the inverter must withstand at least 45 V without being damaged, and 50 V is selected, cf. section 3.1.3 and 3.3.9.

3.2.4 Maximum power point tracking

The inverter must be capable of tracking the maximum power point in order to capture as much energy as possible. The voltage across the investigated PV modules, during normal operation, is located in the span from 23 V to 38 V. Thus this is selected as the range where the inverter must be able to track the maximum power point.

3.2.5 Input Ripple

The ripple current and voltage at the input terminals of the inverter must not cause the European utilization ratio to be lower than 0.985, c.f. chapter 2. Thus, the low frequency voltage ripple, at the terminals, should not exceed 4.1 V (amplitude) at full generation, which corresponds to a 2.2 mF capacitor in parallel with the module.

The High Frequency (HF) ripple, caused by the switching inside the inverter, must not cause any EMI problems. The amplitude of the HF voltage in the prototype must not exceed 0.50 V peak to peak.

3.2.6 Over Voltage Protection

The inverter must be capable to withstand over-voltages caused by nearby lightning, etc. It is recommended to use a surge arrestor (Metal Oxide Varistor) with an inception voltage of 1.2 times nominal voltage [3]. The arrestor should be connected from the positive to the negative input terminals. The inception- and inclination-voltage should therefore be higher than 50 V · 1.2 = 60 V.

3.2.7 Maximum Short Circuit Current

The maximum short-circuit current generated by the investigated PV modules is 7.2 A. A maximum current of 8 A is therefore chosen.

3.3 Inverter – Grid Interface

A survey of existing standards in some IEA countries is given in Table 3.1.

[4] The maximum open circuit voltage is changed from 45 V to 50 V in the 2nd edition of the thesis.

Table 3.1. Survey of existing standards in selected IEA countries, [3], [5], [37].

	Voltage fluctuation	Isolation transformer	Flicker	Harmonics	Power Factor
Australia	200 V -270 V	DC monitoring, Max 120 mAh / day	AS2279	AS2279	> 0.8 @ 20%
Austria	184 V – 253 V	No	-	EN61000-3-2-A	> 0.9
Denmark	207 V – 253 V	HPFI relay - 30 mA, Max 1% of nominal.	EN61000-3-3	EN61000-3-2-A	> 0.95 @ 50%
Germany	216 V – 244 V	No	< 3%	EN61000-3-2-A	> 0.9
Italy	207 V – 253 V	DC monitoring	-	EN61000-3-2-A	> 0.9
Japan	182 V – 222 V	DC monitoring, Max 1% of nominal.	< 10%	THD < 5%, each harm < 2%	> 0.85
Holland	207 V – 244 V	No	IEC1000-2-2	EN61000-3-2-A	> 0.9
Portugal	187 V – 253 V	No	-	EN50160	-
Switzerland	Not specified	DC monitoring	-	EN61000-3-2-A	-
United Kingdom	226 V – 254 V	DC monitoring	< 3%	EN61000-3-2-A	> 0.85
United States	-	DC monitoring	-	THD < 5%, each harm < 2%	> 0.95

3.3.1 Voltage

The nominal voltage for European grids is 230 V ±10% [36]. The inverter must operate without problems when voltage harmonics according to Table 3.2 are present in the grid.

Table 3.2. Values of individual harmonic voltages at the supply-terminals for orders up to 25. The THD of the supply voltage, including all harmonics up to the order 40, shall be less than 8% [3].

Odd harmonics, non multiple of 3		Odd harmonics, multiple of 3		Even harmonics	
Order [h]	Voltage [%]	Order [h]	Voltage [%]	Order [h]	Voltage [%]
1	100	3	5.0	2	2.0
5	6.0	9	1.5	4	1.0
7	5.0	15	0.3	6	0.5
11	3.5	21	0.2	8	0.5
13	3.0	> 21	0.2	10	0.5
17	2.0			12	0.2
19	1.5			> 12	0.2
23	1.5				
25	1.5				
> 25	0.2 + 12.5/h				

3.3.2 Maximum Power

The Netherlands and Switzerland allows connection of small inverters to normal feeders, if the total maximum power generation does not exceed 500 W for a regular feeder (16 A fused - 2,5 mm^2 copper wire) [3]. If this approach is going to be a de-facto standard, the nominal power should be within one of the following values: 500 W, 250 W, 167 W, 125 W or 100 W, in order to allow 1 to 5 AC modules to be connected to the same feeder.

3.3.3 Standby Losses

The power consumption during standby should be as low as possible, in order to raise the inverters overall efficiency. The passive filter included at the output terminals is the main cause for standby losses, if the PV module feeds the internal power supply.

3.3.4 DC-Current

The amount of DC current injected into the grid is important when speaking about saturation of the distribution transformers. The Australian standard AS3300 specifies a daily maximum amount of 0.120 Ah, which equals 5 mA continuously. Japan and Europe requires a maximum DC current of 1% of the nominal current [37], [38].

3.3.5 Frequency

The nominal frequency for European grids is 50 Hz ± 0,5 Hz [36].

3.3.6 Current Harmonics

Most countries have agreed upon the EN61000-3-2-A standard for current harmonics. However, Japan and the US demands a current Total Harmonic Distortion (THD) below 5 %, and any harmonics below 2 % of the fundamental current.

Table 3.3. EN 61000-3-2-A harmonic current limits [3].

Odd harmonics		Even harmonics	
Order [h]	Current [A]	Order [h]	Current [A]
1	16.0	2	1.08
3	2.30	4	0.43
5	1.14	6	0.30
7	0.77	> 8	1.84 / h
9	0.40		
11	0.33		
13	0.21		
> 13	2.25 / h		

3.3.7 Power Factor

The Power Factor (PF) should be close to unity in order not to generate or consume reactive power. Denmark requires a PF better than 0.95 for 50% of nominal power.

3.3.8 Inrush Current

During fault situations on the medium or high voltage overhead lines, these lines may be switched out in order to clear the fault. This causes a sudden voltage drop at the grid and hence the inverter. The inverter must cease to energize the grid if this happens, cf. 3.4.1. Disabling the semiconductors in the output circuit is sufficient. When the voltage restores or the inverter is connected to the grid for the first time, the current into the inverter must not reach damaging values.

3.3.9 Grounding

Equipment ground is required in all countries. System ground is required in some countries for systems with voltages over 50 V (PV module open circuit voltage) [3]. Equipment ground involves that all metallic surfaces, etc., are grounded.

3.4 Safety and Compliances

3.4.1 Islanding Protection

Islanding is the continued operation of the inverter when the grid has been removed by purpose, by accident, or by damage. In other words, the grid has been removed from the inverter, which then only supplies local loads. The inverter must be able to detect an islanding situation, and take appropriated measure in order to protect persons and equipment [3].

The available detection schemes are normally divided into two groups: active and passive. The passive methods do not have any influence on the power quality, since they just monitor grid parameters. The active schemes introduce a disturbance into the grid; hence the power quality is affected, and monitors the effect.

Within the passive methods is detection of: under- and over- voltage and frequency; voltage phase jump; voltage harmonics; and Rate-Of-Change-Of-Frequency (ROCOF). Within the active methods is: detection of grid impedance; detection of grid impedance at specified frequency; slip mode frequency shift; frequency bias; Sandia frequency and voltage shift; frequency jump; and mains monitoring units with allocated all-pole switching devices connected in series (MSD and ENS) [39].

A survey within demands in different IEA countries are given in Table 3.4. Note that the Danish utility companies demand that active methods do not influence the operation of other equipment [37]. The Danish recommendation also states that the ROCOF method is sufficient. The inverter shall cease to inject power into the grid within 0.2 s, if the rate of change exceeds ± 2.5 Hz/s.

Table 3.4: Limits for detection of islanding operation [3], [5], [37].

Country	Voltage range	Frequency range	Disconnect within	Active / passive
Australia	200 V – 270 V	48 Hz – 52 Hz	-	Passive + Frequency shift or impedance.
Austria	230 V, +10%, -15%	50 Hz ± 0.2 Hz	0.2 s / 0.2 s	Passive + impedance (ENS)
Denmark	230 V, +10%, -15%	47 Hz – 51 Hz	1.5 s / 0.5 s	Passive (ROCOF)
Germany	230 V, +10%, -15%	50 ± 0.2 Hz	0.2 s / 0.2 s	Passive + impedance (ENS)
Italy	230 V, +20%, -20%	50 ± 1.0 Hz	0.1 s / 0.1 s	Passive
Holland	230 V, +6%, -20%	50 ± 2 Hz	0.1 s / 2 s	Passive
Portugal	230 V, +15%, -15%	50 ± 0.25 Hz	0.1 s / 0.1 s	-
Switzerland	230 V, +10%, -10%	50 ± 1 Hz	-	-
The UK	240 V, +10%, -10%	44 Hz – 51 Hz	0.5 s / 0.5 s	Passive (ROCOF)

3.4.2 Compliance

Table 3.5: Collection of international standards, which the inverter must fulfill.

	Topic	Standard	Year
Emission	Low frequency current harmonics	EN 61000-3-2	1995
	Voltage fluctuation and flicker	EN 61000-3-3	1995
	Conducted EMI	EN 50081-1	
	Radiated EMI	EN 50081-2	
Immunity	Generic immunity standard	EN 61000-4-1	1992
	Electrostatic discharge (ESD)	EN 61000-4-2	1995
	Radiated electro-magnetic field	EN 61000-4-3	1995
	Electrical fast transient	EN 61000-4-4	1995
	Surge transient	EN 61000-4-5	1995
	Conducted radio-frequency field	EN 61000-4-6	1996
	Voltage dips, interruptions and variations	EN 61000-4-11	1994
Directive	Low voltage directive	LV 73/23/EEC, 93/68/EEC	
	EMC directive	EMC 89/336/EEC, 92/31/EEC	
	Electric safety	EN 60950, KEMA, UL, CE	

3.5 Test plan

A test plan for the developed PV-inverter is intended to be a thorough evaluation that can be used for the characterization of the designed inverter. The plan is based on the international standards and the experience in the field of grid connected PV systems. It covers functional tests, protection tests and field tests. These tests are performed in order to evaluate the following characteristics of the inverter [40]:

- Static power efficiency - The power efficiency of an inverter is defined as the ratio between the power injected into the grid and the power from the PV module.
- Power factor - The purpose of this test is to determine the power factor of the system and see if it is consistent with the international standards.
- Current harmonics - In general the operation of the inverter should not cause excessive distortion of the grid voltage or result in excessive injection of harmonic currents into the grid.
- MPP tracking efficiency.
- Standby losses - The standby loss is defined as the consumption of utility power when the inverter is not operating but under standby conditions.
- Disconnections of ac power line - The purpose of this test is to observe the inverter response under loss of grid connection.
- Disconnections of dc power line - The purpose of this test is to observe the reaction of the inverter when the DC power line is suddenly disconnected.
- AC voltage limits - The purpose of this test is to determine the AC voltage limits (over/under voltage) at which the inverter stops operating.
- Frequency limits - The purpose of this test is to determine the frequency limits (over/under frequency) at which the inverter stops operating.
- Response to abnormal utility conditions - The purpose of this test is to observe and verify the operation of the inverter under abnormal grid conditions.
- Field test - The purpose of this test is to evaluate the performance of the inverter when connected to normally illuminated modules of different technologies. In this test many parameters such as energy efficiency, start up voltage, start up power, stop voltage and standby losses can be measured.

The entire test plan is presented in appendix B.

3.6 Summary

The numbers presented in this specification are used in chapter 4 to find the fittest topology for a 160 W inverter, and are also used in chapter 5 to design the inverter.

Chapter 4

Inverter Topologies

The selection of a suitable power electronic topology for the inverter depends on many different issues besides the electrical specifications, such as: cables; electrolytic capacitors; mechanical / thermal / enclosure demands; silicon devices; magnetics; and efficiency, etc. All the items above must carefully be evaluated for each system layout and inverter topology, in order to find the best inverter topology for a 160-Watt AC-module.

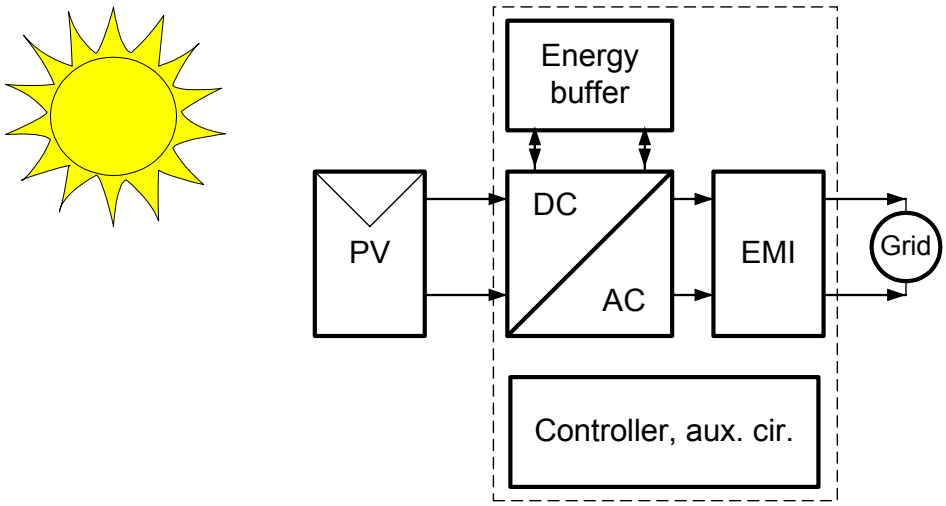

Figure 4.1. Block-diagram for a typical inverter for PV applications. The arrows indicate the direction of power flow.

Figure 4.1 depicts the building blocks for a typical inverter for PV to grid applications. The blocks are: controller with auxiliary circuits such as measuring, protection and internal power supplies, energy buffer for power-decoupling between the PV module and the single-phase grid, Electro Magnetic Interference (EMI) filter for reducing conducted electrical noise, and finally; the power electronic circuit that inverts the generated DC voltage to an AC current.

The following is a State-Of-The-Art (SOTA) analysis of the most common technical solutions for inverters for AC modules up to 300 Watt. The SOTA analysis concludes with a comparison of the different topologies, based on lifetime, components ratings, cost, and European efficiency. Solutions that utilize a Low Frequency (LF) transformer are omitted since this component is regarded as being obsolete. Besides this, inverters with more than two power-processing stages are also omitted. Summaries of inverter topologies for multiple PV modules, LF transformer solutions, multi-stage inverters, and multilevel inverters are given in [6], [8], [9], [10], [11], [15], [41], [42], [43], [44], [45], [46], [47], [48], and [49].

Models for power loss are given in appendices C, E, and F, relationships between component ratings and costs are given in appendix D, and finally the topologies are designed in appendix F.

4.1 System Layout

According to the definition in chapter 1, an AC-Module is the integration of the PV module and the inverter into one unit, see also Figure 4.2. However, integration of the PV module with the inverter may not be an optimum solution, due to problems with enclosure and high temperature.

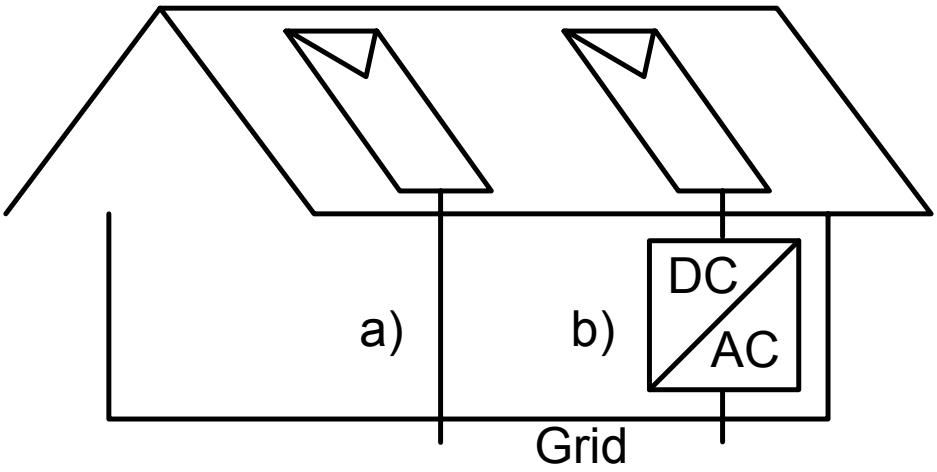

Figure 4.2. The two investigated layouts. A) The inverter and the PV module is integrated into one device, placed on the roof. B) The inverter is located inside the residence and the PV module is located on the roof.

Another solution is to place the inverter indoor, far away from the severe temperature and enclosure demands. On the other hand, this calls for relative long DC-cables with ‘high’ current and hence higher losses compared to AC-cables with ‘low’ current and losses. So what is the optimum placement of the inverter? In order to answer this question the following two items are investigated: 1) Losses in cables between PV module / inverter and inverter / grid. 2) Lifetime of the inverter when exposed to the severe temperatures of the PV modules back plane and the more gentle temperature inside the residence.

4.1.1 Cable Losses

The cable losses are examined first. The PV module is assumed operated at the Maximum Power Point (MPP) by means of a tracker, which continuously adjusts the voltage and current to follow U_{mpp} and I_{mpp}. The power losses associated with the cables are calculated as:

$$P_{cable,dc} = P_{MPP} - P_{inv,in} = R_{cable,dc} \cdot {I_{MPP}}^2 \approx R_{cable,dc} \cdot \left(\frac{P_{MPP}}{U_{MPP}} \right)^2 \text{, and} \tag{4.1}$$

$$P_{cable,ac} = \left(P_{MPP} - P_{cable,dc} \right) \cdot \eta_{inv} - P_{grid} = R_{cable,ac} \cdot {I_{grid}}^2 \approx R_{cable,ac} \cdot \left(\frac{\left(P_{MPP} - P_{cable,dc} \right) \cdot \eta_{inv}}{U_{grid}} \right)^2, \tag{4.2}$$

under the assumption that the voltage drops across the cables are small. The efficiency of the inverter, η_{inv}, is assumed equal to 0.90. The resistances in the two cables are given as:

$$R_{cable} = \rho_{Cu} \cdot \frac{l_{cable}}{A_{cable}}, \tag{4.3}$$

where ρ_{Cu} is the resistivity for copper ($\rho_{Cu} = 17.2 \cdot 10^{-9}$ Ω·m at 20 °C), l_{cable} is the length of the cable and A_{cable} is the cross-section area.

In the next example the cable cross-section is assumed to be 2.5 mm^2 for the AC-cable and 4 mm^2 for the DC-cable (Most PV modules accepts a 4 mm^2 cable). Skin effects are neglected in the calculations, since the skin-depth at 50 Hz is in the vicinity of 10 mm, much higher then the cross-section of a 2.5 mm^2 copper cable. The displacement is varied from 0 to 10 meter, which corresponds to a total cable length 20 meters.

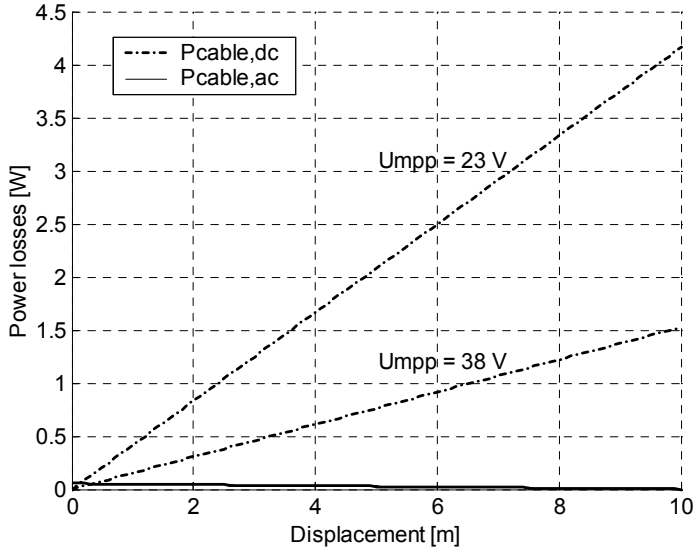

Figure 4.3. Power loss associated with the DC (4.0 mm^2) and AC (2.5 mm^2) cables at the two extremes for the MPP voltage (23 V and 38 V) at P_{MMP} = 160 W, and 90% inverter efficiency. A displacement of 0 m corresponds to 0 m DC-cable and 2×10 m AC-cable. A displacement of 10 m corresponds to 2×10 m DC-cable and 0 m AC-cable.

Figure 4.3 clearly shows that the power loss within the DC cable always is the main contribution to the total cable loss. The calculation shows that 2×10 m AC-cable involves a small power loss around 0.1 W, whereas 2×10 m DC-cable results in losses from 1.5 W to 4.2 W (depending of the MPP voltage). Thus, from this point of view, the inverter should be placed as close to the PV module as possible, e.g. on the rear side of the PV module, or on the supporting structure.

4.1.2 Lifetime of Electrolytic Capacitors

The lifetime of the inverter is mostly determined by the electrolytic capacitors (after this: capacitor) included in the circuit [34], [50], [51], [52]. Hence the number of this fateful component should be kept low. On the other hand, it is impossible to design a single-phase inverter without at least one capacitor for power decoupling between the PV module and the grid.

End of life of the capacitor is defined when one or more of its parameters have changed by a given amount, e.g. [53]:

- Change in capacitance: $\Delta C = 15\%$ for rated voltage below 160 V,
- Change in capacitance: $\Delta C = 10\%$ for rated voltage above 160 V,
- Change in Equivalent Series Resistance: ESR > 2 times the initial value,
- Change in dissipation factor: DF (tan δ) > 1.3 times the rated value,
- Change in leakage current: I_L > the rated value.

The lifetime for an electrolytic capacitor is given by [54]:

$$L_{OP} = L_{OP,0} \cdot 2^{\left(\frac{T_0 - T_h}{\Delta T}\right)}, \tag{4.4}$$

where L_{OP} is the operational lifetime, $L_{OP,0}$ is the lifetime at a hotspot temperature of T_0, T_h is the hotspot temperature and ΔT is the temperature increase which reduces the lifetime with a factor of two. However, the equation assumes a constant temperature, which may be the case when the inverter is placed indoor, but certainly not when the inverter is integrated together with the PV module. In the case of a varying temperature a mean value of (4.4) must be used. The hotspot temperature is equal to $T_h(t)$ and t_{cycle} is the period for one temperature cycle:

$$L_{OP} = \frac{L_{OP,0} \cdot 2^{\left(\frac{T_0}{\Delta T}\right)}}{t_{cycle}} \cdot \int_0^{t_{cycle}} \frac{1}{2^{\left(\frac{T_h(t)}{\Delta T}\right)}} dt\,. \tag{4.5}$$

The hotspot temperature is now determined for the case when the inverter is mounted on the rear side of the PV module. The surface temperature for the capacitor equals the PV module temperature:

$$T_h = T_{cell} + R_{\theta,C} \cdot P_{loss,C}\,, \tag{4.6}$$

where T_{cell} is the PV module temperature, $R_{\theta,C}$ is the thermal resistance for the capacitor, and $P_{loss,C}$ is the loss in the capacitor. The loss inside the capacitor is calculated as:

$$P_{loss,C} = ESR \cdot I_{C,RMS}{}^2 , \tag{4.7}$$

where $I_{C,RMS}$ is the RMS value of the current through the capacitor. When the capacitor is placed in parallel with the PV module or in the DC-link, the RMS value is (calculated as the RMS value of the current in (2.44)):

$$I_{C,RMS} = \frac{P_{MPP}}{U_C} \cdot \sqrt{½} , \tag{4.8}$$

where P_{MPP} is the power generated at the MPP, and U_C is the voltage across the capacitor. The voltage in the DC-link is assumed constant, but the MPP voltage is a function of temperature (and to some extend irradiated power). The MPP voltage is estimated as:

$$U_{MPP} = U_{MPP,STC} + k_{temp} \cdot (T_{cell} - T_{STC}) , \tag{4.9}$$

where $U_{MPP,STC}$ is the MPP voltage at Standard Test Conditions (STC), k_{temp} is the temperature coefficient of the MPP voltage, and T_{STC} is the STC temperature. The PV cell temperature is given as:

$$T_{cell} = T_{abm} + R_{\theta,PV} \cdot P_{sun} , \tag{4.10}$$

where T_{abm} is the ambient temperature, $R_{\theta,PV}$ is the thermal resistance for the PV module, and P_{sun} is the irradiation from the sun. In order to proceed, information about irradiation, ambient temperature and components parameters must be gained.

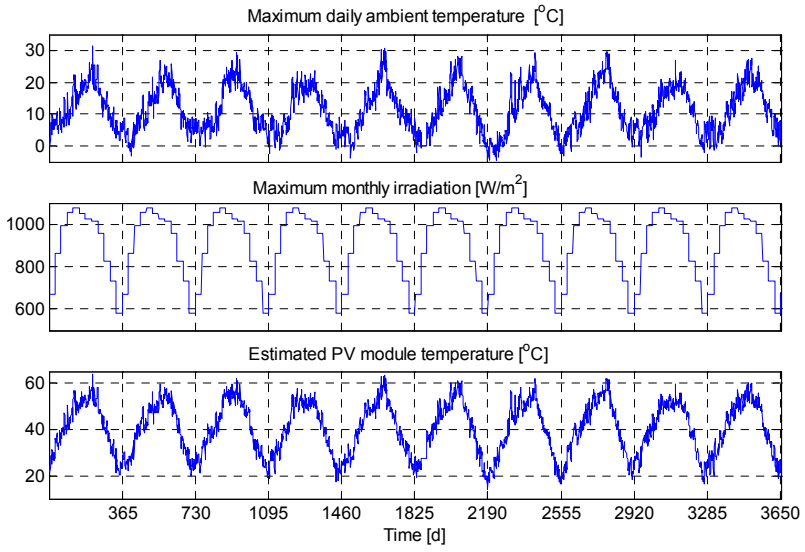

Figure 4.4. Meteorological data for Denmark. Upper) Maximum daily ambient temperature recorded during January the 1st 1990 to December the 31st 1999, Danish Meteorological Institute [55]. Middle) Estimated maximum monthly global irradiation [21]. Lower) Estimated daily maximum PV module temperature.

Assuming two 'long-life' capacitors, one placed in parallel with the PV module (2200 µF @ 63 V) and the other placed in the DC-link (33 µF @ 450 V), cf. chapter 5. Their parameters are given in Table 4.1, and the applied meteorological data is depicted in Figure 4.4 for a ten-year span [21], [55]. The parameters for the PV module at STC are given as: P_{MPP} = 160 W with a temperature coefficient of -0.8 W/K, U_{MPP} = 36 V with a temperature coefficient of -0.16 V/K, and a NOCT value of 47°C. The DC-link voltage is assumed constant at 350 V.

Assuming that the ambient temperature during a day is equal to the maximum temperature recorded that day, and that the irradiation during a month is equal to the maximum irradiation estimated that month results in a very conservative estimation of the lifetime. Thus the results in Figure 4.5, and Table 4.1 should be interpreted with care. On the other hand, daily temperature-variations lead to cracks and breaks in the components due to thermal expansions and contractions. This is not included in the model, and more work should be done in this area in order to come with a more reliable statement.

The maximum temperature difference of the two layouts equals 6.1 °C. Applying this to (4.4), reveals that a capacitor placed in the DC-link will last for 46% longer time, compared to the capacitor placed in parallel with the PV module (assuming same ΔT = 11 K).

Finally, the meteorological data used to estimate the lifetime for the inverter is for Denmark. The prediction is therefore not valid for e.g. south European conditions where the irradiation and ambient temperature can reach as much as 1200 W/m^2 and 40°C.

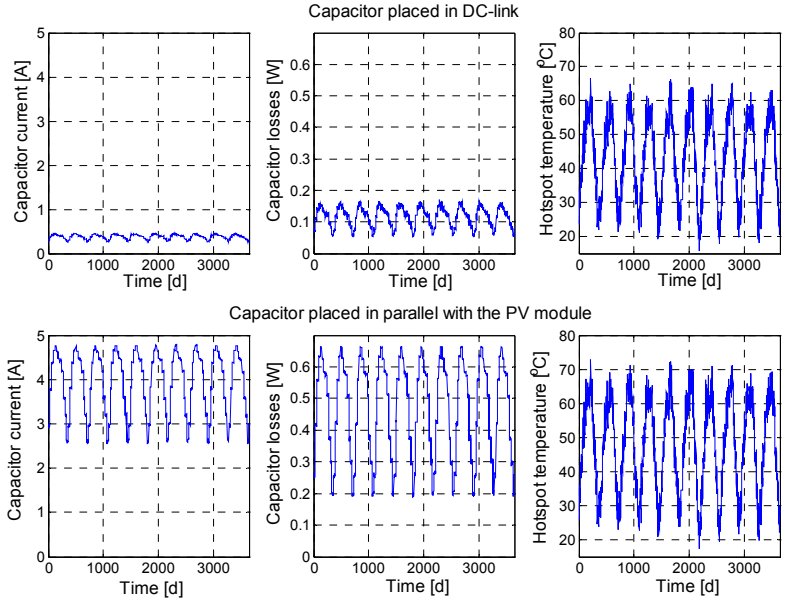

Figure 4.5. Estimated hotspot temperatures. Upper) Axial-type capacitor situated in the DC-link. Lower) Snap-in type capacitor in parallel with the PV module.

Table 4.1. Parameters for four electrolytic capacitors.

Type	PEH536 (snap-in)	PEH534 (snap-in)	PEH532 (snap-in)	PEG124 (axial)
Ratings	2200 μF @ 63 V			33 μF @ 450 V
$L_{OP,0}$ at 85 °C [h]	19 500	13 000	6500	97 000
ΔT [K]	12			11
ESR @ 100 Hz [Ω]	0.055 – 0.062 (average 0.0583)			1.60
Thermal resistance [K/W]	16			26
Maximum steady state temperature for L_{OP} = 30 years (263 000 h) [°C]	40	33	21	69
L_{OP} for ambient temperature-profile in Figure 4.4 [h]	128 000	85 200	42 600	1004 000
Equivalent steady state temperature [°C]	52.4			47.9

4.2 Topologies with a HF-link

The High Frequency (HF) link inverter uses a HF DC-AC inverter to amplify the voltage generated by the PV module, and to modulate the sinusoidal grid current. An AC-AC inverter, which converts the HF current to a Low Frequency (LF) current for the grid, follows the DC-AC inverter, cf. Figure 4.6. This involves that power decoupling must be performed with a large electrolytic capacitor in parallel with the PV module.

Besides this, both stages must be designed to handle a peak power of twice the nominal power, since there is no energy-buffer between them:

$$p_{grid} = 2 \cdot P_{grid} \cdot \sin^2(\omega \cdot t), \tag{4.11}$$

but a possible transformer is operated at high frequency

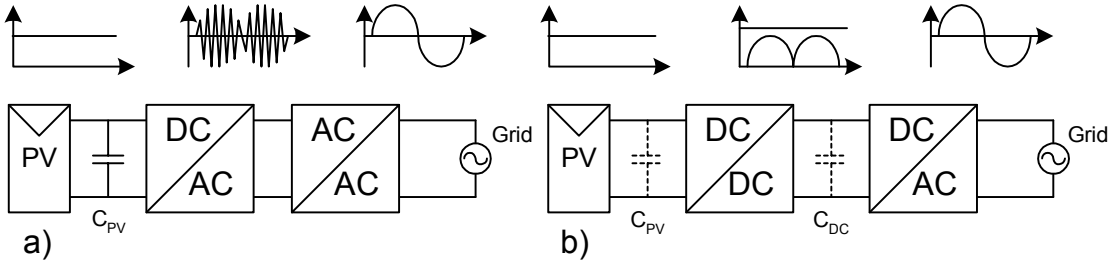

Figure 4.6. Fundamental schematics and waveforms of the currents between the stages for the two types of inverters. A) HF-link, B) DC-link.

4.2.1 Single-Transistor Flyback Type Inverter (Papanikolaou, *et al.* and Achille, *et al.*)

The topology shown in Figure 4.7 is a 100-Watt flyback type inverter [56] and [57]. The circuit is made up around a single-transistor flyback converter, with a center-tapped transformer. The two outputs from the transformer are connected to the grid, one at a time, through two MOSFET', two diodes and a common filter circuit [56]. The flyback converter can in this way produce both a positive and a negative output current. The inverter in [57] is very much alike, except that the output diodes: D_{RECT1} and D_{RECT2}, are omitted. Thus, the two output transistors: S_{AC1} and S_{AC2}, must be switched synchronously with the main transistor S_{PV}, at high frequency. This saves two diodes, but the control of the output transistors becomes in this way more difficult.

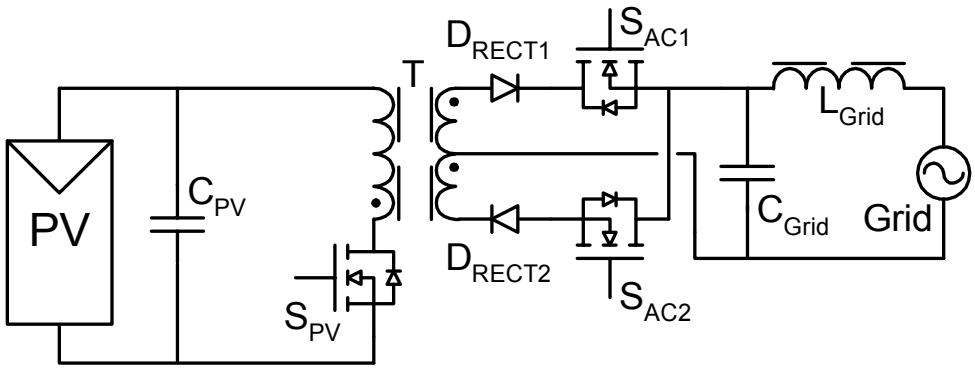

Figure 4.7. 100 Watt single-transistor flyback type HF-link inverter [56].

The flyback converter operates in Discontinuous Conduction Mode (DCM), which involves that the transformer magnetizing current always reaches zero before a new switching cycle is initiated. This is beneficial since DCM involves easy control of the grid current, and that the MOSFET on the PV-side turns on at zero-current. However, a drawback is the high peak current of the main MOSFET and the transformer, in the vicinity of 60 A for a 160-Watt inverter operated at 50 kHz. The two MOSFETs on the grid-side are switched at 100 Hz and at zero-voltage and zero-current.

The voltage on the secondary-side of the transformer is reflected (mirrored) into the primary-side of the transformer, when the main MOSFET is turned off (this is true for all flyback types of circuits). Besides this, an additional over-voltage is likely to occur across the main MOSFET when it is turning off, due to the leakage inductance in the transformer and the magnetizing current.

The over-voltage can be avoided with a dissipative RCD clamp, a non-dissipative LCDD clamp [58], or an active SC clamp [59], but the reflected voltage is incurable. Thus, the main MOSFET must withstand a voltage of magnitude:

$$\hat{U}_{SDC} = \hat{U}_{PV} + \frac{\hat{U}_{grid}}{N} + \hat{U}_{leakage}, \tag{4.12}$$

where N is the transformer turns ratio. However, a solution is to replace the single-transistor flyback with a two-transistor flyback as in the modified Shimizu inverter of section 4.2.3, cf. Figure 4.9. This also solves the problem with the clamp circuit, which can be avoided [60], [61].

Test results in [56] show a maximum efficiency of 96% and at the same time a power factor of 0.955 is achieved (U_{MPP} = 48 V, P_{MPP} = 100 W, U_{grid} = 230 V). The 'low' power factor is caused by a small distortion of the grid current, around zero crossing, where no current is injected into the grid. The Total Harmonic Distortion (THD) can be calculated to 31% when assuming sinusoidal grid voltage.

Finally, both stages must be designed for twice the nominal power, and power decoupling must be achieved with a large electrolytic capacitor in parallel with the PV module.

4.2.2 Combined Flyback and Buck-Boost Type Inverter (Shimizu, *et al.*)

The next topology is a 105-Watt combined flyback and buck-boost inverter [62], cf. Figure 4.8. The need for a large decoupling capacitor is avoided by adding a buck-boost converter to the flyback converter. The mode of operation is a little more impenetrable, than the previous flyback type inverter in Figure 4.7. Thus, it will be revised here.

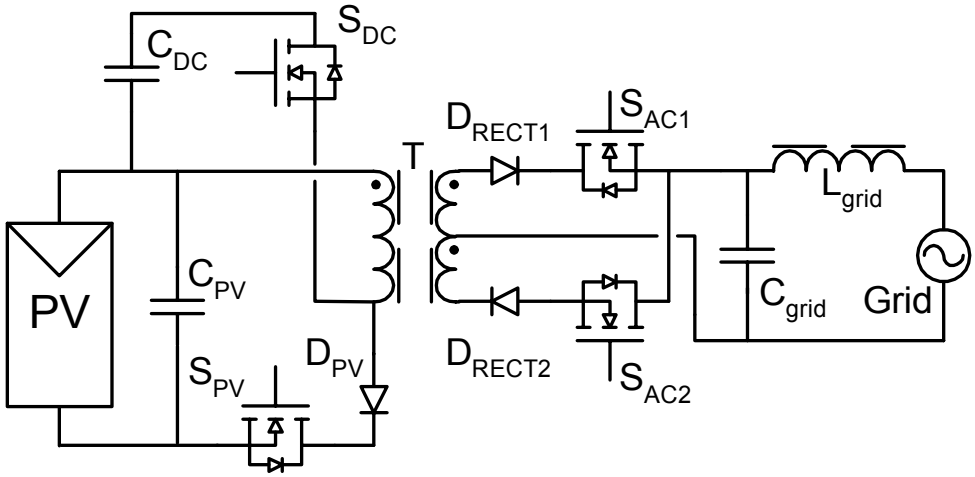

Figure 4.8. Flyback type inverter with high power decoupling [62].

The transistor S_{PV}, the diode D_{PV}, the primary transformer winding, the body diode of S_{DC}, and the capacitor C_{DC} make up a DCM buck-boost converter. The primary-side of the flyback converter is made up around C_{DC}, S_{DC}, D_{PV} and the transformer.

All currents on the PV-side are zero prior to a new cycle (except between the PV module and the capacitor placed in parallel with it), i.e. the converter operates in DCM.

A new cycle starts with turning transistor S_{PV} on, which results in a linear rising magnetizing current. When the current reaches the reference value, transistor S_{PV} turns off and the energy stored in the magnetizing inductance is transferred into the capacitor C_{DC}. Transistor S_{DC} must be turned on while the current is discharging into the capacitor. This involves zero-voltage switching, since its body-diode is conducting. Besides this, one of the transistors in the output stage is turned on simultaneous with turning S_{DC} on. Thus, the transistors on the secondary-side are switched at a high frequency, contrary to the previous flyback inverter.

The magnetizing current continues to decrease after reaching zero, now energized by the capacitor C_{DC}. When the magnetizing current reaches the second reference value, transistor S_{DC} turns off and the energy stored in the magnetizing inductance is transferred into the secondary-side of the transformer and further into the grid. The Diode D_{PV} is included to avoid reverse voltage across the PV module and the capacitor C_{PV} when the energy is transferred into the secondary-side, which involves voltage reflection.

Again, the leakage inductance included in the transformer results in a voltage-spike across the transistor S_{DC} during turn off. A dissipative RCD clamp would normally be used to remove the over-voltage, cf. the previous topology. However, the RCD clamp circuit is interacting heavily with the bust-boost circuit, causing the inverter to malfunction! The paper does not explain how they get around this problem [62]. A solution is the modified Shimizu topology presented in the next section [63]. Finally, the energy storing capacitor, C_{DC}, must carry the entire load current, which increases the demands for its current ripple capabilities.

Test results in [62] show a THD of less than 5% (U_{MPP} = 35 V, P_{MPP} = 30 W, U_{grid} = 85 V), which corresponds to a PF of 0.999.

4.2.3 The Modified Shimizu Inverter (Kjaer, *et al.*)

The next inverter is an enhanced version of the previous topology, rated for 160-Watt, cf. Figure 4.9. The main improvement within this inverter is the replacement of the single-transistor flyback converter with a two-transistor flyback converter, to overcome problems with over-voltage.

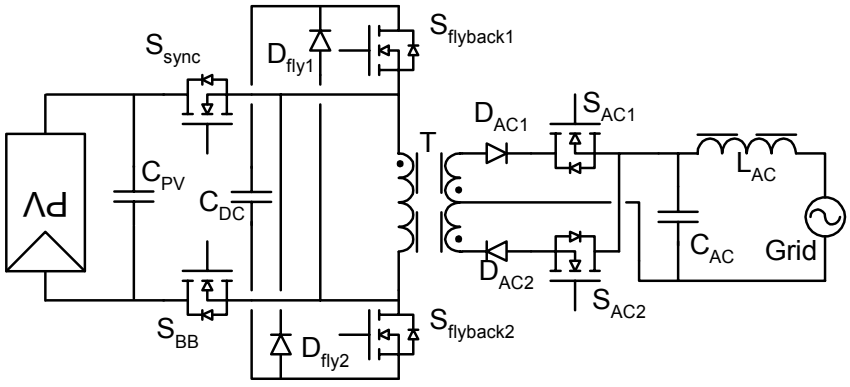

Figure 4.9. Modified Shimizu inverter [63]. Please note that the polarity of the PV module is reversed.

The modified topology is made up around two flyback transistors: $S_{flyback1}$ and $S_{flyback2}$, two flyback diodes: D_{fly1} and D_{fly2}, the buck-boost transistor: S_{BB}, a synchronous-rectified transistor for substitution of D_{PV} in the previous inverter: S_{sync}, a flyback transformer: T (with magnetizing inductance: L_M), AC switches with blocking diodes: S_{AC1}, S_{AC2}, D_{AC1}, and D_{AC2}, output LC filter: C_{AC} and L_{AC}, input capacitor: C_{PV}, and the intermediate capacitor: C_{DC}, [63].

The constant input power from the PV module is processed in the first part of the switching-cycle by the buck-boost converter and stored in the intermediate capacitor. The flyback converter processes a part of the stored energy in the second part of the cycle. The energy stored in the magnetizing inductance is in the third stage transferred to the secondary-side of the transformer and injected into the grid by the output stage and the LC filter. The mode of operation is investigated in details in [63]. Again, the energy storing capacitor, C_{DC}, must carry the entire load current.

Test result in [63] predicts a maximum efficiency of 87% and a European efficiency in the vicinity of 82% (U_{MPP} = 28 V, P_{MPP} = 160 W, U_{grid} = 230 V).

4.2.4 Isolated Ćuk Inverter in Parallel-Parallel Connection (Myrzik)

The topology in Figure 4.10 is a 200-Watt isolated Ćuk inverter in a parallel-parallel configuration [64]. This converter is also operated in DCM, which involves that the current in least one of the inductors (L_{PV} or L_{grid}) must be discontinuous.

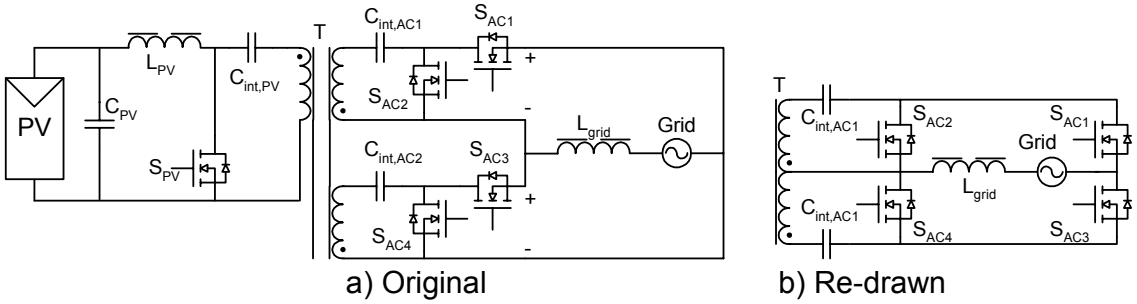

Figure 4.10. Isolated Ćuk inverter in parallel-parallel connection [64].

The pros for DCM operation with continuous current in L_{grid}, are a linear transfer function that makes the control easy, that the size of L_{PV} can be reduced, and that the current injected into the grid is free of HF ripple.

The PV-side of the inverter is a standard Ćuk converter stage. The magnetizing current can be positive and negative, resulting in good utilization of the BH loop of the magnetic material. On the other hand, the intermediate capacitor $C_{int,PV}$ is exposed to large current ripple. Besides, the transistor must withstand the reflected voltage plus some ringing due to the leakage inductance [60], [61].

The grid-side of the inverter is made by two standard Ćuk converter stages, with their outputs connected in anti-parallel. Thus, the first output-stage can produce a positive current into the grid, and the second stage can produce a negative current. The two transistors S_{AC1} and S_{AC3} are switched at 100 Hz, in order to change the direction of the output current, whereas the transistors S_{AC2} and S_{AC4} are continuously switched at the same frequency as the transistor S_{PV}.

No test results are given in [64] for the Ćuk inverter, but results are given for a similar Zeta inverter, see next section.

4.2.5 Isolated Zeta Inverter in Parallel-Parallel Connection (Myrzik)

The inverter in Figure 4.11 is based on the isolated Zeta converter (alias the isolated inverse SEPIC converter [61]) [64]. This inverter is also operated at 200-Watt, and in DCM.

The only difference between the isolated Ćuk- and the isolated Zeta-inverter is the input stage. The PV-side of the inverter is a standard flyback converter stage.

Test result in [64] show a maximum efficiency of 93% at full power generation (P_{MPP} = 200 W, U_{grid} = 230 V).

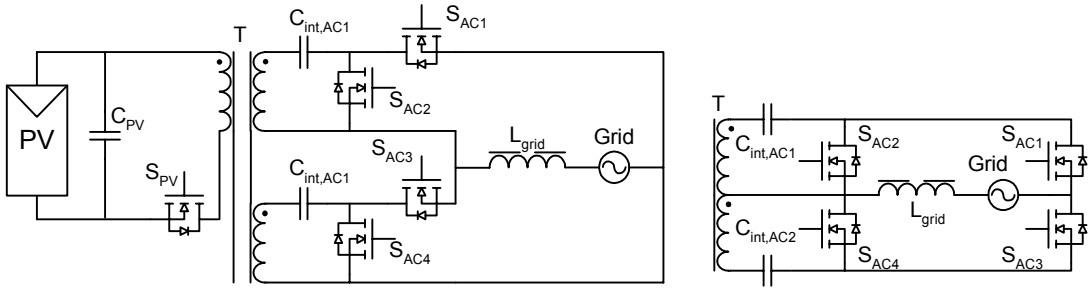

Figure 4.11. Isolated Zeta inverter in parallel-parallel connection [64].

4.2.6 Dual Two-Transistor Flyback Type Inverter (Nagao, *et al.*)

The next topology here is a 160-Watt buck-boost inverter, cf. Figure 4.12 [65]. However, it turned out that what claimed to be a buck-boost inverter is a dual two-transistor flyback inverter! The circuit on the PV-side is made up around an input filter: L_{DC} and C_{PV}, the dual two-transistor stage: S_{PV1} to S_{PV4} and the magnetizing inductance of the transformer. The diode D_{PV} is included in order to block reverse power flow from the grid, but is not necessary if the transformer turns ratio is selected sufficient high.

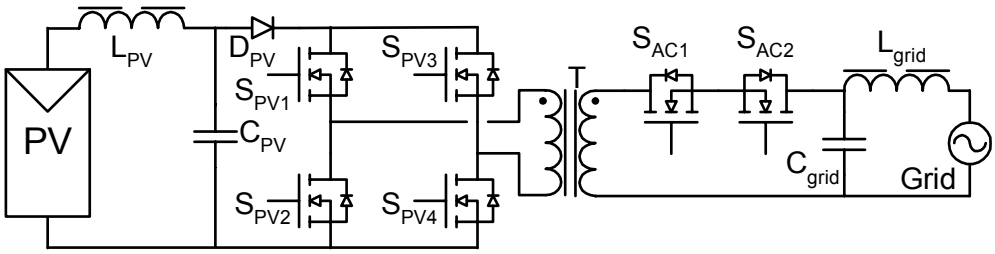

Figure 4.12. Dual two-transistor flyback type inverter [65].

The transistors in the dual two-transistor flyback converter are operated at high frequency, and the transistors in the output-stage are operated at 100 Hz. Transistor S_{AC1} of the output stage is on during the entire positive grid period, and vice versa for transistor S_{AC2}.

Assuming a negative grid voltage, and that all currents are zero (DCM): A new cycle is initiated by turning transistors S_{PV1} and S_{PV4} on (transistors S_{PV2} and S_{PV3} for a positive grid voltage). This causes the magnetizing current to increase from zero. The transistors are kept on in a pre-defined amount of time (a function of required power transfer, and PV voltage). They are then turned off, and the power stored in the magnetizing inductance is transferred into the secondary-side of the transformer. The power is further injected into the grid, through transistor S_{AC2}, the body-diode of transistor S_{AC1}, and the filter (vice versa for a positive grid voltage). Again, a small portion of energy is stored in the leakage inductance. This energy is now recovered by the body-diodes of the transistors S_{PV2} and S_{PV3}. On the other hand, the diode D_{PV} is blocking for the energy recovery, and no further information is given in [65] about the type of applied clamp circuit!

Test result in [65] shows a high power factor (P_{MPP} = 160 W, U_{grid} = 100 V).

4.3 Topologies with a DC-link

The DC-link inverter uses a HF DC-DC converter to amplifying the voltage generated by the PV module. A DC-AC inverter, which inverts the DC current to a sinusoidal current for the grid, follows the DC-DC converter, cf. Figure 4.6.

A small capacitor can be added in the DC-link for power decoupling, if the only task for the DC/DC converter is to amplify the voltage level generated by the PV module. Besides this, it is sufficient to design the DC-DC converter for the nominal power and the DC-AC inverter for twice the nominal power, c.f. (4.11), because of the energy-buffer between the two stages. On the other hand, a large electrolytic capacitor must be added in parallel with the PV module and both stages must be designed for twice the nominal power, if the DC-DC converter also has to modulate the grid current c.f. (4.11), because no energy-buffer is present between the two stages.

4.3.1 Isolated Flyback in Parallel-Series Connection (Kjær, *et al.*)

A novel 160-Watt single stage topology is depicted in Figure 4.13. It is made up around two independent bi-directional flyback converters [66].

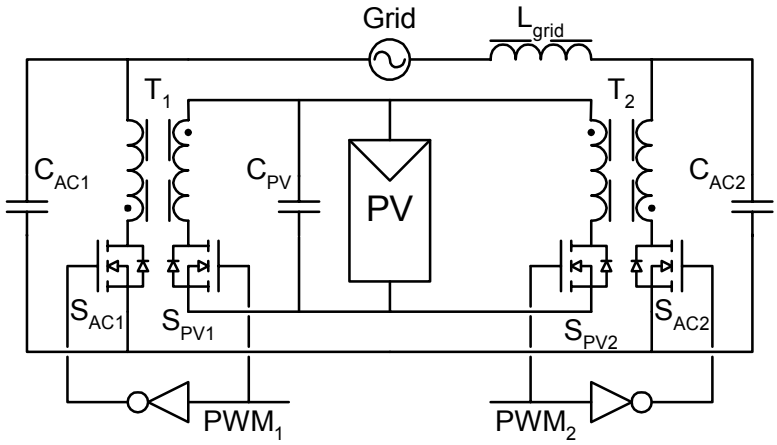

Figure 4.13. A novel solution for the AC Module [66].

The grid is connected in series with the outputs of the two converters, and the PV module is connected in parallel with their inputs.

Unfortunately, the inverter operates in Continuous Conduction Mode (CCM), which makes the control more troublesome, and two clamp circuits (not shown) must be applied to lower the over-voltages generated by the leakage inductances.

The inverter generates an AC voltage across its output terminals by modulating two sinusoidal voltages across the AC capacitors (C_{AC1} and C_{AC2}), with a 180° displacement with respect to each other and with the same DC bias, U_0:

$$u_{CAC1} = \left(U_0 + \frac{\hat{U}_{grid}}{2} \cdot \sin(\omega \cdot t) \right), \tag{4.13}$$

$$u_{CAC2} = \left(U_0 - \frac{\hat{U}_{grid}}{2} \cdot \sin(\omega \cdot t) \right), \tag{4.14}$$

$$U_0 \geq \frac{U_{grid}}{\sqrt{2}}, \tag{4.15}$$

$$u_{out} = u_{CAC1} - u_{CAC2} = \hat{U}_{grid} \cdot \sin(\omega \cdot t), \tag{4.16}$$

Claim: Good power decoupling has not yet been possible for single-stage inverters, without including a large energy-buffering capacitor in parallel with the PV module!

A more ingenious solution is to use the included AC capacitors as energy-buffers. The voltages across the capacitors still have to comply with (4.13) to (4.16), but the bias can be controlled in order to eliminate the ripple. The proposed decoupling scheme is also usable for the DC-AC boost converter in [67], [68], [69] and the isolated Ćuk inverter in parallel-parallel connection.

The required DC bias across the AC capacitors, in order to obtain a high power decoupling and inject a sinusoidal current into the grid is given as [66]:

$$u_0 = \sqrt{\underbrace{\frac{2\cdot\left(P_{PV}-P_{grid}\right)\cdot t}{C_{AC}}}_{1^{st}} + \underbrace{\frac{P_{grid}\cdot\sin\left(2\cdot\omega\cdot t\right)}{\omega\cdot C_{AC}}}_{2^{nd}} - \underbrace{\left(\frac{\hat{U}_{grid}}{2}\cdot\sin\left(\omega\cdot t\right)\right)^2}_{3^{rd}} + \underbrace{U_0{}^2}_{4^{th}}}\,, \tag{4.17}$$

The 1st term under the square-root sign comes from non-unity efficiency ($P_{PV} > P_{grid}$). Hence, this term approaches infinite as time goes by! This is highly undesirable when computing the reference, thus the term must be reset every now and then, or it can simply be omitted by recognizing that we only want to eliminate the ripple in the PV power and not effects caused by non-unity efficiency. The 2nd term originates from the power injected into the grid. The 3rd term comes from the original sinusoidal voltages across the AC capacitors according to (4.13) and (4.14), and the 4th part is the initial voltage.

Simulation results in [66] revealed that the inverter operates a desired, i.e. good power decoupling with small capacitors. However, the currents inside the circuit are rather high, which leads to high power losses (U_{MPP} = 28 V, P_{MPP} = 160 W, U_{grid} = 230 V).

4.3.2 Flyback Converter With LF DC-AC Inverter (Mekhilef, *et al*. and Achille, *et al.*)

The topology in Figure 4.14 is a 150-Watt flyback DC-DC converter together with a LF DC-AC unfolding inverter [70]. Another author [57] applies the same topology for a 100-Watt inverter, except that the grid-filter is removed from the DC-link to the grid-side. The LF DC-AC inverter is in both cases equipped with thyristors, which can be troublesome to turn on, since they require a current into their control terminal.

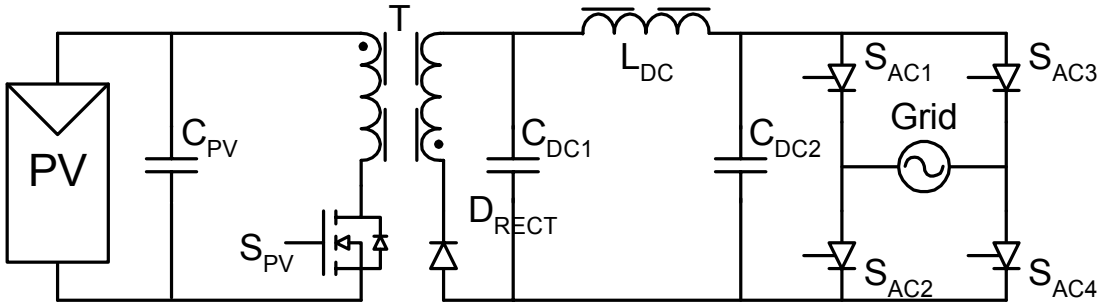

Figure 4.14. Flyback DC-DC converter with unfolding DC-AC inverter [70].

Nothing is stated about the mode of operation of the flyback converter, but it is presumable DCM.

Test results in [70] show good control of the grid current, but no values are given (U_{MPP} = 44 V, P_{MPP} = 150 W, U_{grid} =120 V).

4.3.3 Flyback Converter With PWM DC-AC Inverter (Martins, *et al.*)

The next inverter is a 100-Watt flyback DC/DC converter together with a PWM DC/AC inverter, cf. Figure 4.15 [71], [72].

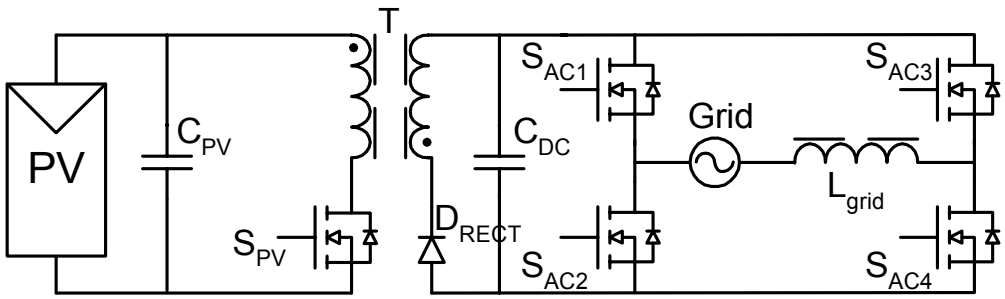

Figure 4.15. Flyback DC-DC converter with PWM inverter [71], [72].

The output stage is now made up around four transistors, which are switched at high frequency. The grid current is modulated by alternately connecting the positive or the negative DC-link voltage (the constant voltage across across C_{DC}) to the inductor L_{grid} in $D \cdot T_{sw}$ seconds, and zero voltage in $(1\text{-}D) \cdot T_{sw}$ (D is the duty cycle and T_{sw} is the switching period). This kind of operation is attractive, since the capacitor C_{DC} now decouples the PV module and the grid. The DC voltage across the capacitor is in the range $230 \cdot \sqrt{2} \cdot (0.85 \ldots 1.10)$ = from 275 V to 360 V. Thus, its size in farads can be much smaller, e.g. 33 µF according to chapter 5, and still obtain the same level of power decoupling as for a 2.2 mF capacitor in parallel with the PV module. This is a reduction of 67 times.

The flyback converter is operated in CCM. This was not desirable for the other flyback topologies, since they had to control the grid current in a direct way. But it is advantageous now since the PWM inverter modulates the grid current. The HF current stress of transistor S_{PV} and the capacitor C_{PV} are in this way reduced to an absolute minimum; the same is true for the losses within these components. A regeneration clamp circuit is applied for the transistor on the PV-side.

Besides this, it becomes sufficient to design the flyback converter for the nominal power, and not twice the nominal power as in the previous sections. The grid connected PWM inverter still has to be designed for twice the nominal power.

Test results in [71] show good control of the grid current, and an efficiency of 74% (U_{MPP} = 30 V, P_{MPP} = 100 W, U_{grid} =212 V).

4.3.4 Series Resonant Converter With Bang-Bang DC-AC Inverter (Lohner, *et al.* and Meinhardt, *et al.*)

The inverter in Figure 4.16 is based on a 110-Watt series resonant DC-DC converter with a HF inverter towards the grid [73], and 250-Watt in [74].

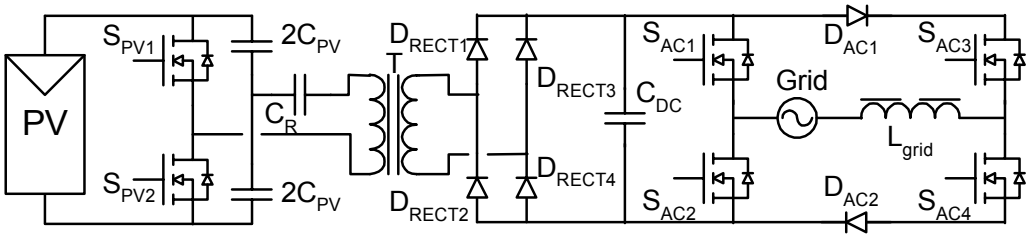

Figure 4.16. Series resonant DC-DC converter with bang-bang DC-AC inverter [73], [74].

The inverter towards the grid is modified in such a way that is can't operate as a rectifier, seen from the grid-side. Adding the diodes D_{AC1} and D_{AC2} in Figure 4.16 will do this. The advantage of this solution is that no inrush current flows when the inverter is connected to the grid for the first time.

The DC-DC converter is based on the series resonant converter, where the leakage inductance in the transformer together with the capacitor inserted in series with the transformer forms a resonant-tank. The resonant tank together with the output-capacitances of the transistors makes the inverter zero-voltage switching. The DC-DC converter is operated at 100 kHz with a duty-cycle slightly smaller than 50% in order to avoid shoot-through. The converter runs in this way with a fixed voltage transfer ratio as a 'DC-transformer'. Thus, no power decoupling is achieved between the PV module and the grid. The switching losses from the DC-DC converter are almost completely avoided but higher losses are expected to appear in the transformer, due to higher currents when compared to a normal non-resonant DC-DC converter. The diodes in the rectifier are current-commutated by the use of the series resonant converter, which produces smaller reverse-recovery losses in the diodes. The efficiency of the series resonant converter is high at low load, but decreases as the load increases, due to high conduction losses [75].

The grid-connected inverter uses both high and low switching frequencies. The left leg in the inverter is controlled by means of a bang-bang controller, alias a hysteresis-band controller. When the absolute error into the controller reaches a certain value, the left leg makes a switch transition that causes the error to fall. This part of the inverter operates at switching frequencies between 20 kHz and 80 kHz depending of the instantaneous grid voltage and commanded current. The right leg of the inverter is switched according to the polarity of the grid voltage, i.e. at 100 Hz. The switching losses are in this way reduced by a ratio of two compared to inverters where both legs are switching at high frequency.

Test results in [74] show good control of the grid current (P_{MPP} = 250 W, U_{grid} =230 V).

The next inverter presented here utilizes the same layout as in [74], cf. Figure 4.16. The inverter given in [73] makes use of integrated magnetic circuits. This means that all the inductors and transformers are incorporated into the Printed Circuit Board (PCB) by means of planar magnetics. The resonant inductor and transformer for the DC-DC converter are made as one magnetic circuit. This is done in order to increase the efficiency and to decrease the cost and size. Two inductors, each of 500 μH, is used towards the grid, they are also put into the PCB. However the power losses in the grid-tied inductors are increased from 100 mW to 500 mW when changing the technology from an ordinary toroidal core to the more sophisticated planar magnetics. The DC-DC converter is switching at 500 kHz in a series-resonant configuration and the grid-connected inverter is switching with 100 Hz. This means that the two stages are not decoupled and a large capacitor is required in parallel with the PV module in order to attenuate the power ripple. Then again the benefit is the total removal of the switching losses in the grid-connected inverter.

Test results in [73] show an efficiency of 87% (U_{MPP} = 30 V, P_{MPP} = 110 W, U_{grid} =230 V).

4.3.5 Series-Parallel Resonant Converter With Unfolding Inverter (Prapanavarat, *et al.*)

The inverter in Figure 4.17 is a 110-Watt Series-parallel resonant DC-DC converter with an LF unfolding inverter [76]. The efficiency for a series-parallel resonant converter is low at medium load but increases with the load [75].

The use of the series-parallel resonant converter is advantageous in this case, since it combines the load-dependent characteristic of the series-resonant converter and the capability to operate at very light load from the parallel-resonant converter. Again, both stages must be designed for twice the nominal power, and a large capacitor must be placed in parallel with the PV module in order to achieve power decoupling.

No test results are shown in [76].

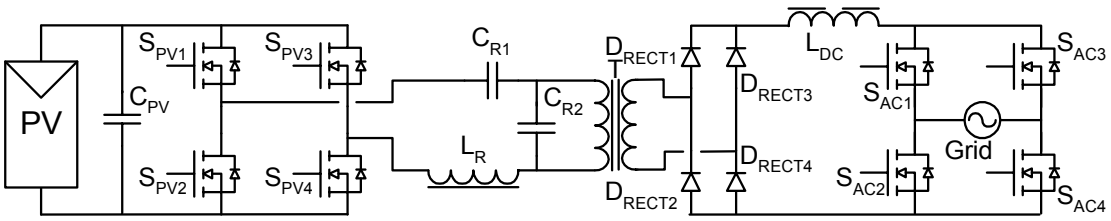

Figure 4.17. Series-parallel resonant DC-DC converter with unfolding DC-AC inverter [76].

4.4 Topologies from Commercial Inverters

4.4.1 OK4E by NKF Electronics, the Netherlands

The first commercial inverter presented is the 100-Watt OK4E [77], [78]. The topology is shown in Figure 4.18. It is made up around a series resonant DC-DC converter. The converter generates a series of unipolar current pulses (between zero and a positive value). This signal is filtered such that only the low frequency remains. The remaining is a rectified sinusoidal waveform, which are 'unfolded' in the next stage to a real sine wave. The switching frequency of the unfolding circuit is 100 Hz.

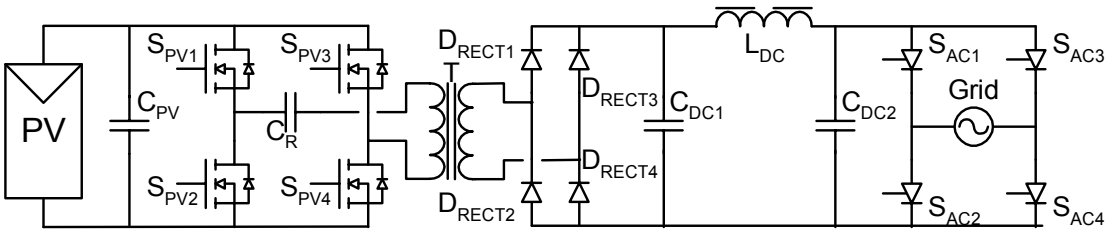

Figure 4.18. OK4E commercial inverter [77], [78].

The modulator for the high frequency DC-DC converter is made with an analogue circuit because it is not yet possible to implement these high frequency modulators in digital circuits, e.g. microprocessors and FPGAs. The remaining control is put into practice by means of a microprocessor that includes the following functions: sine modulation, MPPT, islanding protection. An RS485 interface is also included in the OK4E to enable monitoring and inspection of the circuit.

A final remark is given on the mode of operation below 3% of the rated power [79]. Burst mode operation intends to transform the constant losses from gate drivers, magnetics, etc. into variable losses and in this way to decrease the inverter losses at low irradiance. Besides this, the DC-DC converter may have problems with reaching zero-voltage switching at low generation, which is mitigated by the burst mode operation.

Instead of letting the inverter run all the time at a constant low power, the inverter is turned off and the energy generated from the module is used to charge the decoupling capacitor, C_{PV}, up to $U_{MPP} + \Delta U$. When this limit is reached the inverter wakes up and discharge the capacitor to a voltage level of $U_{MPP} - \Delta U$, see Figure 4.19. This is done at a power level that is close to the inverters optimum, i.e. at highest efficiency.

The grid current is then composed of one or more full-length sine waves when the inverter is running together with some breaks where no power is injected into the grid. Low irradiance gives single bursts with a long break between them and medium irradiance correspond to longer periods of bursts with shorter breaks between them.

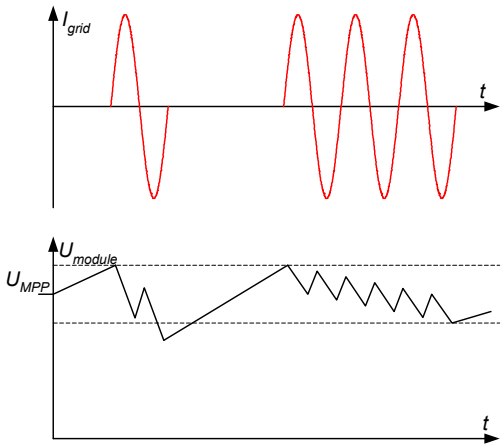

Figure 4.19. Rare and frequent bursts at low and medium irradiance [79].

This mode of operation is only acceptable up to a certain power level, since injecting high power bursts into the grid will cause flicker, which must be avoided. On the other hand, an inverter with nominal power of a few hundred Watts (maximum 500 W, c.f. chapter 3), operating in burst mode below 10% of rated power, cannot create flicker. The power level is simply too low. However, it can be a problem for high power inverters.

Test results in [77] show an efficiency better than 90% over a wide generation range. The power factor is reported better than 0.98 above 50% generation (U_{MPP} = 30 V, P_{MPP} = 110 W, U_{grid} =230 V).

4.4.2 Gridfit 250 by Exendis, the Netherlands / Germany

No diagram is available for the Exendis Gridfit 250-Watt inverter in Figure 4.20. However, it is believed that a DC-DC converter composes the inverter with belonging unfolding LF DC-AC inverter (based on material from Paderborn University, who designed the circuit [80], [81]).

Figure 4.20. Snapshot of the Gridfit 250 inverter.

Test results in [82] claims an European efficiency better than 90%, and standby losses of 0.008 W. The PV module voltage range is defined within 27 V to 50 V, which also is close to the specifications given in Chapter 3.

4.4.3 Soladin 120 by Mastervolt, the Netherlands

The Soladin 120 inverter is a 'plug and play' inverter, based on the topology in Figure 4.21. An inside view of the Soladin 120 is depicted in Figure 4.22. The nominal input power is 90 W at 20 V to 40 V, but the opportunity to operate at peak power of 120 Watt exists.

The push-pull converter (formed by the MOSFETs S_{PV1} and S_{PV2}, the transformer T, and the four diodes D_{RECT1} to D_{RECT4}) is operated in PWM current mode control by a UCC3806 controller. This is beneficial, since even small differences in voltage drops and conduction times for the MOSFETs can result in transformer saturation [61]. A PIC microcontroller generates the reference signal to the UCC3806.

The only signal transferred across the galvanic barrier (the transformer) is the measured grid voltage. This is done with a differential connected OPAMP. Thus, the four MOSFETs (S_{AC1} to S_{AC4}) in the unfolding stage must be 'auto-switching' in the sense that they are controlled by the grid voltage. The inductor L_{grid} in Figure 4.21 is actually formed by two inductors, where one of them is believed to provide power and control-signals to the unfolding inverter.

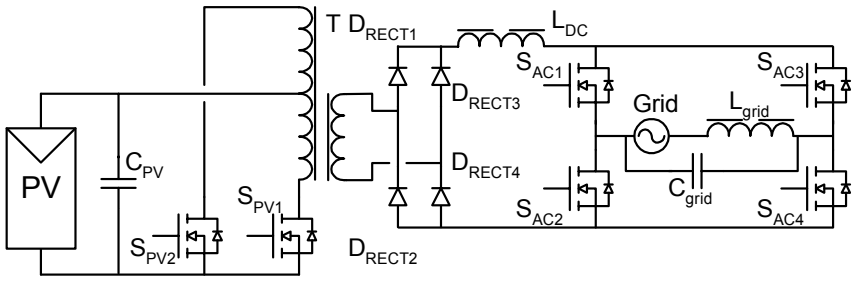

Figure 4.21. Soladin 120 commercial inverter. The schematic is estimated by reverse engineering.

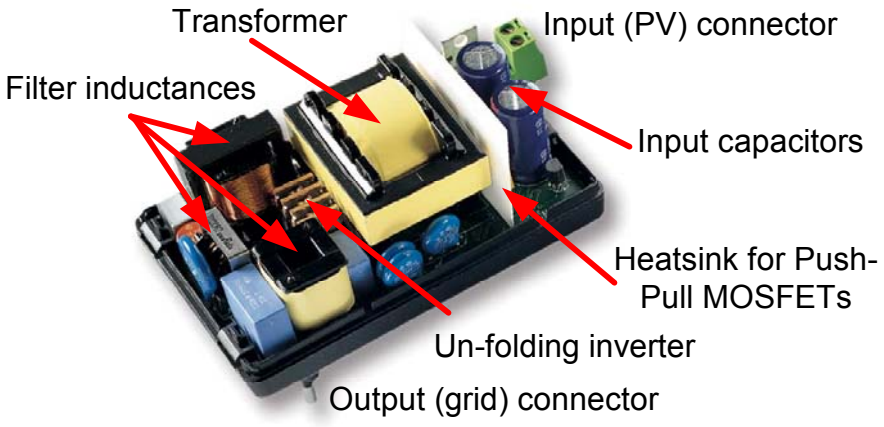

Figure 4.22. A view of the SOLADIN 120 inverter.

Thus, the Soladin 120 inverter is a dual-stage topology without inherent power decoupling. The capacitor in parallel with the PV module is therefore rather larger (2 × 1000 μF @ 50 V, 1000 h lifetime at 105°C), since it must work as an energy buffer. According to the work in Chapter 2, this result in a small-signal amplitude in the range from 1.8 V to 3.0 V, which corresponds to a PV utilization factor from 0.984 to 0.993 at full generation.

No information is gained about the control of the grid current. However it is believed that the inverter applies some kind of sensor-less control, where the instantaneous grid current is estimated on basis of some other measured variables, e.g. instantaneous current into the push-pull converter.

The applied MPPT algorithm is very simple. It simply assumes that the MPP voltage is equal to the open circuit voltage minus 10 V. This is a fast and easy method, but the tracking of the MPP is poor.

The power factor is reported to 0.99 at full generation. The peak efficiency is recorded to 93% at 40 W, and the European efficiency is calculated to 91%.

4.5 Comparison and Selection

Next follows a comparison of the presented topologies, in order to find the best candidate for a 160-Watt AC module. Some of the topologies are not included, since they are known to have problems with high current- and voltage-stress, etc., or are too complex. The selected inverters are investigated for component-stress and -ratings, relative cost and efficiency. The comparison is based on the initial design in appendix F.

The topologies shown previously are re-arranged in order to lighten up the calculation burden. Thus, the various parts of the stages inside the inverters are divided into three parts. Parts A to D is the input stage, from the PV module to the primary transformer winding, cf. Figure 4.23. Parts 1 to 4 are from the secondary transformer winding to the grid for the HF-link inverters, or to the input of the grid-connected inverter for the DC-link inverters, cf. Figure 4.24. Finally, parts α and β are from the output of the DC-link to the grid, cf. Figure 4.25.

Note that only 24 valid combinations exists out of the 4×4×2 = 32 possible solutions. Out of the 24 combinations, only 13 are valid inverter topologies, of witch 8 are investigated with respect to ratings, cost, and European efficiency.

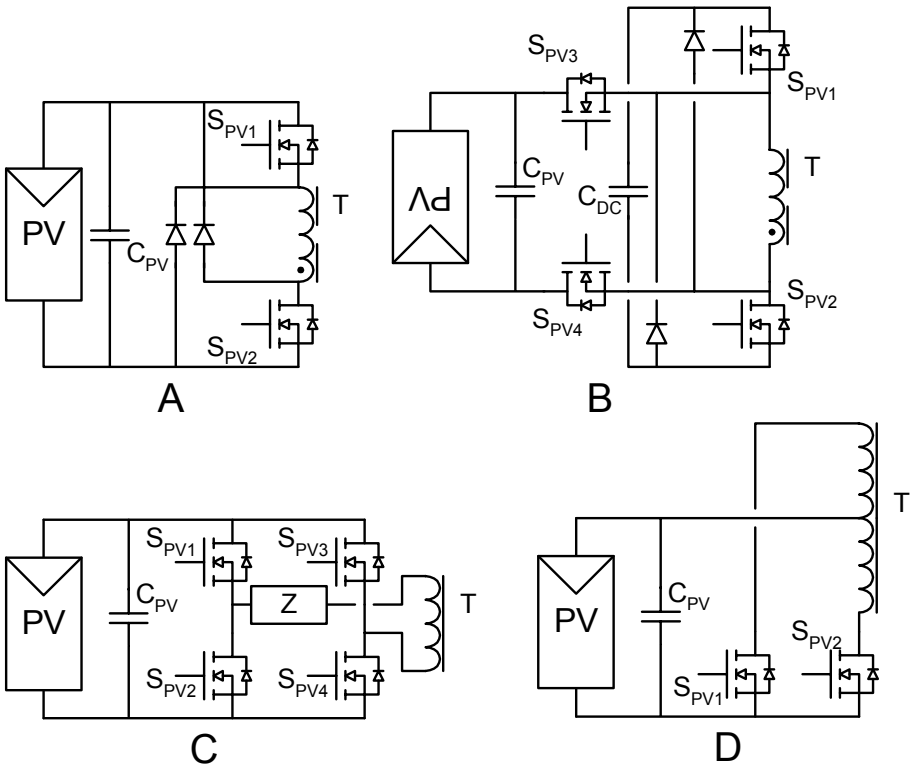

Figure 4.23. Parts A to D are the possible input stages, from the PV module to the primary transformer winding.

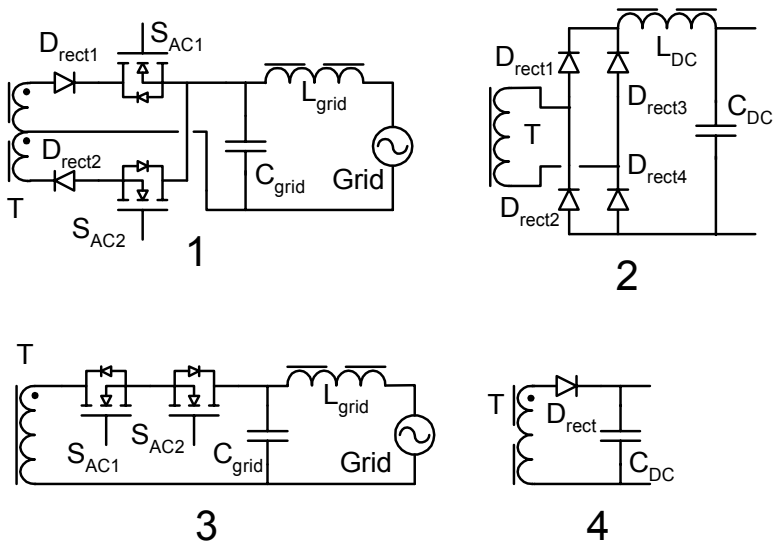

Figure 4.24. Parts 1 to 4 are the possible configurations from the secondary transformer winding to the grid for the HF-link inverters, or to the input of the grid-connected inverter for the DC-link inverters.

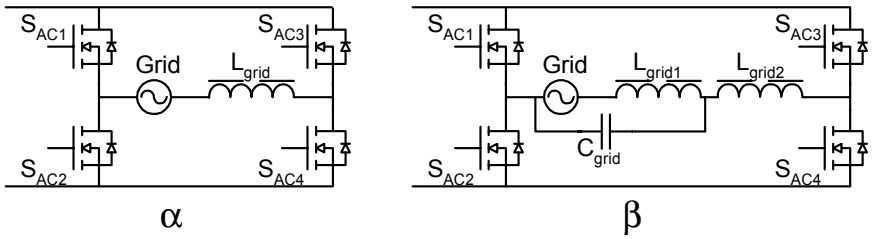

Figure 4.25. Parts α (LF unfolding inverter) and β (HF PWM inverter) are from the output of the DC-link to the grid.

The following electrical specifications are assumed for the purpose of the analysis:

- Nominal PV power is 160-Watt,
- MPP voltage is in the range from 23 V to 38 V, and 45 V at open circuit,
- Grid voltage is in the range from 195 V to 253 V (RMS values),
- Nominal grid voltage is 230 V at 50 Hz,
- Nominal DC-link voltage is 350 V,
- The stages are designed for the worst possible operating point: P_{MPP} = 160 W, U_{MPP} = 23 V, and U_{grid} = 195 V, but must also be operational at U_{OC} = 45 V, and U_{grid} = 253 V.

The following operating conditions are assumed to compare the different topologies:

- Flyback types of inverters are operated at 50 kHz, PWM types DC-DC converters are operated at 110 kHz, and grid-connected PWM inverters are operated at 10 kHz.
- DC-link inductors are operated in CCM down to 5% irradiation (8 W), which corresponds to a maximum ripple current of 46 mA, peak to peak.
- The average current ripple in the innermost grid connected inductor (or DC-link inductor) is equal to 50% of nominal RMS current at nominal voltage ($<\Delta i_L>$ = 0.36 A peak to peak) [83],

$$L = \frac{\hat{u}_{grid}}{\langle \Delta i_L \rangle \cdot f_{sw}} \cdot \left(\frac{1}{\pi} - \frac{m_a}{4} \right), \; m_a = \frac{\hat{u}_{grid}}{U_{DC}}, \tag{4.18}$$

- The copper fill factor, K_U, is 0.40 for transformers and 0.60 for inductors,
- The maximum flux density within magnetic cores is limited to 300 mT.

The following efficiencies are assumed for computing the size of the components:

- Unity efficiency for calculating the component stress',
- 90% efficiency for calculating the de-rating factor (10 W loss in PV-side MOSFETs, 4 W loss in grid-side MOSFETs, and 2 W loss in rectifier diodes),

The following thermal values are assumed:

- The difference between hotspot- and ambient- temperature, for magnetics, must not exceed 40 °C, since it is known that ferrites has lowest loss coefficients at a temperature around 100 °C (temperature inside encapsulation = 60 °C),
- The junction temperature of the semiconductors are not allowed to exceed 100 °C in order to maintain a high reliability (temperature outside encapsulation = 40 °C),

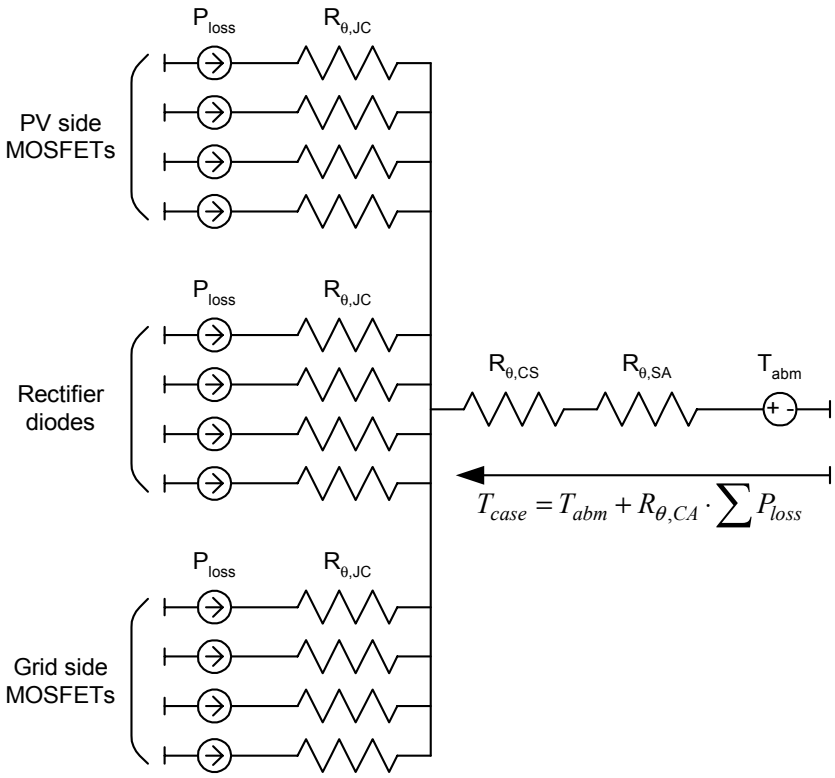

Figure 4.26: Sketch of the thermal circuit of the inverter, with the most important components. The thermal resistances are: $R_{\theta,JC}$ = 1.0 K/W, $R_{\theta,CA}$ = 3.2 K/W. The worst-case case-temperature is estimated to 16 W ·3.2 K/W + 40 °C = 91 °C.

- Power semiconductors are mounted on the encapsulation of the inverter, which has outer dimensions of 5 cm × 10 cm × 10 cm and is assumed made from black oxidized aluminum. The thermal circuit is sketched in Figure 4.26. Thus, the thermal resistance from each semiconductor housing to ambient is estimated to [60]:

$$R_{\theta,CA} = R_{\theta,CS} + R_{\theta,SA} = 3.2\ K/W\ , \tag{4.19}$$

- The semiconductors are assumed housed in TO-220 encapsulations, with a thermal resistance of $R_{\theta,JC}$ = 1.0 K/W.

The values presented above is only to be used in the comparison of the different topologies, and may be subject to changes during an optimization process.

Table 4.2. Calculated maximum current- and voltage-stress, etc., of the components included in the eight investigated topologies. A) The diode is included in the structure of the MOSFET. B) Components included in the rating analysis.

Topology in Figure		4.7	4.9	4.12	4.14	4.15	2* Full	4.16	4.21
Code		A1-	B1-	C3-	A4α	A4β	C2β	C2β	D2α
Frequency [kHz] 1st and 2nd stage		50/0.1	50/50	50/0.1	50/0.1	50/10	110/10	110/10	50/0.1
C_{PV}	C [mF]	2.2	-	2.2		-	-	-	2.2
	û [V]	23-45	-	23-45		-	-	-	23-45
	I [A]	4.9	-	4.9		-	-	-	4.9
S_{PV}	û [V]	2*45	S1&2: 143 S3: 72 S4: 188	4*45	2*45	2*45	4*45	4*45	2*90
	I [A]	16.3	S1&2: 8.5 S3&S4: 12.7	11.5	16.3	12.8	8.0	7.2	7.6
T	I_{tot} [A]	40	24	33	33	26	23	20.4	30
	λ [μV·s]	190	445	190	190	182	95	96	200
	L_m [μH]	2.8	5.4	2.8	2.8	5.2	∞	∞	∞
	N [ ]	16	5.0	16	16	18	18	19	18
Z	L [μH]	-	-	-	-	-	-	3.0	-
	C [nF]	-	-	-	-	-	-	820	-
	û [V]	-	-	-	-	-	-	83	-
	I [A]	-	-	-	-	-	-	10.2	-
D_{rect}	û [V]	1080	1080	A)	1080	1170	810	405	810
	<I> [A]	0.37	0.37	0.37 A)	0.74	0.54	0.29	0.29	0.37
S_{AC}	û [V]	720	720	720	360	400	400	400	360
	I [A]	0.72	0.89	0.72	0.58	0.58	0.58	0.58	0.58
C_{grid}	C [μF]	1.5			See C_{DC}	1.3			See C_{DC}
	û [V]	± 360				± 360			
	I [A]	0.7	1.0	0.7		0.1			
L_{grid}	L [mH]	7.8 (Outermost inductor) B)				7.8 (Innermost inductor) B)			0.5
	î [A]	1.16				1.16			1.16
	I [A]	0.82				0.82			0.82
	$L\cdot\hat{I}\cdot I$ [H·A²]	$7.41\cdot10^{-3}$				$7.41\cdot10^{-3}$			$0.48\cdot10^{-3}$
L_{DC}	L [mH]	-	-	-	-	-	20	-	1.6
	î [A]	-	-	-	-	-	0.53	-	1.16
	I [A]	-	-	-	-	-	0.53	-	0.82
	$L\cdot\hat{I}\cdot I$ [H·A²]	-	-	-	-	-	$5.62\cdot10^{-3}$	-	$1.52\cdot10^{-3}$
C_{DC}	C [μF]	-	68 B)	-	1.5	33 B)			0.22
	û [V]	-	72-143	-	360	280-400			360
	I [A]	-	0.60	-	0.60	0.37			0.02

4.5.1 Maximum Component Stress

Next follows the calculated maximum stress of the components for eight topologies, cf. Table 4.2. The following parameters are computed: size of capacitors and inductors: C, and L, peak voltage across the components: û, average, peak and/or RMS values of the current through the components: <I>, Î, and I. The stress on the components is used in the next section to calculate the required ratings. The equations describing the voltage- and current-stress for the components are give in appendix F. The following changes are adopted:

- All single-transistor flyback inverters are upgraded to two-transistor flyback inverters in order to avoid the need for clamp circuits,
- Diodes in the main-path on the PV-side are removed (if they can be avoided),
- Filter inductors in front of the PV module is not included,
- The components are treated as being ideal (no leakage or resistances),
- On the PV-side: half-bridge converters are replaced with full-bridge converters.

4.5.2 Ratings

The VA rating for a power semiconductor is given as the peak voltage across the device multiplied with the maximum RMS current for MOSFETs, the maximum average current for diodes, and further divided with a de-rating factor, DF:

$$VA = \frac{\hat{U} \cdot I_D}{DF} \,. \tag{4.20}$$

The current is de-rated in order to lower the junction temperature from the 125 °C /150 °C in the datasheet to a more realistic value of maximum 100 °C, cf. section 4.5. The current de-rating factor for MOSFET' is computed as:

$$DF_I = \frac{I_D\big|_{Actual,Tcase=91^\circ C}}{I_D\big|_{Datasheet,Tcase=25^\circ C}} = \frac{\sqrt{\dfrac{T_{junc,1} - T_{case,1}}{R_{\theta,JC} \cdot R_{ds(on),1}}}}{\sqrt{\dfrac{T_{junc,2} - T_{case,2}}{R_{\theta,JC} \cdot R_{ds(on),2}}}} = \sqrt{\frac{T_{junc,1} - T_{case,1}}{R_{ds(on),1}} \cdot \frac{R_{ds(on),2}}{T_{junc,2} - T_{case,2}}} \,, \tag{4.21}$$

where the on-state resistance versus junction temperature is estimated as (from typical data sheet values):

$$R_{ds(on)}(T) = R_{ds(on),25^\circ C} \cdot \left(\frac{T}{125} + 0.80 \right). \tag{4.22}$$

The current de-rating for this particular situation becomes equal to $DF_I = 0.30$ for real case and junction temperatures of 91°C and 100 °C, respectively, and datasheet values of 25 °C and 150 °C, respectively. The voltage de-rating is equal to $DF_U = 0.75$, in order to avoid over-voltages and to increase the reliability [60]. The total de-rating factor is then computed to $DF = 0.75 \cdot 0.30 = 0.225$. This means that a MOSFET designed for a breakdown voltage of 60 V and a continuous drain current of 55 A (datasheet values) should not be exposed to voltages higher than 45 V and currents higher than 16.5 A.

The de-rating for diodes is also given by (4.20), except that the RMS value of the current now is substituted with the mean value, since the mean value is used to calculate the power losses in diodes. The voltage de-rating factor is now $DF_U = 0.80$, and the current de-rating factor is computed as:

$$DF_I = \frac{\langle I_D \rangle\big|_{Actual,Tcase=91^\circ C}}{\langle I_D \rangle\big|_{Datasheet,Tcase=25^\circ C}} = \frac{\left(\dfrac{T_{junc,1} - T_{case,1}}{R_{\theta,JC} \cdot U_{F,1}} \right)}{\left(\dfrac{T_{junc,2} - T_{case,2}}{R_{\theta,JC} \cdot U_{F,2}} \right)} = \frac{T_{junc,1} - T_{case,1}}{U_{F,1}} \cdot \frac{U_{F,2}}{T_{junc,2} - T_{case,2}} \,, \tag{4.23}$$

where the forward voltage drop versus junction temperature is estimated as (from typical data sheet values):

$$U_F(T) = U_{F,25^\circ C} \cdot \left(1.1 - \frac{T}{250} \right). \tag{4.24}$$

Thus, the current de-rating for this particular situation becomes equal to DF_I = 0.17. The total de-rating factor is then computed to DF = 0.80·0.17 = 0.136. This means that a diode designed for a breakdown voltage of 1000 V and a continuous current of 3 A (datasheet values) should not be exposed to voltages higher than 800 V and currents higher than 0.5 A.

The ratings for electrolytic capacitors are calculated as the maximum amount of energy they can store:

$$E_C = \tfrac{1}{2} \cdot C \cdot \hat{U}^2 . \tag{4.25}$$

Finally, the ratings for magnetics are based on the work in appendix E, where the geometrical core constants for transformers, AC inductors and DC inductors are given. The geometrical core constants are:

$$K_{g,Fe} = \frac{\rho \cdot {\lambda_1}^2 \cdot {I_{tot}}^2 \cdot \left(K_{Fe} \cdot {f_{sw}}^{\alpha}\right)^{(2/\beta)}}{4 \cdot K_U \cdot {P_{tot}}^{((\beta+2)/\beta)}} \cdot 10^8 , \tag{4.26}$$

$$K_{g,Fe} = \frac{\rho \cdot \lambda^2 \cdot I^2 \cdot \left(K_{Fe} \cdot {f_{sw}}^{\alpha}\right)^{(2/\beta)}}{2 \cdot K_U \cdot {P_{tot}}^{((\beta+2)/\beta)}} \cdot 10^8 , \tag{4.27}$$

for transformers (4.26) and AC inductors (4.27), and

$$K_g = \frac{\rho \cdot L^2 \cdot {I_{\max}}^2 \cdot I^2}{P_{Cu} \cdot K_U \cdot {B_{\max}}^2} , \tag{4.28}$$

for DC inductors (see appendix E for description of the variables).

Table 4.3. Computed ratings for the components in the eight topologies.

TOPOLOGY IN FIGURE 4.X		7	9	12	14	15	2* FULL	16	22
C_{PV}, C_{DC}	E [J]	2.75	0.87	2.75	2.75	3.34	3.34	3.34	2.75
S_{PV}	Number of dev.	2	4	4	2	2	4	4	2
	U_{BR} [V]	60	S1&2: 191 S3: 96 S4: 251	60	60	60	60	60	120
	I_D [A]	54	S1&2: 28 S3&S4: 42	38 (54)	54	43	27	24	25
	Tot. VA [kVA]	6.4	25.3	9.1	6.5	5.2	6.5	5.8	6.0
T	$K_{g,Fe}$ [cm^x]	0.0115	0.0173	0.0115	0.0115	0.0081	0.0041	0.0041	0.0115
	Core	ETD34	ETD39	ETD34	ETD34	ETD29	EFD30	EFD30	ETD34
Z	$K_{g,Fe}$ [cm^x]	-	-	-	-	-	-	0.009	-
	Core	-	-	-	-	-	-	EFD25	-
	E [J]	-	-	-	-	-	-	0.0033	-
D_{rect}	Number of dev.	2	2	0	1	1	4	4	4
	U_{BR} [V]	1350	1350	-	1350	1460	1010	505	1010
	I_D [A]	2.2	2.2	-	4.4	3.2	1.7	1.7	2.2
	Tot. VA [kVA]	5.9	5.9	-	5.9	4.7	6.9	3.4	8.9
S_{AC}	Number of dev.	2	2	2	4	4	4	4	4
	U_{BR} [V]	960	960	960	480	533	533	533	480
	I_D [A]	2.4	3.0	2.4	1.9	1.9	1.9	1.9	1.9
	Tot. VA [kVA]	4.6	5.8	4.6	3.6	4.1	4.1	4.1	3.6
L_{grid}	K_g [cm^5]	0.104	0.104	0.104	0.104	0.104	0.104	0.104	-
	Core	ETD29	ETD29	ETD29	ETD29	ETD29	ETD29	ETD29	-
L_{DC}	K_g [cm^5]	-	-	-	-	-	0.104	-	0.029
	Core	-	-	-	-	-	ETD29	-	EFD25
Points		32	27	32	34	33	26	28	31

Next follows the expected ratings. Only the ratings for the most important components are included, they are: PV-side capacitor C_{PV}, transistors S_{PV}, transformer T, and components in the resonant circuit, Z. Grid-side diodes D_{rect}, transistors S_{AC}, inductors L_{grid} and L_{DC}, and DC-link capacitor C_{DC}.

The results in Table 4.3 is colored (available in the digital version of the thesis) in green, yellow and red for the best, the medium, and the poor topologies. Green corresponds to four points, yellow to two points, and finally, red to one point. The points are summarized and displayed in the last row. Each of the four PV-side MOSFET' in the topology in Figure 4.12 must have the same ratings as each of the two MOSFET' in the topology in Figure 4.7 in order to have the same overall power loss.

*Table 4.4. Cost based on prices from Farnell-InOne, exclusive of VAT, fees, and shipping, third quarter of 2004 [Online]. The rectifying diodes marked with a * is composed by two diodes in series, in order to reach a high breakdown voltage.*

TOPOLOGY IN FIGURE 4.X		7	9	12	14	15	2* FULL	16	22
C_{PV}, C_{DC}	Capacitor [DKK]	14.87	8.46	14.87	14.87	16.88	16.88	16.88	14.87
S_{PV}	MOSFETs [DKK]	20.30	64.73	40.60	20.30	17.71	27.90	26.49	19.36
	Gate drivers [DKK]	10.00	20.00	20.00	10.00	10.00	20.00	20.00	10.00
T	Magnetics [DKK]	34.51	41.48	34.51	34.51	25.38	25.38	25.38	34.51
Z	Magnetics [DKK]	-	-	-	-	-	-	25.38	-
D_{rect}	Diodes [DKK]	8.62 *	8.62 *	-	7.28 *	6.01 *	9.55	6.11	11.57
S_{AC}	MOSFETs [DKK]	22.28	27.16	22.28	20.95	22.66	22.66	22.66	20.95
	Gate drivers [DKK]	10.00	10.00	10.00	20.00	20.00	20.00	20.00	20.00
L_{grid}	Magnetics [DKK]	25.38	25.38	25.38	25.38	25.38	25.38	25.38	-
L_{DC}	Magnetics [DKK]	-	-	-	-	-	25.38	-	25.38
	Total [DKK]	146.0	205.8	167.6	154.3	144.0	193.1	188.3	156.6

4.5.3 Cost

Next, the relative cost is estimated for the eight topologies, based on the data' in appendix D and the computed ratings. The estimated cost for the components and the inverters are given in Table 4.4. It is important, when making the comparison of the cost, that the housing of the applied semiconductors are the same within the three groups of semiconductors (PV and grid side MOSFET', and rectifier diodes). The prices of the inverters will otherwise have different biases, and the statistical uncertainty will be larger.

It is also essential that the thermal-resistances within the groups are comparative, while a cheap component with a high resistance demands a better heat sink for heat removal, and vice versa (the price for any heat sink is not included here).

The cost computed in this section is not an obtainable one, since many components have been omitted, e.g. connectors, PCB', microcontrollers, EMI-filters, etc. These components are assumed to be equal for all the topologies, and leaving them out of the comparison does therefore not change the overall conclusion.

4.5.4 European Efficiency

The efficiencies at six different operating points are calculated on the basis of the work in appendices C, E and F. The relationship between the on-resistance for the applied MOSFET' and their ratings are shown in Table 4.5. The losses in the eight topologies are broken down in Table 4.7, and the European efficiencies are computed in Table 4.6.

Table 4.5. The survey of the components in appendix D revealed that the average on-state resistance at 25 ℃ for the applied MOSFETs is given as:

Break down voltage Drain current	60 V	100 V	150 V	200 V	250 V	500 V	600 V	1000 V
1 – 3 A	-	-	-	-	-	3.6 Ω	3.7 Ω	5.4 Ω
20 – 30 A	61 mΩ	69 mΩ	80 mΩ	86 mΩ	-	-	-	-
30 – 40 A	37 mΩ	41 mΩ	-	-	51 mΩ	-	-	-
40 – 50 A	24 mΩ	-	-	-	-	-	-	
50 – 60 A	19 mΩ	-	-	-	40 mΩ	-	-	-

Table 4.6. Estimated efficiencies at the six different operating point, and weights for calculating the European efficiencies for the inverters.

Topology in figure 4.X		7	9	12	14	15	2*Full	16	22
Operating point	Weight								
5%	0.03	94.6%	63.8%	95.2%	95.2%	92.0%	92.0%	93.7%	94.1%
10%	0.06	94.2%	70.3%	94.9%	95.1%	91.7%	93.0%	93.7%	96.0%
20%	0.13	93.3%	70.5%	93.2%	93.5%	91.7%	93.2%	92.9%	96.4%
30%	0.10	92.8%	72.7%	93.5%	93.8%	91.3%	92.8%	92.0%	96.3%
50%	0.48	91.4%	71.0%	92.1%	92.5%	90.2%	91.8%	90.4%	95.6%
100%	0.20	88.3%	65.4%	89.0%	89.5%	88.5%	88.8%	86.9%	93.6%
European Efficiency		91.4%	69.7%	92.0%	92.4%	90.3%	91.6%	90.5%	95.4%

Table 4.7. Loss break down for the eight topologies, all in Watts. The losses are estimated for the most important components at six different working points, in order to calculate the European efficiency, η_{EU}.

Topology in Figure 4.x		7	9	12	14	15	2* Full	16	22
Component	Operating-point								
C_{PV}, C_{DC}	5%	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
	10%	0.01	0.02	0.01	0.01	0.00	0.00	0.00	0.01
	20%	0.04	0.08	0.04	0.04	0.01	0.01	0.01	0.04
	30%	0.09	0.18	0.09	0.09	0.02	0.02	0.02	0.09
	50%	0.24	0.47	0.24	0.24	0.05	0.05	0.05	0.24
	100%	0.94	1.51	0.94	0.94	0.17	0.17	0.17	0.94
S_{PV}	5%	0.09+0.10	0.35+2.25	0.09+0.10	0.09+0.10	0.08+0.10	0.01+0.02	0.02	0.01+0.03
	10%	0.28+0.17	1.05+3.35	0.28+0.17	0.28+0.17	0.22+0.16	0.04+0.04	0.09	0.03+0.07
Conduction	20%	0.81+0.28	3.08+4.95	0.81+0.28	0.81+0.28	0.65+0.24	0.18+0.09	0.40	0.14+0.15
&	30%	1.48+0.36	5.69+6.19	1.48+0.36	1.48+0.36	1.19+0.30	0.41+0.14	0.92	0.31+0.23
Switching	50%	3.16+0.47	12.0+8.10	3.16+0.47	3.16+0.47	2.54+0.38	1.13+0.22	2.47	0.86+0.37
	100%	8.30+0.59	30.4+11.1	8.30+0.59	8.30+0.59	6.68+0.44	3.95+0.36	7.85	3.01+0.62
Transformer	5%	0.02+0.01	0.03+0.01	0.01+0.01	0.01+0.01	0.01+0.01	0.24+0.00	0.02+0.00	0.34+0.00
	10%	0.05+0.02	0.07+0.02	0.03+0.02	0.03+0.02	0.02+0.02	0.24+0.00	0.03+0.00	0.35+0.00
Core & Wire	20%	0.10+0.06	0.14+0.05	0.06+0.05	0.06+0.05	0.05+0.06	0.25+0.01	0.06+0.02	0.36+0.02
	30%	0.14+0.12	0.21+0.10	0.09+0.10	0.09+0.10	0.07+0.10	0.25+0.02	0.08+0.04	0.36+0.04
	50%	0.22+0.25	0.33+0.21	0.14+0.20	0.14+0.20	0.11+0.22	0.25+0.04	0.11+0.11	0.35+0.10
	100%	0.35+0.65	0.53+0.53	0.22+0.53	0.22+0.53	0.17+0.57	0.23+0.14	0.16+0.34	0.33+0.34
Z	5%	-	-	-	-	-	-	0.08+0.02	-
	10%	-	-	-	-	-	-	0.10+0.05	-
Capacitor	20%	-	-	-	-	-	-	0.11+0.12	-
Inductor	30%	-	-	-	-	-	-	0.13+0.20	-
	50%	-	-	-	-	-	-	0.15+0.40	-
	100%	-	-	-	-	-	-	0.19+1.02	-
D_{rect}	5%	0.08+0.09	0.04+0.19	-	0.08+0.09	0.06+0.09	0.06+0.02	0.06+0.01	0.08+0.01
	10%	0.18+0.13	0.09+0.28	-	0.18+0.13	0.13+0.13	0.13+0.04	0.13+0.02	0.18+0.03
Conduction	20%	0.36+0.19	0.18+0.40	-	0.36+0.19	0.27+0.19	0.27+0.10	0.27+0.05	0.36+0.06
& Switching	30%	0.56+0.23	0.28+0.49	-	0.56+0.23	0.41+0.23	0.41+0.14	0.41+0.07	0.56+0.09
	50%	0.92+0.30	0.46+0.63	-	0.92+0.30	0.67+0.30	0.67+0.24	0.67+0.12	0.92+0.14
	100%	1.64+0.40	0.82+0.84	-	1.64+0.40	1.19+0.40	1.19+0.42	1.19+0.21	1.64+0.26
S_{AC}	5%	0.05	0.10	0.09+0.09	0.01	0.01+0.30	0.01+0.30	0.01+0.30	0.01
	10%	0.16	0.31	0.25+0.13	0.03	0.03+0.64	0.03+0.64	0.03+0.64	0.03
Conduction	20%	0.45	0.92	0.63+0.19	0.15	0.13+1.34	0.13+1.34	0.13+1.34	0.15
&	30%	0.82	1.71	1.10+0.23	0.34	0.31+2.02	0.31+2.02	0.31+2.02	0.34
Switching	50%	1.75	3.58	2.21+0.30	0.92	0.83+3.33	0.83+3.33	0.83+3.33	0.92
	100%	4.61	8.53	5.43+0.40	2.91	2.62+6.00	2.62+6.00	2.62+6.00	2.91
L_{grid}	5%	0.00	0.00	0.00	0.00	0.00	0.00	0.00	-
	10%	0.01	0.01	0.01	0.01	0.01	0.01	0.01	-
	20%	0.06	0.06	0.06	0.06	0.06	0.06	0.06	-
	30%	0.14	0.14	0.14	0.14	0.14	0.14	0.14	-
	50%	0.38	0.38	0.38	0.38	0.38	0.38	0.38	-
	100%	1.22	1.22	1.22	1.22	1.22	1.22	1.22	-
L_{DC}	5%	-	-	-	-	-	0.00	-	0.00
	10%	-	-	-	-	-	0.01	-	0.00
	20%	-	-	-	-	-	0.04	-	0.01
	30%	-	-	-	-	-	0.09	-	0.02
	50%	-	-	-	-	-	0.24	-	0.06
	100%	-	-	-	-	-	0.75	-	0.18
Total	5%	0.44	2.97	0.39	0.39	0.66	0.66	0.52	0.48
Losses	10%	1.01	5.20	0.90	0.86	1.46	1.23	1.10	0.70
	20%	2.71	10.7	2.48	2.36	3.00	2.48	2.57	1.29
	30%	3.94	15.0	3.59	3.41	4.79	3.95	4.34	2.04
	50%	7.69	26.1	7.10	6.73	8.81	7.38	8.62	3.96
	100%	18.7	55.5	17.6	16.8	18.5	18.0	21.0	10.2

4.6 Conclusion and Summary

Based on the previous analyses on inverter lifetime, cable losses, recent state-of-the-art, component stress, component ratings, relative cost and European efficiency, a conclusion is now stated, in which the fittest topology for a 160-Watt AC module is identified. An outline of the investigated topologies is given below.

Topology in figure	4.7	4.9	4.12	4.14	4.15	2*Full	4.16	4.21
Lifetime	😐	☹	😐	😐	☺	☺	☺	😐
Ratings	☺	😐	☺	☺	☺	😐	😐	☺
Relative cost [DKK]	146	206	168	154	144	193	188	157
European efficiency [%]	91.4	69.7	92.0	92.4	90.3	91.6	90.5	95.4

Regarding life time, a happy smiley is given to these topologies which have low power loss in the power decoupling electrolytic capacitor. A sad smiley is given to these topologies which have high power loss in the capacitor. This is rational since the temperature inside the electrolytic capacitors is the main lifetime limiting factor, cf. section 4.1.2.

A happy Smiley is also given to these topologies, which utilities the used components best. This is also reflected in the relative cost, which is based on the computed rating and a survey within different components.

The relative cost must NOT be interpreted as an obtainable price for the respective inverters, since the price versus ratings for the components is estimated by a survey of Farnell-InOne prices and linear regression between ratings and prices. Besides this, components have been omitted if they are assumed equal for all the topologies, e.g. microcontrollers, dedicated control circuits, measuring circuits, etc. The relative cost should instead by interpret as a weighting of the computed ratings.

Finally, the calculated European efficiency is NOR an available one, since some losses have been omitted, e.g. the self-supply which could amount from 2 W to 10 W, and additional core losses in the flyback-transformers due to the proximity effect (can not be avoided by interleaving the windings, as in a normal transformer [61]).

When these restrictions have been pinpointed, the topology in Figure 4.21 seems to be the best candidate for a high reliable, low cost, and high efficient, 160-Watt inverter for AC module applications.

Another comparison was conducted in 2002 [43], as part of the ‘Solcelle Inverter’ project, from which this Ph.D. is a spin off. The result in [43] is different from the one obtained above, since it pinpoint the dual full-bridge inverter (mentioned as the 2*Full inverter in this chapter) as being the best candidate for an AC module inverter.

The dual-full-bridge inverter, and not the inverter identified in this chapter, was designed in [83] as consequence of [43]. This is why the inverter to be designed in the next chapter is the dual full-bridge inverter, and not the one in Figure 4.21.

Chapter 5

Design of the Photovoltaic Inverter

The design of a power-electronic inverter depends on many issues, such as silicon devices; magnetics; capacitors; gate drives; grid performance; current-, voltage- and temperature-sensing and -protection; control strategies; and implementation, etc., which all must be covered.

The inverter to be designed was selected in chapter 4, and is illustrated in Figure 5.1. An overview of the designed components is given last this chapter, section 5.3.

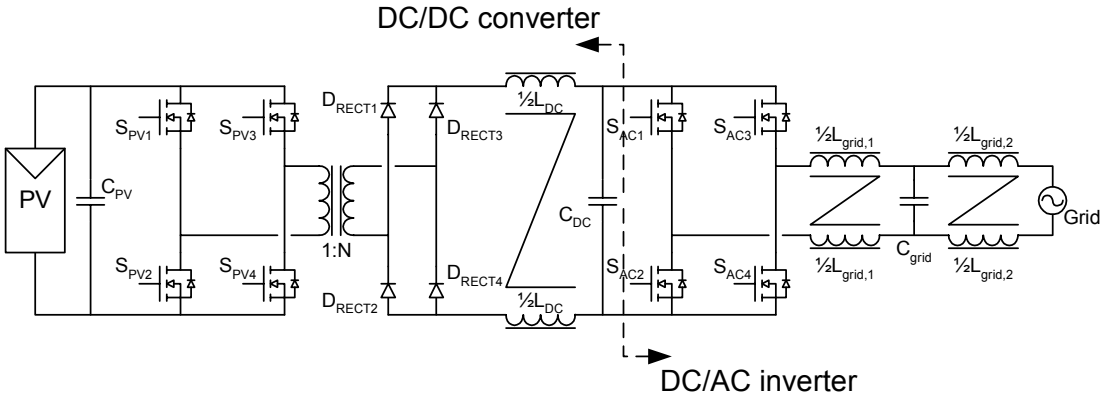

Figure 5.1. Power circuit of the photovoltaic inverter.

The design of the inverter is based on the specifications given in chapter 3. They are shortly reproduced here:

- Nominal photovoltaic power: 160 W,
- Input voltage range, MPP and open circuit: 23 V to 38 V, 50 V max,
- Maximum input current: 8 A,
- LF-voltage at input terminals (100 Hz): 4.1 V, amplitude,
- RF-voltage at input terminals (up to 0.5 MHz): 0.50 V, peak to peak,
- PV-side over-voltage protection limit: 60 V,
- Grid voltage range: 196 V to 253 V, RMS,
- Grid frequency range: 49.5 Hz to 50.5 Hz,
- Current harmonics: According to EN61000-3-2,
- Radio frequency disturbance: According to EN55014,
- Min., nom., and max. DC-link voltage: 300 V, 350 V, and 400 V.

Other demands are (partly from chapter 4, and may be subject to changes in an optimization process):

- DC/DC converter switching frequency: ~ 110 kHz,
- DC/AC inverter switching frequency: ~ 10 kHz,
- Maximum semiconductor junction temperature: 100 °C,
- Maximum case temperature: 90 °C,
- Maximum ambient temperature: 60 °C,

5.1 Grid-Connected DC-AC Inverter

The DC-AC inverter is depicted in Figure 5.1(right). The inverter is made up around a DC-link capacitor C_{DC}, four MOSFETs with freewheeling diodes $S_{AC1} - S_{AC4}$, and an LCL filter composed by $L_{grid,1}$, C_{grid}, and $L_{grid,2}$.

5.1.1 Mode of Operation

The four MOSFETs are operated with PWM, in what is called uni-polar mode. This operation scheme benefits from an apparent doubling of the switching frequency, seen by the grid [60]. A doubling of the frequency causes a halving of the current ripple towards the grid. Hence, smaller filter components are required to meet the electrical-noise reduction specifications.

The voltage generated across the output filter is (see also Fig. 6.21):

$$\begin{aligned} u_{LCL,on} &= U_{DC} - u_{grid}, \quad \text{when } S_{AC2} \text{ and } S_{AC3} \text{ are conducting,} \\ u_{LCL,on} &= -U_{DC} - u_{grid}, \quad \text{when } S_{AC1} \text{ and } S_{AC4} \text{ are conducting,} \\ u_{LCL,off} &= -u_{grid}, \quad \text{when } S_{AC1} \text{ and } S_{AC3}, \text{ or } S_{AC2} \text{ and } S_{AC4} \text{ are conducting,} \end{aligned} \tag{5.1}$$

where U_{DC} is the voltage across the DC-link capacitor (assumed constant), and u_{grid} is the instantaneous grid voltage, which is defined from –325 V to 325 V (corresponds to a RMS value of 230 V). The change in the grid current per switching cycle is then computed as:

$$\Delta i_{grid} = \frac{(U_{DC} - u_{grid}) \cdot D}{2 \cdot L_{grid} \cdot f_{sw}} + \frac{(0 - u_{grid}) \cdot (1 - D)}{2 \cdot L_{grid} \cdot f_{sw}} = \frac{U_{DC} \cdot D - u_{grid}}{2 \cdot L_{grid} \cdot f_{sw}}, \tag{5.2}$$

where L_{grid} is the sum of the two inductors included in the grid-connected filter, f_{sw} is the switching frequency, and D is the duty cycle defining the on-durations of S_{AC3}, compared with the switching period, i.e. $D = T_{on,SAC3} / T_{sw}$. It becomes in this way possible to control the grid current.

5.1.2 DC-link Electrolytic Capacitor

The electrolytic DC-link capacitor is included for power decoupling between the PV-module and the grid.

The size of the decoupling capacitor can be determined when knowing that the power into the DC-link is constant, and that the power drawn from the DC-link follows a $\sin^2(\omega \cdot t)$ waveform:

$$C_{DC} = \frac{P_{DC}}{2 \cdot \omega \cdot \langle U_{DC} \rangle \cdot \tilde{u}_{DC}}, \tag{5.3}$$

where P_{DC} is the average DC-link power, ω is the grid frequency (314 rad/s for European systems), $<U_{DC}>$ is the average DC-link voltage and $\tilde{u}_{DC}$ is the amplitude of the ripple voltage.

The grid current cannot be controlled if the DC-link voltage is lower than the peak grid-voltage plus the voltage drop across the semiconductors and filter. The minimum usefulness DC-link voltage at 10% over-voltage in the grid is $230 \cdot 1.1 \cdot \sqrt{2} \approx 360$ V. The maximum DC-link voltage is specified to 400 V, so a good choice for $<U_{DC}>$ and $\tilde{u}_{DC}$ is ½(360+400) = 380 V and 400-380 = 20 V, respectively.

The size of the DC-link capacitor is computed by (5.3) to 31 µF at 150 W into the DC-link (assuming 10 W loss in the total circuit). A standard capacitor size is 33 µF at 400 V or 450 V. A 450 V capacitor is selected in order to allow for some over voltages, without damaging the capacitor.

5.1.3 MOSFETs

The selection of the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) is a trade off between cost, breakdown voltage, conduction losses and switching speed (and hence switching losses). The MOSFETs for the DC/AC inverter are selected among the CoolMOS type from Infineon, because they have very fine properties in terms of loss versus cost.

A survey of 5 different CoolMOS' is listed in Table 5.1. The best candidate (low cost and high break down voltage) is the SPA04N60C3 or the SPA07N60C3.

Table 5.1. Different CoolMOSs and price per device, from EBV.de.

Type	Break down voltage [V]	Maximum current, RMS [A]	On resistance at 25 °C [Ω]	Price [DKK]
SPA04N50C3	500	4.5	0.95	4.71 at 1 piece
SPA04N60C3	600	4.5	0.95	5.08 at 450 pieces
SPA07N60C3	600	7.3	0.60	7.63 at 45 pieces
SPA08N50C3	500	7.3	0.60	7.63 at 45 pieces
SPB07N60C3	600	7.3	0.60	7.05 at 1000 pieces

The total conduction losses in the MOSFETs, at full generation, amounts to 2× 0.95 Ω · (150 W / 230 V)^2 = 0.81 W, and 0.51 W for the two different MOSFETs. The switching losses are investigated in section 5.1.6, and found to 2.1 W per leg, for the SPA04N60C3 MOSFET. The total power loss in the MOSFETs is summed to 5.0 W, which is the same as 1.25 W per MOSFET. The thermal resistance for the SMD (Surface Mount Device) version of the SPA04N60C3 MOSFET is $R_{\theta,JA}$ = 35 K/W, when mounted on a PCB (Printed Circuit Board) with dimensions 40 mm × 40 mm and 6 cm^2 copper area for drain connection (from datasheet, INFINEON.com). The temperature difference between junction and ambient is computed to 1.25 W · 35 K/W = 44 K. Hence, the junction temperature will exceed the specifications, which is maximum 100 °C for an ambient temperature of 60 °C. This is however not seen as a major problem, since the junction can withstand 150 °C without being damaged (from datasheet).

5.1.4 Grid-Connected Filter

A filter is connected between the MOSFETs and the grid. The filter has three tasks: To convert the voltage generated by the MOSFETs to a current, to reduce the High Frequency (HF) switching noise, and to protect the MOSFETs from transients.

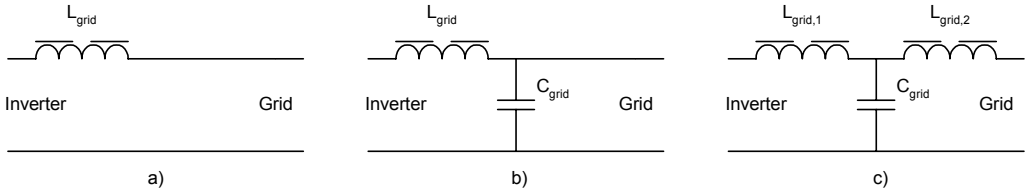

Figure 5.2. Three different types of grid-connected filters. a) L-filter, b) LC-filter, and c) LCL-filter.

The filter is selected to be of the LCL type due to its inherent advantages [84]. At least two other types of filters exist, the L- and the LC-filters. All three types are illustrated in Figure 5.2. The L filter has excellent performance in terms of voltage-to-current conversion, but the damping of the HF noise is rather poor. Also, the LC filter shows good performance in terms of current-to-voltage conversion and noise damping, if the grid-impedance (not depicted in Figure 5.1 nor in Figure 5.2) is high compared to $1/(2\cdot\pi\cdot f\cdot C_{grid})$. On the other hand, the filter capacitor may be exposed to line voltage harmonics, which result in large currents.

The LCL filter shares the same good properties with the L- and the LC-filters. Moreover, the damping of HF noise is better due to the extra inductance, and the capacitor is no more exposed to line voltage distortion. The transfer function for the LCL-filter is (from inverter-voltage to grid-current, assuming zero grid voltage and zero grid impedance):

$$\left.\frac{i_{grid}(s)}{u_{inv}(s)}\right|_{u_{grid}=0} = \frac{1}{Z_{grid,2} + Z_{grid,1} \cdot \left(1 + \frac{Z_{grid,2}}{Z_0}\right)}, \tag{5.4}$$

$$Z_{grid,1} = s \cdot L_{grid,1} + r_{Lgrid,1},$$

$$Z_{grid,2} = s \cdot L_{grid,2} + r_{Lgrid,2},$$

$$Z_0 = \frac{1}{s \cdot C_{grid}} + r_{Cgrid},$$

where $r_{Lgrid,1}$ and $r_{Lgrid,2}$ are the (winding) resistances included in the two inductors and r_{Cgrid} is the resistance included in the capacitor (the equivalent series resistance - ESR). The parallel resistance and series inductance, etc., in the capacitor and parallel capacitance, etc., in the inductors are not included, since they are believed to have minor influence in frequency span of interest. The frequency response of the L- and the LCL-filters are plotted in Figure 5.3, for the values designed later on in this section.

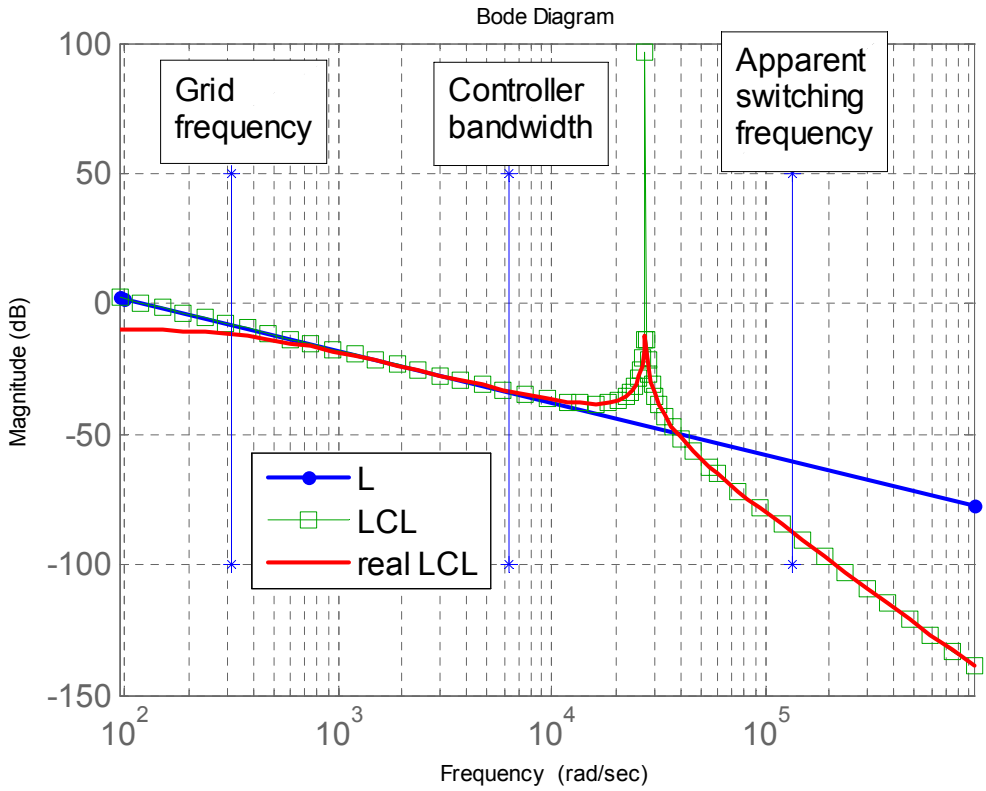

Figure 5.3. Magnitude of the three transfer functions: L-filter, ideal LCL-filter, and LCL-filter with the mentioned parasitic components, but without added damping. The grid frequency is equal to 50 Hz, the bandwidth of the controller is selected to 1 kHz, and the apparent switching frequency is equal to 21.4 kHz. The resonance frequency is computed to 4.63 kHz.

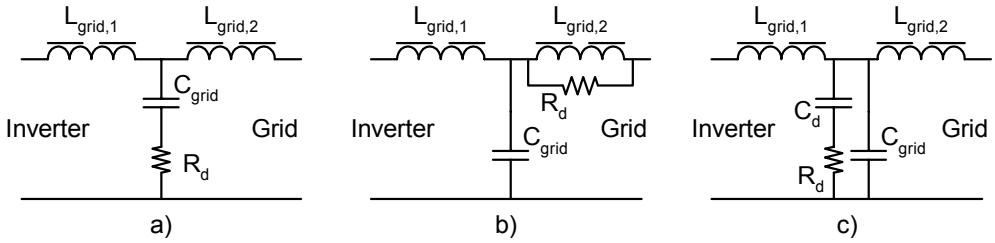

Figure 5.4. Passive damping of the LCL-filter. a) Resistor in series with the filter capacitor [84], b) Resistor in parallel with the grid-connected inductor [85], c) RC damping circuit in parallel with the filter capacitor [61].

The LCL filter is inherently unstable [84]. This is seen by the peak in the transfer-function around the resonant frequency, and some kind of damping must be added to make the filter more stable. This can be done in several ways, as illustrated in Figure 5.4, either by introducing a damping resistor in series with the filter capacitor as in Figure 5.4a) [84], or by adding a damping resistor in parallel with the grid-connected inductor as in Figure 5.4b) [85] and [86]. However, both solutions result in poor damping of the high-frequency switching harmonics, due to a reduced filter order (from –60 dB/dec. to –40 dB/dec.). A third solution is to include a damping circuit, made up around a resistor and a capacitor in series, in parallel with the filter capacitor as in Figure 5.4c) [61], but this is also a more expensive solution, since it requires an extra capacitor, which size must be larger than the filter capacitors ($C_d > C_{grid}$). A final solution would be to use some kind of active damping in the current controller, but this is not investigated here. The final design of the damping circuit is done in chapter 6, together with the design of the grid current controller, where the selected topology is the one presented in Figure 5.4-a).

The LCL filter resonant frequency must be lower than half the apparent switching frequency, i.e. $\omega_{res} \leq 2 \cdot \pi \times f_{sw}$ for uni-polar switching [84]. The resonant frequency is given as:

$$\omega_{res} = \sqrt{\frac{L_{grid,1} + L_{grid,2}}{C_{grid} \cdot L_{grid,1} \cdot L_{grid,2}}}, \qquad (5.5)$$

$$\omega_{res} = 2 \cdot \pi \cdot \sqrt{f_{CTRL} \cdot 2 \cdot f_{sw}}.$$

The resonant frequency is selected to be equal to the geometrical-mean of the grid-current controller bandwidth and the apparent switching frequency. When the sizes of the two inductors, selected in the next section, and the desired resonant frequency are known, the size of the filter capacitor can be determined as:

$$C_{grid} \geq \frac{L_{grid,1} + L_{grid,2}}{\omega_{res}^{\,2} \cdot L_{grid,1} \cdot L_{grid,2}}. \qquad (5.6)$$

However, the larger C_{grid} is the larger reactive current will be drawn from the grid during idle mode. This is not desirable since a reactive current includes power loss in the grid-connected inductor, due to the winding resistance.

An EFD high-grade ferrite core is used to realize $L_{grid,1}$ and a Kool Mμ ring core is used to realize $L_{grid,2}$.

The HF current ripple in $L_{grid,1}$ is high compared to $L_{grid,2}$ where almost non HF ripple is present. This is beneficial, since the high-grade ferrite core can withstand a high flux-density without saturating too much, whereas the Kool Mμ starts to saturate at low current, but the level of saturation is low, this is illustrated in Figure 5.5.

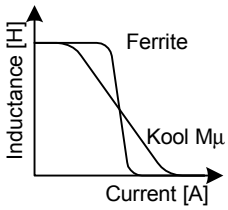

Figure 5.5. Inductance versus current for high-grade ferrite and Kool Mμ.

The behavior of the Kool Mμ material results in that the resonance frequency is not constant, and that the stability of the current controller may be affected, when the power level is changed. This is investigated later on in chapter 6.

The maximum obtainable value of $L \cdot I \cdot \hat{I}$ for five EFD and ETD cores made from high-grade ferrite are listed in Table 5.2, together with their prices, cf. from appendix E. The maximum obtainable value of $L \cdot \hat{I}^2$ for three ring-cores made from the Kool Mμ material is also listed in Table 5.2 [87], together with their prices (without fixing hardware) (Avnet components, 2002). The maximum RMS and peak values are obtained at 150 W and 85% of nominal grid voltage to 0.77 A and 1.1 A.

Table 5.2. Comparison of five ETD/ETD cores and three ring cores. The copper fill factor is made equals to 0.6, and the peak flux density to 300 mT.

Core type	Maximum value of $L \cdot I \cdot \hat{I}$	Obtainable inductance	Cost
EFD25 – 3C90	4.0 mH·A^2	3.7 mH	12.16 DKK
EFD30 – 3C90	5.7 mH·A^2	5.8 mH	18.35 DKK
ETD29 – 3C90	8.9 mH·A^2	9.6 mH	25.38 DKK
ETD34 – 3C90	13 mH·A^2	15 mH	34.51 DKK
ETD39 – 3C90	22 mH·A^2	25 mH	41.48 DKK
Kool Mμ ring core: 77314-A7	2 mH·A^2	1.7 mH	7.44 DKK
Kool Mμ ring core: 77935-A7	5 mH·A^2	4.2 mH	8.99 DKK
Kool Mμ ring core: 77071-A7	7 mH·A^2	5.9 mH	13.06 DKK

Selecting the switching frequency is a trade-off between switching losses in the MOSFETs, emitted HF noise, and grid current control (hence the microcontroller in which the control algorithms are to be implemented).

When the uni-polar PWM scheme is used to modulate the voltage across the filter inductance, the frequency content in the output voltage is distributed around $2 \times f_{sw} \times n \pm f_{grid} \times k$ [60], where n is the harmonic number and k are the sidebands. The EMC conducted noise standard EN55014 covers the frequency range from 150 kHz to 30 MHz. The most severe harmonics of the switching frequency should for that reason be located below 150 kHz, in order to lower the specifications for the EMI filter (included between the inverter in the grid). This can be reformulated into $f_{sw} < 150\ \text{kHz} / (2 \times n)$, when neglecting the side bands.

The components included in the LCL filter are then selected to minimize the cost, when the resonant frequency is fixed. Table 5.3 shows the 15 different possibilities to obtain a resonant frequency of 29.1 krad/s, when the switching frequency is 10.7 kHz. As seen, the cheapest solution for this particular frequency is to use an EFD25 core (3.7 mH) and a Kool Mμ 77935 core (4.2 mH) together with a film-capacitor of 680 nF. This amounts to a price of DKK 24.9 for the LCL-filter.

Table 5.3. Evaluation of the 3×5 different solutions to obtain a resonant frequency of 29.1 krad/s. The computed values are for the required filter capacitor in nF, and the values in brackets is the total cost for the LCL filter. The green highlighted cofiguration is the cheapest, and the red the most expensive.

Core types	EFD25	EFD30	ETD29	ETD34	ETD39
77314	1200 (27.3)	1000 (30.7)	820 (37.2)	820 (46.3)	820 (53.3)
77935	680 (24.9)	560 (30.9)	470 (37.7)	390 (46.6)	330 (53.4)
77071	560 (29.3)	470 (35.3)	330 (41.9)	330 (58.0)	270 (57.6)

Table 5.4. Evaluation of four different switching frequencies. The frequency response for the filter with n equal to 7 is shown in Figure 5.3. The prices for the film capacitors are given in appendix D. The controller bandwidth is selected to 1 kHz.

Harmonic number, n	4	5	6	7
Switching frequency [kHz]	18.7	15.0	12.5	10.7
LCL filter resonant frequency. Desired and obtained [krad/s]	38.4 35.5	34.4 32.4	31.4 29.3	29.1 27.3
$L_{grid,1}$ [mH]	3.7	3.7	3.7	3.7
$L_{grid,2}$ [mH]	1.7	1.7	1.7	4.2
C_{grid} [nF]	680	820	1000	680
Total cost for the LCL filter (without damping) [DKK]	23.4	24.0	24.5	24.9

It seems reasonable, based on the above discussion, to select n between 4 and 7. The cost of the LCL-filter, without damping, is evaluated in Table 5.4 for different values of n.

The switching frequency is selected to 10.7 kHz, in order not to overload the available microcontroller (Infineon C167CS-LM). The switching frequency can always be increased, when the exact execution time for the Interrupt Service Routine (ISR) is known (it is assumed that the current control algorithm is hosted in the ISR, which updates the duty cycle for each switching period).

The design of the inverter-connected inductor, $L_{grid,1}$, is given in appendix E. The length of the air-gap is computed to 1.08 mm, but should be adjusted to reach the designed value, due to fringing flux. The number of turns is computed to 234. The cross-sectional area and diameter for the wire is computed to 0.103 mm^2 and 0.36 mm. The wire resistance is calculated to 1.94 Ω at 25 °C, which results in 1.14 W winding losses.

The design of the grid-connected inductor, $L_{grid,2}$, is based on the CAD software in [87]. The CAD software computes the following solution: inductance at full load: 4.2 mH, inductance at no load: 7.9 mH, number of turns: 290, wire size: AWG#24 (bare area: 0.205 mm^2), copper fill factor: 0.48, DC resistance of winding: 1.14 Ω at 25 °C, and winding losses: 0.67 W. As seen, the inductance is falling as function of load current, also discussed above and in Figure 5.5.

5.1.5 Inrush Current Limitation

A current limiting resistor must be applied to limit inrush when the inverter is connected to the grid for the first time, and the DC-link capacitor is discharged. Once the voltage across the DC-link has reached approximate 95% of the peak value of the grid, the current limiting resistor is actively by-passed by a MOSFET or a relay, or passively by-passed with a diode.

The inrush circuit can be realized in several ways, cf. Figure 5.6. The selection of which type to select is based on power loss and cost. The three solutions are compared in Table 5.5.

Most relays (scheme 1) in the required power range have a power consumption of minimum 140 mW and the price is around 15 – 25 DKK, and requires some kind of drive circuit, e.g. an OPAMP.

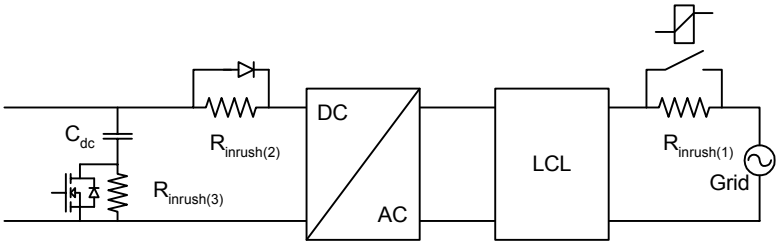

Figure 5.6. Three possible solutions for the inrush current limitation. (1) The inrush-limiting resistor is placed on the AC side and bypassed with a relay. (2) The resistor is placed in the DC-link and bypassed with a diode. (3) The resistor is placed in series with the DC-link capacitor and bypassed with a MOSFET.

The forward voltage drop of the diode (scheme 2) and the average current through it determines the power loss. A resistor must be placed in parallel with the diode, in order to allow the current from the full-bridge to flow back into C_{DC}, when unity power factor is not achieved. The conduction loss in the diode can be simplified to:

$$P_{diode} \approx U_0 \cdot \frac{P_{DC}}{U_{DC}}, \tag{5.7}$$

where P_{DC} is the average power handled by the diode, U_0 is the forward voltage drop and U_{DC} is the average DC-link voltage. Assuming 350 V in the DC-link, a forward voltage drop across the diode of 1.3 V and a DC-link power in the profile of the European efficiency calculations, yields an average loss of 322 mW. The reverse recovery losses are not considered, but could be just as high!

The on-resistance of the MOSFET (scheme 3) and the RMS current through it determines the power loss. The conduction loss in the MOSFET can be simplified to (partly from equations (4.7) and (4.8)):

$$P_{MOSFET} \approx \frac{R_{ds(on)}}{2} \cdot \left(\frac{P_{DC}}{U_{DC}} \right)^2 , \tag{5.8}$$

where $R_{ds(on)}$ is the on-resistance. Applying the same data' as above, yields an average loss of 37 mW. The MOSFET solution also requires a drive circuit, but it does not have to feed a continuous current, which was the case of the relay solution. Thus, it is believed to be cheaper.

Table 5.5. Comparison of three different inrush-limiting solutions.

Scheme	Average power loss	Price
Relay (1)	140 mW	22.75 DKK at 500+ (NEC EA2-5NU)
Diode (2)	322 mW	App. 2 DKK
MOSFET (3)	37 mW	4.71 DKK (same family as in the output stage)

The comparison in Table 5.5 reveals that scheme 3 is the best solution, when power loss is the issue. Besides, the diode scheme suffers from additional losses in the resistor when reverse current are generated from the full-bridge. Finally, the relay scheme is very expensive compared to the two others, but does not include any extra inductances in the path DC-link capacitor to inverter circuit (e.g. the inductances included in the leads of the diode or MOSFET). An additional inductance here can results in over-voltages across the four MOSFETs in the DC-AC inverter, according to L·di/dt.

The size of the resistor is determined by the amount of damping (ξ) required in the path: LCL filter, inrush resistor, and the DC-link capacitor. It can be shown that the required resistance is equal to:

$$R_{inrush} = 2 \cdot \xi \cdot \sqrt{\frac{L_{grid,1} + L_{grid,2}}{C_{DC}}} = 2 \cdot \xi \cdot Z_0 , \tag{5.9}$$

where Z_0 is the natural impedance of the LCL filter together with the DC-link capacitance, and ξ is the damping ratio, selected to unity. For the DC-link capacitor equal to 33 μF, and a total inductance of 3.7 mH + 4.2 mH (from Table 5.4), this gives a resistor of minimum 31 Ω.

5.1.6 Gate Drive and Gate Resistors

The MOSFETs in the DC-AC inverter must be interfaced to the control circuit. This includes power supplies and command signals for the MOSFETs. Four ways of realizing the gate drive for a high side MOSFET is depicted in Figure 5.7 [88].

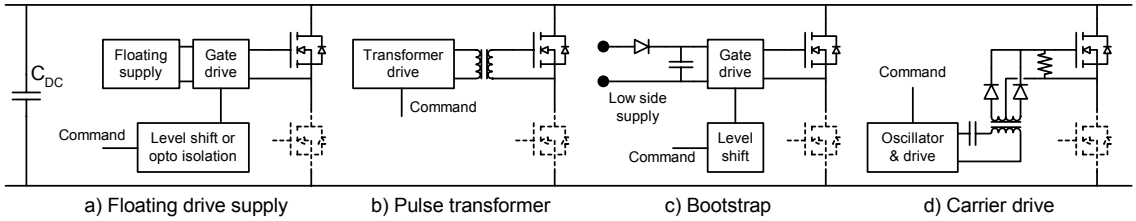

Figure 5.7. Basic circuits for four different ways of realizing the gate drive circuit for a high side MOSFET [88].

Table 5.6. Price comparison of a three possible gate-drive schemes.

Scheme	Cost at Farnell
1:1 or 1:1:1 Pulse-transformer, C & D Technologies	25.50 DKK at 250+
Boot-strap IC, International rectifier, IR 2109	15.40 DKK at 500+
Boot-strap IC, ST Microelectronics, L6384	10.29 DKK at 100+

The pulse-transformer in Figure 5.7b) and the carrier-drive in Figure 5.7d) schemes both require a transformer and belonging drive to transmit power and control signal to the MOSFETs. This makes an expensive solution, cf. Table 5.6. The switching performance of the gate signal is poor compared to the other two solutions but can be improved with added complexity. The gate control for the floating-drive-supply in Figure 5.7a) and the carrier-drive schemes are good (full control for infinite period of time), whereas it is not possible to keep the MOSFET on for more than a few milliseconds for the other two solutions. This is however not a problem, while the largest on duration for a MOSFET included in the DC-AC inverter equals $T_{sw} \times D_{max} \approx 93\ \mu s \cdot 0.93 = 87\ \mu s$.

The power supply for the bootstrap in Figure 5.7c) (and for the floating drive supply) can also be used to supply measuring circuits for grid voltage and current, if necessary. On the other hand, two floating power supplies are required for the scheme in Figure 5.7a), which makes it an expensive solution. The bootstrap drive is therefore selected, since it is cheap, flexible and offers full gate control for sufficient time.

The combined low- and high-side bootstrap drive IC must include a shutdown input, a control input and its current capabilities must be high enough to ensure fast switching. The L6384 bootstrap gate drive IC from ST Microelectronics is selected while it offers good price and current source/sink (+400 mA / -650 mA) capabilities. This IC includes a combined shutdown and blanking-time input (the blanking time is adjustable from 0.4 μs to 3.1 μs), and internal bootstrap diode circuit. The total gate-circuit, for one inverter leg, is depicted in Figure 5.8. The special arrangement of the gate resistors allows different turn-on and turn-off time constants, and in the same time, the upper section of the bootstrap circuit is protected against damaging under voltages [89]. However, the placement of the resistor $R_{g(off),1}$ affects the charging of the bootstrap capacitor, and should therefore be sufficient small.

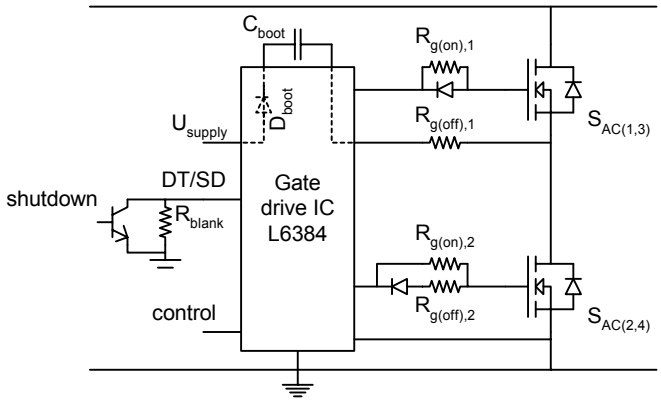

Figure 5.8. Gate driver circuit with bootstrap supply, blanking time programming and shutdown. Note the special arrangement of the gate-resistors, especially the circuit for the upper MOSFETs. This allows different turn-on and turn-off time constants for the MOSFETs, and protects the bootstrapped section from damaging under-voltages [89].

The L6384 includes an internal bootstrap circuit, where only an external capacitor is required for operation. The bootstrap capacitor is designed according to:

$$u_{supply(highside)} > U_{thresshold(off)}, \tag{5.10}$$

to make sure that the high-side circuit does not go into Under Voltage Lock Out (UVLO). The UVLO protection is disabled (i.e. the gate-driver turns on) at maximum 12.5 V, and enables again at maximum 10.5 V (i.e. the gate-driver turns off).

The voltage drop across the boost-strap diode circuit is:

$$u_{drop(diode)} = \frac{Q_{boot} \cdot \left(R_{ds(on)} + R_{g(off),1}\right)}{t_{charge}}, \tag{5.11}$$

where $R_{ds(on)}$ is the on-resistance in the diode circuit (from datasheet: 125 Ω), $R_{g(off),1}$ is the turn-off resistor for the upper MOSFET (designed later on to 23.7 Ω), t_{charge} is the charge duration for the bootstrap capacitor, which equals the low side turn on time ($t_{charge,min}$ = 1/(10.7 kHz)·0.07 = 6 µs). The bootstrap charge equals [89]:

$$Q_{boot} = Q_{gate} + Q_{ls} + \left(i_{leak(gs)} + i_{quies(boot)} + i_{leak(boot)}\right) \cdot t_{on}, \tag{5.12}$$

where Q_{gate} is the high side MOSFET gate charge, Q_{ls} is the level shifter charge, $i_{leak(gs)}$ is the leakage current through the gate-source path of the MOSFET, $i_{quies(boot)}$ is the bootstrap circuit quiescent current, and $i_{leak(boot)}$ is the bootstrap circuit leakage current. The time t_{on} is the high side on duration ($t_{on,max}$ = 1/(10.7 kHz)·0.93 = 87 µs). The size for the bootstrap capacitor then equals:

$$C_{boot} > \frac{Q_{boot}}{\Delta u_{boot}}, \tag{5.13}$$

where Δu_{boot} is the HF voltage ripple across the bootstrap capacitor, peak to peak.

The total charge is calculated by (5.12) to 25 nQ + 3 nQ + (100 nA + 200 µA +10 µA) · 87 µs = 46 nQ. The voltage drop across the diode equals 46 nQ · 150 Ω / 6 µs = 1.2 V according to (5.11). Hence, a supply voltage of no less than 13 V must be present at all times, in order to operate the bootstrap circuit. The size of the bootstrap capacitor is given by (5.13) to 46 nQ / 0.1 V = 460 nF.

The values of the resistors used in the gate circuit are selected to lower the switching and Reverse Recovery (RR) losses in the MOSFETs and freewheeling diodes (the body diodes included in the MOSFETs). The theory is described in appendix C. Figure 5.9 shows the instantaneous power loss in an inverter leg, over 10 ms. The values of the resistors are found to (at a supply voltage of 13 V): $R_{g(on)}$ = 32 Ω, and $R_{g(off)}$ = 20 Ω. This involves the following component values in Figure 5.8: $R_{g(on),1}$ = 20 Ω, $R_{g(off),1}$ = 12 Ω, $R_{g(on),2}$ = 32 Ω, and $R_{g(off),2}$ = 56 Ω. The total switching losses in a leg then amount to 2.1 W, which corresponds to approximate 1.0 W per MOSFET.

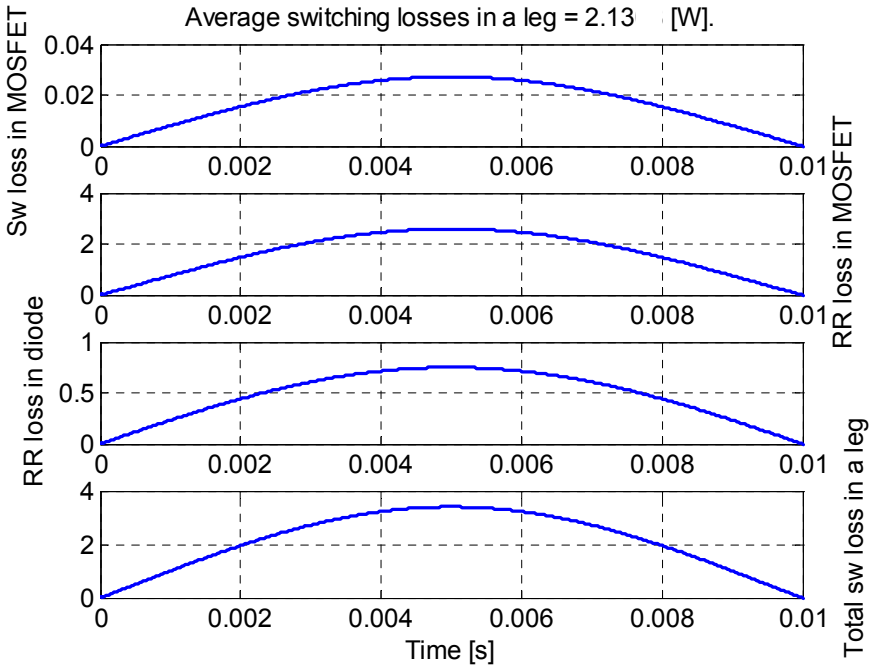

Figure 5.9. Instantaneous power losses in an inverter leg, during half a mains period at full generation.

A blanking time is inserted between turning one MOSFET off and turning the other on. This is done to avoid a 'shoot-through' situation where both MOSFETs are turned on. The blanking time must be larger than the turn-off sequence. The duration of the turn-off sequence is computed to approximately 40 ns. The blanking time is selected 10 times larger to make sure than the shoot-through situation is avoided. The blanking time is then computed to 0.4 µs, which corresponds to a programming-resistor, R_{blank} in Figure 5.8, of 47 kΩ.

5.1.7 Simulated Results

The inverter is simulated at the six operation points, in order to verify the design. The simulations are carried out in PSIM®, with closed-loop current control, and without blanking-time. No grid-impedance or grid voltage harmonics are present. The switching frequency is equal to 10.7 kHz.

The results are given in Table 5.7. The European efficiency is calculated to 93.8% for the DC-AC inverter, when the most dominant losses are included (conductions losses in the DC-link capacitor, MOSFETs, free wheeling diodes, LCL-filter, and switching losses in MOSFETs and diodes).

Table 5.7. Summary of simulated results for the DC/AC inverter.

Operating point	5%	10%	20%	30%	50%	100%
PV power [W]	8.0	17.3	36.0	54.4	89.0	158.7
DC-link power [W] (when including the computed efficiency for the DC-DC converter)	5.6	13.9	32.0	49.6	83.8	149.4
DC-link voltage: Average and peak to peak ripple [V]	360 4.9	360 7.8	360 11.6	360 15.9	360 25.4	360 42.4
Grid voltage, RMS [V]	230	230	230	230	230	230
$L_{grid,1}$ current, RMS [mA]	241	246	273	316	424	674
$L_{grid,2}$ current, RMS [mA]	40	63	137	211	354	634
C_{grid} current, RMS [mA]	250	250	249	250	250	249
Grid power, Mean [W]	3.3	11.4	30.1	47.2	80.3	144.7
DC-link capacitor current, RMS [mA]	179	182	195	218	276	416
Efficiency [%] (from DC-link to grid)	59%	82%	94%	95%	96%	97%
Burst mode, mean grid power [W]	5.1	12.9	30.5	-	-	-
Burst mode, RMS grid current [mA]	219	239	322	-	-	-
Burst mode efficiency [%] (5 bursts)	90%	93%	95%	-	-	-
Burst mode, discharging power [W]	50	56	74	-	-	-
Charging time [ms]	155	61	26		-	-
Discharging time [ms]	20	21	21	-	-	-

However, using burst mode operation at low irradiation, as described in [79] and section 4.4.1, increases the European efficiency from 93.8% to 95.5%. The purpose of burst mode operation is to transform constant losses into variable losses. E.g. the loss in the damping resistor is equal to $20\ \Omega \cdot (0.25\ \text{A})^2 = 1.3$ W when the inverter is running, no matter of what power is injected into the grid. The losses in the gate-circuit are also independent of the power level.

Burst mode operation is simulated as follows, also illustrated in Figure 4.19: The inverter is in idle mode when the DC-link voltage is below 400 V, and power is injected into the DC-link from the DC/DC converter (5.6 W in this case). The inverter wakes up when the voltage exceeds 400 V, and injects power into the grid until the DC-link voltage has decreased to 330 V. The power stored in the DC-link capacitor is given by (5.14) to 0.84 J, and the time it takes to charge it is computed by (5.15) to 150 ms. It is desirable to inject power into the grid in multiples of 20 ms, in order not to cause too many harmonics and DC injection. Assuming that the inverter is operated in 20 ms, the discharging power is computed by (5.16) to 48 W.

$$\Delta E_{CDC} = ½ \cdot C_{DC} \cdot \left({U_{DC,\max}}^2 - {U_{DC,\min}}^2 \right) = ½ \cdot 33\mu F \cdot \left((400V)^2 - (330V)^2 \right) = 0.84J, \quad (5.14)$$

$$T_{charge} = \frac{\Delta E_{CDC}}{P_{DC}} = \frac{0.84J}{5.6W} = 150ms, \quad (5.15)$$

$$P_{discharge} = \frac{\Delta E_{CDC} + P_{DC} \cdot T_{discharge}}{T_{discharge}} = \frac{0.84J + 5.6W \cdot 20ms}{20ms} = 48W. \quad (5.16)$$

Burst mode operation is used up to a power level, where the charge- and discharge- durations are equal (20 ms). This level is computed to 0.84 J / 20 ms = 42 W, where the discharging power is equal to 84 W. The burst-mode efficiency at this level is 95.5%, whereas the continuous operating efficiency is 94.2%. Burst mode operation is not described further in this thesis, but is a future possibility.

Finally, the HF spectrum of the grid current is also simulated. The results are shown in Figure 5.10. The simulation reveals a small elevation of the noise current around the resonant frequency for the LCL filter. The amplitude of the first switching harmonic at 21.4 kHz is equal to 7.5 mA and the amplitude of the seventh harmonic at 149.8 kHz is equal to 11 µA. The impedance of a 50 Ω || 50 µH Line Impedance Stabilizing Network (LISN) is also shown in Figure 5.10, and amount to 34 Ω ∠ 47° at 150 kHz. Thus, the peak voltage across the LISN at 150 kHz is computed to 377 µV, which is the same as 52 dBµV. The EN55022 quasi-peak limit at 150 kHz is equal to 66 dBµV, so the damped LCL filter is capable of damping the HF noise in acceptance with the standard. However, this simulation only focuses on Differential Mode (DM) noise caused by the switching, and not Common Mode (CM) noise generated by capacitive couplings between alternating potentials, etc., so the results in Figure 5.10 must be interpreted with care, but it seems that the designed filter is capable of damping the HF noise up to at least 1 MHz.

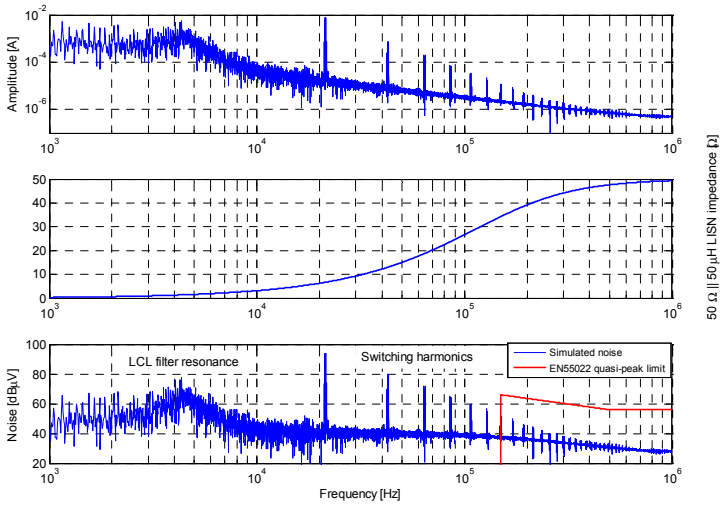

Figure 5.10. Simulated results for the grid-connected inverter at 145 W. The upper graph shows the simulated content of HF grid currents. An insignificant resonance is seen at approximately 4 kHz, which comes from the resonant frequency of the LCL-filter. The middle graph illustrates the impedance characteristic of a 50 Ω || 50 µH Line Impedance Stabilizing Network (LISN). The lower graph shown the corresponding voltage drop across the LISN, together with the quasi-peak limits defined in EN55022.

The DC-AC inverter is now designed. The initial design is verified with simulations in PSIM® and seems to operate as desired. The next issue is the DC-DC converter, which interfaces the PV-module to the DC-link. This is done in the next section.

5.2 PV-Connected DC-DC Converter

The inverter includes a DC-DC converter for amplifying the voltage and a DC-AC inverter for modulating the grid current. The DC-DC converter is depicted in Figure 5.1(left). The converter is made up around an input capacitor C_{PV}, four MOSFETs with freewheeling diodes $S_{PV1} - S_{PV4}$, a high frequency transformer with turns ratio 1:N, four diodes embedded in a full-wave rectifier $D_{RECT1} - D_{RECT4}$, the DC-link inductance and capacitance, L_{DC} and C_{DC}, respectively.

5.2.1 Mode of Operation

The principle is as follows, cf. Figure 5.11: Both converter branches are operated with a duty cycle slightly less than 50% in order to avoid a shoot-through in the legs [60]. Varying the overlap between the two branches then controls the output voltage. The dutycycle seen by the load (transformer), D_{load}, is computed as twice the phase-difference between the legs (maximum 180º) divided with 360º.

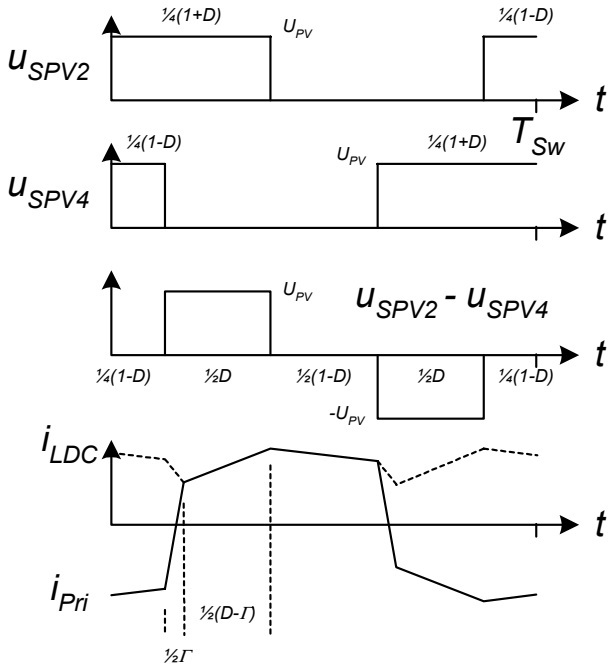

Figure 5.11. Typical operation for the full bridge DC/DC converter. From the top to bottom: voltage across transistor S_{PV2}; voltage across transistor SP_{V4}; voltage across the transformer primary side; current through DC-link inductor and primary transformer current (assumed unity turns ratio) [90], [91].

Another reason not to use a strictly 50% duty cycle is, that the transformer current is used to commutate the transistors during the blanking time. The output capacitors, see Figure C.2 in appendix C, included in the MOSFETs are charged/discharged automatically during the blanking time period, thus the converter is operated in Zero Voltage Switching (ZVS) mode, which gives low losses. However, measures must be taken in order to assure ZVS down to no-load.

The input to output voltage relationship should be rather simple for this DC/DC converter, due to its similarity with the buck converter. Thus, the relationship between input- and output-voltages should be: $U_{DC} / U_{PV} = D_{load} \times N$.

Unfortunately, the leakage inductance included in the transformer, L_{lk}, changes this correlation into a somewhat more complicated expression. The fraction of the switching period, Γ, where the current through the leakage inductance is changing from positive to negative (or vice versa), cf. Figure 5.11, is denoted the slew interval, and given by [90], [91]:

$$\begin{aligned}
\Gamma &= \frac{-b-\sqrt{b^2-4\cdot a\cdot c}}{2\cdot a}, \\
a &= \frac{U_{DC}'}{U_{PV}}\cdot\left(\frac{L_{lk}}{L_{DC}'}\right)^2+\frac{L_{lk}}{L_{DC}'} \\
b &= \frac{2\cdot U_{DC}'\cdot L_{lk}}{U_{PV}\cdot L_{DC}'}-\frac{L_{lk}}{L_{DC}'}-\frac{U_{PV}\cdot L_{DC}'}{U_{DC}'\cdot L_{lk}}-\frac{U_{PV}}{U_{DC}'}+1, \\
c &= \frac{U_{DC}'}{U_{PV}}-1+\frac{2\cdot\left(L_{lk}+L_{DC}'\right)}{T_{sw}\cdot R_{load}'},
\end{aligned} \tag{5.17}$$

where U_{DC}' is the normalized DC-link voltage (making a unity transformer turns ratio), L_{DC}' is the normalized filter inductance in the DC-link, R_{load}' is the normalized equivalent load, and T_{sw} is the switching period. The normalization is given by:

$$\begin{aligned}
U_{DC}' &= \frac{U_{DC}}{N}, \\
L_{DC}' &= \frac{L_{DC}}{N^2}, \\
R_{load}' &= \frac{U_{DC}'^2}{P_{DC}}.
\end{aligned} \tag{5.18}$$

Another definition of Γ is [90], [91]:

$$\Gamma = \frac{D\cdot U_{PV}-U_{DC}'}{U_{PV}+U_{DC}'\cdot\frac{L_{lk}}{L_{DC}'}}. \tag{5.19}$$

Combining (5.17) and (5.19) yields the maximum switching frequency and amount of inductance, at which the power P_{DC} can be transferred from the PV module to the DC-link:

$$\Gamma = \frac{D \cdot U_{PV} - U_{DC}'}{U_{PV} + U_{DC}' \cdot \frac{L_{lk}}{L_{DC}'}} = \frac{-b - \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} \Leftrightarrow \tag{5.20}$$

$$c = \frac{b^2 - (2 \cdot a \cdot \Gamma + b)^2}{4 \cdot a} \Leftrightarrow$$

$$f_{sw(\max)} = \left(c + 1 - \frac{U_{DC}'}{U_{PV}} \right) \cdot \frac{U_{DC}'^2}{2 \cdot (L_{lk} + L_{DC}') \cdot P_{DC}}.$$

The limit where the converter enters Discontinuous Conduction Mode (DCM) is given as [90], [91]:

$$R_{DCM} = \frac{2 \cdot (L_{lk} + L_{DC}') \cdot f_{sw}}{1 - \frac{U_{DC}'}{U_{PV}}} = \frac{U_{DC}'^2}{P_{DCM}}, \tag{5.21}$$

where P_{DCM} is the power level into the DC-link at which the converter enters DCM operation.

5.2.2 Main Circuit

The steady state voltage gain is computed as (assuming no leakage inductance in the transformer $\Rightarrow \Gamma=0$):

$$\frac{U_{DC}}{U_{PV}} = N \cdot D. \tag{5.22}$$

The initial transformer turns ratio is computed as (assuming unity duty cycle):

$$N \geq \frac{U_{DC,\max}}{U_{PV,\min}}, \tag{5.23}$$

which is evaluated to 400 V / 23 V = 17.4, and rounded up to 18. The initial duty cycle, D_{load}, is then defined in the span from 0.37 to 0.97.

The switching frequency is set to 110 kHz, with a turns-ratio of 18 and a DCM power level, P_{DCM}, of 5% of full power (8.2 W at 28.6 V). The total amount of inductance needed is then given by (5.21):

$$(L_{DC}' + L_{LK}) \cdot f_{sw} = \frac{(350V/18)^2}{2 \cdot 8.2W} \cdot \left(1 - \frac{350V/18}{28.6V} \right) = 7.4\Omega. \tag{5.24}$$

The leakage inductance is later on determined to maximum 80 nH, thus the required DC-link inductance becomes equal to: $L_{DC}' = 67\ \mu H \Rightarrow L_{DC} = 22$ mH.

Simulations in PSIM® shows, that the deigned circuit can generate around 368 V in the DC-link, when the voltage from the PV module is 23.0 V and the load in the DC-link is 160 W (assuming unity efficiency). Hence, the design is fulfilling the demands.

5.2.3 Transformer

The applied volt-second during the positive portion of the voltage (the maximum value for one switching period) is for Continuous Conduction Mode (CCM):

$$\lambda_1 = \int_{t_1}^{t_2} u_1 \, dt = \frac{U_{PV} \cdot D_{load} \cdot T_{SW}}{2} = \frac{U_{DC}}{2 \cdot N \cdot f_{sw}}, \tag{5.25}$$

and is evaluated to 400 V / (2×18×110 kHz) = $100 \cdot 10^{-6}$ V·s. As seen, the applied volt-second is independent of the PV operating point, assuming CCM.

The RMS value of the primary transformer current is equal to (assuming infinite magnetizing and DC-link inductances):

$$I_{\mathrm{Pr}i} = \underbrace{\frac{I_{PV}}{D_{load}}}_{\text{Peak value of pulse-train}} \cdot \overbrace{\sqrt{D_{load}}}^{\text{peak 2rms value for pulsetrain}} = I_{PV} \cdot \sqrt{\frac{1}{D_{load}}} = P_{PV} \cdot \sqrt{\frac{N}{U_{PV} \cdot U_{DC}}}, \tag{5.26}$$

where I_{PV} is the average PV current. The primary current is evaluated to 90 W × √ (18 / (31.0 V × 350 V)) = 3.7 A at 50% generation, and 6.8 A at full generation. This corresponds to a total current, I_{tot} in (5.27), of 7.4 A and 13.6 A, respectively.

Next, a proper core size and material is to be selected. The core geometrical constant for this application is computed as (from appendix E):

$$\begin{aligned} K_{g,Fe} &= \frac{\rho \cdot {\lambda_1}^2 \cdot {I_{tot}}^2 \cdot \left(K_{Fe} \cdot {f_{sw}}^{\alpha}\right)^{(2/\beta)}}{4 \cdot K_U \cdot {P_{tot}}^{((\beta+2)/\beta)}} \cdot 10^8 \\ &= \frac{\left(2.30 \cdot 10^{-6}\,\Omega \cdot cm\right) \cdot \left(100 \cdot 10^{-6}\,V \cdot s\right)^2 \cdot \left(13.6A\right)^2 \cdot \left(85 \cdot 10^{-9} \cdot \left(110kHz\right)^{1.70}\right)^{(2/2.55)}}{4 \cdot \left(0.4\right) \cdot {P_{tot}}^{((\beta+2)/\beta)}} \cdot 10^8 \\ &= \frac{3.99 \cdot 10^{-3}}{{P_{tot}}^{1.78}}, \end{aligned} \tag{5.27}$$

where P_{tot} is the total power loss in the transformer. The maximum difference between ambient and the core temperature is not allowed to exceed 40°C, cf. appendix E.

The EFD20 core made from 3F3 ferrite is evaluated to be too small, so the EFD25 core is now evaluated. The maximum allowable loss for the EFD25 core is 1.19 W, thus the required core geometrical constant for the EFD25 is 0.0029 cm^x, according to (5.27). The real core geometrical constant for the EFD25 is 0.0033 cm^x, so this core is for the moment being accepted as large enough.

The optimum peak flux density is computed as:

$$B_{opt} = \sqrt[(2+\beta)]{10^8 \cdot \left(\frac{\rho \cdot {\lambda_1}^2 \cdot {I_{tot}}^2}{2 \cdot K_U}\right) \cdot \left(\frac{MLT}{W_A \cdot {A_C}^2}\right) \cdot \left(\frac{1}{K_{Fe} \cdot \left(\frac{2 \cdot {U_1}^2}{\pi^2 \cdot {\lambda_1}^2}\right)^{(\alpha-1)} \cdot V_C \cdot {f_{sw}}^{(2-\alpha)} \cdot \beta}\right)} \tag{5.28}$$

The operating point to be optimized is at 50% generation, in order to optimize the European efficiency (the highest weight for the EU efficiency is at 50%).

(5.29)

$$B_{opt} = \sqrt[(2+2.55)]{10^8 \cdot \left(\frac{\left(2.30 \cdot 10^{-6}\,\Omega \cdot cm\right) \cdot \left(100 \cdot 10^{-6} V \cdot s\right)^2 \cdot \left(7.4A\right)^2}{2 \cdot \left(0.4\right)} \right) \cdot \left(\frac{4.64cm}{0.402cm^2 \cdot \left(0.580cm^2\right)^2} \right)}$$

$$\times \sqrt[(2+2.55)]{\left(\frac{1}{\left(85 \cdot 10^{-9}\right) \cdot \left(\frac{2 \cdot \left(24.6V\right)^2}{\pi^2 \cdot \left(100 \cdot 10^{-6} V \cdot s\right)^2} \right)^{(1.70-1)} \cdot \left(3.3cm^3\right) \cdot \left(110kHz\right)^{(2-1.70)} \cdot \left(2.55\right)} \right)}$$

$$B_{opt} = \sqrt[(4.55)]{10^8 \cdot \left(1.57 \cdot 10^{-12}\right) \cdot \left(34.3\right) \cdot \left(3.73 \cdot 10^{-3}\right)}$$

$$B_{opt} = 93mT.$$

A peak flux density of 0.09 T seems small, when known that ferrites can be operated up to approximate 0.3 T without saturating. However, the computed flux density assures minimum core- and winding-losses in the transformer, and is therefore adopted in the further design.

The number of turns on the primary side is computed as:

$$n_1 = \frac{\lambda_1}{2 \cdot B_{opt} \cdot A_C} = \frac{100 \cdot 10^{-6} V \cdot s}{2 \cdot \left(93mT\right) \cdot \left(0.58cm^2\right)} = 9.3\,, \tag{5.30}$$

and is rounded down to 9, which involves a peak flux density of 96 mT. The saturation flux density for the 3F3 material is higher than 300 mT, so the selected core is so far suitable.

Next is the core- and winding-loss evaluated at full power generation:

$$P_{Fe} = K_{Fe} \cdot \left(\frac{2 \cdot {U_1}^2}{\pi^2 \cdot {\lambda_1}^2} \right)^{\alpha-1} \cdot {B_{\max}}^{\beta} \cdot V_C \cdot {f_{sw}}^{(2-\alpha)} \tag{5.31}$$

$$P_{Fe} = 85 \cdot 10^{-6} \cdot \left(\frac{2 \cdot \left(23.4V\right)^2}{\pi^2 \cdot \left(100 \cdot 10^{-6} V \cdot s\right)^2} \right)^{1.70-1} \cdot \left(96mT\right)^{2.55} \cdot \left(3.3cm^3\right) \cdot \left(110kHz\right)^{(2-1.70)} \cdot \frac{1}{1000}$$

$$P_{Fe} = 0.25W,$$

and

$$P_{Cu} = \left(\frac{\left(2.30 \cdot 10^{-6}\,\Omega \cdot cm\right) \cdot \left(100 \cdot 10^{-6} V \cdot s\right)^2 \cdot \left(13.6A\right)^2}{4 \cdot (0.4)} \right) \cdot \left(\frac{4.64cm}{0.402cm^2 \cdot \left(0.580cm^2\right)^2} \right) \cdot \left(\frac{1}{96mT} \right)^2. \tag{5.32}$$

$$P_{Cu} = 0.99W.$$

The total losses inside the core are summed to 1.24 W, and the thermal resistance for the EFD25 core is 34 K/W. The temperature difference is computed to 42 °C, which is above the specification of 40 °C.

The transformer design is back to square one (if the maximum allowable temperature rise is equal to 40 °C) and a new core size is therefore selected. The core is selected to the EFD30, which can withstand a power loss of 1.55 W, and has a core geometrical constant of 0.0041 cm^x. Unfortunately, the EFD30 3F3 core was not available at the component vendor, for which reason the transformer core in up-graded to the ETD29.

Table 5.8. Evaluation of the three core sizes at full power generation.

Core size	Optimum and obtained peak flux density [mT]	Number of turns on the primary side.	Core loss [W]	Windings loss [W]	Temperature difference [°C]
EFD25	93 / 96	9	0.25	0.99	42
EFD30	77 / 81	9	0.23	0.86	28
ETD29	63 / 66	10	0.16	0.59	18

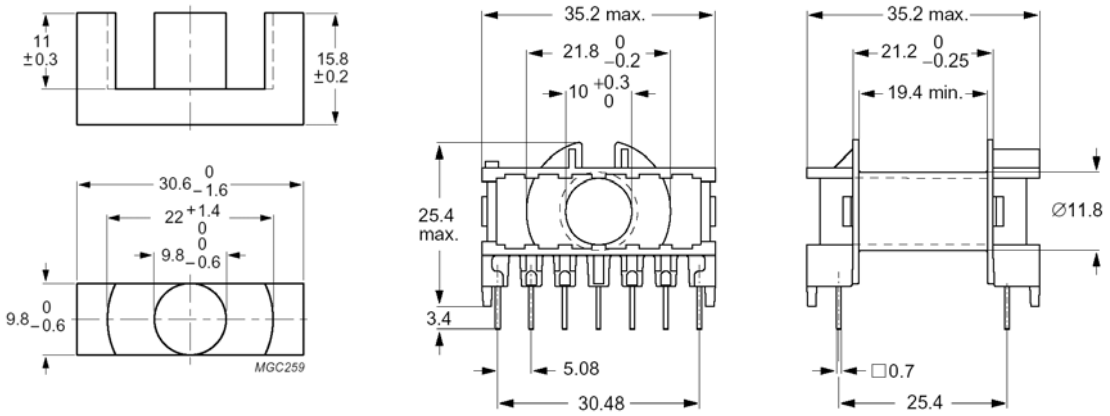

Figure 5.12. Physical dimensions for the ETD29 core.

A sketch of the ETD29 core is depicted in Figure 5.12. The results from the iterations are given in Table 5.8.

The number of turns on the primary side is computed to 10, and on the secondary side to 180. The area allocation for each side is fifty-fifty. The cross-sectional area and diameter for the secondary side wire is computed to 0.106 mm^2 and 0.367 mm. The maximum allowable wire diameter at 110 kHz and 100 °C is:

$$d_W \le 2\times\delta = 2\times\sqrt{\frac{\rho}{\pi\cdot\mu_0\cdot f}} = 2\times\sqrt{\frac{23.0\cdot10^{-9}\,\Omega\cdot m}{\pi\cdot\mu_0\cdot 110kHz}} = 2\times 0.230mm = 0.46mm. \tag{5.33}$$

Thus, the secondary windings do not need to be of the Litz-wire type, and the diameter is selected to 0.35 mm. The wire resistance is computed to 1.71 Ω at 25 °C and 2.28 Ω at 100 °C. The cross-sectional area and the diameter for the primary side wire are computed to 1.90 mm^2 and 1.56 mm. The diameter for the primary windings is also selected to 0.35 mm, which involves an area of 0.096 mm^2. Thus, 20 strands must be placed in parallel, in order to reach the designed area. The wire resistance is computed to 4.7 mΩ at 25 °C and 6.4 mΩ at 100 °C. The copper fill factor is evaluated to:

$$K_U = \frac{0.096mm^2 \cdot (1 \times 180 + 20 \times 10)}{95mm^2} = 0.385, \tag{5.34}$$

which is lower than the maximum of 0.4 as specified in appendix E.

Finally, the magnetizing inductance is computed to (2200 nH ± 25%)·10^2 = 165 µH ~ 275 µH, and the leakage inductance is computed to, appendix E:

$$L_{lk} \approx \frac{\mu_0 \cdot MLT \cdot b_W \cdot n_1^2}{3 \cdot P^2 \cdot h_W} = \frac{\mu_0 \cdot (5.3cm) \cdot (6mm) \cdot (10)^2}{3 \cdot P^2 \cdot (19mm)} = \frac{700nH}{P^2}, \tag{5.35}$$

where P is the number of interfaces between winding sections, see Figure 5.13 for definitions. The number of interfaces is selected to 3, as illustrated right most in Figure 5.13. This leakage inductance is then computed to 80 nH.

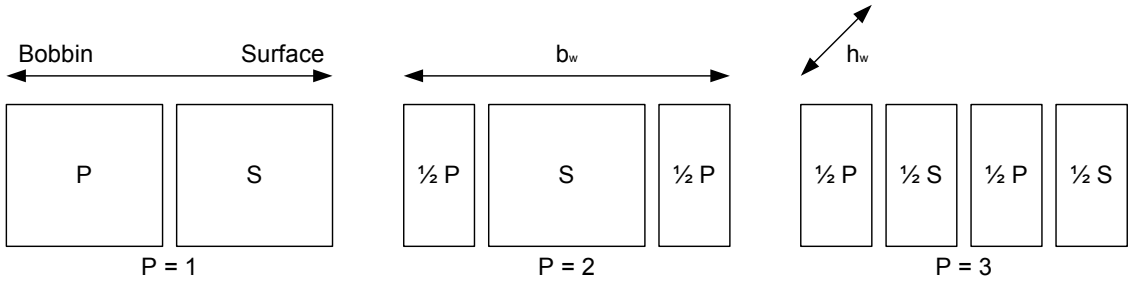

Figure 5.13. Definitions of P, b_w = 6 mm, and h_w = 19 mm.

5.2.4 DC-link Inductor

The size of the DC-link inductor was found to 10.6 mH[5] in section 5.2.2, and a suitable core is selected next. The maximum RMS value of the current through the inductor is 160 W / 300 V = 0.53 A, and the maximum peak current is 0.53 A (assuming no ripple and unity efficiency). The L·I·Î value is evaluated to 2.98·10^{-3} H·A^2, and the selected core must be able to withstand this. The EFD25 made from 3C90 material is good for 3.29·10^{-3} H·A^2 at 25 °C and 2.85·10^{-3} H·A^2 at 100 °C and is therefore selected.

The length of the air-gap is computed to: 0.74 mm, but should be adjusted to reach the designed value, due to fringing flux. The number of turns is computed to 335. The cross-sectional area and diameter for the wire is computed to 0.072 mm^2 and 0.30 mm. The wire resistance is calculated to 3.78 Ω at 25 °C and 5.06 at 100 °C.

Another solution is to use a Kool Mµ ring core. The core is calculated by the CAD software from Magnetics, Inc., [87] with the following inputs: DC-current: 0.43 A, ripple-current: 40 mA peak-to-peak, frequency: 220 kHz, full load inductance: 11 mH, current density: 500 A/cm^2. The resulting core is: part number 77310-7, permeability: 125, physical dimensions: 0.9" × 0.3" (outer diameter and height), cost without header: 7.14 DKK (from Avnet, 2002).

[5] The value of app. 11 mH is erroneous; the correct value is 22 mH (updated in the 2nd edition).

The CAD software computes the following parameters: inductance at full load: 11 mH, inductance at no load: 30 mH, number of turns: 590, wire size: AWG#28 (bare area: 0.080 mm^2), copper fill factor: 0.45, DC resistance of winding: 4.47 Ω at 25 °C, and total losses: 0.94 W.

5.2.5 DC-link Film Capacitor

A film capacitor is placed in the DC-link. The purpose of this capacitor is to create a low impedance path for the HF ripple current, since the power-decoupling electrolytic capacitor is good only up to some kHz. The peak to peak current ripple through the inductor, and hence the capacitor, is approximated to (note that the inductor sees twice the switching frequency because of the full-wave rectification, for which reason it is $2 \cdot f_{sw}$ in the denominator):

$$\Delta i_{LDC} = \frac{u_{LDC} \cdot \Delta T}{L_{DC}} \approx \frac{\left(U_{PV} \cdot N - U_{DC}\right) \cdot \left(D_{load} - \Gamma\right)}{L_{DC} \cdot \left(2 \cdot f_{sw}\right)}, \left(D_{load} - \Gamma\right) = \frac{U_{DC}}{U_{PV} \cdot N}, \tag{5.36}$$

which can be evaluated to 17 mA for 23 V at the input of the inverter. The voltage ripple, peak to peak is computed as the delta charge divided with the amount of capacitance (partly from [60]):

$$\Delta u_{CDC} = \frac{1}{C_{DC}} \cdot \frac{1}{2} \cdot \frac{\Delta i_{LDC}}{2} \cdot \frac{T_{sw}}{4} = \frac{\Delta i_{LDC}}{16 \cdot C_{DC} \cdot f_{sw}}. \tag{5.37}$$

The HF ripple is merely selected to 10 mV peak to peak. A film capacitor of 820 nF is therefore adopted.

5.2.6 Rectifier Diodes

The diodes in the rectifier has to withstand the reflected voltage from the PV-side, that is 18×45 V = 810 V (turn ratio multiplied with maximum operational PV voltage), which calls for 1000 V diodes (when applying a de-rate factor of 0.80). The average current through each rectifier-diode is equal to the average current in the DC-link inductor divided with the number of legs in the rectifier (2):

$$\left\langle i_D \right\rangle = \frac{\left\langle I_{LDC} \right\rangle}{2} = \frac{P_{DC}}{2 \cdot \left\langle U_{DC} \right\rangle}, \tag{5.38}$$

and can in the worst case be evaluated to ½(160 W / 300 V) = 0.27 A. The power loss in the rectifier can be broken down to conduction and reverse recovery losses (from appendix C):

$$\begin{aligned} P_{RECT} &= 4 \cdot P_{diode,cond} + 4 \cdot P_{diode,RR}, \\ P_{diode,cond} &\approx U_F \cdot \left\langle i_D \right\rangle, \\ P_{diode,RR} &\approx I_{RR} \cdot N \cdot U_{PV} \cdot \frac{t_{rr} \cdot s}{6 \cdot \left(s+1\right)} \cdot f_{sw}, \end{aligned} \tag{5.39}$$

where U_F is the forward voltage drop of the diode, I_{rr} and t_{rr} are the reverse recovery current and time, respectively, and s is the ‘snappiness’ factor.

Unfortunately, the junction-capacitance of the diodes and the transformer leakage inductor makes an un-damped second order system. Hence, a 100% overshoot in the voltage across the diodes is expected. This means that the diodes must be rated to 2 kV, or that the system must include some damping. This results in three solutions as illustrated in Figure 5.14:

1. One 2 kV device is used for each rectifier-diode,
2. One 1 kV device, with some damping is used for each rectifier-diode (the RC damping circuit can also be placed in parallel with the secondary winding),
3. Two 1 kV devices, connected in series and perhaps with some balancing circuit, are used for each rectifier-diode.

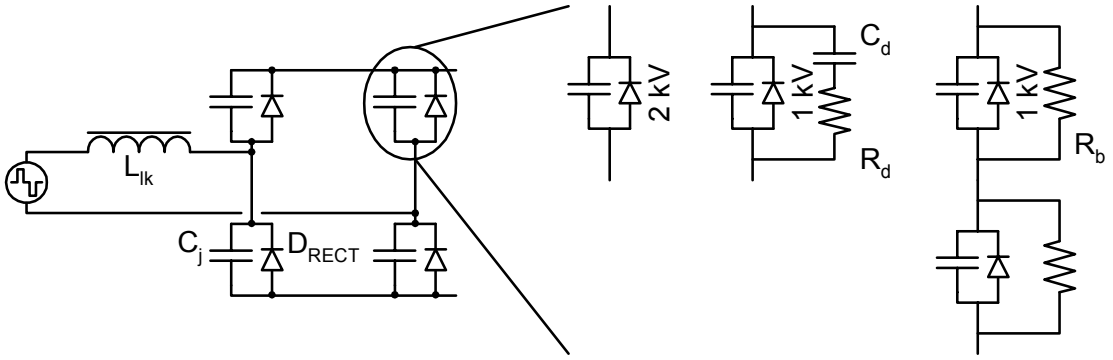

Figure 5.14. Rectifier circuit with parasitic components, and three possible arrangements of the diodes.

Table 5.9. Evaluation of the three different rectifier solutions. The power loss is estimated for 100% irradiation. Transformer leakage inductance, referring to the secondary side = 25.9 μH. Resonant frequency = $1/\sqrt{(2 \cdot L_{lk} \cdot C_j)}$.

Vishay		Solution 1	Solution 2	Solution 3
Diode	Number and Type	4 × RGP02-20E	4 × RGP02-16E	8 × RGP10M
	Ratings	2000 V and 0.5 A	1600 V and 0.5 A	1000 V and 1.0 A
	Forward voltage drop [V]	1.8	1.8	1.3
	Peak voltage (U_{PV} = 45V)	1500	1250 V	800
	Junction capacitance [pF]	5.0	5.0	15
Resistor		-	1 × 6.8 kΩ	8 × 6 MΩ
Capacitor		-	1 × 300 pF	-
Power loss per component [W]	Conduction	0.39	0.39	0.28
	RR	0.74	0.74	0.62
	Damping / balancing	-	5.90	0.00
	Total	4.5	10.4	7.2
Cost, diodes [EURO]		0.39	0.70	0.50

The three solutions are evaluated in Table 5.9. The damping in Figure 5.14-2) is achieved by connecting a damping-circuit in parallel with the secondary windings of the transformer. The size of the capacitor is selected to 20 times the junction capacitance of one diode. The size of the damping resistor is found by trial and error, to obtain a maximum over voltage of maximum 0.8 × 1600 V = 1280 V (de-rate factor multiplied with break down voltage). The size of the balancing resistors is found as $\frac{1}{2}U_{DC}$ divided with ten times the reverse current = 175 V / (3 μA × 10) = 6 MΩ. The cheapest, and most efficient, solution is the rectifier with 2 kV diodes.

The power loss per diode at full load is (conduction and reverse recovery from (5.39)): 0.39 W + 0.74 W > 1.1 W. The thermal resistances for the RGP02-20E diode are found in the datasheet to 30 K/W and 65 K/W, for junction-to-lead and junction-to-ambient, respectively (mounted on a PCB, with 9.5 mm lead length). The temperature difference between the junction and ambient is: 1.1 W · 65 K/W = 73 °C. This results in a junction temperature of 133 °C, at an ambient temperature of 60 °C. Hence, some kind of heat sink must be applied, with a total thermal resistance of no more than: (100 °C – 60 °C) / 1.1 W = 36 K/W, since the maximum junction temperature is specified to 100 °C.

A fourth solution, which is not investigated here, is to use an active clamp circuit in the DC-link [92]. The active clamp circuit is made up around a film capacitor, in series with a MOSFET, in parallel with the output of the rectifier. This can effectively clamp the voltage across the diodes to app. 850 V, and remove unwanted ringing. A fifth solution is to use avalanche rated diodes. Avalanche is the mode of operation where the voltage across the device exceeds the nominal breakdown value, and thus the device starts to conduct. This is normally equal to destruction of the device, but an avalanche rated device can withstand it.

5.2.7 MOSFETs

The MOSFETs must withstand the open-circuit PV module voltage, which is 45 V. Thus, the break down voltage should be, when accounting for the de-rating: 45 V / 0.75 = 60 V. The RMS value of the current, I_{SPV}, through each MOSFET is found from (5.26) to:

$$I_{SPV} = P_{PV} \cdot \sqrt{\frac{N}{2 \cdot U_{PV} \cdot U_{DC}}} = 160W \cdot \sqrt{\frac{18}{2 \cdot 28.1V \cdot 350V}} = 4.84A \,. \tag{5.40}$$

According to chapter 4, the current must be de-rated with a factor of:

$$DF_I = \frac{I_D\big|_{Actual,Tcase=90^\circ C}}{I_D\big|_{Datasheet,Tcase=25^\circ C}} = \sqrt{\frac{100°C - 90°C}{0.07\Omega \times 1.6} \cdot \frac{0.07\Omega \times 2.3}{175°C - 25°C}} = 0.31 \,. \tag{5.41}$$

The current de-rating is computed assuming that the case temperature is maximum 90 °C, and that the junction temperature is maximum 100 °C.

The selected MOSFET must be able to carry a RMS current of 4.84 A / 0.31 = 15.6 A. The chosen MOSFET is the ST Microelectronics STP 16NF06L, which is rated to a breakdown voltage of 60 V, an on-resistance of 70 mΩ, and a continuous current of 16 A (At case and junction temperatures of 25 °C and 175 °C, respectively). This particular MOSFET shows low internal capacitances and low gate charges, thus it is assumed being very fast.

The conduction loss in a MOSFET amounts to 0.07 Ω·(4.84 A)^2 = 1.64 W at full generation, and 6.6 W in total for all four MOSFETs. The temperature difference between junction and ambient is not allowed to exceed 40 °C, according to the specifications, and the temperature drop from junction to case is equal to 1.64 W · 3.33 K/W = 5.5 °C, the thermal resistance is given in the data sheet. The maximum allowable thermal resistance for the heat sink and mounting pads is computed to (40 °C – 5.5 °C) / 6.6 W = 5.3 K/W.

5.2.8 Input Capacitor

The purpose of the input capacitor is to decouple the HF current ripple, generated by the DC-DC converter, from the PV module.

Fourier analysis is used to compute the spectral content of a pulse train with duty cycle D and unity amplitude, as:

$$\imath(D,N) = \frac{2}{\pi \cdot N} \cdot \sin(D \cdot N \cdot \pi), \tag{5.42}$$

where N is the order of the harmonics. The peak value (amplitude) of the pulse train is given as its mean value divided with the duty cycle:

$$\hat{I} = \frac{\langle I_{PV} \rangle}{D}. \tag{5.43}$$

By combining (5.43) with (5.42), the real spectral content appears:

$$\hat{I}(D,N) = \hat{I} \cdot \imath(D,N) = 2 \cdot I_{PV} \cdot \left| \frac{\sin(D \cdot N \cdot \pi)}{D \cdot N \cdot \pi} \right|, \tag{5.44}$$

which has a theoretical maximum value 2·I_{PV}, for D·N·π = 0. The spectral content of a pulse train, given by (5.44) is depicted in Figure 5.15. The required impedance to damp the HF voltage ripple is given as:

$$Z(s) = \frac{U_{noise}(s)}{I_{noise}(s)} = \frac{U_{limit}(s)}{\hat{I}(s)}, \tag{5.45}$$

where U_{limit} is the limit given in the specifications, and Î is the peak current given in (5.44). The required filter-capacitance to suppress the switching-harmonics is:

$$C_{PV} = \frac{1}{2 \cdot \pi \cdot f \cdot Z} = \frac{1}{2 \cdot \pi \cdot 220\ kHz \cdot 50\ m\Omega} = 15\ \mu F. \tag{5.46}$$

The value computed in (5.46) is not the same as the power decoupling capacitor discussed in chapter 2. The required damping and capacitances for different harmonics is shown in Table 5.10.

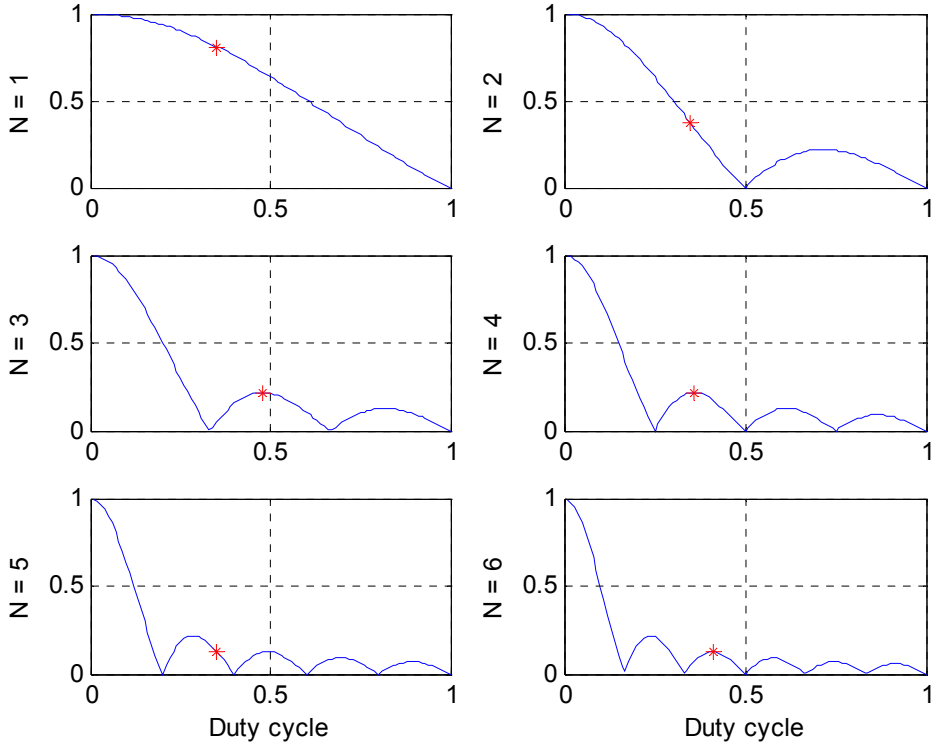

Figure 5.15. Spectral content of a unity pulse train. The stars indicate the worst-case amplitude, when the duty cycle is defined between 0.35 and 0.97.

A 15 µF film capacitor is a large capacitor. The design of the capacitor should therefore be subject to an optimization process, where the radiated HF noise from the inverter should be measured.

Table 5.10. Computation of required damping, for different harmonics.

Harmonic number, N	1	2	3	4	5	6
Frequency [kHz]	220	440	660	880	1100	1320
Limit, peak to peak	0.50 V					
D worst case, from Figure 5.15	0.35	0.35	0.48	0.36	0.35	0.41
Î(D,n), unity amplitude [ ]	0.81	0.37	0.22		0.13	
Î, I_{MPP} = 6.2 A [A]	10.0	4.6	2.7		1.6	
Required Damping | Z(s) | [mΩ]	50	230	185		310	
Capacitance to obtain the required damping [µF]	15	1.5	1.3	1.0	0.5	0.4

5.2.9 Controller

The control circuit is based on the UCC3895 IC from UNITRODE / TEXAS INSTRUMENTS. Quotation from the datasheet:

"*The UCC3895 is a phase shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant frequency switching pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part can be used either as a voltage mode or a current mode controller.*"

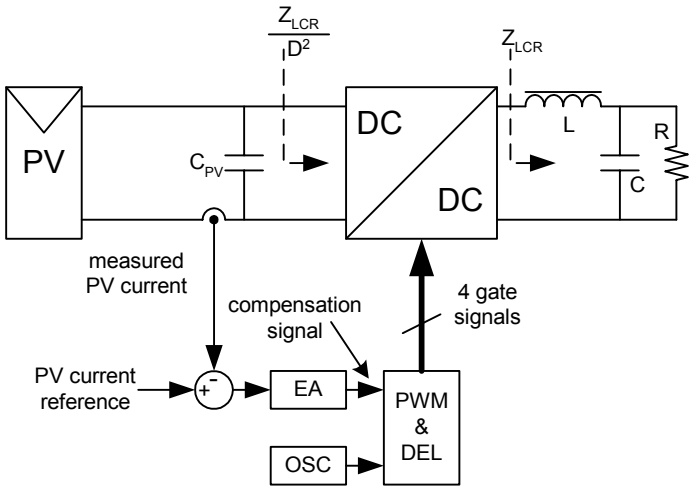

Figure 5.16. Block diagram of the DC-DC converter with the proposed controllers.

The input voltage from the PV module is given in the range from 23 V to 45 V, and the output voltage across the DC-link is defined from 300 V to 400 V. Besides this, the DC-AC inverter controls the magnitude of the output voltage, so the task for the controller is to regulate the input current of the PV-module.

A block diagram of the PV module, with DC-DC converter, measuring circuit and controller is illustrated in Figure 5.16. It consists of an Error Amplifier (EA), a PWM block together with the oscillator (OSC) and blanking time circuit (DEL). The proposed control structure is depicted in Figure 5.18.

The aim of the PI controller is to regulate the PV-module current, even that the DC-link and the PV-module voltages are non-constant in order to operate the module at the desired working point. A small signal model is needed of the DC-DC converter in order to design a feasible controller.

The influence of the slew-rate, discussed in section 5.2.2, is omitted to keep the following derivation simple. This is convenient since the real transfer function for the DC-DC converter is rather complicated, due to the presence of the leakage inductance in the transformer [90], [91]. The impedance of the DC-link is given as (by inspection of Figure 5.16, L = DC-link inductor, C = DC-link capacitor, R = equivalent load resistance, and assuming no other components):

$$Z_{LCR} = \frac{s^2 \cdot LCR + s \cdot L + R}{s \cdot CR + 1} \tag{5.47}$$

.

The relationship between input and output voltages and current is then:

$$Z_{LCR} = \frac{u_{out}}{i_{out}} = \frac{u_{in} \cdot D}{i_{in} \cdot \frac{1}{D}} = \frac{u_{in}}{i_{in}} \cdot D^2 \Leftrightarrow \qquad (5.48)$$
$$\frac{u_{in}}{i_{in}} = \frac{Z_{LCR}}{D^2}.$$

When the input capacitor, C_{PV}, is included the following transfer function appears (the parallel connection of a capacitor and the impedance in (5.48)):

$$\frac{u_{in}}{i_{in}} = \frac{Z_{LCR}}{D^2} \left\| \frac{1}{s \cdot C_{PV}} \right. \qquad (5.49)$$

Rearranging and expanding (5.49) into its large- and small-signal components yields:

$$\left(U_{in} + \tilde{u}_{in}\right) \cdot \left(s \cdot C_{PV} + \frac{\left(D + \tilde{d}\right)^2}{Z_{LCR}(s)} \right) = I_{in} + \tilde{i}_{in}, \qquad (5.50)$$

where uppercase letters denoted steady-state DC values and lowercase letters with a tilde denotes small-signal values. The brackets are removed and terms containing two or more small-signal quantities are neglected:

$$Z_{LCR}^{-1} \cdot \left(D^2 \cdot U_{in} + 2 \cdot D \cdot \tilde{d} \cdot U_{in} + D^2 \cdot \tilde{u}_{in}\right) + s \cdot C_{PV} \cdot \left(U_{in} + \tilde{u}_{in}\right) = I_{in} + \tilde{i}_{in}. \qquad (5.51)$$

Thus, the large- and small-signal models are:

$$I_{in} = \left(\frac{D^2}{Z_{LCR}} + s \cdot C_{PV} \right) \cdot U_{in} = \frac{D^2 \cdot U_{in}}{R} \; for \; s = 0, \qquad (5.52)$$
$$\tilde{i}_{in} = \frac{2 \cdot D \cdot \tilde{d} \cdot U_{in} + D^2 \cdot \tilde{u}_{in}}{Z_{LCR}} + s \cdot C_{PV} \cdot \tilde{u}_{in}.$$

The transfer function searched for is $H(s) = \tilde{i}_{in}(s) / \tilde{d}(s)$, which describes the perturbations in the input current as a function of the perturbations in the duty cycle. Assuming that the input voltage does not have any small-signal content, i.e. $\tilde{u}_{in} = 0$, the transfer function can be derived from (5.52):

$$\tilde{i}_{in} = \frac{2 \cdot D \cdot \tilde{d} \cdot U_{in}}{Z_{LCR}} \Leftrightarrow \qquad (5.53)$$
$$H(s) = \frac{\tilde{i}_{in}(s)}{\tilde{d}(s)} = \frac{2 \cdot D \cdot U_{in}}{Z_{LCR}(s)} = 2 \cdot U_{out} \cdot \frac{1}{Z_{LCR}(s)}.$$

The UCC3895 controller includes an Error Amplifier (EA) that can be programmed into many types of controllers, e.g. lead, lag, lead-lag, P, PI, PD, PID, etc, by a few external components. It is decided to use a classical PI controller, as it is known to remove any steady state errors. A part of the internal structure of the UCC3895 is sketched in Figure 5.17, together with the external components needed for the PI controller (without anti-windup circuit).

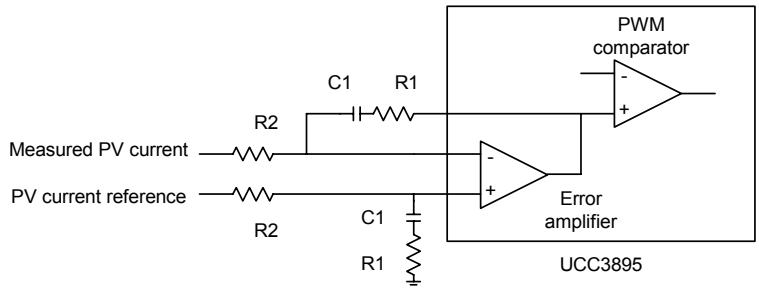

Figure 5.17. PWM comparator and Error Amplifier block diagram for the UCC3895.

The transfer function for the EA circuit is given by:

$$EA(s) = \frac{\frac{1}{s \cdot C1} + R1}{R2} = \frac{\frac{s \cdot C1 \cdot R1 + 1}{s \cdot C1}}{R2} = \frac{s \cdot C1 \cdot R1 + 1}{s \cdot C1 \cdot R2} = K_P \cdot \frac{T_I \cdot s + 1}{T_I \cdot s} \Leftrightarrow \tag{5.54}$$

$$K_P = \frac{R1}{R2}, \quad T_I = R1 \cdot C1.$$

The transfer function for the PWM comparator is determined by the oscillator frequency and min/max input/output signals [60] and [93]:

$$PWM(s) = G_M \cdot \frac{\frac{2}{T_{OSC}}}{s + \frac{2}{T_{OSC}}}, \tag{5.55}$$

$$G_M = \frac{\max(duty) - \min(duty)}{\max(comp) - \min(comp)}, \tag{5.56}$$

where T_{OSC} is the period for the oscillator (assuming $T_{OSC} = T_{sw}$), and G_M is the gain included in the circuit. The low pass filter is included to model the inherent delay, of half a switching period, in the comparator. This part can however be excluded, since the developed transfer function only is valid up one-tenth of the switching frequency. The maximum and minimum obtainable values are 0.99 and 0.00 for the duty cycle, and 2.35 V and 0.20 V for the oscillator signal. The gain is thereby computed to 0.46.

The control structure is depicted in Figure 5.18, and the open-loop transfer function is computed as:

$$OL(s) = EA(s) \cdot PWM(s) \cdot H(s), \tag{5.57}$$

$$OL(s) = K_P \cdot \frac{T_I \cdot s + 1}{T_I \cdot s} \cdot G_M \cdot \frac{\frac{2}{T_{OSC}}}{s + \frac{2}{T_{OSC}}} \cdot \frac{2 \cdot U_{out} \cdot (s \cdot CR + 1)}{s^2 \cdot LCR + s \cdot L + R},$$

$$OL(s) = K_P \cdot G_M \cdot 2 \cdot U_{out} \cdot \frac{T_I \cdot s + 1}{T_I \cdot s} \cdot \frac{\alpha}{s + \alpha} \cdot \frac{s \cdot CR + 1}{s^2 \cdot LCR + s \cdot L + R}, \alpha = \frac{2}{T_{OSC}}.$$

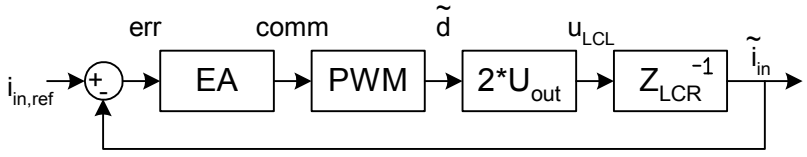

Figure 5.18. Small signal representation for the DC-DC converter with feedback.

The characteristic equation for the closed loop transfer function is:

$$charac(s) = T_I \cdot s \cdot (s+\alpha) \cdot \left(s^2 \cdot LCR + s \cdot L + R\right) + K_P \cdot G_M \cdot 2 \cdot U_{out} \cdot (T_I \cdot s + 1) \cdot \alpha \cdot (s \cdot CR + 1). \quad (5.58)$$

The PI controller is tuned in MATLAB® and tested in PSIM®. A set of parameters that works fine is: $T_I = 220 \cdot 10^{-6}$, and $K_P = 0.15$ (C1 = 100 nF, R1 = 2.2 kΩ and R2 = 14.7 kΩ), cf. Figure 5.19 to Figure 5.21.

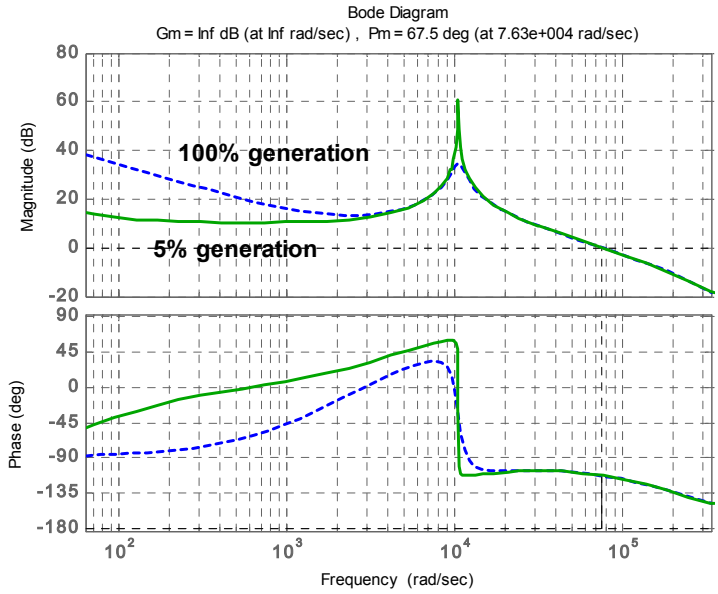

Figure 5.19. Open-loop Bode plot for the current controller, at 5% and 100% generation, from 10 Hz to ½f_{sw} = 55 kHz. The peak in the transfer function occurs at the resonant-frequency for the output filter: 1/√(L_{DC}·C_{DC}) = 1/√(11 mH· 820 nF) = 10.5 krad/s (is lowered to 1.6 krad/s when the electrolytic capacitor is included).

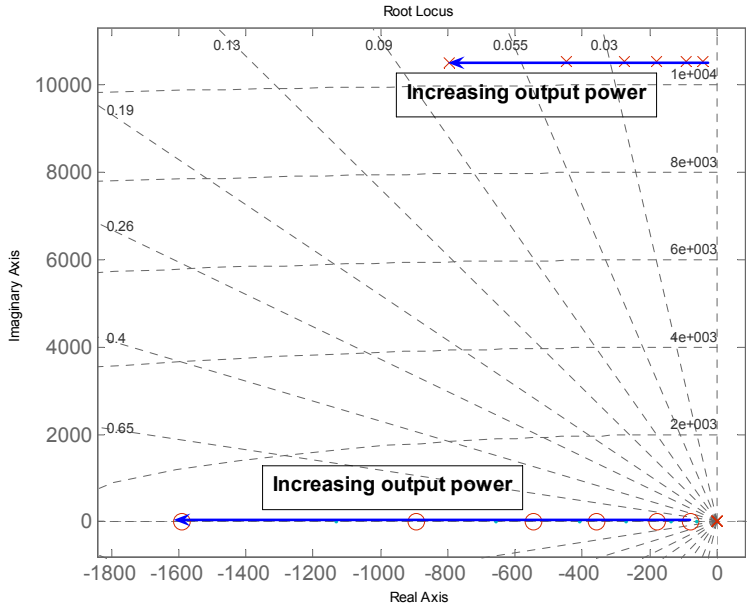

Figure 5.20. Closed loop root locus for the current controller at 8, 18, 36, 55, 90, and 160 W.

The open-loop bode plot in Figure 5.19 reveals that the gain margin is infinite and that the phase margin is equal to 67°, which yields a stable system. This is also seen in the root-locus in Figure 5.20, where all poles and zeros are located in left half plane. The calculated results in MATLAB® and the simulated results in PSIM® agree very well, as seen in Figure 5.21. Besides this, the PV current contains some high frequency currents, due to the switching of the inverter. This is, of course not, included in the linearized and averaged transfer function in (5.57).

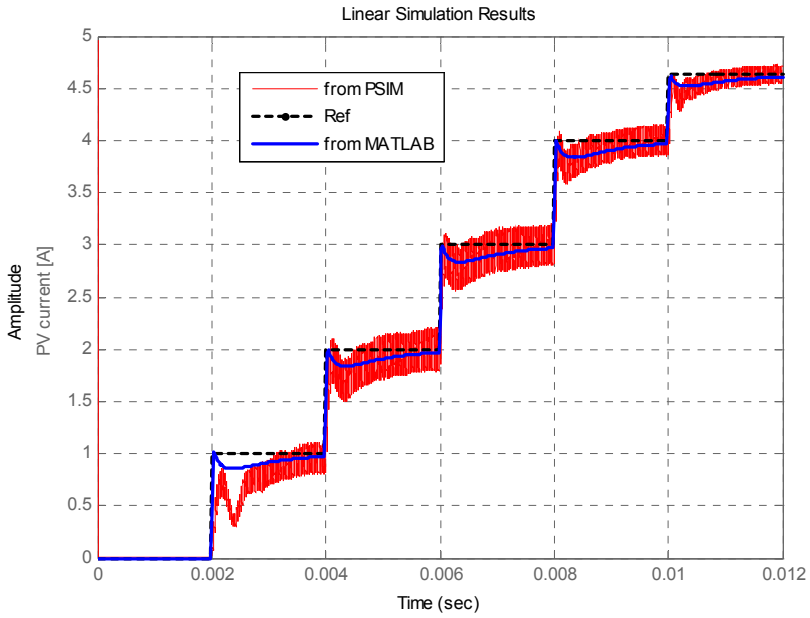

Figure 5.21: Calculated and Simulated results. The calculated time-domain response is equal to the simulated response, except to the absence of the HF ripple.

Another important issue is the 'audio susceptibility', which is the same as immunity to voltage variations in the DC-link. This is important, since a large voltage ripple is present in the DC-link, during part and full generation, cf. section 5.1.2. The maximum amplitude of the ripple is computed to 21 V at 100 Hz. The transfer function in (5.51) is expanded, and terms containing $u_{in} \cdot D$ are substituted with u_{out}:

$$Z_{LCR}^{-1} \cdot \left(D \cdot U_{out} + 2 \cdot \tilde{d} \cdot U_{out} + D \cdot \tilde{u}_{out}\right) + s \cdot C_{PV} \cdot \left(U_{in} + \tilde{u}_{in}\right) = I_{in} + \tilde{i}_{in} . \tag{5.59}$$

The small-signal transfer function, neglecting the input capacitor due to its small value, equals:

$$\tilde{i}_{in} = \frac{2 \cdot \tilde{d} \cdot U_{out} + D \cdot \tilde{u}_{out}}{Z_{LCR}} . \tag{5.60}$$

The small signal representation in Figure 5.18 can be redrawn, as in Figure 5.22.

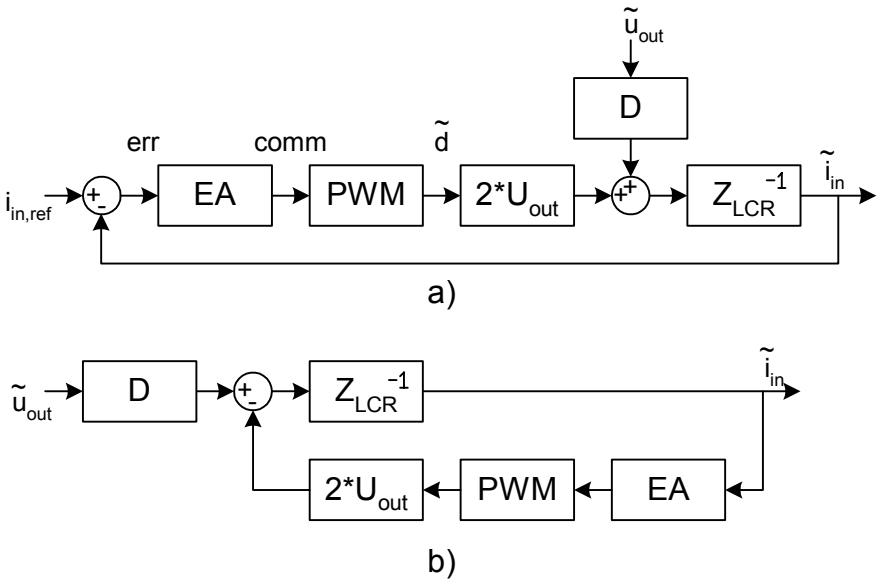

Figure 5.22. Small signal representation for the DC/DC converter with feedback. a) with perturbation of DC-link voltage, b) redrawn into standard layout with $i_{in,ref} = 0$.

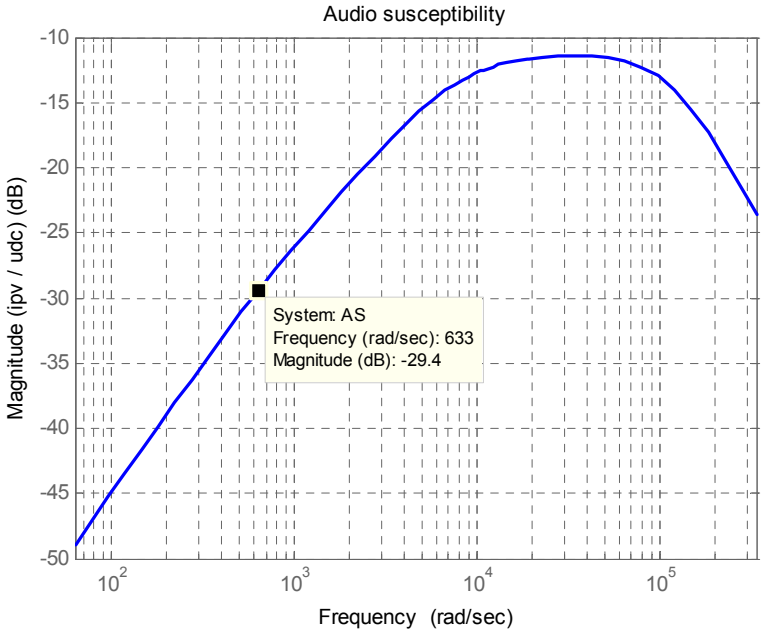

Figure 5.23. Bode plot of the audio susceptibility: $\tilde{\imath}_{in}(s) / \tilde{u}_{out}(s)$.

The closed loop transfer function of $\tilde{\imath}_{in}(s) / \tilde{u}_{out}(s)$ is found by inspection (excluding the input capacitor):

$$\frac{\tilde{i}_{in}(s)}{\tilde{u}_{out}(s)} = D \cdot \frac{1}{Z_{LCR}(s) + 2 \cdot U_{out} \cdot PWM(s) \cdot EA(s)}. \tag{5.61}$$

The magnitude of (5.61) is depicted in Figure 5.23. The plot shows that the amplitude of the small-signal current is equal to -30 dB at 100 Hz. This corresponds to an amplitude of 0.04 A when a ripple voltage with an amplitude of 21 V, is present in the DC-link. The impedance of the PV module is found in chapter 2 as U_{MPP}/I_{MPP} (only valid around the Maximum Power Point). Thus, the 100 Hz voltage ripple seen by the PV module is approximate equal to: 0.04 A * (28.1 V / 5.70 A) = 0.2 V at full generation, and neglecting the small input capacitor of 820 nF since is do not have any influence on a 100 Hz signal (X_C @ 100 Hz = 1940 Ω). This is much lower than the specification of 4.1 V.

5.2.10 Gate-Driver

The selected gate driver IC is the L6385 from ST Microelectronics, which includes two control inputs, one for each of the MOSFETs in a converter leg. The L6385 also includes an internal bootstrap circuit, like the L6384 used for the DC-AC inverter. The design of the gate-drive circuit is also similar to that of the L6384, used in the DC-AC inverter.

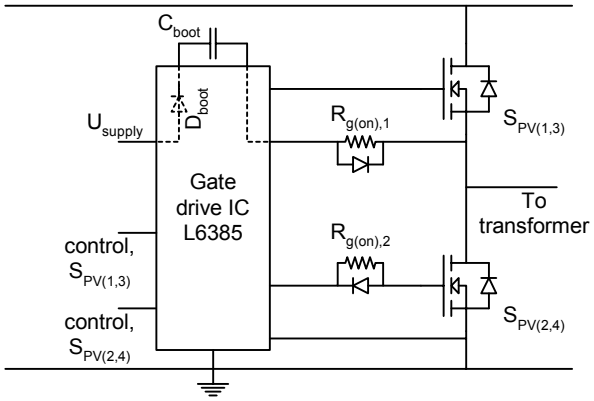

Figure 5.24. Gate driver circuit with bootstrap supply, and two control inputs.

The bootstrap capacitor is designed according to (5.10), to make sure that the high-side driver does not go into UVLO (Under Voltage Lock Out). The UVLO protection is disabled at maximum 10.5 V, and enables again at maximum 9.2 V. The voltage drop across the boost-strap diode circuit is computed by (5.11), where $R_{g(off),1}$ is omitted and the charge time is equal to the low side turn on time (4.5 µs). The bootstrap charge is computed by (5.12). The time t_{on} is the high side on duration (4.5 µs). The size of the bootstrap capacitor is then computed by (5.13).

The total charge transferred through the bootstrap circuit is mostly determined by the total gate charge of the MOSFET, which equals 12 nC. The total charge is calculated by (5.12) to 16 nQ. The voltage drop across the diode equals 16 nC · 125 Ω / 4.5 µs = 0.44 V according to (5.11). Hence, a supply voltage of no less than 10.5 V must be present at all times, in order to operate the bootstrap circuit. The size of the bootstrap capacitor is given by (5.13) to 16 nQ / 0.1 V ≈ 160 nF.

The turn-on gate resistors is merely selected to 11 V / 400 mA = 27.4 Ω, and the turn-off resistors are not used. This results in a 'slow' turn-on process and a 'fast' turn-off sequence. The resistors are further adjusted in the laboratory, to reach lowest power loss.

5.2.11 Simulated Results

The converter is simulated at the six operation points, in order to verify the design. The DC-AC inverter is substituted with an equivalent load resistance. The simulations are carried out in PSIM®, with open-loop current regulation and large-signal [60]. This means that the controllers are omitted, and that the duty cycle is changed manually, to reach the specified operating point. A clamp circuit, 50 pF in series with 8 kΩ, is placed in parallel with the secondary transformer winding, to lower the ringing from the transformer leakage inductance and diode junction capacitance.

The results are given in Table 5.11. The European efficiency is calculated to 91.6% for the DC/DC converter, when the most dominant losses are included (conductions losses in MOSFETs, transformer, rectifier diodes, DC-link inductor, switching losses in MOSFETs and diodes, and iron losses in the transformer).

Table 5.11. Summary of simulated results for the DC/DC converter.

Operating point	5%	10%	20%	30%	50%	100%
PV voltage: Average and peak to peak ripple [V]	27.6 0.07	30.0 0.08	31.3 0.15	31.7 0.22	30.9 0.35	28.5 0.52
PV current: Average and peak to peak ripple [A]	0.29 0.01	0.58 0.02	1.15 0.03	1.72 0.04	2.88 0.08	5.57 0.19
PV power [W]	8.0	17.3	36.0	54.4	89.0	158.7
Duty cycle, D [-]	0.567	0.694	0.683	0.683	0.706	0.750
DC-link voltage: Average and peak to peak ripple [V]	350 0.05	350 0.05	350 0.04	350 0.06	350 0.05	350 0.03
DC-link current Average and peak to peak ripple [mA]	16 45	40 52	91 54	142 55	239 53	427 43
DC-link power [W]	5.6	13.9	32.0	49.6	83.8	149.4
Equivalent load resistance [Ω]	21750	8800	3830	2470	1462	820
Primary transformer current: RMS and peak [A]	0.5 0.5	0.9 1.3	1.6 2.2	2.3 3.1	3.7 5.2	6.7 8.1
Rectifier peak voltage [V]	760	890	918	946	964	864
Mode of operation	DCM	CCM	CCM	CCM	CCM	CCM
Efficiency [%]	70%	80%	89%	91%	94%	94%

The simulations shows that the designed circuit fulfills the demands given in the introduction to this chapter, and is therefore accepted.

5.3 Evaluation of the Total Inverter

The evaluation of the inverter includes an estimation of the cost and the efficiency.

5.3.1 Components and Cost

Table 5.12. Cost estimation for the DC-AC inverter and the DC-DC converter.

Component	Ratings	Type	Price [DKK] at quantity	Vendor
Grid-connected DC-AC Inverter				
DC-link electrolytic capacitor	33 μF & 450 V ESR = 1.60 Ω	Evox-Rifa PEG 124YJ2330Q	32.75 at 100+	RS
DC-AC inverter MOSFETs	4.5 A & 600 V $R_{ds(on)}$ = 0.95 Ω	Infineon SPA04N60C3	5.08 at 450	EBV
Inverter connected inductor	3.7 mH & 1.94 Ω	Ferroxcube EFD25 – 3C90	12.16 at 500+	Farnell
Grid connected inductor	4.2 mH & 1.14 Ω	Magnetics, Inc. Kool Mμ core: 77935	8.99 at 1000+	BFI
Filter capacitor	680 nF & 275 Vac ESR = 0.23 Ω	Epcos B81130B1684M	3.77 at 1000+	Farnell
Damping resistor	22 Ω & 2 W R_{th} = 75 K/W	BC components 2306 198 53229	1.14 at 10 000+	Farnell
Inrush MOSFET	4.5 A & 500 V $R_{ds(on)}$ = 0.95 Ω	Infineon SPA04N50C3	4.71 at 1	EBV
Inrush resistor	39 Ω & 2 W R_{th} = 75 K/W	BC components 2306 198 53399	1.14 at 10 000+	Farnell
DC-AC inverter gate driver	+400 mA -600 mA	ST Microelectronics L6384	10.29 at 100+	Farnell
Boot strap capacitor	1 μF & 63 V	Epcos B32520C474K	1.45 at 500+	Farnell
Total DC-AC inverter	-	-	108 (app. 14 €)	-
Module-connected DC-DC Converter				
Transformer	-	Ferroxcube ETD29 – 3F3	25.38 at 500+	Farnell
DC-link inductor	11 mH & 4.47 Ω	Magnetics, Inc. Kool Mμ core: 77310	7.14 at 1000+	BFI
DC-link film capacitor	1000 nF & 275 Vac	Epcos B81130C1105M	4.92 at 1000+	Farnell
Rectifier diodes	2000 V & 0.5 A	Vishay RGP02-20E	0.72 at 5500+	EBV
DC-DC converter MOSFET	16 A & 60 V $R_{ds(on)}$ = 0.07 Ω	ST Microelectronics STP 16NF06L	4.35 at 1000+	Farnell
Input film capacitor	15 μF & 100 V	Epcos B32524Q1156K	14.20 at 1000+	Farnell
Controller	-	Unitrode / Texas Instr. UCC3895	40.85 at 100+	EBV
DC-DC converter gate driver	+400 mA -600 mA	ST Microelectronics L6385	10.29 at 100+	Farnell
Boot strap capacitor	470 nF & 63 V	Epcos B32520C474K	1.45 at 500+	Farnell
Total DC-DC converter	-	-	136 (app. 18 €)	-

The costs of the designed components amount to 244 DKK excl. VAT (app. 32 €). This is however believed to decrease when an eventual mass-production is started, due to the benefits of large-scale production. Besides, the prices used for estimating the cost of the power-circuit is based on different quantities, which is not fair when computing the cost.

5.3.2 Efficiency

The total efficiency is estimated on basis of the results in Table 5.7 and Table 5.11. The power consumed by the internal power supply are excluded in the calculations, but are assumed to be maximum 10 W for the entire inverter. The results are given in Table 5.13.

The European efficiency is evaluated to 86.3%, compared to 91.6% computed in chapter 4. The difference is mainly due to additional losses in the LCL filter and in the inrush-MOSFET, which was not included in the calculations in chapter 4.

Table 5.13. Efficiencies for the DC-AC inverter at six different operating points.

Operating point	5%	10%	20%	30%	50%	100%
Weight	0.03	0.06	0.13	0.10	0.48	0.20
PV power [W]	8.0	17.3	36.0	54.4	89.0	158.7
DC-link power [W]	5.6	13.9	32.0	49.6	83.8	149.4
Grid power [W]	3.3	11.4	30.1	47.2	80.3	144.7
Power loss in DC-DC converter [W]	2.4	3.4	4.0	4.8	5.2	9.3
Power loss in DC-AC inverter [W]	2.3	2.5	1.9	2.4	3.5	4.7
Total power loss [W]	4.7	5.9	5.9	7.2	8.7	14.0
Efficiency [%]	41.3%	65.9%	83.6%	86.8%	90.2%	91.2%

5.3.3 Summary

The inverter topology selected in chapter 4 was designed is this chapter. This covers the design of the grid-connected DC/AC inverter and the module-connected DC/DC converter, both rated to 160 W. The power-stages have been designed with focus on low power-loss and low cost. The cost for the designed components is estimated to approximately 250 DKK, excl. VAT, and the European efficiency to approximate 86%.

The power electronic circuits for the inverter are now designed, and the controllers for the inverter are designed in the next chapter.

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Chapter 6

Design of Controllers in PV-Inverter

The inverter hardware and the current controller for the DC-DC converter were designed in chapter 5. The other controllers are designed in this chapter, this includes: Maximum Power Point Tracker (MPPT) for the PV module, Phase Locked Loop (PLL) to track the fundamental component of the grid voltage, DC-link voltage controller, and grid current controller. They are illustrated in Figure 6.1

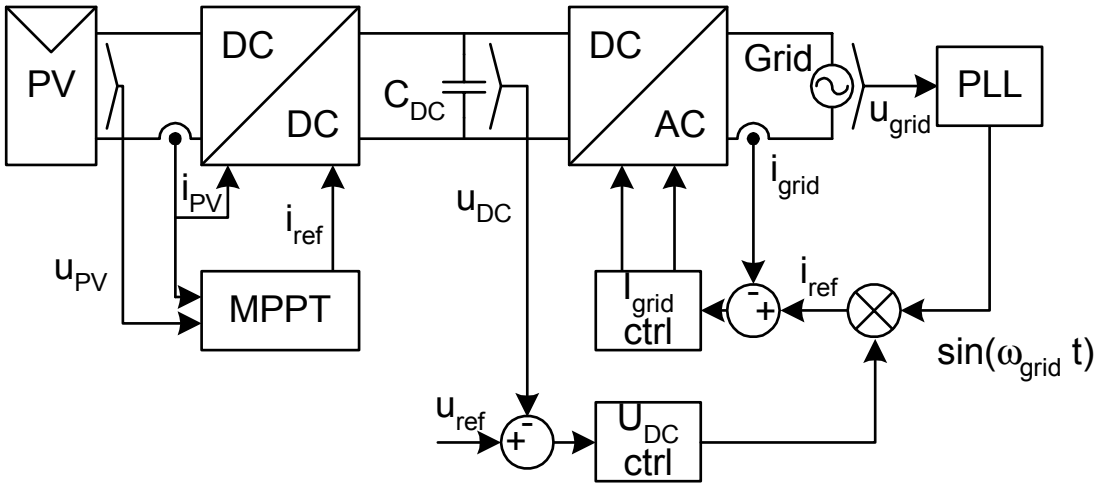

Figure 6.1. Block diagram of the inverter with different control structures.

The controllers are hosted in an Interrupt Service Routine (ISR) running at 10.7 kHz, which also is the switching frequency. The ISR is running on an Infineon C167 CS-LM microcontroller, with a 25 MHz clock-frequency, Pulse Width Modulator (PWM), and 16 multiplexed 10-bit ADC channels.

6.1 Maximum Power Point Tracker (MPPT)

The operating point where the PV module generates the most power is denoted the Maximum Power Point (MPP) which co-ordinates are: U_{MPP}, $I_{MPP.}$ The available power from the PV module is a function of solar irradiation, module temperature, and amount of partial shadow, as seen in Figures 2.4, 2.5, and 2.8 in chapter 2. Thus, the MPP is never constant but varies all the time. Sometimes it changes rapidly due to fast changes in the weather conditions[6], other times it is fairly constant when no clouds are present. Four major types of tracking algorithms (MPPT) are available, they are (in order of complexity, simplest first):

- Constant fill-factor (voltage or current)
- Sweeping
- Perturb and observe (hill-climbing)
- Incremental conductance

Other types of algorithms also exist, e.g. fuzzy-logic, neural-networks, monitor/reference cells, etc. They are however not reviewed here, due to their elevated complexities, or the need for additional PV cells for monitoring purpose.

6.1.1 Constant Fill-Factor

The constant fill-factor algorithms assume that the MPP voltage is given as a constant fraction of the open circuit module voltage, U_{OC}, or that the MPP current is given as a constant fraction of the short circuit module current, I_{SC} [94], [95]. These fraction are denoted the fill-factors, i.e. (and typical values):

$$FF_U = \frac{U_{MPP}}{U_{OC}} = 0.8, \tag{6.1}$$

$$FF_I = \frac{I_{MPP}}{I_{SC}} = 0.9, \tag{6.2}$$

and is assumed constant for all PV-modules, cell temperatures and solar irradiations.

Mode of operation: It is assumed that the PV module is operated at a given point. The MPPT algorithm turns off the converter for a short duration, e.g. 10 ms, and reads the open circuit voltage or the short circuit current. The reference for the module-voltage or -current for the next operating period, e.g. 1 second, is then given by the (6.1) or (6.2), with an assumed fill-factor ■

The algorithm is easy to implement in the ISR. On the other hand, it includes two serious limitations. First, it assumes that the fill-factor is constant for all PV modules in the world, regardless of temperature and irradiation. This is, of course, not true. Second, rapid clouds may be present, thus the MPP may change faster than the 'normal operating period', 1 second in the foregoing example. This also leads to a lower generation than possible.

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[6] The irradiance can change as much as 500 W /(m^2·s), or from zero to bright sunlight in 2 seconds. Measured during springtime 2005 with a pyranometer (included in the 2nd edition).

The fill factor for a given PV module and temperature can however be determined by scanning its voltage/current characteristics. This is done in [94] where the entire voltage/current characteristic is obtained by scanning the module in 25 ms, with a pause of several minutes in between. The actual fill factor, FF_I, is computed by (6.2) and stored for later use. The dynamic of the fill factor is very low so the pause of several minutes is not a problem. The obtained fill factor is then used to compute the current reference based on the short circuit current, which is recorded every 80 ms. This approach can also be used with the voltage fill factor, FF_U, but the relationship between the open circuit voltage and the MPP voltage is not as unique as for the current fill factor [96].

The largest disadvantage with this scheme is that the module must be short-circuited now and then (80 ms in [96]) in order to compute the actual fill factor and the current reference.

6.1.2 Sweeping

The basic sweeping algorithm is operating in a similar way as the constant fill-factor algorithm. As the name indicates, the algorithm performs a sweep in the modules power characteristic.

Mode of operation: It is assumed that the PV module is operated at a given point. The algorithm commands the converter to make a sweep in the modules characteristic. Simultaneously, the voltages and currents are recorded and the available power is calculated for each point. The point where the power is largest, the MPP, is stored and used as a new reference for the following period of normal operation, e.g. 1 second ■

This algorithm is a little harder to implement in the ISR, due to the calculations of the power. Besides this, it must also include a comparator function in order to locate the MPP. The basic sweeping algorithm suffers from the same limitation as the constant fill-factor algorithm: Rapid clouds may be present, thus the MPP may change faster than the ‘normal operating period’.

Besides, if the sweep-duration is too long, the irradiance may have changed and the recorded curve corresponds to two different irradiations. This can be mitigated by starting the sweep at zero voltage, i.e. measuring the actual short circuit current. The sweep is then continued to open circuit conditions while all the different operating points are investigated for available power. Finally, the module is short circuited again and the new short-circuit current are measured. Following, the irradiance has changed if the measured short-circuit currents does not agree with each other, and nothing can really be stated about the location of the MPP.

6.1.3 Perturb and Observer

The perturb-and-observe algorithm is also known as the ‘climbing hill’ approach. The reference is constantly changed, and the resulting power is compared with the previous power, and a decision about the direction of MPP can thus be stated [97].

Mode of operation: It is assumed that the PV module is operated at a given point. The voltage reference of the PV module is initialized to $U_{PV}^*[n]$. After the reference has been reached, the generated power $P_{PV}[n]$, is calculated and stored. The reference is then changed to $U_{PV}^*[n+1]$, and the generated power, $P_{PV}[n+1]$, is computed and stored. If $P_{PV}[n] > P_{PV}[n+1]$, the MPP is located in the opposite direction of which the reference was changed. Thus, the new reference should be equal to: $U_{PV}^*[n+2] = U_{PV}^*[n+1] - \Delta U$. In the opposite case where $P_{PV}[n] < P_{PV}[n+1]$, the MPP is located in the same direction as the change in the reference, and the new reference should be in the same direction: $U_{PV}^*[n+2] = U_{PV}^*[n+1] + \Delta U$ ■

This way of searching in the MPP is fast when the irradiance is constant. On the other hand, it includes some limitations. First, the generated power is fluctuating around the MPP, while the PV voltage is alternating around the MPP. Making ΔU sufficient small can mitigate this. However, this is on the cost of increasing the searching time when large variation in the irradiance is present. It is preferred to make ΔU large to catch the MPP during rapid changes, since the power loss due to the oscillations around the MPP is small. A large ΔU also enhances the signal-to-noise ratio in the sensed current.

Second, rapidly changing in the irradiation can lead to a wrong decision about the direction of the MPP [28]. This can however be solved by introducing a third reference, $U_{PV}^*[n+3]$, [98], [99]. Another solution is to ensure that the change in power as function of the change in the voltage-reference always is larger than the change in power due to change in radiation [116].

6.1.4 Incremental Conductance

The incremental conductance (IndCond) algorithm is based on the fact that the negative value of the instantaneous conductance ($-s_{PV} = -i_{PV}/u_{PV}$) and the incremental conductance ($ds_{PV} = di_{PV}/du_{PV}$), is equal at the MPP [28]. This is verified in (6.3):

$$\begin{aligned}
&\frac{\partial p_{PV}}{\partial u_{PV}} = 0 \Leftrightarrow \\
&\frac{\partial \left(u_{PV} \cdot i_{PV}\right)}{\partial u_{PV}} = 0 \Leftrightarrow \\
&\frac{d u_{PV}}{d u_{PV}} \cdot i_{PV} + \frac{d i_{PV}}{d u_{PV}} \cdot u_{PV} = 0 \Leftrightarrow \\
&i_{PV} + \frac{d i_{PV}}{d u_{PV}} \cdot u_{PV} = 0 \Leftrightarrow \\
&\frac{d i_{PV}}{d u_{PV}} = -\frac{i_{PV}}{u_{PV}} \Leftrightarrow \\
&\frac{\Delta i_{PV}}{\Delta u_{PV}} = -\frac{i_{PV}}{u_{PV}}.
\end{aligned} \tag{6.3}$$

Mode of operation: It is assumed that the PV module is operated at a given point. The current and voltage are sampled and the differences are calculated as: $\Delta i = i[n] - i[n-1]$ and $\Delta u = u[n] - u[n-1]$, where [n] denotes the newly sampled values and [n-1] denotes the previous samples. If Δu is equal to zero, the sign on Δi is used to determine in which direction the MPP is located. If Δu is non-zero, the sign of $\Delta i/\Delta u + I/U$ is used to determine the direction. The new current reference is then based on the previous reference plus the information about the direction. This is illustrated in Figure 6.2 ■

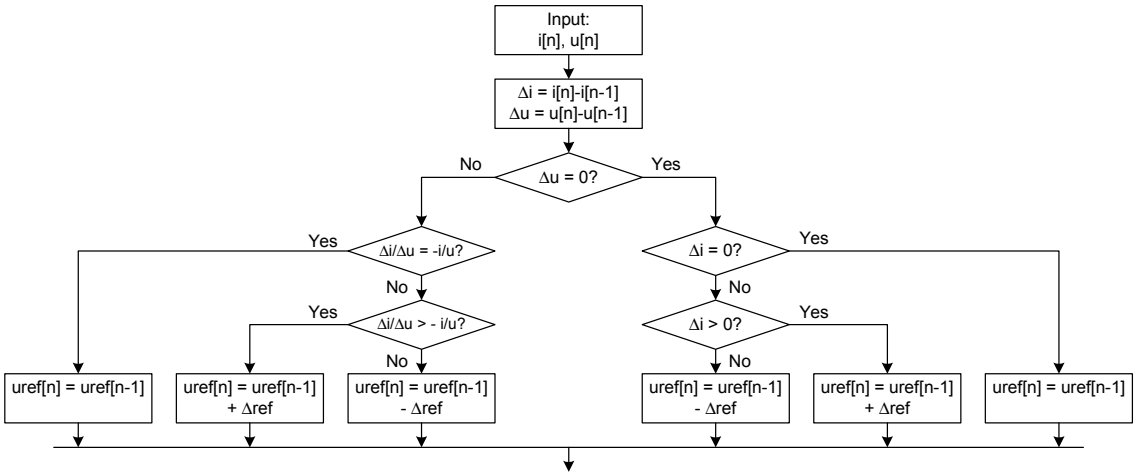

Figure 6.2. Flow chart of the incremental conductance MPPT algorithm [28].

The algorithm is bypassed by the conditions: $\Delta i = 0$ and $\Delta i/\Delta u + i/u = 0$, when the MPP is tracked, thus the power is no more fluctuating around the MPP.

The largest disadvantage with the IndCond algorithm, as with the other algorithms, is the problem of tracing the global maximum when the module is partial shadowed, c.f. Figure 2.8. Adding a scan mode to the algorithm can solve this. This is done in [100] where the voltage/current characteristic is scanned, during 40 ms, every 12 second, with a high amplitude signal to increase the signal-to-noise ratio. This also helps to increase the resolution of the sensed current, which can be a problem at low irradiance. The output from the scan is the co-ordinates for the global MPP, which then is used as the new reference before the IndCond algorithm is turned on again. This approach does not require any additional hardware. Another solution during partial shadowing is to make an initial estimation of u_{MPP}/i_{MPP} as $(0.8 \cdot U_{OC})/(0.9 \cdot I_{SC})$ [101], where U_{OC} and I_{SC} is monitored in the same way as in section 6.1.1. This helps to track the global MPP, even under severe partial shadow. However, this solution requires an additional circuit to perform the online estimation of U_{OC} and I_{SC}. Some issues about digital implementation of the IndCond algorithm are given in [102].

6.1.5 Proposed MPPT

All the algorithms presented above include some disadvantages such as: erroneously detection of the MPP during rapid changes in the irradiation and under partial shadow; need for additional circuits for monitoring the closed loop current and open loop voltage; and fluctuation around the MPP. A solution is an extended sweep algorithm, presented in Figure 6.3.

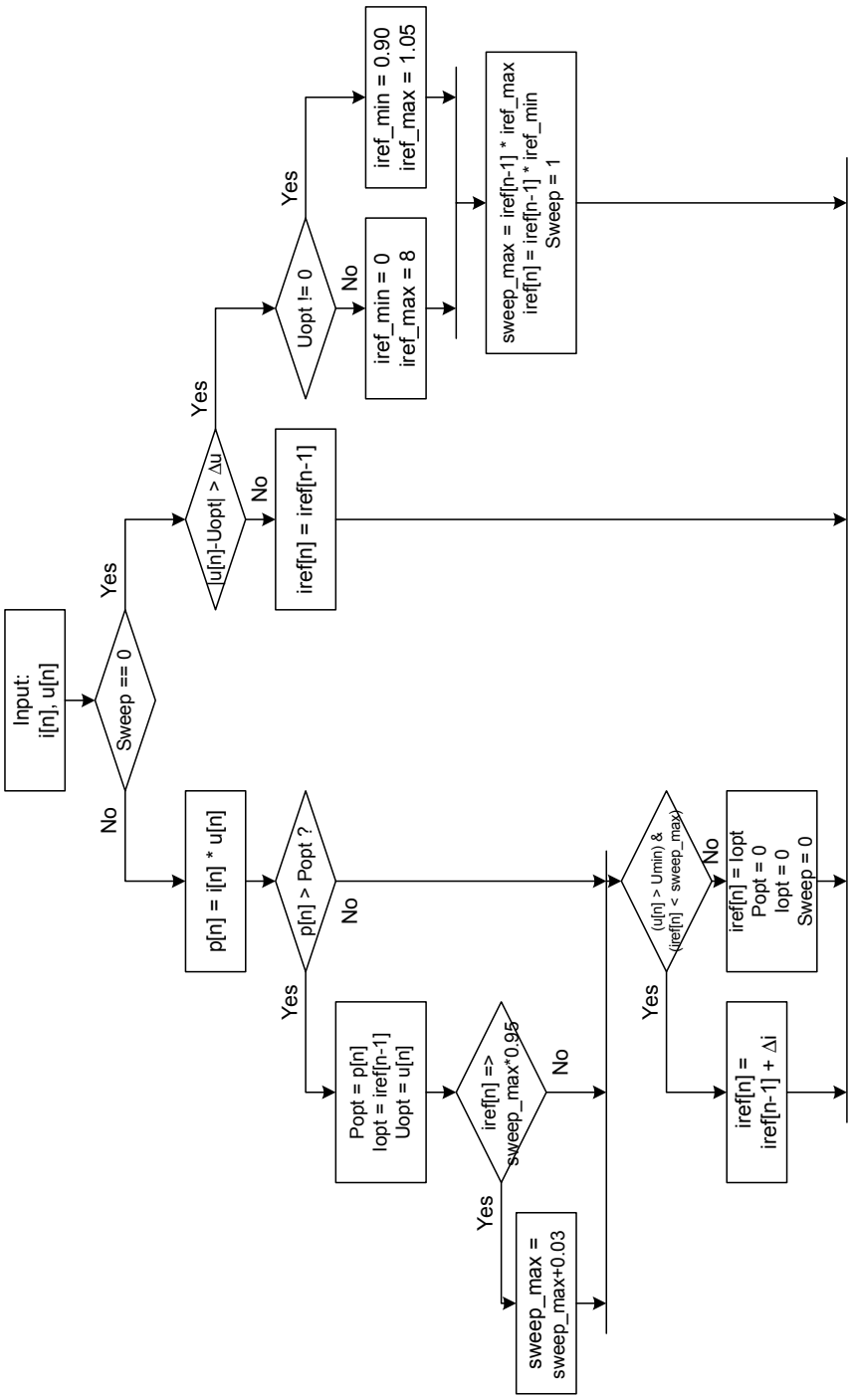

Figure 6.3. Flow chart for the proposed MPPT.

Mode of operation: It is assumed that the PV module is operated at a given point. While this is on going, the algorithm is monitoring the instantaneous module voltage, which should be equal to the recorded MPP voltage. Due to changes in temperature and/or irradiation, the instantaneous voltage will also change if the current is kept constant. Thus, instead of performing a new sweep every 10th second, or so, a new sweep is only initialized when the module voltage has changed more than ΔU from the original MPP voltage. Moreover, the sweeping range is necessarily not equal to the entire module current range (from open circuit operation to the short circuit operation), but could be a fraction of the original MPP current, e.g. ΔI. This ensures a fast sweep, where only a little energy is lost ■

The size of ΔU to start a new sweep is a trade off between power lost due to deviation from the real MPP during monitoring, and stability of the algorithm, i.e. how often the characteristic is swept. The change in the voltage across the module, Δu_{PV}, when the input current to the DC-DC converter is constant and the short-circuit current is changed by an amount of Δi_{SC}, is (partly from equation (2.7)):

$$\Delta u_{PV} \approx \frac{U_{MPP}}{I_{MPP}} \cdot \Delta i_{SC}\,, \tag{6.4}$$

when operated in the nearby region of the MPP. The threshold value to initiate a new sweep is set to 3% of the actual MPP current, which involves that sweep-mode is entered when the voltage has changed more than 3% from the previous MPP voltage.

The sweeping range is merely selected to be equal to $0.90 \cdot I_{MPP}$ to $1.05 \cdot I_{MPP}$, but is increased by additional 0.03 if the recorded power in the last sweeping-point exceeds the power in the next-last point. This is done to ensure that the MPP always will be tracked during the sweep. An Under-Voltage-Lock-Out (UVLO) is also included in the algorithm, not illustrated in Figure 6.3, which decreases the current reference to 0.90 if the PV module voltage decreases below 20.0 V and starts the sweeping mode. This to ensure than the voltage never collapses.

Finally, the algorithm must be able to follow the maximum rate-of-change-of-current, di_{sc}/dt, is order to track the MPP during rapid changes in the irradiation. The rate-of-change-of-current is proportional to the rate-of-change-of-irradiation, which is assumed to have a maximum value of 1000 W/(m^2·s)[6]. The STC short circuit current for modules is measured at 1000 W/m^2. Thus, the duration of the sweep, from zero-current and until the module voltage reached a predefined minimum, should not be larger than 1 second.

6.1.6 Simulated Results

The proposed MPPT algorithm is simulated in MATLAB/SIMULINK. The models of the PV module and the DC-DC converter are implemented in SIMULINK, together with the MPPT algorithm. The algorithm is programmed in C-code and compiled into an s-function for SIMULINK. The model of the PV module is based on the Shell Ultra175 module, operated at various irradiations but constant cell temperature. The temperature is kept constant, in order to make a simple prediction of the maximum available power for a given amount of irradiation.

The following is applied to all simulations: The function generating the normal-distribution irradiation is sampled every 0.5 s. The output from the normal-distribution generator is multiplied with a noise-signal with mean 1.0 and variance $(0.01/3)^2$ (corresponds to a signal within the range from app. 0.99 to 1.01). Finally, the irradiance is rate-limited to ± 1000 W/(m^2·s), in order to keep realistic rate-of-change-of-irradiance.

A simulation of increasing and decreasing irradiation is depicted in Figure 6.4. Another set of eight simulations, with two different mean irradiations and four different variances are also made in order to evaluate the steady state efficiency of the MPPT algorithm at low and high irradiation. The results are presented in Table 6.1.

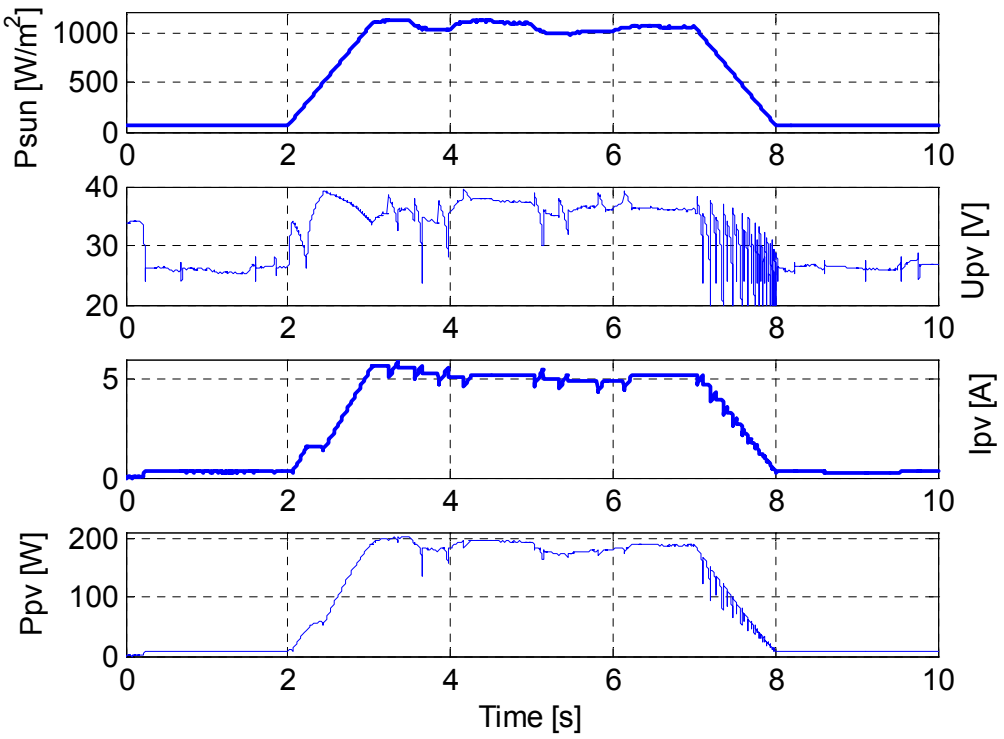

Figure 6.4. Simulated results for the proposed MPPT algorithm. The total efficiency is evaluated to 98.0%. From top and down: 1) Upper is shown the amount of solar irradiation. The high-level irradiation is defined in the span from 990 W/m^2 to 1140 W/m^2 in the time span from 3.0 s to 7.0 s. The low-level irradiation is approximately 60 W/m^2. 2) Voltage across the PV module. 3) Current drawn from the PV module. 4) Power generated by the PV module.

The total MPPT efficiency (simulated) in Figure 6.4 is evaluated to 98.0%, and can be broken down to the following intervals (P_{PV}/P_{MPP}):

- Low irradiation (app. 60 W/m^2): 28.5 J / 30.2 J = 94.3%,
- Increasing irradiation: 92.7 J / 99.5 J = 93.2%,
- High irradiation (app. 1100 W/m^2): 741 J / 748 J = 99.1%,
- Decreasing irradiation: 92.4 J / 96.6 J = 95.7%.

This shown that the efficiency is good; both for low, high, increasing and decreasing irradiation. Similar measurements are shown in Figure 7.17

The steady state performance evaluated in Table 6.1 shows that the proposed algorithm is capable of tracking the MPP with good accuracy, even that the irradiation is constantly changing (like the span from time = 3.0 s to 7.0 s in Figure 6.4). The proposed MPPT algorithm is therefore considered designed.

Table 6.1. Simulated results for the proposed MPPT algorithm.

Mean irradiation [W/m^2]	100	100	100	100	1000	1001	1002	1003
Standard deviation [W/m^2]	0.34	2.2	4.3	6.4	2.9	21.2	41.3	60.7
Variance [(W/m^2)^2]	0.11	4.8	18.3	40.9	8.6	448	1708	3689
Maximum ripple amplitude [W/m^2]	1.2	4.0	7.3	10.7	11	40	73	106
Captured energy [J]	132.9	133.2	133.4	133.7	1743	1725	1738	1760
MPP energy [J]	133.0	133.0	133.1	132.4	1753	1755	1758	1737
MPPT efficiency [%]	99.9	99.8	99.7	99.0	99.4	98.3	98.9	98.7

6.2 Phase Locked Loop

The aim of the Phase Locked Loop (PLL) is to track the fundamental grid voltage, even though that severe background harmonics are present. Thus, the PLL can be regarded as a high-order band-pass filter, with zero phase distortion.

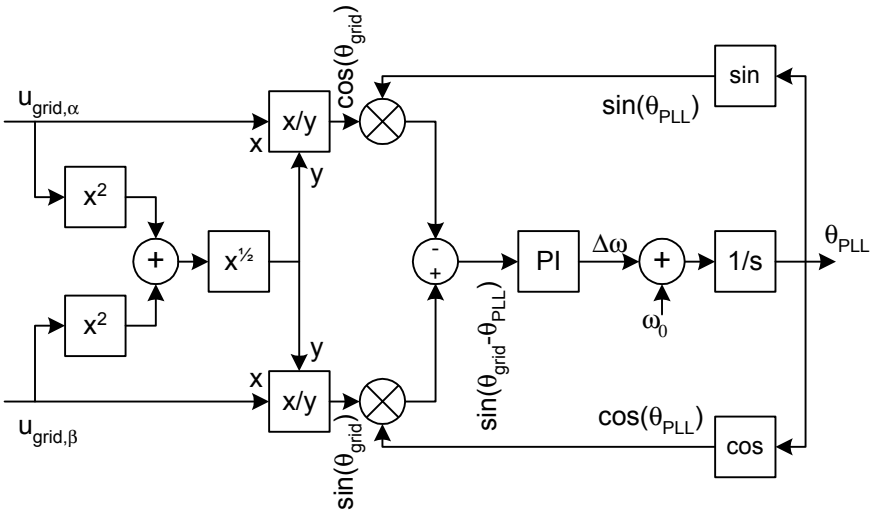

Figure 6.5. Phase Locked Loop (PLL) used to synchronize a 3 phase dynamic voltage restorer with the grid in [103].

The basic structure of the PLL is shown in Figure 6.5 [103]. However, [103] do not contain any information about how to tune the PLL structure.

The inputs to the structure are the α and β components of the grid-voltage, which is not possible for a single-phase grid. The output from the PLL is the fundamental sine wave. The structure uses a normalization of the grid amplitude. This is rather time-consuming in the ISR, since it requires two multiplications, two divisions and a square-root operation. This is not necessary, since the amplitude otherwise just is included as a part of the proportional gain in the PI controller. A revised PLL structure is depicted in Figure 6.6, where $\hat{U}_{grid,1}$ is the amplitude of the fundamental component at 50 Hz.

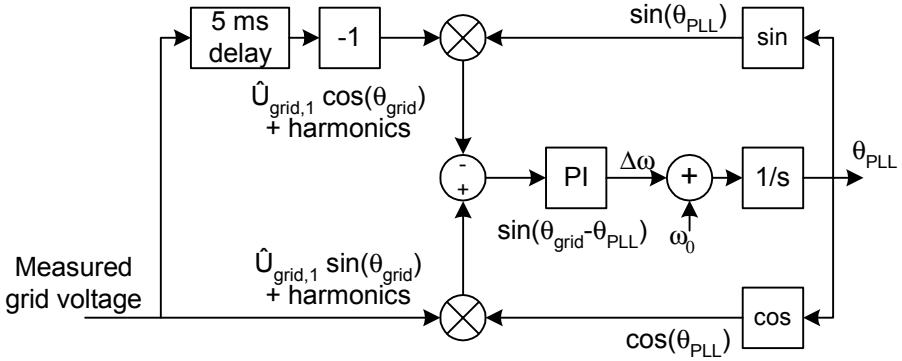

Figure 6.6. Revised PLL structure, assuming a constant frequency of the grid voltage).

The error into the PI controller included in the PLL structure is given by inspection of Figure 6.6 and assuming no harmonics and a constant frequency of 50 Hz:

$$err = \hat{u}_{grid} \cdot \sin(\theta_{grid}) \cdot \cos(\theta_{PLL}) - \hat{u}_{grid} \cdot \cos(\theta_{grid}) \cdot \sin(\theta_{PLL}) = \hat{u}_{grid} \cdot \sin(\theta_{grid} - \theta_{PLL}), \tag{6.5}$$

where θ_{grid} and θ_{PLL} are the phase of the utility grid and the output of the PLL, respectively. The right-most equals-sign can be shown valid through the multiplication- and addition-formulas for trigonometric functions. The input to the PI controller is linearized around a working point, in order to tune the parameters within the PI controller.

Recognizing that error into the PI controller (θ_{grid} - θ_{PLL}) is equal to zero at steady state operation, the linearized error into the PI controller can be described by a Taylor series as:

$$f(x) \approx f(X_0) + f'(X_0) \cdot (x - X_0) \Leftrightarrow \sin(x)\big|_{x=0} = \cos(0) \cdot (x - 0) = x\,. \tag{6.6}$$

Thus, the error into the PI controller becomes:

$$err \approx \hat{u}_{grid} \cdot (\theta_{grid} - \theta_{PLL})\,. \tag{6.7}$$

The linearized small-signal transfer function of the PLL is:

$$PLL(s) = \frac{\hat{u}_{grid} \cdot PI(s) \cdot \frac{1}{s}}{1 + \hat{u}_{grid} \cdot PI(s) \cdot \frac{1}{s}} = \frac{\hat{u}_{grid} \cdot PI(s)}{s + \hat{u}_{grid} \cdot PI(s)} = \frac{\frac{\hat{u}_{grid} \cdot Kp}{T_i} \cdot (T_i \cdot s + 1)}{s^2 + \hat{u}_{grid} \cdot K_p \cdot s + \frac{\hat{u}_{grid} \cdot K_p}{T_i}}, \tag{6.8}$$

which is a typical second order system with one real zero. K_p is the proportional gain, and T_i is the integrator time constant. The natural frequency and damping can thus be stated as:

$$\omega_n = \sqrt{\frac{\hat{u}_{grid} \cdot K_p}{T_i}}, \tag{6.9}$$

$$\xi = \sqrt{\frac{\hat{u}_{grid} \cdot T_i \cdot K_p}{4}}, \tag{6.10}$$

An optimal damping ratio in terms of rise time and overshoot is known to be $\sqrt{1/2}$ [93]. Moreover, the relationship between the natural frequency and the rise time for a second order system (without zeros) is known to be [93]:

$$t_r \approx \frac{1.8}{\omega_n}. \tag{6.11}$$

The parameters describing the PI controller can then be specified in terms of rise time, and grid voltage amplitude:

$$T_i \approx \frac{\sqrt{2}}{\omega_n} \approx 0.79 \cdot t_r, \tag{6.12}$$

$$Kp \approx \frac{\omega_n \cdot \sqrt{2}}{\hat{u}_{grid}} \approx \frac{2.55}{t_r \cdot \hat{u}_{grid}}. \tag{6.13}$$

For a rise time of 10 ms, with optimal damping and European systems, the parameters of the PI controller equals: $K_p = 0.78$, and $T_i = 7.9 \times 10^{-3}$. A Bode plot is shown in Figure 6.7 for different values of the amplitude of the grid voltage, $\hat{u}_{grid}$, and fixed controller parameters.

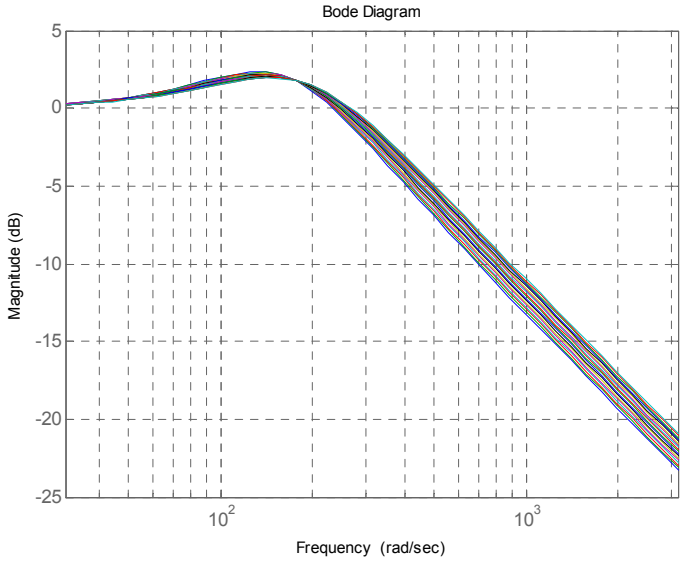

Figure 6.7. Bode plot of the closed loop transfer function, when the peak grid voltage is swept from 275 V to 360 V. Controller parameters: $K_p = 0.783$, and $T_i = 7.86 \times 10^{-3}$, x-axis span: 5 Hz to 500 Hz.

The cosine-component of the grid voltage, $\cos(\theta_{grid})$, is computed by delaying the measured grid voltage, $\sin(\theta_{grid})$, with 90° (corresponds to 5 ms at 50 Hz) and multiplying the result with –1, cf. Figure 6.6. Differentiating or integrating the measured grid voltage could also estimate the cosine component. The delay-procedure is also used to compute the cosine component of the PLL output. This is done to reduce the phase error at frequencies different from 50 Hz (the 90 degree phase in the delay block).

If the 90° phase of the delay is incorrect, i.e. the grid frequency differs from the nominal 50 Hz, the output from the 5 ms delay-block in Figure 6.6 is $\cos(\theta_{grid})+A\cdot\sin(\theta_{grid})$. Assuming that a cosine trigonometric function is used to compute the $\cos(\theta_{PLL})$, the error into the PI controller then becomes:

$$\begin{aligned} err,\cos &= \hat{u}_{grid}\cdot\sin(\theta_{grid})\cdot\cos(\theta_{PLL})-\hat{u}_{grid}\cdot[\cos(\theta_{grid})+A\cdot\sin(\theta_{grid})]\cdot\sin(\theta_{PLL}) \\ &= \hat{u}_{grid}\cdot\sin(\theta_{grid}-\theta_{PLL})+\hat{u}_{grid}A\cdot\sin(\theta_{grid})\cdot\sin(\theta_{PLL}), \end{aligned} \tag{6.14}$$

which contains an additional AC component at $\omega_{grid} + \omega_{PLL}$ rad/s (the right-most part of the equation). On the other hand, if the cosine of the PLL is substituted with another 5 ms delay-block, the error into the PI controller becomes:

$$\begin{aligned} err,5ms &= \hat{u}_{grid}\cdot\sin(\theta_{grid})\cdot[\cos(\theta_{PLL})+A\cdot\sin(\theta_{PLL})]-\hat{u}_{grid}\cdot[\cos(\theta_{grid})+A\cdot\sin(\theta_{grid})]\cdot\sin(\theta_{PLL}) \\ &= \hat{u}_{grid}\cdot\sin(\theta_{grid}-\theta_{PLL}), \end{aligned} \tag{6.15}$$

which is equal to the result in (6.5). Thus the errors cancels each other, and no oscillations are present. This is also verified in Figure 6.8 and Figure 6.9.

The PI controller and integrator for the PLL is implemented in discrete time by emulation, cf. section 6.6.2.

6.2.1 Simulated Results

Three events are simulated in the first simulation, cf. Figure 6.8, Figure 6.9 and Figure 6.10. They are: voltage jumps from 230 V to 196 V, to 253 V and back to 230 V; phase jumps from 0° to -30°, to +30° and back to 0°, and frequency jumps from 50 Hz to 48 Hz, to 52 Hz, and back to 50 Hz. Both implementations of $\cos(\theta_{PLL})$ is shown, in order to evaluate the theory given above. Each of the components in the grid voltage is given as:

$$\begin{aligned} u_{grid,n} &= \hat{U}_{grid,n}\cdot\sin(\theta_{grid,n}) \\ \theta_{grid,n} &= \int n\cdot\omega_{grid}\,dt+\theta_{grid,0} \end{aligned} \tag{6.16}$$

where $u_{grid,n}$ is the time value of the n^{th} component, $\hat{U}_{grid,n}$ is the amplitude of the n^{th} component, $\theta_{grid,n}$ is phase of the n^{th} component, ω_{grid} is the fundamental angular frequency og the grid, and $\theta_{grid,0}$ is the phase of the entire voltage.

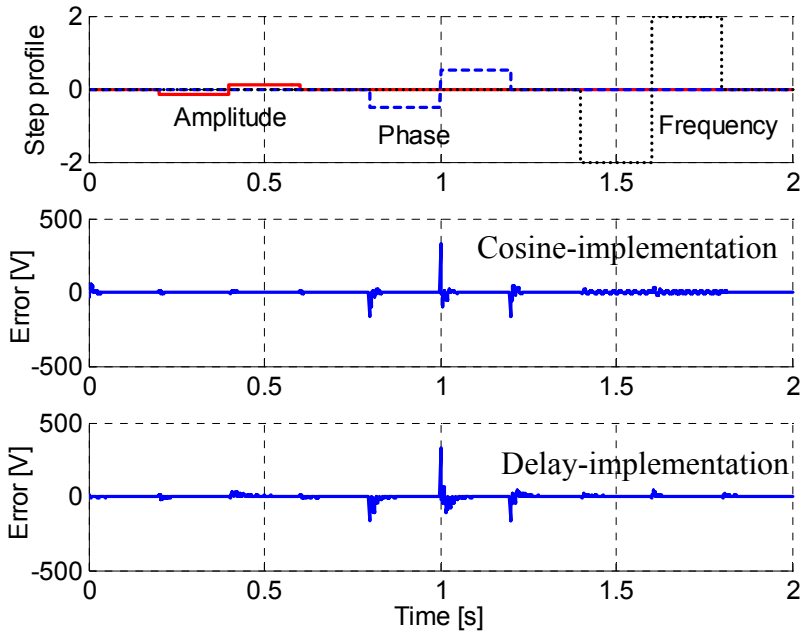

Figure 6.8. Simulated results. Upper is the step profiles shown: voltage –15% & 10%, phase: ±30 degrees (±0.52 rad), frequency: ± 2 Hz. Middle is the error between the PLL output and the real grid, when a cosine is used in the PLL structure. Lowest is the error, when the cosine is replaced with a 5 ms delay block.

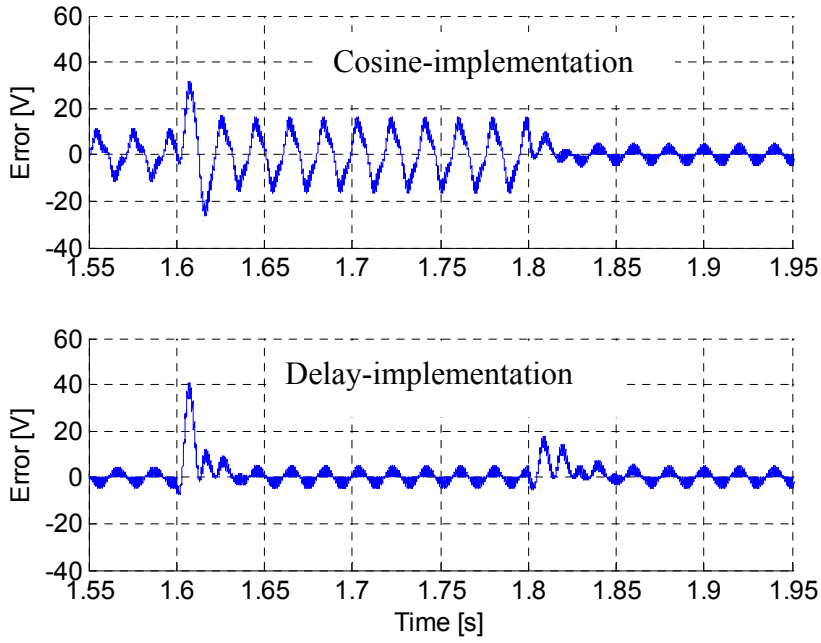

Figure 6.9. Simulated results. Zoom of the two lower plots in Figure 6.8, from time = 1.55 s to 1.95 s. The cosine implementation includes some oscillation in the output of the PLL when the grid frequency is shifted with ± 2 Hz. These oscillations are not seen in the delay-implementation.

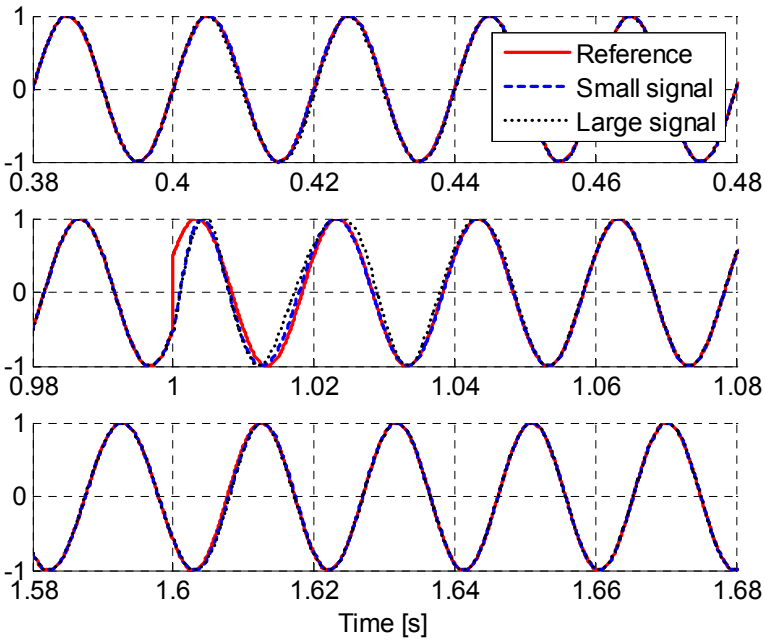

Figure 6.10. Simulated results for the PLL small-signal and large-signal models (steps in amplitude, phase, and frequency according to Figure 6.8). The solid lines are the fundamental from the grid, which is used as reference. The dashed lines are from a small-signal model, based on (6.8), (6.57) and (6.58). The dotted lines are from the large-signal model in Figure 6.6, also implemented in discrete time and with the 5 ms delay.

The simulation reveals that an AC component is present in the difference between the output of the PLL and the fundamental of the grid (the error into the PI controller), when a cosine-trigonometric function is used to compute $\cos(\theta_{PLL})$. This is best seen in Figure 6.9. The AC component is removed when the cosine-function is substituted with the delay-approach. The results in Figure 6.10 shows that the developed small-signal model in (6.8) agrees with the large-signal model in Figure 6.6.

6.3 Detection of Islanding Operation

A simple islanding detection scheme is implemented in the inverter. The grid voltage must be within 230 V $\pm$ $^{10\%}_{15\%}$ and the grid frequency must be within 50 $\pm$ 2 Hz. The inverter must cease injecting power into the grid, within 0.1 second, if these limits are broken, cf. chapter 3.

Table 6.2. Simulated voltage harmonics in the grid. RMS value of fundamental component = 230.0 V, RMS value of all components = 231.3 V, and THD = 10.5%

Harmonic number [ ]	1	3	5	7	9	11	13
Voltage [V]	230	5.0%	6.0%	5.0%	1.5%	3.5%	3.0%
Phase [degree]	178.2	0	0	0	0	0	0

The grid voltage can be monitored in many different ways: Average of the absolute grid voltage, Root Means Square (RMS) of the grid voltage, amplitude detection of the grid voltage by using the $\sin^2(x) + \cos^2(x) = 1$ relationship, and Fourier sine-transform of the grid voltage:

$$\left\langle \left| U_{grid} \right| \right\rangle_{20ms} = \frac{1}{20ms} \cdot \int_0^{20ms} \left| u_{grid} \right| dt \ , \tag{6.17}$$

$$\left(U_{grid} \right)^2 = \frac{1}{20ms} \cdot \int_0^{20ms} \left(u_{grid} \right)^2 dt \ , \tag{6.18}$$

$$\left(\hat{U}_{grid} \right)^2 = \left(u_{grid} \right)^2 + \left(delay\left(u_{grid}, 5ms \right) \right)^2 \ , \tag{6.19}$$

$$\hat{U}_{grid} = \frac{2}{20ms} \cdot \int_0^{20ms} u_{grid} \cdot \sin(\theta_{PLL}) \, dt \ . \tag{6.20}$$

Simulations are used to evaluate all four algorithms.

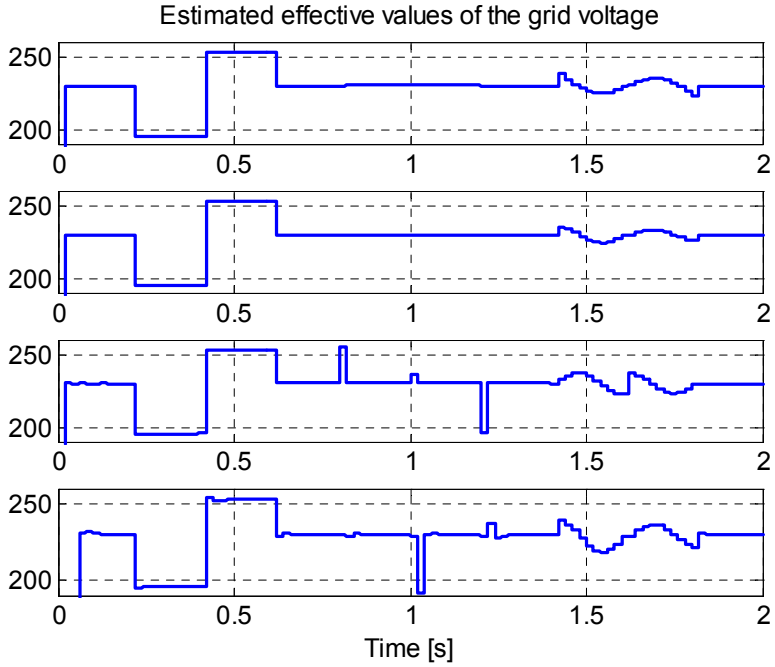

Figure 6.11. Simulated results. The grid voltage is equal to the one in Figure 6.8, which contains steps in amplitude, phase and frequency. From top and down: Average of absolute grid voltage, Root mean square, sin-cosine relationship, and Fourier sine-transform.

The results in Figure 6.11 are for shifts in grid-amplitude, -phase and -frequency, without harmonics, like in Figure 6.8. All four algorithms are detecting the correct value when amplitude jumps are present, but all are having troubles with detecting the correct values (and RMS value of 230 V) when the frequency is shifted. This is caused by the fact that the correct time of integration no more is equal to 20 ms, or that the correct delay time no more is equal to 5 ms. The last two algorithms have slight problems in detecting the correct value during the phase jump, but they obtain correct values after the transients.

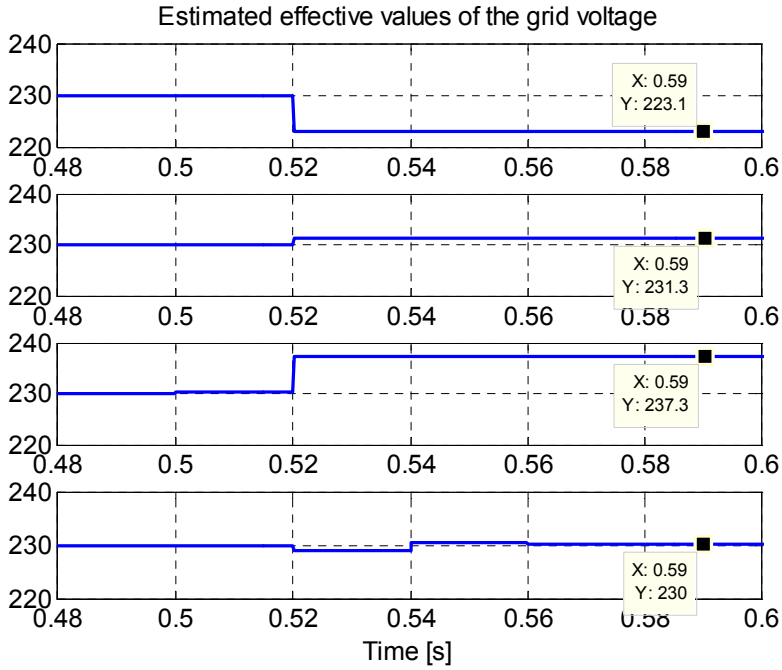

Figure 6.12. Simulated results. The grid voltage is equal to the one in Table 6.2, which contains many harmonics. The harmonics are turned on at time = 0.50 s. The RMS value is equal to 230.0 V before the harmonics are turned on, and 231.3 V after. From top and down: Average of absolute grid voltage, Root mean square, sin-cosine relationship, and Fourier sine transform.

The results in Figure 6.12 are when severe harmonics are present in the grid voltage, according to Table 6.2. Only the RMS and the Fourier sine-transform algorithms succeed in estimating the correct values. The averaging algorithm underestimates the value and the sin-cosine relationship algorithm overestimates it.

The averaging algorithm is far the easiest to implement in the ISR since it only requires an integrator. The RMS and the Fourier sine-transform algorithms are a little more demanding, since they do also require a multiplication of two time-varying signals. Finally, the sin-cosine relationship algorithm requires a 5 ms delay of the sampled signal and two multiplications (the delay is already included in the PLL), or a 5 ms delay of the sampled signal, raised to the second power (not included in the PLL). Taking all these issues into consideration, the RMS algorithm seems to be the best candidate for detecting the level of voltage, both in term of precision and implementation.

The frequency of the grid is monitored by the output of the PI controller included in the PLL structure. The output of the PI controller is equal to the difference between the actual frequency and the nominal frequency (ω_0 in Figure 6.6).

The output from the calculation of the RMS value of the grid voltage, and the output from the PI controller are both fed to a detection circuit similar to the one illustrated in Figure 6.13. The purpose of the circuit is to detect if its input parameter is outside the premised range. The output signal of the circuit goes low, indicating an islanding situation, if the input signal exceeded the limit in more than 0.1 second. This is done to avoid nuance tripping of the inverter, in case of the normal dynamics events (phase and amplitude jumps) in the grid.

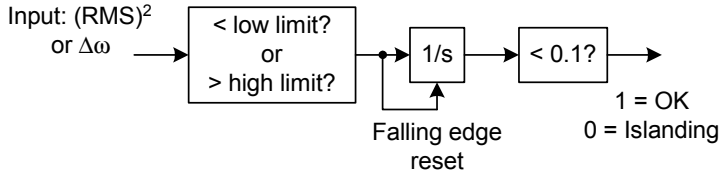

Figure 6.13. Islanding detection circuit for the RMS value or frequency of the grid voltage. The input signal must be outside its limits in least 0.1 second, before the inverter is stopped, this to avoid nuance tripping. The limits in the right-most block are equal to (230 V · 0.85)² and (230 V · 1.10)². The limits is substituted with $\pm 2 \cdot 2\pi$ for the frequency monitoring scheme.

6.4 Control of DC-link Voltage

6.4.1 DC-link Voltage Reference

The reference for the DC-link voltage is made as a function of grid voltage and power injected into the grid, in order to keep the DC-link voltage as low as possible. This is desirable in order to keep the switching losses in the MOSFETs low. The reference is based on the peak grid voltage and voltage drop across the MOSFETs and LCL filter in the DC-AC inverter:

$$U_{DC,\min} = \langle U_{DC} \rangle - \tilde{u}_{DC} \geq \left(U_{grid} + \frac{P_{DC} \cdot Z_{cond}}{U_{grid}} \right) \cdot \sqrt{2} \,, \tag{6.21}$$

where $<U_{DC}>$ is the average DC-link voltage, $\tilde{u}_{DC}$ is the amplitude of the 100 Hz ripple in the DC-link, P_{DC} is the DC-link power, Z_{cond} is the impedance included in two MOSFETs and the LCL filter, and assuming unity efficiency and power factor.

The amplitude, $\tilde{u}_{DC}$, is computed in chapter 5 as $P_{DC} / (2 \cdot \omega \cdot <U_{DC}> \cdot C_{DC})$. Substituting this into (6.21), and re-arranging the terms yields:

$$\begin{aligned} \langle U_{DC} \rangle &= U_{DC,\min} + \frac{P_{DC}}{2 \cdot \omega \cdot \langle U_{DC} \rangle \cdot C_{DC}} \Leftrightarrow \\ \langle U_{DC} \rangle^2 &= U_{DC,\min} \cdot \langle U_{DC} \rangle + \frac{P_{DC}}{2 \cdot \omega \cdot C_{DC}} \Leftrightarrow \,, \\ \langle U_{DC} \rangle^2 &- U_{DC,\min} \cdot \langle U_{DC} \rangle - \frac{P_{DC}}{2 \cdot \omega \cdot C_{DC}} = 0 \end{aligned} \tag{6.22}$$

which is a typical second-order polynomial, where the positive root is equal to the desired reference:

$$\langle U_{DC} \rangle = \frac{U_{DC,\min} \pm \sqrt{U_{DC,\min}{}^2 + \frac{2 \cdot P_{DC}}{\omega \cdot C_{DC}}}}{2} \,, \tag{6.23}$$

By using (6.23) as a reference for the DC-link voltage, it is ensured that there always is enough voltage to keep the grid current under control. And in the meantime, the DC-link voltage is kept at a minimum. The expression in (6.23) is linearized around an operating point, while the square-root operation requires a lot of computational time in the ISR. The reference for the DC-link voltage is given as:

$$U_{DC,ref} = U_{DC(0)} + \alpha \cdot \left(P_{DC} - P_{DC(0)}\right) + \beta \cdot \left(U_{grid} - U_{grid(0)}\right), \tag{6.24}$$

where $U_{DC(0)}$, $P_{DC(0)}$ and $U_{grid(0)}$ are the nominal operating points. The coefficients $U_{DC(0)}$, α and β are given as:

$$U_{dc(0)} = \sqrt{2} \cdot U_{grid(0)} = \hat{U}_{grid(0)}, \tag{6.25}$$

$$\alpha = \frac{1}{\sqrt{2}} \cdot \frac{2 \cdot Z_{cond} + \dfrac{1}{2 \cdot \omega \cdot C_{dc}}}{U_{grid(0)}}, \tag{6.26}$$

$$\beta = \sqrt{2}\,. \tag{6.27}$$

The following nominal points are merely selected: $U_{grid(0)}$ = 195 V (230 V ·0.85), $P_{DC(0)}$ = 0 W, Z_{cond} = 6.2 Ω, ω = 314 rad/s, and C_{DC} = 33 µF. The reference is thereby given as:

$$U_{DC,ref} = 0.22 \cdot P_{DC} + \hat{U}_{grid}\,. \tag{6.28}$$

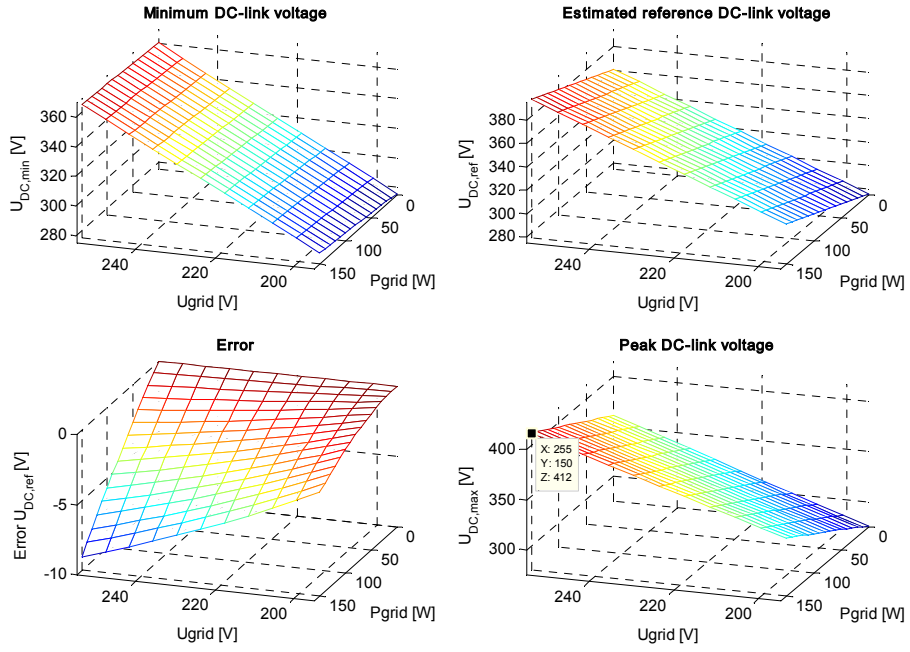

Figure 6.14. Upper Left) Minimum DC-link voltage, based on (6.21). Upper Right) Estimated DC-link voltage reference, based on (6.28). Lower Left) Difference between original expression (6.23) and linearized expression (6.28). Selecting other values for the nominal operating points could decrease the error. Lower Right) Maximum DC-link voltage, based on (6.28) and the prediction of the amplitude of the DC-link voltage ripple in chapter 5.

The reference computed by (6.28) is depicted in Figure 6.14, together with error between the real and the estimated references, and the minimum and maximum DC-link voltages. The maximum level in the DC-link reaches 412 V at a grid voltage of 255 V and a power generation of 150 W. The DC-link capacitor is rated to 450 V and the MOSFETs are rated to 600 V, so the level of 412 V is not seen as a problem.

6.4.2 DC-link Voltage Controller

The aim of the DC-link controller is to control the average value of the DC-link voltage. The 100 Hz ripple in the DC-link is therefore not considered.

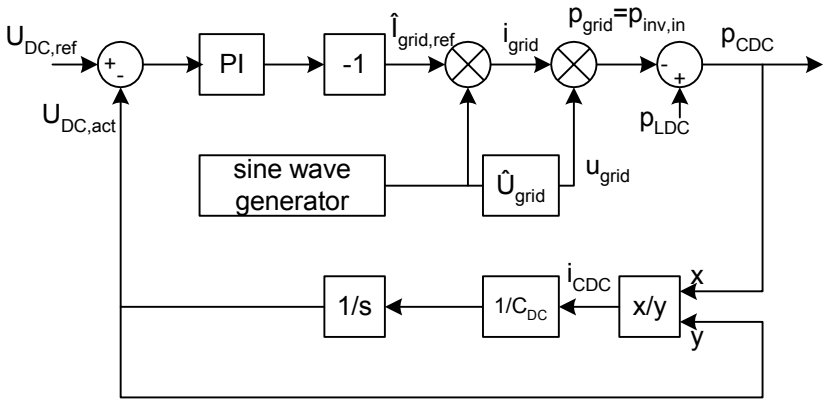

Figure 6.15. Block diagram representation of the interaction between the DC-link capacitor, the PI controller and the power injection into the grid.

The control loop depicted in Figure 6.15 is made up around a PI controller, a part including a sine raised to the second power (the two mixers denoted by ⊗) to model the pulsating power injected into the grid. A division (gain of $1/u_{DC}$) for modeling the current drawn from the DC-link capacitor, and a power of magnitude p_{LDC} to model the current injected into the DC-link from the DC-DC converter. The DC-link is modeled as a capacitor by the blocks: $1/C_{DC}$ and the integrator.

The system presented in Figure 6.15 must be linearized, in respect to the sinusoidal raised to the second power, and the division with u_{DC}. The part including the sine raised to the second power is averaged over a half grid period (this corresponds to neglecting the 100 Hz ripple in the DC-link), which yields:

$$gain = \frac{1}{10ms} \cdot \int_0^{10ms} \sin^2(2 \cdot \pi \cdot 50 \cdot t)\, dt = 0.5\,, \tag{6.29}$$

thus, the relationship between power injected into the grid and the command current is (assuming that the grid current follows the command!):

$$\langle Pgrid \rangle = \frac{\hat{U}grid \cdot \hat{I}grid}{2}\,. \tag{6.30}$$

The division with u_{DC} is non-linear, since u_{DC} is the variable that must be controlled. It can be linearized by a Taylor approximation:

$$\frac{1}{u_{DC}} \approx \frac{2 \cdot U_{DC,0} - u_{DC}}{U_{DC,0}^{\,2}} \approx \frac{1}{U_{DC,0}}, \tag{6.31}$$

for $u_{DC} \approx U_{DC,0}$, where $U_{DC,0}$ is the value, that the function is linearized around. A new system can thus be drawn, cf. Figure 6.16.

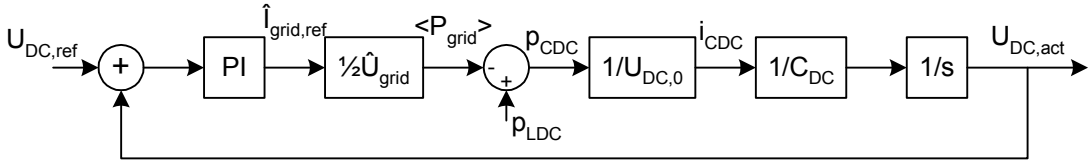

Figure 6.16. Redrawn structure for the DC-link voltage controller.

The closed loop transfer function is:

$$H(s) = \frac{K_{sys} \cdot K_p \cdot (s \cdot T_i + 1)}{s^2 \cdot T_i \cdot C_{DC} + K_{sys} \cdot K_p \cdot (s \cdot T_i + 1)}, \; K_{sys} = \frac{\hat{u}_{grid}}{2 \cdot U_{DC,0}}. \tag{6.32}$$

It turns out that the system is a second order system, with one real zero. Thus, the system can be evaluated by the damping ratio and the natural frequency:

$$\omega_n = \sqrt{\frac{K_{sys} \cdot K_p}{T_i \cdot C_{DC}}}, \quad \xi = \frac{K_{sys} \cdot K_p}{2 \cdot \omega_n \cdot C_{DC}}. \tag{6.33}$$

The controller cannot be too fast, while this would cause the grid current to become distorted, since (assuming that the grid current follows the command):

$$i_{grid} = \hat{I}_{grid,ref} \cdot \sin(\omega \cdot t), \tag{6.34}$$

where $\hat{I}_{grid,ref}$ is the output from the PI controller, which is composed by a part originating from the proportional (P) gain and a part from the integrator (I). The part from the integrator is assumed to be a constant DC value, but the part from the proportional gain is equal to a 100 Hz signal:

$$\hat{I}_{grid,ref,P} = (U_{DC,ref} - U_{DC,act}) \cdot K_p = \tilde{u}_{DC} \cdot K_p. \tag{6.35}$$

The current therefore contains a 3rd harmonic component, with amplitude K_p /2 (the ½ due to multiplication of two sine waves with different frequencies). The maximum allowable proportional gain is therefore:

$$K_p \le \frac{2 \cdot \hat{I}_{grid,3}}{\tilde{u}_{DC}}, \tag{6.36}$$

where $\hat{I}_{grid,3}$ is the amplitude of the 3rd harmonic (maximum 4% of nominal current: $\hat{I}_{grid,3}$ = 36 mA [4], [104]) and the amplitude of the DC-link ripple voltage is 20 V). The maximum allowable value of K_p is thereby $3.6 \cdot 10^{-3}$.

The maximum rate-of-change-of-power (dp/dt) during normal operation is assumed equal to 200 W/s, and the DC-link voltage must not increase beyond 450 V during this transient, in order not to damage the DC-link capacitor. The input power to the DC-link voltage transfer function is given as:

$$\frac{U_{DC}(s)}{P_{DC}(s)} = \frac{s \cdot \frac{1}{U_{DC,0} \cdot C_{DC}}}{s^2 + s \cdot \frac{K_{sys} \cdot K_p}{C_{DC}} + \frac{K_{sys} \cdot K_p}{T_i \cdot C_{DC}}} \quad . \tag{6.37}$$

The time history for the transfer function in (6.37), when exposed to a ramp in power, can be found through inverse Laplace transformation. The time-domain function is:

$$u_{DC}(t) = \frac{dP_{PV}}{dt} \cdot n \cdot \left(1 - \exp(-a \cdot t) \cdot \left(\cos(b \cdot t) + \frac{a}{b} \cdot \sin(b \cdot t)\right)\right) \tag{6.38}$$

$$n = \frac{1}{U_{DC,0} \cdot C_{DC} \cdot (a^2 + b^2)} = \frac{1}{U_{DC,0} \cdot C_{DC} \cdot \omega_n{}^2}$$

where dP_{PV}/dt is the slope in PV-power. The in- or decrease in DC-link voltage during a power-ramp is (neglecting the dynamics at the beginning of the ramp):

$$\Delta U_{DC} = \frac{dP_{PV}}{dt} \cdot \frac{T_i}{U_{DC,0} \cdot K_p \cdot K_{sys}} = \frac{dP_{PV}}{dt} \cdot \frac{1}{U_{DC,0} \cdot C_{DC} \cdot \omega_n{}^2} \, . \tag{6.39}$$

Assuming that the grid voltage is equal to 230 V + 10%, and the power is ramping from zero to 150 W. The maximum reference for the DC-link voltage is given by (6.28) to 391 V, and the amplitude of the 100 Hz ripple is found in chapter 5 to 20 V. This involves a peak value of approximately 410 V. The DC-link voltage is allowed to reach 430 V during this transient, which is below the ratings for the DC-link capacitor.

The value T_i / K_p in (6.39) is computed to 17.9. Combining this with (6.33) and $\xi = 0.71$ yields: $K_p = 2.9 \cdot 10^{-3}$ which is lower than the value computed in (6.36), $T_i = 51 \cdot 10^{-3}$, and $\omega_n = 28$ rad/s. The PI controller for the DC-link voltage is implemented in discrete time by emulation, cf. section 6.6.2.

6.4.3 Simulated Results

The difference between the reference and the actual DC-link voltage during the power ramp (200 W/s) is simulated to 21.6 V, cf. Figure 6.17, which also is the value predicted by (6.39) at the given operating conditions. The amplitude of the third harmonic grid current (assuming infinite good current controller) is equal to 29 mA, cf. Figure 6.19, which is the same as 3.2% of the fundamental. This is also the value predicted by (6.36) and the values designed above. Thus, the DC-link voltage controller does not compromise the grid current beyond the specifications and is therefore accepted.

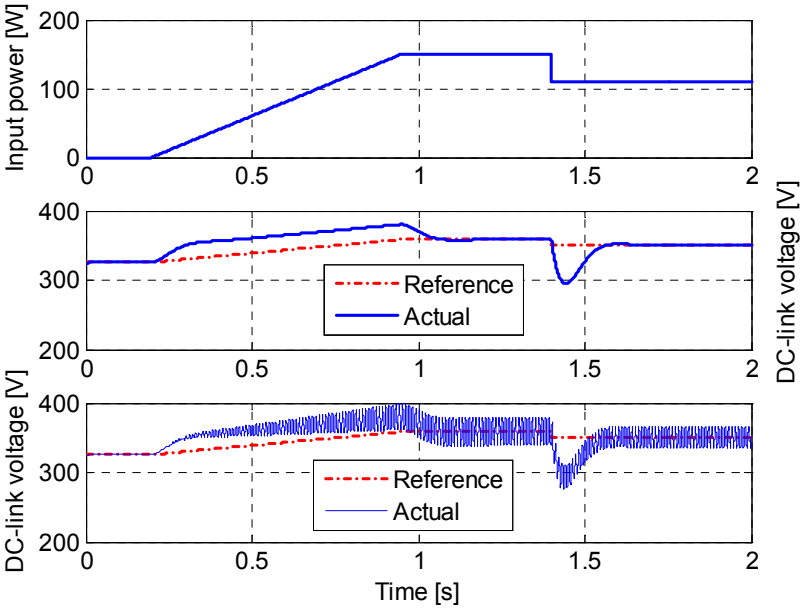

Figure 6.17. Simulated results, U_{grid} = 230 V. Upper is shown the power into the DC-link, injected by the DC/DC converter. The slope of the ramp is equal to 200 W/s, and the step is equal to -40 W. The graph in the middle shows the reference for the DC-link voltage, and the voltage simulated by the average model in Figure 6.16. The lowest plot depicts the simulation results from the large-signal model in Figure 6.15.

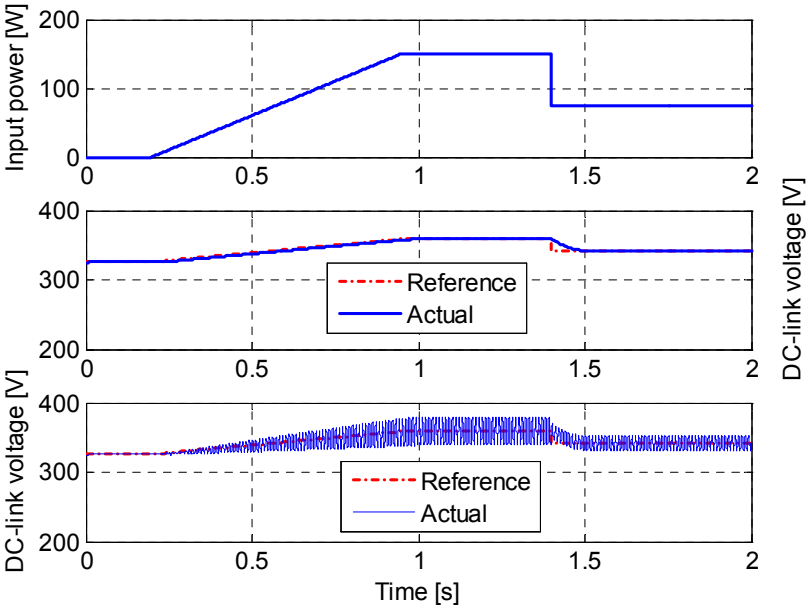

Figure 6.18. Simulated results with feed forward of the power generated by the PV module, U_{grid} = 230 V. Upper is shown the power into the DC-link, injected by the DC/DC converter. The slope of the ramp is equal to 200 W/s, and the step is equal to -80 W. The graph in the middle shows the reference for the DC-link voltage, and the voltage simulated by the average model in Figure 6.16.

However, the DC-link voltage tends to collapse ($u_{DC} < u_{grid}$) during a negative step in the power, as seen in Figure 6.17. This is not good since the DC-AC inverter then operates as a rectifier and causes large grid harmonics. This is believed to be a rare phenomenon and is therefore not regarded as being a problem. On the other hand, a feed-forward of the generated PV power can be used to improve the dynamics of the system, as illustrated in Figure 6.18. The feed forward is given as:

$$i_{feed-forward} = \frac{2 \cdot P_{PV}}{\hat{U}_{grid}}, \tag{6.40}$$

where $\hat{U}_{grid}$ is the amplitude of the grid voltage, and the computed PV power is already available from the MPPT algorithm.

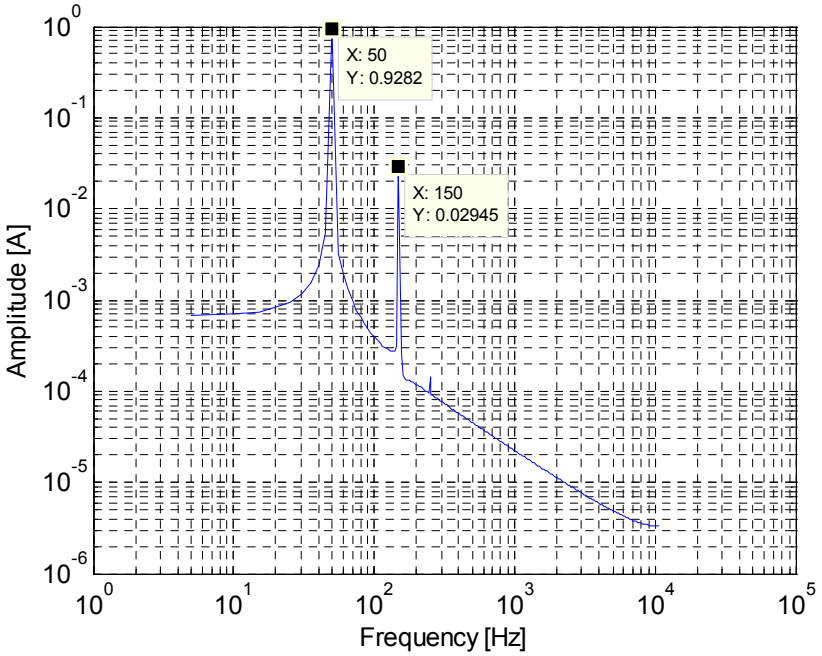

Figure 6.19. Simulated results of a FFT of the grid current. The amount of 3rd harmonic is equal to 3.2% of the fundamental, so the IEC61727 CDV and the IEEE 1547 standards are fulfilled.

6.5 Control of Grid Current

The grid current controller is designed in this section. Before continuing the design, information about the sample-and-hold of the grid current must be gained. Assuming that the grid current is sampled at random, within the switching period, the sampled signal will be constructed by the average current plus some noise. The average current is equal to the mean value of the current over the switching period. An anti-aliasing filter must therefore be inserted between the current transducer and the sample-and-hold circuit, to suppress the noise. The filter includes a phase-lag, which reduces the overall dynamics of the current controller.

On the other hand, the sampled signal can be made equal to the average current, without noise, if the current is sampled at the beginning, the middle or the end of the switching period. This is illustrated in Figure 6.20. An anti-aliasing filter is therefore not required, which results in better controller performance.

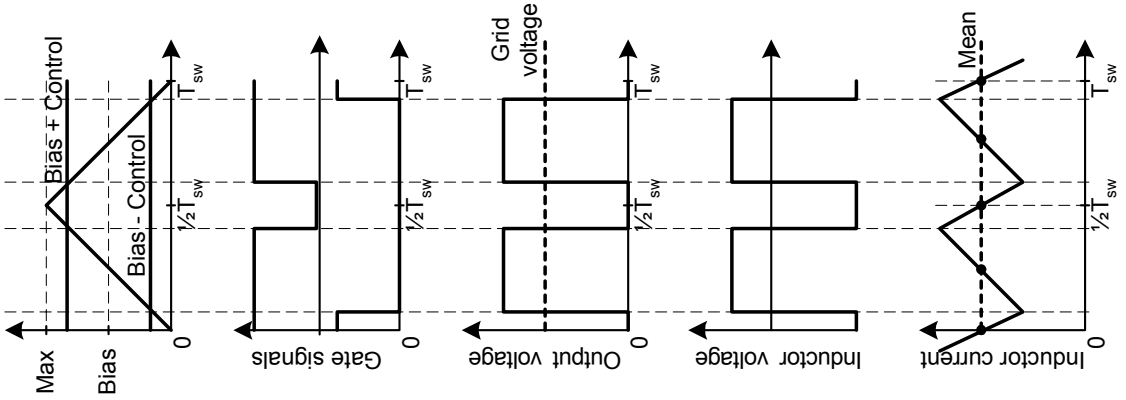

Figure 6.20. PWM with unipolar voltage switching. From top to bottom (left to right): Counter signal and the two duty-cycle signals (bias+control, and bias-control); Gate signals for the two legs (a high signal corresponds to a high output voltage, and vice versa); Output voltage from the inverter; Voltage across the LCL filter; Corresponding grid current. The dots on the grid current are where the instantaneous values are equal to the mean value.

Several types of controllers exist, e.g. the classical PI and lead-lag controllers [86], [93], and the newly discovered P+resonant controller [105], [106]. The classical controllers are good for controlling DC signals but not for alternating signals, whereas the P+resonant controller can be tuned to a specific frequency. This includes that a feed forward of the grid voltage must be used together with a classical controller; this is not necessary with the P+resonant controller.

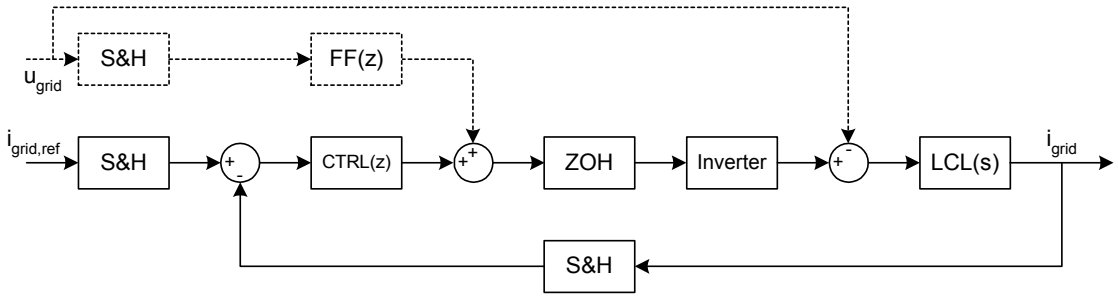

Figure 6.21. Continuous- and discrete-time system for the design of the current controller (the unit delay included in the micro-controller is assumed included in the ZOH block). The system drawn with solid lines is the primary controller circuit. The system drawn with dotted lines represents the disturbance from the grid voltage, and the corresponding feed forward.

The dynamics of the grid current is comparable with the sampling time. The grid current controller can therefore not be designed by emulation, but must be designed with discrete design [93]. The total system to be designed is illustrated in Figure 6.21, and a model of the LCL filter is shown in Figure 6.22.

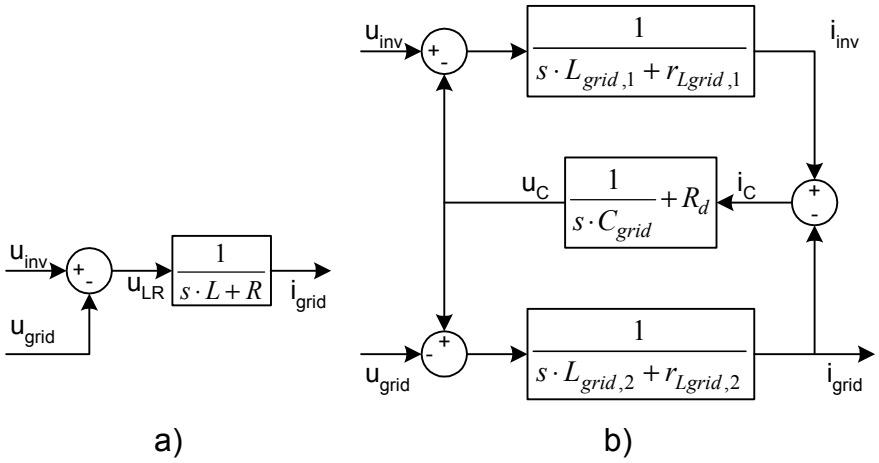

Figure 6.22. Model of the grid-connected filter. A) Simple LR representation of the filter (valid up to app. $^{1}/_{10}$ of the resonance frequency of the LCL filter) for the design of the controller, B) Extended model for evaluation of stability and for simulations [84].

The design of the controller is based on the assumption that the bandwidth of the system is lower than the resonant frequency of the LCL filter. Thus, the LCL filter is regarded as an LR filter (the inductors and their winding resistance). The stability of the filter is, however, evaluated for the entire LCL filter including damping.

The low frequency s-domain transfer function for the LR filter, without the filter capacitor, is:

$$LR(s) = \frac{i_{grid}(s)}{u_{LR}(s)} = \frac{1}{s \cdot L + R} = \frac{\frac{1}{L}}{s + \frac{R}{L}} = \frac{1}{R} \cdot \frac{\frac{R}{L}}{s + \frac{R}{L}} = \frac{1}{R} \cdot \frac{\alpha}{s + \alpha}, \alpha = \frac{R}{L}, \tag{6.41}$$

where L is the sum of $L_{grid,1}$ (connected with the inverter) and $L_{grid,2}$ (connected with the grid), and R is the sum of their winding resistances, $r_{Lgrid,1}$ and $r_{Lgrid,2}$. The transfer function is transformed into discrete time by the Zero Order Hold (ZOH) method:

$$LR(z) = \frac{1}{R} \cdot \frac{1-\beta}{z-\beta}, \quad \beta = \exp(-\tfrac{R}{L} \cdot T_{sa}) = \exp(-\alpha \cdot T_{sa}), \tag{6.42}$$

where T_{sa} is the sampling time, in this case equal to the switching frequency. The transfer function for the discrete controller is:

$$ctrl(s) = K_p \cdot \frac{z-A}{z-B}. \tag{6.43}$$

Note that the transfer function in (6.43) can be used to obtain a normal PI controller by letting $A = 1\text{-}T_{sa}/T_i$, and $B = 1$. The open loop transfer function is then:

$$OL(z) = \underbrace{K_p \cdot \frac{z-A}{z-B}}_{ctrl} \cdot \underbrace{\frac{1}{z}}_{MC} \cdot \underbrace{\frac{1}{R} \cdot \frac{1-\beta}{z-\beta}}_{LR}, \tag{6.44}$$

when including the unit-delay (1/z) from the micro controller (MC). The pole in the LR filter can be canceled with the zero included in the controller: z-A = z-β ⇒ A = β. The new open loop transfer function is then:

$$OL(z) = \frac{K_p \cdot (1-\beta)}{R} \cdot \frac{1}{(z-B)\cdot z}. \tag{6.45}$$

The parameter β can be approximated to:

$$\beta \approx 1 - \alpha \cdot T_{sa}, \tag{6.46}$$

when $\alpha \cdot T_{sa}$ is small. The closed loop transfer function is then:

$$CL(z) \approx \frac{K_p \cdot T_{sa}}{K_p \cdot T_{sa} + L \cdot (z-B)\cdot z}, \tag{6.47}$$

which has the following poles:

$$z_{1,2} = \frac{B}{2} \pm \sqrt{\frac{B^2}{4} - \frac{K_p \cdot T_{sa}}{L}}. \tag{6.48}$$

The bandwidth of the controller is to be placed between the resonant-frequency of the LCL filter (from 3.5 kHz to 4.9 kHz, nominal 4.4 kHz, depending of the amount of saturation of the inductors) and the fundamental frequency of the grid (50 Hz), thus 1.0 kHz may be a choice. The damping is selected to 0.707, which yields good response in terms of overshoot and rise time. This can be translated into the following poles for the closed loop s-domain transfer function:

$$\begin{aligned} s_{1,2} &= -\xi \cdot \omega_n \pm j \cdot \omega_n \cdot \sqrt{1-\xi^2} \\ s_{1,2} &= 4443 \cdot (-1 \pm j) \end{aligned}, \tag{6.49}$$

which again can be translated into z-domain poles:

$$\begin{aligned} z_{1,2} &= \exp(s_{1,2} \cdot T_{sa}) \\ z_{1,2} &= 0.601 \pm j \cdot 0.268 \end{aligned}. \tag{6.50}$$

This is matched with the solutions in (6.48): A = 0.965, B = 1.2 and K_p = 36, for a total inductance in the LCL filter equal to 7.9 mH. However, the designed controller is unstable in open loop due to the pole in z = 1.2, which is outside the unit circle! This is not a problem as long as the feedback path exists, but opening the path results in an exponential growing oscillation at the output of the controller. This could be the situation if the DC-link voltage is too low to generate the required voltage drop across the inductor, i.e. the inverter is saturated.

The parameter B is therefore selected to 1, which corresponds to a normal PI controller. The price for this is that poles no more can be placed at the desired point. The damping is still desired to be 0.707. Thus, the following equality can be stated:

$$0.5 \pm j \cdot b = \exp\left(\omega_n \cdot \frac{(-1 \pm j)}{\sqrt{2}} \cdot T_{sa}\right). \tag{6.51}$$

This corresponds to that $\omega_n \cdot T_{sa} / \sqrt{2} = 0.5397$. For $T_{sa} = 1/10600$, the natural frequency equals 8090 rad/s (1290 Hz), and the pole in the z-domain equals $0.500 \pm j \cdot 0.300$. The proportional gain in (6.48) is then computed to $K_p = 28.5$, and the integrator time constant is evaluated to $T_i = 0.0027$. The system is verified for stability versus parameter variation in the LCL filter in Figure 6.23.

The integrator included in the PI controller is turned off if the output from the controller is becoming too high. This is also known as anti-windup. This is necessary if the commanded output (the sum of the feed forward path and the output from the PI controller) is exceeding the available voltage in the DC-link.

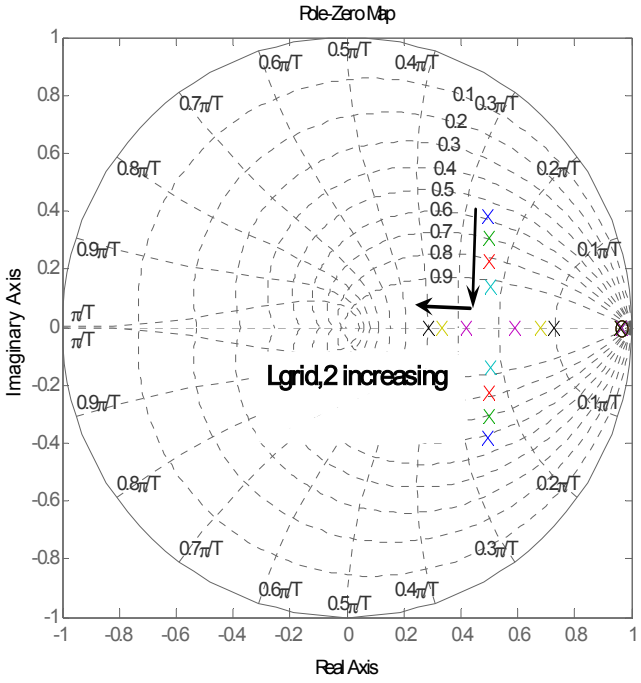

Figure 6.23. Closed loop pole-zero map of the designed controller, when $L_{grid,2}$ changes from 3 mH to 9 mH (expected values when the current decreases, cf. chapter 5). The system is therefore robust to the expected variations in the parameters.

6.5.1 Damping

The model of the damped LCL filter in Figure 6.22 is now used together with the designed controller to evaluate the stability. The s-domain transfer function for the full model of the LCL filter is, c.f. equation (5.4):

$$LCL(s) = \frac{i_{grid}(s)}{u_{inv}(s)}\bigg|_{u_{grid}=0} = \frac{1}{Z_{grid,2} + Z_{grid,1} \cdot \left(1 + \frac{Z_{grid,2}}{Z_0}\right)}, \tag{6.52}$$

$$Z_{grid,1} = s \cdot L_{grid,1} + r_{Lgrid,1},$$

$$Z_{grid,2} = s \cdot L_{grid,2} + r_{Lgrid,2},$$

$$Z_0 = \frac{1}{s \cdot C_{grid}} + R_d,$$

where C_{grid} is the size of the filter capacitor and R_d is the size of the damping resistor. Again, the ZOH approach is used to translate the s-domain transfer function into z-domain. The pole-zero placement of the system is evaluated in Figure 6.24 as a function of the value of the damping resistor. The damping resistor is selected to 33 Ω, which is enough to ensure stability, cf. Figure 6.24.

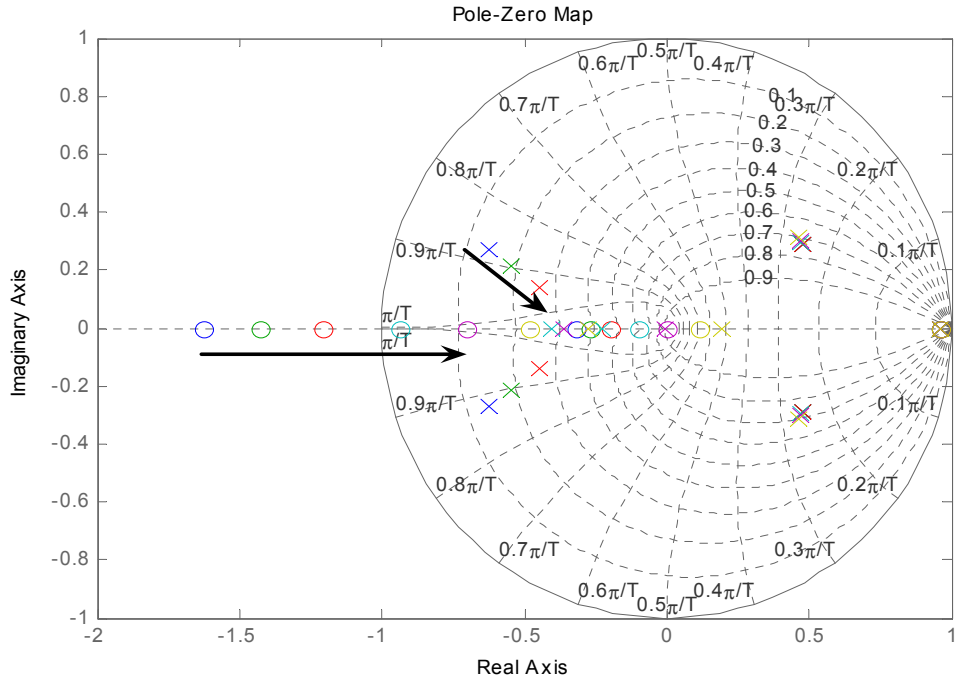

Figure 6.24. Closed loop pole-zero map of the designed controller, when R_d is defined as $R_d \in \{10, 15, 22, 33, 47, 68\}$. A damping resistor of 33 Ω is enough to drag the zero into the unit circle (the RHP zero is moved into the LHP). The corresponding pole location is located in 0.40 with a damping of 0.28.

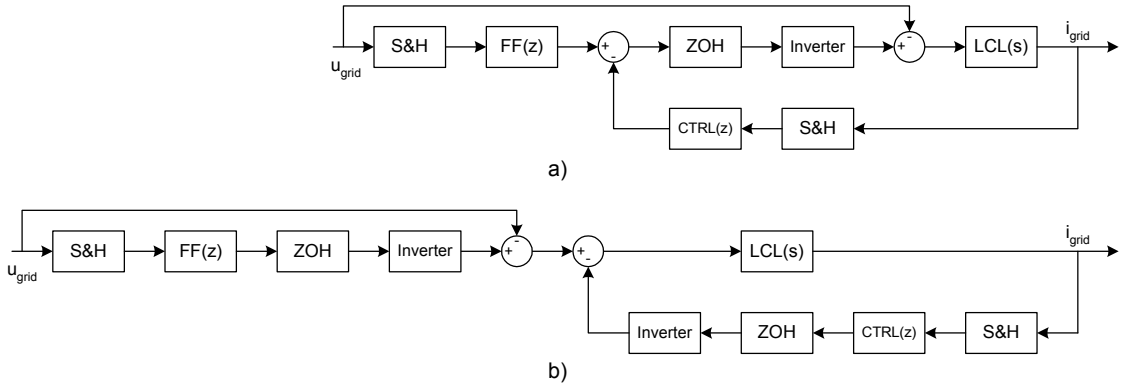

Figure 6.25. The system used to investigate the feed forward action. The unit delay included in the micro-controller is assumed included in the ZOH block. The inverter is assumed to be ideal. A) The diagram before de-coupling of the two loops. B) After the loops are de-coupled. The reference for the grid current, $i_{grid,ref}$, is made equal to zero, for the purpose of the analysis.

6.5.2 Grid Voltage Feed Forward

The system in Figure 6.21 includes a disturbance from the grid voltage, which must be cancelled since the current controller is not fast enough to compensate for the grid voltage. The system investigated is illustrated in Figure 6.25.

The transfer function for the left-most loop in Figure 6.25 must be equal to zero for all frequencies that are multiples of 50 Hz, in order to neutralize the effect from the grid voltage. The Bode plot for the right-most loop in Figure 6.25 is given in Figure 6.26. The Bode plot predicts that the 230 V at 50 Hz in the grid results in a current of approximate 5 A, if not compensated for.

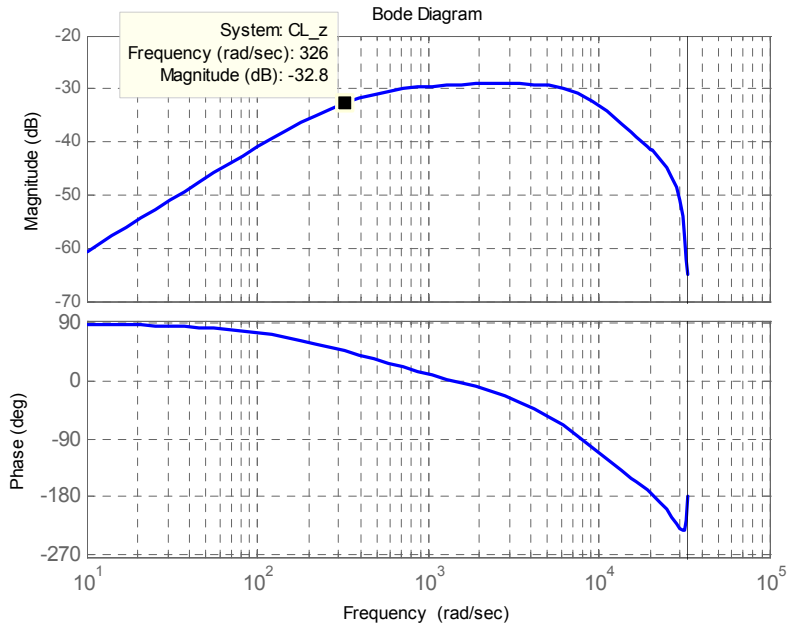

Figure 6.26. Bode plot for the grid-voltage to grid-current loop. A non-compensated grid voltage of 230 V at 50 Hz involves a grid current of approximate 5 A.

Three different types of feed forward are now investigated. The simplest solution is to make the feed forward compensation, FF(z), equal to one. The total feed forward path ($FF(z)\cdot z^{-1}$ -1) then becomes:

$$H_{unity}(z) = FF(z)\cdot z^{-1} - 1 = \frac{1-z}{z} \tag{6.53}$$

Another solution is to make FF(z) equal to a one sample predictor ($Y/X = 2\text{-}z^{-1}$), in order to overcome the one sample delay in the micro-controller:

$$H_{1\_predictor}(z) = FF(z)\cdot z^{-1} - 1 = \frac{2\cdot z - 1 - z^2}{z^2}. \tag{6.54}$$

A third solution is to sample the grid voltage and store the value for 20 ms, and then use it as the feed-forward:

$$H_{2\pi delay} = FF(z)\cdot z^{-1} - 1 = z^{-212} - 1 \tag{6.55}$$

where the 212 sample delay is calculated as 20 ms·10.6 kHz. The Bode plots for all three approaches are depicted in Figure 6.27. The one step predictor is better than the unity feed forward, and the 2π delay is better than the predictor. However, delaying the signal with 212 samples yields a poor feed forward when the frequency in not exactly 50 Hz. The delay-approach is better than the unity-approach, if the grid frequency is within 10.6 kHz / (212 ± 1) = 49.77 Hz to 50.24 Hz.

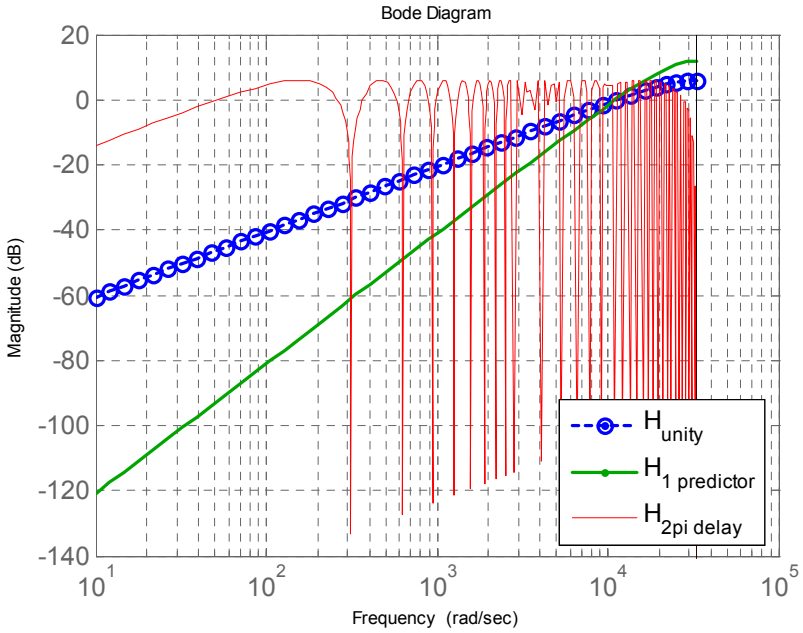

Figure 6.27. Bode plot for unity, one sample predictor, and 2π delay feed forward scheme. The resulting grid-current, at 50 Hz, for the two feed forward schemes are approximated to 0.17 A, 0.01 A, and 0.00 A, respectively.

6.5.3 Blanking Time Compensation

In order to avoid shoot-through in the MOSFETs included in the DC/AC inverter, a blanking time is introduced between the turn-off and the turn-on signals. The blanking time was found in chapter 5 to 0.4 µs. The blanking time changes the output voltage from the inverter, and introduces low order harmonics in the grid current, as seen in Figure 6.29.

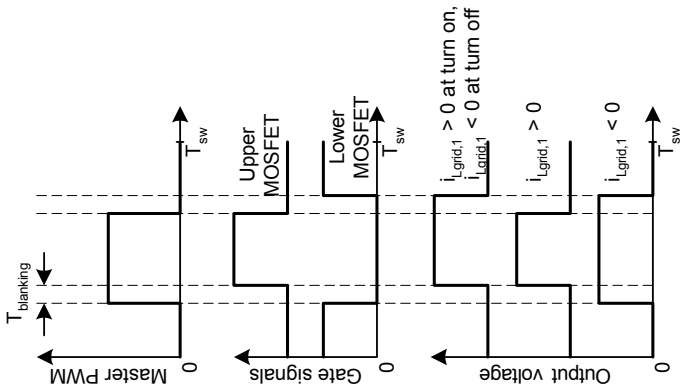

Figure 6.28. Influence of the blanking time on the output voltage.

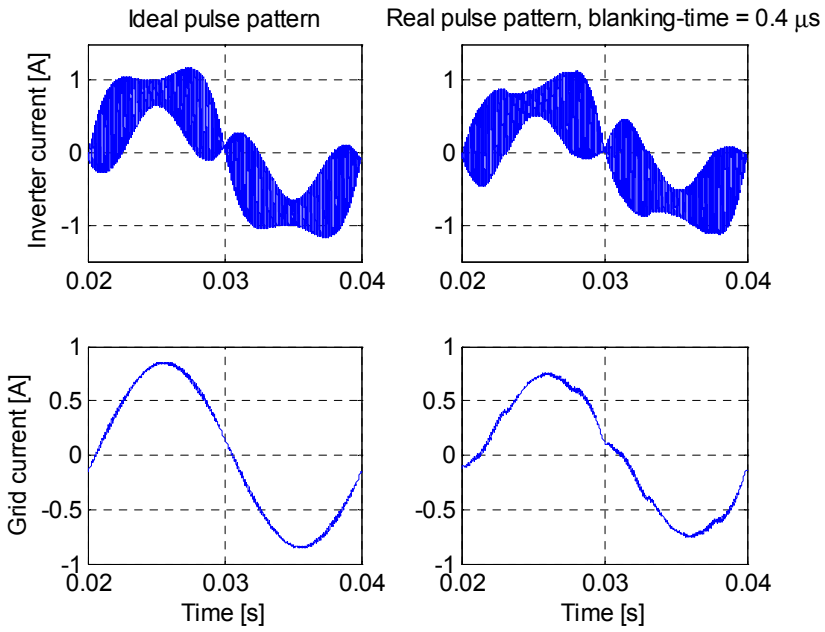

Figure 6.29. Simulated results, comparing the inverter- and grid-currents at ideal and real pulse pattern. The RMS values of the grid currents are 0.60 A and 0.52 A, for the ideal and the real pulse pattern, and the reference is equal to 0.65 A for both pulse patterns. The low frequency (≤ 1050 Hz) THD is evaluated to 1.6% and 6.4% for the ideal and the real pulse pattern.

The influence of the blanking time is dependent of the direction of the current at the time of commutation of the MOSFETs; this is illustrated in Figure 6.28. The average value of the output voltage is decreased when the output current is positive, and increased when the current is negative. However, no blanking time effects are present when the current passes through zero during the switching period [107], since they cancels each other out. The blanking time effect can be compensated in several ways:

- Make $L_{grid,1}$ small enough so that the current always passes through zero during a switching period, even under high power generation. This requires a new design of the LCL filter and the requirements/stress for filter components would be higher. This is not feasible for high power inverters, but perhaps for low power ones.
- Use a P+resonant controller for each harmonic generated by the blanking time effect [106]. This requires a better/faster microcontroller, since it must perform more calculations in every interrupt.
- Decrease the blanking time as much as possible, c.f. Table 6.3, and accept the resulting grid current as being good enough.
- Increase or decrease the commanded duty cycle according to the direction of the current. This requires information about the zero crossing of the current in $L_{grid,1}$, which can be obtained with an analogue circuit or determined inside the micro-controller.

Table 6.3. Comparison of current harmonics versus blanking time, without any compensation. The $\%THD_i$ is computed to 1.6%, 6.4% and 18.7% for the three cases.

Harmonic order	1	3	5	7	9
Current at no blanking time	851 mA	0.8%	0.9%	0.4%	0.4%
Current at 0.4 µs blanking time	732 mA	3.8%	2.6%	3.4%	2.5%
Current at 1.4 µs blanking time	567 mA	9.3%	12.7%	9.5%	3.4%

The blanking time is not compensated for in the developed inverter, but the blanking time is decreased as much as possible to obtain a low distortion of the grid current, c.f. Table 6.3. This is done, since a compensation algorithm requires too much computational time inside the selected microcontroller.

6.6 Implementation Issues

6.6.1 Signal Resolution and Anti Aliasing Filters

The five signals to be converted from analog to digital are given in Table 6.4, together with their range, resolution with a 10-bit AD converter, noise contents and -3 dB bandwidth for the anti-aliasing filter.

The bandwidth for the anti-aliasing filter is specified in the light of the resolution of the ADC and the amplitude of the noise, as:

$$f_{-3dB} = f_{noise} \cdot \sqrt{\frac{k^2}{1-k^2}}, \quad k = \frac{½ \cdot resolution}{A_{noise}}, \tag{6.56}$$

where f_{noise} is the fundamental frequency of the noise, A_{noise} is the amplitude of the noise, and finally, the resolution is computed as the increase in signal per bit in the ADC. This ensures that the amplitude of the noise signal is decreased below half the resolution of the ADC. The effects on the grid -voltage and -current measurements are assumed small; hence they do not have any influence on the design of the controllers.

Table 6.4. Signals to be converted, and required cut-off frequency for the anti-aliasing filters.

Variable	Measuring range	Resolution with 10 bit ADC	HF noise, fundamental amplitude and frequency	Anti aliasing filter Bandwidth
DC-link voltage	0 V to 450 V	0.44 V	0.65 V at 21.2 kHz	7.6 kHz
Grid voltage	-375 V to +375 V	0.73 V	0.05 V at 21.2 kHz	None (5.7 kHz)
Grid current	-2 A to 2 A	3.9 mA	7.5 mA at 21.2 kHz	5.7 kHz
PV voltage	0 V to 50 V	0.05 V	0.50 V at 220 kHz	22 kHz
PV current	0 A to 8 A	7.8 mA	70 mA at 220 kHz	12 kHz

6.6.2 Discrete Time Implementation of Controllers

The dynamics for the PI controllers and the integrator included in the PLL and the DC-link controllers are much lower than the sampling time. It is therefore sufficient to translate them into discrete time by using emulation [93]. The difference-equation for the PI controller is equal to (when using backward Euler):

$$\begin{aligned} Y[n] &= \frac{Ts}{Ti} \cdot e[n] + Y[n-1], \\ PI[n] &= Kp \cdot (e[n] + Y[n]), \end{aligned} \tag{6.57}$$

where e[n] is the n^{th} error into the controller, and Y[n] is the n^{th} output from the integrator. The difference-equation for the integrator is:

$$Y[n] = Ts \cdot X[n] + Y[n-1], \tag{6.58}$$

where X[n] is the n^{th} input into the integrator, and Y[n] is the n^{th} output from the integrator.

Two tables, each with 5 ms × 10.6 kHz +1 = 54 places, are defined to store the values of the sampled grid voltage and the calculated fundamental sine, in order to calculate the corresponding cosine values. The sine-function in Figure 6.6 is implemented by using a lookup-table, which it is much faster than using the sin-function in the C math-library.

6.7 Evaluation of the Controllers

This chapter deals with the design of the controllers included in the inverter. This includes:

- Optimizing the load of the PV module in order to capture the highest amount of energy, despite that the solar irradiation and cell temperature never is constant. Four types of Maximum Power Point Trackers (MPPT) have been discussed and a novel MPPT algorithm has been developed, to overcome some of the shortages with the present algorithms.

- Tracking of the fundamental grid voltage, by means of a Phase Locked Loop (PLL), in order to synchronize the inverter to the grid, and to generate a high quality waveform-reference for the grid current.
- Detection of islanding operation by means of voltage and frequency monitoring. The frequency deviation is obtained from the PLL and the grid voltage is monitored by its RMS value.
- Control of the DC-link voltage, in order to keep it within reasonable bound. This also includes a variable reference as function of grid voltage and power. The possibility to add a feed forward of the generated power by the PV module was briefly discussed, in order to enhance the dynamics of the controller.
- Control of the grid current in order to inject a sinusoidal current, with low harmonics, into the grid. This controller is designed by the discrete design methodology because the bandwidth of the system is high compared with the sample/switching frequency. The stability is evaluated for different values of the damping resistance in the grid-connected LCL filter, whereas the design of the controller is based on an LR filter equivalent.
- Some additional parts to enhance the quality of the grid current (feed forward control of the grid voltage and blanking time compensation).

All the controllers have been designed by standard design techniques, and verified by simulation in MATLAB® / SIMULINK® and PSIM®.

Chapter 7

Testing the Inverter

The purpose of this chapter is to validate the designed inverter in respect to the specifications in chapter 3, and hereby the design in chapter 5 and 6. A summary of the obtained results and the specifications are revised in Table 7.1. A photograph of the prototype is shown in Figure 7.1, and a schematic representation of the main circuit in Figure 7.2.

DC-DC converter connected to the PV module.

Microcontroller, connected to a host PC.

DC-AC inverter connected to the grid (two PCB').

Internal switch mode power supply (with battery back-up).

Figure 7.1. Picture of the second prototype realized in the laboratory at IET-AAU.

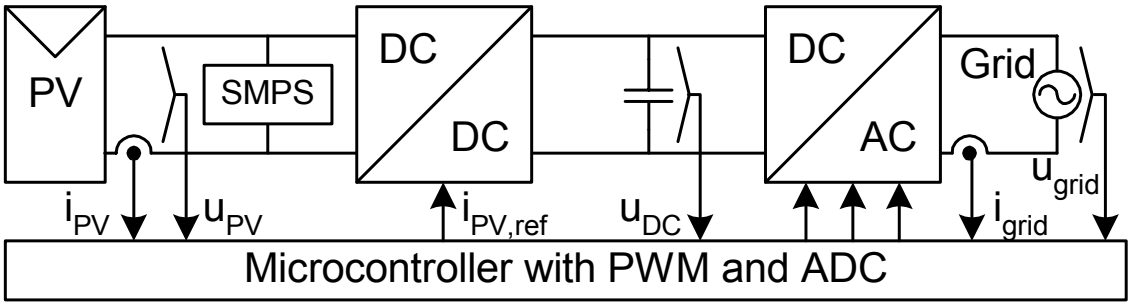

Figure 7.2. Block diagram of the inverter. SMPS = Switch Mode Power Supply, PWM = Pulse Width Modulator, ADC = Analog-to-Digital Converter.

7.1.1 Review of Specifications

Table 7.1 serves to compare the specified and obtained values.

Table 7.1. Review of some of the specifications given in chapter 3, and obtained values. TBD = To Be Determined.

Interfaces and Parameters		Specified value	Obtained value	Observed?
PV	Nominal PV module power	160 W	Min. 150 W	(Yes)
	Maximal open circuit voltage	50 V	Min. 42 V	(Yes)
	Maximum power point range	23 V to 38 V	20 V to 38 V	Yes
	Ripple at nominal power (LF amplitude, and HF peak-peak)	4.1 V / 0.5 V	0.06 V / 0.7 V	Yes / No
	Maximum short circuit current	8 A	Min. 6.4 A	(Yes)
	MPP current range	0 - 7.2 A	Saturates at 5 A	No
Grid	Nominal grid voltage	230 V ± 10%	230 V ± 10%	Yes
	Nominal grid frequency	49.5 Hz to 50.5 Hz	Not tested for.	TBD
	Non islanding operating range, voltage	195 V to 253 V	197 V to 255 V	Yes
	Non islanding operating range, frequency	48 Hz to 52 Hz	Not tested for.	TBD
	Standby losses	-	0.5 W	-
	Current harmonics	EN61000-3-2-A	-	Yes
		82/308/CDV	-	No
	Power factor at 50% of nominal power	0.95	0.98	Yes
	Inrush current and voltage	< 13 A, < 450 V	0.5 A / 350 V	Yes

7.1.2 Realized Prototype

The realized prototype includes a Switch Mode Power Supply (SMPS) to supply power to the internal sub-circuits. The PV module energizes the SMPS, in order to minimize the standby consumption from the grid. A battery back-up circuit is included to provide power to the circuits in case of PV voltage collapse. The SMPS is based on a flyback converter, with seven outputs and a MAX5020 dedicated controller [108]. The input power to the SMPS is about 9 W at 28 V, and the efficiency is measured to approximately 70%. The prototype also includes five measuring and conditioning circuits to make suitable inputs to the microcontroller, and some protection circuits.

The realized prototype differs in some points from the designed one. The changes are given in Table 7.2. The largest differences are the diodes included in the rectifier in the DC-DC converter, and the switching frequency. The diodes were original designed to withstand 2 kV, but the diodes in the prototype can only withstand 1.2 kV. A software protection is therefore included in the microcontroller, which turns the inverter off if the PV voltage exceeds 38 V during operation. The switching frequency of the DC-AC inverter part has been decreased to 8 kHz, in order to have enough time to perform all control loops (MPPT, DC-link voltage, grid current, etc.) in the interrupt service routine. The parameters in the grid current controller are therefore re-calculated and the performance of the controller will be affected in a negative way, since the bandwidth of the system is comparable with the updating frequency.

Table 7.2. Realized values within the prototype.

Issue	Designed value	Realized value
Transformer turns ratio	18.0	17.7
DC-link inductor core	Kool Mμ 77310-7 core (11 mH)	3F3 ETD29 core (9.4 mH)
DC-link electrolytic capacitor	33 μF	47 μF
Input capacitor	15 μF film	100 μF electrolytic and 100 nF film
Grid capacitor	680 nF	1.2 μF
Inverter connected inductor, $L_{grid,1}$	EFD25 (3.7 mH)	ETD29 (6.5 mH)
Grid connected inductor, $L_{grid,2}$	Kool Mμ 77935-7 core (4.2 mH)	Kool Mμ 77211-7 core (1.4 mH)
LCL filter resonance frequency	4.35 kHz	4.28 kHz
Rectifier diodes, and break down voltage	RPG02-20E, 2000 V	DSEI12-12A, 1200 V Snubber: 120Ω + 110pF
Switching frequency	10.6 kHz	8.0 kHz
Blanking time	0.4 μs	0.6 μs (1.4 μs)
Current reference waveform generator	PLL	Sampled grid voltage

7.1.3 Layout of Measurements

The measurements on the realized prototype are made both at the Danish Technological Institute (DTI) [109], an independent test-house, and at Aalborg University (AAU).

The layout of the test-bed is illustrated in Figure 7.3. The inverter is tested with a 72 cells 170-Watt BP5170 PV module at DTI and a 50 cells SOLEL PV module at AAU. Some of the measurements, made at DTI, are performed with a PV module emulator, and at AAU, with the SOLEL PV module shadowed and connected in parallel with a current controlled DC power supply. This is done to obtain the same operating conditions, or when solar irradiation was too low to operate the inverter.

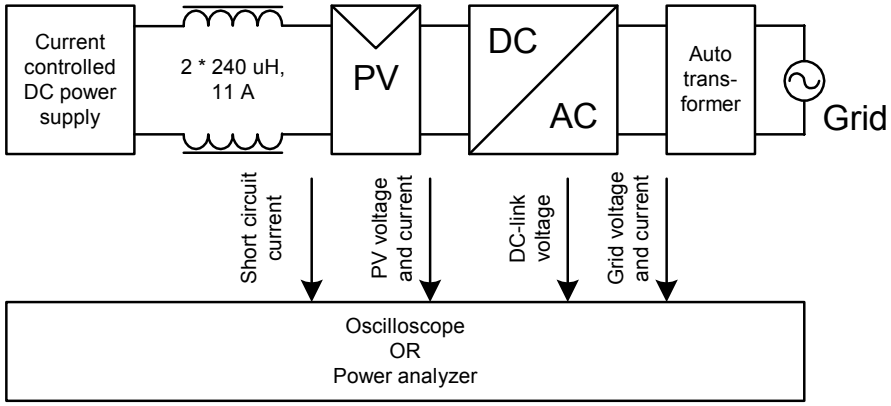

Figure 7.3. General setup for the measurements. The current controlled DC power supply is used to generate/simulate the short-circuit current for the shadowed PV module (AAU), or module emulator (DTI), when the available amount of sunlight is too low. The autotransformer is used to adjust the grid voltage during measurements.

A galvanic isolated autotransformer is inserted between the grid and the inverter, in order to adjust the grid voltage during operation, and to protect the prototype. The impedance seen by the inverter is therefore higher compared to the case where the transformer is omitted, and the resonant frequency of the designed LCL filter is not equal to the designed value, but lower. The performance of the grid current controller is therefore also altered.

The results presented in the following sections are marked with the origin of the measurement (DTI, AAU), and type of measuring device: OSC: Screen/memory dump from the oscilloscope, MC: memory dump from the microcontroller, PM: PM100 power analyzer, DL: data-loggers, and CT: PV curve tracer.

7.2 Test of Grid Interface

The purpose of this section is to validate the interface between the inverter and the grid. This includes both steady state and dynamic measurements of the grid current.

7.2.1 Grid Current Versus Blanking Time

The purpose of this test is to shown the performance of the grid current controller versus the blanking time. Two different blanking times are investigated, first 1.4 μs (which was an initial value) and later 0.6 μs, which is the final value. The results are depicted in Figure 7.4 to Figure 7.7. The results are summarized in Table 7.3. The THD computed in chapter 6 is 18.7% and 6.4% for blanking times of 1.4 μs and 0.4 μs, respectively, and with a sinusoidal waveform reference. The obtained THD for the 1.4 μs blanking time, 18.1%, is close to the simulated one. But the obtained THD for the 0.6 μs blanking time, 17.8%, is far away from the simulated one. On the other hand, results in [86] which applied the same control structure for a 1 kW fuel cell inverter shows a THD of 37% at 100 W, 19% at 200 W, and 7.3% at 840 W. So compared to these results, the obtained results are satisfactory, and within the obtainable range.

Comparing the memory dumps from the microcontroller shows that the total and the fundamental RMS value of the error into the PI controller are lowest for the 0.6 μs blanking time.

Table 7.3. Comparison of 1.4 μs and 0.6 μs blanking time (AAU, PM/MC).

Blanking time	1.4 μs		0.6 μs	
Measuring devise:	PM100	Microcontroller	PM100	Microcontroller
PV short circuit current	4.60 A	-	4.60 A	-
PV current	4.22 A	-	3.50 A	-
PV voltage	23.9 V	-	27.6 V	-
PV power	100.8 W	-	96.6 W	-
Grid voltage	234 V	233 V	232 V	233 V
Grid current	0.34 A	0.35 A	0.34 A	0.34 A
RMS value of error into the controller	-	0.087 A	-	0.062 A
RMS value of fundamental component into the controller	-	0.075 A	-	0.046 A
Grid power	79.2 W	81.5 W	77.7 W	78.6 W
Grid apparent power	80.0 VA	82.6 VA	78.1 VA	79.2 VA
Power factor	0.990	0.987	0.995	0.992
Grid voltage THD	1.7%	5.5%	2.1%	4.7%
Grid current THD	18.1%	14.2%	17.8%	13.9%

7.2.2 Grid Current Performance

The Total Harmonic Distortion (THD) and Power Factor (PF) are measured to see whether the EN61000-3-2 standard [3], the DEFU recommendation [37], and the CEN requirements [38] are fulfilled. However, the EN61000-3-2 standard does not specify the THD, but specifies the individual components. They are therefore also measured. The THD and PF for three different grid voltages are given in Table 7.4. The amplitude of the harmonic currents for app. 60% generation is depicted in Figure 7.8 and for app. 40% power in Figure 7.9.

Table 7.4. Measured %THD_i and PF versus grid power and voltage (AAU, PM).

U_{grid}	P_{grid}	THD_I	PF
207 V	101 W	11.7%	0.992
230 V	117 W	17.5%	0.988
248 V	109 W	15.3%	0.990

Based on the measurement, it is concluded that the inverter is fulfilling the requirements given by the Danish Utilities. The power factor is better than 0.95 at 50% generation. But the inverter does not fulfill the limits of the CEN 82/308/CDV requirements. This is however not a problem since the CEN standard still is a draft.

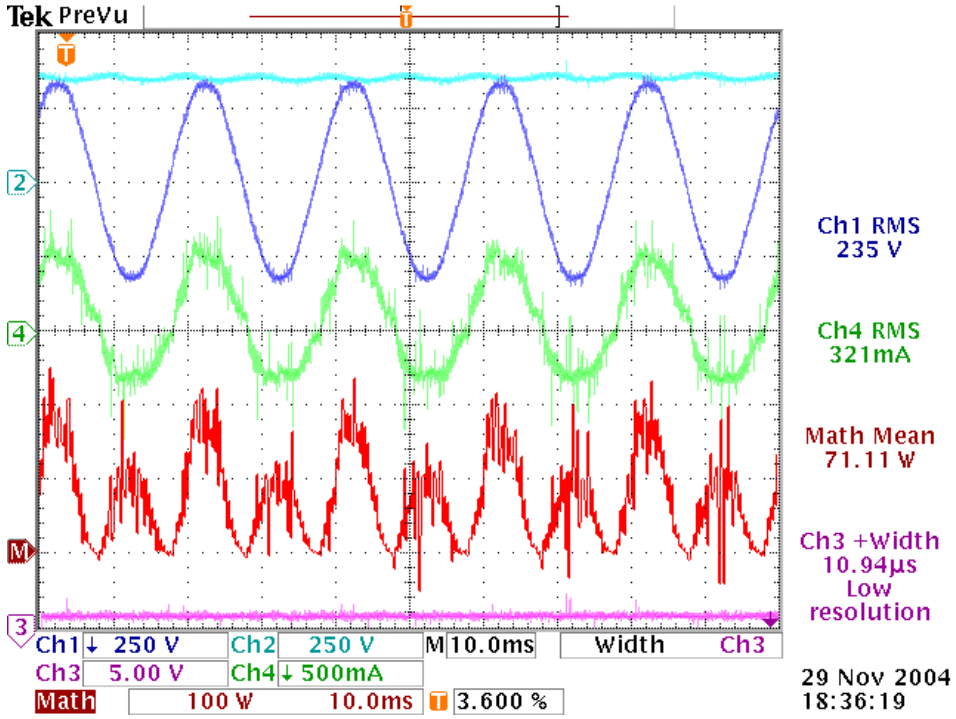

Figure 7.4. Measured results with 1.4 µs blanking time, screen dump from oscilloscope (AAU, OSC). Ch1 is grid voltage, Ch2 is DC-link voltage, Ch3 is the trig signal from the microcontroller, Ch4 is the grid current, and finally, Math is the grid power.

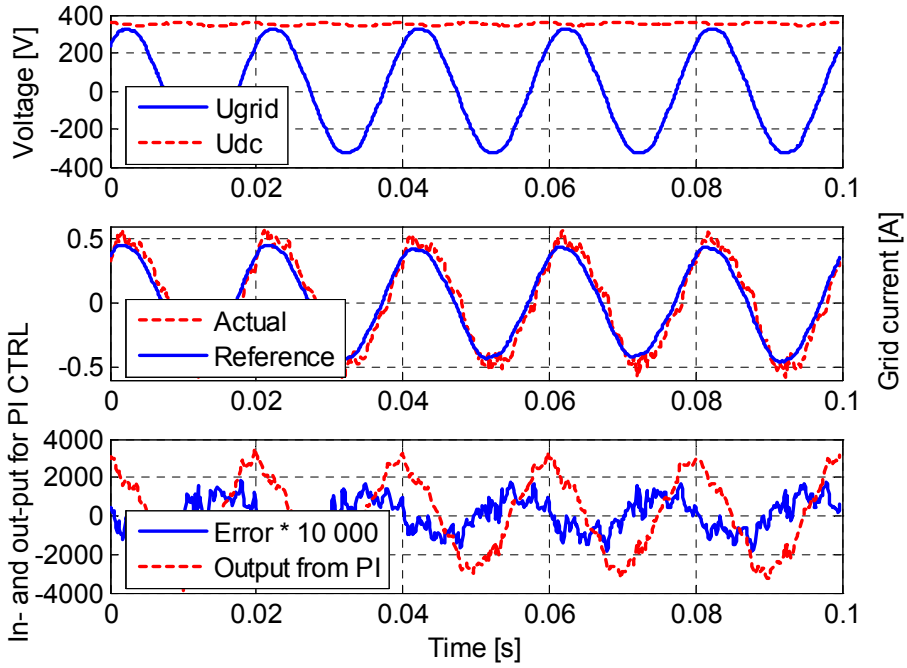

Figure 7.5. Measured results with 1.4 µs blanking time, memory dump from microcontroller (AAU, MC).

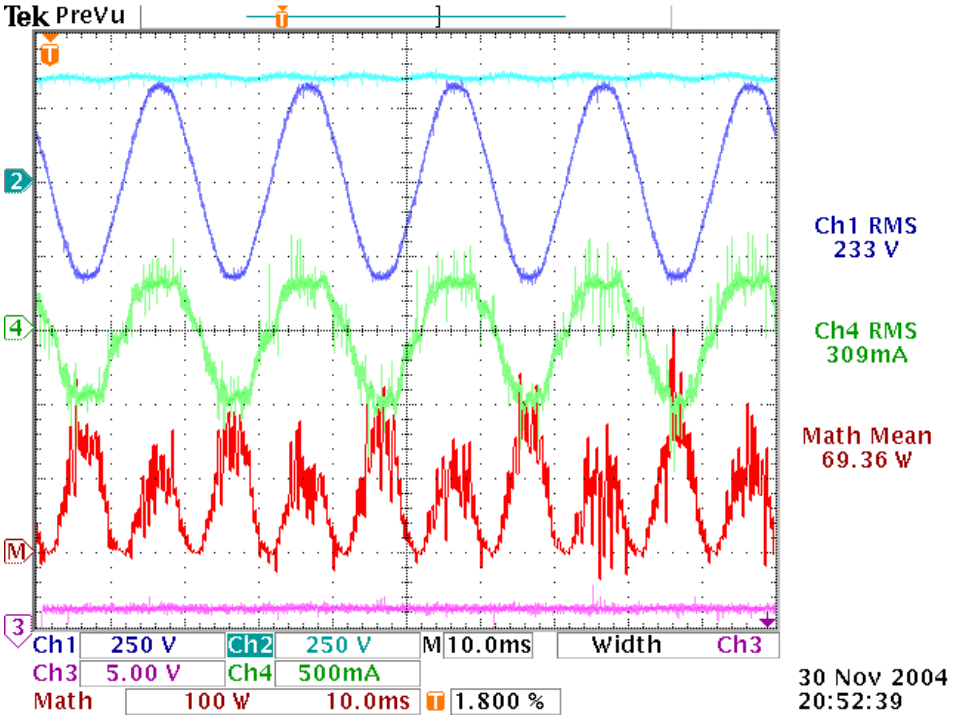

Figure 7.6. Measured results with 0.6 µs blanking time, screen dump from oscilloscope (AAU, OSC). Ch1 is grid voltage, Ch2 is DC-link voltage, Ch3 is the trig signal from the microcontroller, Ch4 is the grid current, and finally, Math is the grid power.

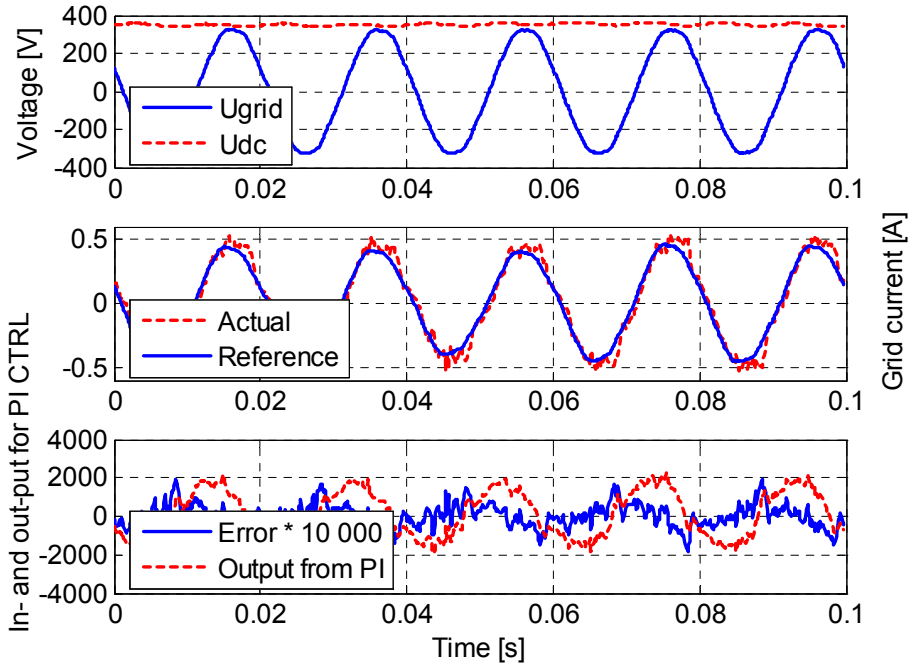

Figure 7.7. Measured results with 0.6 µs blanking time, memory dump from microcontroller (AAU, MC).

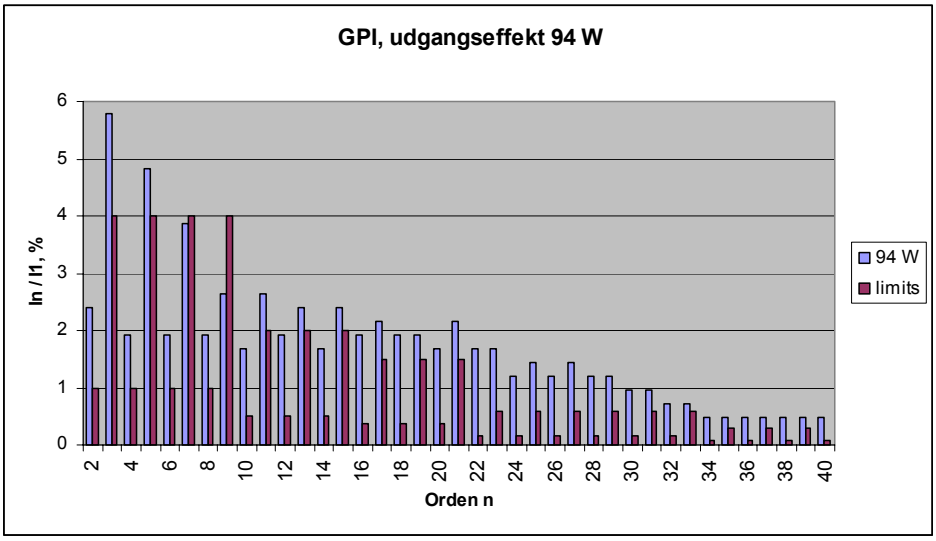

Figure 7.8. Measured amplitude of the harmonic components at 1.4 µs blanking time, and their limits according to [38] (DTI, DL).

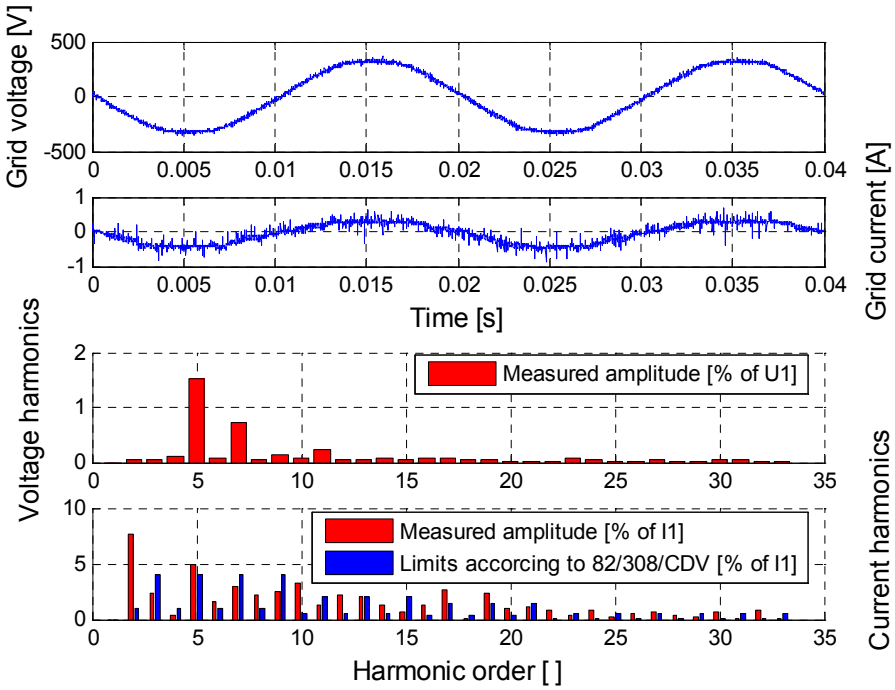

Figure 7.9. Measured amplitude of the harmonic components at 0.6 µs blanking time, and their limits according to [38] (AAU, OSC). Grid power is equal to 62.3 W with a power factor of 0.959 and a current THD of 12.4%.

7.2.3 Inrush Sequence

The purpose of testing the inrush sequence is to see if the grid current and the DC-link voltage increase beyond harmful values during inrush. The DC-link capacitor is rated to 450 V and the MOSFET' in the inverter can withstand a peak current of 13 A, and these values must not be exceeded. The measured grid current and voltage, and DC-link voltage are depicted in Figure 7.10, during an inrush sequence. As seen, both the current and voltage is kept below the limits, thus the inrush-circuit is capable of protecting the inverter.

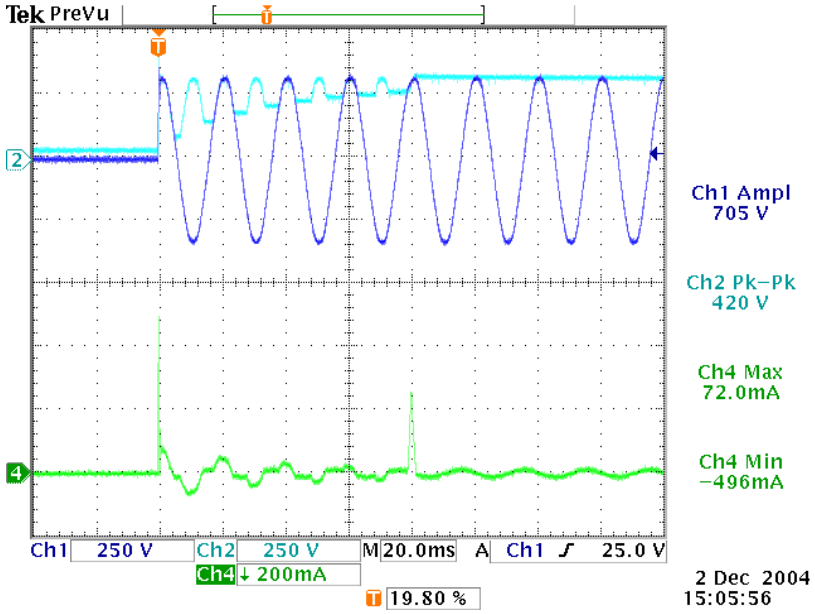

Figure 7.10. Measured results for the inrush (AAU, OSC). Oscilloscope screen dump with: Ch1: u_{grid}, Ch2: u_{DC}, and Ch4: i_{grid}. The peak value of the grid voltage, at turn on, is about 350 V, which results in an inrush current of about 0.5 A. The inrush circuit is bypassed at time 80 ms after the voltage is applied.

7.2.4 Step and Ramp in PV Power

The aim of this test is to evaluate the designed DC-link controller. The DC-link voltage must not exceed 430 V during a power ramp of 200 W/s, and it must not collapse (decrease to the value of the instantaneous grid voltage) during a power step of -40 W at nominal conditions, cf. chapter 6.

The results from the test are shown in Figure 7.11 and Figure 7.12. The maximum voltage, in Figure 7.11, equals 380 V at a power ramp of 135 W / 1.8 s = 75 W/s, recorded at a DC-link voltage reference of 360 V, and a 100 Hz ripple with amplitude 12 V. The additional voltage in the DC-link caused by the ramp is computed to 380 V – (360 V + 12 V) = 8 V. Since the additional voltage is proportional with the slope of the ramp, cf. chapter 6, the maximum additional voltage is computed to 30 V at a slope of 200 W/s and with a DC-link capacitance of 33 µF. The maximum voltage in the DC-link is therefore computed to: 380 V + 20 V + 30 V = 430 V (average value + amplitude of 100 Hz ripple + additional voltage caused by the ramp), with a capacitor of 33 µF, a RMS value of 253 V for the grid voltage, and 150 W into the DC-link. This is also the designed value. The voltage in the DC-link, in Figure 7.12, is seen to collapse to the peak-value of the grid voltage (328 V) when the PV current is stepped from 5.16 A to 3.48 A (approximately from 135 W to 91 W). However, the voltage is restored within 120 ms, and operation is continued. The designed controller is therefore regarded as to fulfill the demands.

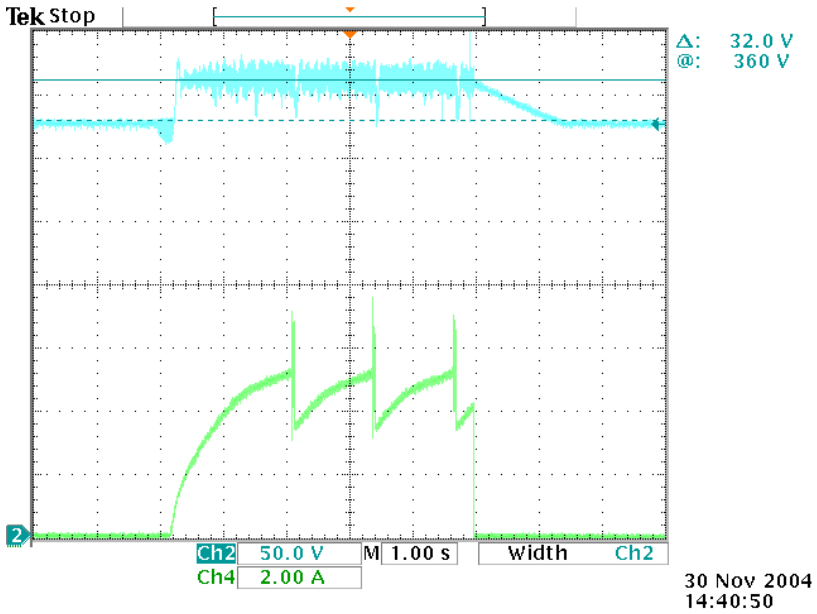

Figure 7.11. Measured results of DC-link voltage versus ramps and steps in PV current (AAU, OSC). The maximum PV power is equal to 135 W, corresponds to a PV current of 5.12 A at 26.4 V.

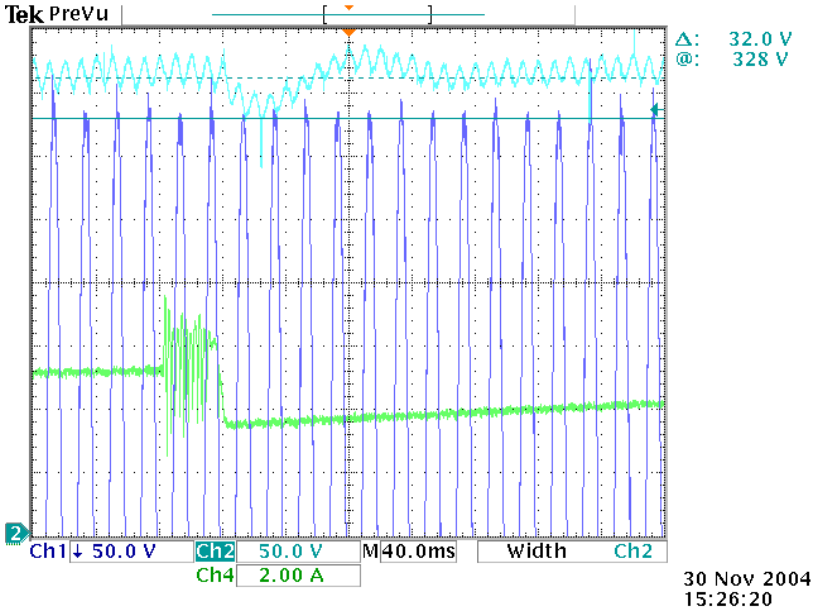

Figure 7.12. Measured results of DC-link voltage at a step in PV current, from 5.16 A to 3.48 A (AAU, OSC). Ch1: positive part of the grid voltage, Ch2: DC-link voltage, Ch4: PV current.

7.2.5 Islanding Detection

The evaluation of the islanding detection is performed at DTI. The rms value of the grid voltage is computed and sampled every 20 ms, over 200 seconds. The computed value is in Figure 7.13 compared with the current drawn from the PV module. The specifications for non-islanding operation are given in the span from 195 V to 253 V. The microcontroller detects the islanding operation mode when the voltage is outside the range from 197 V to 255 V, which is very close to the specifications, and seems to be small bias of 2 V somewhere in the hard- or soft-ware. The voltage detection-algorithm is therefore regarded as fulfilling the specifications. The frequency detection-algorithm is not tested.

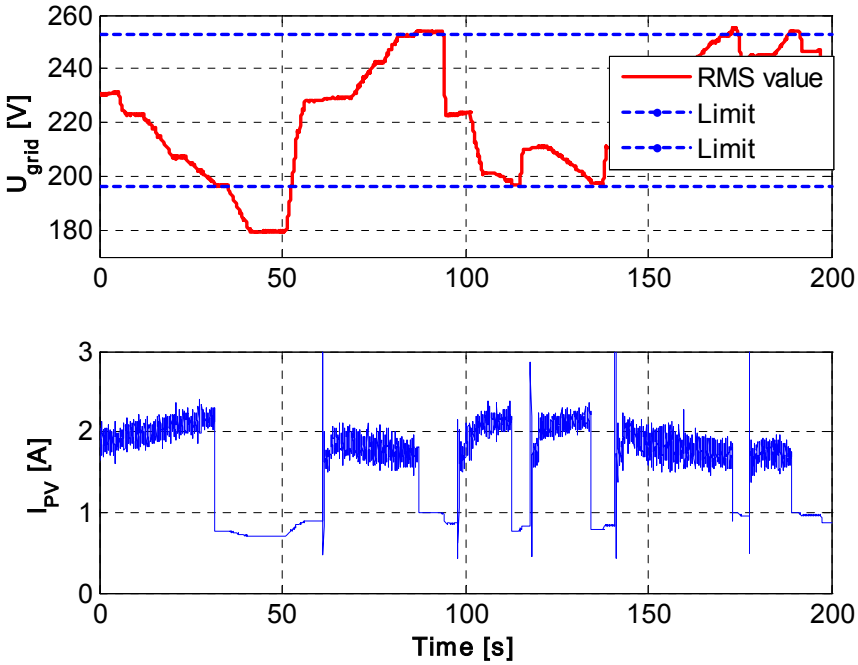

Figure 7.13. Detection of islanding operation (DTI, DL). The RMS value of the grid voltage is shown in the upper plot, and the current drawn from the PV module in the lower plot (computed every 20 ms). The current drawn from the PV module decreases to 0.7 A (for internal supply), when the grid voltage exceeds the limits.

7.2.6 Steady State Results

The purpose of this section is to compare the measured values with the simulated values in chapter 5. The results presented in Table 7.5, show that the power factor is better than 0.98 at 50% power. The European efficiency, see equation (1.1) for a definition, for the DC/AC inverter alone (without DC/DC converter) is estimated to 93.3%. This is a small value, which is influenced by the measuring accuracy, especially in the very low power area. A better accuracy can be achieved by using a calorimeter test-bed.

The energy consumed by the inverter in standby is measured and averaged, by a PM100 power analyzer, to about 0.5 W. This is a low value, which is regarded as being good.

Table 7.5. Measured results for the DC/AC inverter (AAU, PM).

Operating point	5%	10%	20%	30%	50%	100%
Corresponding PV power [W]	6.4	13.5	26.7	39.4	65.5	130.2
Input power to the DC-link [W]	2.5	9.8	20.4	33.2	53.0	114
DC-link voltage [V]	349	350	348	349	352	351
Grid voltage, RMS [V]	232	232	232	233	233	234
Grid current, RMS [mA]	40	50	90	140	220	470
Grid power, Mean [W]	1.4	8.5	18.9	31.3	50.6	109
Total Harmonic Distortion (THD_i) [%]	> 100	96.3	49.0	30.2	17.9	13.5
Power Factor (PF) [ ]	0.152	0.729	0.904	0.961	0.987	0.994
DC-AC inverter efficiency [%]	56.0	86.7	92.6	94.3	95.5	95.6

7.3 Test of Photovoltaic Module Interface

The purpose of this section is to validate the interface between the inverter and the PV module. This includes steady state and dynamic measurements of the PV voltage and current.

7.3.1 Maximum Power Point Tracker

The dynamic performance of the MPPT algorithm is tested, in order to see how it performs during rapidly changes in the weather situation. The results of a long-term test with a BP5170 module are shown in Figure 7.14 and Figure 7.15. The results in Figure 7.14 shows a maximum rate-of-change-of-irradiance of -180 W/(m^2·s) at times 200 s and 527 s. This causes the inverter to stop by Under Voltage Lock Out (UVLO) protection; because the PV voltage decreases below 16 V. Operation is resumed after 60 seconds by a manual start command, at low irradiation (a real inverter should of course start automatically when the voltage has been restored). As seen in Figure 7.15, the proposed MPPT fails to track the MPP in some of the time. On the other hand, the MPP is tracked with a high accuracy from time zero to 200 s, from 460 s to 530 s, from 650 s to 1130 s (except of a very fast transient at time 1080 s), and again from 1620 s to 1970 s. Thus, the fail to track the MPP is believed to be a 'teething trouble' and can easily be solved.

The dynamic efficiency of the proposed MPPT algorithm is estimated to 122.4 kJ / 143.4 kJ = 85.3% in Figure 7.15. The efficiency is computed as E_{PV} / E_{MPP}, where E_{PV} is the energy captured from the module and E_{MPP} is the theoretical MPP energy. The theoretical value is calculated on the basis of the BP5170 data-sheet, recorded irradiance and an ambient temperature, T_{abm}, of 16 °C:

$$T_{cell} = T_{abm} + R_{\theta,JA} \cdot (P_{sun} - P_{PV}), \tag{7.1}$$

where $R_{\theta,JA}$ is the thermal resistance for the module, estimated to 0.034 K/W. The data for the BP5170 module are, at Standard Test Conditions (STC), cf. chapter 2: short-circuit current, I_{sun} = 5.00 A, short-circuit current temperature-coefficient, k_{temp} = 0.0033 A/K, reserve saturation current, $i_{rs,STC}$ = 894 nA, and diode quality factor, A = 1.537.

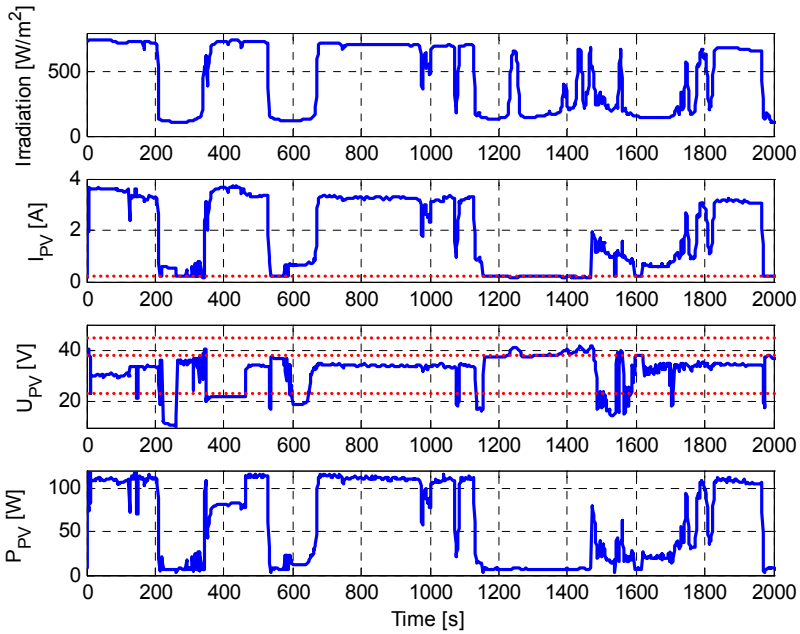

Figure 7.14. Dynamic test of the MPPT (DTI, DL). From top and down: 1) Solar irradiation, 2) Current drawn from the PV module, 3) Voltage across the PV module and specifications for MPP range and maximum open circuit voltage, 4) Generated power. Note the idle current of 0.2 A, when the inverter is stopped, which is used by the internal SMPS.

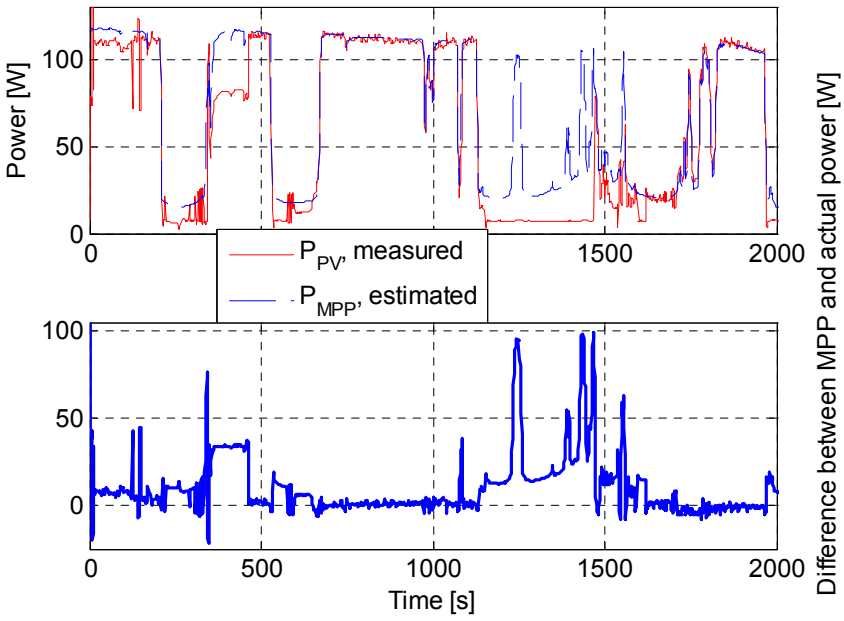

Figure 7.15. Measured results for the MPPT (DTI, DL). The MPPT efficiency is estimated to 85.3% and the efficiency of the PV module (BP 5170) is estimated to 15.6%.

The results of three short-term tests, with the shadowed SOLEL module, are shown in Figure 7.17 to Figure 7.19. The available MPP power versus applied short-circuit current for the SOLEL module is plotted in Figure 7.16, when the setup in Figure 7.3 is applied. The measured result in Figure 7.17 is in agreement with the simulated results in Figure 6.4 and the efficiency is estimated to 98.1% (from Figure 7.16). The response of the MPPT algorithm is also tested with a 0.8 Hz signal in Figure 7.18. Once again, the MPPT shows fine properties in terms of tracking accuracy (note that the efficiency is estimated to 100.5%, which of course is not possible). Finally, a start and stop situation is shown in Figure 7.19. The inverter is started at time 1.3 s and the MPP is located after 2 seconds, which is fast.

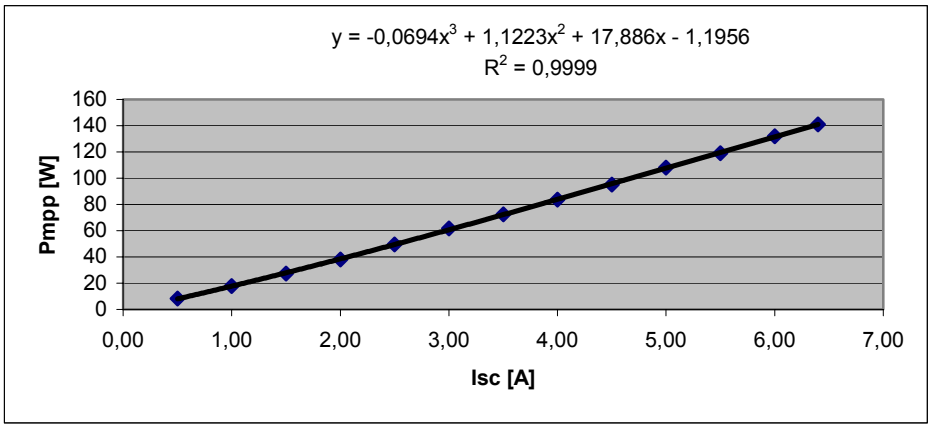

Figure 7.16. Measured MPP power versus short circuit current for the SOLEL module (AAU, OSC).

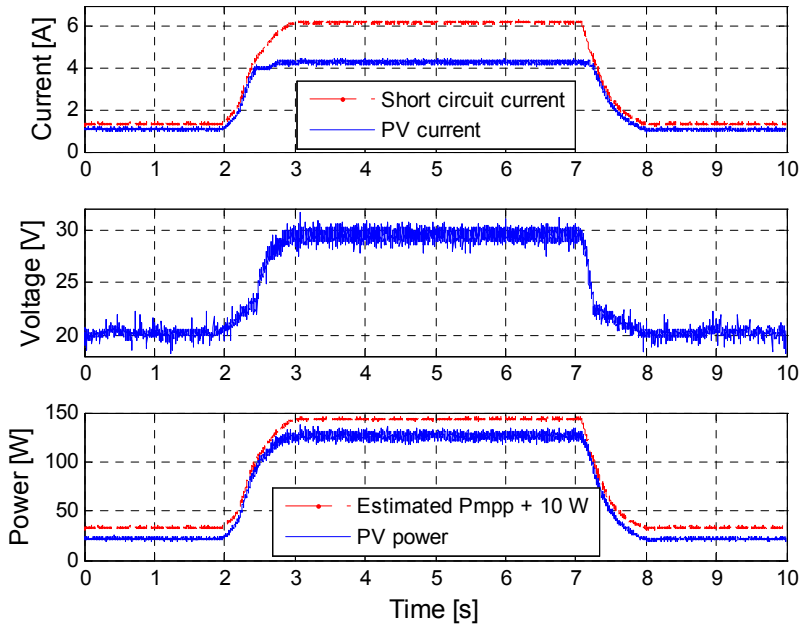

Figure 7.17. Measured results for the proposed MPPT algorithm (AAU, OSC). The efficiency is estimated to 98.1%. The measured results are comparable with the simulated results in Figure 6.5. Note that the estimated MPP power is biased with 10 W in order to separate the curves.

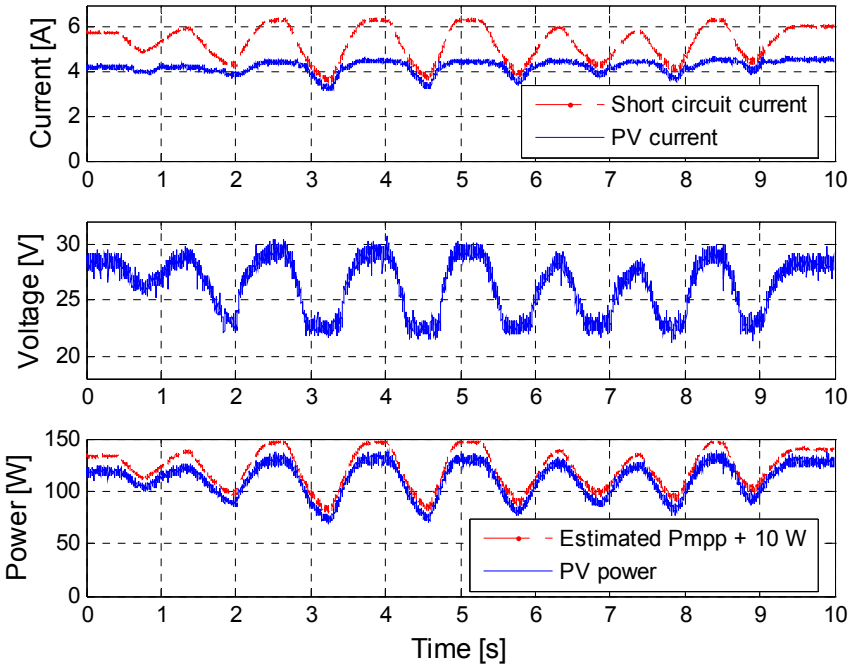

Figure 7.18. Measured results for the proposed MPPT algorithm during rapid changes in irradiation (AAU, OSC). The efficiency is estimated to 100.5%! Note that the estimated MPP power is biased with 10 W in order to separate the curves.

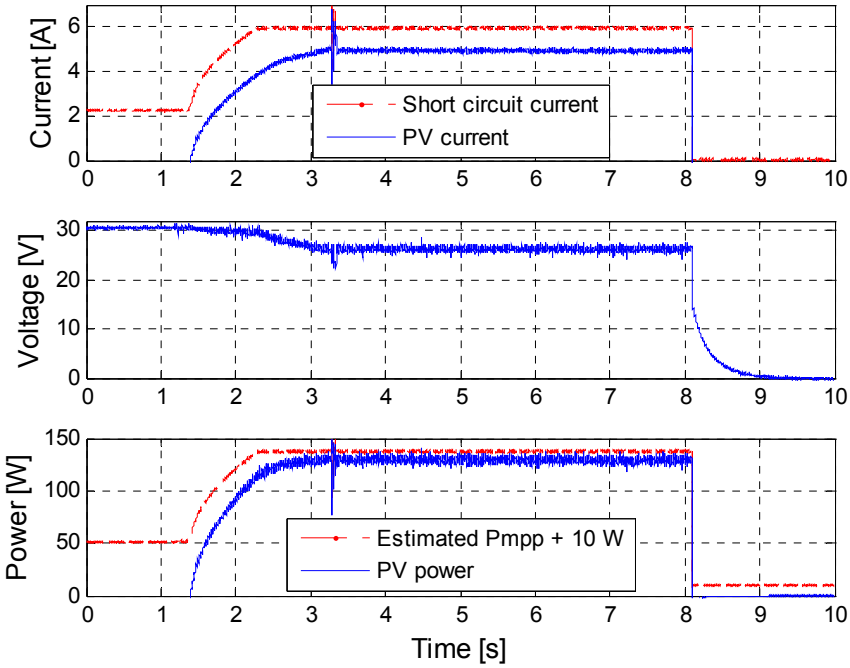

Figure 7.19. Measured results for the proposed MPPT algorithm, during start up and abrupt disconnection of the PV module (AAU, OSC). The efficiency is estimated to 99.4, evaluated over time = 1.36 s to 8.09 s. Note that the estimated MPP power is biased with 10 W in order to separate the curves.

The steady state MPPT efficiency is measured by means of a PV emulator. The emulator is made up around a series connection of 43 diodes (BYW29E-150), which again are connected in parallel with a current source. The voltage-power characteristic for the emulator is measured with a curve-tracer for six different short circuit currents, c.f. Figure 7.20. The characteristic for each level of short-circuit current is measured immediate after the inverter has been operated with the emulator. The temperature of the diodes is therefore assumed constant, which is important since their characteristic is a function of temperature. The steady state efficiency at six different operating points is given in Table 7.6. The steady state efficiency is measured to approximately 99%.

Table 7.6. Measured MPPT efficiencies (DTI, DL/CT). The MPP power is found by curve-tracing the PV emulator, cf. Figure 7.20.

MPP power [W]	23.1	35.2	47.2	59.3	101.5	143.3
Actual P_{PV} [W]	22.9	34.9	46.7	58.2	100.7	142.3
Efficiency [%]	99.1%	99.1%	98.9%	98.1%	99.2%	99.3%

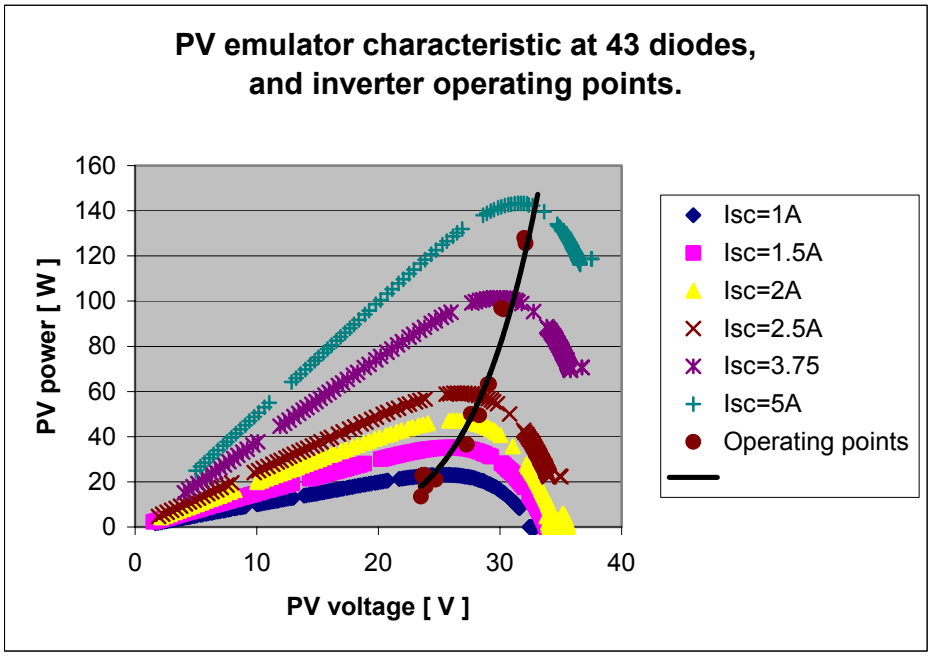

Figure 7.20. Measured characteristic for 43 diode PV emulator, together with 17 inverter operating points (DTI, CT). The operating points are very close to the real MPP.

7.3.2 Audio Susceptibility

The purpose of this test is to see whether the low-frequency voltage ripple at the terminals of the module fulfills the requirements. The LF amplitude is allowed to reach 4.1 V at full generation. The amplitudes of the PV current, PV voltage, and DC-link voltage at 100 Hz are measured to: 10.5 mA, 35 mV, and 7.8 V, cf. Figure 7.21, at an PV power of 100 W at 27.9 V. The amplitude of the ripple across the PV module was predicted in chapter 5 to 0.2 V at full generation.

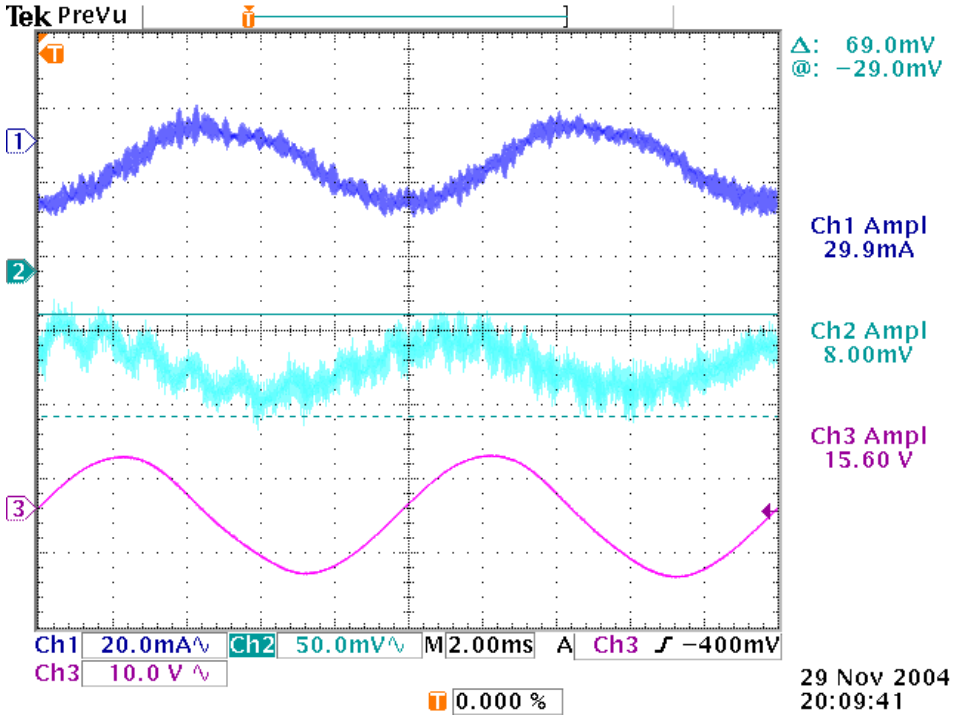

Figure 7.21. Measured signals for audio Susceptibility (AAU, OSC). Ch1 is the PV current, Ch2 is the PV voltage, and Ch3 is the DC-link voltage. Note that the oscilloscope is set to AC for all signals (denoted by the ~). Furthermore, the signals are averaged over 512 samples, in order to remove the HF noise.

7.3.3 Steady State Results

The purpose of this section is to compare the measured values with the simulated values in chapter 5. The European efficiency for the DC/DC converter alone is estimated to 81.7%, which is far away from the 91.6% estimated in chapter 5. The very low efficiency at 5% power is caused by excessive loss in the MOSFETs, since the load current is too low to provide zero-voltage-switching (ZVS). This is verified by measuring the temperature of the encapsulation, which increases suddenly at low power, indicating loss of ZVS.

Table 7.7. Measured results for the DC/DC converter (AAU, PM).

Operating point	5%	10%	20%	30%	50%	100%
PV power [W]	6.5	13.1	27.0	42.0	68.1	134
PV current [A]	0.38	0.67	1.29	1.91	2.96	5.12
PV voltage [V]	17.0	19.5	20.9	22.0	23.0	26.2
Average and peak-to-peak of DC-link voltage [V]	360/5	360/8	360/10	360/10	360/14	360/24
Average DC-link current [mA]	7	21	57	91	160	331
Power into the DC-link	2.5	7.6	20.4	32.7	59.2	119
Grid power [W]	1.4	6.4	18.9	30.8	56.4	113
DC-DC converter efficiency [%]	38.5	58.0	75.6	77.9	86.9	88.8

7.4 Additional Tests

7.4.1 Steady State Efficiency

The steady-state efficiency is measured and depicted in Figure 7.22, with and without the internal power consumption. The total loss in the inverter can be described by a second-order polynomial (without internal consumption):

$$P_{loss,DTI} \approx 0.0012 \cdot {P_{PV}}^2 - 0.0122 \cdot P_{PV} + 0.7519,\ R^2 = 0.9766, \qquad (7.2)$$

$$P_{loss,AAU} \approx 0.00003 \cdot {P_{PV}}^2 + 0.1018 \cdot P_{PV} + 6.2965,\ R^2 = 0.9771,$$

for an input power in the range from 20 Watt to 128 Watt. Applying these equations to the six operating point used to specify the European efficiency, cf. chapter 1, yields the losses and efficiencies in Table 7.8. The European efficiency is computed to 90.0% for the measurements conducted at DTI and 77.0% for the measurements conducted at AAU.

Table 7.8. Measured and interpolated efficiencies, without the internal SMPS (DTI, DL).

Input power	5%	10%	20%	30%	50%	100%
Input power	8 W	16 W	32 W	48 W	80 W	160 W
Loss	0.73 W	0.86 W	1.59 W	2.93 W	7.46 W	29.5 W
Efficiency (TI)	90.9%	94.6%	95.0%	93.9%	90.7%	81.6%
Efficiency (AAU)	21.1%	48.6%	70.0%	73.6%	83.2%	85.3%

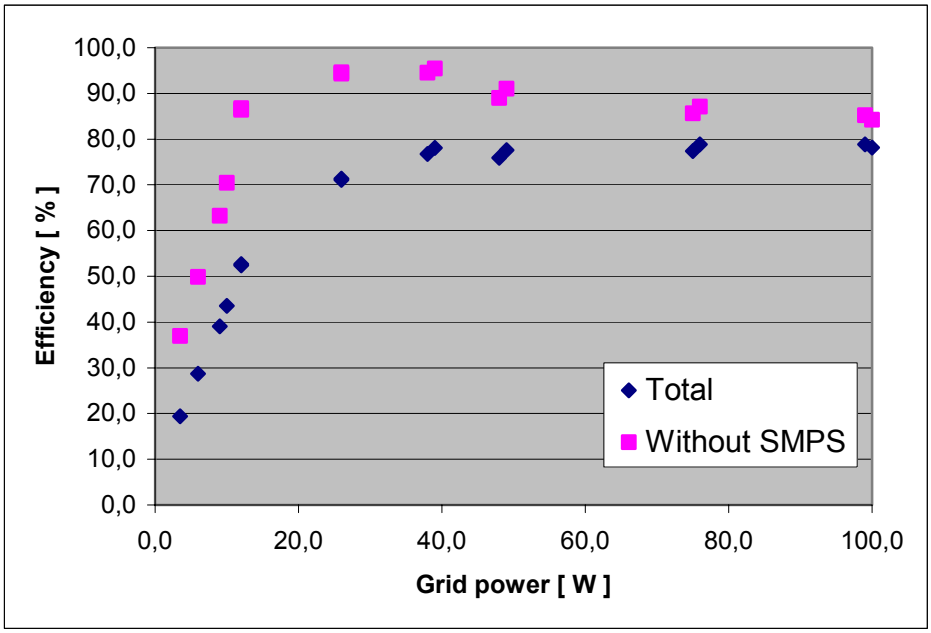

Figure 7.22. Measured efficiency, with and without internal SMPS (DTI, DL).

7.5 Summary

Various test results has been presented in this chapter, e.g. grid and maximum power point tracking (MPPT) performances. The results are summarized in Table 7.1, together with the specifications. As seen, most of the specified values are kept, and a few are still to be determined.

The only two specifications, which are not fulfilled, is the 82/308/CDV standard for grid current harmonics and the amount of high frequency ripple voltage at the input terminals. On the other hand, the 82/308/CDV is not a valid standard yet, so the EN61000-3-2-A standard is instead used to make the final evaluation of the inverter. According to this standard, the inverter is operating in satisfactory manners.

The MPPT algorithm has also been tested intensively. The results indicate a few teething problems during rapid changes in the weather conditions, but they are believed to be easily solved. The efficiency of the MPPT, neglecting the problems mentioned above, is measured to 98% - 100% which is very good.

Finally, the European efficiency, from captured PV power to injected grid power, is measured to 90.0% at DTI and to 77.0% at AAU, without internal power consumptions. Using different types of measuring-devices probably causes the large difference in measured efficiency. Which results is most correct is uncertain, but the result recorded at AAU is believed to be closer to the actual value, than the one recorded at DTI.

A conclusion on the entire project will be stated in chapter 8.

Chapter 8

Conclusion

The photovoltaic (PV) module is an all-electrical device that converts sunlight into electrical DC power. Solid-state power electronic inverters have been used to connect PV modules to the AC utility grid since the early seventies. The inverter has two major tasks: to inject a sinusoidal current into the grid, and to optimize the operating point of the PV modules, to capture the maximum amount of energy.

Large, megawatt, PV systems were connected to the grid in the eighties, but the trend is now to connect smaller systems to the grid, in order to overcome certain problems, like non-flexible designs, mismatch losses between the PV modules, etc. These systems are either based on the string-concept, with multiple modules connected in series, or on a single PV module.

The main objective for this thesis was to develop an inverter for the AC module, with special focus on cost, reliability, and efficiency. A topology, among several different, has been pinpointed as the best candidate based on detailed analysis. The inverter has been optimized in respect to cost, reliability, efficiency, and a prototype has been build and tested.

8.1 Summary

The PV module has been addressed in chapter 2, starting with a historical review of the state of the PV technology, and a short review of different technologies, e.g. mono-crystalline silicon modules and thin film modules is done. The mechanism behind the photon-to-electron conversion inside the PV module was also shortly discussed. This ended up with a model of the PV module, taking into account the inherent PN junction and the current generated by the incoming sunlight. Other parts inside the PV module are also briefly described, e.g. resistances and capacitances. The model was used to investigate the role of partial-shadow and voltage/current ripple at the PV module terminals, in respect to power degradation.

Based on the analysis of the PV module, the present and expected future standards for the grid-interface, the specifications for the inverter to be designed were put up in chapter 3. The main specifications are: PV module voltage is defined in the range from 23 V to 50 V. Maximum PV power is equal to 160 W. The RMS value of the grid voltage is guaranteed in the span 197 V - 253 V, by the utility companies, and the power factor shall be better than 0.95 at 50% generation (80 W).

Two different systems layouts, the PV module and inverter integrated into one device, placed on the roof, or the inverter situated inside the residence, were investigated in chapter 4 to find pros and cons for each layout. The examination focused on the hotspot temperature of the electrolytic capacitors included in the design, which is known to be the main lifetime limiting component.

A literature study of 14 different topologies was conducted, and the 8 most promising topologies have been compared with respect to; maximum stress of the components, component ratings, relative cost, and European efficiency, in order to find the best solution according to the main objective for the project. The most promising solution, in terms of ratings, cost (157 DKK ≈ 21 €), and European efficiency (95.4%) was found to be a push-pull DC-DC converter, modulating a rectified sinusoidal output current, together with a DC-AC inverter switching at twice the line frequency, to unfold the rectified sinusoidal current into the grid current.

The selected inverter was designed in chapter 5, with the specifications in mind and focus on cost and efficiency. For example, the size of the grid-connected filter was cost-optimized by searching the solution within 15 combinations of different inductor and capacitor sizes, when the resonant frequency of the filter was kept constant. The size of the transformer included in the DC-DC converter was chosen as a tradeoff between power losses and cost, whereas the size of the DC-link inductor was optimized in respect to its cost.

A dedicated current mode controller (integrated circuit - IC) is used to control the DC-DC converter, where the reference is the current drawn from the PV module. It becomes in this way possible to regulate the operating point of the PV module.

The controllers included in the microcontroller are designed in chapter 6, which includes: a Maximum Power Point Tracker (MPPT) for optimizing the captured energy from the PV module, a Phase Locked Loop (PLL) to synchronize the inverter with the grid, detection of islanding operation, control of the DC-link voltage, and control of the grid current.

A survey of different MPPT algorithms showed that the traditional algorithms all have some problems with finding the Maximum Power Point (MPP). A novel MPPT algorithm has been proposed and tested with both a PV emulator and with real PV modules.

A single phase PLL is also designed for the inverter. Two different implementations of the trigonometric functions were discussed in order to minimize the ripple into the included PI controller when the actual frequency does not agree with the nominal frequency. The frequency output from the PLL is also used to determine the state of islanding operation, together with the determination of the value of the grid voltage. Four different schemes for computing the value of the grid voltage have been evaluated, and the RMS approach has been identified as the most accurate solution.

The reference for the DC-link voltage is made equal to a function of peak grid voltage and average power injected into the grid, in order to keep the DC-link voltage as low as possible, and hereby lowering the switching losses in the MOSFETs and protecting the electrolytic capacitor in the DC-link. The controller is based on a classical PI controller, where the output from the PI controller is the peak current reference. The values of the parameters included in the PI controller are designed so as not to cause too much third harmonic current injection into the grid, caused by the twice-the-line-frequency voltage ripple in the DC-link.

Finally, the grid current controller is also based on the PI controller, with a feed forward of the grid voltage. The stability of the system is evaluated for parameter variations in the grid-connected, reduced order, LR-filter. The stability is also evaluated for the full-order model of the LCL filter, and a proper size of the damping resistor, included in the LCL filter, is determined to obtain a minimum-phase system. Three possible voltage feed-forward schemes were shortly discussed, and a 20 ms delayed signal is applied in the control. Compensation of the blanking time effect was also discussed in brief, to reduce the harmonic currents. No compensation should be used, but the blanking time is kept small, without causing shoot-through in the MOSFETs.

Finally, the realized prototype is evaluated in chapter 7, including a list of changes between the designed and the realized inverter. The evaluation includes measurements on the interfaces between the grid and the inverter, and between the PV module and the inverter.

8.2 Achievements

The main objective for the research presented in this thesis has been to develop an inverter for the AC module, which is the combination of a single PV module and a DC-AC inverter connected to the grid. Focus has been on obtaining a low-cost solution with high reliability, i.e. long lifetime, and high efficiency. This has been accomplished by theoretical analysis of cost, efficiency and ratings for many different inverter topologies, on which basis a topology was selected for further design. The design of the selected topology was also based on theoretical analysis, supported by numerical simulations and measurements on the realized prototype. The main conclusions and originalities for this thesis are listed here (in order of appearance in the thesis):

- A theory for the reduction in available power from the PV module, as function of low frequency ripple in the modules voltage and current, is presented. The theory predicts a power loss of 1%, i.e. a utilization ratio of 99%, for a mono-crystalline PV module when the amplitude of the ripple voltage is equal to 6% of the MPP voltage, and a loss of 2% when the ripple equals 8.5%. Such work has not been seen in the literature. The voltage ripple can be reduced to an acceptable level by adding a large 2200 μF electrolytic capacitor at 63 V in parallel with a standard 72 cells, 170-Watt module. Another solution is to include a decoupling capacitor in the DC-link, between the two power stages, where its size can be reduced to 33 μF at 450 V.

- The lifetime of the inverter is analyzed, when located in- and out-door, respectively. The main limiting factor is assumed to be the above-mentioned power decoupling capacitor, either placed in parallel with the PV module or in the DC-link. However, other failure-mechanisms do also exist, but are omitted in the analysis. The desired lifetime for the inverter is equal to 25 years, based on the specified PV module lifetime. It is concluded that the capacitor must be placed in the DC-link, between the two power stages, if the inverter is to be integrated with the PV module. On the other hand, the capacitor can either be placed in parallel with the PV module or in the DC-link if the inverter is to be placed indoor. The conclusion is based on measured daily maximum temperature over a span of ten years, and computed monthly maximum solar irradiation.

- Two novel inverter topologies, the modified Shimizu inverter, and the isolated flyback in parallel-series connection, were presented. Both inverters offer good power decoupling with small capacitors, the flyback inverter even with film capacitors, but they suffer from large internal currents that results in low efficiencies.

- A method for analytic comparison of different inverter topologies, with focus on component stress and ratings, cost, and efficiency, is proposed. The methodology ensures that the components in the different topologies are exposed to the same amount of electrical and thermal stress, so as to make a fair comparison.

- A novel Maximum Power Point Tracker (MPPT) algorithm, which solves some problems within the standard algorithms with tracking the MPP during partial shadow of the PV module and rapid changes in the weather conditions, is proposed. The algorithm initially locates the global MPP by sweeping (scanning) the voltage-current characteristic of the PV module. The co-ordinates for the MPP is recorded, and the recorded MPP current is used as a new reference for the next period of normal operation (non-scanning period), until the voltage across the PV module changes more than ΔU from the recorded MPP voltage. Tests conducted at the Danish Technological Institute (DTI) shows that the MPPT algorithm has an average steady state efficiency of 99.0%, for available power in the range from 23 W to 143 W, which is regarded as being excellent. However, the test at DTI also showed that the algorithm has some teething problems: the algorithm sometimes causes the voltage across the PV module to collapse and stays there for a long time. However, this is believed to be of minor significance, and can easily be corrected. Tests made at Aalborg University (AAU) show excellent tracking capabilities during rapid changes in the solar irradiation.

- A method to optimize the components in a LCL filter, in respect to cost, is suggested. The scheme was used with success, reducing the cost of the LCL filter from 58.0 DKK to 24.9 DKK, without compromising the specifications. The optimal number of turns on the primary/secondary side for transformers and inductors is based on the new 'modified core geometrical constant' approach. The approach combines the 'modified Steinmetz equation' for computing the core loss in magnetic components, and the standard K_g method, to compute the number of turns.

- Finally, the realized prototype is tested against the specifications, at AAU. The measurements show that the inverter is close to keep all the demands, which includes operating range (voltage and current) for the PV module, and the grid, interfaces. The grid voltage monitoring is capable of detecting islanding operation, within the specified range, but the frequency monitoring is omitted in the prototype and therefore not tested. Nor is the inverter tested for successfully operation within the nominal range of the grid frequency. The standby power consumption from the grid is measured to 0.5 W, which is low. The amount of harmonic current injected into the grid is lower then the limits given in the EN61000-3-2 standard, but too high to fulfill the 82/308/CDV draft. The power factor at 50% of nominal power is measured to 0.98, which is higher than the 0.95 required by the Danish Utilities. Last, but not least, the European efficiency of the realized prototype is measured to 90.0% at DTI, and 77.0% at AAU, both without the internal power supplies. Which results is most correct is still uncertain.

Based on the conclusions given above, all the objectives for the project are believe fulfilled.

8.3 Future Work

Some aspects of inverters for PV applications have been treated in this research project. Nevertheless, there are still many interesting aspects and many problems to be investigated in the future. Some of them are listed here (in order of appearance in the thesis, if included):

- Diagnosis of the PV module(s): Online detection of partial shadow(s) of the module(s) and determination of the series resistance, in the module(s) and connections, can inform the operator to inspect the systems for bad connectors, and suggest her/him to remove the source of the partial shadow (e.g. a local impurity of the module or a tree/flagstaff).

- A deeper investigation of the inverters lifetime, based on hourly temperature variation and the applied power semiconductors, is probably needed to reach the desired lifetime of 25 years. The analysis applied in this thesis only accounts for the daily maximum-temperature inside the applied electrolytic capacitor.

- The inverter topology suggested in chapter 4 (Figure 4.21) should be designed, realized and tested against the inverter designed in this thesis, to see which is the best candidate for the AC module.

- Burst-mode operation should be analyzed in depth and tested on the realized prototype in respect to increased efficiency and degradation of grid performance. It is believed that burst-mode can increase the efficiency, but it may also cause flicker on the grid, if large amounts of PV power is installed.

- An active clamp circuit should be included in the DC-DC converter to lower the requirements for the diodes included in the rectifier, and to increase the efficiency.

- Cost and loss comparison of the voltage-source DC-DC converter, which is applied in this project, and the current-source DC-DC converter. The current-source converter also solves the problems with the requirements for the diodes included in the rectifier, but other problems may appear.

- Further investigations of different controllers for the grid current, e.g. the P+resonant controller, and repetitive control for cancellation of harmonic currents are interesting. The effect of compensating the blanking time should be investigated, to get a better grid performance in terms of lower harmonics, etc.

- The inverter should be tested for immunity to abnormal grid operation, e.g. voltage swells and sags, and phase jumps. Besides, the immunity to notches and spikes should be investigated.

- Analyze the impact on the grid performance (power quality) when multiple inverters are connected to a local grid. Especially, the effect from different waveform generators, for the current reference, and different current control strategies should be investigated. Both when the grid voltage is a pure sinusoidal and when it contains harmonics.

- Make a SWOT (Strengths, Weaknesses, Opportunities and Threats) analysis of the AC module concept, to see whether it is better than other concepts, e.g. the string and the multi-string concepts.

- Finally, the next step for product development is to optimize the inverter in respect to the microcontroller, the switch mode power supply, measuring- and protection-circuits, etc. This also includes that a printed circuit board must be designed, with additional space for EMI filters, since these filters are not designed in this project.

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Appendix A

PV Module Survey

This appendix covers 9 manufacturers of PV-modules. A total count of 35 mono- and multi-crystalline 72-cells PV modules is listed. All data are given recorded at Standard Test Condition (STC). The reverse saturation current, I_{RS}, and diode quality factor, A, are calculated by the equations given in chapter 2.

Company	Type	P_{MPP} [W]	U_{MPP} [V]	I_{MPP} [A]	U_{OC} [V]	I_{SC} [A]	K_{temp} [mA/K]	I_{RS} [uA]	A [.]	NOCT [°C]	Area [m^2]	$R_{\theta,JA}$ [K/W]
BP Solar	3160	160	35.1	4.55	44.2	4.80	3.1	3.49	1.69	47	1.26	0.027
	4170	170	34.7	4.90	44.0	5.40	3.5	61.9	2.09	47	1.26	0.027
	4160	160	35.4	4.52	44.2	4.90	3.2	13.9	1.87	47	1.26	0.027
	7180	180	36.2	5.00	44.8	5.40	3.5	9.71	1.83	47	1.26	0.027
	7175	175	36.0	4.90	44.4	5.30	3.4	10.7	1.83	47	1.26	0.027
	7170	170	35.8	4.80	44.2	5.20	3.4	12.0	1.84	47	1.26	0.027
	3150	150	34.5	4.35	43.5	4.75	3.1	31.2	1.97	47	1.26	0.027
Eurosolare	ML16/150	150	35.0	4.30	43.5	4.90	-	-	-	50	1.28	0.029
	ML16/135	135	33.0	4.10	42.0	4.80	-	-	-	50	1.28	0.029
	PN12/130	130	30.6	4.25	38.0	4.60	-	-	-	50	1.28	0.029
	PN16/160	160	35.5	4.50	44.0	4.90	-	-	-	50	1.28	0.029
	PN16/150	150	35.0	4.30	43.2	4.80	-	-	-	50	1.28	0.029
	PN16/140	140	34.2	4.10	42.6	4.60	-	-	-	50	1.28	0.029
Evergreen Solar	EC102	102	32.4	3.15	40.0	3.75	3.3	311	2.30	44	0.98	0.031
	EC110	110	32.7	3.36	40.0	3.84	3.4	46.7	1.91	44	0.98	0.031
	EC115	115	33.0	3.48	40.0	3.86	3.4	6.19	1.62	44	0.98	0.031
PhotoWatt	PW1650	175	34.8	5.03	43.2	5.30	-	-	-	-	1.36	-
	PW1650	165	34.4	4.80	43.2	5.10	-	-	-	-	1.36	-
	PW1650	155	34.0	4.56	43.0	4.80	-	-	-	-	1.36	-
Sharp	NTS5E3E	185	36.2	5.11	44.9	5.75	4.4	64.9	2.13	-	1.30	-
	NTR5E3E	175	35.4	4.95	44.4	5.55	4.3	102	2.20	-	1.30	-
	NEQ5E3E	165	34.6	4.77	43.1	5.35	3.7	69.5	2.07	-	1.30	-
Shell	Ultra175	175	35.4	4.95	44.6	5.43	1.4	40.1	2.04	46	1.32	0.025
	Ultra165	165	35.0	4.72	44.5	5.40	1.4	387	2.52	46	1.32	0.025
	Plus160	160	34.0	4.71	43.1	5.20	1.5	67.5	2.07	44	1.32	0.023
	Plus150	150	33.0	4.55	42.6	5.10	1.5	230	2.30	44	1.32	0.023
SolarWorld	SW155	155	34.6	4.50	43.1	4.90	2.0	16.7	1.85	45	1.30	0.024
	SW165	165	35.4	4.70	43.3	5.10	2.0	6.82	1.73	45	1.30	0.024
	SW175	175	36.1	4.90	44.1	5.20	2.1	1.77	1.60	45	1.30	0.024
	SW155	155	33.5	4.70	42.1	5.20	2.6	103	2.10	45	1.30	0.024
	SW165	165	34.6	4.80	43.0	5.30	2.7	37.6	1.96	45	1.30	0.024

Company	Type	P_{MPP} [W]	U_{MPP} [V]	I_{MPP} [A]	U_{OC} [V]	I_{SC} [A]	Ktemp [mA/K]	I_{RS} [uA]	A [.]	NOCT [°C]	Area [m^2]	$R_{\theta,JA}$ [K/W]
Solterra	Sol130	130	34.0	3.82	-	-	-	-	-	-	1.27	-
	Sol140	140	34.3	4.08	-	-	-	-	-	-	1.27	-
	Sol150	150	34.7	4.32	-	-	-	-	-	-	1.27	-
Sunpower	SPR-210	210	40.0	5.25	47.8	5.65	-	-	-	49	1.24	0.029
	SPR-200	200	40.0	5.00	47.8	5.40	-	-	-	51	1.24	0.031

The minimum and maximum insulation, P_{sun}, is assumed equal to 60 W/m^2 and 1200 W/m^2, respectively. The minimum and maximum ambient temperature, T_{abm}, is further assumed equal to –10 °C and 40 °C, respectively. The PV cell temperature at open circuit conditions is estimated as

$$T_{cell} = T_{abm} + \frac{45.6°C - 20°C}{800W/m^2} \cdot P_{sun}, \tag{A.1}$$

where the temperature of 45.6 °C is the average NOCT for the highlighted PV modules.

After making 208 calculations with the PV modules given above, and the theory in chapter 2, the maximum MPP (Maximum Power Point) voltage, U_{MPP}, was recorded to 37.4 V at an irradiation of 360 W/m^2 and an ambient temperature of –10 °C. The minimum MPP voltage was recorded to 22.9 V for a small PV module with a nominal power of 102 watt, and 25.4 V for a 150 watt PV module. Both recorded at an irradiation of 1200 W/m^2 and an ambient temperature of 40 °C. Another 104 calculations revealed that the maximum open circuit voltage, U_{OC}, is equal to 45.1 V at an irradiation of 360 W/m^2 and an ambient temperature of –10 °C. Finally, 52 simulations showed that the maximum MPP power, P_{MPP}, equal 189 W at an irradiation of 1200 W/m^2 and an ambient temperature of 25 °C.

Simple calculations, c.f. chapter 2, reveals that the maximum short-circuit current, I_{SC}, equals 7.2 A, at an irradiation of 1200 W/m^2 and an ambient temperature of 40 °C.

$$i_{sun} = \left(i_{sun,STC} + k_{temp} \cdot (78.4°C - 25.0°C)\right) \cdot \frac{1200W/m^2}{1000W/m^2}. \tag{A.2}$$

Thus, the following specifications for the PV module interface is hereby recommended:

- Maximum MPP current, I_{MPP}: 6.2 A,
- Maximum input current, I_{SC}: 7.2 A,
- MPP voltage range, U_{MPP}: 23 V to 38 V,
- Maximum open loop voltage, U_{OC}: 50 V,
- Nominal power, P_{MPP}: 160 W,
- Maximum MPP power: 190 W.

The following six operating points (corresponds to the Shell Ultra175 PV module) are defined, in order to evaluate the European efficiency [15].

Operating point	5%	10%	20%	30%	50%	100%
Meteorological conditions	60 W/m^2 10 °C	120 W/m^2 12 °C	240 W/m^2 15 °C	360 W/m^2 18 °C	600 W/m^2 24 °C	1200 W/m^2 40 °C
Cell temperature	12 °C	16 °C	23 °C	30 °C	43 °C	78 °C
Power [W]	8.2 W	17.5 W	36.3 W	54.9 W	89.9 W	160.3 W
Voltage [V]	28.6 V	30.1 V	31.2 V	31.5 V	31.0 V	28.1 V
Current [A]	0.29 A	0.58 A	1.16 A	1.74 A	2.90 A	5.70 A

Appendix B

PV Inverter Test Plan

This appendix is a reproduction from [40].

An inverter used in grid connected photovoltaic (PV) systems must satisfy some specifications, which are stated by national and international standards. The test plan described below is intended to be a thorough evaluation that can be used for the characterization of the designed inverter. The plan is based on the international standards and the experience in the field of grid connected PV systems. It covers functional tests, protection tests and field tests. These tests are performed in order to evaluate the following characteristics of the inverter:

- Static power efficiency
- Power factor
- Current harmonics
- Maximum Power Point Tracking (MPPT) efficiency
- Standby losses
- Disconnections of AC power line
- Disconnections of DC power line
- AC voltage limits
- Frequency limits
- Response to abnormal utility conditions
- Field test

B.1Power Efficiency

The power efficiency of an inverter is defined in the IEC 61683 [110] as the ratio between the delivered power and the absorbed power.

B.1.1 Test Circuit

For efficiency test the following equipments are required:

- Power analyzer
- PV-array simulator

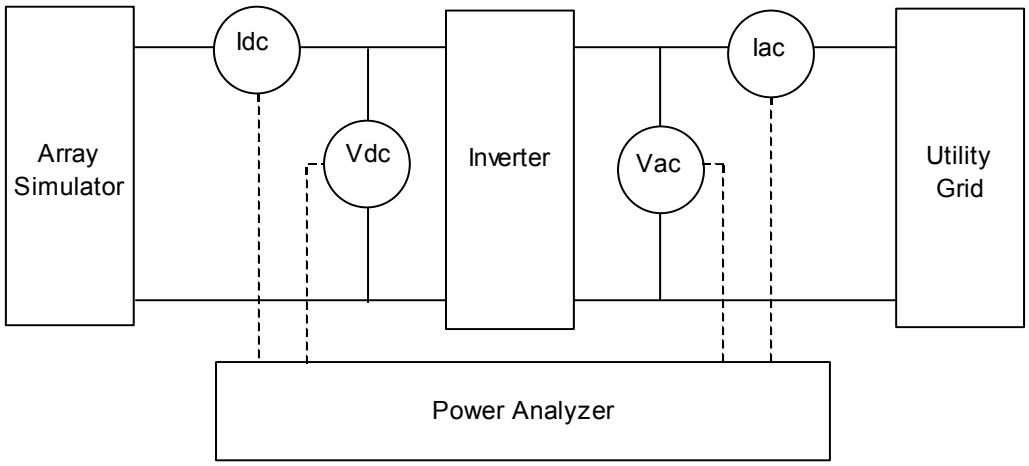


Figure B.1. Set-up for power efficiency test.

B.1.2 Procedure

Power efficiency is calculated from the measured values of the delivered power and the absorbed power. Both powers represent the average of n values sampled within a period not less than 30 seconds. The average of the sampled values is acceptable if the MPPT and input source (PV-array simulator) interact in such a way that the input voltage values varies by less than 5%.

Measurements should be performed for power levels of 5%, 10%, 20%, 25%, 30%, 40%, 50%, 75%, 80%, 100% and 120% of inverter rating at the following inverter input voltages:

- Minimum rated input voltage
- Nominal input voltage or the average of its input range
- 90% of inverters maximum input voltage

From the measurements, the power efficiency curve can be generated and the European efficiency can be calculated easily as follows [15]:

$$\eta_{EU} = 0.03 \cdot \eta_{5\%} + 0.06 \cdot \eta_{10\%} + 0.13 \cdot \eta_{20\%} + 0.10 \cdot \eta_{30\%} + 0.48 \cdot \eta_{50\%} + 0.20 \cdot \eta_{100\%} \quad \text{(B.1)}$$

The European efficiency is a proposed measure for the averaged efficiency in relation to irradiation for the European countries.

B.2Power Factor

The purpose of this test is to determine the power factor of the system and see if it is consistent with the international standards. According to Report IEA T5-06: 2000 [111], the power factor should be higher than 0.95 at a power level above 20% of rated power.

B.2.1 Test Circuit

This test can be done simultaneously with the power efficiency test. However, there is no need to measure the input power. Therefore, the following equipments are needed:

- Power analyzer, Oscillostore P 513
- PV-array simulator

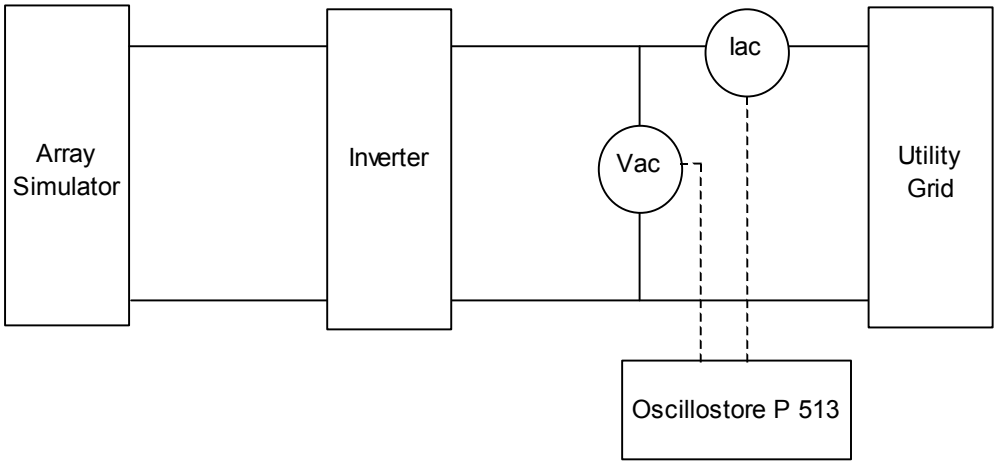


Figure B.2. Set-up for power factor test.

B.2.2 Procedure

I order to se if the power factor of a PV system connected to utility satisfies the international standards it is necessary to determine the power factor at different power levels. To do so, the circuit shown in Figure B.2 is set up and the array simulator is adjusted such that its MPP voltage is equal to the nominal input voltage of the inverter. The data for power factor is then collected at power levels of 20%, 40%, 80% and 100% of inverter rating, according the recommendations of IEA Task V [111].

B.3 Current Harmonics

The Total Harmonic current Distortion (THD_I) is defined as:

$$THD_I = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1}, \tag{B.2}$$

where I_1 = RMS value of the fundamental current, I_n = RMS value of harmonic current of order n.

In general the operation of the PV system should not cause excessive distortion of the utility voltage waveform or result in excessive injection of harmonic currents into the utility system. Suggested limits for current harmonics at full power is 5% for total harmonic current distortion and 3% for individual current harmonics. These limits are recommended in IEEE std. 929-2000 as stated in report IEA T5-06: 2000 [111].

B.3.1 Test Circuit

The following equipments are required to perform this test:

- Power analyzer, Oscillostore P 513
- PV-array simulator

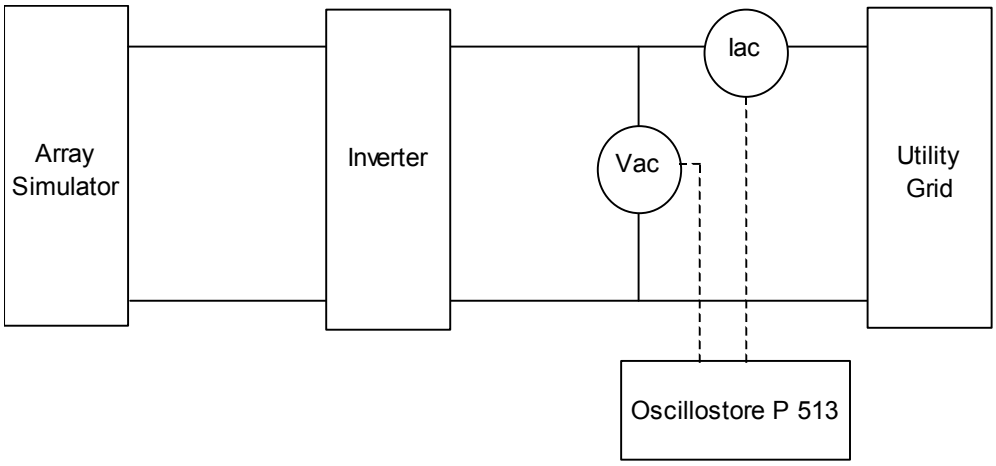


Figure B.3. Set-up for current harmonics test.

B.3.2 Procedure

In this test the harmonic current to the grid must be measured while the inverter is operating at its nominal output power and nominal input voltage. Therefore the PV-array simulator must be adjusted accordingly. A power analyzer is connected to AC output of the inverter and the current harmonic distortion data are collected. The power analyzer must have a response of at least the 25th harmonics [111]. Note that this test can be done simultaneously with the power efficiency test.

B.4Maximum Power Point Tracking Efficiency

The static MPP efficiency can be defined as:

$$\eta_{MPP} = \frac{100\%}{P_{MPP} \cdot T_m} \int_o^{T_m} P_{DC}(t) \cdot dt \,, \tag{B.3}$$

where $P_{DC}(t)$ is the DC power of inverter input, T_m is the duration of the measurement, and P_{MPP} is the available PV power at MPP of the array.

B.4.1 Test Circuit

For MPP tracking efficiency test the following equipments are required:

- Power analyzer, Oscillostore P 513
- Data logger, Squirrel SQ 1600
- PV-array
- IV curve tester
- PC

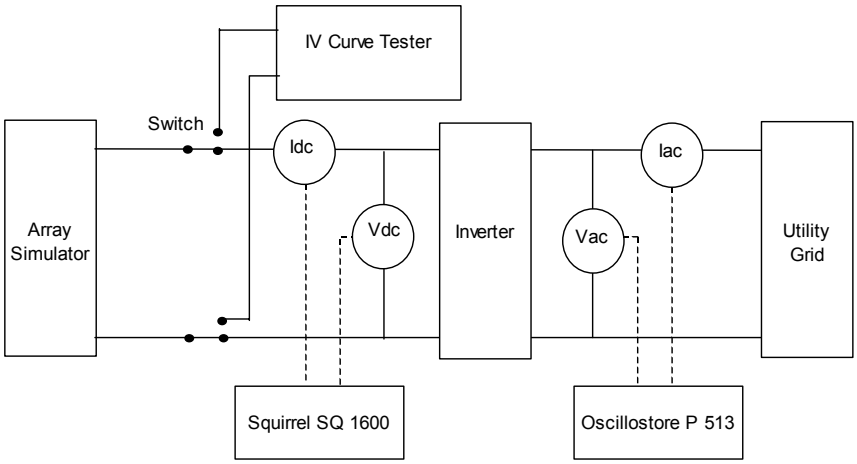


Figure B.4. Set-up for MPP tracking efficiency test.

B.4.2 Procedure

To begin the test, the PV-array simulator is adjusted to meet the inverter input nominal voltage. The integral part in equation (B.3) represents the energy absorbed by the inverter during the interval T_m. During the test, the absorbed energy is measured from a set of power amplitude sampled each 10 seconds over a period of 60 seconds. The PV array simulator is then disconnected from the inverter and then connected to the IU curve tester to measure the actual available power at MPP. The test is performed for power levels of 10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, and 100% of inverter output rating. For more details se the procedure described in ECN-C-01-095 [112]

B.5Standby Losses

The standby loss is defined in the IEC 61683 [110] as the consumption of utility power when the inverter is not operating but under standby conditions. The inverter is under standby conditions when the input voltage decreases below the minimum operating voltage due to bad weather conditions or during night.

B.5.1 Test Circuit

For evaluation of standby losses the following equipments are needed:

- Power analyzer, Oscillostore P 513
- PV-array simulator
- Digital multimeter

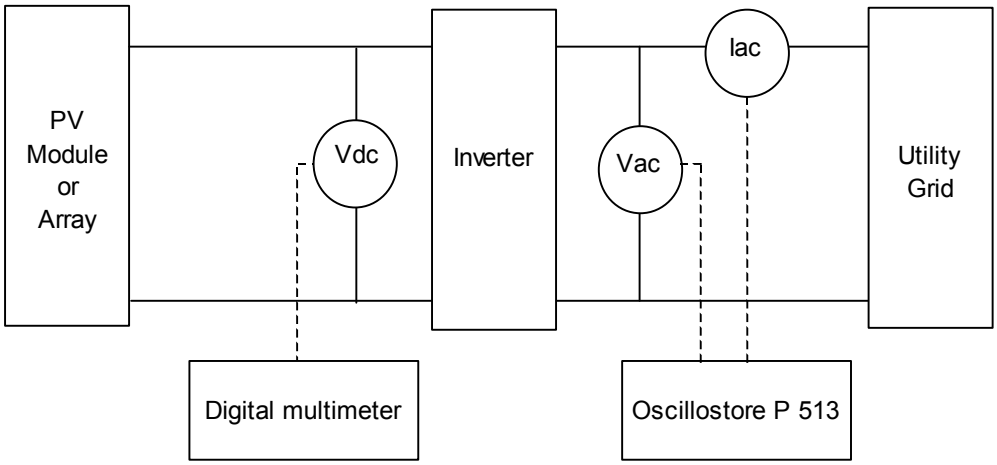


Figure B.5. Set-up for the evaluation of standby losses.

B.5.2 Procedure

A PV module/array, whose characteristics satisfy the input ratings of the inverter under test, is connected to the inverter. The system is put under weather conditions such that the input voltage of the inverter is below the minimum operating value. The situation corresponding to standby losses during the night can be achieved by covering the PV module/array. Under these conditions the power consumption of the inverter is measured. The standby loss is measured using the power analyzer and the input voltage is always measured using the digital multimeter to guarantee that the input voltage is less than the minimum operating input voltage of the inverter. The standby losses are measured and collected using the power analyzer.

B.6Disconnection of AC Power Line

The purpose of this test is to observe the inverter response under loss of utility condition. Under such a condition it is expected that the voltage at the inverter output drops to zero after a very short period of time known as the trip time. The inverter allowable maximum trip time differs from standard to standard and depends on the local loads and on the encountered abnormal condition. For example, EnergieNed [112] demands a safeguard, which reacts within 0.1 seconds if the grid voltage drops below 80% of the nominal value. The IEEE 929 [113] requires a maximum trip time of 120 cycles for a deviation in voltage from 50% to 88% of the nominal value. Under abnormal conditions, the inverter will actually remain connected to the utility to allow sensing of utility electrical conditions to be used by reconnect feature. The inverter should automatically reconnect to the utility if the normal conditions are sensed. However, according to the IEC 617227 [104], a time delay from 30 sec to 3 min should be allowed to avoid excessive nuisance tripping.

B.6.1 Test Circuit

For disconnection of AC power line test the following equipments are required:

- Power analyzer, Oscillostore P 513
- PV-array simulator
- Oscilloscope

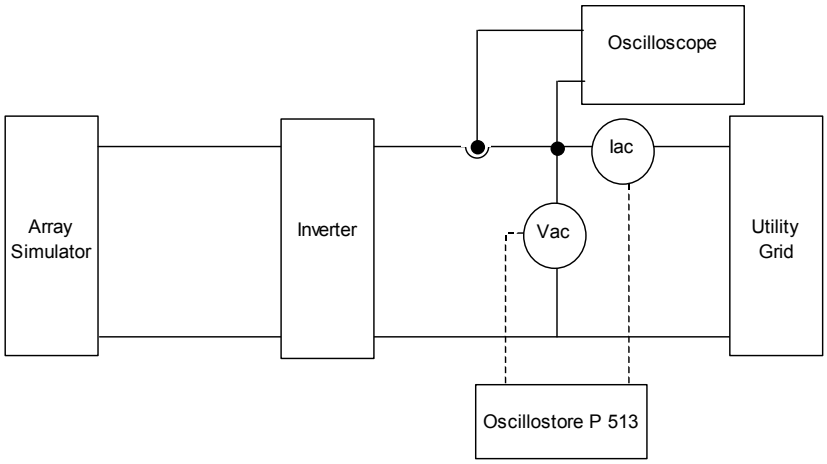


Figure B.6. Set-up for disconnection of AC power line test.

B.6.2 Procedure

The procedure described in reference [104] is followed in order to determine the time it takes the inverter to disconnect from the utility under disconnection of AC power line condition. At two different power levels 25% and 100% of inverter output rating, the grid is disconnected and the AC-side voltage and current are monitored using an oscilloscope. To determine the recovery time, the utility is reconnected and again the AC-side voltage and current are monitored. During this test, the array simulator is adjusted to meet the nominal input ratings of the inverter.

B.7Disconnection of DC Power Line

The purpose of this test is to observe the reaction of the inverter when the DC power line is suddenly disconnected.

B.7.1 Test Circuit

For disconnection of DC power line test the following equipments are required:

- Power analyzer, Oscillostore P 513
- PV-array simulator
- Oscilloscope

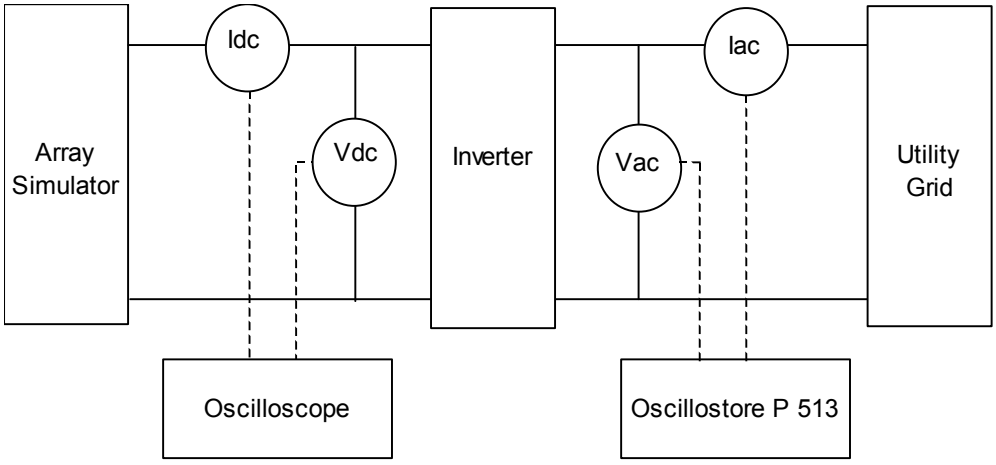


Figure B.7. Set-up for disconnection of DC power line test.

B.7.2 Procedure

Again the procedure described in reference [112] is followed in order to observe the reaction of the inverter under the loss of DC power line condition. This procedure requires that measurements be done at two different power levels 25% and 100% of inverter output rating and at two different array configurations. These configurations represent the minimum and maximum input conditions according to the inverter specifications. The oscilloscope is used to monitor the DC-side voltage and current and to measure the time it takes the inverter to stop operation.

B.8AC Voltage Limits

The purpose of this test is to determine the AC voltage limits (over/under voltage) at which the inverter stops operating.

B.8.1 Test Circuit

The following equipments are needed in order to perform this test:

- Power analyzer, Oscillostore P 513
- PV-array simulator
- Grid simulator

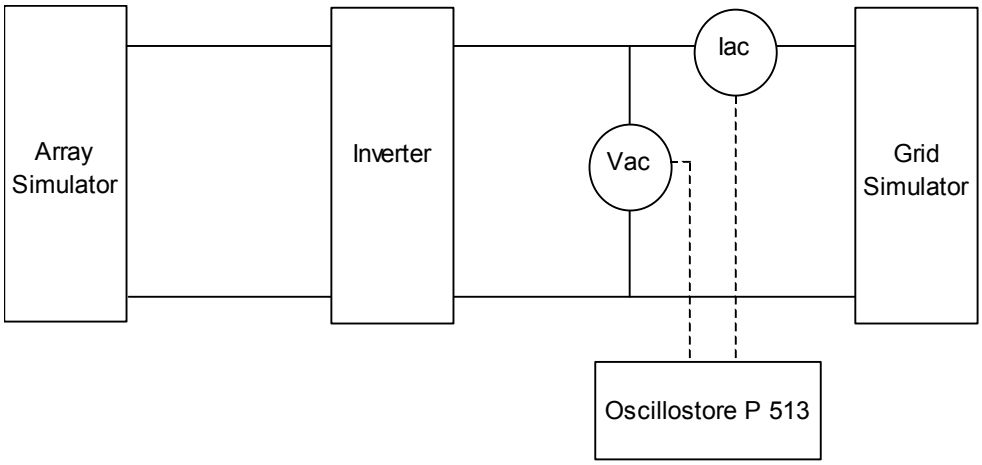


Figure B.8. Set-up for determining the AC voltage limits.

B.8.2 Procedure

The procedure described in reference [112] is followed to perform this test. As a starting point, the PV array simulator is adjusted to meet the inverter nominal input voltage. Then the inverter output power is set to 50% of the nominal output power and the grid voltage is set to its nominal value. The grid voltage is slowly increased or decreased by steps of 0.1V/sec until the inverter stops providing energy to the utility. At each step the grid voltage is recorded. The last recorded voltage levels, just before the inverter stops providing energy to the utility, represent the AC voltage limits.

B.9Frequency Limits

The purpose of this test is to determine the frequency limits (over/under frequency) at which the inverter stops operating.

B.9.1 Test Circuit

The following equipments are needed in order to perform this test:

- Power analyzer, Oscillostore P 513
- PV-array simulator
- Grid simulator

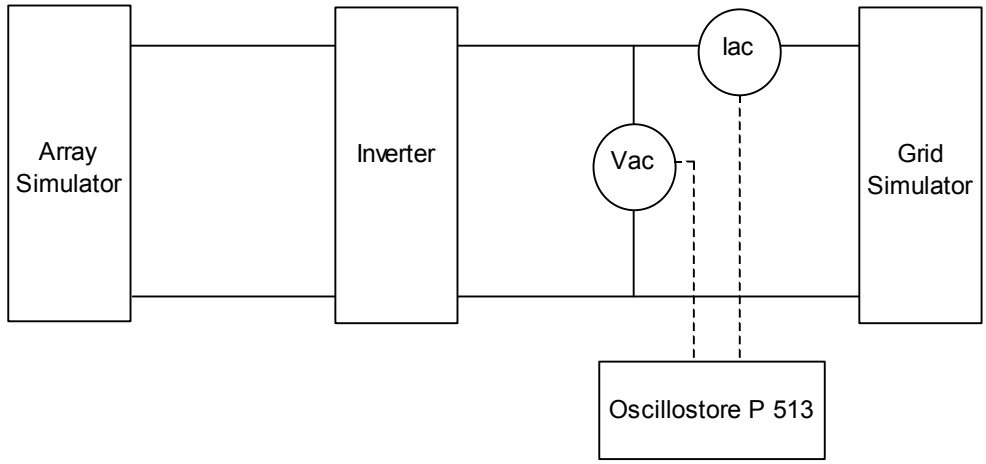


Figure B.9. Set-up for determining the frequency limits.

B.9.2 Procedure

The procedure described in reference [112] is followed to perform this test. As a starting point, the PV array simulator is adjusted to meet the inverter nominal input voltage. Then the inverter output power is set to 50% of the nominal output power and the grid voltage is set to its nominal value. The frequency limits are determined by slowly increasing and decreasing the grid frequency by 0.1Hz/sec until the inverter stops providing energy to the utility. At each step the grid frequency is recorded. The last recorded values of frequency, just before the inverter stops operating, represent the frequency limits.

B.10 Response to Abnormal Utility Conditions

The purpose of this test is to observe and verify the operation of the inverter under abnormal utility conditions. The abnormal utility conditions of concern are voltage and frequency excursions above or below the specified values. According to the IEC 61727 [112], the operating voltage window is 88% to 110% of nominal voltage and the operating frequency window is 47 to 50.5 Hz. It is expected that the inverter cease to energize the utility power line whenever the voltage or frequency at the point of utility connection deviates from the allowable value within a very short period of time depending on the abnormal condition and local loads. After the utility has been recovered for 30 sec to 3 min, the inverter must automatically reconnect the utility.

B.10.1 Test Circuit

In order to observe and record the operation of the inverter under abnormal utility conditions, the following equipments are required:

- Power analyzer, Oscillostore P 513
- PV-array simulator
- Grid simulator
- Oscilloscope

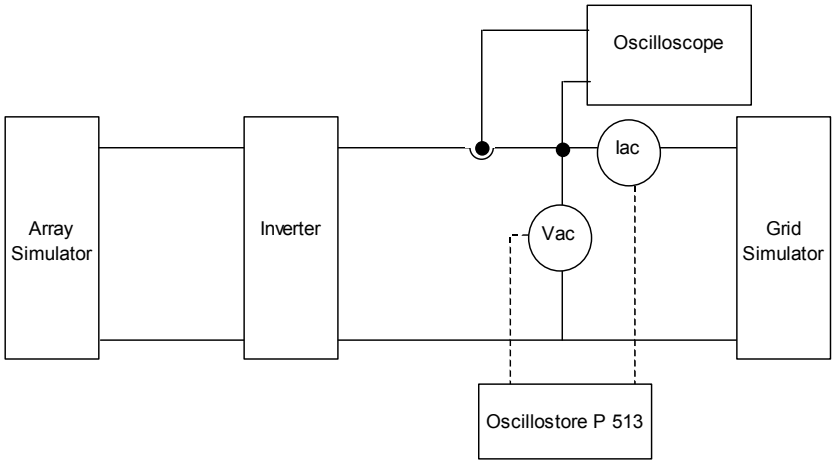


Figure B.10. Set-up for verifying the inverter operation under abnormal utility conditions.

B.10.2 Procedure

In this test the inverter is set at a power level of 50% of output rating at nominal grid voltage. The PV array simulator is adjusted to meet the inverter nominal input voltage. For a stepwise change of the voltage or frequency from the nominal value to the upper or lower limit, the current and voltage waveforms on the AC-side, as well as the trip time, are measured using an oscilloscope. For more details see the procedure described in reference [112].

B.11 Field Test

The purpose of this test is to evaluate the performance of the inverter when connected to normally illuminated modules of different technologies (for example c-Si modules and a-Si modules, i.e. crystalline and amorphous silicon modules). In this test many parameters such as energy efficiency, start up voltage, start-up power, stop voltage and standby losses can be measured.

B.11.1 Test Circuit

In this test the following equipments are needed:

- c-Si module(s)
- a-Si module(s)

- Reference cell
- Temperature sensor
- Data logger
- PC

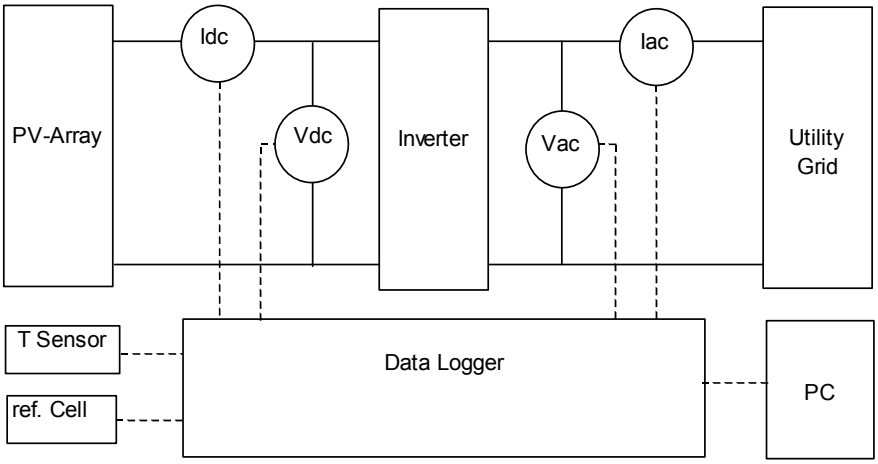


Figure B.11. Set-up for field test.

B.11.2 Procedure

A solar energy generator made up of one or more c-Si modules is connected to the inverter. The solar generator is located outdoors with optimal orientation. The solar generator must have characteristics, which are consistent with the nominal input ratings of the inverter. For a clear sky day the following parameters are recorded each 5 min: input current, input voltage, output current, output voltage, power factor, module temperature, and incident solar radiation. Repeat the test for a-Si modules. From the measured data the inverter energy efficiency, standby losses, start up voltage, start up power and stop voltage can be extracted. Comparing the measured DC current and voltage with the theoretical values can evaluate the MPP tracking. Theoretical values can be calculated from the connected module(s) characteristics and the measured values for incident solar radiation and cell temperature.

Appendix C

Losses and Efficiency

The topic for this appendix is to develop equations for the power losses in the used components. The losses included in the inverters can be broken down to:

C.1 Conduction Losses in Resistive Elements

The conduction losses in capacitors, magnetics, resistors, and semiconductors may be calculated as:

$$P_{device,cond} = r_{(on)} \cdot \underbrace{\left(\sqrt{\frac{1}{T}\int i_d{}^2 \, dt} \right)^2}_{I_d} + U_0 \cdot \underbrace{\frac{1}{T}\int i_d \, dt}_{\langle I_d \rangle}, \tag{C.1}$$

where $r_{(on)}$ is the resistance in the device, i_d is the instantaneous current through the device, U_0 is the voltage drop across the PN junction (if any) and T is the time of integration.

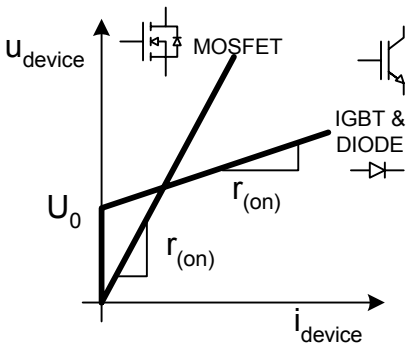


Figure C.1. Typical static characteristics of a power MOSFET, an IGBT and a power diode. The voltage drop over the IGBT / MOSFET is also a function of the applied control voltage.

C.2Switching Losses in MOSFETs and Diodes

C.2.1 MOSFET [60], [61]

The conduction losses in a MOSFET are given by (C.1), and the switching losses are calculated next. The losses in a MOSFET (in series with a freewheeling diode, cf. Figure C.2-a) can be broken down into three parts: a part originating from the gate-circuit; another part from normal switching (turning on and off); and finally a part generated by the reverse-recovery phenomena within the freewheeling diode.

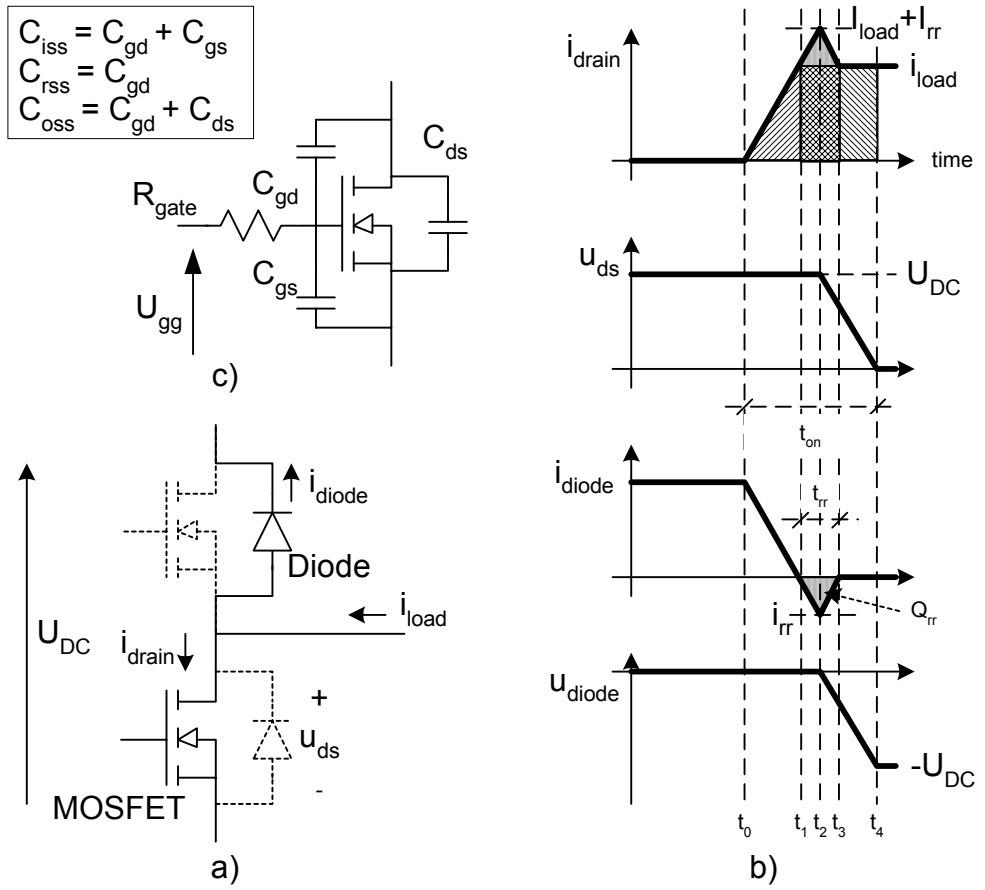


Figure C.2. a) The investigated circuit, composed by a MOSFET in series with a freewheeling diode. b) Transient turn-on waveforms for a MOSFET with freewheeling diode. c) Circuit model for MOSFETs for transient analysis.

The gate circuit loss is given as:

$$P_{MOSFET,gate} = Q_{gate} \cdot U_{gs} \cdot f_{sw}, \tag{C.2}$$

where Q_{gate} is the applied charge to the gate circuit at each switching, U_{gs} is the steady-state gate-source voltage applied to the gate circuit, and f_{sw} is the switching frequency. The power loss associated with the switching is given by:

$$P_{MOSFET,SW} = f_{sw} \cdot \int_0^{T_{sw}} u_{ds} \cdot i_d \; dt \,, \tag{C.3}$$

where u_{ds} is drain-source voltage across the MOSFET, and i_d is the drain current through the MOSFET. Assuming that the drain current increases during t_0 to t_1, no reverse-recovery, and that the drain-source voltage decreases during time t_3 to t_4, (C.3) can be simplified to:

$$P_{MOSFET,SW} \approx \langle I_{load} \rangle \cdot \langle U_{DC} \rangle \frac{t_{ri} + t_{fv} + t_{rv} + t_{fi}}{2} \cdot f_{sw} \tag{C.4}$$

where $<I_{load}>$ is the average load current during the commutation sequence, $<U_{DC}>$ is the average DC-link voltage across the MOSFET during the commutation sequence, $t_{on} = t_{ri} + t_{fv}$ and $t_{off} = t_{rv} + t_{fi}$ is the amount of time it takes for the MOSFET to turn-on and turn-off, respectively. The duration t_{on} is defined in Figure C.2-b as $(t_4-t_3) + (t_1-t_0)$.

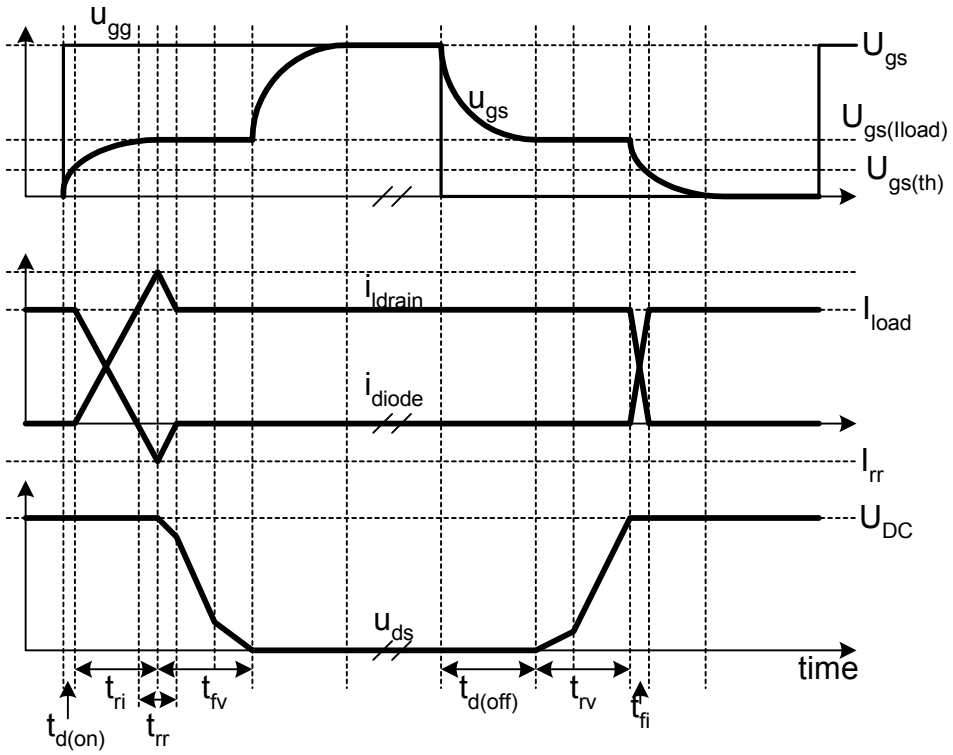


Figure C.3. Turn-on and turn-off voltage and current waveforms of a MOSFET in series with a freewheeling diode [60].

Next follows the equations for the different periods of the switching sequence. A complete turn-on and turn-off cycle for a MOSFET, together with a freewheeling diode, is depicted in Figure C.3, with all currents, voltages, and times defined [60], see also Figure C.2-c.

The signal from the gate drive IC goes high at time zero, causing the gate-source voltage to rise according to

$$u_{gs} = U_{gs} \cdot \left(1 - \exp\left(\frac{-t}{\tau_{on}}\right)\right), \begin{cases} \tau_{on(HV)} = R_{gate(on)} \cdot C_{iss} \ (for\ u_{ds} > U_{gs(Iload)}) \\ \tau_{on(LV)} = R_{gate(on)} \cdot C_{iss} \ (for\ u_{ds} < U_{gs(Iload)}) \end{cases} \tag{C.5}$$

where C_{iss} is the MOSFET input capacitance, and $R_{gate(on)}$ is the turn-on gate resistance. During the first part of the turn-on sequence, the voltage across the MOSFET equals the DC-link voltage, which involves that the input capacitance is low. The turn-on delay time can be expressed as:

$$t_{d(on)} = -\tau_{on(HV)} \cdot \ln\left(1 - \frac{U_{gs(th)}}{U_{gs}}\right) \tag{C.6}$$

where $U_{gs(th)}$ is the MOSFET threshold voltage. The voltage across the MOSFET is still equal to the DC-link voltage. The current rise time is given by:

$$t_{ri} = -\tau_{on(HV)} \cdot \left(\ln\left(1 - \frac{U_{gs(Iload)}}{U_{gs}}\right) - \ln\left(1 - \frac{U_{gs(th)}}{U_{gs}}\right)\right) \tag{C.7}$$

where $U_{gs(Iload)}$ is the gate-source voltage at which the MOSFET is conducting the full load current (operating in the active region), given as:

$$U_{gs(Iload)} = \frac{I_{load}}{g_{fs}} + U_{gs(th)} \tag{C.8}$$

where g_{fs} is the transconductance of the MOSFET. The fall time for the voltage across the MOSFET is divided into two parts. One at which the drain-source voltage is higher than the gate-source voltage, and one where the opposite is true. The voltage fall times are given as:

$$\begin{aligned} t_{fv(HV)} &= \frac{U_{DC} - U_{gs(Iload)}}{U_{gs} - U_{gs(Iload)}} \cdot R_{gate(on)} \cdot C_{rss} \ (for\ u_{ds} > u_{gs(iload)}) \\ t_{fv(LV)} &= \frac{U_{gs(Iload)}}{U_{gs} - U_{gs(Iload)}} \cdot R_{gate(on)} \cdot C_{rss}, (for\ u_{ds} < u_{gs(iload)}) \\ t_{fv} &= t_{fv(HV)} + t_{fv(LV)} \end{aligned} \tag{C.9}$$

where C_{rss} is the reverse transfer capacitance.

The turn-off sequence is almost identical to the reverse of the turn-on. The signal from the gate drive IC goes low at time zero, causing the gate-source voltage to fall according to:

$$u_{gs} = U_{gs} \cdot \exp\left(\frac{-t}{\tau_{off}}\right), \begin{cases} \tau_{off(LV)} = R_{gate(off)} \cdot C_{iss} \ (for\ u_{ds} < u_{gs(iload)}) \\ \tau_{off(HV)} = R_{gate(off)} \cdot C_{iss} \ (for\ u_{ds} > u_{gs(iload)}) \end{cases} \tag{C.10}$$

where $R_{gate(off)}$ is the turn-off gate resistance. During the first part of the turn-off sequence, the voltage across the MOSFET equals $r_{ds(on)} \cdot I_{load}$, which involves that input capacitance is high. The turn-off delay is expressed as:

$$t_{d(off)} = -\tau_{off(LV)} \cdot \ln\left(\frac{U_{gs(Iload)}}{U_{gs}}\right). \tag{C.11}$$

The rise time for the voltage across the MOSFET is also divided into two parts. One at which the drain-source voltage is lower than the gate-source, and one where the opposite is true. The voltage rise times are given as:

$$t_{rv(LV)} = R_{gate(off)} \cdot C_{rss} \ (for\ u_{ds} < u_{gs}) \tag{C.12}$$
$$t_{rv(HV)} = \frac{U_{DC} - U_{gs(Iload)}}{U_{gs(Iload)}} \cdot R_{gate(off)} \cdot C_{rss} \ (for\ u_{ds} > u_{gs})$$
$$t_{rv} = t_{rv(LV)} + t_{rv(HV)}$$

And finally, the current fall time is given by:

$$t_{fi} = -\tau_{off(HV)} \cdot \ln\left(\frac{U_{gs(th)}}{U_{gs(Iload)}}\right). \tag{C.13}$$

The reverse-recovery of the freewheeling diode imposes an additional current in the MOSFET (only during the MOSFET turn-on transient). The correct waveform of the drain-source voltage starts to decrease at t_2 when reverse-recovery is present, cf. Figure C.2-b. However, the voltage is assumed to start decreasing at t_3, in order to lighten the calculations and parameter extraction. This involves an over-estimate of the RR associated loss. The additional loss from the reverse-recovery is given as:

$$P_{MOSFET,RR} = \left(\langle I_{load} \rangle \cdot t_{RR} + Q_{RR}\right) \cdot \langle U_{DC} \rangle \cdot f_{sw}, \tag{C.14}$$

where Q_{RR} is the charge removed from the diode during the reverse-recovery, and t_{RR} is the duration of the reverse-recovery, defined as t_3-t_1.

C.2.2 Diode

The reverse-recovery also includes losses in the diode. Once again, to simplify the calculations, the voltage across the diode is now assumed to increase during t_2 to t_3. This also involves an over-estimate of the loss. The switching loss in the diode is:

$$P_{diode,RR} = I_{RR} \cdot \langle U_{DC} \rangle \cdot \frac{t_{rr} \cdot s}{6 \cdot (s+1)} \cdot f_{sw}, \tag{C.15}$$

where s is the diode snappiness factor, defined as: $s = (t_3\text{-}t_2) / (t_2\text{-}t_1)$ in Figure C.2-b. The snappiness factor is large for soft reverse-recovery diodes, which show higher losses and lower EMI than abrupt diodes with a smaller snappiness factor.

The switching losses in a leg in the DC-AC inverter (two MOSFETs with freewheeling diodes) arises from two times hard switching (two times loss-less soft switching) and one time reverse recovery losses during each switching period. Hence, the switching losses in a leg are given as:

$$P_{leg} = 2 \cdot P_{MOSFET,SW} + P_{MOSFET,RR} + P_{diode,RR}\ . \tag{C.16}$$

C.2.3 Parameter Extraction

The parameters used in the equations above must be determined from the respective datasheets. The gate charge, Q_{gate}, the MOSFET capacitances at low and high drain-source voltage, C_{iss} and C_{rss}, the gate-source threshold voltage, $U_{gs(th)}$, and the transconductance, g_{fs}, are readily available from the datasheets. All the other parameters must be extracted, they are: t_{rr}, Q_{rr}, and s, since they are only listed for a single operating point in most datasheets.

Both the reverse-recovery time and charge are proportional to the breakdown voltage of the diode [60]. Thus, the diodes used for the calculations should be divided into different voltage classes. Besides this, they are also related to the load current and the rate-of-change-of-current, dI_R / dt, during the MOSFET turn-on [60]:

$$t_{rr} = k_{trr} \cdot \sqrt{\frac{\langle I_{load} \rangle}{dI_R / dt}}, \tag{C.17}$$

$$I_{rr} = k_{irr} \cdot \sqrt{\langle I_{load} \rangle \cdot dI_R / dt}, \tag{C.18}$$

where k_{trr} and k_{irr} are some constant, which must be extracted from the data in the datasheets.

The rate of change in the current is given as

$$\frac{dI_R}{dt} = \frac{I_{load}}{t_{ri}}. \tag{C.19}$$

The reverse-recovery charge can be estimated from Figure C.2-b as:

$$Q_{rr} \approx ½ \cdot t_{rr} \cdot I_{rr}, \tag{C.20}$$

by geometry.

C.3 Components Applied in Chapter 4

The parameters for the components for estimating the power losses are given as:

- PV-side MOSFET (Vishay SUP60N06-18): 60 V, 60 A, $R_{ds(on)}$: 18 mΩ, $V_{gs(th)}$: 3.0 V, $C_{rss(LV)}$: 500 pF, $C_{rss(HV)}$: 100 pF, $C_{iss(HV)}$: 2.2 nF, g_{fs}: 33 Ω^{-1}.
- PV-side MOSFET (Intersil RFP40N10): 100 V, 40 A, $R_{ds(on)}$: 40 mΩ, $V_{gs(th)}$: 3.0 V, $C_{rss(LV)}$: 1000 pF, $C_{rss(HV)}$: 100 pF, $C_{iss(HV)}$: 2.8 nF, g_{fs}: 33 Ω^{-1}.
- PV-side MOSFET (IRF IRFB31N20D): 200 V, 31 A, $R_{ds(on)}$: 82 mΩ, $V_{gs(th)}$: 4.3 V, $C_{rss(LV)}$: 1000 pF, $C_{rss(HV)}$: 80 pF, $C_{iss(HV)}$: 2.4 nF, g_{fs}: 17 Ω^{-1}.
- PV-side MOSFET (Fuji 2SK3554-01): 250 V, 37 A, $R_{ds(on)}$: 100 mΩ, $V_{gs(th)}$: 4.0 V, $C_{rss(LV)}$: 1000 pF, $C_{rss(HV)}$: 15 pF, $C_{iss(HV)}$: 2.0 nF, g_{fs}: 16 Ω^{-1}.
- PV-side MOSFET (Intersil NDP6060): 60 V, 48 A, $R_{ds(on)}$: 25 mΩ, $V_{gs(th)}$: 3.0 V, $C_{rss(LV)}$: 500 pF, $C_{rss(HV)}$: 150 pF, $C_{iss(HV)}$: 1.2 nF, g_{fs}: 19 Ω^{-1}.
- PV-side MOSFET (IRF RFZ34E): 60 V, 28 A, $R_{ds(on)}$: 42 mΩ, $V_{gs(th)}$: 3.0 V, $C_{rss(LV)}$: 200 pF, $C_{rss(HV)}$: 80 pF, $C_{iss(HV)}$: 680 pF, g_{fs}: 7.6 Ω^{-1}.
- PV-side MOSFET (IRF IRF3315): 150 V, 27 A, $R_{ds(on)}$: 70 mΩ, $V_{gs(th)}$: 3.0 V, $C_{rss(LV)}$: 1000 pF, $C_{rss(HV)}$: 160 pF, $C_{iss(HV)}$: 1300 pF, g_{fs}: 11.4 Ω^{-1}.

- PV-side capacitor: 2.2 mF, 50 V, ESR = 58 mΩ.
- DC-link capacitor: 68 µF, 160 V, ESR = 1.50 Ω.
- DC-link capacitor: 33 µF, 450 V, ESR = 1.60 Ω.
- Resonant capacitor: 820 nF, 160 V, ESR = $30 \cdot 10^{-9} \cdot \pi \cdot f^2 \cdot C$
- Grid-side MOSFET (ST Microelectronics STP3NB100FP): 1000 V, $R_{ds(on)}$: 5.4 Ω.
- Grid-side MOSFET (IRF IRFI820G): 500 V, $R_{ds(on)}$: 3.0 Ω.
- Grid-side MOSFET (Infineon SPB02N60S5): 600 V, 1.8 A, $R_{ds(on)}$: 2.7 Ω, $V_{gs(th)}$: 4.5 V, $C_{rss(LV)}$: 40 pF, $C_{rss(HV)}$: 4.4 pF, $C_{iss(HV)}$: 240 pF, g_{fs}: 1.4 Ω^{-1}.
- Rectifying diode (ST Microelectronics STTA206S): 600 V, 2 A, U_F: 1.3 V, t_{rr}: 50 ns, I_{rr}: 2.0 A.

Appendix D

Cost Estimation

The relationship between cost and ratings of the power electronic components is analyzed in this appendix.

D.1 Magnetics

A survey within different core-types (EFD, ETD, UI, EI, etc.) made from ferrite, shows that the cheapest available type is the ETD. The core material is selected as the FERROXCUBE 3C90, which is easily available for this survey. The two measures of core size are given as:

$$K_{g,Fe} = \frac{W_A \cdot (A_C)^{(2\cdot(\beta-1)/\beta)}}{MLT \cdot l_m^{(2/\beta)}} \cdot \underbrace{\left[\left(\frac{\beta}{2}\right)^{\left(\frac{-\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right]^{\left(\frac{\beta+2}{-\beta}\right)}}_{=0.294 \text{ for } \beta=2.55}, \tag{D.1}$$

$$K_g = \frac{{A_C}^2 \cdot W_A}{MLT}, \tag{D.2}$$

where $K_{g,Fe}$ and K_g are the core geometrical constants [61]. A_C is core cross-sectional area, W_A is the core window area, l_m is the magnetic length, MLT is the mean length per turn, and β is a (ferrite) material coefficient. These measures are also defined in appendix E, design of magnetics, based on electrical specification and can thus be used to select a proper core size.

Table D.1. Price comparison of five magnetics. Note that the selected core material is 3C90, and not 3F3 as designed for, since they were not available. Prices from Farnell-InOne, exclusive of VAT, fees, and shipping, third quarter of 2004 [Online]. The prices in brackets for the EFD cores are estimated on base on the size of the three ETD cores.

Type	Core geometrical constant		Price per part (DKK)			Total (DKK)
3C90	K_g [cm^5]	$K_{g,Fe}$ [cm^x]	500 Bobbin	1000 Core	1000 Clips	500 Magnetics
EFD 25	0.029	0.0033	15.07	6.52	1.46	31.03 (12.16)
EFD 30	0.047	0.0041	14.78	8.12	2.21	35.44 (18.35)
ETD 29	0.104	0.0081	9.12	6.81	1.32	25.38
ETD 34	0.193	0.0115	17.09	7.25	1.46	34.51
ETD 39	0.401	0.0173	16.52	10.87	1.61	41.48

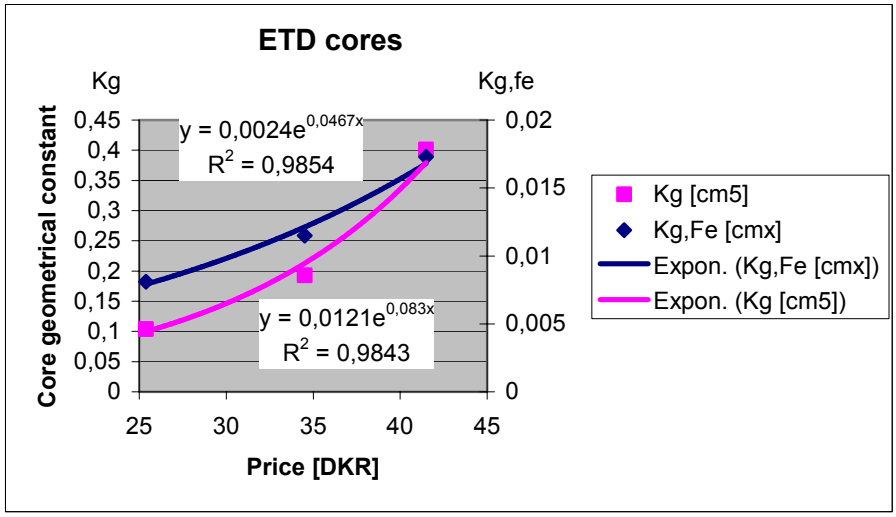


Figure D.1. Comparison of three magnetics based on the ETD29…39 cores.

D.2 Electrolytic Capacitors

The capacitors in this survey are specified to an operational lifetime of 2000 h at 105°C. The results are given in Table D.2 and Figure D.2. A linear regression predicts a price per Joule ($E = ½ \cdot C \cdot U^2$) as:

$$DKR = 3.41 \cdot E + 5.49 \; . \tag{D.3}$$

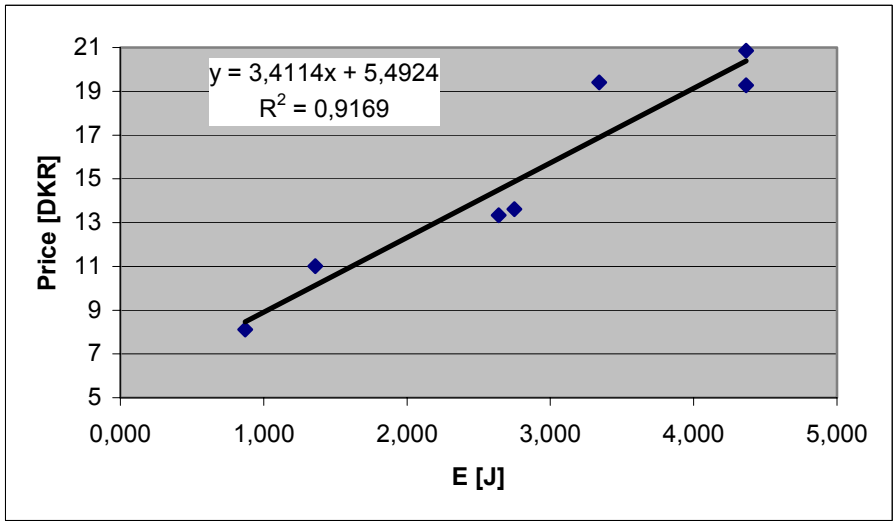


Figure D.2. Comparison of seven electrolytic capacitors for power decoupling.

Table D.2. Price comparison of eight electrolytic capacitors. Prices from Farnell-InOne, exclusive of VAT, fees, and shipping, third quarter of 2004 [Online].

Capacitance [μF]	Break down voltage [V]	Energy [J]	Price [DKK]
2200	50	2.750	13.62
2200	63	4.366	20.86
2200	63	4.366	19.27
68	160	0.870	8.12
68	200	1.360	11.01
33	400	2.640	13.34
33	450	3.341	19.41

D.3 Film Capacitors

The X2 EMI-suppressors film capacitors in this survey are specified to 250 V ac. The results are given in Table D.3 and Figure D.3. A regression predicts a price per nano-Farad as:

$$DKR = 1.52 \cdot \exp(0.0013 \cdot C[nF]) . \quad \text{(D.4)}$$

Table D.3. Price comparison of 18 X2 EMI-suppressing film capacitors. Prices from Farnell-InOne, exclusive of VAT, fees, and shipping, fourth quarter of 2004 [Online].

Capacitance [nF]	Price [DKK]
47	1.45
68	1.45
82	1.45
100	1.45
120	1.67
150	1.88
180	2.01
220	2.17
270	2.54
330	2.90
390	3.12
470	3.33
560	3.55
680	3.77
820	4.35
1000	4.92
1200	7.68
1500	10.44

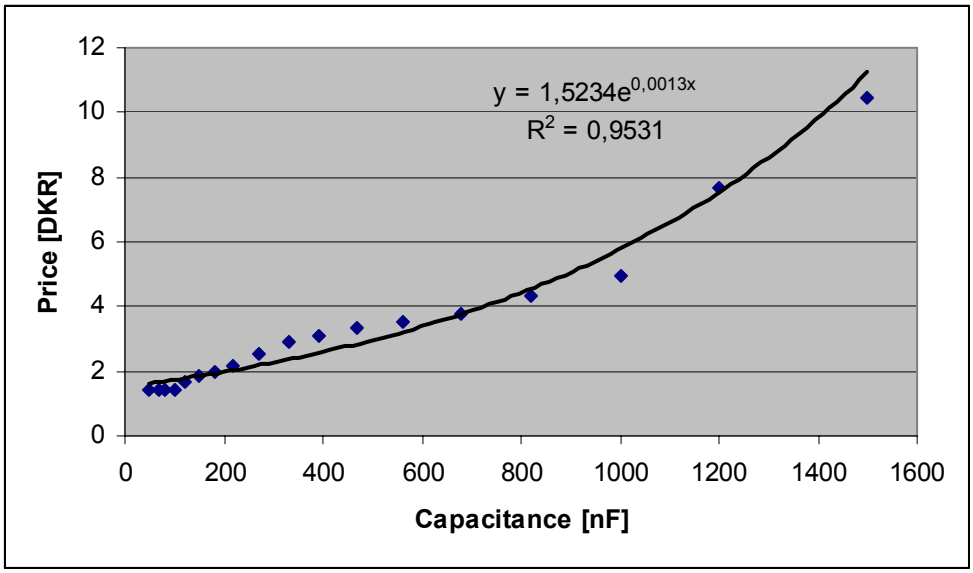


Figure D.3. Comparison of 18 film capacitors for EMI suppressing.

D.4 MOSFETs

In order to lower the statistical uncertainty, the MOSFETs in this survey are grouped according to their location, either on the PV-side or the grid-side. All MOSFETs are housed in a TO-220 encapsulation.

The results for the 43 PV-side MOSFETs are tabulated in Table D.4 and depicted in Figure D.4. A linear regression predicts a price per kVA as:

$$DKR = 1.96 \cdot kVA + 3.80 \,. \tag{D.5}$$

The results for the seven grid-side MOSFETs are tabulated in Table D.5 and depicted in Figure D.5. A linear regression predicts a price per kVA as:

$$DKR = 4.24 \cdot kVA + 1.37 \,. \tag{D.6}$$

Table D.4. Price comparison of 43 MOSFETs for the PV side. Prices from Farnell-InOne, exclusive of VAT, fees, and shipping, third quarter of 2004 [Online].

Type	Manufacturer	Break down Voltage -U_{BR}	Continuous current - I_D	$R_{ds(on)}$	Encapsulation	Ratings [kVA]	Price [DKK]
2SK2173	TOSHIBA	60	50	0.0250	TO-3P	3.0	24.78
2SK2267	TOSHIBA	60	60	0.0150	TO-264	3.6	53.36
2SK2313	TOSHIBA	60	60	0.0150	TO-3P	3.6	34.35
IRFZ44V	IRF	60	55	0.0165	TO-220	3.3	7.54
IRFZ44R	IRF	60	50	0.0280	TO-220	3.0	7.54
IRFZ48R	IRF	60	50	0.0180	TO-220	3.0	19.27
FQP50N06	FAIRCHILD	60	50	0.0220	TO-220	3.0	4.35
FQPF85N06	FAIRCHILD	60	53	0.0100	TO-220F	3.2	10.44
FQA47P06	FAIRCHILD	60	55	0.0260	TO-3P	3.3	12.32
MTP52N06V	ON	60	52	0.0220	TO-220	3.1	12.61

Type	Manufacturer	Break down Voltage -U_{BR}	Continuous current - I_D	$R_{ds(on)}$	Encapsulation	Ratings [kVA]	Price [DKK]
STP55NF06	STM	60	50	0.0150	TO-220	3.0	7.54
STP55NF06FP	STM	60	50	0.0150	TO-220FP	3.0	8.12
STP60NF06	STM	60	60	0.0140	TO-220	3.6	8.40
STP60NE06-16	STM	60	60	0.0160	TO-220	3.6	10.78
RFP50N06	INTERSIL	60	50	0.0220	TO-220	3.0	13.19
SUP60N06-18	VISHAY	60	60	0.0180	TO-220AB	3.6	11.59
IRFZ44E	IRF	60	48	0.023	TO-220AB	2.9	9.71
MTP36N06V	ON	60	32	0.040	TO-220AB	1.9	9.27
MTP50N06V	ON	60	42	0.028	TO-220AB	2.5	11.89
MTP30N06VL	ON	60	30	0.050	TO-220AB	1.8	10.29
2SJ334	TOSHIBA	60	30	0.060	TO-220ISOL	1.8	24.93
2SK2266	TOSHIBA	60	45		TO-220	2.7	11.16
2SK2312	TOSHIBA	60	45	0.025	TO-220ISOL	2.7	26.23
STP45NE06L	STM	60	45	0.028	TO-220	2.7	8.12
STP60NE06-16FP	STM	60	35	0.016	TO-220FP	2.1	12.02
FQPF50N06	FAIRCHILD	60	31	0.022	TO-220FP	1.9	4.78
FQPF65N06	FAIRCHILD	60	40	0.016	TO-220FP	2.4	6.81
STP45NF06L	FAIRCHILD	60	38	0.022	TO-220	2.3	6.95
STP60NE06-16FI	FAIRCHILD	60	35		ISOWATT220	2.1	15.07
RFP30N06LE	INTERSIL	60	30	0.047	TO-220	1.8	7.25
NDP6060L	INTERSIL	60	48	0.025	TO-220	2.9	7.54
NDP6060	INTERSIL	60	48	0.025	TO-220	2.9	7.54
RFZ34E	IRF	60	28	0.042	TO-220AB	1.7	6.23
2SK2232	TOSHIBA	60	25	0.080	TO-220ISOL	1.5	7.25
IRF540	STM	100	28	0.077	TO-220	2.8	5.50
2SK2314	TOSHIBA	100	27	0.130	TO-220	2.7	8.26
IRL540	IRF	100	28	0.077	TO-220	2.8	15.36
IRFB23N15D	IRF	150	23	0.090	TO-220	3.5	9.57
IRF540	IRF	100	28	0.077	TO-220	2.8	19.41
IRF3315	IRF	150	27	0.070	TO-220	4.1	12.46
STP22NE10L	STM	100	22	0.070	TO-220	2.2	4.78
STP24NF10	STM	100	26	0.055	TO-220	2.6	5.65
IRF540N	IRF	100	27	0.052	TO-220	2.7	12.75
RL540N	IRF	100	30	0.044	TO-220	3.0	13.04
IRFI1310N	IRF	100	22	0.036	TO-220	2.2	20.48
IRFP250N	IRF	200	30	0.075	TO-247	6.0	32.90
IRFB23N20D	IRF	200	24	0.100	TO-220	4.8	11.45
IRFB31N20D	IRF	200	31	0.082	TO-220	6.2	14.34
MTP40N10E	ON	100	40	0.040	TO-220	4.0	20.86
RFP40N10	INTERSIL	100	40	0.040	TO-220	4.0	8.40
BUZ345	INFINEON	100	41	0.045	TO-218	4.1	43.47
IRFP150	IRF	100	40	0.055	TO-247	4.0	30.43
STP40NF10L	STM	100	40	0.028	TO-220	4.0	8.12
IRF1310N	IRF	100	41	0.036	TO-220	4.1	22.89
FQA55N25	FAIRCHILD	250	55	0.040	TO-3P	13.8	29.56
IRFP264	IRF	250	38	0.075	TO-247	9.5	59.56
2SK3554-01	FUJI	250	37	0.026	TO-220	9.3	27.82

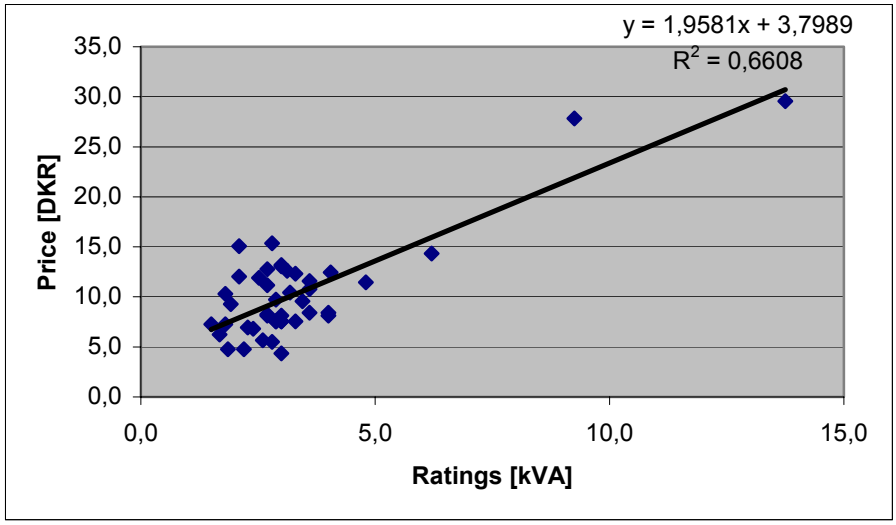


Figure D.4. Comparison of 43 MOSFETs for the PV side.

Table D.5. Price comparison of seven MOSFETs for the grid side. Prices from Farnell-InOne, exclusive of VAT, fees, and shipping, third quarter of 2004 [Online].

Type	Manufacturer	Break down Voltage -U_{BR}	Continuous current - I_D	$R_{ds(on)}$	Encapsulation	Ratings [kVA]	Price [DKK]
STP3NB100	STM	1000	3.0	6.0	TO -220	3.0	13.04
STP3NB100FP	STM	1000	3.0	6.0	TO -220	3.0	15.21
IRFI820G	IRF	500	2.1	3.0	TO -220	1.1	8.40
FQPF4N50	FAIRCHILD	500	2.3	2.7	TO -220	1.2	3.92
PHP2N50E	PHILIPS	500	2.0	5.0	TO -220	1.0	5.22
PHP2N60E	PHILIPS	600	1.9	4.4	TO -220	1.1	6.81
SPB02N60S5	INFINEON	600	1.8	3.0	TO -263	1.1	5.37

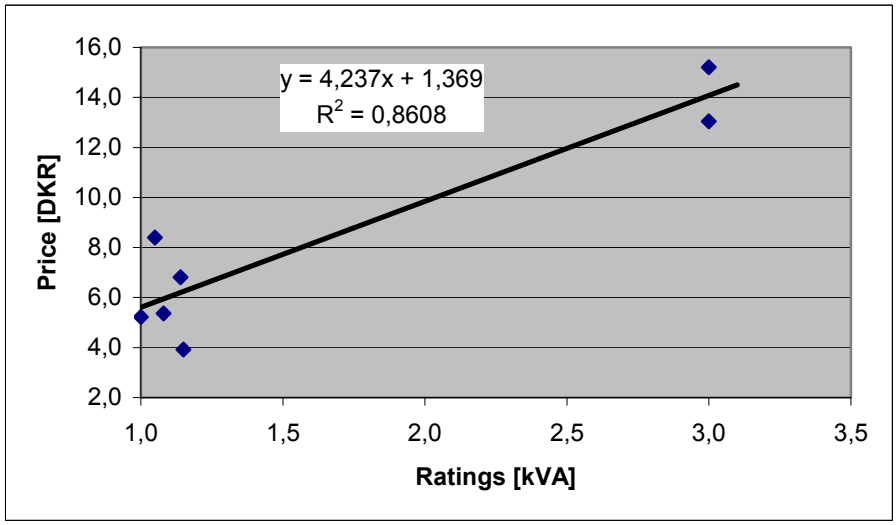


Figure D.5. Comparison of seven MOSFETs for the grid side.

D.5 Diodes

The results for the 17 rectifying diodes are tabulated in Table D.6 and depicted in Figure D.6. A linear regression predicts a price per kVA as:

$$DKR = 1.00 \cdot kVA + 0.67 \,. \tag{D.7}$$

However, it was difficult to locate diodes rated for more than 1200 V. Thus, in the cases where 1350 V and 1460 V diodes are required, two diodes of half the voltage are connected in series.

Table D.6. Price comparison of 17 diodes. Prices from Farnell-InOne, exclusive of VAT, fees, and shipping, third quarter of 2004 [Online].

Type	Manufacturer	Break down Voltage -U_{BR}	Continuous current - I_D	Ratings [kVA]	Price [DKK]
FFPF05U120S	FAIRCHILD	1200	5.0	6.0	4.20
STTA512D	STM	1200	5.0	6.0	6.95
STTA512F	STM	1200	5.0	6.0	8.99
PS3010R	MULTICOMP	1000	3.0	3.0	2.25
BYV96E	PHILIPS	1000	1.6	1.6	1.02
UF5408	VISHAY	1000	3.0	3.0	5.65
FR307	MULTICOMP	1000	3.0	3.0	3.77
BYG21M	VISHAY	1000	1.5	1.5	0.72
HER308G	MULTICOMP	1000	3.0	3.0	3.48
BYV27-600	PHILIPS	600	1.6	1.0	1.38
STTA206S	STM	600	2.0	1.2	4.49
BYV95C	PHILIPS	600	1.6	1.0	1.76
RS2J	VISHAY	600	1.5	0.9	1.48
BYG20J	VISHAY	600	1.5	0.9	0.79
BYT79-500	PHILIPS	500	15.0	7.5	7.25
BYV29-500	PHILIPS	500	9.0	4.5	5.94
BYV34-500	PHILIPS	500	10.0	5.0	6.23

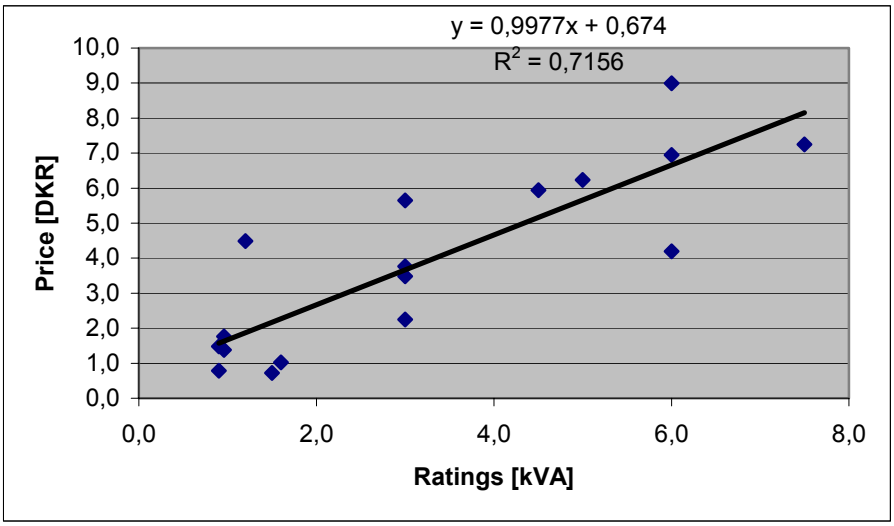


Figure D.6. Comparison of 17 diodes for the rectifier.

Appendix E

Design of Magnetics

The methodology for design of magnetic circuits is presented in this appendix. The procedures are based on [61] with some modifications. The main modification is within the design of transformers and AC-inductors, where the standard Steinmetz equation has been replaced with the modified Steinmetz equation [115], in order to deal with non-sinusoidal excitations.

Eddy current losses in the windings are divided into losses originating from the skin effect, and the proximity effect. The skin effect can be avoided by selecting a conductor (or several strands in parallel if a low resistance is required) with a diameter smaller than the skin depth. Interleaving the windings can mitigate the proximity effect. Both these measures are applied in order to raise the efficiency. Thus, the skin- and the proximity-losses are therefore not concerned. However, interleaving the winding does not decrease the proximity losses much in flyback and SEPIC converters [61], [114].

E.1 Symbol List

DESCRIPTION	SYMBOL	DIMENSION
MAXIMUM OPERATING FLUX DENSITY	B_{max}	[T]
OPTIMUM OPERATING FLUX DENSITY	B_{opt}	[T]
TOTAL DC AND AC MAXIMUM OPERATING FLUX DENSITY	$B_{max,AC+DC}$	[T]
APPLIED VOLT-SECONDS ON THE J^{TH} WINDING	λ_j	[V·S]
NUMBER OF TURNS ON THE J^{TH} WINDING	n_j	[ ]
WINDING RATIO BETWEEN THE PRIMARY AND THE J^{TH} WINDING	N_j	[ ]
APPLIED INSTANTANEOUS VOLTAGE ON THE J^{TH} WINDING	u_j	[V]
RMS VALUE OF APPLIED VOLTAGE ON THE J^{TH} WINDING	U_j	[V]
CORE LOSS	P_{Fe}	[W]
CORE LOSS COEFFICIENT	K_{Fe}	-
CORE LOSS COEFFICIENT	α	-
CORE LOSS COEFFICIENT	β	-
CORE LOSS DENSITY	P_V	[KW/M^3]
VARIABLES USED TO EXTRACT THE CORE LOSS COEFFICIENTS	n, x, y, z, K_1, K_2, K_3	-

EQUIVALENT RE-MAGNETIZING FREQUENCY	f_{eq}	[HZ]
SWITCHING FREQUENCY	f_{sw} (= 1 / T_{sw}), f	[HZ]
RATE OF CHANGE OF FLUX DENSITY	dB / dt	[T/S]
WIRE EFFECTIVE RESISTIVITY	ρ	[Ω·M]
WINDOW FILL FACTOR	K_U	[ ]
DESCRIPTION	SYMBOL	DIMENSION
TOTAL WINDING LOSS	P_{Cu}, $P_{Cu,tot}$	[W]
TOTAL TRANSFORMER LOSS = P_{CU} + P_{FE}	P_{tot}	[W]
RMS VALUE OF CURRENT THROUGH THE J^{TH} WINDING	I_j	[A]
DC CURRENT IN A WINDING	I_{DC}	[A]
WINDOW AREA ALLOCATION FOR THE J^{TH} WINDING	α_j	[ ]
TOTAL RMS WINDING CURRENT, REFERRED TO THE PRIMARY	I_{tot}	[A]
WINDING RESISTANCE	R	[Ω]
CORE TEMPERATURE	T_{core}	[°C]
AMBIENT TEMPERATURE	T_{abm}	[°C]
CORE THERMAL RESISTANCE	$R_{\theta,core}$	[K/W]
CORE GEOMETRICAL CONSTANT	K_g	[m^5]
CORE GEOMETRICAL CONSTANT	$K_{g,Fe}$	-
CORE CROSS SECTIONAL AREA	A_C	[m^2]
CORE VOLUME	V_C	[m^3]
MEAN LENGTH PER TURN	MLT	[m]
CORE WINDOW AREA	W_A	[m^2]
MAGNETIC PATH LENGTH	l_m	[m]
WINDINGS DEPTH	b_W	[m]
WINDINGS HIGHT	h_W	[m]
NUMBER OF INTERFACES BETWEEN THE WINDINGS	P	[ ]
AIR GAP LENGTH	l_g	[m]
WIRE AREA FOR THE J^{TH} WINDING	$A_{W,j}$	[m^2]
DIAMETER FOR THE J^{TH} WINDING	$d_{W,j}$	[ ]
SKIN DEPTH	δ	[m]
AREA CORRESPONDING TO THE SKIN DEPTH	A_δ	[m^2]
PERMEABILITY OF FREE SPACE	μ_0	[H/M]
RELATIVE PERMEABILITY	μ_r	[ ]
INDUCTANCE FACTOR	A_L	[H / $TURNS^2$]
MAGNETIZING INDUCTANCE FOR A TRANSFORMER	L_M	[H]
LEAKAGE INDUCTANCE FOR A TRANSFORMER	L_{lk}	[H]
DESIGNED INDUCTANCE	L	[H]

E.2 Prerequisites

Both the core- and the winding-losses should be taken into consideration when designing AC inductors and transformers. It is assumed that no DC component is present.

E.2.1 Flux Density

The peak flux density generated by the primary winding in a transformer is:

$$B_{\max} = \frac{\lambda_1}{2 \cdot n_1 \cdot A_C}, \tag{E.1}$$

where λ_1 is the applied volt-second during the positive portion of the voltage:

$$\lambda_1 = \int_{t_1}^{t_2} u_1 \, dt. \tag{E.2}$$

E.2.2 Core Loss

The core loss in magnetics is typical estimated by the classical Steinmetz equation, also in [61]. However, when the excitation is non-sinusoidal (as it is with most power electronics), the calculation must be based on the modified Steinmetz equation [115]:

$$P_{Fe} = K_{Fe} \cdot f_{eq}^{\alpha-1} \cdot B_{\max}^{\beta} \cdot V_C \cdot f_{sw}, \tag{E.3}$$

where K_{Fe}, α and β are some parameters depending on the chosen material. V_C is the core volume, and f_{eq} is the equivalent frequency of re-magnetization:

$$f_{eq} = \frac{1}{2 \cdot B_{\max}^{\,2} \cdot \pi^2} \cdot \int_0^{T_{sw}} \left(\frac{dB}{dt} \right)^2 dt, \tag{E.4}$$

where T_{sw} is the period of a switching ($T_{sw} = 1 / f_{sw}$), and dB/dt is the rate-of-change of the flux density. Inserting (E.1) into (E.4) yields a new expression for the equivalent frequency:

$$f_{eq} = \frac{1}{2 \cdot B_{\max}^{\,2} \cdot \pi^2 \cdot n_1^{\,2} \cdot A_C^{\,2}} \cdot \int_0^{T_{sw}} u_1^{\,2} \, dt. \tag{E.5}$$

Equation (E.5) can be further simplified from the definition of the RMS value:

$$f_{eq} = \frac{1}{2 \cdot B_{\max}^{\,2} \cdot \pi^2 \cdot n_1^{\,2} \cdot A_C^{\,2}} \cdot \frac{U_1^{\,2}}{f_{sw}}, \tag{E.6}$$

where U_1 is the RMS value of the applied voltage. Using (E.1) in (E.6) involves:

$$f_{eq} = \frac{2 \cdot U_1^{\,2}}{\pi^2 \cdot f_{sw} \cdot \lambda_1^{\,2}}. \tag{E.7}$$

Examples: A) Sinusoidal excitation of peak 100 V at 25 kHz yields: $U_1 = 70.7$ V, $f_{sw} = 25$ kHz, and $\lambda_1 = 1.27 \cdot 10^{-3}$ V·s, which yields an equivalent frequency of 25 kHz. B) Square-wave excitation of peak 100 V at 25 kHz yields: $U_1 = 100$ V, $f_{sw} = 25$ kHz, and $\lambda_1 = 2.00 \cdot 10^{-3}$ V·s, which yields an equivalent frequency of 20.3 kHz.

The core loss is then given by:

$$P_{Fe} = K_{Fe} \cdot \left(\frac{2 \cdot U_1^{\,2}}{\pi^2 \cdot f_{sw} \cdot \lambda_1^{\,2}} \right)^{\alpha-1} \cdot B_{\max}^{\beta} \cdot V_C \cdot f_{sw}, \tag{E.8}$$

which can be further reduce to:

$$P_{Fe} = K_{Fe} \cdot \left(\frac{2 \cdot U_1^{\,2}}{\pi^2 \cdot \lambda_1^{\,2}} \right)^{\alpha-1} \cdot B_{\max}{}^{\beta} \cdot V_C \cdot f_{sw}{}^{(2-\alpha)}, \tag{E.9}$$

This is where the approach in this thesis differs from the procedure given in [61].

E.2.3 Winding Loss

The winding loss is calculated by:

$$P_{Cu,tot} = \frac{\rho \cdot MLT}{W_A \cdot K_U} \cdot \sum_{j=1}^{J} \frac{I_j^{\,2} \cdot n_j^{\,2}}{\alpha_j}, \tag{E.10}$$

where α_j is the area allocation for the j^{th} winding. The allocation for each winding must be optimized in respect to the total copper loss. It can be shown that the optimum allocation for the k^{th} winding is:

$$\alpha_k = \frac{I_k \cdot n_k}{\sum_{j=1}^{J} I_j \cdot n_j}. \tag{E.11}$$

The total copper loss in (E.10), when applying (E.11), can be further reduced to:

$$P_{Cu} = \left(\frac{\rho \cdot \lambda_1^{\,2} \cdot I_{tot}^{\,2}}{4 \cdot K_U} \right) \cdot \left(\frac{MLT}{W_A \cdot A_C^{\,2}} \right) \cdot \left(\frac{1}{B_{\max}} \right)^2, \tag{E.12}$$

where I_{tot} is equal:

$$I_{tot} = \sum_{j=1}^{J} \frac{n_j}{n_1} \cdot I_j \ . \tag{E.13}$$

E.2.4 Optimum Flux Density

The optimum flux density involves that the total loss is reduced to an absolute minimum, i.e.:

$$\frac{d\,P_{tot}}{d\,B_{\max}} = \frac{d\,(P_{Fe} + P_{Cu})}{d\,B_{\max}} = 0. \tag{E.14}$$

The derivative of the winding loss is:

$$\frac{d\,P_{Cu}}{d\,B_{\max}} = -\left(\frac{\rho \cdot \lambda_1^{\,2} \cdot I_{tot}^{\,2}}{2 \cdot K_U} \right) \cdot \left(\frac{MLT}{W_A \cdot A_C^{\,2}} \right) \cdot \left(\frac{1}{B_{\max}} \right)^3, \tag{E.15}$$

and the derivative of the core loss is:

$$\frac{d\,P_{Fe}}{d\,B_{\max}} = K_{Fe} \cdot \left(\frac{2 \cdot U_1^{\,2}}{\pi^2 \cdot \lambda_1^{\,2}} \right)^{\alpha-1} \cdot V_C \cdot f_{sw}{}^{(2-\alpha)} \cdot \beta \cdot B_{\max}{}^{(\beta-1)}. \tag{E.16}$$

Letting (E.15) equal to (E.16) and solving for the optimum flux density yields:

$$B_{opt} = \sqrt[(2+\beta)]{10^8 \cdot \left(\frac{\rho \cdot {\lambda_1}^2 \cdot {I_{tot}}^2}{2 \cdot K_U}\right) \cdot \left(\frac{MLT}{W_A \cdot {A_C}^2}\right) \cdot \left(\frac{1}{K_{Fe} \cdot \left(\frac{2 \cdot {U_1}^2}{\pi^2 \cdot {\lambda_1}^2}\right)^{(\alpha-1)} \cdot V_C \cdot {f_{sw}}^{(2-\alpha)} \cdot \beta}\right)}. \quad \text{(E.17)}$$

ATTENTION: All parameters must be included in: cm, cm^2, cm^3, Ω·cm, W/cm^3. Example: $\beta = 2.55$, $\rho = 1.72 \cdot 10^{-6}$ Ω·cm, $\lambda_1 = 190 \cdot 10^{-6}$ V·s, $I_{tot} = 44$ A, $K_U = 0.4$, MLT = 6.0 cm, $W_A = 1.23$ cm^2, $A_C = 0.971$ cm^2, $K_{Fe} = 85 \cdot 10^{-9}$ $W/(cm^3 \cdot T^{\beta})$, $U_1 = 15.3$ V, $V_C = 7.64$ cm^3, and $f_{sw} = 50$ kHz. Thus, according to [61] the optimal flux density equals 187 mT, which corresponds to 5.23 turns on the primary side. Whereas the approach applied here yields 206 mT, which corresponds to 4.75 turns on the primary side.

E.3 Transformer Design

E.3.1 Core Size

Start to obtain the nominal operating point and specifications for the transformer. Nominal operating point parameters: applied volt-second λ_1, total current I_{tot}, RMS value of the applied voltage U_1, and switching frequency f_{sw}. Next, select a core type and material, and obtain the following parameters: mean length per turn MLT, winding area W_A, core cross sectional area A_C, core volume V_C, and the material coefficients K_{Fe}, α, and β. Finally, specify the window utilization K_U (equal to 0.4 for transformers), and winding resistivity ρ ($\rho_{Cu} = 23.0 \cdot 10^{-9}$ Ω·m at 100 °C).

A procedure is given in [61] for selecting a proper core size. The core geometrical constant for a given core, size and material, is:

$$K_{g,Fe} = \frac{W_A \cdot (A_C)^{(2\cdot(\beta-1)/\beta)}}{MLT \cdot {l_m}^{(2/\beta)}} \cdot \underbrace{\left[\left(\frac{\beta}{2}\right)^{\left(\frac{-\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)}\right]^{\left(\frac{\beta+2}{-\beta}\right)}}_{=0.294 \text{ for } \beta=2.55}, \quad \text{(E.18)}$$

where l_m is the mean magnetic length. The required core geometrical constant for a given application is (in cm^x):

$$K_{g,Fe} = \frac{\rho \cdot {\lambda_1}^2 \cdot {I_{tot}}^2 \cdot \left(K_{Fe} \cdot {f_{sw}}^{\alpha}\right)^{(2/\beta)}}{4 \cdot K_U \cdot {P_{tot}}^{((\beta+2)/\beta)}} \cdot 10^8. \quad \text{(E.19)}$$

Thus, the value in (E.19) based on the application, must be smaller than the value in (E.18) for the selected core, size and material. ATTENTION: In order to get a trustworthy result from (E.19), the term $(K_{Fe} \cdot {f_{sw}}^{\alpha})$ must be inserted in $[W/(cm^3 \cdot T^{\beta})]$, and ρ in [Ω·cm].

However, this procedure does not comply with the novel design-scheme given here. On the other hand, the error is believed to be sufficient small to be neglected.

E.3.2 Evaluate the Selected Core Size

Calculate the optimum flux density from (E.17), and core- and windings-losses from (E.12) and (E.9), respectively. The optimum flux density found in (E.17) must not exceed the saturation flux density. The core temperature can be estimated by conventional thermal analysis as:

$$T_{core} = T_{abm} + R_{\theta,core} \cdot \left(P_{Fe} + P_{Cu}\right), \tag{E.20}$$

where $R_{\theta,core}$ is the thermal resistance. The optimum core temperature for ferrites is usually within 80 °C to 110 °C, optimum in the sense of minimum core loss. Thus, the core temperature should be in the vicinity of 100 °C.

A larger core (or better material) must be selected if the temperature or flux density exceeds the limits. A larger core involves lower losses, lower thermal resistance, and lower flux density.

E.3.3 Primary and Secondary Turns Number

The number of turns on the primary side is given by (E.1) and (E.17):

$$n_1 = \text{ceil}\left(\frac{\lambda_1}{2 \cdot B_{opt} \cdot A_C}\right), \tag{E.21}$$

and on the secondary side:

$$n_j = n_1 \cdot \left(\frac{n_j}{n_1}\right) = n_1 \cdot N_J . \tag{E.22}$$

E.3.4 Area Allocation

The area allocation for each winding is optimized in order to lower the losses, from (E.11) and (E.13):

$$\alpha_j = \frac{n_j \cdot I_j}{n_1 \cdot I_{tot}}, \tag{E.23}$$

E.3.5 Windings

The wire size is calculated as:

$$A_{W,j} \le \frac{\alpha_j \cdot K_U \cdot W_A}{n_j}, \tag{E.24}$$

$$d_{W,j} = \sqrt{\frac{4 \cdot A_{W,j}}{\pi}}. \tag{E.25}$$

The wire must be split up into several parallel strands (Litz-wire) if the diameter in (E.25) is larger than one skin-depth [61], in order to lower the skin- and proximity-effects. However, [60] claims that it is sufficient to apply Litz-wire if the diameter is larger than two times the skin-depth:

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu_0 \cdot f}}, \tag{E.26}$$

$$d_W \le \delta, \quad Erickson$$

$$d_W \le 2 \cdot \delta, \quad Mohan$$

The number of strands, and their area (computed from the skin depth) are then (by using the result in [60]):

$$n_{W,j} \le \frac{A_{W,j}}{A_\delta}, \tag{E.27}$$

$$A_\delta = \frac{\rho}{\mu_0 \cdot f}. \tag{E.28}$$

E.3.6 Inductances

Finally, the magnetizing and leakage [60] inductances are estimated as:

$$L_M = A_L \cdot {n_1}^2 = \frac{\mu_0 \cdot \mu_r \cdot A_C \cdot {n_1}^2}{l_m}, \tag{E.29}$$

$$L_{lk} \approx \frac{\mu_0 \cdot MLT \cdot b_W \cdot {n_1}^2}{3 \cdot P^2 \cdot h_W}, \tag{E.30}$$

where A_L is the inductance factor, b_W is the depth of the windings, h_W is the height of the windings, and P is the number of interfaces between the windings.

E.4 AC Inductor

The AC inductor is applied in e.g. resonant converters, where both the winding- and core-losses are significant. In other words, the high frequency component of the flux density is large. The AC inductor design is based on the same methodology as the transformer design.

E.4.1 Core Size

Start to obtain the nominal operating point and specifications for the AC inductor. Nominal operating point parameters: inductance L, applied volt-second λ, RMS value of the current I_L, RMS value of the applied voltage U, and switching frequency f_{sw}. Next, select a core type and material, and obtain the following parameters: mean length per turn MLT, winding area W_A, core cross sectional area A_C, core volume V_C, and the material coefficients K_{Fe}, α, and β. Finally, specify the window utilization K_U (0.6 for inductors), and winding resistivity ρ.

The required core geometrical constant for a given applications is (in cm^x):

$$K_{g,Fe} = \frac{\rho \cdot \lambda^2 \cdot I^2 \cdot \left(K_{Fe} \cdot f_{sw}{}^{\alpha}\right)^{(2/\beta)}}{2 \cdot K_U \cdot P_{tot}{}^{((\beta+2)/\beta)}} \cdot 10^8 \,. \tag{E.31}$$

ATTENTION: In order to get a trustworthy result from (E.31), the term ($K_{Fe} \cdot f_{sw}{}^{\alpha}$) must be inserted in [W/(cm^3·T$^{\beta}$)], and ρ in [Ω·cm].

E.4.2 Evaluate the Selected Core Size

The optimum flux density is then computed by (E.17), where I_L is substituted with I_{tot}, U_1 with U, and λ_1 with λ. The optimum flux density must not exceed the saturation flux density. The core- and windings-losses are given by (E.12) and (E.9), respectively, and the core temperature by (E.20).

A larger core (or better material) must be selected, if the temperature or flux density exceeds the limits.

E.4.3 Number of Turns

The number of turns is given by (E.21), where λ_1 is changed to λ.

E.4.4 Air Gap Length

An air gap must typically be included in order to reach the designed inductance:

$$l_g = \frac{\mu_0 \cdot A_C \cdot n^2}{L}. \tag{E.32}$$

The expression for the air gap is only approximate since it neglects fringing flux in the air gab, and adjustment should be applied to reach the specified inductance.

E.4.5 DC Component

Saturation can occur if a DC current, I_{DC}, is present is the windings. The peak flux density when a DC current flows in the windings is:

$$B_{\max,AC+DC} = B_{\max} + \frac{L \cdot I_{DC}}{n \cdot A_C}, \tag{E.33}$$

where B_{max} is the 'normal' peak flux density within the core, given by (E.1).

E.4.6 Wire Size

The wire size is calculated by (E.24) and (E.25), where α_j is omitted, n_j is substituted with n found in section E.4.3, and $d_{W,j}$ is substituted with d_W.

The wire must be split up into several strands in parallel (Litz wire), if the diameter in (E.25) is larger than the skin-depth in (E.26). The number of strands in the Litz wire is given by (E.27) and (E.28), where $n_{W,j}$ is substituted with n_W, and $A_{W,j}$ is substituted with A_W.

E.5 DC Inductor

The greater part of the losses in a DC inductor comes from the windings, and only a small fraction of the losses is generated in the core. In other words, the high frequency component of the flux density is small. Thus, the core loss is not taken into consideration when designing DC inductors.

E.5.1 Core Size

The selected core must have a geometrical constant, K_g, which satisfies:

$$K_g = \frac{{A_C}^2 \cdot W_A}{MLT} \geq \frac{\rho \cdot L^2 \cdot {I_{\max}}^2}{R \cdot K_U \cdot {B_{\max}}^2} = \frac{\rho \cdot L^2 \cdot {I_{\max}}^2 \cdot I^2}{P_{Cu} \cdot K_U \cdot {B_{\max}}^2}. \tag{E.34}$$

where I_{max} is the peak winding current, and I is the RMS winding current.

E.5.2 Air Gap Length

An air gap must be included in order to decrease the flux density within the core:

$$l_g = \frac{\mu_0 \cdot L \cdot {I_{\max}}^2}{A_C \cdot {B_{\max}}^2}. \tag{E.35}$$

The expression for the air gap is only approximate since it neglects fringing flux in the air gab, and adjustment should be applied to reach the specified inductance.

E.5.3 Windings

The number of turns is given as:

$$n = \frac{L \cdot I_{\max}}{A_C \cdot B_{\max}}. \tag{E.36}$$

The design for the windings is similar to that of section E.4.6.

E.6 Parameter Extraction

The parameters K_{FE}, α and β must be extracted from the datasheet. The other core parameters in (E.17), MLT, W_A, A_C, and V_C are all readily available in the datasheet. Coded linear regression analysis is used to get reliable values of the coefficients. The coding is obtained by taking the logarithm on both sides of (E.3) yields (and assuming a sinusoidal excitation):

$$\log(P_V) = \log(K_{Fe}) + \beta \cdot \log(B) + \alpha \cdot \log(f), \tag{E.35}$$

where P_V is the core loss density in kW/m^3 (= mW/cm^3). The linear regression then yields:

$$\begin{bmatrix} n & \sum x & \sum y \\ \sum x & \sum x^2 & \sum x \cdot y \\ \sum y & \sum x \cdot y & \sum y^2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} \sum z \\ \sum z \cdot x \\ \sum z \cdot y \end{bmatrix} = \begin{bmatrix} K_1 \\ K_2 \\ K_3 \end{bmatrix}, \tag{E.36}$$

where n is the number of points in the set data-set, x = log(f), y = log(B), z = log(P_V), K_1 = log(K_{Fe}), $K_2 = \alpha$, and $K_3 = \beta$.

The regression analysis in (E.36) is used on the 3F3 ferrite, with n = 9 points. The data' are presented in Table E.1, together with the results.

Table E.1. Parameter extraction for the FERROXCUBE 3F3 material at 100 °C and sinusoidal excitation. $K_{Fe} = 85.0 \cdot 10^{-6}$, $\alpha = 1.70$, $\beta = 2.55$, RMS error = 29.0.

Number	B_{max} [mT]	F [Hz]	Pv [mW/cm^3]	Estimated [mW/cm^3]	Square error
1	60	100 000	20 (0.02 W/cm^3)	20 (0.020 W/cm^3)	0
2	100	100 000	70 (0.07 W/cm^3)	73 (0.073 W/cm^3)	9
3	200	100 000	500 (0.50 W/cm^3)	429 (0.429 W/cm^3)	5041
4	50	200 000	40 (0.04 W/cm^3)	41 (0.041 W/cm^3)	1
5	100	200 000	200 (0.20 W/cm^3)	238 (0.238 W/cm^3)	1444
6	140	200 000	550 (0.55 W/cm^3)	560 (0.560 W/cm^3)	100
7	30	400 000	40 (0.04 W/cm^3)	36 (0.036 W/cm^3)	16
8	70	400 000	300 (0.30 W/cm^3)	311 (0.311 W/cm^3)	121
9	100	400 000	800 (0.80 W/cm^3)	771 (0.771 W/cm^3)	841

E.7 Data for Selected EFD and ETD 3F3 Cores

Next follows some data' for selected EFD and ETD 3F3 cores. The thermal resistance is calculated on the basis of [60], and the maximum allowable power loss is calculated on the basis of a 40 °C difference between the ambient- and the core hotspot-temperature, based on (E.20). The maximum value of L·Î·I is computed by (E.34), and obtained for $K_U = 0.6$, and $B_{max} = 0.3$ T.

Core type	EFD20	EFD25	EFD30	ETD29	ETD34	ETD39
Cross sectional area - A_C [mm^2]	31.0	58.0	69.0	76.0	97.1	125
Core volume - V_C [mm^3]	1460	3300	4700	5470	7640	11 500
Mean length per turn – MLT [mm]	36.5	46.4	52.9	53.0	60.0	69.0
Core window winding area - W_A [mm^2]	26.4	40.2	52.3	95.0	123	177
Magnetic path length - l_m [mm]	47.0	57.0	68.0	72.0	78.6	92.2
Geometrical constant - K_g [cm^5]	0.007	0.029	0.047	0.104	0.193	0.401
[Geometrical constant - $K_{g,Fe}$ (β = 2.55) [cm^x]	0.0015	0.0033	0.0041	0.0081	0.0115	0.0173
Thermal resistance - $R_{\theta,core}$ [K/W]	53	34	26	24	19	15
Maximum loss for a 40 °C difference between ambient and hotspot temperature [W]	0.76	1.19	1.55	1.68	2.08	2.69
Maximum obtainable value of L·Î·I [H·A^2]	$1.29 \cdot 10^{-3}$	$3.29 \cdot 10^{-3}$	$4.78 \cdot 10^{-3}$	$7.41 \cdot 10^{-3}$	$11.2 \cdot 10^{-3}$	$18.4 \cdot 10^{-3}$

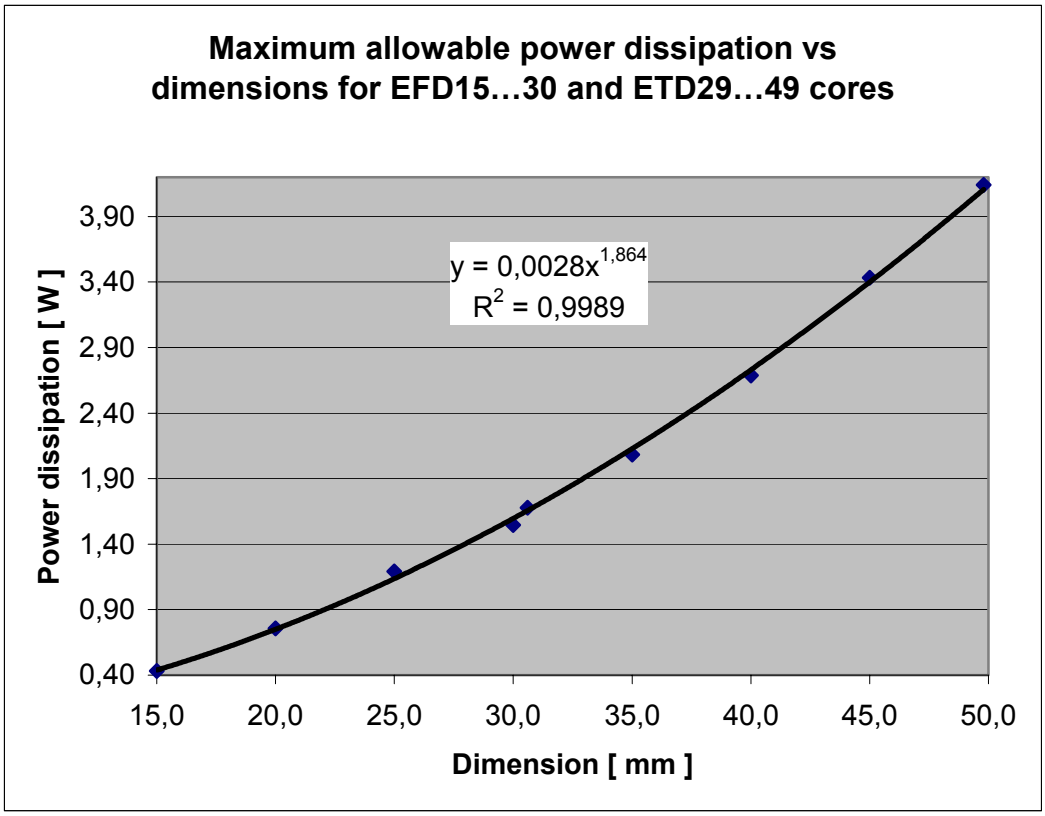


Figure E.21. The maximum power dissipation is computed on the basis of a maximum temperature difference of 40 ℃ between the core and ambient. The thermal resistance is computed on basis of [60]. The dimension on the x-axis is the length (width) of the core.

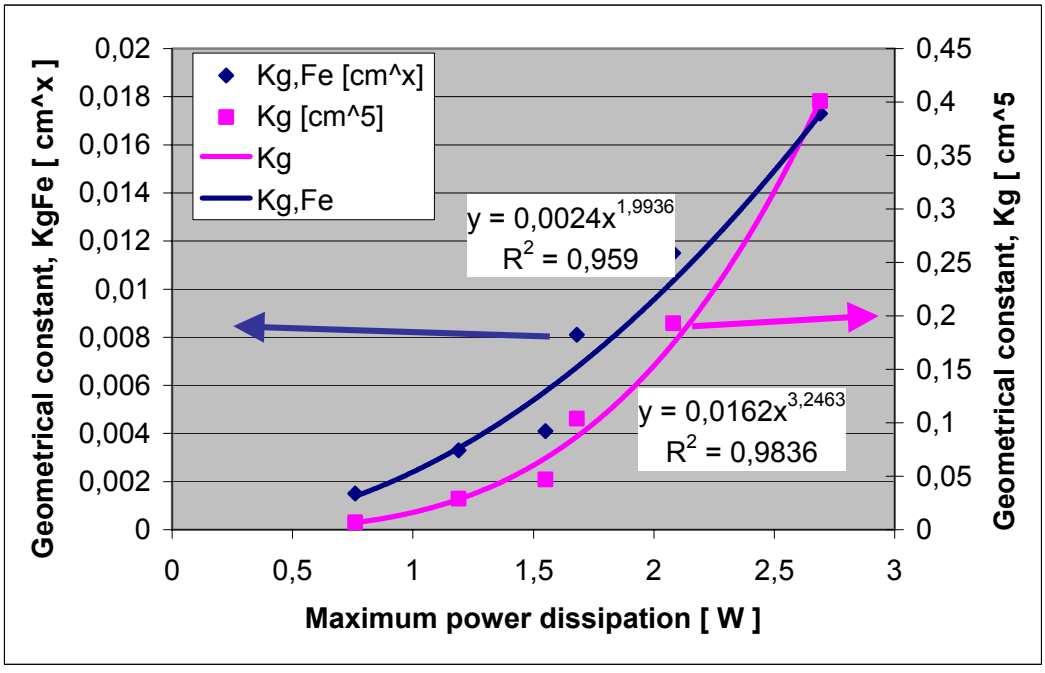


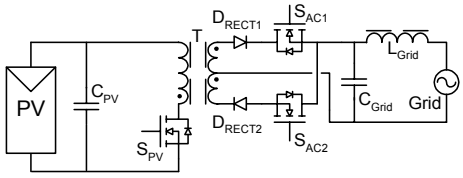
Figure E.2. Core geometrical constants as functions of maximum allowable power dissipation for EFD-20, -25, -30 and ETD-29, -34, and -39 cores.

Appendix F

Design and Ratings for the Inverters in Chapter 4

The inverters in chapter 4 are designed in this appendix. The work is used to estimate their cost and efficiency.

F.1 Topology in Figure 4.7



The magnetizing current is depicted in Figure F.1,

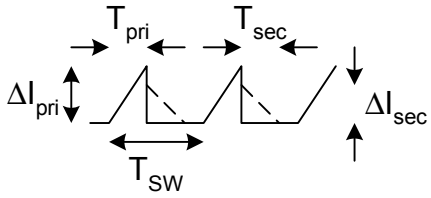


Figure F.1. Magnetizing current.

The current increases from zero to $\hat{I}_{pri}$ during the on period:

$$\hat{I}_{pri} = \frac{U_{PV} \cdot T_{pri}}{L_M}, \tag{F.1}$$

where L_M is the magnetizing inductance and U_{PV} is the voltage across the PV module. The transferred power is given as:

$$P = ½ \cdot L_M \cdot \hat{I}_{pri}^{\,2} \cdot f_{sw}, \tag{F.2}$$

where f_{sw} is the switching frequency. Insertion of (F.1) into (F.2) yields:

$$P = \frac{U_{PV}{}^2 \cdot T_{pri}{}^2 \cdot f_{sw}}{2 \cdot L_M}. \tag{F.3}$$

The amplitude of the current on the secondary side is $\hat{I}_{pri}/N$ where N is the transformer turns ratio, and the magnetizing inductance reflected into the secondary is $L_{M,sec} = L_M \cdot N^2$. Applying this to (F.1) yields the secondary conduction time:

$$T_{\sec} = \frac{\hat{I}_{pri} \cdot L_M \cdot N}{u_{grid}}, \tag{F.4}$$

where u_{grid} is the instantaneous grid voltage. Using the expression for $\hat{I}_{pri}$ in (F.1) results in:

$$T_{\sec} = T_{pri} \cdot \frac{U_{PV} \cdot N}{u_{grid}}. \tag{F.5}$$

The sum of T_{sec} and T_{pri} should not exceed T_{sw} in order to stay in DCM:

$$T_{SW} \geq T_{pri} \cdot \left(1 + \frac{U_{PV} \cdot N}{u_{grid}}\right). \tag{F.6}$$

The transformer turns ratio must be large enough to avoid rectifier operation:

$$N \geq \frac{U_{grid,\max}}{U_{PV,\min}} = \frac{230V \cdot \sqrt{2} \cdot 1.1}{23V} = 15.6, \tag{F.7}$$

thus the turns-ratio is selected to N = 16. Applying this in (F.6) together with the lowest voltages yields:

$$T_{SW} \geq T_{pri} \cdot \left(1 + \frac{U_{PV,\min} \cdot N}{u_{grid,\min}}\right) = T_{pri} \cdot \left(1 + \frac{23 \cdot 16}{230V \cdot \sqrt{2} \cdot 0.85}\right) = T_{pri} \cdot 2.33. \tag{F.8}$$

Thus, the maximum primary conduction time for a given switching frequency is:

$$T_{pri} = \frac{1}{2.40 \cdot f_{sw}}. \tag{F.9}$$

The switching frequency is merely selected to 50 kHz, which involves that T_{pri} must not exceed 8.3 µs. Applying this in (F.3) together with a transferred power of 2·160 W yield a magnetizing inductance of 2.8 µH. The conduction times are evaluated below

U_{grid} / U_{PV}	23 V	45 V
T_{pri} dependent of U_{PV}	8.23 µs	4.21 µs
T_{sec} at 277 V	10.93 µs	10.94 µs
T_{sec} at 358 V	8.46 µs	8.47 µs

Thus, the total conduction time is given in the range from 12.7 µs to 19.2 µs, with a switching time of 20 µs. Thus, DCM is always guaranteed.

Next follows the calculations of the RMS values of the currents inside the circuit. The RMS value of a triangular current, like the magnetizing current, is known to be equal to:

$$I = \hat{I} \cdot \sqrt{\frac{D}{3}}, \tag{F.10}$$

where D is the duty cycle. If, for some reasons, Î and D are not constant (which they are not is the case of a grid connected inverter), the real RMS value is (averaged over a grid period):

$$I = \sqrt{\frac{1}{3 \cdot T_{grid}} \cdot \int_0^{T_{grid}} \hat{I}^2 \cdot D \, dt}, , \tag{F.11}$$

where T_{grid} is the fundamental period for the grid (e.g. 20 ms for European grids). The squared peak current is found from (F.2) together with $p_{grid} = 2 \cdot P_{PV} \cdot \sin^2(\omega \cdot t)$:

$$\hat{I}_{pri}^{\,2} = \frac{4 \cdot P_{PV} \cdot \sin^2(\omega \cdot t)}{L_M \cdot f_{sw}}, \tag{F.12}$$

and the duty cycle is given as $D_{pri} = T_{pri}/T_{sw}$:

$$D_{pri} = \frac{2 \cdot \left|\sin(\omega \cdot t)\right| \cdot \sqrt{f_{sw} \cdot P_{PV} \cdot L_M}}{U_{PV}}. \tag{F.13}$$

Inserting (F.12) and (F.13) into (F.11), rearranging and integrating yields:

$$I_{pri} = \frac{4}{3} \cdot \sqrt{\frac{2 \cdot P_{PV}}{\pi \cdot U_{PV}} \cdot \frac{P_{PV}}{L_M \cdot f_{sw}}}. \tag{F.14}$$

Thus, the maximum RMS value of the primary current equals 16.3 A. The RMS value of the currents on the secondary side is:

$$I_{\mathrm{sec},1} = I_{\mathrm{sec},2} = \frac{I_{pri}}{N \cdot \sqrt{2}}, \tag{F.15}$$

which is equal to 2×0.72 A. The RMS value of the grid current is:

$$I_{grid} = \frac{P_{grid}}{U_{grid}}, \tag{F.16}$$

thus, the HF current through the filter capacitor equals:

$$I_{Cgrid} = \sqrt{\left(\frac{I_{pri}}{N}\right)^2 - I_{grid}^{\,2}}, \tag{F.17}$$

if all of the HF ripple is trapped in the capacitor.

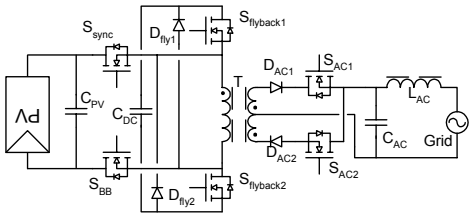
The mean value of the current through the diodes on the secondary side is simply given as:

$$\left\langle I_{\mathrm{sec},1} \right\rangle = \left\langle I_{\mathrm{sec},2} \right\rangle = \frac{P_{grid} \cdot \sqrt{2}}{U_{grid} \cdot \pi}. \tag{F.18}$$

Finally, the voltage-stress on the diodes and MOSFETs on the grid side is:

$$\hat{U}_d = \hat{U}_{grid} + N \cdot \hat{U}_{PV} \qquad \text{(F.19)}$$
$$\hat{U}_{MOSFET} = 2 \cdot \hat{U}_{grid}$$

F.2 Topology in Figure 4.9



The design of the inverter of Figure 4.9 is based on [63].

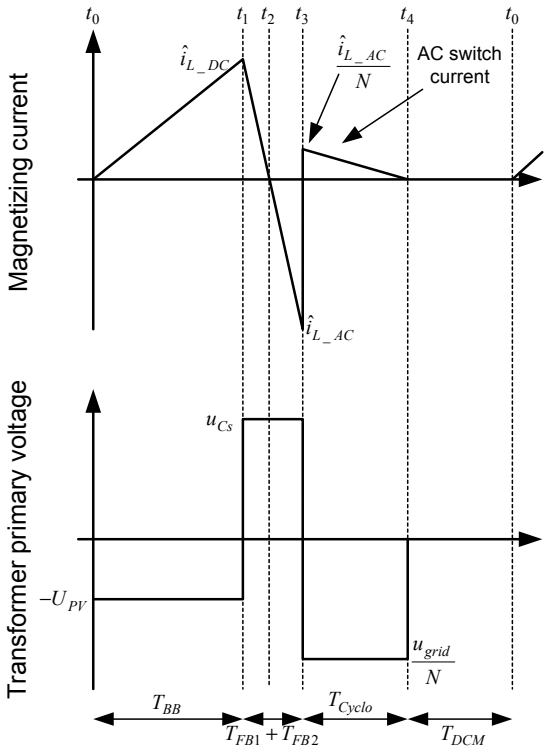


Figure F.2. Waveforms within the inverter in figure 4.9.

The voltage class for transistor S_{BB} (buck-boost) is selected to 250 V, thus the voltage across it must NOT exceed 250 V·0.75 = 188 V. The maximum voltage across the DC-link capacitor is then:

$$\hat{U}_{CDC} = \hat{U}_{BB} - \hat{U}_{PV}\,, \qquad \text{(F.20)}$$

which equals 188 V – 45 V = 143 V. This is also the maximum voltage across the two transistors S_{PV1} and S_{PV2}. The transformer turns ratio is given by:

$$N = \frac{\hat{U}_{Drect} - \hat{U}_{grid}}{\hat{U}_{CDC}}. \tag{F.21}$$

The peak voltage across the diodes in the output stage is selected to 1080 V, as in the previous inverter. Thus, the turns ratio becomes equal to (1080 V – 358 V)/143V = 5.0. Finally, the peak voltage across S_{sync} (synchronous rectifier) equals:

$$\hat{U}_{SPV4} = \frac{\hat{U}_{grid}}{N}, \tag{F.22}$$

which then becomes equal to 72 V, which also in the minimum voltage across the DC capacitor.

The size of this inductor should be determined so that the amount of energy required per switching period can be handled. The total duty cycle for the transistors is:

$$D = \hat{I}_{LM(DC)} \cdot L_M \cdot f_{sw} \cdot \left(\frac{1}{U_{PV}} + \frac{1+\sqrt{2}}{U_{CDC}} + \frac{N}{U_{grid}} \right) < 1, \tag{F.23}$$

and should be smaller than one, in order to stay in DCM. For D_{max} = 0.95, U_{PV} = 23 V, U_{CDC} = 72 V, N = 5.0 and U_{grid} = 230 V ·0.85, the term $\hat{I}_{LM(DC)} \cdot L_M \cdot f_{sw}$ equals 9.26 V. The power drawn from the PV module can be stated as:

$$P_{PV} = \tfrac{1}{2}\left(\hat{I}_{LM(DC)} \cdot L_M \cdot f_{sw}\right) \cdot \hat{I}_{LM(DC)}, \tag{F.24}$$

thus, $\hat{I}_{LM(DC)}$ equals 34.6 A. The switching frequency is selected to 50 kHz, thus the magnetizing inductance equals 5.3 μH.

The RMS value of the currents through the transistors S_{PV3} and S_{PV4} are:

$$I_{SPV3} = I_{SPV4} = I_{pri1} = \sqrt{\frac{2 \cdot I_{PV} \cdot \hat{I}_{LM(DC)}}{3}}, \tag{F.25}$$

where $\hat{I}_{LM(DC)}$ is given as:

$$\hat{I}_{LM(DC)} = \sqrt{\frac{2 \cdot P_{PV}}{L_M \cdot f_{sw}}}. \tag{F.26}$$

The peak magnetizing current then equals 34.7 A, and the RMS value of the current through transistors S_{PV3} and S_{PV4} are 12.7 A. The RMS value of the currents through transistors S_{PV1} and S_{PV2} are:

$$I_{SPV1} = I_{SPV2} = I_{pri2} = \sqrt{\frac{\hat{I}_{LM(DC)}{}^3 \cdot L_M \cdot f_{sw}}{U_{CDC}} \cdot 0.733}, \tag{F.27}$$

under the assumption that U_{CDC} does not contain any AC components. This is however not the case!

Numerical evaluation of (F.27) with $U_{CDC} = 113+30 \cdot \sin(2 \cdot \pi \cdot 100 \cdot t)$ yields:

$$I_{SPV1} = I_{SPV2} = I_{pri2} = \sqrt{\hat{I}_{LM(DC)}{}^3 \cdot L_M \cdot f_{sw} \cdot 7.50 \cdot 10^{-3}}, \tag{F.28}$$

for a capacitor voltage of:

$$u_{CDC} = \sqrt{{U_0}^2 + \frac{P_{PV} \cdot \sin(2 \cdot \omega \cdot t)}{\omega \cdot C_{DC}}}, \quad U_0 = \sqrt{\frac{{U_{\min}}^2 + {U_{\max}}^2}{2}}, \tag{F.29}$$

Applying (F.29) also yields the required C_{DC}:

$$C_{DC} = \frac{P_{PV}}{\omega \cdot \left({\hat{U}_{CDC}}^2 - {U_0}^2\right)}, \tag{F.30}$$

which is computed to 66 µF (U_0 = 113 V).

The numerical evaluation of (F.27) was given in (F.28), with a computed coefficient of $\sqrt{(7.50 \cdot 10^{-3})} = 0.087$, which is close to $\sqrt{(0.733/105)} = 0.084$. Thus, the equation in (F.27) is regarded as being valid, even for large variation in u_{CDC} (here tested with a ripple of 30 V amplitude compared to the DC value of 113 V).

The RMS value of the current through transistors S_{PV1} and S_{PV2} are then computed to 8.5 A.

The RMS value of the primary transformer current is given by combining (F.25) and (F.27): ($I_{pri,1}$ = 12.7 A, $I_{pri,2}$ = 8.5 A)

$$I_{pri} = \sqrt{{I_{pri1}}^2 + {I_{pri2}}^2}, \tag{F.31}$$

which is equal to 15.3 A. The secondary windings currents are computed as in (F.14) and (F.15):

$$I_{\text{sec},1} = I_{\text{sec},2} = \frac{\frac{4}{3} \cdot \sqrt{\frac{P_{PV}}{\pi \cdot U_0}} \cdot \sqrt{\frac{P_{PV}}{L_M \cdot f_{sw}}}}{N}, \tag{F.32}$$

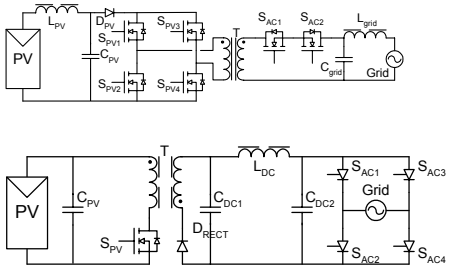
which is evaluated to 0.89 A. The HF current through the filter capacitor equals:

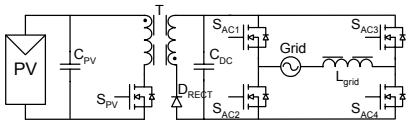
$$I_{Cgrid} = \sqrt{2 \cdot {I_{\text{sec},1}}^2 - {I_{grid}}^2}, \tag{F.33}$$

if all of the HF ripple is trapped in the capacitor, which equals 0.87 A.

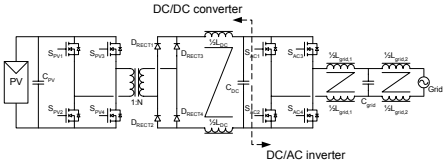
F.3 Topologies of Figures 4.12 to 4.15

The design of the three topologies in Figures 4.12 to 4.15 (excluding Figure 4.13) follows the procedure in section F.1.





F.4 Two Times Full-Bridge Topology



Minimum voltage in the DC link, to inject a sinusoidal current into the grid, is:

$$U_{DC,\min} = \left(U_{grid} + \frac{P_{grid} \cdot Z}{U_{grid}} \right) \cdot \sqrt{2} \,, \tag{F.34}$$

where Z is the impedance of the grid filter and transistors. Assuming 144 W (90% efficiency) at 230·0.85 V in the grid, and an impedance of 5 Ω in the MOSFETs and the grid filter yields a minimum DC-link voltage of 282 V. The amplitude of voltage ripple is given as:

$$\tilde{u}_{DC} = \frac{P_{grid}}{2 \cdot \omega \cdot C_{DC} \cdot U_{DC,0}} \,, \tag{F.35}$$

The voltage set-point is based on the amplitude of the grid voltage, the size of the DC-link capacitor and the power injected into the grid:

$$U_{DC,0} = \frac{U_{DC,\min} + \sqrt{U_{DC,\min}{}^2 + \dfrac{2 \cdot P_{grid}}{\omega \cdot C_{DC}}}}{2} \,, \tag{F.36}$$

The DC-link voltage is limited to 400 V at 10% over-voltage in the grid and 144 W. The minimum voltage is computed by (F.34) to 362 V, and by using (F.35) and (F.36), the required DC-link capacitance is calculated to 33 µF. The DC-link voltage is then defined in the range from 362 V to 398 V, with the set-point equal to 380 V. The transformer turns ratio is given by:

$$N \geq \frac{U_{DC,\max}}{U_{PV,\min}} \,, \tag{F.37}$$

which equals N = 18, for 400 V in the DC-link and 23 V across the PV module. The size of the DC-link inductor is given as:

$$L_{DC} = \frac{\left(U_{PV} \cdot N - U_{DC,0} \right) \cdot U_{DC,0}{}^2}{4 \cdot f_{sw} \cdot N \cdot U_{PV} \cdot P_{CCM}} \,, \tag{F.38}$$

where P_{CCM} is the load point where the inductor is designed to start operating in Continuous Conduction Mode (CCM). The largest value of L_{DC} is reached for maximum U_{PV} and $U_{DC,0}$. The ripple voltage in the DC-link is small at P_{CCM}, thus it is neglected. For a switching frequency of 111 kHz and P_{CCM} = 8 W, the required inductance becomes equal to 20 mH.

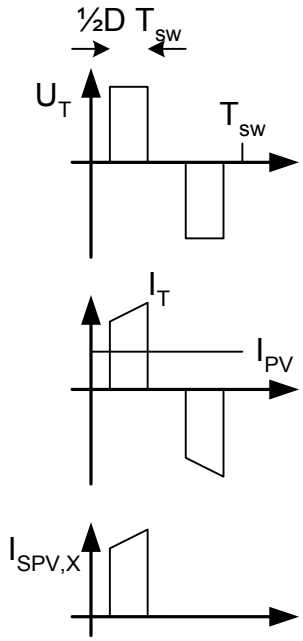


Figure F.3. Waveforms within the DC-DC converter.

The mean amplitude of the transformer current is calculated as:

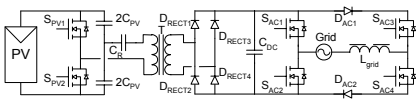
$$\left\langle \hat{I}_T \right\rangle = \frac{I_{PV}}{D}, \tag{F.39}$$

and the RMS value is given as:

$$I_T = \frac{I_{PV}}{D} \cdot \sqrt{D} = I_{PV} \cdot \sqrt{\frac{1}{D}}, \tag{F.40}$$

assuming that the DC-link inductance is large. Thus, the maximum transformer current equals 160 W / 23 V · √(1/0.38) = 11.3 A, and the RMS value of the transistor currents 11.3 A / √2 = 8.0 A.

F.5 Topology of Figure 4.16



The design of the series-resonant DC-DC converter is based on [75]. The load quality factor is computed as:

$$Q_L = \frac{\sqrt{\left(\frac{N \cdot \eta}{M_V}\right)^2 - 1}}{\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}}, \tag{F.41}$$

where η is the initial efficiency, M_V is the DC to DC voltage gain, and ω_0 is the resonant frequency. The maximum voltage gain is M_V = 400 V / 23 V = 17.4, the efficiency is guessed to 0.95. Hence a transformer turns ratio of minimum 18.3 must be adopted, therefore N = 19. The resonant frequency is set to 100 kHz, and the lowest operating frequency to 110 kHz. Thus, the load quality is calculated to 1.45.

The equivalent load seen by the resonant-tank is:

$$R_{eq} = \frac{{U_{DC}}^2}{P_{PV} \cdot \eta} \cdot \frac{8}{(\pi \cdot N)^2}, \tag{F.42}$$

which is evaluated to 1.33 Ω. Finally, the values of the resonant components are:

$$L_R = \frac{Q_L \cdot R_{eq}}{\omega_0}, \tag{F.43}$$

$$C_R = \frac{1}{Q_L \cdot R_{eq} \cdot \omega_0},$$

they are computed to 3.1 μH and 825 nF. A standard capacitor size is 820 nF and L is made equal to 3.0 μH. Thus, the resonant frequency equals 101.5 kHz and the load quality factor: 1.44.

The maximum voltages across the resonant components are:

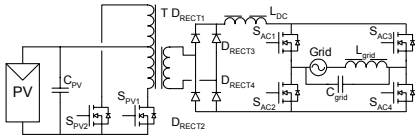
$$\hat{U}_{LR} = \hat{U}_{CR} = \frac{4 \cdot U_{PV} \cdot Q_L}{\pi}, \tag{F.44}$$

which has a maximum of 83 V. The maximum resonant current is:

$$\hat{I}_R = \frac{\hat{U}_{LR}}{\sqrt{\frac{L_R}{C_R}}}, \tag{F.55}$$

which yields 44 A peak and 30 A RMS. This is however NOT the normal operating point, but worst case if the converter is operated at the resonant frequency with a short-circuited output.

F.6 Topology of Figure 4.22



The transformer turns ratio is given by (F.37) to 18. The averaged output voltage from the rectifier is given as $u_{grid} \approx u_{DC} = 2 \cdot U_{PV} \cdot N \cdot D$, where $D \in [0 \ldots 0.5]$ is the duty cycle for each transistor.

The RMS value of the current through the PV side transistors is (assuming a large inductor in the DC-link and constant power flow):

$$I_{SPV,x} = \hat{I}_{SPV,x} \cdot \sqrt{D} \,. \tag{F.56}$$

However, the power flow and duty cycle varies during the period of the grid, for which reason (F.56) must be averaged:

The average current over a switching period in each transistor is given as:

$$\begin{aligned} &\left\langle I_{SPV,x} \right\rangle_{Tsw} = \left\langle I_{PV} \right\rangle \cdot \sin^2(\omega \cdot t) \\ &\Downarrow \\ &\left\langle I_{SPV,x} \right\rangle_{Tgrid} = \tfrac{1}{2} \left\langle I_{PV} \right\rangle \end{aligned} \quad , \tag{F.57}$$

which also is given as:

$$\left\langle I_{SPV,x} \right\rangle_{Tsw} = \hat{I}_{SPV,x} \cdot D \,, \tag{F.58}$$

where D is equal to:

$$D = \hat{D} \cdot \left| \sin(\omega \cdot t) \right|, \quad \hat{D} \in [0 \ldots 0.5], \tag{F.59}$$

Thus, the peak current during a grid period is:

$$\hat{I}_{SPV,x} = \frac{\left\langle I_{PV} \right\rangle \cdot \left| \sin(\omega \cdot t) \right|}{\hat{D}} \,. \tag{F.60}$$

The RMS value of the current through the PV side transistors is:

$$I_{PV,x} = \sqrt{\frac{1}{T} \cdot \int_0^T \hat{I}_{PV,x}{}^2 \cdot D \, dt} \,, \tag{F.61}$$

which can be evaluated to:

$$I_{PV,x} = \left\langle I_{PV} \right\rangle \sqrt{\frac{4}{3\pi \cdot \hat{D}}} \,. \tag{F.62}$$

The maximum RMS value of the current is given for maximum generation and lowest voltage on the PV module and the grid. The RMS values are then evaluated to 7.8 A.

Appendix G

Meteorological Data

Table G.1. Meteorological data, by courtesy of the Danish Technological Institute.

TI/spo **Fil:** **FordelingAaretsTimevaerdier 051201** **Dato:** **06-12-2001**

Azimuth:	0	grd
Tilt:	42	grd
Meteorologi data:	Danish Design Reference Year (DRY)	
Total global solindstråling i horisontalplan iflg. DRY:	1002,39	kWh
Beregnet global solindstråling i modulplan korrigeret for "incidence angle":	1150,36	kWh

Global horisontal solindstråling						Global solindstråling i modulplan korrigeret for "incidence angle "					
Interval nr	Interval-grænse	W/m2	Timer	% af tiden	Kontrol af total energi	Interval nr	Interval-grænse	W/m2	Timer	% af tiden	Kontrol af total energi
			8760		*1004,2*				*8760*	*100%*	*1153,4*
	0	=0	4074	46,51%			0	=0	4074	46,51%	
1	25	>0 <=25	950	10,84%	11,9	1	25	>0 <=25	1016	11,60%	12,7
2	50	>25 <=50	477	5,45%	17,9	2	50	>25 <=50	546	6,23%	20,5
3	75	>50 <=75	360	4,11%	22,5	3	75	>50 <=75	353	4,03%	22,1
4	100	>75 <=100	286	3,26%	25,0	4	100	>75 <=100	253	2,89%	22,1
5	125	>100 <=125	234	2,67%	26,3	5	125	>100 <=125	193	2,20%	21,7
6	150	>125 <=150	202	2,31%	27,8	6	150	>125 <=150	170	1,94%	23,4
7	175	>150 <=175	174	1,99%	28,3	7	175	>150 <=175	139	1,59%	22,6
8	200	>175 <=200	158	1,80%	29,6	8	200	>175 <=200	113	1,29%	21,2
9	225	>200 <=225	150	1,71%	31,9	9	225	>200 <=225	133	1,52%	28,3
10	250	>225 <=250	130	1,48%	30,9	10	250	>225 <=250	126	1,44%	29,9
11	275	>250 <=275	114	1,30%	29,9	11	275	>250 <=275	71	0,81%	18,6
12	300	>275 <=300	118	1,35%	33,9	12	300	>275 <=300	79	0,90%	22,7
13	325	>300 <=325	107	1,22%	33,4	13	325	>300 <=325	84	0,96%	26,3
14	350	>325 <=350	98	1,12%	33,1	14	350	>325 <=350	90	1,03%	30,4
15	375	>350 <=375	104	1,19%	37,7	15	375	>350 <=375	93	1,06%	33,7
16	400	>375 <=400	86	0,98%	33,3	16	400	>375 <=400	74	0,84%	28,7
17	425	>400 <=425	76	0,87%	31,4	17	425	>400 <=425	71	0,81%	29,3
18	450	>425 <=450	79	0,90%	34,6	18	450	>425 <=450	58	0,66%	25,4
19	475	>450 <=475	75	0,86%	34,7	19	475	>450 <=475	66	0,75%	30,5
20	500	>475 <=500	68	0,78%	33,2	20	500	>475 <=500	55	0,63%	26,8
21	525	>500 <=525	69	0,79%	35,4	21	525	>500 <=525	54	0,62%	27,7
22	550	>525 <=550	61	0,70%	32,8	22	550	>525 <=550	59	0,67%	31,7
23	575	>550 <=575	53	0,61%	29,8	23	575	>550 <=575	71	0,81%	39,9
24	600	>575 <=600	57	0,65%	33,5	24	600	>575 <=600	66	0,75%	38,8
25	625	>600 <=625	54	0,62%	33,1	25	625	>600 <=625	49	0,56%	30,0
26	650	>625 <=650	50	0,57%	31,9	26	650	>625 <=650	54	0,62%	34,4
27	675	>650 <=675	42	0,48%	27,8	27	675	>650 <=675	45	0,51%	29,8
28	700	>675 <=700	45	0,51%	30,9	28	700	>675 <=700	30	0,34%	20,6
29	725	>700 <=725	40	0,46%	28,5	29	725	>700 <=725	44	0,50%	31,4
30	750	>725 <=750	41	0,47%	30,2	30	750	>725 <=750	48	0,55%	35,4
31	775	>750 <=775	35	0,40%	26,7	31	775	>750 <=775	49	0,56%	37,4
32	800	>775 <=800	30	0,34%	23,6	32	800	>775 <=800	42	0,48%	33,1
33	825	>800 <=825	25	0,29%	20,3	33	825	>800 <=825	37	0,42%	30,1
34	850	>825 <=850	20	0,23%	16,8	34	850	>825 <=850	34	0,39%	28,5
35	875	>850 <=875	11	0,13%	9,5	35	875	>850 <=875	35	0,40%	30,2
36	900	>875 <=900	6	0,07%	5,3	36	900	>875 <=900	34	0,39%	30,2
37	925	>900 <=925	1	0,01%	0,9	37	925	>900 <=925	34	0,39%	31,0
38	950	>925 <=950	0	0,00%	0,0	38	950	>925 <=950	24	0,27%	22,5
39	975	>950 <=975	0	0,00%	0,0	39	975	>950 <=975	31	0,35%	29,8
40	1000	>975 <=1000	0	0,00%	0,0	40	1000	>975 <=1000	23	0,26%	22,7
					0,0	41	1025	>1000 <=1025	22	0,25%	22,3
					0,0	42	1050	>1025 <=1050	10	0,11%	10,4
					0,0	43	1075	>1050 <=1075	3	0,03%	3,2
					0,0	44	1100	>1075 <=1100	2	0,02%	2,2
					0,0	45	1125	>1100 <=1125	1	0,01%	1,1
					0,0	46	1150	>1125 <=1150	0	0,00%	0,0
					0,0	47	1175	>1150 <=1175	1	0,01%	1,2
					0,0	48	1200	>1175 <=1200	1	0,01%	1,2
					0,0	49	1225	>1200 <=1225	0	0,00%	0,0
					0,0	50	1250	>1225 <=1250	0	0,00%	0,0

The solar irradiation for a Danish Reference Year (DRY) is presented in this appendix, cf. Table G.1.

The data is split up into two sets, the left and the right main-column. The indication for each minor-column is: interval number [-], interval-limit [W/m^2], irradiation [W/m^2], hours of irradiation [h], hours in pro cent of total time [%] and a control of the total energy [kWh]. The control value is given as:

$$E[n] = \tfrac{1}{2} \cdot (irradiation[n] + irradiation[n-1]) \cdot t[n] \cdot \tfrac{1}{1000} \quad [kWh], \tag{G.1}$$

where E[n] is the nth energy, irradiation[n] and irradiation[n-1] is the power limits associated with the nth energy and t[n] is the duration where the nth irradiation is available.

The left column is based on a Danish Design Reference Year (DRY) and shows the expected distribution of global irradiation into a horizontal level. The right column is corrected according to a module pointing towards 0° azimuth (pointing direct toward south) and a tilt of 42°, which gives the maximum annual energy.

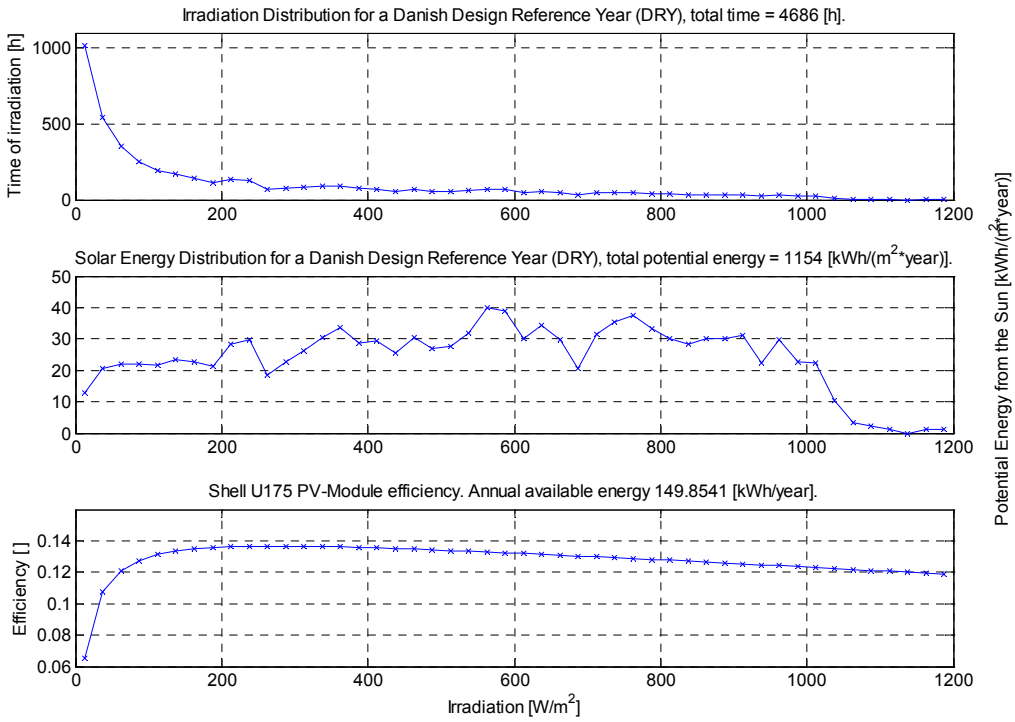


Figure G.1. Meteorological data. Upper) Irradiation probability for a Danish Design Reference Year. Middle) Energy distribution for a Danish Design Reference Year. Lower) Estimated efficiency for the Shell U175 PV module.

The total energy captured per PV module is computed to 150 kWh/m^2 for the Shell Ultra 175 module (72 cells of 12.5 cm × 12.5 cm). The module efficiency is computed for the cell temperatures given in appendix A.

Appendix H

Publications

The papers in this list have all been published in national/international magazines or at conferences, as part of the 'Solcelle Inverter' project. They are available from personal request to S.B. Kjær.

S.B. Kjær, *Solcelleteknologiens status i Danmark*, Elteknik 19. årgang, nr. 2, pp. 18-19, 2002.

S.B. Kjær, J.K. Pedersen, F. Blaabjerg, *Power inverter topologies for photovoltaic modules – a review*, IEEE proc. of the 37th annual industry application conference (IAS'02), vol. 2, pp. 782-788, 2002.

S.B. Kjær, F. Blaabjerg, *Design optimization of a single phase inverter for photovoltaic applications*, IEEE proc. of the 34th power electronics specialists conference (PESC'03), vol. 3, pp. 1183-1190, 2003.

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