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Aalborg University
Institute of Energy Technology

Vestas Wind Systems A/S

Modeling and Comparison of Power Converters for Doubly Fed Induction Generators in Wind Turbines

by

Lars Helle

Dissertation submitted to the Faculty of Engineering and Science at Aalborg University, Denmark, in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering.

Aalborg University, Denmark
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Preface

This dissertation is submitted to the faculty of Engineering and Science at Aalborg University, Denmark, in partial fulfillment of the requirement for the Ph.D-degree in electrical engineering. The work and research documented in the thesis has been carried out at Institute of Energy Technology (IET), Aalborg University, and has been skillfully supervised by associate professor Stig Munk Nielsen. Further, the project was guided by a steering committee consisting of professor and dean Frede Blaabjerg (IET), Anders Rebsdorf, Björn Andresen and Eckardt Siebenthaler - all three former colleagues at Vestas Wind Systems (VWS). I would like to thank all of them for their support and valuable inputs during the project period.

I appreciate the financial support from Vestas Wind Systems and Aalborg University who has funded the project. Also, I want to express my thanks to external professor Paul Thøgersen and Danfoss Drives, for supporting the laboratory test setup.

To all my former colleagues at IET, I owe thanks for their friendship, help and support during the entire project period. Especially I appreciate the fruitful discussions and valuable inputs from Gert K. Andersen, Kim B. Larsen and Allan H. Jørgensen - all of them still good colleagues in my present employment at Vestas wind Systems. Also I owe thanks to Kenneth Krabbe (VWS) for his support during the last phase of the project and for his careful review of the final report.

As a part of the Ph.D-programme, I spent three month visiting professor Prasad Enjeti at Texas A&M University in College Station, U.S. Apart from the technical support and fruitful discussions I would like to thank professor Enjeti for his efforts on helping my family and I to find an apartment in College Station. Special thanks go to Mr. Sangsung Kim, his wife Miwha and Mr Shehab Ahmed for taking good care of my family and I during our stay in College Station.

Finally I am deeply grateful to my wife Tina and our children Oskar, Viktor and Thea for their patience and support, especially during the last years where the project had to be carried out in our spare time.

Sønderup, April 10, 2007

Lars Helle

Making progress is only possible through dead ends.

- Helmut Heissenbüttel

Abstract

During the last decades, renewable energy resources have become an ever increasing part of the world wide power generation and especially energy produced by wind turbines has captured a significant part of this power production. This large penetration of wind power has caused increased focus on the generated power quality and controllability. A consequence of this increased focus has been an ever increased set of requirements formulated in national grid requirement. These requirements has forced wind turbines to evolve from a simple *generator on a stick* into complicated miniature power plants - an evolution which has taken place in a very short time. Further, besides the increased complexity of the wind turbines, the tendency during the late nineties and in the beginning of the new millennium has been, that the size of the turbines has doubled every third year - a progress putting a very high stress on the design engineers employed in the wind industry. Such a progress may force design engineers to adopt common practice from more or less related technologies rather than finding the optimum solution for the specific application. For instance when applying power electronic converters to wind turbines in order to comply with requirements, almost all manufactures has chosen a solution based on the well known two-level voltage source inverter.

The main focus in this thesis is to establish a simple, fast and accurate simulation tool for evaluating different converter topologies for use in a wind turbine based on the doubly-fed induction generator. The objective is to be able to compare the turbine efficiency when using the different converter topologies. The thesis has treated four converter topologies - the commonly used back-to-back two-level voltage source converter, the more un-matured matrix converter, the back-to-back transistor clamped three-level voltage source converter and finally the back-to-back diode clamped three-level voltage source converter.

To evaluate the consequences of applying different converter topologies in a wind turbine application based on the doubly-fed induction generator sufficiently detailed models of the surrounding wind turbine components such as the generator, the gear box, the blades and the transformer have to be derived. The first part of the thesis has treated the modeling approach applied on the surrounding components. The models are wherever possible based on the governing equations with coefficients obtainable from standard data sheets.

The most substantial part of the thesis has been dedicated to the modeling of the considered converter topologies. For each of the considered converters, analytical models has been derived representing the component losses. The component losses within the considered converters depend on the specific turbine design as well as on the operating conditions such as generator speed, generated power, inverter power factor and modulation method. Regarding modulation methods, an in-dept investigation on existing as well as new modulation methods are provided and especially for the latter three converter topologies a lot of efforts have been put into the development of new modulation methods. Actually, for the matrix converter three new modulation schemes has been derived and evaluated, whereas for the three-level inverter topologies four new modulation methods have been proposed. The functionality of most of the developed modulation methods have been demonstrated on an experimental test-setup. Apart from the loss modeling approach, models and methods to estimate the average temperature and peak temperature of the individual components without entering time consuming time-step simulations has been derived - methods applicable to determine the actual design margin for a specific converter design. Although not a part of the thesis these fast predicting thermal models will in a longer term be usable to estimate problems related to power cycling and thermal cycling of the power semiconductors within a specific turbine design. To obtain a fair comparison some initial design guidelines for each of the converters has been outlined concerning components ratings, filter design issues and choice of switching frequency.

Finally, all the developed wind turbine component models have been implemented in a simulation tool *D'rives* enabling a fast and fair comparison of the considered converter topologies. Besides enabling a comparison on the turbine efficiency (and turbine component efficiency), the tool enables an investigation on the actual design margin in terms of determining the component peak temperature for a given load profile. Actually, for a fair comparison, the design margin for each converter should be in the same range. The tool has been demonstrated on selected turbine designs and for the present designs, it appears that the back-to-back transistor clamped three-level voltage source converter actually is the best choice (although insignificant) when considering the turbine efficiency - or more specific the annually generated energy. However as will appear during the thesis, several degrees of freedom exist within the turbine design and clearly, changes within the design may change the results obtained from the present design examples.

Resumé

Gennem de seneste årtier har energiproduktion baseret på vedvarende energikilder udgjort en stadig stigende andel af den samlede globale energiproduktion. I elproduktionen har især vindmøller vist sig at være et næsten konkurrencedygtigt alternativ til traditionel elproduktion - en konkurrencedygtighed, som til stadighed øges. Den stigende udbredelse af vindmøller sammenholdt med den mere eller mindre uforudsigelige natur af vinden har imidlertid bevirket at tilslutningsbetingelserne for vindmøller er skærpet væsentligt - en udvikling som på relativt kort tid har bevirket at vindmøller har udviklet sig fra at være en "simpel generator på en pind" til et kompliceret miniaturekraftværk. Foruden de skærpede tilslutningsbetingelser har tendensen inden for vindmølleudvikling gennem slutningen af halvfemserne og i begyndelsen af de nye årtusinde været at møllestørrelsen er fordoblet hvert tredje år - en udvikling som har holdt vindmølledesignere under et voldsomt pres. Under sådanne forhold tvinges designerne til at adoptere løsninger fra beslægtede fagområder frem for at søge den optimal løsning til netop deres applikation. Eksempelvis har stort set alle fabrikanter valgt at benytte en traditionel to-niveau konverter i bestræbelserne på at opnå et system med variabelt omløbstal.

Fokusområdet i denne afhandling er at etablere et simpelt, hurtigt og nøjagtigt simuleringsværktøj med henblik på at kunne evaluere forskellige konvertertopologier til anvendelse i en vindmølle applikation baseret på den dobbelt fødede asynkrongenerator. Målet er at opnå en fair sammenligning mellem de betragtede konvertere hvor sammenligningsparameteren er det samlede systems virkningsgrad eller mere præcist den årlige energiproduktion. I afhandlingen sammenlignes 4 forskellige konvertertopologier - den typisk anvendte back-to-back koblede spændingsstive to-niveau konverter, den væsentlig mindre udbredte matrix konverter, og endelig 2 afarter af den back-to-back koblede spændingsstive tre-niveau konverter.

For at kunne evaluere konsekvenserne af at anvende de forskellige konvertertopologier i en vindmølleapplikation baseret på den dobbelt-fødede asynkrongenerator er det nødvendigt at modeldanne de øvrige systemkomponenter i en tilstrækkelig detaljeret grad. Det øvrige system består i væsentlige træk af generator, gearkasse, vinger og transformator. Den første del af afhandlingen er dedikeret til denne modeldannelse og modellerne er primært baseret på velkendte ligninger med let opnåelige ligningskoefficienter.

Det væsentligste bidrag fra denne afhandling ligger i selve modeldannelsen af de betragtede konvertere. For hver af disse konvertere er der udledt analytiske udtryk for effekttabene afsat i de enkelte komponenter. De afsatte tab afhænger af det specifikke vindmølledesign såvel som de operationelle forhold såsom rotationshastighed, effektproduktion, powerfaktor og modulationsmetode. Specielt hvad angår modulationsmetoder er der i afhandlingen foretaget en tilbundsgående analyse af eksisterende modulationsmetoder, ligesom der er udviklet nye modulationsmetoder. Specifikt er der for matrix konverteren udviklet tre nye modulationsstrategier mens der for de to tre-niveau konverterne er udviklet 4 nye modulationsstrategier. Funktionaliteten af de udviklede modulationsstrategier er for størstedelens vedkommende demonstreret i en testopstilling. Foruden bestemmelse af konvertertab er modellerne anvendelige til at beregne middeltemperaturer og peaktemperaturer i de enkelte komponenter - uden at det indebærer langsommelige tids-steps simuleringer. Disse metoder er specielt anvendelige til at kortlægge et aktuelt konverterlayouts designmargin. Herudover vil metoden på sigt være anvendelig til at estimere problemer såsom termisk cycling og power cycling i et specifikt vind mølle design. For at opnå en fair sammenligning er der for hver af de betragtede konvertere udarbejdet en initial-design guideline som vedrører emner såsom strøm- og spændingsrating, filter design og valg af switchfrekvens.

Grundet den store mængde af analytiske udtryk til beskrivelse af komponentbelastninger, komponenttab og komponenttemperaturer er samtlige ligninger implementeret i et beregningsværktøj med navnet D′rives. Det grafiske brugerinterface i D′rives sikre en hurtig og overskueligt sammenkædning af de relevante ligninger samt indlæsning af korrekte systemparametre. Ved hjælp af dette beregningsværktøj kan forskellige konverterdesigns og/eller forskellige konvertertopologier sammenlignes i løbet af ganske få sekunder. Derudover kan et aktuelt konverter design evalueres for, om det temperaturmæssigt overholder en given designspecifikation i hele det forventede belastningsområde. For at opnå en fair sammenligning imellem forskellige konvertertopologier skal alle konverterne tilnærmelsesvis have samme designmargin. Simuleringsværktøjet er i afhandlingen demonstreret på udvalgte vindmølledesigns og for de aktuelle sammenligninger vil en tre-niveau transistor-clamped konverter være det bedste valg (om end ubetydeligt) når der sammenlignes på systemets virkningsgrad eller mere præcist på den årlige energiproduktion. Som det imidlertid vil fremgå af afhandlingen er der i mølledesignet mange frihedsgrader og ændringer i de sammenlignede designs kan meget vel føre til et ændret resultat.

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Part I

Preliminaries

Chapter 1

Introduction

FOR centuries the winds have been used to grind grain and although present applications powered by the wind have other purposes than grinding grain, almost any wind powered machine - no matter what job it does - is still called a *windmill*. In the 1920´s and 1930´s, before electric wires were stretched to every community, small wind generators were used to power lights and appliances. At the instance of the growth in the world-wide infrastructure with widely distributed electrical power, the use of wind generators has been almost suspended for several decades. Among others, a consequence of the oil shock of the 1970´s is that the global energy policy of today is towards renewable energy resources and for that reason, the windmill has become its renaissance.

This chapter introduces the reader to the trends in modern wind turbine application especially with focus on the generator system. Advantages of variable speed wind turbines compared with the constant speed wind turbine are explained and a brief *state-of-the-art* in wind turbine generating systems are presented. Subsequently the aim and the contributions of the thesis are stated and finally the structure of the report is outlined.

1.1 Wind turbines

Since the mid eighties the world-wide installed wind turbine power has increased dramatically and several international forecasts expect the growth to continue. Fig. 1.1a shows the accumulated world-wide installed wind power from 1982 to 2005 [1]. Supporting these forecasts are a number of national energy programmes that proclaim a high utilization of wind power. Among these, the European Commission has scheduled 12% penetration of renewable energy by the year 2010 [24] and the objective for the United States is 10.000 MW of installed capacity by the year 2010 [22]. These high political ambitions along with a fast progress in generator concepts, semiconductor devices and solid materials have founded a strong basis for the development of large and cost competitive wind turbines. Figure 13.1b shows the annual average size in kW for wind turbines installed world wide in the period from 1982 to 2004 and figure 13.1c shows

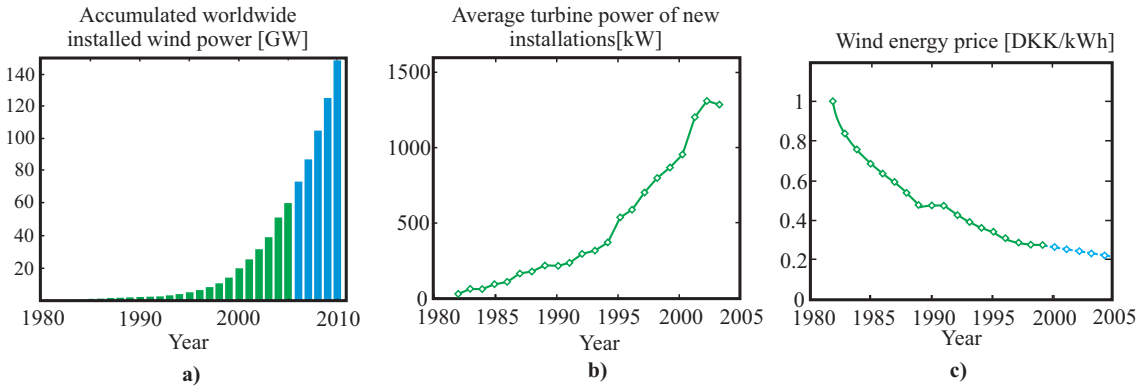

Figure 1.1: *Trends in the field of wind turbines. a) Accumulated worldwide installed wind power [1, 2]. b) The average turbine power for wind turbines installed from 1982-2006 [4, 42]. c) Estimated costs of wind generated electricity in Denmark. The blue lines indicate a prognosis [4].*

the estimated costs of wind generated electricity in Denmark during the last 20 years [4][1].

Until the very late nineties, the constant speed wind turbine, using either a synchronous generator or a conventional induction generator, has been the preferred choice [34]. However as the ratings of the wind turbines have increased and the use of wind turbines have become more and more widespread, a couple of problems with the constant speed wind turbine occurred, which had made other alternatives more attractive.

1.1.1 Constant speed wind turbines

Among others, a reason for the prevalent use of fixed speed wind turbines is the simple and reliable generator construction, which for small wind turbines seems to be the most cost per kWh competitive concept. However, in large wind turbines and particular in wind turbine farms, the problems concerning the fixed speed operation become significant. To deal with these problems several precautions have to taken, which might reduce the reliability and competitiveness of the fixed speed system. Below are some of the drawbacks associated with the fixed speed wind turbine explained.

Energy capture

A problem concerning the design of a constant speed wind turbine is the choice of a nominal wind speed at which the wind turbine produces its rated power. This problem arises from the fact that the energy capture of the wind is a nonlinear function depending on the ratio between wind speed and rotor tip speed. In general the power transmitted

[1]The calculations of figure 13.1c are based on 20 years depreciation, 5% interest rates and a siting in roughness class 1.

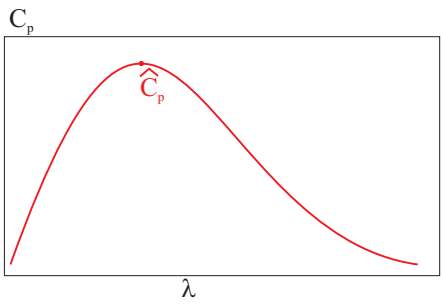

Figure 1.2: *Power performance coefficient C_p versus tip speed ratio λ.*

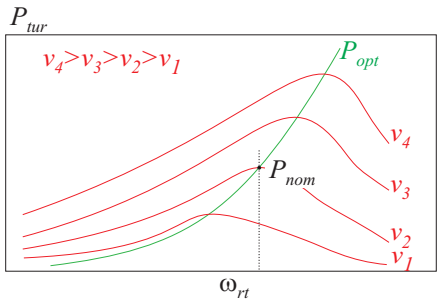

Figure 1.3: *The power transmitted to the hub shaft at different wind speeds.*

to the hub shaft of the wind turbine is expressed as [44]:

$$P_{tur} = \frac{1}{2} C_p \rho_{air} A_v v_{wind}^3 \tag{1.1}$$

where A_v is the area swept out by the turbine blades, ρ_{air} is the mass density of air, v_{wind} is the velocity of the wind and C_p is the power performance coefficient. The power performance coefficient varies considerably for various designs, but in general it is a function of the blade tip speed ratio λ and the pitch angle θ_{pitch}. The blade tip speed ratio λ is defined as:

$$\lambda = \frac{v_{tip}}{v_{wind}} = \frac{r_{rt}\omega_{rt}}{v_{wind}} \tag{1.2}$$

where v_{tip} is the blade tip speed, r_{rt} is the radius of the propeller and ω_{rt} is the angular velocity of the propeller. Fig. 1.2 shows a typical relation between the power performance coefficient and the tip speed ratio.
The problem concerning the energy capture from constant speed wind turbines is visualized in Fig. 1.3, where the power transmitted to the hub shaft versus rotor speed is plotted for different wind speeds, $v_1 ... v_4$. From Fig. 1.3 it appears, that at wind speeds above and below the rated wind speed, the energy capture does not reach the maximum value.

By the use of a variable speed wind generating system, the energy capture may be extended, gaining a higher system efficiency [34].

In almost any literature treating variable speed wind turbines, this statement is one of the major arguments for the use of variable speed wind turbines and for instance, in [28], McIver et al. obtained 9-15% increase in the energy capture by use of the variable speed concept. However, in [5] a fixed speed wind turbine and a variable speed wind turbine were compared, and in spite of several other superior properties of the variable speed wind turbine, it was stated that no significant improvement in the energy capture was achieved by introducing variable speed[2].

[2]The conclusion in [5] was based on experimental data. Unfortunately, due to the fact, that the stator connected converter used in [5] had a switching frequency of only 600 Hz, the conclusion is not necessarily the general truth.

Mechanical stress

Another problem concerning the fixed speed wind turbine is the design of the mechanical system. Due to the almost fixed speed of the wind turbine every fluctuations in the wind power is converted to torque pulsations which cause mechanical stresses. To avoid breakdowns, the drive train and gear-box of a fixed speed turbine must be able to withstand the absolute peak loading conditions and consequently additional safety factors need to be incorporated into the design [41].

The mechanical dimensions of a variable speed wind turbine might be reduced in comparison with the mechanical dimensions of a fixed speed wind turbine.

In [31] the shaft torque pulsations of different variable speed wind turbine schemes are compared to the torque pulsations of a constant speed wind turbine, and the results shows significant improvements by the use of variable speed wind turbines.

Power quality

The power generated from a fixed speed wind turbine is sensitive to fluctuations in the wind. Due to the steep speed-torque characteristics of an induction generator, any change in the wind speed is transmitted through the drive train on to the grid [41]. An improvement of the power quality is the pitch control which to a certain extent is able to compensates slow variations in the wind by pitching the rotor blades and thereby changing the power performance coefficient C_p. The pitch control are not able to compensate for gusts and the fast periodic torque pulsations which occur at the frequency the blades pass the tower. The rapidly changing wind power may create an objectionable voltage flicker, which causes annoyances to the human eye in shape of disturbances in the light.

Another power quality problem of the fixed speed wind turbine is the reactive power consumption. Many of the electrical networks, to which wind farms are connected, are weak with high source impedances. The output power of a constant speed wind turbine changes constantly with the wind conditions, resulting in voltage fluctuations at the point of connection. Due to these voltage fluctuations the constant speed wind turbine draws varying amounts of reactive power from the utility grid which increases both the voltage fluctuations and the line losses. To improve the power quality of wind turbines, large reactive components, active as well as passive, are often used to compensate the reactive power consumption [36].

Voltage flicker in the utility grid caused by rapid fluctuations in the turbine power could be reduced by use of a variable speed wind turbine generating system [46]. Due to the power electronic utility interface provided with variable speed generating systems it is also possible to improve the poor displacement factor associated with induction generators [37].

To get an impression of the size of a compensation installation, [36] treats a static VAr compensator for a 24 MW wind turbine farm and it is found that the necessary installation amounts to 8.8 MVAr.

Until recently wind turbines were treated as small embedded generator units with no contribution to the overall power system stability control and as so wind turbines were required to disconnect from the utility grid in occurrence of abnormal grid conditions. Recently national grid operators such as E.ON in Germany, Eltra in Denmark and Scottish and Southern Energy plc. in Scotland [6, 23], have reconsidered these easy terms and formulated some quite tough requirements regarding power factor control and ride through capability - requirements for which constant speed wind turbines are not very well suited.

1.1.2 Variable speed wind turbines

Initiated by the disadvantages in the use of constant speed wind turbines described above, the standard of modern wind energy conversion is variable speed constant frequency generating systems. This section tends to give a survey over reported variable speed generating systems used in wind turbine applications. For each of the reported systems a brief description of the mode of operation is given together with an evaluation of advantages and disadvantages associated with the present drive topology.

Improved speed range by rotor impedance control

The use of adjustable resistors for starting and speed control of wound-rotor slip-ring induction machines (DFIG) is well treated in the literature, [11] and [33]. In [43] a partly controlled three phase rectifier is connected to the rotor circuit and loaded either with fixed resistances or without them, while the stator is connected directly to the supply grid. By controlling the equivalent rotor resistance the speed range of the machine is improved. Fig. 1.4 on the following page shows the proposed circuit topology. Fig. 1.5 illustrates the principles in the rotor resistance control. By a proper control of the rotor resistance, torque pulsations caused by variations in the wind power can be reduced at the expense of speed pulsations and additional losses. In [45], the simple rotor resistance control is extended to rotor impedance control, offering the opportunity of partly improving the power factor. The system suffers from a low efficiency at improved power factor. To avoid the brushes, [45] proposed a controllable rotor circuit rotating on the generator shaft. This concept is among others used by Vestas Wind Systems in some of

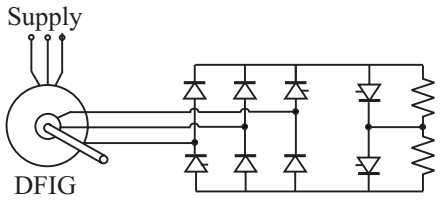

Figure 1.4: *Topology for improving the speed range by adjusting the rotor resistance.*

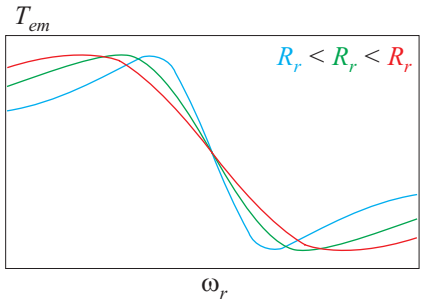

Figure 1.5: *Controlling the rotor resistance, the torque-speed characteristic of the machine can be shaped.*

their Optislip® concepts. The advantages of this concept are: simple circuit topology, improved operating speed range compared to the conventional induction generator. To a certain extent this topology can reduce the mechanical stresses and power fluctuations caused by wind gusts. The stator of the machine is connected directly to the supply grid and the power semiconductors are rated only to handle the slip power. The disadvantages are: the operating speed range is limited to a few percent above synchronous speed (for generation mode), and only poor control of active and reactive power is obtained. The slip-power is dissipated in the adjustable rotor resistance and furthermore the presence of the step up gear increases the costs and weight of the system, and causes a slight decrease in the system efficiency.

Converter controlled induction generator

A simple method for obtaining a full variable speed wind turbine system is to apply a bi-directional power converter to a conventional induction generator. Solutions based on this concept are treated in [29, 34, 35]. Some of the advantages in this topology are that the active and reactive power is controllable, the generator is durable and requires only a minimum of maintenance. Furthermore, the large amount of knowledge in the field of speed controlled induction machine might be applicable in wind turbine applications [34]. The disadvantages are the presence of the step up gear and the fact that the power converter must handle the full rated power of the system. In [31] it is claimed that in low power wind turbines, this solution provides the highest efficiency.

Multi pole synchronous generators

A common reported solution to avoid the step up gear between the propeller and the generator is the use of a multi pole synchronous generator, either with permanent magnets (PMG) [9, 10, 25, 48] or externally magnetized (SG). In [38] a 400 kW wind turbine system is designed, based on a permanent magnet generator. The designed generator has 168 poles, resulting in a synchronous speed of 35.7 RPM. Besides the absence of the step-up gear some of the reported advantages are: less acoustic noise, full control of active and reactive power and high efficiency. A consequence of the high pole number is that the PMG becomes physically larger than machines including a step-up gear and

still, the full rated power has to be handled by the power converter. Another disadvantage of the PMG is the large amount of magnetic material which is a large contributor to the total cost of the system. The latter might change if the forecasts on magnetic materials are to be believed. Alternatively, the synchronous generator can be externally magnetized. By this the permanent magnets are avoided and the generator voltage becomes controllable, however at the expense of additional rotor losses. The externally magnetized multi pole synchronous generator is commercially used by the German wind turbine manufacture Enercon in their large megawatt wind turbines.

Switched reluctance generators

In papers considering the switched reluctance generator (SRG) for wind turbine applications, the most common argument is the high efficiency, the reduced costs, due to the simple construction of the generator [27] and the opportunity of eliminating the step-up gear. In [39] a comparison between a SRG wind turbine system and a variable speed IG system was performed, and it was found that the SRG based system has 6% higher efficiency and 13% reduced costs. The reliability of these results is however debatable because the comparison was based on *typical* values for the efficiency of controlled rectifiers, IG, SRG, VSI and CSI. Also the estimation of costs is based on a cost factor estimate and in this estimate no passive components are incorporated. The advantages of using the SRG are: elimination of the gear box is possible, high reliability and low generator costs, due to the simple structure of the generator [40]. High efficiency of the generator. Lower diameter than a direct driven synchronous generator. More simple converter and a higher power-to-weight ratio [8]. The disadvantages are: relatively high VA-ratings of the converter, and high converter losses due to the high amount of field energy which has to be supplied and removed for each stroke. The VA ratings of the power converter might be reduced by implementing permanent magnets in the generator [14], but clearly this increases the costs and the complexity of the generator. Furthermore, the mechanical stress of the generator are high due to the high torque ripple and finally, the full power of the generating system has to be handled by the power converter.

Cascaded generator systems

Except for the rotor impedance control, a major drawback of the generator systems treated so far, is that the power converter has to handle the rated power of the system. One way to avoid a full rated power converter is by using a cascaded generator. According to [21], a cascaded generator has the properties that the frequency converter only handles a part of the full power and the presence of slip-rings is avoided. Among others, the brushless doubly-fed reluctance generator (BDFRG), the brushless doubly-fed induction generator (BDFIG) and the cascaded doubly-fed induction generator (CDFIG) all have these properties and in addition they offer the opportunity of full active and reactive power control. Fig. 1.6 on the next page shows the topology of these three cascaded generators.

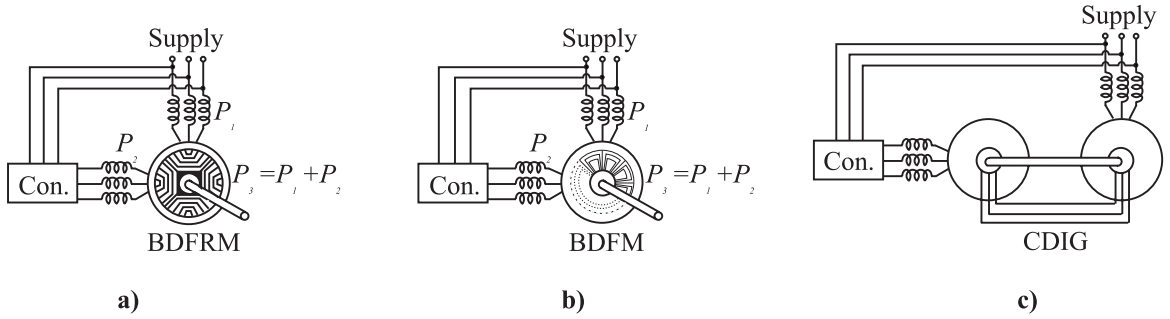

Figure 1.6: *Cascaded generator topologies.* **a)** *The brushless doubly-fed induction generator.* **b)** *The brushless doubly-fed reluctance generator.* **c)** *The cascaded doubly-fed induction generator.*

In [7] a BDFIG variable speed wind generating system with a speed range between 1200 RPM and 2000 RPM was developed. In this system, the converter was rated to handle 25% of the full power. It was stated that the generator efficiency is comparable to that of a conventional induction generator while the efficiency of the converter was higher than the efficiency of a full scale converter, giving an overall higher efficiency. Further advantages are: compact design (almost comparable to a conventional IG) [41] and better harmonic characteristics because most of the power is generated directly to the grid [37]. A wind power generating system based upon the BDFRG is described in [47]. The reported advantages are: Higher generator efficiency compared to the BDFIG due to the absent of copper losses in the rotor circuit. Enhanced reliability and reduced costs are also achieved due to the absent of the rotor windings and the brushes. Finally, the controllability and flexibility of the generating system are accentuated. However, an insufficiency of the work carried out in [47] is that the conclusions are only based on simulation results. In [3] it is mentioned that the design of the rotor is quite complex and is a compromise between complexity, efficiency and torque per volume. The third of the reported cascaded generators in wind turbine generating systems is the CDIG [21]. The CDIG consists in principle of two doubly-fed slip-ring induction generators where the two rotors are mechanically and electrically connected (no brushes are in use). In [21] two equal sized slip-ring induction generators were used. By this arrangement the power converter had to handle 50% of the rated power while full active and reactive power control was achieved. A drawback of this method is that the axial length of the generator is higher than other generators [41].

Doubly-fed induction generators

Early attempts to make variable speed wind turbines in the megawatt range were based on the doubly-fed induction generator (DFIG). For instance, the Growian turbine erected in Germany in the early 1980´s was a 3MW variable speed wind turbine based on the DFIG and controlled by a thyristor based cyclo converter. Although the Growian turbine turned out to be an economical and technical disaster, it was one of the pioneering projects leading to the success of present wind turbines. Still at the

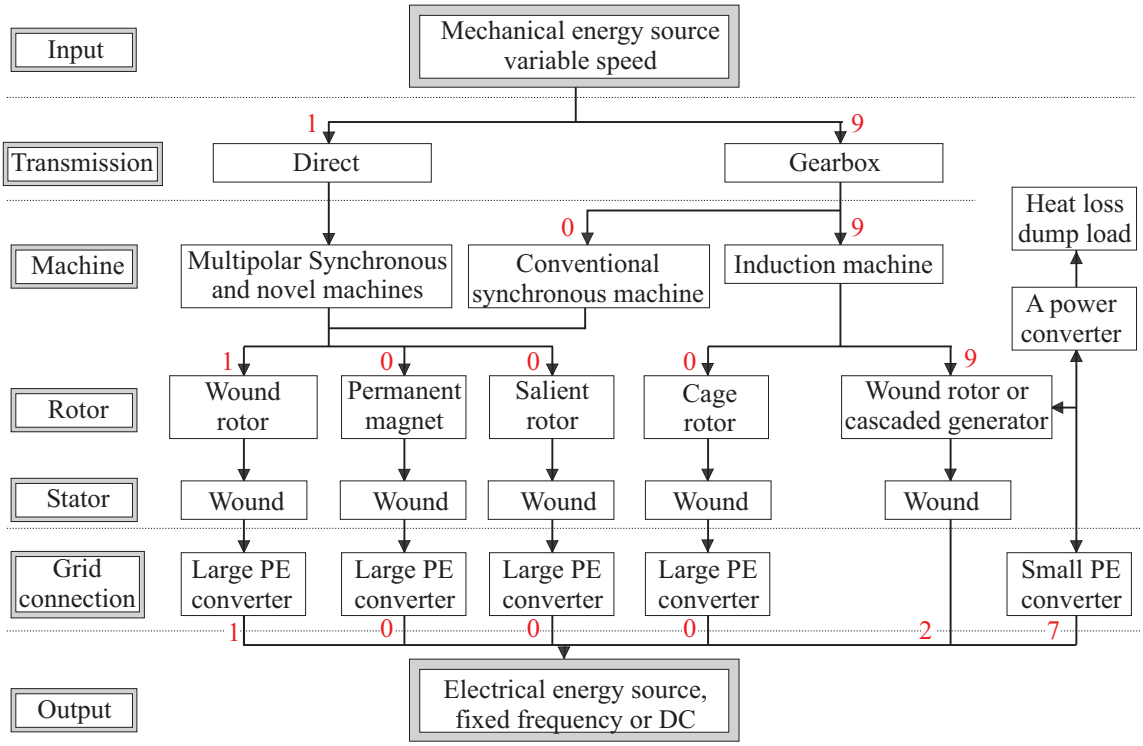

Figure 1.7: *Conversion process from wind energy to electrical energy [13].*

present level of technology, the DFIG seems to be the most serious competitor to the conventional constant-speed constant-frequency wind turbine, - at least according to the amount of literature available. In many aspects, the DFIG is related to the cascaded generators in the way, that the converter only has to handle the slip-fraction of the total power, but unlike the cascaded generators, the control of the DFIG is obtained directly through the rotor circuit of the generator. Compared to the cascaded generators, the doubly-fed induction generator is less complex while having the same nice properties of full active and reactive power control. However, these superior properties are achieved at the expense of introducing slip-rings in the system. Besides the slip rings, another drawback of the DFIG is the need for a step-up gear.

1.1.3 State of the art

Introducing the variable speed concept in wind turbines has obviously produced a large variety of applicable solutions both with regards to machine type and with regards to converter topology. Fig. 1.7 surveys the different generator concepts discussed in the preceding sections. However, regardless of the large variety of generator concepts, a look among the 10 largest wind turbine manufactures in the world forms the picture, that the DFIG equipped with a back-to-back two level power converter is occupying the de-facto standard position for variable speed wind turbines [13]. The numbers in Fig. 1.7 represents a count of the manufactures using the specified topology. Out of ten manufactures, seven of them use the DFIG in a slip recovery system, two use a constant

speed solution and only one believes in a solution based on the multi pole synchronous generator.

Regarding the power capability of present wind turbines, the state of the art turbine size (made up in December 2006), seems to be in the vicinity of 3-4 MW, although some manufactures announce an approaching introduction of turbines in the 6-7MW range.

1.2 Problem statement

As indicated by the technical report *"Conceptual survey of Generators and Power Electronics for Wind Turbines"* from Risø National Laboratory [13], only a few references covers a survey and a comparison among different topologies while solutions and innovations for a specific topology are numerous. The goal of this project is to establish some tools for making a fair comparison between different topologies. This is obviously an overwhelming task and surely some limitations have to be introduced. Before stating the limitations of the comparison, the motivation for entering this huge work is discussed and the scope of the thesis is defined.

1.2.1 Motivation

Wind turbines are developing very rapidly and have, during the nineties, evolved from small generators *on a stick* to highly complicated and advanced miniature power plants. However, in such a fast progressing industry, wind turbine manufactures often have to choose a kind of *standard solution*, relying on choices made for instance by the variable speed drive industry, without considering alternative - and maybe more suitable - solutions. In the future, when the turbine units are entering into the tens-of-megawatt range, the turbine manufactures may have to reconsider their choices and designs and pay even more attention to the issues given below:

- Power losses.
- Volume and weight.
- Reliability.

Decreasing the power losses of the system will gain the annual energy production and thereby the economical profit for the wind turbine owner (and the wind turbine manufacturer). Further, decreasing the power losses reduces the need for internally cooling facilities, thereby reducing weight and volume.

As the turbine power increases, weight and volume become very (maybe the most) crucial factors in the design of the wind turbines. As an example, in today′s state of the art wind turbines, the weight of the nacelle, hub and blades accounts for among 110 tons,

constituting a serious transportation problem, both with regard to weight and volume.

Finally, as wind turbines are penetrating the public supply grid to a considerable extent, the demands to reliability and availability increases correspondingly. Further, since wind turbines and wind turbine parks are often located in remote areas (even off-shore), service and maintenance has to be quite rare and preferably on scheduled tasks.

1.2.2 Scope of the thesis

In the light of the increasing interest on variable speed wind turbines and the numerous amount of publications treating variable speed wind turbines, it is conspicuous that only a few papers compares different topologies. In [12], Grauers presented an efficiency evaluation of three different generator concepts for variable speed wind turbines, concluding that a multipole permanent magnet generator is the most efficient generator choice for a variable speed wind turbine. However, this work only focused on the generator and it is strongly believed that incorporating the efficiency of the power converter will change this picture - at least at the present level of semiconductor technology. In [20], Hoffmann et al. investigated different turbine configurations with regard to energy capture, but the main focus were on the blade control rather than on the variable speed configuration.

A thorough comparison, involving different generator concepts and converter topologies is obviously an almost overwhelming task and in order to reduce this task, it is chosen to believe in the mainstream of wind turbine manufactures counting on the DFIG and instead questioning the conservative adhere to the conventional back-to-back two-level converter. Hence, the main scope of this thesis is to evaluate different converter topologies for use in a variable speed wind turbine based on the DFIG. A thorough evaluation should obviously include and weight the various motivation factors, because gained performance with respect to one of the motivating factors might very well be overruled by a decreased performance in other aspects. For instance, a slight gain in the annual energy production might very well be of minor importance if the converter structure is much heavier and voluminous. However, the evaluation criteria for this comparison will primarily be the converter efficiency, or more specific, the annual energy production, given a certain wind distribution, while evaluation of volume, weight and reliability will be performed on a qualitative basis only.

Compared to the back-to-back two-level converter, which at present is the prevalent choice, alternative converter topologies are quite non-mature, making an immediate comparison unfair and in absolute favor of the back-to-back two-level converter. Hence, a part of this thesis is dedicated to mature alternative converter topologies in order to obtain a fair comparison. Besides maturing alternative topologies, another challenge is to establish an equal set of evaluation criteria. From this, problem #1 arises:

Problem #1

> Investigation of selected converter topologies, including some maturing efforts. In order to compare the different converter topologies, some evaluation tools have to be established. To exemplify the derived tools, the tools will be used to evaluate the considered topologies with regards to their annual energy capture in a specific state of the art turbine application.

To obtain a fair outcome of the comparison formulated in problem #1, the considered power converters will have to be designed to have an equal power capability in the entire operating range. Hence problem #2 to be addressed in this thesis is:

Problem #2

> Development of a tool suitable for determining the power capability of a certain converter design

1.2.3 Limitations

Besides the limitation introduced by considering only the DFIG, the converter investigation is limited to focus only on the following four inverters although other alternatives are known to exist:

- The back-to-back two-level voltage source converter.
- The matrix converter.
- The back-to-back diode clamped three-level voltage source converter.
- The back-to-back transistor clamped three-level voltage source converter.

As mentioned previously, to exemplify the derived comparison tools, a 2 MW wind turbine is considered having some pre-determined characteristics. Obviously, the results and conclusions obtained when looking at a turbine of another size and with different characteristics will probably change. However, at this point it should be emphasized that the important aspect is the evaluation method rather than the specific result. That is:

The present turbine size of 2 MW is only used to exemplify the evaluation methods.

System under considerations

The system under consideration is shown in Fig. 1.8. In the present case, the system is a 2 MW wind turbine based on the DFIG. The system is connected to the 10 kV supply grid through a transformer with a secondary winding voltage of 690 V (phase-phase).

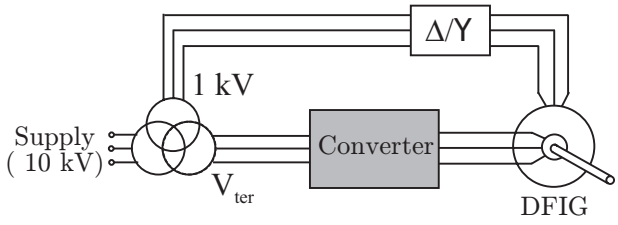

Figure 1.8: *Doubly-fed induction generator system.*

The stator of the DFIG is connected to this secondary winding, however with the possibility to connect the generator in either star or delta connection, thereby increasing the speed range of the system at low power and at the same time reducing the system losses. Since the considered converters do not have the same properties with regards to voltage gain etc. it is assumed that the voltage at the tertiary winding as well as the winding ratio of the generator can be used as design variables. In the system, components and characteristics such as gear type, blade characteristics, electrical generator- and transformer characteristics (except the winding ratio) are predetermined and is described in chapter 2 concerning the modeling of the system.

1.3 Contributions

Although it is not the author′s privilege to judge the novelty and significance of his own work, it may be worthwhile to spend a few lines pointing out, in which areas special efforts were made in order to come up with new ideas and thoughts. Below is a list of areas to which special attention have been paid:

Comparison of different converter topologies: Comparison of different converter topologies for use in a variable speed wind turbine based on the doubly-fed induction generator [15]

New modulation strategies for the matrix converter : In the efforts on maturing the matrix converter, one task was to investigate and develop new modulation strategies having better harmonic properties and/or lower switching losses compared to existing strategies. Some of these efforts are described in [19, 26].

Tools for evaluating different modulation strategies: Besides developing new modulation strategies, a survey on the literature covering matrix converters revealed that unlike for the two- and three-level inverters, no methods existed for evaluating modulation strategies for the matrix converter. It was found worthwhile to spend some efforts developing a comparison method similar to those for two- and three-level inverters. The comparison method is described in [17].

New modulation strategies for the three-level converter: As for the matrix converter, the study on three-level converters (and multi-level inverters in general) revealed that the maturing process for the three-level inverters needed a little

injection with regards to modulation strategies. Hence, some efforts were also dedicated to develop new modulation strategies for the three-level converter, especially with focus on harmonic properties, switching losses and DC-link balancing [18, 16].

The citations mentioned above are all enclosed in Appendix C-I. Besides the work documented in this thesis and in the publications cited above, the intensive work in converter topologies for the doubly-fed induction machine has made it possible to partly contribute to the following work:

Patent WO 01/91279 A1 [32]: The patent entitled "Variable Speed Wind Turbine having a Matrix Converter", International publication number WO 01/91279 A1 was partly initiated by the work described in chapter 4 of the this thesis. The content of the patent was formulated in co-operation with Anders V. Rebsdorf a former colleague at Vestas Wind Systems.

The book "Control in Power Electronics" [30]: Chapter 13 of the book *"Control in Power Electronics"*, covering wind turbine systems was written, based on knowledge obtained during the Ph.D.-programme. The chapter is a general survey over different wind turbine concepts, including some control aspects and was written in co-operation with Frede Blaabjerg.

The technical report "Risø-R-1205(EN)" [13] .Chapter 3 of the technical report *"Risø-R-1205(EN)"*, entitled *"Conceptual survey of Generators and Power Electronics for Wind Turbines"* covers different converter topologies for use in variable speed wind turbines and was based on a preliminary survey report written in the early stage of the Ph.D-programme.

1.4 Outline of the report

The main report is divided into separate parts dedicated to pursue the stated problems. Actually, the report consists of three parts, the first part *Preliminaries* covers the introduction to variable speed wind turbines, and in particular an introduction and modeling of the variable speed wind turbine based on the doubly-fed induction generator. The second part *Converter modeling* is aimed to the modeling and maturing efforts performed in order to be able to compare the different converter topologies. The third and last part concerns the comparison of the considered systems along with the conclusion and the perspectives of the accomplished work. Besides the three parts forming the main report, a fourth part is added, covering a number of appendices and the publications published by the author.

To structure the individual parts, each part is divided in an appropriate number of chapters. The part- and chapter structure is outlined in Fig. 1.9 on the facing page.

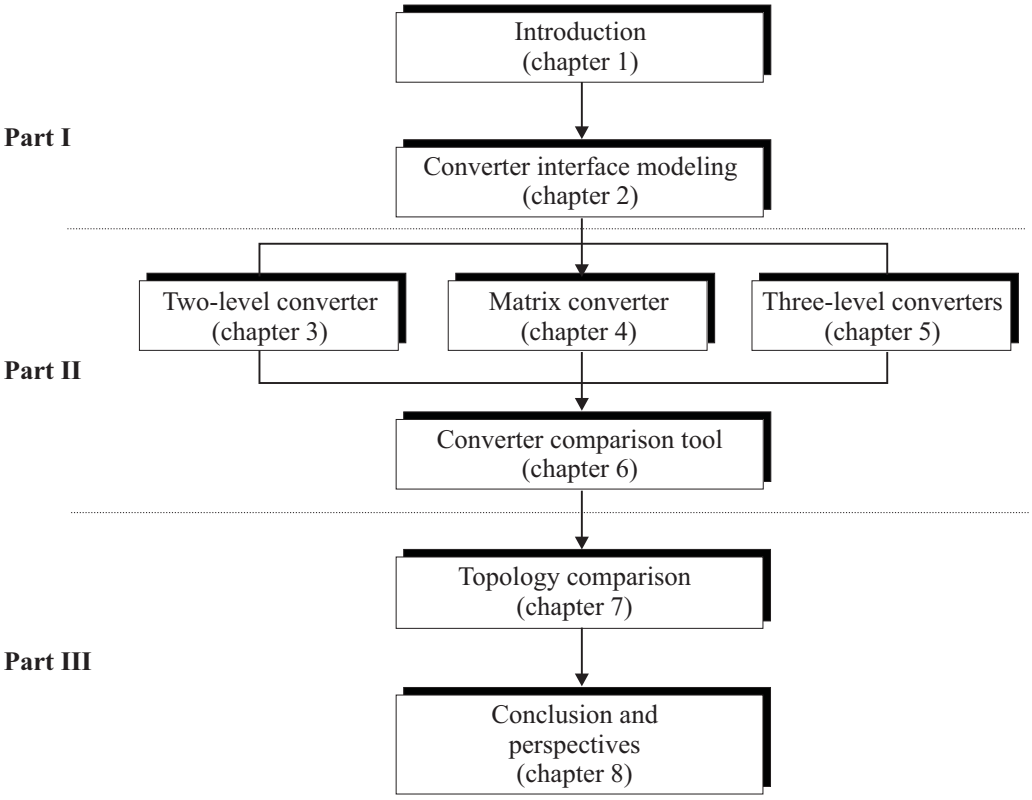

Figure 1.9: *The structure of the report.*

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Chapter 2

Modeling of wind turbine system

WHEN evaluating the different converter topologies with regards to the annual energy production of the turbine it is likely to expect that besides the power losses in the converter, the performance and characteristics of the converter may influence the power losses in the interfering components and hence affect the annual energy production in a quite complicated manner. Hence, to evaluate the converter topologies with regards to annual energy production of the turbine, it is necessary to establish adequate models of the components interfering with the converter. Fig. 2.1 illustrates the components interfacing to the power converter in a doubly-fed system.

With reference to Fig. 2.1, this modeling chapter begins with a description of the available wind power and then step by step establishing models of each component in Fig. 2.1 in order to predict the power flow and in the final stage predict the annual energy production. The last step in Fig. 2.1 represents the supply grid but since the energy production is evaluated at the point of connection, no loss models of the grid are needed. However, the grid, or rather the grid operator sets some demands to the grid connected wind turbine and hence to the converter design. Hence, these demands will be outlined in this chapter. The models established in this chapter along with the converter models and converter features described in chapter 3 to chapter 5 are to be used in a design and comparison tool. The developed design and comparison tool will be presented in chapter 6.

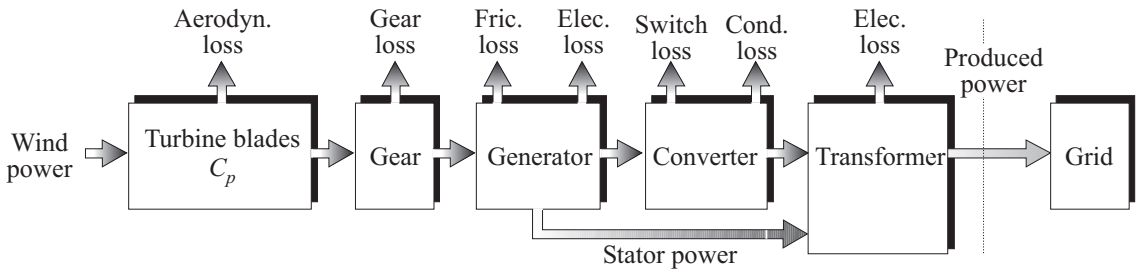

Figure 2.1: *Components interfacing to the power converter.*

2.1 Model of the wind power

The power in the wind can be modeled as the super position of two components [9]:

- The macro-scale air flow, i.e. average wind speed.
- The micro-scale air flow, i.e. rapid wind speed changes such as wind gusts.

The macro-scale air flow is imposed by local low-pressure and high-pressure zones and is characterized by slowly varying conditions. Thus, the macro-scale air flow may represent the average wind speed or the wind energy which is desirable to extract. The micro-scale air flow is caused by e.g. obstacles in the terrain creating fast fluctuations in the wind speed at a given site and hence quite fast transients in the available power. As discussed in chapter 1, these wind speed fluctuations may cause a number of problems especially in connection with constant speed wind turbines.

2.1.1 Power in the wind

From the definition of kinetic energy [3], the power in the wind, P_{wind}, blowing perpendicular to a surface A_v with a constant speed v_{wind} can be calculated by:

$$P_{wind} = \frac{1}{2} \cdot \rho_{air} \cdot A_v \cdot v_{wind}^3 \tag{2.1}$$

where ρ_{air} is the mass density of air. Fig. 2.2 shows the per unit area wind power as a function of the wind speed. To model the power in the wind, a description of the wind speed is needed.

2.1.2 Wind speed distribution

Short term wind distribution

The short term wind speed, for instance describing both the micro-scale air flow and the hourly varying macro-scale air flow, could be generated by the empirical model described in [9]. The empirical model uses the spectral power density $S(f_{fwind})$ calculated for different wind frequency components f_{wind}. The spectral power density of the wind is given by:

$$S(f_{wind}) = \frac{\frac{h}{\overline{V}_{wind}} \cdot \sigma_{wind}^2}{f_m \left(1 + \frac{3}{2 \cdot f_m} \left(f_{wind} \cdot \frac{h}{\overline{V}_{wind}}\right)\right)^{\frac{5}{3}}} \tag{2.2}$$

where $\overline{V}_{wind}$ is the average wind speed in the considered frequency spectrum, h is the height above ground, f_m is a fluctuation constant (assumed to be 0.06) and σ_{wind} is the wind speed standard deviation given by the turbulence times the average wind speed. Using the wind power spectrum calculated for the different frequency components, the

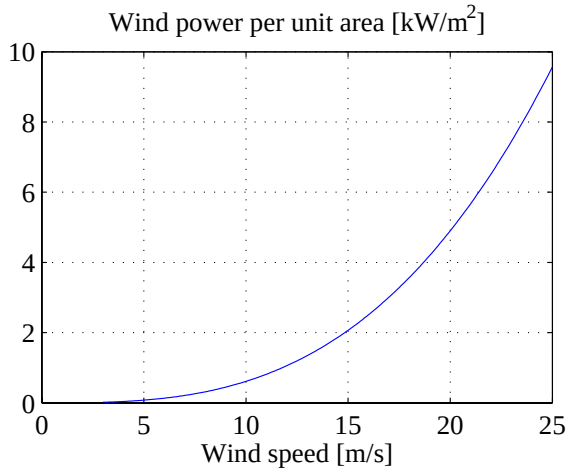

Figure 2.2: *Power in the wind per unit area.*

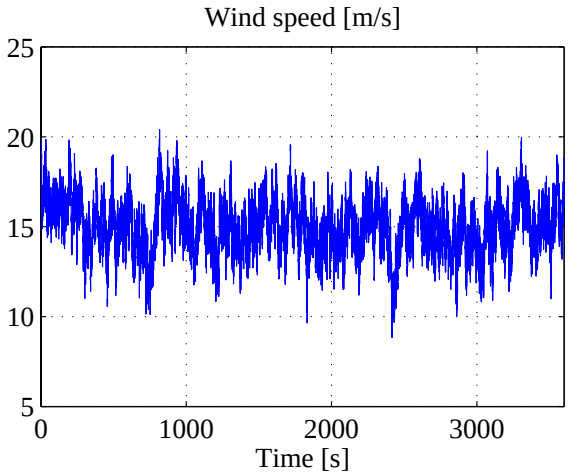

Figure 2.3: *Short term wind speed. Average wind speed is 15 m/s.*

hourly wind speed can be modeled by:

$$v_{wind} = \overline{V}_{wind} + \sqrt{2} \cdot \sum_{i=f_{wind,min}}^{f_{wind,max}} \sqrt{S(f_{wind,i}) \cdot \Delta f_{wind}} \cdot \cos(2 \cdot \pi \cdot f_{wind,i} \cdot t + \beta_i) \qquad (2.3)$$

where β_i is a random number between 0 and 2π and Δf_{wind} is the frequency spacing between the considered wind frequencies. Fig. 2.3 shows the wind speed, generated by (2.3) with a turbulence of 0.1, a mean wind speed of 15 m/s and a height above ground of 80 meters.

Annual wind speed distribution

Besides the hourly wind speed described by (2.3), a model of the annual distribution of the hourly average wind speed is needed. The hourly average wind speed distribution throughout the year is often modeled by the Weibull distribution function given by [4]:

$$P(\underline{V}_{wind}, c, a) = \frac{c}{a^c} \cdot \overline{V}_{wind}^{c-1} \cdot e^{-\left(\frac{\overline{V}_{wind}}{a}\right)^c} \qquad (2.4)$$

where $\overline{V}_{wind}$ is the wind speed range in which the wind distribution is evaluated. The constants c and a are parameters in the distribution function. Table I shows standard values of the factors a and c for different site classifications . Having the parameters in the Weibull distribution, the annual average wind speed $\overline{v}_{wind}$ can then be calculated by:

$$\overline{v}_{wind} = \Gamma\left(\frac{1}{c} + 1\right) \cdot a \qquad (2.5)$$

where $\Gamma(1/c + 1)$ is the generalized faculty function of $1/c$ [7]. Using (2.5), with the parameters from Table I gives an annually average wind speed of 7.5 m/s for typical

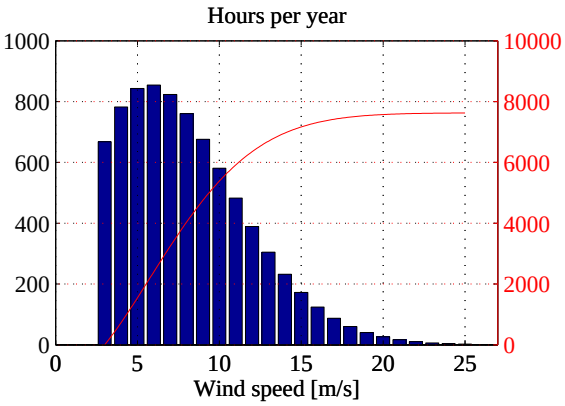

Figure 2.4: *Annual wind distribution for an on-shore site.*

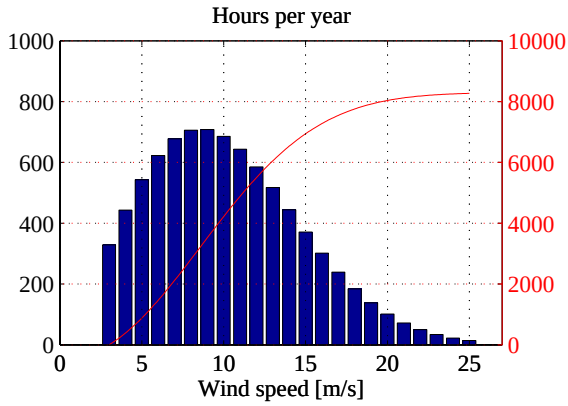

Figure 2.5: *Annual wind distribution for an off-shore site.*

on-shore turbines (IEC III) and 10.1 m/s for a high-wind off shore site (IEC I). Fig. 2.4 and 2.5 show the wind distribution for a typical on-shore site and an off-shore site respectively. Although factors as reliability and intervals between maintenance may influence the annual energy production it is assumed that the availability of the turbine is 100% and hence, according to the wind distributions in Fig. 2.4 and Fig. 2.5, an on-shore turbine is producing power 7757 hours per year while an off-shore turbine is producing power 8122 hours per year. (Assuming a cut-in wind speed of 3 m/s and a cut-out wind speed of 25 m/s). . The accumulated hours of operation is shown on the right axis of Fig. 2.4 and Fig. 2.5.

2.1.3 Limitations

As described above, models exist for both the micro-scale air flow and the hourly varying macro scale air flow. However, to utilize the information in such detailed wind models in the prediction of the annual energy production requires quite good knowledge of the dynamics both in the pitch control system and in the power converter control system. For that reason the wind speed is only modeled as an hourly average, described by (2.4). A justification of this limitation can be found in [8] where it is stated that the error obtained by omitting the turbulent wind component is within a few percent, provided

TABLE I: *Wind distribution parameters.*

Site classification	Parameter a	Parameter c	Annual average wind speed [m/s]
IEC I site	11.38	2	10.1
IEC II site	9.60	2	8.5
IEC III site	8.46	2	7.5
IEC IV site	6.77	2	6.0

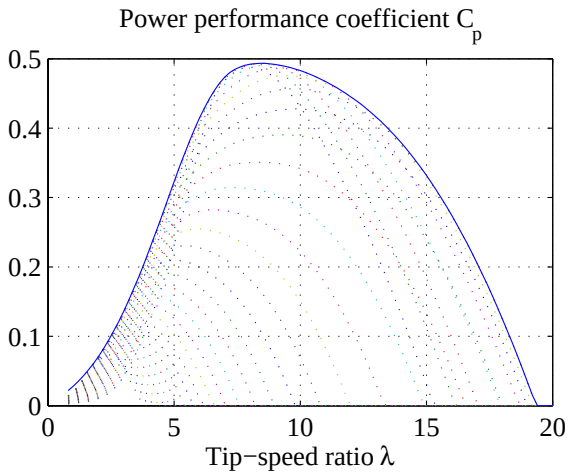

Figure 2.6: *The power performance curve versus tip-speed ratio, plotted for different pitch angles.*

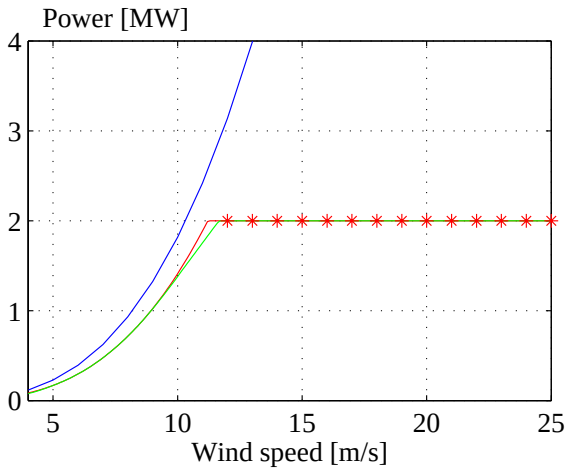

Figure 2.7: *Power extracted from the wind. The blue curve represents the theoretical maximum while the red curve represents the extracted power.*

that the turbulent component is within a reasonable range.

2.2 Model of the turbine blades

The purpose of a turbine blade model is to calculate the power extracted from the wind and transferred into mechanical power in the shape of torque and rotational speed on the turbine shaft. Since the turbine blade design along with the operation of the turbine have a high impact on the energy capture it is necessary to incorporate a quite good steady state model of the turbine blades - a model which basically is described by the power performance coefficient C_p.

2.2.1 Power performance coefficient

As discussed in chapter 1, the power captured from the wind depends on the blade design, the pitch angle θ_{pitch} and the tip speed ratio λ - all described by the power performance coefficient $C_p(\theta_{pitch}, \lambda)$. Ideally, the maximum power, which can be extracted from the wind is about 59% - the so-called Betz limit - but in practical blade designs, the maximum value is in the interval between 0.4 and 0.5 [18]. Fig. 2.6 shows the power performance coefficient C_p versus tip-speed ratio λ for a 45 meter long blade applicable for a 3 MW turbine. The curves indicated by dotted lines correspond to different pitch angles while the solid line indicates the power performance coefficient when tracking the optimum pitch angle. In the model of the turbine blades, it is assumed that the turbine tracks the optimum pitch angle as long as the generated turbine power is below the nominal power of the system. When the generated turbine power reaches the nominal power, i.e. nominal power generated to the grid, the pitch angle is controlled to keep

the turbine power at the nominal value. As so, the turbine blade model is described by a 2-D look-up table with the tip speed ratio λ and the available wind power P_{wind} as inputs and then using interpolation between the table values to find the pitch angle θ_{pitch} and thereby the power performance coefficient C_p.

2.2.2 Power transferred to the hub

Using the turbine blade characteristics in Fig. 2.6, the power extracted from the wind P_{tur} can be calculated by[1]:

$$P_{tur} = \frac{1}{2} C_p \rho_{air} A_v v_{wind}^3 \tag{2.6}$$

Fig. 2.7 on the preceding page shows the power extracted from the wind as a function of the wind speed. The blue curve represents the theoretical maximum extractable power while the red curve represents the extracted power assuming that the turbine tracks the optimum tip-speed ratio as long as the turbine operates below nominal power. At nominal power, the turbine blades are pitched out of the wind, in order to keep the extracted power at a constant level. In Fig. 2.7 this constant level is 2 MW but in order to compensate losses in the remaining turbine parts this power level will be slightly higher. Further, when evaluating different concepts, the speed range of the turbine may for some reason be limited and hence the turbine will have to operate at a non-optimum tip-speed ratio which also will change the red curve in Fig. 2.7. As an example, the green curve in Fig. 2.7 appears if the maximum tip speed is limited[2] to 72m/s. Having the tip speed and power extracted from the wind the rotational speed ω_{r0} and torque T_{r0} on the main shaft can be calculated:

$$\omega_{r0} = \frac{\lambda \cdot v_{wind}}{r_{rt}} \tag{2.7}$$

$$T_{r0} = \frac{P_{tur} \cdot r_{rt}}{\lambda \cdot v_{vwind}} \tag{2.8}$$

where r_{rt} is the radius of the swept area, i.e. the length of the turbine blade.

2.3 Model of the gear train

In wind turbines containing a gear box, a considerable part of the turbine losses are dissipated in the gear box. Since the speed operating area may differ from one turbine topology to another, speed- and torque dependent losses (if any) in the gear box may change the loss distribution and hence the result on generated energy. For instance, limiting the speed operating range will on the one hand reduce the energy captured from the wind (as described in section 1.1.1) but on the other, the losses of the gear box may decrease correspondingly. Hence the losses of the gear box have to be modeled.

[1]This expression has already been stated in eq. 1.1 on page 5 but for completeness of the model description it is repeated in this context.

[2]This limit could e.g. be introduced to lower the emitted noise from the wind turbine.

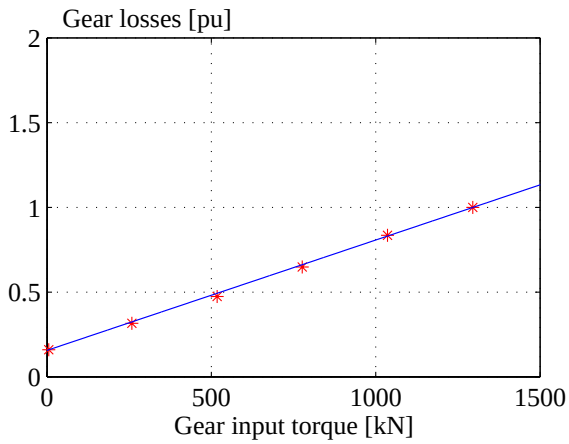

Figure 2.8: *Gear losses versus input torque to the gear. The rotational speed ω_{r0} is fixed to 1.75 [rad/s].*

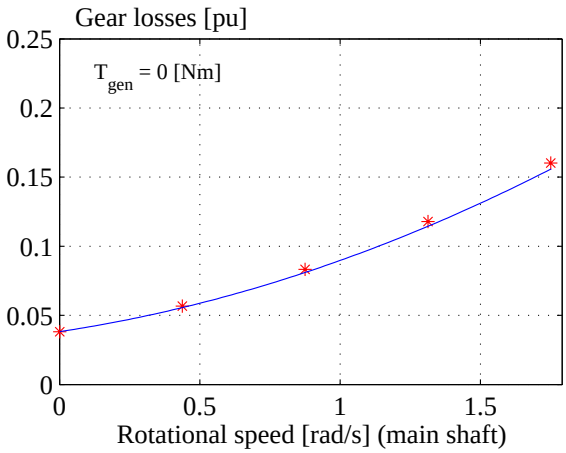

Figure 2.9: *Gear losses versus rotational speed. The output torque T_{gen} of the gear is 0 [Nm].*

2.3.1 Gear loss model

Input to the gear model is the applied torque and rotational speed on the main shaft of the turbine while output from the model is the torque and rotational speed applied on the generator shaft. To calculate these output quantities, the power losses in gear box have to be modeled. Based on the normalized loss data in Table II and Table III, presenting load dependent losses and speed dependent losses respectively, the following loss model of the gear box is assumed [14]:

$$P_{gear,loss} = \underbrace{k_{g1} \cdot \omega_{r0}^2}_{\text{Viscous fric.}} + \underbrace{k_{g2} \cdot \omega_{r0}}_{\text{Static fric.}} + \underbrace{k_{g3} \cdot \omega_{r0} \cdot T_{r0}}_{\text{Mesh fric.}} + \underbrace{k_{g4}}_{\text{Aux power}} \tag{2.9}$$

To justify the modeling approach described by eq. (2.9), the term $k_{g1} \cdot \omega_{r0}^2$ represents some viscous friction losses arising from e.g. friction in the bearings, $k_{g2} \cdot \omega_{r0}$ and $k_{g3} \cdot T_{r0} \cdot \omega_{r0}$ represents some losses due to static friction , where it is assumed that the static friction increases as the torque increases due to torsion deformation of the

TABLE II: *Measured gear loss data.*

Gear input torque [kN]	Gear loss [pu] (ω_r = 1.75 [rad/s])
6.86	0.160
260.0	0.315
519.4	0.474
778.2	0.648
1037.7	0.835
1297.1	1

TABLE III: *Measured gear loss data*

Rotational speed [rad/s]	Gear loss data ($P_{gear,out}$ = 0 [kW])
0	0.038
0.438	0.057
0.875	0.083
1.313	0.118
1.750	0.160

TABLE IV: *Normalized gear loss modeling parameters.*

Description	Symbol	Value	Unit
Viscous friction coefficient	k_{g1}	0.0209	[pu]
Static friction coefficient	k_{g2}	0.0307	[pu]
Mesh friction coefficient	k_{g3}	$3.72{\cdot}10^{-7}$	[pu]
Constant loss	k_{g4}	0.0382	[pu]

gear box and due to the friction from the teeth sliding on each other. The latter is also denoted mesh friction. Finally, the constant loss contribution k_{g4} models the power used for cooling and circulation of the gear oil. Fitting the modeling approach in eq. (2.9) on the measured data in Table II and Table III give the parameter values listed in Table IV. The solid line in Fig. 2.9 and Fig. 2.8 is obtained using the model in eq. (2.9) while the (*) represent the measured data in Table II and Table III.

2.3.2 Power transferred to the generator

In steady state operation, the rotational speed on the primary- and secondary side relates to each other simply by the gear ratio N_{gear}:

$$\omega_{gen} = N_{gear} \cdot \omega_{r0} \tag{2.10}$$

where ω_{gen} is the speed on the high speed shaft and ω_{r0} is the speed of the main shaft. For the turbine considered in this context, the gear ratio, N_{gear}, is 100.5. To satisfy energy conservation, the steady state torque T_{gen} applied to the generator shaft is then given by:

$$T_{gen} = \frac{\omega_{r0} \cdot T_{r0} - P_{gear,loss}}{\omega_{gen}} \tag{2.11}$$

2.4 Model of the generator

As the component interfacing directly to the power converter, the doubly-fed induction generator has a great impact on both the converter design and the converter losses and as so the modeling of the generator may appear a little more detailed than the modeling approaches described in the previous sections. The modeling described in this section has two purposes 1) establish a model in order to be able to calculate the generator losses. 2) Establish a model to be able to calculate the currents and voltages which the power converter should be able to manage. The starting point for the generator modeling is the parameters normally available in the generator documentation provided by the generator manufacturer[3]. However, since some of these parameter values are to be considered as confidential material they are intentionally not listed in the thesis.

[3]Data sheets provided by the generator manufactures to Vestas Wind Systems A/S and as so not necessarily public available.

TABLE V: *Generator friction loss modeling parameters.*

Description	Symbol	Value	Unit
Static friction coefficient	k_1	$5.49 \cdot 10^{-4}$	[pu]
Viscous friction coefficient	k_2	$1.61 \cdot 10^{-6}$	[pu]
Ventilation friction loss	k_3	$1.58 \cdot 10^{-7}$	[pu]

2.4.1 Generator loss model

The considered losses in the DFIG are: the friction losses, the copper losses and the iron losses.

Friction losses

Conventionally, friction losses of electrical machines are modeled by [6, 15]:

$$P_{fric} = \underbrace{k_1 \cdot \omega_{gen}}_{\text{Static fric.}} + \underbrace{k_2 \cdot \omega_{gen}^2}_{\text{Viscous fric.}} + \underbrace{k_3 \cdot \omega_{gen}^3}_{\text{Ventilation}} \tag{2.12}$$

where the total friction losses consist of the sum of static friction losses, viscous friction losses and ventilation losses. Fitting the model in eq. (2.12) on the measured generator losses in Table VI, the loss coefficients in Table V are obtained. The measured and modeled friction losses are shown in Fig. 2.10.

Copper losses

The copper losses of the generator is simply modeled by:

$$P_{cu} = 3 \cdot \left(R_s \cdot I_s^2 + R_r \cdot I_r^2\right) \tag{2.13}$$

TABLE VI: *Measured friction losses.*

Rotational speed [rad/s]	Friction losses [pu]
0.0	0.0
89.0	0.161
115.2	0.322
117.3	0.342
147.7	0.624
159.2	0.765
169.6	0.906
175.9	1

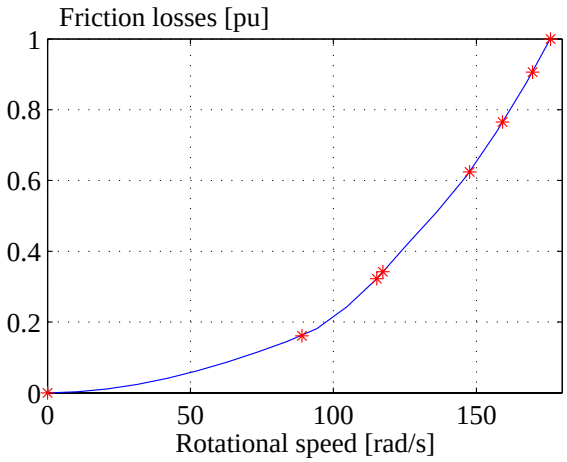

Figure 2.10: *Measured and modeled rotational losses.*

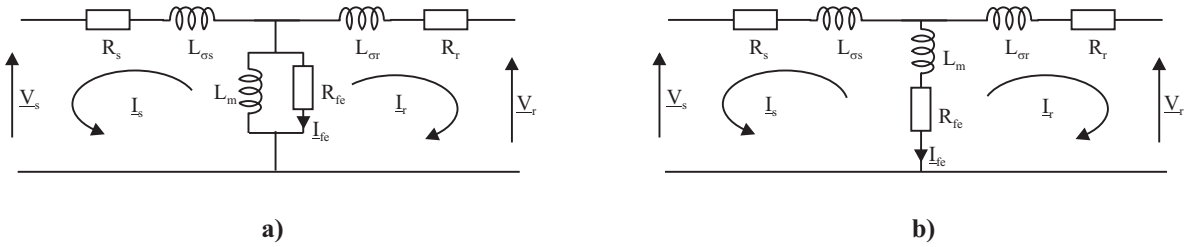

Figure 2.11: *Iron loss modeling approaches.* **a)** *Iron loss resistance in parallel.* **b)** *Iron loss resistance in series.*

where R_s and R_r are the stator- and rotor resistance respectively and I_s and I_r are the stator- and rotor currents. Since the actual value of the resistances very much depend on the winding temperature, i.e. the loading conditions as well as the rotor resistance changes with the changes in the slip[4], eq. (2.13) will have to account for both winding temperature and generator speed. These secondary effects are treated in section 2.4.3.

Iron losses

The iron losses P_{fe} of an induction machine are typically modeled by a resistor R_{fe}, placed either in parallel or in series with the magnetizing inductance [1]. Fig. 2.11 shows the two different modeling approaches. For most applications (motor drives), the two models only manage to calculate equal losses in one certain working condition (a certain voltage and frequency) while in all other conditions different results are obtained. In the present application the magnetization level and the stator frequency is nearly constant, determined by the applied stator voltage and hence it does not matter on the results whether a series model or a parallel model is used. The iron losses are simply modeled as:

$$P_{fe} = 3 \cdot R_{fe} \cdot I_{fe}^2 \tag{2.14}$$

where I_{fe} is the current through the (fictional) iron loss resistance, c.f. Fig. 2.11.

2.4.2 Power transferred to the converter

Input to the generator model is the power (in shape of torque T_{gen} and rotational speed ω_{gen}) applied on the generator shaft, the stator voltage $\underline{V}_s$ and the desired stator reactive power Q_s, while output from the model has to be stator current $\underline{I}_s$, rotor current $\underline{I}_r$ and rotor voltage $\underline{V}_r$. By use of the equivalent diagrams in Fig. 2.11 and neglecting the iron loss resistance, the steady state equations for the doubly-fed induction generator become:

$$\begin{bmatrix} \underline{V}_s \\ \underline{V}_r \end{bmatrix} = \begin{bmatrix} -R_s - j \cdot \omega_s \cdot L_s & -j \cdot \omega_s \cdot L_m \\ j(\omega_r - \omega_s)L_m & -R_r + j(\omega_r - \omega_s)L_r \end{bmatrix} \cdot \begin{bmatrix} \underline{I}_s \\ \underline{I}_r \end{bmatrix} \tag{2.15}$$

[4]The slip is defined in eq. (2.16).

where the quantities $\underline{V}$ and $\underline{I}$ represent phasors, ω_s is the grid angular frequency and ω_r is the rotor angular frequency in electrical measure[5]. Introducing the slip s defined by:

$$s = \frac{\omega_r - \omega_s}{\omega_s} \tag{2.16}$$

eq. (2.15) is rewritten in the form:

$$\begin{bmatrix} \underline{V}_s \\ \underline{V}_r \end{bmatrix} = \begin{bmatrix} -R_s - j \cdot \omega_s \cdot L_s & -j \cdot \omega_s \cdot L_m \\ j \cdot s\omega_s \cdot L_m & -R_r + j \cdot s \cdot \omega_s L_r \end{bmatrix} \cdot \begin{bmatrix} \underline{I}_s \\ \underline{I}_r \end{bmatrix} \tag{2.17}$$

By inversion of the generator impedance matrix in eq. 2.17, the generator stator - and rotor currents become:

$$\begin{bmatrix} \underline{I}_s \\ \underline{I}_r \end{bmatrix} = \begin{bmatrix} a_{11} + j \cdot b_{11} & a_{12} + j \cdot b_{12} \\ a_{21} + j \cdot b_{21} & a_{22} + j \cdot b_{22} \end{bmatrix} \cdot \begin{bmatrix} \underline{V}_s \\ \underline{V}_r \end{bmatrix} \tag{2.18}$$

where the parameters $a_{11}..b_{22}$ are given by:

$$a_{11} + j \cdot b_{11} = \frac{-R_r + j \cdot s\omega_s \cdot L_r}{R_s R_r - s \cdot \omega_s^2 (L_m^2 - L_s L_r) + j \cdot \omega_s (L_s R_r - s \cdot R_s L_r)} \tag{2.19}$$

$$a_{12} + j \cdot b_{12} = \frac{j \cdot \omega_s L_m}{R_s R_r - s \cdot \omega_s^2 (L_m^2 - L_s L_r) + j \cdot \omega_s (L_s R_r - s \cdot R_s L_r)} \tag{2.20}$$

$$a_{21} + j \cdot b_{21} = \frac{-j \cdot s\omega_s \cdot L_m}{R_s R_r - s \cdot \omega_s^2 (L_m^2 - L_s L_r) + j \cdot \omega_s (L_s R_r - s \cdot R_s L_r)} \tag{2.21}$$

$$a_{22} + j \cdot b_{22} = \frac{-R_s - j \cdot \omega_s \cdot L_s}{R_s R_r - s \cdot \omega_s^2 (L_m^2 - L_s L_r) + j \cdot \omega_s (L_s R_r - s \cdot R_s L_r)} \tag{2.22}$$

The effort left is then to find the rotor voltage which have to be applied by the rotor inverter. From the definition of reactive stator power Q_s given by:

$$Q_s = 3\Im m(\underline{V}_s \cdot \underline{I}_s^*) \tag{2.23}$$

and substituting the stator current $\underline{I}_s$ by the expression in eq. (2.18), the imaginary component of the rotor voltage V_{r2} becomes:

$$V_{r2} = \frac{V_{s2}\, a_{12}\, V_{r1} - {V_{s2}}^2 b_{11} - b_{11}\, {V_{s1}}^2 - V_{s1}\, b_{12}\, V_{r1} - \frac{1}{3} Q_s}{V_{s1}\, a_{12} + V_{s2}\, b_{12}} \tag{2.24}$$

To derive the real part of the rotor voltage V_{r1} the active power balance of the generator is used:

$$\omega_{gen} T_{gen} = P_s + P_r + P_{gen,loss} \tag{2.25}$$

where $P_{gen,loss}$ is the generator power losses given by the sum of eq. (2.12), eq. (2.13) and eq. (2.14) and the rotor active power P_r and stator active power P_s is given by:

$$P_r = 3\Re e(\underline{V}_r \cdot \underline{I}_r^*) \tag{2.26}$$

$$P_s = 3\Re e(\underline{V}_s \cdot \underline{I}_s^*) \tag{2.27}$$

[5]The rotor angular frequency in electrical measure ω_r is simply related to the mechanical angular frequency of the rotor ω_{gen} by the number of pole pairs P_p. That is: $\omega_r = P_p \cdot \omega_{gen}$

Combining eq. (2.18), (2.25), (2.26) and (2.27), the real part of the phasor $\underline{V}_r$ can be found by solving the second order equation:

$$k_1 V_{r1}^2 + k_2 V_{r1} + k_3 = 0 \tag{2.28}$$

where the coefficients $k_1..k_3$ are given by

$$k_1 = \frac{a_{22}\left(b_{12}^2 V_{s2}^2 + a_{12}^2 V_{s1}^2 + b_{12}^2 V_{s1}^2 + a_{12}^2 V_{s2}^2\right)}{\left(b_{12}V_{s2} + a_{12}V_{s1}\right)^2} \tag{2.29}$$

$$\begin{aligned} k_2 = & \frac{\left(a_{12}^3 + a_{21}a_{12}^2 + b_{12}^2 a_{12} + 2b_{12}a_{22}b_{11} - b_{12}b_{21}a_{12}\right)V_{s1}^3}{\left(V_{s2}b_{12} + V_{s1}a_{12}\right)^2} + \\ & \frac{\left(b_{12}^3 + a_{12}^2 b_{12} + a_{12}a_{21}b_{12} - b_{21}b_{12}^2 - 2a_{12}a_{22}b_{11}\right)V_{s2}^3}{\left(V_{s2}b_{12} + V_{s1}a_{12}\right)^2} + \\ & \frac{\left(b_{12}^3 + a_{12}^2 b_{12} - b_{12}^2 b_{21} + a_{21}b_{12}a_{12} - 2b_{11}a_{12}a_{22}\right)V_{s1}^2 V_{s2}}{\left(V_{s2}b_{12} + V_{s1}a_{12}\right)^2} + \\ & \frac{\left(a_{12}^3 + a_{12}^2 a_{21} + 2b_{12}a_{22}b_{11} + b_{12}^2 a_{12} - b_{21}a_{12}b_{12}\right)V_{s1}V_{s2}^2}{\left(V_{s2}b_{12} + V_{s1}a_{12}\right)^2} + \\ & \frac{\frac{2}{3}\left(b_{12}V_{s1} - a_{12}V_{s2}\right)a_{22}Q_s}{\left(V_{s2}b_{12} + V_{s1}a_{12}\right)^2} \end{aligned} \tag{2.30}$$

$$\begin{aligned} k_3 = & \frac{(b_{11}^2 a_{22} - b_{11}b_{21}a_{12} + b_{12}b_{11}a_{12} + a_{11}a_{12}^2)V_{s1}^4}{(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{(a_{11}b_{12}^2 - a_{12}b_{11}b_{12} - b_{11}a_{21}b_{12} + b_{11}^2 a_{22})V_{s2}^4}{(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{(-b_{11}a_{12}^2 + b_{12}^2 b_{11} - b_{11}b_{21}b_{12} - b_{11}a_{21}a_{12} + 2a_{11}b_{12}a_{12})V_{s1}^3 V_{s2}}{(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{(b_{11}b_{12}^2 - a_{12}^2 b_{11} - b_{11}b_{21}b_{12} - b_{11}a_{21}a_{12} + 2a_{11}a_{12}b_{12})V_{s2}^3 V_{s1}}{(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{(2b_{11}^2 a_{22} + a_{11}b_{12}^2 + a_{11}a_{12}^2 - b_{11}b_{21}a_{12} - b_{11}a_{21}b_{12})V_{s1}^2 V_{s2}^2}{(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{(2b_{11}a_{22} - b_{21}a_{12} + b_{12}a_{12})V_{s1}^2 Q_s}{3(V_{s2}b_{12} + V_{s1}a_{12})^2} + \frac{(\frac{1}{3}P_{gen,loss}a_{12}^2 - \omega_{gen}T_{gen}a_{12}^2)V_{s1}^2}{3(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{(2b_{11}a_{22} - a_{21}b_{12} - a_{12}b_{12})V_{s2}^2 Q_s}{3(V_{s2}b_{12} + V_{s1}a_{12})^2} + \frac{(P_{gen,loss}b_{12}^2 - \omega_{gen}T_{gen}b_{12}^2)V_{s2}^2}{3(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{(b_{12}^2 Q_s - a_{21}a_{12}Q_s - a_{12}^2 Q_s - b_{21}b_{12}Q_s)V_{s1}V_{s2}}{3(V_{s2}b_{12} + V_{s1}a_{12})^2} + \\ & \frac{a_{22}Q_s^2 + (6P_{gen,loss}b_{12}a_{12} - 6\omega_{gen}T_{gen}b_{12}a_{12})V_{s1}V_{s2}}{9(V_{s2}b_{12} + V_{s1}a_{12})^2} \end{aligned} \tag{2.31}$$

It should be noted, that alignment of the stator voltage phasor $\underline{V}_s$ to e.g. the real axis of the coordinate system, i.e $V_{s2} = 0$, significantly reduce the efforts of calculating the coefficients $k_1..k_3$. However, for completeness the coefficients are derived for an arbitrary alignment of the stator voltage phasor.

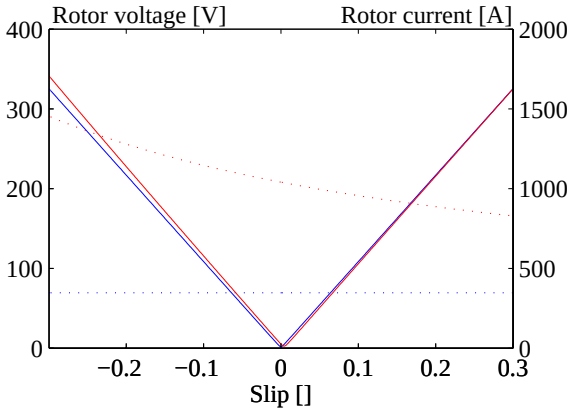

Figure 2.12: *Rotor voltage (-) and rotor current (· · ·) calculated at no load (-) and full load (-) respectively.*

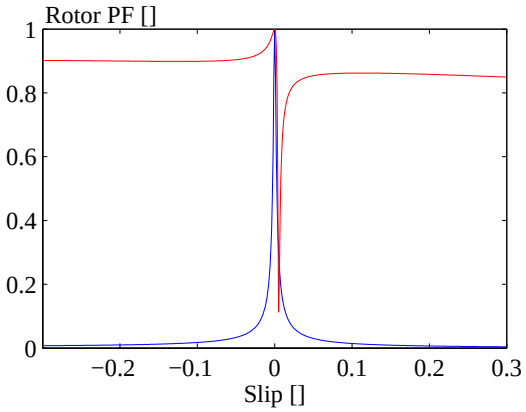

Figure 2.13: *Load angle of rotor inverter vs. slip, calculated at no load (-) and full load (-) respectively.*

Solving eq. (2.28) and choosing the solution implying the lowest amount of circulating power, i.e lowest amplitude of the rotor voltage, the real part of the rotor voltage can finally be calculated. Fig. 2.12 shows the rotor voltage and the rotor current as a function of the slip, calculated at no load and full load respectively. Fig. 2.13 shows the corresponding load angle of the rotor inverter, also in both no load and full load condition.

2.4.3 Generator secondary effects

Principally, the power losses of the generator has been described by eq. (2.12), eq. (2.13) and eq. (2.14) and the power transferred to the converter has been described by eq. (2.18) eq. (2.24), and eq. (2.28) but since a number of secondary effects may change some of the implied parameters and hereby the calculated losses, currents and voltages, this section will describe the modeling of some of the major secondary effects.

Modeling of skin effects

In large machines, skin effects in the rotor windings are quite pronounced and hence the rotor resistance increases when the slip frequency increases (regarding skin effects, the slip is evaluated as an absolute value). To account for the skin effects, the rotor resistance has been modeled as a linear function of the slip frequency given by [19, 20]:

$$R_r = R_{r|s=0} + |s| \cdot (R_{r|s=1} - R_{r|s=0}) \tag{2.32}$$

where $R_{r|s=0}$ is the rotor resistance at synchronous speed and $R_{r|s=1}$ is the rotor resistance measured in a blocked rotor test. Fig. 2.14 shows the slip dependent rotor resistance of the considered generator - normalized to the rotor resistance value at synchronous speed, i.e. s=0.

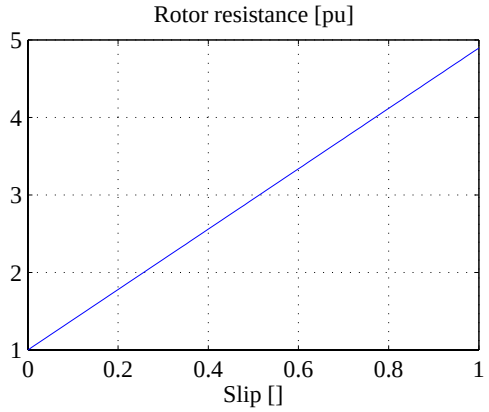

Figure 2.14: *Rotor resistance dependency of the slip. The rotor resistance is normalized to the rotor resistance at synchronous speed.*

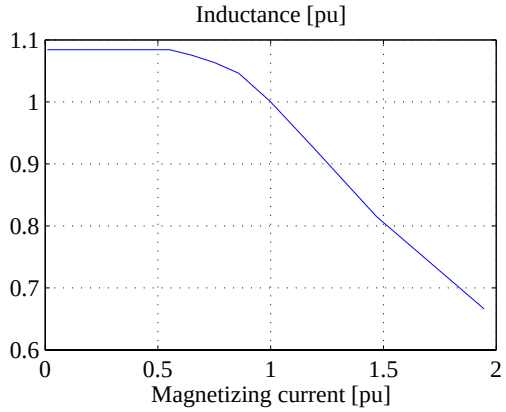

Figure 2.15: *Main inductance vs. magnetizing current. The main inductance is normalized to the inductance value at nominal load.*

Modeling of saturation effects

Another secondary effect which may influence the calculated losses as well as the calculated currents and voltages is the saturation of the main inductance L_m. As argued in the modeling of the iron losses on page 32, the magnetization level in the doubly-fed system is almost fixed by the applied stator voltage and hence it may appear non relevant for the steady state considerations. However, over- and under voltages at the grid as well as high demands for reactive power consumption/generation may change the generator magnetization level and hence for converter design purposes it may be important to include the saturation effect. Fig. 2.15 illustrates the saturation effect of the main inductance in the considered generator. The inductance and magnetizing current is normalized to their values at nominal loading conditions.

Modeling of thermal effects

The last of the considered secondary effects is the temperature dependency of the generator resistances. To account for the temperature effects, the temperature of the windings have to be estimated. The steady state temperature T_s of the stator and T_r of the rotor is determined as:

$$T_s = \alpha_s \cdot P_{s,loss} + T_{amb} \tag{2.33}$$

$$T_r = \alpha_r \cdot P_{r,loss} + T_{amb} \tag{2.34}$$

where the thermal resistance α_s and α_r of the stator and rotor respectively are calculated from the temperature rice at nominal load. Based on the calculated temperatures, the resistances of the stator- and rotor winding in the present working point is calculated

as:

$$R_s = R_{s0} + \alpha_{cu} \cdot (T_s - T_0) \tag{2.35}$$

$$R_r = R_{r0} + \alpha_{cu} \cdot (T_r - T_0) \tag{2.36}$$

The resistances R_{s0} and R_{r0} are the stator- and rotor resistance measured at temperature T_0. The coefficient α_{cu} is the temperature coefficient of resistivity of the considered material.

2.4.4 Simplified generator model

For the purpose of pre-design issues and rough calculations, the comprehensive generator modeling approach described so far seems to be a little too complicated and detailed. Hence, for these purposes a more straight forward method is desirable, although this is obtained on the expense of precision.

Assuming an ideal lossless generator, i.e. a generator with no leakage inductances and no resistances, it appears from eq. 2.17 that stator voltage and rotor voltage is simply related by the slip of the generator:

$$|\tilde{\underline{V}}_r| = s|\underline{V}_s| \tag{2.37}$$

where the $\tilde{}$ indicates that the result is obtained under the assumption of an ideal generator. Continuing this simplified approach, the relation between shaft power given by $\omega_{gen}T_{gen}$, stator power $\tilde{P}_s$ and rotor power $\tilde{P}_r$ can be derived from eq. (2.18), (2.25), (2.26) and (2.27):

$$\tilde{P}_s = \frac{\omega_{gen}T_{gen}}{1+s} \tag{2.38}$$

$$\tilde{P}_r = \frac{s(\omega_{gen}T_{gen})}{1+s} \tag{2.39}$$

The reactive rotor power is given by:

$$\tilde{Q}_r = s \cdot \left(Q_s^* + \frac{3|\underline{V}|_s^2}{\omega_s L_m} \right) \tag{2.40}$$

where Q_s^* is the desired reactive power to be generated from the stator. The rotor current, can then be roughly estimated by:

$$|\tilde{\underline{I}}_r| = \frac{\sqrt{\tilde{P}_r^2 + \tilde{Q}_r^2}}{3 \cdot s \cdot |\underline{V}_s|} \tag{2.41}$$

In eq. (2.37) and eq. (2.41) it is assumed that the generator winding ratio, i.e. ratio between rotor windings and stator windings, is unity. To account for an arbitrary winding ratio, eq. (2.37) should be multiplied by the winding ratio whereas eq. (2.41) should be divided by the winding ratio.

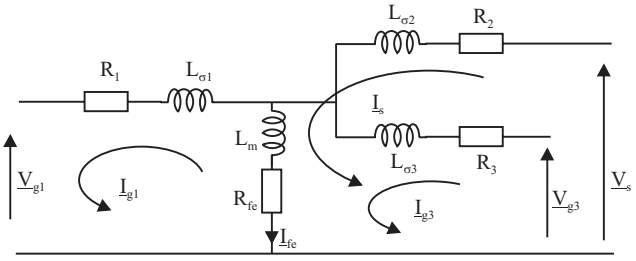

Figure 2.16: *Equivalent diagram of the three phase three winding transformer. All parameters are transferred to the primary side.*

2.5 Model of the transformer

According to Fig. 2.1 on page 23 the last component to be modeled is the transformer. The purpose of the transformer modeling is: 1) To calculate the losses in the transformer and 2) to calculate the power transferred to the grid (which actually was the purpose of all the modeling approaches described in this chapter). Input to the transformer model is the voltage applied on the primary side of the transformer, i.e. the grid voltage $\underline{V}_{g1}$, the current generated by the generator stator $\underline{I}_s$ and the current generated by the grid side inverter $\underline{I}_{g3}$ while output have to be the current $\underline{I}_{g1}$ generated to the grid and the voltages $\underline{V}_s$ and $\underline{V}_{g3}$ applied on the generator stator and grid inverter respectively . Fig. 2.16 shows an equivalent diagram of the three winding transformer, defining the current directions and parameters used in the transformer modeling.

2.5.1 Transformer losses

The considered transformer losses are: Copper losses and iron losses.

Copper losses

From the notation in the transformer equivalent diagram in Fig. 2.16, the copper losses of the transformer is simply modeled by:

$$P_{cu,trafo} = 3 \cdot (R_1 \cdot I_{g1}^2 + R_2 \cdot I_s^2 + R_3 \cdot I_{g3}^2) \tag{2.42}$$

Iron losses

As for the generator, the iron losses $P_{fe,trafo}$ of the transformer can be modeled either as a resistance in series or in parallel with the mutual inductance. As argued previously, since the voltage and frequency applied to the transformer is almost constant, it does not matter on the results whether a series or parallel model is used. For the series model (as shown in Fig. 2.16) the transformer iron losses are simply calculated by:

$$\begin{aligned} P_{fe,trafo} &= 3 \cdot (R_{fe} \cdot I_{fe}^2) \\ &= 3 \cdot (R_{fe} \cdot |\underline{I}_{g1} - \underline{I}_s - \underline{I}_{g3}|^2) \end{aligned} \tag{2.43}$$

2.5.2 Power transferred to the grid

The steady state equation for the transformer is given by:

$$\underbrace{\begin{bmatrix}\underline{V}_{g1}\\ \underline{V}_{s}\\ \underline{V}_{g3}\end{bmatrix}}_{\underline{V}_{trafo}} = \underbrace{\begin{bmatrix}-R_1-R_{fe}-j\omega_s L_1 & j\omega_s L_m & j\omega_s L_m\\ -j\omega_s L_m & R_2+R_{fe}+j\omega_s L_2 & j\omega_s L_m\\ -j\omega_s L_m & j\omega_s L_m & R_3+R_{fe}+\omega_s L_3\end{bmatrix}}_{\underline{\underline{X}}_{trafo}} \underbrace{\begin{bmatrix}\underline{I}_{g1}\\ \underline{I}_{s}\\ \underline{I}_{g3}\end{bmatrix}}_{\underline{I}_{trafo}} \tag{2.44}$$

where $L_{1..3}$ is the self inductance of the considered winding i.e. $L_{1..3} = L_{\sigma 1..3} + L_m$, L_m is the mutual inductance and $R_{1..3}$ is the resistance of the considered winding. The parameters used for the transformer modeling are all derived from standard measurements, i.e. short circuit and no load tests. Since the unknowns in eq. (2.44) are the grid current $\underline{I}_{g1}$, the stator voltage $\underline{V}_s$ and the grid inverter voltage $\underline{V}_{g3}$, the equation has to be rearranged. In short form, eq. (2.44) can be written as:

$$[\underline{V}_{trafo}] = [\underline{\underline{X}}][\underline{I}_{trafo}] \tag{2.45}$$

and by inversion of the impedance matrix $\underline{\underline{X}}$, the transformer currents can be calculated by:

$$[\underline{I}_{trafo}] = [\underline{\underline{Y}}][\underline{V}_{trafo}] \tag{2.46}$$

Combining eq. (2.45) and eq. (2.46) the unknown currents and voltages can be found:

$$\begin{bmatrix}\underline{I}_{g1}\\ \underline{V}_{s}\\ \underline{V}_{g3}\end{bmatrix} = \begin{bmatrix}\frac{y_{11}}{(1-y_{12}x_{21}-y_{13}x_{31})} & \frac{(y_{12}x_{22}+y_{13}x_{32})}{(1-y_{12}x_{21}-y_{13}x_{31})} & \frac{(y_{12}x_{23}+y_{13}x_{33})}{(1-y_{12}x_{21}-y_{13}x_{31})}\\ \frac{x_{21}y_{11}}{(1-y_{12}x_{21}-y_{13}x_{31})} & \frac{x_{21}(y_{12}x_{22}+y_{13}x_{32})}{(1-y_{12}x_{21}-y_{13}x_{31})+x_{22}} & \frac{x_{21}(y_{12}x_{23}+y_{13}x_{33})}{(1-y_{12}x_{21}-y_{13}x_{31})+x_{23}}\\ \frac{x_{31}y_{11}}{(1-y_{12}x_{21}-y_{13}x_{31})} & \frac{x_{31}(y_{12}x_{22}+y_{13}x_{32})}{(1-y_{12}x_{21}-y_{13}x_{31})+x_{32}} & \frac{x_{31}(y_{12}x_{23}+y_{13}x_{33})}{(1-y_{12}x_{21}-y_{13}x_{31})+x_{33}}\end{bmatrix}\begin{bmatrix}\underline{V}_{g1}\\ \underline{I}_{s}\\ \underline{I}_{g3}\end{bmatrix} \tag{2.47}$$

where x_{ij} and y_{ij} are the i, j element in the X and Y matrices in eq. (2.45) and eq. (2.46).

2.5.3 Transformer secondary effects

As for the generator, secondary effects such as saturation and thermal effects may slightly change the calculated transformer voltages and transformer currents. To include these secondary effects, the procedures described in section 2.4.3 on page 35 have to be applied on the transformer parameters.

2.6 Grid interface

As a consequence of the increasing wind power penetration, the different national grid operators are more and more concerned about the stability and reliability of their power systems [5]. Hence, during the last few years, several national grid codes have been published, concerning the behaviour of the wind turbine (or wind turbine park), both

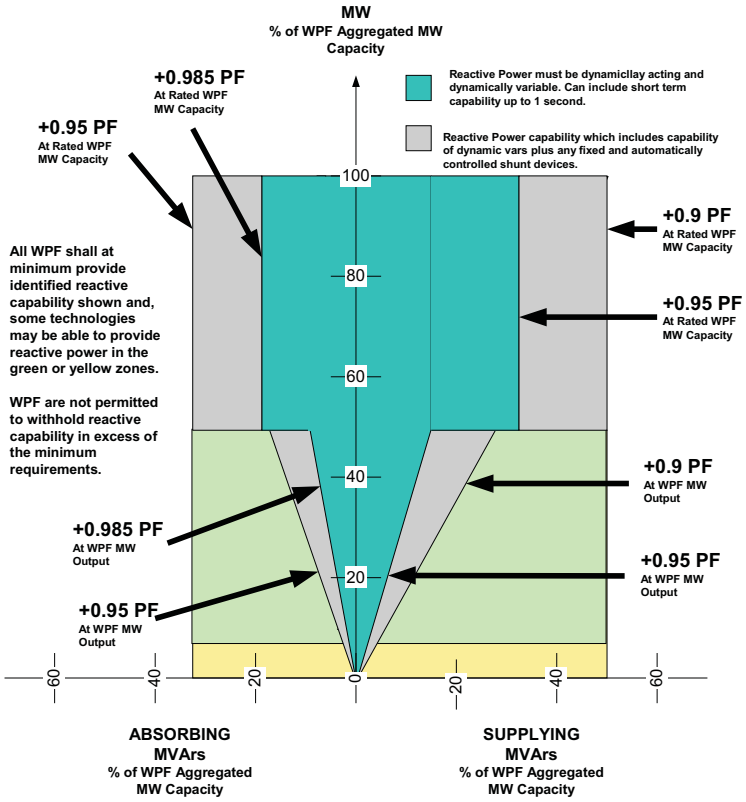

Figure 2.17: *Example of the reactive power capability requirement [2]*

under normal operation and during grid faults [11, 12, 13, 16]. Since the national grid codes around the world are quite different and the individual grid codes are changing quite often, the demands listed in this section should be considered as examples and as they appeared at the time this chapter was prepared.

For the purpose of this thesis, only the requirements regarding steady state operation are considered. Further since the national requirements deviate very much from each other and since some of the requirements may have an influence on the converter evaluation results it will be stretched out for which requirement the converters are to be evaluated.

2.6.1 Reactive power generation and voltage regulation

To provide voltage control in the point of common connection (PPC), many grid codes include requirements for the reactive power capability of a wind turbine (or wind turbine park). An example of such requirements for reactive power capability is shown Fig. 2.17. The requirements illustrated in Fig. 2.17 distinguishes between dynamically controllable reactive power and more or less statically controllable reactive power, where the dynamically controllable reactive power may have to be provided by an active converter e.g. the rotor- or grid inverter in the doubly fed system while the statically part of the reactive power may be provided by passive shunt elements. If the dynamically controllable power are to be provided by the converter in the doubly fed system it obviously influence

TABLE VII: *Reactive power requirements.*

Grid code	Country/region	PF-range (Absorb-supply)
AESO	Canada (Alberta)	0.9-0.9
E.ON	Germany	0.95-0.95
ESB	Ireland	0.95-0.85
NECA	Australia	1 - 0.95
NGC	England/Wales	0.95-0.95
Elkraft/Eltra	Denmark	1

the converter ratings and the system power losses. Further, since other national grid codes have other requirements for the reactive power capability, the converter design and evaluation results will be influenced by the considered grid code. To exemplify the diversity among the different grid codes Table VII lists the reactive power requirements from some selected grid codes.

In the evaluation of the converter topologies in this thesis, the Danish requirements will be used, i.e. the turbine should provide no reactive power consumption or generation. However, all equations and methods described throughout the thesis can be applied for any reactive power requirements.

2.6.2 Voltage and frequency range

As for the reactive power requirements, the steady state voltage and frequency range in which the turbines are required to remain connected deviate very much from one grid code to another. Fig. 2.18 and Fig. 2.19 illustrate some selected requirements on the voltage and frequency range[6], all normalized to their nominal values. The upper voltage limit (even the short term limits) clearly influence the choice of converter voltage ratings (or converter voltage level) while the lower steady state voltage levels influence the current ratings of the converter. To comply with the selected voltage requirements in Fig. 2.18 the converter will have to be designed for 25% over-voltage and 10% under-voltage unless other precautions are incorporated in the turbine design. Regarding the frequency the lower limits may slightly influence the magnetization level of the generator and transformer and thereby increase the current ratings of the rotor inverter.

In the converter evaluation throughout this thesis, nominal voltage and frequency will be used, both for the converter design and the converter evaluation.

[6]The voltage requirements are normally stated on the HV side of the main transformer in PCC.

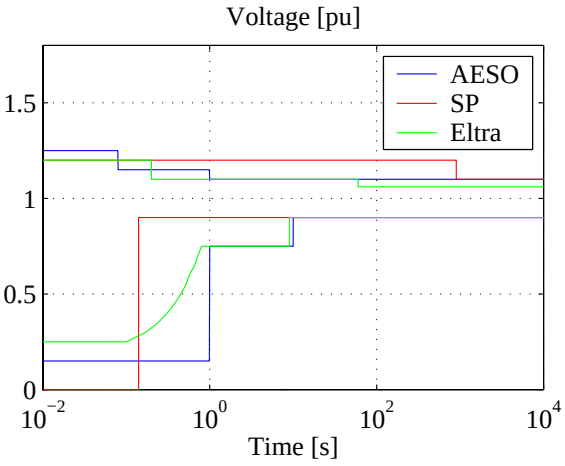

Figure 2.18: *Voltage range requirements for wind turbines.*

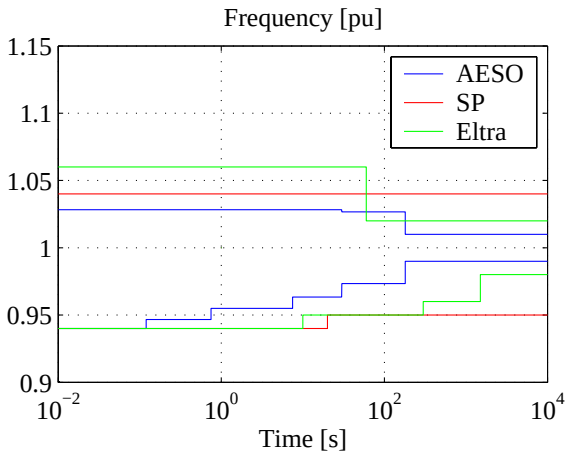

Figure 2.19: *Frequency requirements for wind turbines.*

2.6.3 Power quality

Current harmonics in the supply grid are undesirable since they increase the grid power losses and causes voltage fluctuations, especially in weak electrical networks. Generally, the allowed emission of current harmonics depend on the stiffness of the supply grid, and requirements on harmonics are often stated on the voltage in PCC rather than the generated currents. Guidelines such as the IEEE 519 actually specifies limits for both the allowable harmonic current content and on the allowable voltage distortion at PCC whereas [17] solely calculates the amount of allowable current harmonics based on the allowable harmonic voltage. According to [17], the allowable harmonic current content can be calculated by:

$$I_n \leq V_n \cdot \sqrt{\frac{1+(\tan(\Psi_{sc}))^2}{1+(n\cdot\tan(\Psi_{sc}))^2}} \cdot \frac{S_{sc}}{S_{trafo}} \tag{2.48}$$

where I_n is the considered harmonic current, V_n is the allowed harmonic voltage, S_{sc} is the short circuit power in PCC, Ψ_{sc} is the short circuit angle and S_{trafo} is the apparent power rating of the main transformer. In addition to the individual harmonic limits, the total harmonic distortion THD_i of the input current is in some cases considered. The total harmonic distortion of the current, THD_i in percent, is defined as [10]:

$$THD_i = 100 \times \sqrt{\sum_{h\neq 1}\left(\frac{I_h}{I_1}\right)^2} \tag{2.49}$$

2.7 Summary

This chapter has described the modeling of the components interfacing directly or indirectly to the power converter. The purpose of the modeling has been: 1) to identify the power flow and thereby identify the current and voltage ratings for the considered

converter and 2) to calculate the losses of the different components in order to evaluate the annual energy production. Since the upcoming national grid codes have a high impact on the necessary converter rating, the last section summarized some of the most important steady state grid code demands.

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[19] S.E. Zocholl. Inductioin motors Part I. Technical report, Schweitzer Engineering Laboratories, Inc.

[20] S.E. Zocholl. Inductioin motors Part II. Technical report, Schweitzer Engineering Laboratories, Inc.

Part II

Converter modeling

Chapter 3

The back-to-back two-level voltage source converter

SINCE the appearance of power electronic valves with intrinsic gate-turn-off capability, the two level voltage source converter has been the most widely used power processing converter for three phase motor drive applications. Probably due to the maturity obtained in the drives industry during more than a decade, the two-level voltage source converter was widely adopted by the wind turbine industry for use in large scale wind turbines in the late nineties.

Since the back-to-back two-level voltage source converter seems to be the preferred converter topology in wind turbine applications, the purpose of this chapter is to establish a foundation to compare and evaluate the back-to-back two-level voltage source converter against other converter topologies applicable for the doubly-fed wind turbine system. The chapter starts with a review on previous work, especially with focus on the use of back-to-back two-level voltage source converters in doubly-fed wind turbine applications followed by a description of the operating principles of the converter. As the control of the active switches - known as modulation - is closely related to the operating principles of the converter and crucial in the calculation of the converter losses, the chapter is continued with a quite detailed description of the most accepted modulation techniques. Finally, to be used in a converter comparison and converter evaluation, the power losses of the back-to-back two-level voltage source converter are modeled and some design aspects and design guidelines regarding component ratings are outlined.

3.1 Previous work

The majority of variable speed three phase motor drive systems covered by literature and used in industry are uni-directional with regard to power flow and although uni-directional power converters are operational in the doubly-fed wind turbine system like e.g. the so-called static Kramer drive [13, 23] or the VCRS system [1, 35] proposed by Vestas, the most efficient operation of such a doubly-fed system is achieved by use

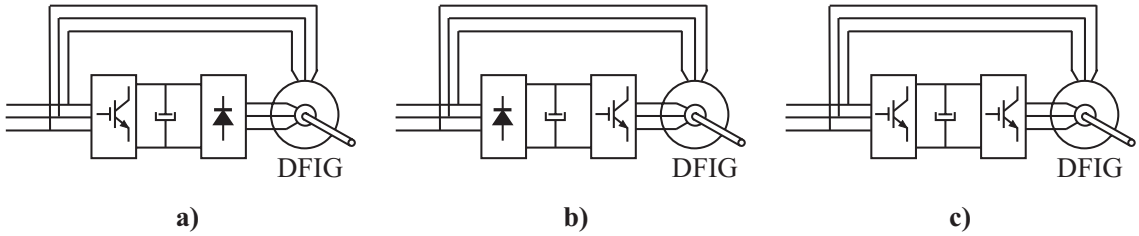


Figure 3.1: *Different wind turbine systems based in the doubly-fed induction generator and the two-level voltage source inverter.* **a)** *The static Kramer drive.* **b)** *The VCRS system.* **c)** *The back-to-back two level voltage source converter.*

of a bi-directional power converter. The three different doubly-fed induction generator based systems are illustrated in Fig. 3.1.
From the operating principles of the doubly-fed induction generator described in section 2.4 it appears that, since power is prevented from being supplied to the rotor circuit, the static Kramer drive in Fig. 3.1a is only able to generate power when operating above synchronous speed. Further, due to the passive diode rectifier on the generator side, the magnetization of the generator has to be provided from the stator, thereby reducing this systems ability to provide an efficient reactive power control. On the other hand, the VCRS system in Fig. 3.1b is only able to generate power when operating below synchronous speed while the back-to-back system shown in Fig. 3.1c is able to generate power both above and below synchronous speed which allows this system to track the optimum tip speed in a larger speed range than the static Kramer drive and the VCRS system. Further, the back-to-back system is able to provide reactive power control [36, 42] and harmonic compensation [24] both by the grid side inverter and by the rotor side inverter. From the early nineties, the majority of technical publications on variable speed wind turbines have concerned the back-to-back topology in Fig. 3.1c.

Among publications concerning the back-to-back two-level voltage source converter in wind turbine applications a bulk of these have dealt with the control aspects. Especially, focus has been on the field oriented control [12, 40, 42] and position sensor-less control [3, 4, 8, 41]. Regarding the power yield of a wind turbine based on the back-to-back two-level voltage source converter only a few comparisons has been presented. However, focus in these comparisons has been on the influence of the blade control/design [29, 39] and on the generator choice/design [14, 31] while no detailed analysis of the relationship between power yield and converter design/control (modulation) has been published. Obviously, a reason for this lack of interest is that an efficiency increase by choice/design of generator or by blade design/control is more or less directly reflected in the overall turbine efficiency while an increase in the converter efficiency is only reflected in the overall turbine efficiency by about one tenth[1]. Nevertheless, the tools and methods obtained by evaluating the converter in the doubly-fed system can be directly applied

[1]This is due to the fact that the power converter in a doubly-fed system normally processes about 10% of the overall generated power.

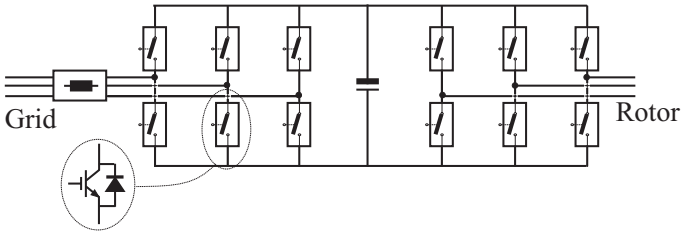


Figure 3.2: *The back-to-back two-level voltage source converter topology.*

on a full-scale converter system (which seems to be the choice for the coming turbine generations) where the converter processes the full power of the system and hence where the converter efficiency is directly reflected in the turbine efficiency.

3.2 Operating principles

The back-to-back two-level voltage source converter is a bi-directional power converter consisting of two conventional two-level voltage source inverters coupled in a back-to-back fashion. The topology is shown in Fig. 3.2.

3.2.1 Reference voltage generation

The aim for both the grid side inverter and the rotor side inverter is to synthesize a voltage that satisfy the current demand on the generator side and grid side respectively. Typically, the grid side current demand is controlled in order to keep the DC-link voltage on a certain level while the generator side current level is controlled to achieve a certain active and reactive power generation as discussed in section 2.4. To illustrate the inverter reference voltage generation Fig. 3.3 and Fig. 3.4 show typical realizations of the grid inverter reference voltage generation [30][2] and rotor inverter reference voltage generation [42] respectively.

[2]The dynamic cross coupling compensation described in [30] is not shown in Fig. 3.3.

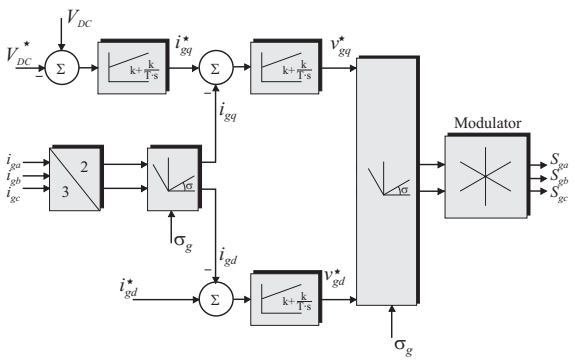


Figure 3.3: *Grid inverter reference voltage generation.*

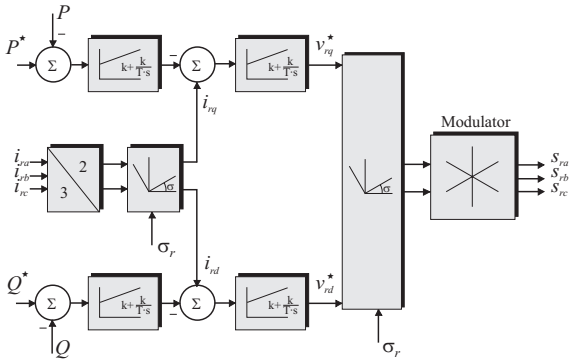


Figure 3.4: *Rotor inverter reference voltage generation.*

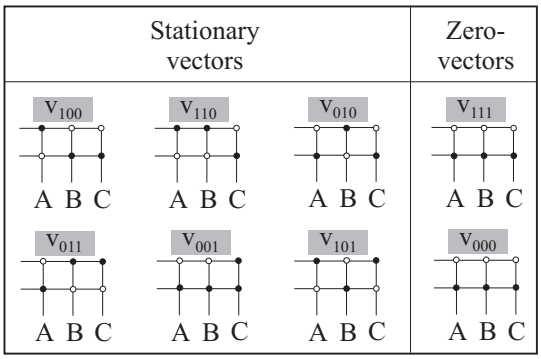


Figure 3.5: *The eight possible switch states of the voltage source inverter.*

With reference to Fig. 3.3, input to the control of the grid side inverter is the DC-link voltage reference V_{DC}^*. The DC-link voltage reference is compared with the actual DC-link voltage V_{DC} and the voltage error is fed to a PI controller. The PI-controller outputs an active current reference i_{gq}^* i.e. a current reference in the synchronously rotating reference frame. This current is compared with the actual active current i_{gq} derived from the measured grid currents and the current error is fed to another PI-controller which outputs the active voltage reference v_{gq}^* - still in the synchronously rotating reference frame. Together with the reactive voltage reference v_{gd}^*, the voltages are then transformed back into the stationary reference frame and then fed into the space vector modulator. The transformation from stationary reference frame to rotating reference frame and vice versa is based on a reliable estimate of the grid angle σ_g. Different methods exists for estimating this angle but a further explanation is referred to [2, 10]. Similar considerations goes for the rotor side inverter control in Fig. 3.4 where input is the reference for active power P^* and reactive power Q^* of the turbine.

3.2.2 Voltage synthesizing

Since the two inverters of the back-to-back two-level converter are operated individually, the operating principles can be explained by inspection of only one of the inverters. The inverter has three output ports which can be clamped to either the upper DC-link bus or to the lower DC-link bus. By this, the output of the inverter can achieve eight different switch combinations, i.e. eight legal voltages at the output ports. Fig. 3.5 shows the possible switch combinations. By a proper control of the switch states, the voltage source inverter are able to synthesize the desired output voltage. The control of the switch states are known as modulation.

3.3 Modulation

Although the goal of the modulation is to synthesize a desired output voltage, several methods are applicable, ranging from simple sinusoidal carrier based modulation to sophisticated methods like random modulation [5]. In the present work only modulation

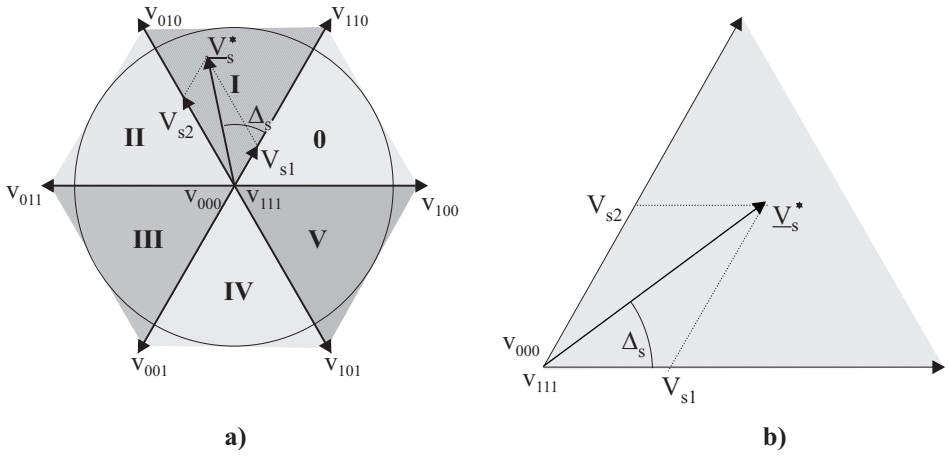


Figure 3.6: *The eight allowed switch combinations for the voltage source inverter and the corresponding space vectors.*

methods based on the space vector approach are described and only the most widely accepted modulation strategies are discussed.

3.3.1 Space vector approach

In the space vector modulation approach [22] the three time domain output voltage references $v_A^\star$, $v_B^\star$ and $v_C^\star$ are transformed into the complex valued space vector coordinate system by the following[3]:

$$\underline{V_s^\star} = \frac{2}{3}\left(v_A^\star + v_B^\star e^{j\frac{2\pi}{3}} + v_C^\star e^{j\frac{4\pi}{3}}\right) \tag{3.1}$$

By this, the three reference voltages become a vector with constant magnitude and rotating with constant angular velocity in the complex space-vector plane (provided that the reference voltages are symmetrical and their frequencies are constant).

Using eq. (3.1) on the possible switch-states of the voltage source inverter, c.f. Fig. 3.5 on the facing page, it appears that all the switch combinations become stationary vectors with amplitudes equal to $\frac{2}{3}$ of the DC-link voltage. Fig. 3.6a shows the space vector representation of the output voltages of the voltage source inverter.
With reference to Fig. 3.6b, a given reference vector $\underline{V_s^\star}$ can be realized by applying the two adjacent stationary vectors and a zero-vector for an angle dependent time duration (duty-cycles). In order to establish expressions for the duty-cycles which are independent

[3]It should be noted that the voltage reference vector $\underline{V_s^\star}$, consisting of a real and an imaginary part, actually constitute the two inputs to the modulator box in Fig. 3.3 and Fig. 3.4 on page 49.

of, in which sector the voltage reference vector is located, the angle Δ_s is defined as:

$$\Delta_s = \mod\left(\left(\omega_s t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \tag{3.2}$$

where $\omega_s t = 0$ is defined as the positive zero crossing of the phase A reference voltage ($v_A^\star = \sqrt{2}V_A^* \cdot \sin(\omega_s t)$). By this the angle Δ_s is in the interval: $\Delta_s \in [0..\frac{\pi}{3}]$. For a given reference voltage vector $\underline{V_s^\star}$, the fractional on-times $\delta_{1..2}$ for the adjacent stationary vectors can be calculated as:

$$\begin{aligned} V_{s1} &= |\underline{V_s^\star}|\frac{\sin\left(\frac{\pi}{3} - \Delta_s\right)}{\cos\left(\frac{\pi}{6}\right)} = \delta_1 \cdot \frac{2}{3} \cdot V_{DC} \\ \Downarrow & \\ \delta_1 &= \frac{\sqrt{3}|\underline{V_s^\star}| \cdot \sin\left(\frac{\pi}{3} - \Delta_s\right)}{V_{DC}} \end{aligned} \tag{3.3}$$

$$\begin{aligned} V_{s2} &= |\underline{V_s^\star}|\frac{\sin\left(\Delta_s\right)}{\cos\left(\frac{\pi}{6}\right)} = \delta_2 \cdot \frac{2}{3} \cdot V_{DC} \\ \Downarrow & \\ \delta_2 &= \frac{\sqrt{3}|\underline{V_s^\star}| \cdot \sin\left(\Delta_s\right)}{V_{DC}} \end{aligned} \tag{3.4}$$

where V_{DC} is the DC-link voltage. Having the fractional on-time duration for the two adjacent stationary vectors, the remaining part of the switching period are to be completed by use of the zero-vectors v_{000} or/and v_{111}. The fractional on-time for the zero-vector is given by:

$$\delta_0 = 1 - (\delta_1 + \delta_2) \tag{3.5}$$

Although, eq. (3.3) and eq. (3.4) gives the fractional on-times for the two stationary vectors adjacent to the reference vector, it should be noted that these modulation functions are limited by the following constraint :

$$\delta_{0..2} >= 0 \tag{3.6}$$

To comply with this constraint, it appears that the maximum amplitude of the output phase voltage is restricted to $\frac{1}{\sqrt{3}}$ times the DC-link voltage (which also is the theoretical maximum voltage transfer ratio for the voltage source inverter [17] without entering overmodulation).

3.3.2 Modulation index

In this context, the modulation index will be defined as[4]:

$$M = \frac{|v_A^\star|}{|\hat{v_A}^\star|} \tag{3.7}$$

[4]In the technical literature some confusion exists regarding the definition of modulation index. In some publications the modulation index equals unity at the boundary where the sinusoidal carrier based modulation enters overmodulation. In the present definition of modulation index this boundary occurs at a modulation index of $\sqrt{3}/2$.

where $\hat{v}^\star$ denotes the phase A voltage reference at which the space vector modulation approach enters the over-modulation range. By this definition, the modulation index becomes unity at the over-modulation boundary. The boundary for overmodulation is shown as the circle on Fig. 3.6.

From the definition in eq. (3.7), the desired RMS inverter reference phase voltage $V_A^\star$ is related to the modulation index by:

$$V_A^\star = \frac{M}{\sqrt{6}} V_{DC} \tag{3.8}$$

3.3.3 Vector sequences

Although eq. (3.3) and eq. (3.4) determines the fractional on-times per switching period for the two adjacent vectors, the realization of a given reference vector can be performed in an arbitrary number of ways and the only requirement is that the volt-second balance of the active vectors are satisfied within each switching period. However, in practice only about eight different methods have gained a wide acceptance [16]. In this thesis, only modulation methods based on the space vector approach will be treated. Actually, those to be treated are[5]:

- Suboptimal modulation (subopt)[6] [18] also known as SVPWM
- Symmetrical flat-top modulation (sft)[6] [11] also known as DPWM1.
- Asymmetrical shifted left flat-top modulation (aslft)[6] [28] also known as DPWM0.
- Asymmetrical shifted right flat-top modulation (asrft)[6] [28] also known as DPWM2.

Before entering into a description of each modulation strategy, some general remarks on the four strategies are to be added.

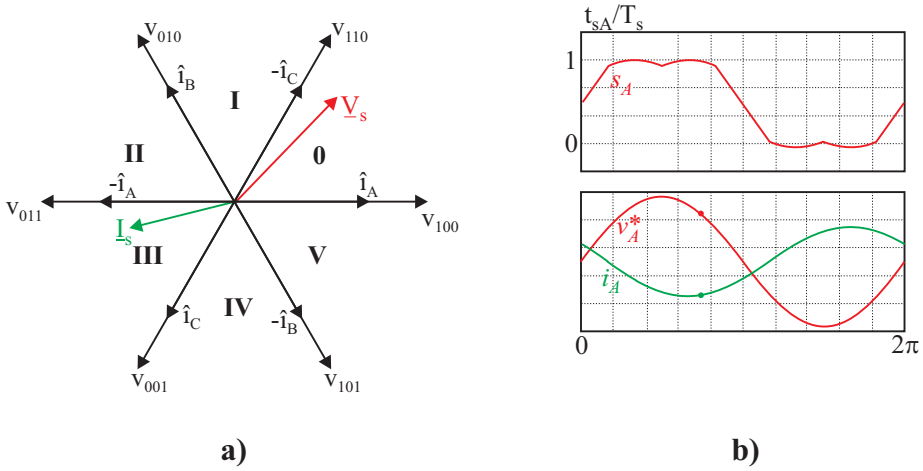
All the considered modulation strategies have switching sequences which are distributed symmetrical around the center of the switching period, and the shift between any two switch-states within a switching period are only allowed to involve one branch switch over (BSO). Finally, to make it easier to discuss and distinguish between the different modulation methods, it is appropriate to define the two dummy variables δ_{low} and δ_{high}:

$$\delta_{low} = \frac{\delta_{000}}{\delta_{000} + \delta_{111}} \tag{3.9}$$

$$\delta_{high} = \frac{\delta_{111}}{\delta_{000} + \delta_{111}} \tag{3.10}$$

[5]The references cited behind each of the modulation method do not necessarily provide the most comprehensive and adequate description but according to the authors reference list, these papers should be acknowledged as the inventors of the respective modulation schemes.

[6]The abbreviations are used in the comparison of the modulation schemes.



a) b)

Figure 3.7: *Illustration of the suboptimal modulation.*

TABLE I: *Switching table for the suboptimal modulation of the B6-inverter.*

	$\frac{1}{4}\delta_0$	$\frac{1}{2}\delta_1$	$\frac{1}{2}\delta_2$	$\frac{1}{2}\delta_0$	$\frac{1}{2}\delta_2$	$\frac{1}{2}\delta_1$	$\frac{1}{4}\delta_0$
Sector 0	v_{000}	v_{100}	v_{110}	v_{111}	v_{110}	v_{100}	v_{000}
Sector I	v_{111}	v_{110}	v_{010}	v_{000}	v_{010}	v_{110}	v_{111}
Sector II	v_{000}	v_{010}	v_{011}	v_{111}	v_{011}	v_{010}	v_{000}
Sector III	v_{111}	v_{011}	v_{001}	v_{000}	v_{001}	v_{011}	v_{111}
Sector IV	v_{000}	v_{001}	v_{101}	v_{111}	v_{101}	v_{001}	v_{000}
Sector V	v_{111}	v_{101}	v_{100}	v_{000}	v_{100}	v_{101}	v_{111}

which expresses the utilization of the two zero vectors v_{000} and v_{111} (δ_{000} is the on-time ratio for zero-vector v_{000}, and δ_{111} for the zero-vector v_{111}).

The first modulation method (subopt) belongs in the category of continuous modulation schemes while the latter three modulation methods, all are special cases of the generalized discontinuous modulation [15]. These discontinuous modulation methods uses the redundancy of the two zero vectors v_{000} and v_{111} to reduce the number of switchings per switching period. Actually this redundancy can be used to prevent switchings in the inverter phase leg carrying the instantaneously highest current. This can be complied as long as the angle ϕ between inverter phase voltage and phase current is in the in interval $\phi \in [-\frac{\pi}{3}..\frac{\pi}{3}; \frac{2\pi}{3}..\frac{4\pi}{3}]$). In the following, a brief description of each modulation method is given, followed by a comparison and an evaluation of the methods.

Suboptimal modulation (subopt)

In the suboptimal modulation, also called the space-vector PWM (SVPWM), because this modulation technique was the first in which the space vector theory was used to calculate the on-times [9], the two zero-vectors v_{000} and v_{111} are equally used within a switching period, i.e. $\delta_{low} = \delta_{high}$=0.5. Table I shows the switching sequences for the suboptimal modulation technique for each of the 6 sectors. The sector definition

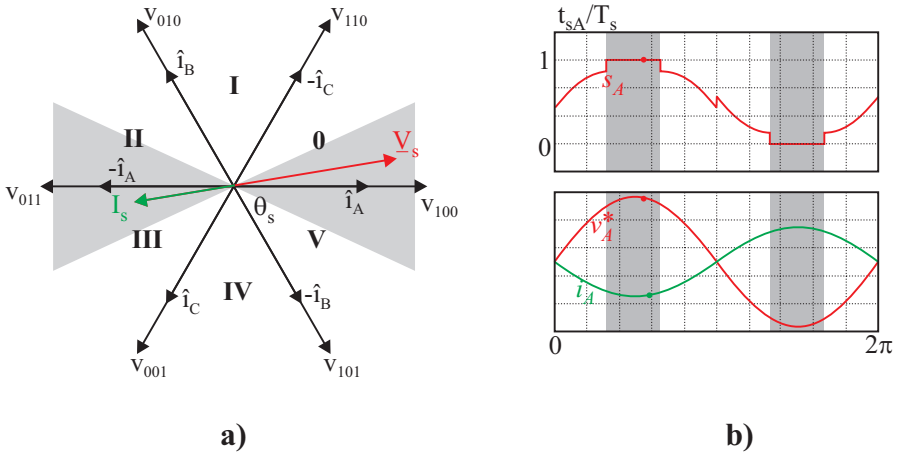


Figure 3.8: *Illustration of the symmetrical flat top modulation.*

TABLE II: *Switching table for the sft-modulation of the B6-inverter.*

		$\frac{1}{2}\delta_0$	$\frac{1}{2}\delta_1$	$\frac{1}{2}\delta_2$	δ_0	$\frac{1}{2}\delta_2$	$\frac{1}{2}\delta_1$	$\frac{1}{2}\delta_0$
Sector 0	$\Delta_s \leq \frac{\pi}{6}$	–	v_{100}	v_{110}	v_{111}	v_{110}	v_{100}	–
	$\Delta_s > \frac{\pi}{6}$	v_{000}	v_{100}	v_{110}	–	v_{110}	v_{100}	v_{000}
Sector I	$\Delta_s \leq \frac{\pi}{6}$	–	v_{110}	v_{010}	v_{000}	v_{010}	v_{110}	–
	$\Delta_s > \frac{\pi}{6}$	v_{111}	v_{110}	v_{010}	–	v_{010}	v_{110}	v_{111}
Sector II	$\Delta_s \leq \frac{\pi}{6}$	–	v_{010}	v_{011}	v_{111}	v_{011}	v_{010}	–
	$\Delta_s > \frac{\pi}{6}$	v_{000}	v_{010}	v_{011}	–	v_{011}	v_{010}	v_{000}
Sector III	$\Delta_s \leq \frac{\pi}{6}$	–	v_{011}	v_{001}	v_{000}	v_{001}	v_{011}	–
	$\Delta_s > \frac{\pi}{6}$	v_{111}	v_{011}	v_{001}	–	v_{001}	v_{011}	v_{111}
Sector IV	$\Delta_s \leq \frac{\pi}{6}$	–	v_{001}	v_{101}	v_{111}	v_{101}	v_{001}	–
	$\Delta_s > \frac{\pi}{6}$	v_{000}	v_{001}	v_{101}	–	v_{101}	v_{001}	v_{000}
Sector V	$\Delta_s \leq \frac{\pi}{6}$	–	v_{101}	v_{100}	v_{000}	v_{100}	v_{101}	–
	$\Delta_s > \frac{\pi}{6}$	v_{111}	v_{101}	v_{100}	–	v_{100}	v_{101}	v_{111}

refers to Fig. 3.7a. Fig. 3.7b shows the voltage reference v_A^* and the corresponding modulation function s_A for inverter branch A. The modulation function s_A is given by:

$$s_A = \frac{1}{2}\left(1 + \frac{2}{\sqrt{3}}\frac{v_A^*}{\hat{v}_A^*} + v_0\right) \quad \text{where } v_0 = \begin{cases} \frac{1}{2}\frac{v_A^*}{\hat{v}_A^*} & \text{if} \quad |v_C^*| > |v_A^*| < |v_B^*| \\ \frac{1}{2}\frac{v_B^*}{\hat{v}_B^*} & \text{if} \quad |v_A^*| > |v_B^*| < |v_C^*| \\ \frac{1}{2}\frac{v_C^*}{\hat{v}_C^*} & \text{if} \quad |v_B^*| > |v_C^*| < |v_A^*| \end{cases} \tag{3.11}$$

Symmetrical flat top modulation (Sft)

The discontinuous modulation scheme, known as symmetrical flat top modulation (sft-modulation) or DPWM1 [15, 16][7], is designed to minimize the switching losses whenever the phase current and phase voltage are in phase (or counter phase). This is obtained by letting δ_{low} equal zero for the first 30° of the even sectors and one for the last 30° of

[7] In this context the name *symmetrical flat top modulation* is preferred since this name closely relates to the shape of the modulation waveform, c.f. Fig. 3.8b

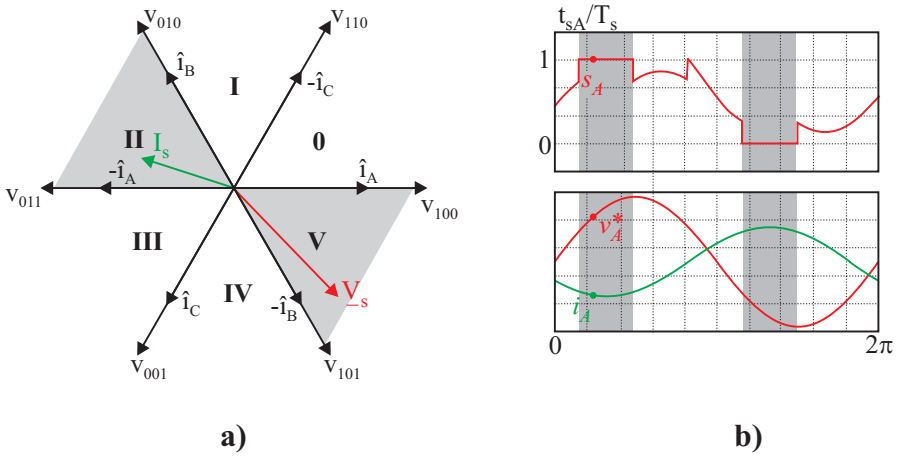


Figure 3.9: *Illustration of the asymmetrical shifted left flat top modulation.*

TABLE III: *Switching table for the asymmetrical shifted left flat top modulation.*

	$\frac{1}{2}\delta_2$	$\frac{1}{2}\delta_1$	δ_0	$\frac{1}{2}\delta_1$	$\frac{1}{2}\delta_2$
Sector 0	v_{110}	v_{100}	v_{000}	v_{100}	v_{110}
Sector I	v_{010}	v_{110}	v_{111}	v_{110}	v_{010}
Sector II	v_{011}	v_{010}	v_{000}	v_{010}	v_{011}
Sector III	v_{001}	v_{011}	v_{111}	v_{011}	v_{001}
Sector IV	v_{101}	v_{001}	v_{000}	v_{001}	v_{101}
Sector V	v_{100}	v_{101}	v_{111}	v_{101}	v_{100}

the even sectors. In the odd sectors, the order of δ_{low} and δ_{high} is reversed. Fig. 3.8a shows the voltage space vector hexagon for the voltage source inverter along with the hexagon for the phase current amplitudes. Fig. 3.8b shows the voltage reference v_A^* and the corresponding modulation function s_A for inverter branch A. The modulation function for the Sft-modulation is given by:

$$s_A = \frac{1}{2}\left(1+\frac{2}{\sqrt{3}}\frac{v_A^*}{\hat{v}_A^*}+v_0\right) \quad \text{where } v_0 = \begin{cases} \frac{|v_A^*|}{v_A^*} - \frac{v_A^*}{\hat{v}_A^*} & \text{if} \quad |v_C^*| < |v_A^*| > |v_B^*| \\ \frac{|v_B^*|}{v_B^*} - \frac{v_B^*}{\hat{v}_B^*} & \text{if} \quad |v_A^*| < |v_B^*| > |v_C^*| \\ \frac{|v_C^*|}{v_C^*} - \frac{v_C^*}{\hat{v}_C^*} & \text{if} \quad |v_B^*| < |v_C^*| > |v_A^*| \end{cases} \tag{3.12}$$

The shaded area of Fig. 3.8 illustrates the zone, where phase leg A is clamped to either the upper DC-branch or the lower DC-branch. For phase leg B and C, the clamping interval is rotated $\mp 60°$. Table II summarizes the sector dependent switching sequences of the sft-modulation. The angle Δ_s in Table II is the reference voltage angle in the actual sector, c.f. Fig. 3.6 and eq. (3.2).

Asymmetrical shifted left flat top modulation (Aslft)

The second discontinuous modulation scheme is the asymmetrical shifted left flat top modulation (aslft) also called DPWM0-modulation. As the name implies, the clamping

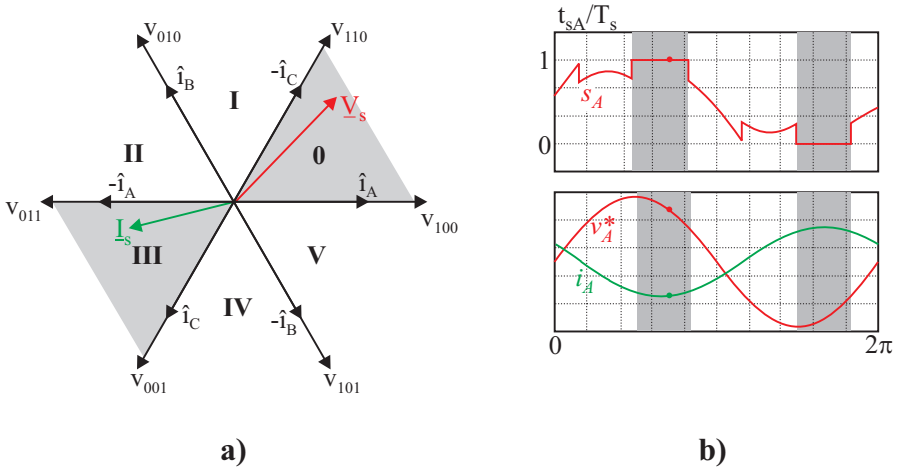


Figure 3.10: *Illustration of the asymmetrical shifted right flat top modulation.*

period for a phase leg is shifted to the left compared to the symmetrical flat top modulation. The shift is obtained by letting δ_{low} equal one in the even sectors and zero in the odd sectors. By this, the aslft-modulation is switching loss optimized for a 30° leading current. The aslft-modulation is illustrated in Fig. 3.9. The modulation function for the aslft-modulation is given by:

$$s_A = \frac{1}{2}\left(1+\frac{2}{\sqrt{3}}\frac{v_A^*}{\hat{v}_A^*}+v_0\right) \text{ where } v_0 = \begin{cases} \frac{|v_A^*|}{v_A^*} - \frac{v_A^*}{\hat{v}_A^*} & \text{if} \quad |v_{C0}^*| > |v_{A0}^*| < |v_{B0}^*| \\ \frac{|v_B^*|}{v_B^*} - \frac{v_B^*}{\hat{v}_B^*} & \text{if} \quad |v_{A0}^*| > |v_{B0}^*| < |v_{C0}^*| \\ \frac{|v_C^*|}{v_C^*} - \frac{v_C^*}{\hat{v}_C^*} & \text{if} \quad |v_{B0}^*| > |v_{C0}^*| < |v_{A0}^*| \end{cases} \quad (3.13)$$

where v_{A0}^*, v_{B0}^* and v_{C0}^* are phase shifted by -$\pi/6$ relative to v_A^*, v_B^* and v_C^* respectively. The sector dependent switching sequences are listed in Table III.

Asymmetrical shifted right flat top modulation (Asrft)

The last of the discontinuous modulation schemes - at least to be treated in this context - is the so-called asymmetrical shifted right flat top modulation (asrft) or DPWM2. According to Fig. 3.10 the asrft-modulation is obtained by letting δ_{low} equal zero in the even sectors and one in the odd sectors. By this, the asrft-modulation is switching-loss optimized for a 30° lagging current, c.f Fig. 3.10b. The modulation function for the asrft-modulation is given by:

$$s_A = \frac{1}{2}\left(1+\frac{2}{\sqrt{3}}\frac{v_A^*}{\hat{v}_A^*}+v_0\right) \text{ where } v_0 = \begin{cases} \frac{|v_A^*|}{v_A^*} - \frac{v_A^*}{\hat{v}_A^*} & \text{if} \quad |v_{C2}^*| > |v_{A2}^*| < |v_{B2}^*| \\ \frac{|v_B^*|}{v_B^*} - \frac{v_B^*}{\hat{v}_B^*} & \text{if} \quad |v_{A2}^*| > |v_{B2}^*| < |v_{C2}^*| \\ \frac{|v_C^*|}{v_C^*} - \frac{v_C^*}{\hat{v}_C^*} & \text{if} \quad |v_{B2}^*| > |v_{C2}^*| < |v_{A2}^*| \end{cases} \quad (3.14)$$

where v_{A2}^*, v_{B2}^* and v_{C2}^* are phase shifted by $\pi/6$ relative to v_A^*, v_B^* and v_C^* respectively. Table IV summarizes the sector dependent switching sequences for the asrft-modulation.

TABLE IV: *Switching table for the asymmetrical shifted right flat top modulation.*

	$\frac{1}{2}\delta_1$	$\frac{1}{2}\delta_2$	δ_0	$\frac{1}{2}\delta_2$	$\frac{1}{2}\delta_1$
Sector 0	v_{100}	v_{110}	v_{111}	v_{110}	v_{100}
Sector I	v_{110}	v_{010}	v_{000}	v_{010}	v_{110}
Sector II	v_{010}	v_{011}	v_{111}	v_{011}	v_{010}
Sector III	v_{011}	v_{001}	v_{000}	v_{001}	v_{011}
Sector IV	v_{001}	v_{101}	v_{111}	v_{101}	v_{001}
Sector V	v_{101}	v_{100}	v_{000}	v_{100}	v_{101}

3.3.4 Evaluation of the modulation methods

Although all the modulation methods described in the preceding section satisfy the volt-second balance and thereby complies the desired voltage reference, the modulation methods behaves differently when considering e.g. switching losses, conducting losses and harmonic content. To be able to compare and in a final stage select an appropriate modulation method for the voltage source inverters the modulation methods have to be evaluated on an equal basis. In this section the harmonic content for the different modulation methods are evaluated in order to be able to select a switching frequency which for a certain modulation method generate an acceptable harmonic content. The switching losses and conducting losses and their relation to the selected modulation method are discussed in section 3.4.

Harmonic performance

To evaluate the output voltage quality, the harmonic flux is considered [16, 21]. Presumed that the flux error equals zero in the beginning and at the end of each switching sequence, the N^{th} carrier cycle harmonic flux $\tilde{\psi}$ can be calculated by:

$$\tilde{\psi} = \int_{NT_s}^{(N+1)T_s} (\underline{V}_s - \underline{V}_s^{\star}) dt \tag{3.15}$$

where $\underline{V}_s$ is a stationary output vector. To be able to compare the modulators for the different converters, the per carrier harmonic flux error $\tilde{\psi}$ in eq. (3.15), is normalized to the product of the maximum voltage amplitude $|\underline{\hat{V}}_s|$ and the switching period. That is:

$$\tilde{\psi}_n = \frac{1}{T_s|\underline{\hat{V}}_s|} \cdot \tilde{\psi} \tag{3.16}$$

For the two-level voltage source inverter, the maximum voltage amplitude equals $V_{DC}/\sqrt{3}$. The normalized per-carrier cycle RMS value of the harmonic flux $\tilde{\psi}_{RMS,n}$ can be calculated by:

$$\langle \tilde{\psi}_{RMS,n} \rangle_{T_s} = \sqrt{\int_0^1 \left(\tilde{\psi}_n \cdot \tilde{\psi}_n^* \right) dt} \tag{3.17}$$

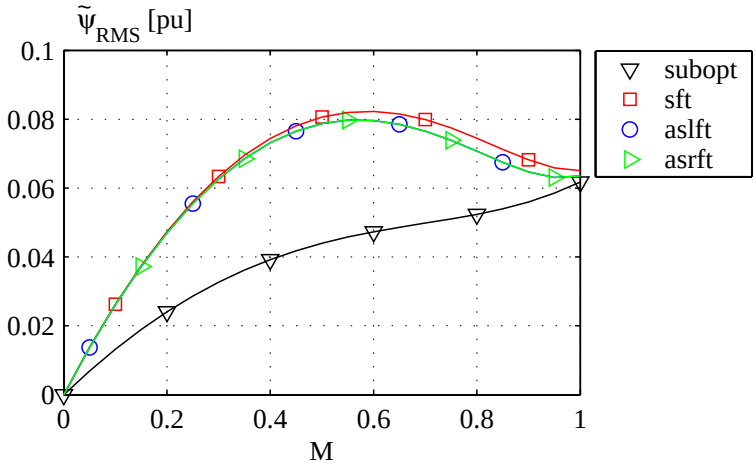


Figure 3.11: *The harmonic flux distortion of the different modulation methods, normalized according to eq. (3.16).*

where $\tilde{\psi}_n^*$ is the complex conjugate of $\tilde{\psi}_n$. Since the flux error characteristics have six fold symmetry per fundamental, the RMS harmonic flux value of the voltage source inverter can be calculated in the following:

$$\tilde{\psi}_{RMS,n} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left(\langle \tilde{\psi}_{RMS,n} \rangle_{T_s}\right)^2 d\Delta_s} \tag{3.18}$$

Fig. 3.11 shows the RMS-value of the harmonic flux as a function of the modulation index for the different modulation methods. For the nominal operation point, i.e. nominal modulation index M, Fig. 3.11 can be used to adjust the switching frequency of the different modulation methods in order to achieve a certain harmonic flux distortion. This issue is discussed in section 3.5.4 on page 81.

3.4 Loss evaluation

For the purpose of an RMS value model usable both to calculate the per-fundamental converter losses and the designing semiconductor temperatures, it is necessary to establish analytical expressions for the conduction losses and switching losses, taking into account both the modulation method, the modulation index M, and the load angle ϕ of the inverter. This section is aimed to derive these analytical expressions.

3.4.1 Conducting losses of the switches

In this context, the conducting losses of a semiconductor device, i.e transistor and diode, are simply modeled by [37]:

$$P_{t,cond} = V_{t0}(T) \cdot I_{t,avg} + R_t(T) \cdot I_t^2 \tag{3.19}$$

$$P_{d,cond} = V_{d0}(T) \cdot I_{d,avg} + R_d(T) \cdot I_d^2 \tag{3.20}$$

where $I_{x,avg}$ is the average current through the considered component, I_x is the RMS current through the considered component, $V_{x0}(T)$ is the temperature dependent threshold

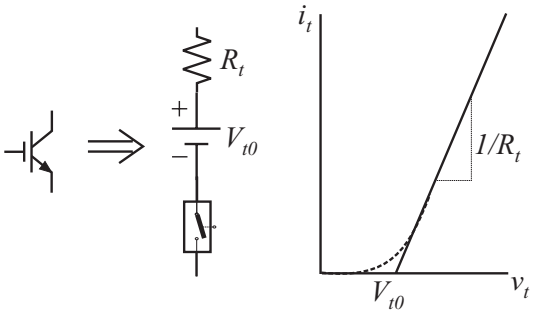


Figure 3.12: *Model of the transistor voltage drop.*

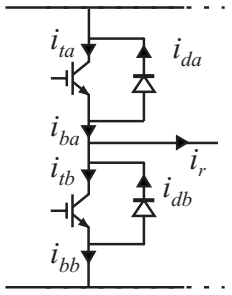


Figure 3.13: *Definition of* current direction.

voltage of the considered component and $R_{x0}(T)$ is the temperature dependent resistance of the considered component. The threshold voltage and on-resistance can either be found from data sheets or derived by the procedure described in Appendix A. Fig. 3.12 illustrates the applied modeling approach of the voltage drop across the semiconductor device (in the present case, the transistor voltage drop) along with an illustration of the actual voltage drop (shown by the dash line).

Unfortunately there is no simple relationship between the RMS output current I_r and the current in the diode I_d and transistor I_t. In fact, the current distribution between diode and IGBT is a function of both the modulation index M and the displacement angle ϕ between inverter phase voltage and current. Further, from the switching functions of the considered modulation methods illustrated in Fig. 3.7, 3.8, 3.9 and 3.10 it appears that the current distribution between diode and transistor even may differ from one modulation method to another. In [7], the inverter losses for two different modulation methods were evaluated but only the integral-form of the expression were derived while the results were evaluated numerically. For the purpose of a fast evaluation method a closed form expression of the current distribution is needed. To obtain a closed form expression of the current through the diode and transistor, an approach was given in [27, 6] and [38] which all to a certain extent evaluated the diode- and transistor current using sinusoidal modulation[8]. However, the expressions in these publications are only valid for sinusoidal modulation.

To derive a closed-form expression for the diode - and transistor current, the current definitions in Fig. 3.13 are used. From Fig. 3.13 the relation between diode current i_d and transistor current i_t at any time instant is given by:

$$i_{bx} = i_{tx} - i_{dx} \tag{3.21}$$

where the index x may be substituted by either a or b, c.f. Fig. 3.13. The average

[8]In the final stage the closed form expressions in [38] were obtained from curve fitting on simulated results and does not represent an exact solution. Fortunately this was an easy task for sinusoidal modulation due to a nearly linear relation between transistor RMS current and the product of inverter power factor and modulation index.

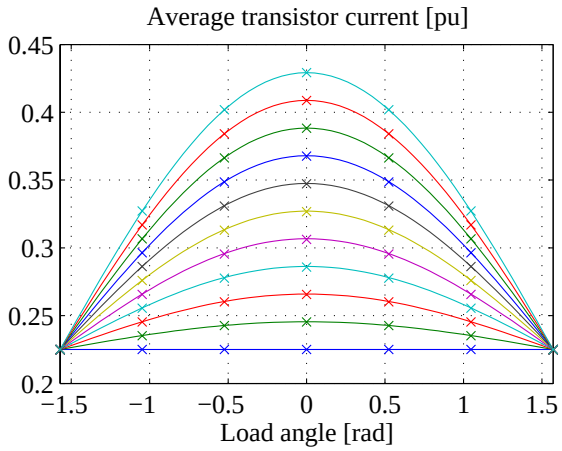


Figure 3.14: *Per unit average current through transistor as a function of the load angle. $M \in [0, 0.1 ...1]$.*

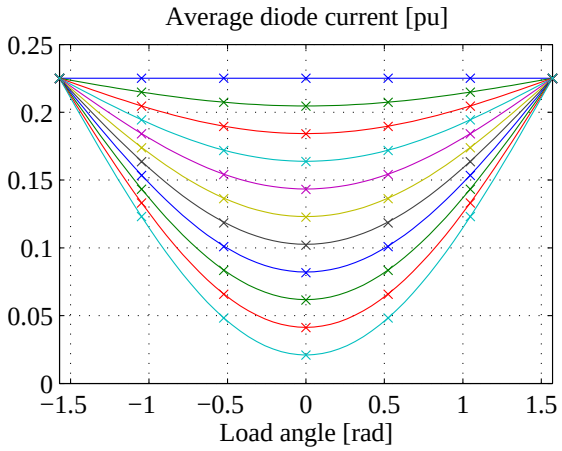


Figure 3.15: *Per unit average current through diode as a function of the load angle. $M \in [0, 0.1 ...1]$.*

current through the transistor and diode respectively can be evaluated by:

$$I_{t,avg} = \frac{1}{T_0}\int_{\phi}^{\pi+\phi}(s_A i_r)d\theta \tag{3.22}$$

$$I_{d,avg} = \frac{1}{T_0}\int_{\phi}^{\pi+\phi}((1-s_A) i_r)d\theta \tag{3.23}$$

where ϕ is the angle between phase current and reference phase voltage, θ is an integration variable and s_A is the modulation function given by either eq. (3.11), (3.12), (3.13) or (3.14). Using the expressions for the modulation functions, it can be shown that the average current through the transistor $I_{t,avg}$ and diode $I_{d,avg}$ is independent of the chosen modulation method and given by[9]:

$$I_{t,avg} = \left(\frac{\sqrt{2}}{2\pi} + \frac{\sqrt{6}}{12}M\cos(\phi)\right) I_r \tag{3.24}$$

$$I_{d,avg} = \left(\frac{\sqrt{2}}{2\pi} - \frac{\sqrt{6}}{12}M\cos(\phi)\right) I_r \tag{3.25}$$

where I_r is the RMS output phase current - assuming a pure sinusoidal current waveform. The expressions in eq. (3.24) and (3.25) are valid whenever the active power flow is out of the inverter. In case the power flows in the opposite direction, the expression for diode- and transistor average current has to be exchanged. Fig. 3.14 and Fig. 3.15 shows the average transistor current and diode current respectively. The average currents are plotted as a function of the load angle and shown for different values of the modulation index.

Using the definition of RMS current and the modulation functions in either eq. (3.11),

[9]Comparing the results obtained in [38] with the results in eq. (3.24) and eq. (3.25) it is important to note that the definition of modulation index is not identical and hence the constants do not comply.

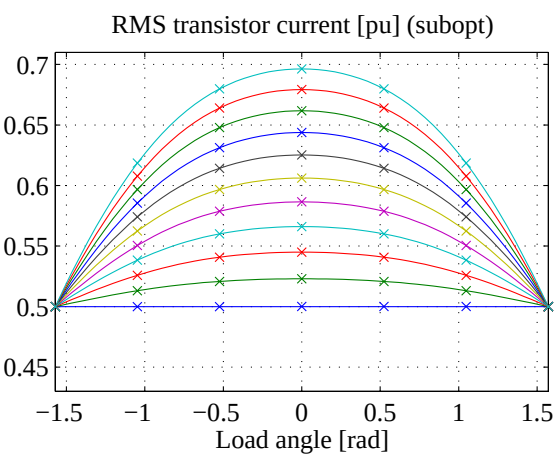


Figure 3.16: *Per unit RMS current through transistor as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

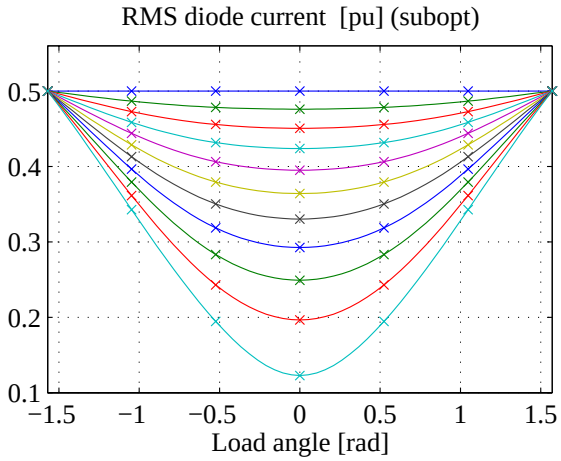


Figure 3.17: *Per unit RMS current through diode as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

(3.12), (3.13) or (3.14), the RMS current through the transistor and diode can similarly be evaluated by:

$$I_t = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\pi+\phi}(s_A i_r^2)d\theta} \tag{3.26}$$

$$I_d = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\pi+\phi}((1-s_A) i_r^2)d\theta} \tag{3.27}$$

where θ is used as an integration variable. Unfortunately, unlike the average current expression, the closed form expression for the RMS current is dependent on the chosen modulation method. In the following, the RMS current expressions are derived for the different modulation methods. It is important to note that the derived expressions are valid for power flowing out of the inverter while for power entering the inverter, the diode and transistor current expressions have to exchanged.

Suboptimal modulation

The closed form solution to eq. (3.26) and eq. (3.27) using the suboptimal modulation method, i.e. the modulation function given by eq. (3.11), is given by:

$$I_t = \begin{cases} \left(\frac{-M+3\pi-4M\cos(\phi)^2+8\sqrt{3}M\cos(\phi)}{12\pi}\right)^{\frac{1}{2}} I_r & |\phi| < \frac{\pi}{6} \\ \left(\frac{2M\left(2+\frac{\sqrt{3}}{2}\sin(|2\phi|)-\cos(\phi)^2-2\sin(|\phi|)+2\sqrt{3}\cos(\phi)\right)+3\pi}{12\pi}\right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < |\phi| < \frac{\pi}{2} \end{cases} \tag{3.28}$$

$$I_d = \begin{cases} \left(\frac{1}{2} - \frac{-M+3\pi-4M\cos(\phi)^2+8\sqrt{3}M\cos(\phi)}{12\pi}\right)^{\frac{1}{2}} I_r & |\phi| < \frac{\pi}{6} \\ \left(\frac{1}{2} - \frac{2M\left(2+\frac{\sqrt{3}}{2}\sin(|2\phi|)-\cos(\phi)^2-2\sin(|\phi|)+2\sqrt{3}\cos(\phi)\right)+3\pi}{12\pi}\right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < |\phi| < \frac{\pi}{2} \end{cases} \tag{3.29}$$

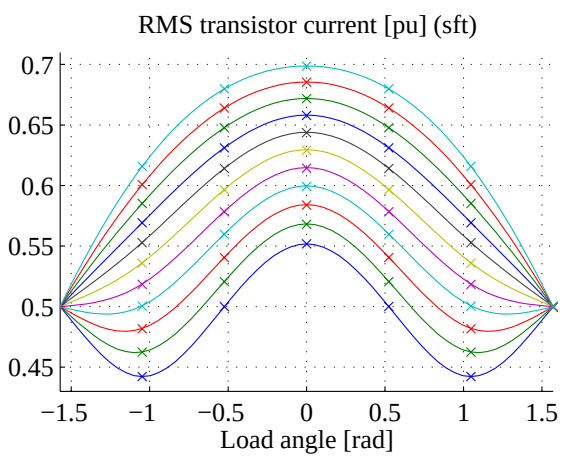


Figure 3.18: *Per unit RMS current through transistor as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

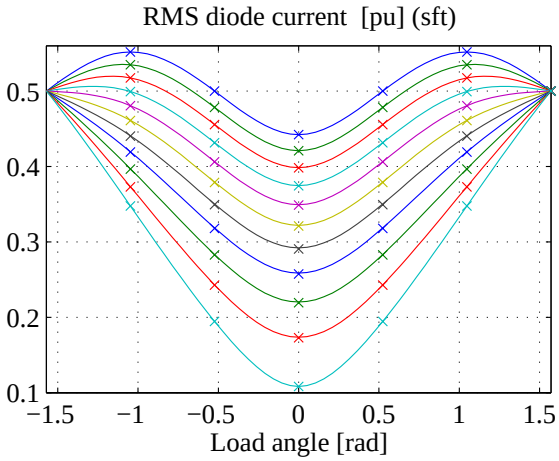


Figure 3.19: *Per unit RMS current through diode as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

The per unit transistor current and diode current when using suboptimal modulation is shown in Fig. 3.16 and 3.17 respectively. The per unit currents are shown as a function of the load angle and plotted for different values of the modulation index. To validate the derived expressions in eq. (3.28) and eq. (3.29) a simulation model was established. The simulated values are marked with an "x" and as shown the simulated and calculated values are identical.

Symmetrical flat top modulation

Using the symmetrical flat top modulation, given by eq. (3.12), the closed form expression for the RMS current through the transistor and diode becomes:

$$I_t = \begin{cases} \left(\frac{(6-8M)\sqrt{3}\cos(\phi)^2 + M\sqrt{3}(4+8\cos(\phi)) - 8M\sin(|\phi|)}{12\pi} + \right. & \\ \left. \frac{(4M-3)\sin(|2\phi|) - 3\sqrt{3} + 2\pi + 6|\phi|}{12\pi} \right)^{\frac{1}{2}} I_r & |\phi| < \frac{\pi}{3} \\ \left(\frac{(4M-3)\sin(|2\phi|) + 3\pi - 3|\phi|}{6\pi} \right)^{\frac{1}{2}} I_r & \frac{\pi}{3} < |\phi| < \frac{\pi}{2} \end{cases} \tag{3.30}$$

$$I_d = \begin{cases} \left(\frac{1}{2} - \frac{(6-8M)\sqrt{3}\cos(\phi)^2 + M\sqrt{3}(4+8\cos(\phi))}{12\pi} + \right. & \\ \left. \frac{-8M\sin(|\phi|) + (4M-3)\sin(|2\phi|) - 3\sqrt{3} + 2\pi + 6|\phi|}{12\pi} \right)^{\frac{1}{2}} I_r & |\phi| < \frac{\pi}{3} \\ \left(\frac{1}{2} - \frac{(4M-3)\sin(|2\phi|) + 3\pi - 3|\phi|}{6\pi} \right)^{\frac{1}{2}} I_r & \frac{\pi}{3} < |\phi| < \frac{\pi}{2} \end{cases} \tag{3.31}$$

The calculated and simulated per unit RMS currents are shown in Fig. 3.18 and Fig. 3.19. The currents are calculated as a function of the load angle ϕ and shown for different values of the modulation index M.

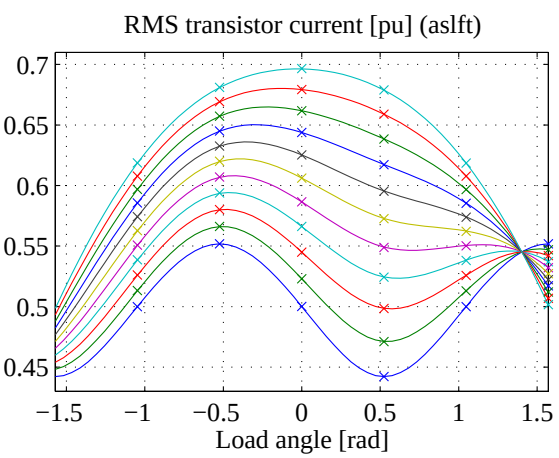


Figure 3.20: *Per unit RMS current through transistor as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

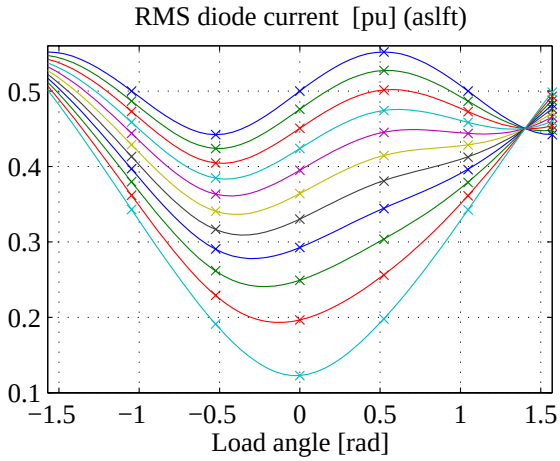


Figure 3.21: *Per unit RMS current through diode as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

Asymmetrical shifted left flat top modulation

Using the asymmetrical shifted left flat top modulation described by the modulation function in eq. (3.13), the closed form expression for the RMS diode- and transistor current can be derived as:

$$I_t = \begin{cases} \left(\frac{(4\sqrt{3}M-6)\sin(2\phi)+8\sqrt{3}M\cos(\phi)}{12\pi} + \frac{-8M\sin(\phi)-M\left(1+4\cos(\phi)^2\right)+3\pi+6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi < \frac{\pi}{6} \\ \left(\frac{\left(3\sqrt{3}M-3\right)\sin(2\phi)-2M+\left(10M-6\sqrt{3}\right)\cos(\phi)^2+3\sqrt{3}+5\pi-6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < \phi < \frac{\pi}{2} \\ \left(\frac{\left(6\sqrt{3}-14M\right)\cos(\phi)^2+\left(\sqrt{3}M-3\right)\sin(2\phi)}{12\pi} + \frac{M\left(10+8\sin(\phi)+8\sqrt{3}\cos(\phi)\right)+\pi-3\sqrt{3}-6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} < \phi < -\frac{\pi}{6} \end{cases} \quad (3.32)$$

$$I_d = \begin{cases} \left(\frac{1}{2} - \frac{(4\sqrt{3}M-6)\sin(2\phi)+8\sqrt{3}M\cos(\phi)}{12\pi} + \frac{-8M\sin(\phi)-M\left(1+4\cos(\phi)^2\right)+3\pi+6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi < \frac{\pi}{6} \\ \left(\frac{1}{2} - \frac{\left(3\sqrt{3}M-3\right)\sin(2\phi)-2M+\left(10M-6\sqrt{3}\right)\cos(\phi)^2+3\sqrt{3}+5\pi-6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < \phi < \frac{\pi}{2} \\ \left(\frac{1}{2} - \frac{\left(6\sqrt{3}-14M\right)\cos(\phi)^2+\left(\sqrt{3}M-3\right)\sin(2\phi)}{12\pi} + \frac{M\left(10+8\sin(\phi)+8\sqrt{3}\cos(\phi)\right)+\pi-3\sqrt{3}-6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} < \phi < -\frac{\pi}{6} \end{cases} \quad (3.33)$$

The calculated and simulated per unit RMS currents when using the asymmetrical shifted left flat top modulation are shown in Fig. 3.20 and Fig. 3.21. The currents are shown as a function of the load angle and plotted for different values of the modulation index.

Asymmetrical shifted right flat top modulation

Using the asymmetrical shifted right flat top modulation given by the switching function in eq. (3.14), the closed form expressions for the RMS transistor- and diode current can be derived as:

$$I_t = \begin{cases} \left(\frac{\left(6-4\sqrt{3}M\right)\sin(2\phi)-6\phi+3\pi}{12\pi} + \frac{M\left(8\sin(\phi)+8\sqrt{3}\cos(\phi)-4\cos(\phi)^2-1\right)}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi < \frac{\pi}{6} \\ \left(\frac{\left(3-\sqrt{3}M\right)\sin(2\phi)+\left(6\sqrt{3}-14M\right)\cos(\phi)^2}{12\pi} + \frac{M\left(8\sqrt{3}\cos(\phi)-8\sin(\phi)+10\right)-3\sqrt{(3)}+\pi+6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < \phi < \frac{\pi}{2} \\ \left(\frac{(10M-6\sqrt{3})\cos(\phi)^2-2M}{12\pi} + \frac{(3-3\sqrt{3}M)\sin(2\phi)+5\pi+3\sqrt{3}+6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} < \phi < -\frac{\pi}{6} \end{cases} \tag{3.34}$$

$$I_d = \begin{cases} \left(\frac{1}{2} - \frac{\left(6-4\sqrt{3}M\right)\sin(2\phi)-6\phi+3\pi}{12\pi} + \frac{M\left(8\sin(\phi)+8\sqrt{3}\cos(\phi)-4\cos(\phi)^2-1\right)}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi < \frac{\pi}{6} \\ \left(\frac{1}{2} - \frac{\left(3-\sqrt{3}M\right)\sin(2\phi)+\left(6\sqrt{3}-14M\right)\cos(\phi)^2}{12\pi} + \frac{M\left(8\sqrt{3}\cos(\phi)-8\sin(\phi)+10\right)-3\sqrt{(3)}+\pi+6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < \phi < \frac{\pi}{2} \\ \left(\frac{1}{2} - \frac{(10M-6\sqrt{3})\cos(\phi)^2-2M}{12\pi} + \frac{(3-3\sqrt{3}M)\sin(2\phi)+5\pi+3\sqrt{3}+6\phi}{12\pi} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} < \phi < -\frac{\pi}{6} \end{cases} \tag{3.35}$$

The calculated and simulated per unit RMS currents when using asymmetrical shifted right flat top modulation are shown in Fig. 3.22 and Fig. 3.23. The currents are calculated as a function of the load angle and shown for different values of the modulation index.

3.4.2 Switching losses

As in the case with the conducting losses, the switching losses of a two-level voltage source inverter also depend on the chosen modulation strategy [16]. Assuming the inverter component switching losses to be proportional to the switched voltage and

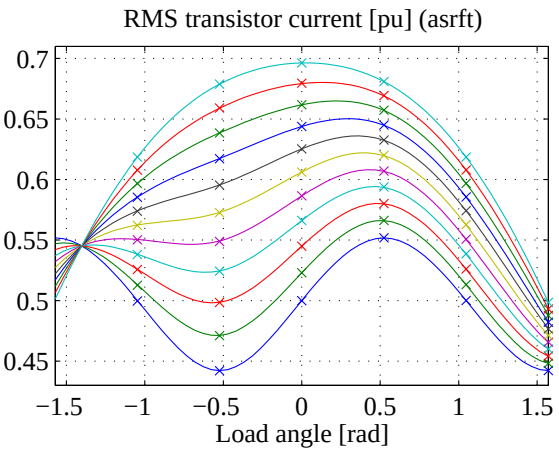


Figure 3.22: *Per unit RMS current through transistor as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

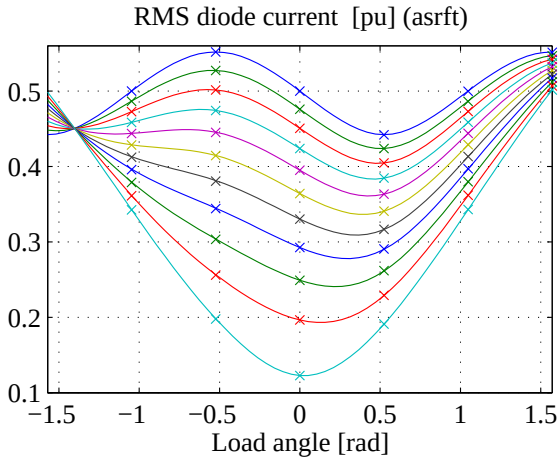


Figure 3.23: *Per unit RMS current through diode as a function of the load angle. $M \in [0, 0.1 \ldots 1]$.*

the switched current [26] and accounting only for the fundamental component of the load current, the switching losses can be analytically modeled for any given modulation strategy. The transistor and diode inverter switching losses per fundamental can be evaluated by:

$$P_{t,sw} = V_{DC} \cdot E_{sw0,t}(T) \cdot f_{sw} \cdot I_{sw,avg} \tag{3.36}$$

$$P_{d,sw} = V_{DC} \cdot E_{sw0,d}(T) \cdot f_{sw} \cdot I_{sw,avg} \tag{3.37}$$

where $E_{t,sw0}$ is the sum of the per unit VA transistor turn on and turn off switching energy, $E_{d,sw0}$ is sum of the per unit VA diode turn on and turn off switching energy, V_{DC} is the DC-link voltage, f_{sw} is the switching frequency and $I_{sw,avg}$ is the average switched device current. The per unit VA switching energies can either be found from data sheets or derived by the procedure described in Appendix A. The average switched device current is given by:

$$I_{sw,avg} = \frac{1}{4\pi} \int_0^{2\pi} \tilde{i}_{sw}(\theta) d\theta \tag{3.38}$$

where $\tilde{i}_{sw}(\theta)$ is the switching current function The switching current function equals zero in the intervals where modulation ceases (in case of discontinuous modulation) and the absolute value of the corresponding phase current value elsewhere. To obtain a closed form expression for the switching losses, the switching current function has to be evaluated for the different modulation methods.

Suboptimal modulation

In the suboptimal modulation scheme, the switchings of each device are equally distributed within the fundamental period and hence the switching losses are independent of the load angle ϕ between current and inverter voltage. Evaluation of the switching

current function for the suboptimal modulation gives:

$$\begin{aligned} I_{sw,avg} &= \frac{1}{4\pi}\int_0^{2\pi} \tilde{i}_{sw}(\theta)d\theta \\ &= \frac{\sqrt{2}}{\pi} I_r \end{aligned} \tag{3.39}$$

where I_r is the RMS output phase current of the inverter.

Symmetrical flat top modulation

Using a discontinuous modulation methods like the symmetrical flat top modulation it clearly appears from the modulation function illustrated in Fig. 3.8 on page 55 that the switching current function depends on the load angle ϕ, i.e angle between inverter reference voltage and phase current. For the symmetrical flat top modulation the closed form expression for the switching current function can be derived as:

$$\begin{aligned} I_{sw,avg} &= \frac{1}{4\pi}\int_0^{2\pi} \tilde{i}_{sw}(\theta)d\theta \\ &= \begin{cases} -\frac{\sqrt{2}(\cos(\phi)-2)}{2\pi} I_r & |\phi| < \frac{\pi}{3} \\ \frac{\sqrt{(6)}\sin(|\phi|)}{2\pi} I_r & \frac{\pi}{3} < |\phi| < \frac{2\pi}{3} \\ \frac{\sqrt{2}(\cos(\phi)+2)}{2\pi} I_r & \frac{2\pi}{3} < |\phi| < \pi \end{cases} \end{aligned} \tag{3.40}$$

Asymmetrical shifted left flat top modulation

The closed form expression for the switching current function when using the asymmetrical shifted left flat top modulation can be derived as:

$$\begin{aligned} I_{sw,avg} &= \frac{1}{4\pi}\int_0^{2\pi} \tilde{i}_{sw}(\theta)d\theta \\ &= \begin{cases} -\frac{\sqrt{2}\left(\cos(\phi-\frac{\pi}{6})-2\right)}{2\pi} I_r & |\phi-\frac{\pi}{6}| < \frac{\pi}{3} \\ \frac{\sqrt{(6)}\sin(|\phi-\frac{\pi}{6}|)}{2\pi} I_r & \frac{\pi}{3} < |\phi-\frac{\pi}{6}| < \frac{2\pi}{3} \\ \frac{\sqrt{2}\left(\cos(\phi-\frac{\pi}{6})+2\right)}{2\pi} I_r & \frac{2\pi}{3} < |\phi-\frac{\pi}{6}| < \pi \end{cases} \end{aligned} \tag{3.41}$$

Asymmetrical shifted right flat top modulation

Finally, the closed form expression for the switching current function when using the asymmetrical shifted right flat top modulation can be derived as:

$$\begin{aligned} I_{sw,avg} &= \frac{1}{4\pi}\int_0^{2\pi} \tilde{i}_{sw}(\theta)d\theta \\ &= \begin{cases} -\frac{\sqrt{2}\left(\cos(\phi+\frac{\pi}{6})-2\right)}{2\pi} I_r & |\phi+\frac{\pi}{6}| < \frac{\pi}{3} \\ \frac{\sqrt{(6)}\sin(|\phi+\frac{\pi}{6}|)}{2\pi} I_r & \frac{\pi}{3} < |\phi+\frac{\pi}{6}| < \frac{2\pi}{3} \\ \frac{\sqrt{2}\left(\cos(\phi+\frac{\pi}{6})+2\right)}{2\pi} I_r & \frac{2\pi}{3} < |\phi+\frac{\pi}{6}| < \pi \end{cases} \end{aligned} \tag{3.42}$$

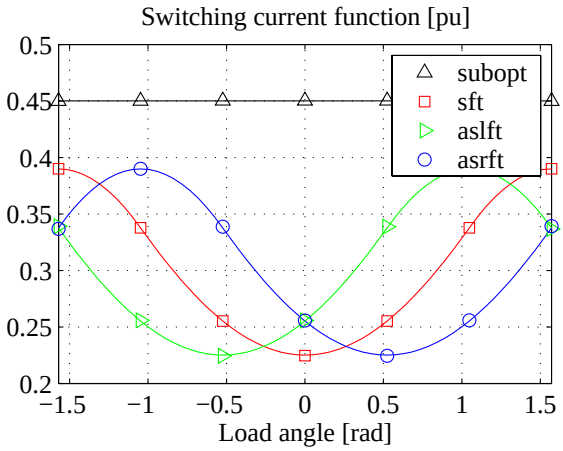


Figure 3.24: *The switching current function (normalized to the RMS output current) for the different modulation methods.*

The switching current functions for the different modulation methods are shown in Fig. 3.24.

3.4.3 Thermal modeling

The thermal modeling of the switches has two purposes:

1. To calculate the per fundamental average temperature in order to derive the correct values for resistances and on-state voltage drops under the actual temperature conditions[10].

2. To calculate the peak temperature within a fundamental period in order to validate a certain converter design[11].

Fig. 3.25a illustrates a simple one dimensional approach to calculate the junction temperature of the semiconductor components in a half bridge module [26], where the index notation of the power losses, e.g. P_{ta}, follows the notation in Fig 3.13 on page 60. Each of the semiconductor power losses are modeled as a current source feeding into a thermal impedance denoted by Z_{thxx}. As illustrated in Fig. 3.25b, the thermal impedances can be composed of one or more series connected RC-elements. The temperature source $k \cdot T_{xx}$ illustrates a thermal coupling between a transistor and a diode having current conduction in the same half period of a fundamental and finally the temperature source T_{amb} makes it possible to offset the temperature estimation by the ambient temperature. Based on the thermal modeling approach in Fig. 3.25 the goal is to derive a method which enables estimation of the average and peak junction temperatures, only

[10] Assuming the resistances and on-state voltage drops to be linear dependent on the component temperature, this approach will generate the correct per fundamental power losses.

[11] Especially in the doubly-fed system, this seems to be a very important issue due to the low fundamental frequency of the rotor inverter. Due to the low frequency, very high temperature variations within a fundamental period can be expected.

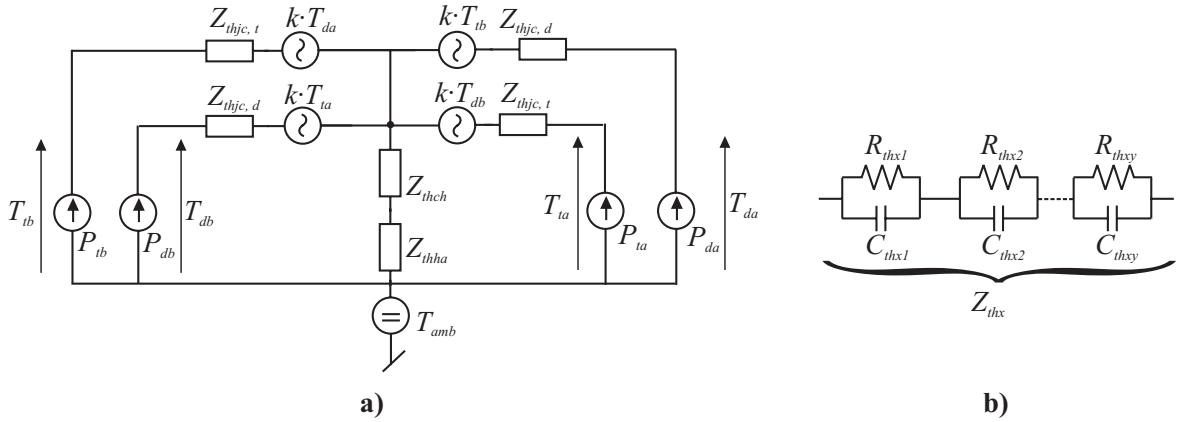


Figure 3.25: *Illustration of the simple thermal models used to estimate switch temperatures.* **a)** *Thermal model of a half bridge module.* **b)** *Model of a thermal impedance Z_{th}.*

with information on the modulation method dependent semiconductor losses calculated in section 3.4 and the thermal parameters in Fig. 3.25.

Average temperatures

Neglecting the thermal coupling between the components in the half bridge module, the average temperature of the individual components can simply be calculated by:

$$T_{tx} = P_{tx} \cdot \sum_{w=1}^{y} R_{thxw,t} + 2 \cdot (P_{tx} + P_{dx}) \cdot (R_{thch} + R_{thha}) + T_{amb} \tag{3.43}$$

$$T_{dx} = P_{dx} \cdot \sum_{w=1}^{y} R_{thxw,d} + 2 \cdot (P_{tx} + P_{dx}) \cdot (R_{thch} + R_{thha}) + T_{amb} \tag{3.44}$$

where T_{tx} is the average transistor temperature, T_{dx} is the average diode temperature and $R_{thxx,x}$ is the thermal resistances in the thermal model in Fig. 3.25b.

Peak temperatures

During operation at low frequencies ($f_s < 10$ Hz) the temporal variability of the power losses within a fundamental causes similar junction temperature variations. To estimate these temperature variations with a high accuracy, detailed knowledge of thermal structure of the semiconductor component is needed as well as an accurate prediction of the semiconductor losses as a function of time is required.

The thermal modeling of the semiconductor device may be accomplished by FEM analysis [34] or by three-dimensional electrical circuit equivalents while the semiconductor losses may be derived from a time consuming numerical simulation. However, none of these approaches are suitable for the purpose of the present approach since: 1) the necessary thermal data are generally not available and 2) the mentioned approaches are

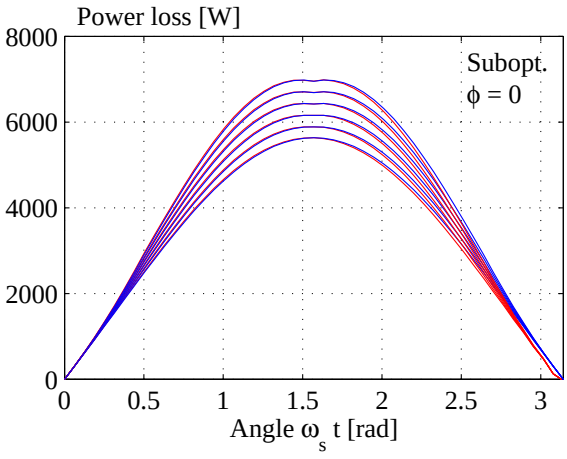


Figure 3.26: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using suboptimal modulation.*

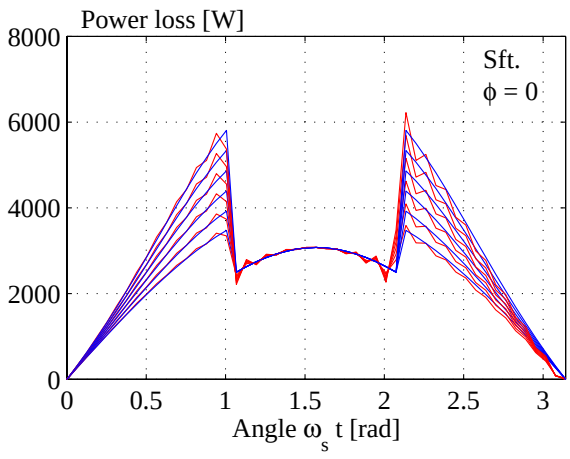


Figure 3.27: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using symmetrical flat top modulation.*

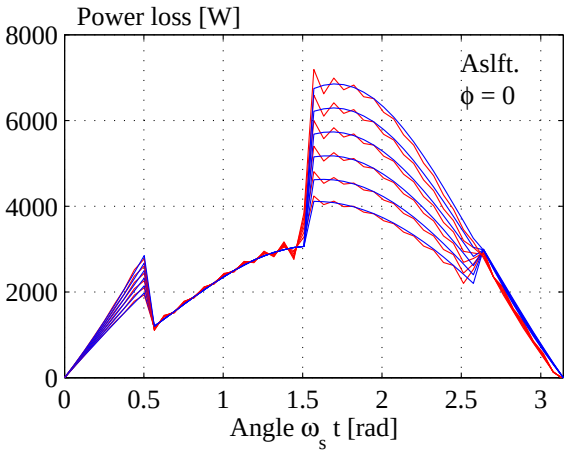


Figure 3.28: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using asymmetrical shifted left flat top modulation.*

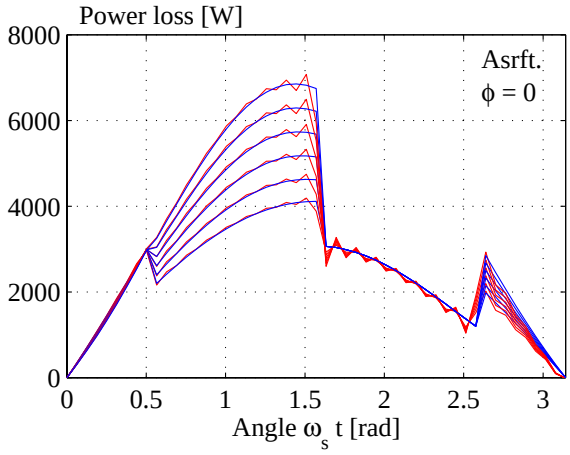


Figure 3.29: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using asymmetrical shifted right flat top modulation.*

very time consuming which is against the intention of the present work. The approach considered in this context is based on the one-dimensional thermal model illustrated in Fig 3.25, and the approach is to model the losses as sinusoidal functions with a DC-offset representing the average losses. By this approach, the thermal problem is reduced from a complex numerical iteration task to simple scalar expressions. By the present approach, the transistor losses $\tilde{p}_{tx}$ and diode losses $\tilde{p}_{dx}$ are estimated by:

$$\tilde{p}_{tx}(t) \quad = \quad P_{tx} + \sum_{n=1}^{\infty} \left(p_{t,an} \cdot \cos\left(n \cdot \omega_s \cdot t\right) + p_{t,bn} \cdot \sin\left(n \cdot \omega_s \cdot t\right) \right) \tag{3.45}$$

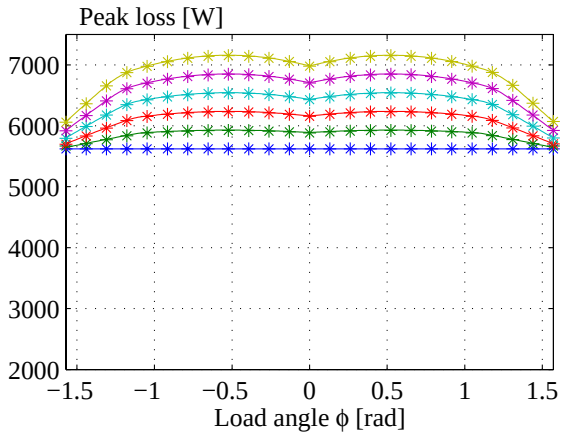


Figure 3.30: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using suboptimal modulation.*

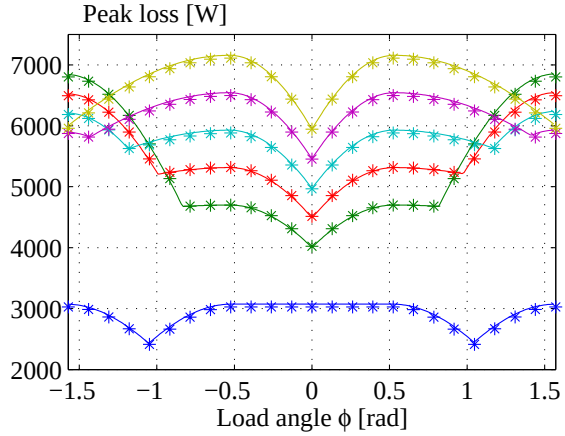


Figure 3.31: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using symmetrical flat top modulation.*

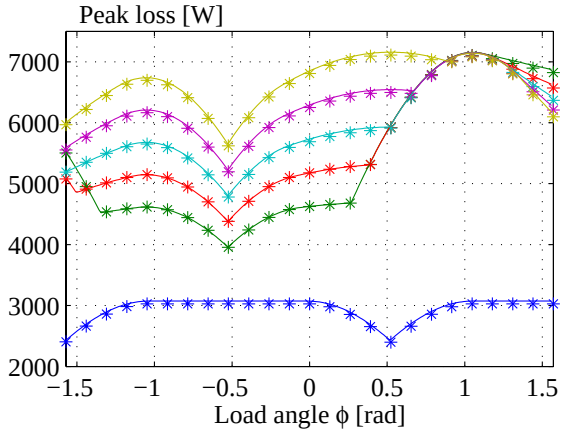


Figure 3.32: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using asymmetrical shifted left flat top modulation.*

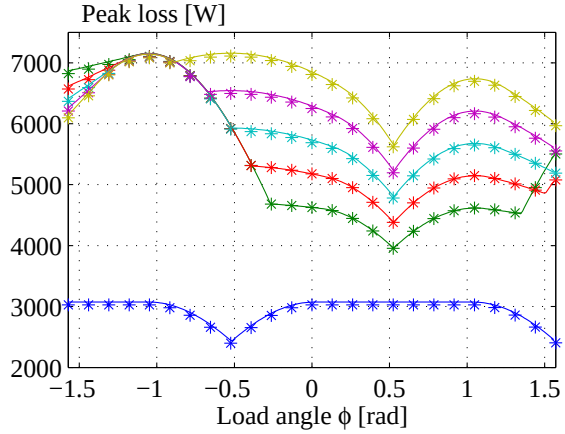


Figure 3.33: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using asymmetrical shifted right flat top modulation.*

$$\tilde{p}_{dx}(t) = P_{dx} + \sum_{n=1}^{\infty} \left(p_{d,an} \cdot \cos\left(n \cdot \omega_s \cdot t\right) + p_{d,bn} \cdot \sin\left(n \cdot \omega_s \cdot t\right) \right) \tag{3.46}$$

where the coefficients $p_{t,an}$, $p_{t,bn}$, $p_{d,an}$ and $p_{d,bn}$ are found from a Fourier analysis of the actual transistor losses and diode losses. The actual transistor and diode losses where derived in section 3.4 and are given by:

$$p_{tx}(t) = \left(V_{DC} \cdot E_{sw0,t}(T) \cdot f_{sw} \cdot \tilde{i}_{sw,t}(\theta) + V_{t0}(T) \cdot i_t(\theta) + R_t \cdot i_t^2(\theta) \right) \tag{3.47}$$

$$p_{dx}(t) = \left(V_{DC} \cdot E_{sw0,d}(T) \cdot f_{sw} \cdot \tilde{i}_{sw,d}(\theta) + V_{d0}(T) \cdot i_d(\theta) + R_d \cdot i_d^2(\theta) \right) \tag{3.48}$$

Fig. 3.26 - Fig. 3.29 illustrates the present approach when applied on the four

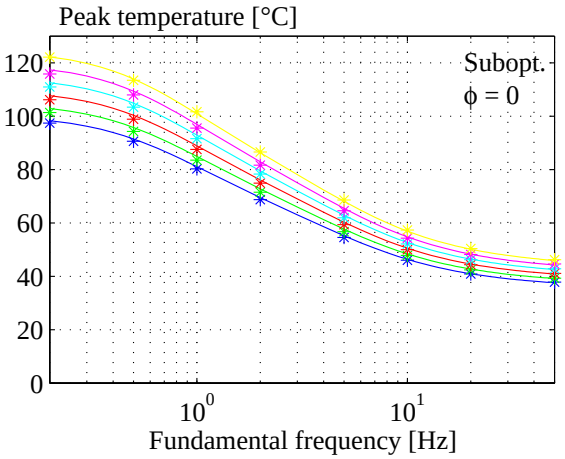


Figure 3.34: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using suboptimal modulation.*

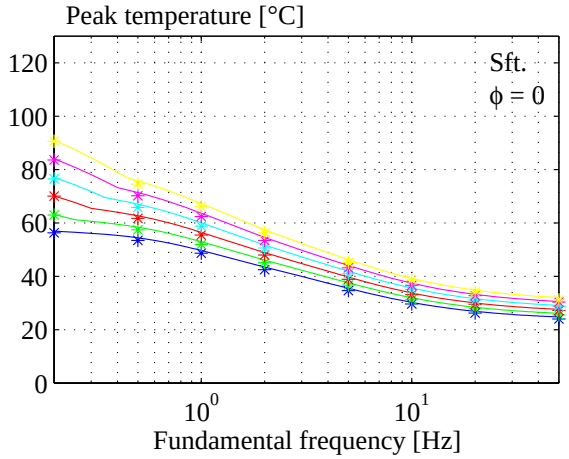


Figure 3.35: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using symmetrical flat top modulation.*

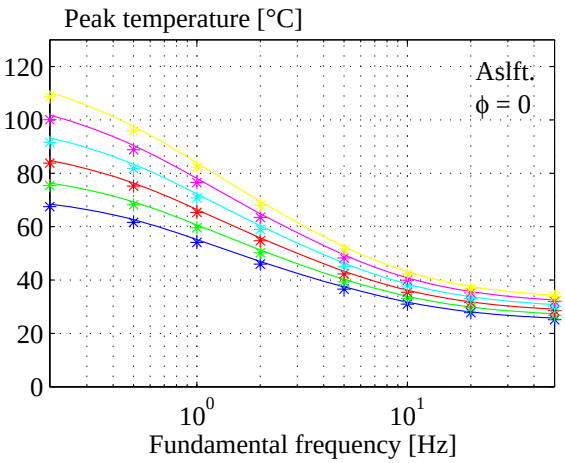


Figure 3.36: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using asymmetrical shifted left flat top modulation.*

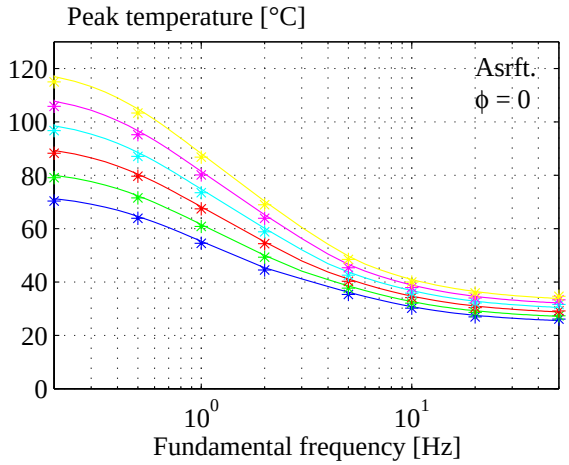


Figure 3.37: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using asymmetrical shifted right flat top modulation.*

considered modulation strategies. The blue curves show the real losses derived from a numerical simulation whereas the red curves show the losses calculated from eq. (3.45) - eq. (3.48) when the number of harmonics n is limited to 25. To further demonstrate the strength of the present approach, Fig. 3.30 - Fig. 3.33 shows the peak power losses in a transistor. The peak power losses are calculated as a function of the load angle ϕ and shown for different values of the modulation index. The power losses marked with (*) are simulated losses using the real loss distribution on a thermal model as shown

TABLE V: *Thermal parameters used in the example of Fig. 3.34 - Fig. 3.37.*

Symbol	Value	Unit	Symbol	Value	Unit
$R_{thjc1,t}$	3.4	[K/kW]	$C_{thjc1,t}$	107	[K/mWs]
$R_{thjc2,t}$	9.6	[K/kW]	$C_{thjc2,t}$	18.8	[K/Ws]
$R_{thjc3,t}$	7.0	[K/kW]	$C_{thjc3,t}$	5.7	[K/Ws]
$R_{thjc1,d}$	12.0	[K/kW]	$C_{thjc1,d}$	2.5	[K/mWs]
$R_{thjc2,d}$	12.0	[K/kW]	$C_{thjc2,d}$	417	[K/Ws]
$R_{thjc3,d}$	18.0	[K/kW]	$C_{thjc3,d}$	13.9	[K/Ws]
$R_{thjc4,d}$	20.0	[K/kW]	$C_{thjc4,d}$	2.00	[K/Ws]
R_{thca}	11	[K/kW]	C_{thca}	$--$	[K/Ws]

in Fig. 3.25 while temperatures calculated by the present approach are shown by solid lines. Assuming that the thermal capacitance of the case to ambient structure of the semiconductor module is sufficiently large to suppress temperature variations in the considered frequency range, the peak junction temperature of the transistor and diode can be estimated by:

$$\tilde{T}_{tx} = T_{tx} + \sum_{n=1}^{\infty} \left((p_{t,an} \cdot \cos(n \cdot \omega_s \cdot t) + p_{t,bn} \cdot \sin(n \cdot \omega_s \cdot t)) \sum_{w=1}^{y} Z_{thxw,t}(n \cdot \omega_s) \right) \quad (3.49)$$

$$\tilde{T}_{dx} = T_{dx} + \sum_{n=1}^{\infty} \left((p_{d,an} \cdot \cos(n \cdot \omega_s \cdot t) + p_{d,bn} \cdot \sin(n \cdot \omega_s \cdot t)) \sum_{w=1}^{y} Z_{thxw,d}(n \cdot \omega_s) \right) \quad (3.50)$$

where T_{tx} and T_{dx} are the average component temperature calculated by the expression given in eq. (3.43) and eq. (3.44). Fig. 3.34 - Fig. 3.37 demonstrate the present approach for calculating peak junction temperature. The junction temperatures are calculated as a function of the fundamental frequency and shown for different values of the modulation index. The temperatures marked with (*) are simulated temperatures using the real loss distribution on a thermal model as shown in Fig. 3.25 while temperatures calculated by the approach given in eq. (3.49) and eq. (3.50) are shown by solid lines.

The thermal parameters used to exemplify the peak temperature estimation approach are listed in Table V.

3.4.4 Inductor power losses

The inductor power losses P_L are composed of copper losses, hysteresis losses and eddy current losses. That is:

$$P_L = P_{cu} + P_{hy} + P_{ed} \quad (3.51)$$

Copper losses

The copper losses in the inductor are due to the effective resistance R_L of the windings.

$$P_{cu} = R_L I_L^2 \tag{3.52}$$

Where the effective resistance is a function of the inductor design, the inductor temperature and the frequency of the inductor current. For a given load current and a desired inductor value, Appendix B provides a detailed inductor design tool from which the effective resistance R_L of the inductor can be extracted.

Hysteresis losses

The empirical Steinmetz equation expresses the specific hysteresis loss as an exponential function of the frequency f and the maximum flux density $\hat{B}_c$. Provided that the magnetizing current is purely sinusoidal, the hysteresis loss can be expressed by:

$$P_{hy} = M_L \cdot c_m \cdot f^{\alpha} \cdot \hat{B}_c^{\beta} \tag{3.53}$$

where M_L is the weight of the core material c_m, α and β are material property constants. Despite, the formula in (3.53) is a well established expression for the hysteresis losses, manufactures of iron cores rather provide graphical presentation of the loss characteristic than providing the material property constants. Appendix B provides a detailed description on the extraction of the material property constants c_m, α and β as well as a design procedure for determining core material mass, given the nominal current and the desired inductance value. The design values for the current and inductance are discussed in section 3.5.

Eddy current losses

To account for the eddy current losses the empirical Steinmetz equation is used:

$$P_{ed} = M_L \cdot \frac{\sigma_c \cdot \tau}{12\rho_c} \left(\frac{dB}{dt}\right)^2 \tag{3.54}$$

where σ_c is the conductivity of the core material, τ is the thickness of the lamination and ρ_c is the mass density of the used core material. For a more detailed description on the modeling of the inductor power losses, see Appendix B.

3.5 Design aspects

Although the modeling approach described in the preceding sections in some sense has provided most of the equations for use in the converter design it may be difficult to extract the essential parts and for that reason it seems convenient to have some less complex design guidelines, at least for an initial design approach. This section is aimed to provide some rough design guidelines for the components in the back-to-back two-level

voltage source converter. Having this rough converter design, the loss- and temperature modeling approach described in this chapter can then be used to evaluate whether the designed converter does comply with the specified performance specification.

3.5.1 Design of switches

The aspects regarding the switch design describes some rough current rating estimations based on the ideal generator model discussed on page 37 and some rules of thumb regarding choice of switch for a given DC-link voltage. However regarding the latter aspect it is important to note that the voltage design margin very much depend on the specific power layout.

Current ratings

Neglecting the generator losses, the active power to be handled by the back-to-back converter is given by:

$$\tilde{P}_r = \frac{s(\omega_{gen} T_{gen})}{1+s} \tag{3.55}$$

where ω_{gen} is the angular velocity (in rad/s) of the generator shaft, T_{gen} is the torque applied on the generator shaft and s is the slip defined by[12]:

$$s = \frac{N_p \cdot \omega_{gen} - \omega_s}{\omega_s} \tag{3.56}$$

where N_p is the number of pole pairs in the generator and ω_s is the angular velocity of the grid voltage applied on the stator. Further, the reactive power to be handled by the rotor inverter $\tilde{Q}_r$ is given by:

$$\tilde{Q}_r = s \cdot \left(Q_s^* + \frac{3|\underline{V}_s|^2}{\omega_s L_m} \right) \tag{3.57}$$

where Q_s^* is the desired reactive power to be generated from the stator, $|\underline{V}_s|$ is the RMS stator phase voltage and L_m is the magnetizing inductance of the generator. The rotor current $\tilde{I}_r$, can then be roughly estimated by:

$$|\underline{\tilde{I}}_r| = \frac{1}{N_{gen}} \cdot \frac{\sqrt{\tilde{P}_r^2 + \tilde{Q}_r^2}}{3 \cdot s \cdot |\underline{V}_s|} \tag{3.58}$$

where N_{gen} is the winding ratio between rotor and stator. Neglecting the converter losses, the power to be handled by the grid side inverter equals the rotor power $\tilde{P}_r$. Hence the grid inverter current $\tilde{I}_g$ can the be estimated by:

$$|\underline{\tilde{I}}_{g3}| = \frac{\sqrt{\tilde{P}_r^2 + (Q_{g3}^*)^2}}{3 \cdot |\underline{V}_{g3}|} \tag{3.59}$$

[12]Please note that the definition of slip is positive for super synchronous speed - a definition contrary to the definition normally used in text books concerning electrical machinery.

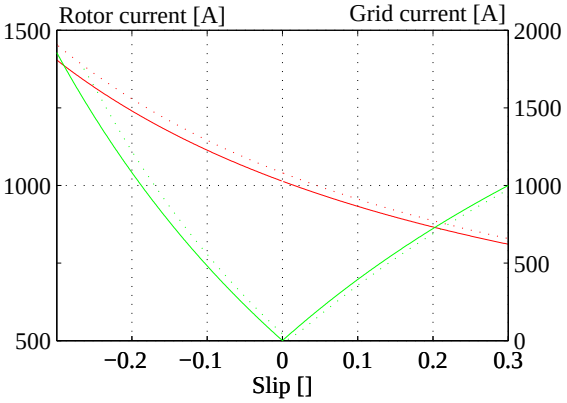


Figure 3.38: *Estimated (-) and actual (· · ·) current ratings for the grid side inverter (-) and the rotor side inverter (-).*

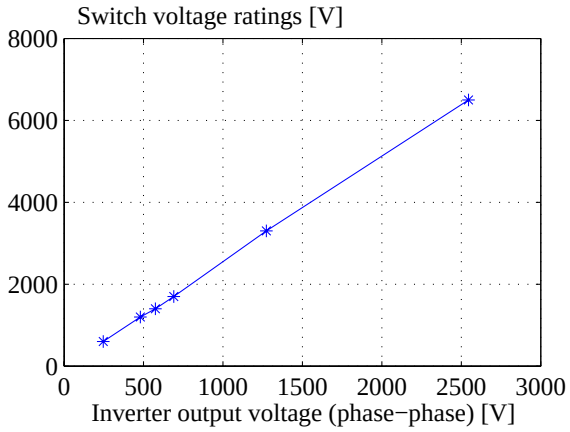


Figure 3.39: *Typical relation between DC-link voltage and switch voltage.*

where Q^*_{g3} is the reactive power generated to the grid by the grid side inverter. Fig. 3.38 demonstrate an example of these simple calculations of the rotor currents and grid currents compared with the actual values. As a final remark regarding the current ratings of the switches in the back-to-back converter it should be noted that since the converter has to handle a bi-directional power flow, the diodes and transistors have to be rated for almost the same current[13].

Voltage ratings

In order to be able to control the generated power in a certain slip range, the rotor side inverter has to be able to generate voltages higher than the voltage appearing on the rotor terminal of the generator. Assuming an ideal generator, the voltage at the rotor terminals of the generator can be approximated by:

$$|\tilde{\underline{V}}_r(s)| = s \cdot |\underline{V}_s| \cdot N_{gen} \tag{3.60}$$

Further to control the power flow to/from the grid, the grid side inverter has to be capable of generating voltages higher than the grid voltage. The necessary grid inverter phase voltage V_{gc} can be approximated by:

$$|\tilde{\underline{V}}_{gc}| = |\underline{V}_{g3} + j \cdot \omega_s \cdot L_g \cdot \tilde{\underline{I}}_g(\hat{s})| \tag{3.61}$$

where $|\underline{V}_{g3}|$ is the transformer phase voltage at the grid side of the inverter and $\tilde{\underline{I}}_g(\hat{s})$ is the grid current appearing at the maximum slip, c.f. Fig. 3.38. Hence the DC-link voltage of the back-to-back two-level voltage source converter has to obey the following

[13] In conventional drives and in wind turbines based on full-scale converters the power flow is normally uni-directional and hence the current shear between transistor and diodes is unequal, cf. section 3.4.

constrains:

$$V_{DC} > \hat{s} \cdot \sqrt{6}|\underline{V}_s| \cdot N_{gen} \tag{3.62}$$

$$\wedge$$

$$V_{DC} > \sqrt{6}|\underline{V}_{g3} + j \cdot \omega_s \cdot L_g \cdot \tilde{\underline{I}}_g(\hat{s})| \tag{3.63}$$

The grid side voltage $|\underline{V}_{g3}|$ should be the maximum appearing value for which the turbine is expected to be in normal operation, c.f. section 2.6.2.

The selection of a switch for a certain DC-link voltage has to incorporate some voltage margin to cope with the transient voltage spikes occurring at each switching instant due to stray inductances, both inside the switch and in the surrounding DC-link circuit. This voltage design margin especially has to include the overvoltages arising from the turn-off transients in case of short circuit failures. Fig. 3.39 shows typical relation between output inverter voltage (phase-phase) and voltage ratings of an applicable switch [25]. However it should be noted that the necessary voltage design margin is very dependent on the DC-link design and the switch turn-off behavior in case of a failure.

3.5.2 Design of boost inductance

In order to be able to design the boost inductance, the necessary inductance value and inductance current rating have to be found. Having the desired inductance and the current rating, the boost inductance can be designed according to the procedure described in Appendix B. Further, from the design procedure the loss parameters necessary for the loss calculations can be determined.

Inductance value

In dynamic operation, i.e. when the rotational speed varies up to the maximum specified slip $\hat{s}$, the grid inverter still has to be able to control the power to/from the DC-link. From eq. (3.63) it appears that the maximum inductance value depends on the DC-link voltage and the grid voltage. Rearranging eq. (3.63) the following constrain regarding the boost inductance is obtained:

$$L_g \leq \frac{-\hat{Q}^*_{g3} + \sqrt{9|\hat{\underline{V}}_{gc}|^2|\hat{\underline{I}}_{g3}|^2 - \hat{P}_r^2 - 2\hat{P}_r\hat{Q}^*_{g3}}}{\omega_g|\hat{\underline{I}}_{g3}|^2} \tag{3.64}$$

where $|\hat{\underline{V}}_{gc}|$ and $|\hat{\underline{I}}_{g3}|$ are the maximum necessary grid inverter voltage and current given by eq. (3.61) and eq. (3.59) respectively.

Current rating

The current ratings of the boost inductance has to be designed for the current given by eq. (3.59).

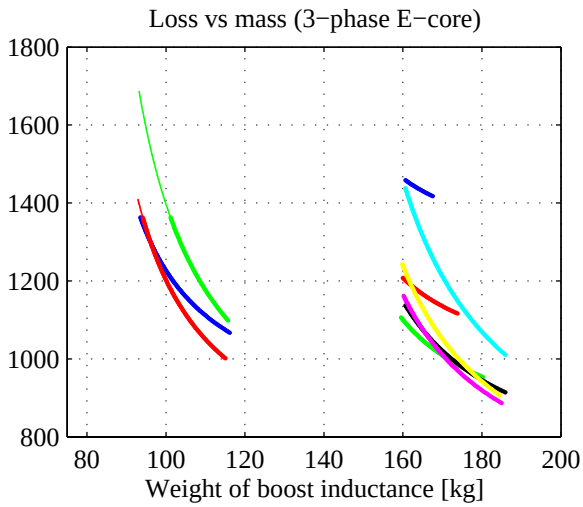


Figure 3.40: *Core designs. Losses vs. mass of the three-phase inductor plotted for current densities between 1.5 - 8 A/mm^2.*

By use of the iterative design procedure described in Appendix B, it is possible to design an inductor complying with the specifications. Fig. 3.40 shows an example of the outcome of the present design procedure.

Fig. 3.40 shows the calculated losses for 7 different inductances[14] (0.3mH to 0.6mH stepped by 50μH) as a function of the mass of the inductor. The calculations are repeated for different current densities (1.5 A/mm^2 to 8 A/mm^2). The bold lines corresponds to core designs where the temperature is kept below the maximum allowable temperature while thin lines corresponds to designs which do not comply with the temperature specifications.

3.5.3 Design of DC-link

Although the design of the DC-link is not a necessary task for the loss calculation approach, it is a general issue in the converter design. Especially, the presence of the two active inverters feeding harmonic currents into the DC-link capacitors make the DC-link design a little more complex than the DC-link design of conventional uni-directional drives. In general, the DC-link design include the following considerations [19]:

- Harmonic current ratings in steady-state operation.
- Peak-voltage suppression in case of a grid failure.
- Suppress the effect of a transient power mismatch between grid side inverter and rotor side inverter.

[14] In the present example, the product of the inductance and the switching frequency is kept constant at 2.0

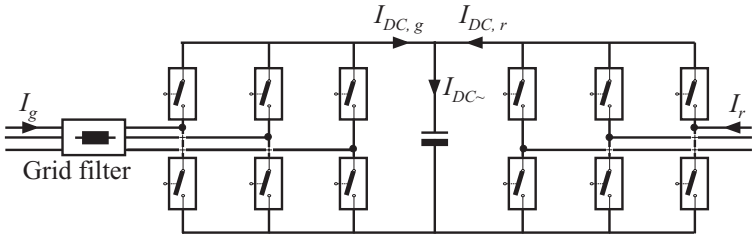


Figure 3.41: *Definition of the DC-link currents.*

In this context, only the design considerations regarding the steady state operation are discussed. In the harmonic current calculation, the current definitions in Fig. 3.41 are used.

Current contribution from the two-level rotor side inverter

The current fed from the rotor side to the DC-link $I_{DC,r}$ can be calculated from the switch states presented in section 3.3. Due to the six fold symmetry, it is sufficient to consider only the interval from 0 to $\frac{\pi}{3}$ [20]:

$$I_{DC,r} = \sqrt{\frac{6}{2\pi}\int_0^{\pi/3}(\delta_1 \cdot i_A^2 + \delta_2(-i_C)^2)d\Delta_s} \tag{3.65}$$

where the duty-cycle functions δ_1 and δ_2 is given by:

$$\begin{aligned} \delta_1 &= M_r \cdot \sin\left(\frac{\pi}{3} - \Delta_s\right) \\ \delta_2 &= M_r \cdot \sin\left(\Delta_s\right) \end{aligned} \tag{3.66}$$

and the phase currents are given by:

$$\begin{aligned} i_A &= \sqrt{2} \cdot I_r \cdot \cos(\Delta_s + \phi_r) \\ i_C &= \sqrt{2} \cdot I_r \cdot \cos\left(\Delta_s + \phi_r - \frac{4\pi}{3}\right) \end{aligned} \tag{3.67}$$

By insertion of eq. (3.66) and eq. (3.67) into eq. (3.65), the following closed form expression is obtained:

$$I_{DC,r} = I_r\sqrt{\frac{M_r}{\pi}(1 + 4\cos^2(\phi_r))} \tag{3.68}$$

Fig. 3.42 shows the RMS DC-link current from the rotor side inverter as a function of the load angle ϕ_r and the modulation index M_r. The DC-link current $I_{DC,r}$ calculated by eq. (3.68) can be considered as being composed of an average value $I_{DC,r=}$ and a ripple current $I_{DC,r\tilde{}}$ related by:

$$I_{DC,r} = \sqrt{I_{DC,r=}^2 + I_{DC,r\tilde{}}^2} \tag{3.69}$$

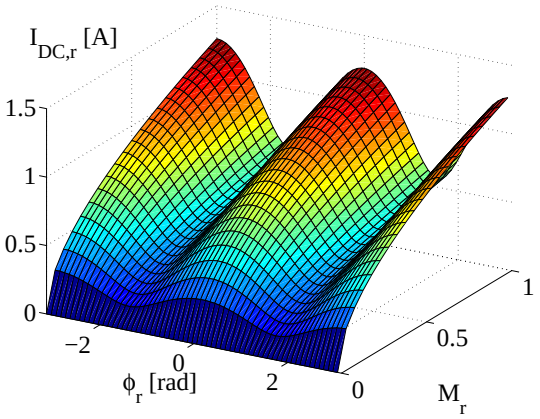


Figure 3.42: *The DC-link current $I_{DC,r}$ (RMS) due to the switching operation of the rotor inverter.*

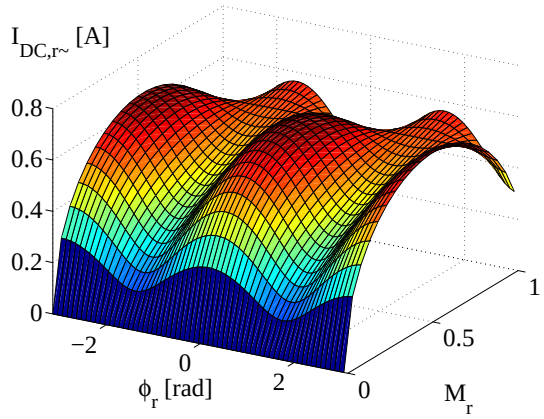


Figure 3.43: *The DC-link capacitor current $I_{DC,\tilde{r}}$ (RMS) due to the switching operation of the rotor inverter.*

The average current $I_{DC,r=}$ fed from the rotor circuit to the DC-link is by:

$$I_{DC,r=} = \frac{6}{2\pi} \int_0^{\frac{\pi}{3}} (\delta_1 \cdot i_A + \delta_2(-i_C)) d\Delta_s \tag{3.70}$$

On a closed for, the average current $I_{DC,r=}$ becomes:

$$I_{DC,r=} = \frac{\sqrt{6}}{2} M_r \cdot \cos(\phi_r) \cdot I_r \tag{3.71}$$

Since the current through the DC-link capacitors do not contain any DC-component, the current through the capacitors originating from the rotor side inverter can be derived as:

$$I_{DC,\tilde{r}} = \frac{1}{2} I_r \sqrt{\left(\frac{16}{\pi} - 6M_r\right) M_r \cdot \cos^2(\phi_r) + \frac{4}{\pi} M_r} \tag{3.72}$$

Fig. 3.43 shows the harmonic DC-link capacitor current originating from the rotor side inverter as a function of the load angle ϕ_r and the modulation index M_r.

Current contribution from the two-level grid side inverter

The current contribution from the grid side inverter is derived similar to the derivation of the current contribution from the rotor side inverter. The harmonic capacitor current originating from the grid side inverter is given by:

$$I_{DC,\tilde{g}} = \frac{1}{2} I_g \sqrt{\left(\frac{16}{\pi} - 6M_g\right) M_g \cdot \cos^2(\phi_g) + \frac{4}{\pi} M_g} \tag{3.73}$$

where ϕ_g is the angle between the grid inverter reference voltage and the grid current and M_g is the modulation index of the grid side inverter.

Current stresses on the DC-link capacitors

Although having the current contribution from both the grid side inverter and the rotor side inverter, the current stress on the DC-link is still quite complex to derive. Actually, in the general form, each harmonic component (h) of the grid- and rotor side inverter has to be added vectorially. That is [33, 32]:

$$\begin{aligned} I_{DC\tilde{}}^2 &= \sum_{h=1}^{\infty}(\underline{I}_{DC,\tilde{g}}(h) + \underline{I}_{DC,\tilde{r}}(h))^2 \\ &= \sum_{h=1}^{\infty}(I_{DC,\tilde{g}}^2(h) + I_{DC,\tilde{r}}^2(h) + 2 \cdot I_{DC,\tilde{g}}(h) \cdot I_{DC,\tilde{r}}(h)\cos(\theta_g(h) - \theta_r(h))) \end{aligned} \quad (3.74)$$

where $\theta_g(h)$ and $\theta_r(h)$ is the angle of the individual harmonic. The angle of the harmonics depend on the synchronization of the grid side modulator and rotor side modulator. Clearly, the expression of the DC-link harmonic current, involving the need for a harmonic analysis is of limited value in a rough DC-link design. However, with the assumption that the grid side inverter and rotor side inverter are operated at different switching frequencies and in addition, contains no common higher harmonics, the current stress on the DC-link capacitors can be approximated by:

$$I_{DC\tilde{}} = \sqrt{I_{DC,\tilde{g}}^2 + I_{DC,\tilde{r}}^2} \quad (3.75)$$

From eq. (3.74) it appears that selecting the switching frequencies of the grid side inverter and rotor side inverter with an integer multipla in difference and further synchronizing the modulators the DC-link capacitor current may be reduced from the values obtained by the expression in eq. (3.75). Fig. 3.44 shows an example of the DC-link capacitor current as a function of the wind speed for a typical wind turbine application when using eq. (3.75).

3.5.4 Modulation strategy and switching frequency

From the evaluation of harmonic flux distortion discussed in section 3.3.4 it appears that in order to obtain the same harmonic performance in a nominal working condition, i.e. for a nominal modulation index, the switching frequency should be selected according to both the chosen modulation method and the nominal modulation index. For this purpose it is convenient to establish an expression for a switching frequency correction factor $k_{sw,v}$. Hence, using the suboptimal modulation method as basis, the switching frequency correction factor expresses the factor by which the switching frequency has to be increased for any other modulation method in order to obtain the same harmonic performance as for the suboptimal modulation method. Using the result of the harmonic flux distortion evaluation presented in Fig. 3.11 on page 59 and evaluating the ratio between the harmonic flux distortion of the suboptimal modulation method and any of the other modulation methods, the switching frequency correction factor can be found.

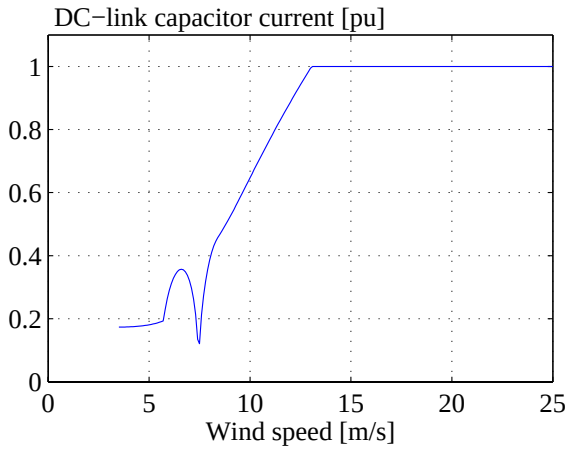


Figure 3.44: *The current through the DC-link capacitors as a function of the wind speed in a typical wind turbine application.*

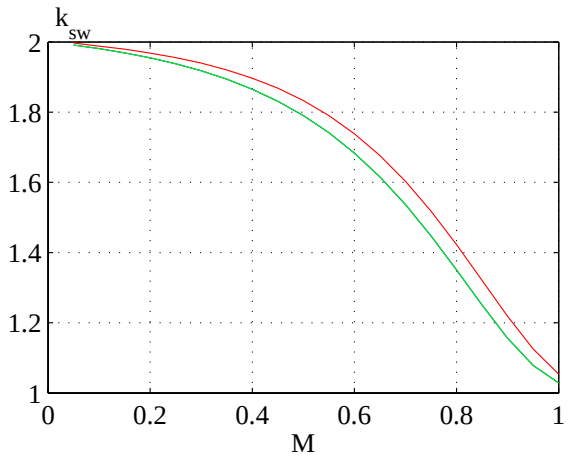


Figure 3.45: *The switching frequency correction factor. (-) is for the sft-modulation method while (-) is for the aslft- and asrft-modulation methods.*

For the symmetrical flat top modulation method, the switching frequency correction factor can be approximated by:

$$k_{sw,v} = 6.236M_0^5 - 13.730M_0^4 + 9.603M_0^3 - 3.338M_0^2 + 0.291M_0 + 1.987 \qquad (3.76)$$

where M_0 is the modulation index at nominal working conditions. For the two asymmetrical modulation methods (aslft and asrft) the switching frequency correction factor can be approximated by:

$$k_{sw,v} = 7.088M_0^5 - 15.15M_0^4 + 10.51M_0^3 - 3.696M_0^2 + 0.291M_0 + 1.982 \qquad (3.77)$$

Fig. 3.45 shows the switching frequency correction factor as a function of the nominal modulation index. From Fig. 3.45 it appears, that depending on the nominal modulation index, the switching frequency for the discontinuous modulation methods should be between 1.05 and 2 times higher than for the for the suboptimal modulation method in order to achieve the same harmonic performance.

3.6 Model of the back-to-back two level voltage source converter

Input to the back-to-back two-level voltage source converter model are both given from the generator side and from the grid side, i.e. from the transformer. Input to the rotor side inverter are the rotor voltage, rotor current, load angle and frequency, all given by the generator modeling approach described in section 2.4. Input to the grid side inverter are the grid voltage, i.e. the voltage on the tertiary side of the transformer, c.f section 2.5, the grid frequency and the desired reactive power generation from the grid

side inverter. Based on these input, the converter model has to output the resulting grid current supplied to the tertiary transformer windings along with internal values such as the converter losses and temperatures.

3.6.1 Converter losses

Depending on the chosen modulation method (can be selected differently for the grid side inverter and the rotor side inverter), the total converter losses can be derived from the equations given in section 3.4. The losses of the rotor side inverter, $P_{inv,r}$, is given by:

$$\begin{aligned} P_{inv,r} &= 6\left(P_{cond,tr} + P_{cond,dr} + P_{sw,tr} + P_{sw,dr}\right) \\ &= 6\left(V_{tr0}(T)\cdot I_{avg,tr} + R_{tr}(T)\cdot I_{tr}^2 + V_{d0}(T)\cdot I_{avg,dr} + R_{dr}(T)\cdot I_{dr}^2\right) + \\ &\quad 6\cdot V_{DC}\cdot f_{swr}\cdot\left(E_{sw0,tr}(T) + E_{sw0,dr}(T)\right) I_{swr,avg} \end{aligned} \tag{3.78}$$

The current quantities in eq. (3.78) has to be evaluated according to the chosen modulation strategy. The modulation method dependent expression for the current quantities were derived in section 3.4.

Similarly, the grid side inverter losses may be evaluated:

$$\begin{aligned} P_{inv,g} &= 6\left(P_{cond,tg} + P_{cond,dg} + P_{sw,tg} + P_{sw,dg}\right) \\ &= 6\left(V_{tg0}(T)\cdot I_{avg,tg} + R_{tg}(T)\cdot I_{tg}^2 + V_{d0}(T)\cdot I_{avg,dg} + R_{dg}(T)\cdot I_{dg}^2\right) + \\ &\quad 6\cdot V_{DC}\cdot f_{swg}\cdot\left(E_{sw0,tg}(T) + E_{sw0,dg}(T)\right) I_{swg,avg} \end{aligned} \tag{3.79}$$

The grid inductor power losses P_L are calculated according to eq. (3.51) on page 73.

3.6.2 Power transferred to the transformer

According to eq. (2.47) on page 39 input to the transformer modeling approach is the grid inverter current $\underline{I}_{g3}$, the stator current I_s and the primary side voltage $\underline{V}_{g1}$. Hence, besides the converter losses, the only necessary output from the converter modeling is the grid inverter current.

$$\underline{I}_{g3} = \frac{\left(P_r - \left(P_{inv,r} + P_{inv,g} + P_L\right)\right) + j\cdot Q_g^*}{3\cdot \underline{V}_{g3}} \tag{3.80}$$

3.7 Summary

This chapter has provided a comprehensive overview of the back-to-back two-level voltage source converter, conventionally used in variable speed wind turbines. The section was introduced by an explanation of the operating principles followed by a detailed description of the most commonly used modulation methods. For the considered modulation methods, harmonic performance were evaluated in order to be able to select a

switching frequency with comparable harmonic distortion. Further, closed form analytical expressions for the modulation method dependent conducting losses and switching losses has been derived. With the purpose of including the switch temperature in the converter loss evaluation, analytical expressions for the average switch temperature has been derived. Further, due to the fact that the rotor inverter in the doubly-fed system is operated at low frequencies the peak temperature deviate quite much from the average temperature. Hence for the purpose of a fast validation of a certain converter design, some analytical approximations has been proposed. Finally, to be able to predimension the back-to-back two-level voltage source converter, some rules of thumb regarding switch current ratings, switch voltage ratings, DC-link design and inductor design have been presented.

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Chapter 4

The matrix converter

SINCE the early nineties matrix converters have received considerable attention and especially in applications requiring bi-directional power flow, the matrix converter might become a competitive alternative to the conventional back-to-back voltage source converter. A forte of the matrix converter is the direct AC to AC conversion, by which the large energy storage element of conventional converters is avoided. Due to this lack of the energy storing element, many publications express expectations of a higher efficiency and a more compact design [6, 15, 20, 51].

The main purpose of this chapter is to derive some tools enabling an investigation on whether the matrix converter is competitive to the two-level back-to-back voltage source converter with regards to efficiency - especially when considered in the specific application of a wind turbine based on the doubly-fed induction generator. The chapter starts with a historical review on the matrix converter which in brief terms presents the evolution of the converter and lists the most significant publications. As the matrix converter is a quite rarely used and unknown type of power converter in a commercial aspect, the operating principles of the converter are explained in detail. This explanation especially focuses on the control of the switches - known as modulation - which for the matrix converter is a little more complex than for the two-level inverter as the grid current and generator voltage has to be shaped by the same switch combinations. The chapter includes a discussion of known modulation principles as well as development of three new modulation schemes. To be able to compare and select a modulation strategy for the matrix converter, the discussed modulation strategies are evaluated with regard to their waveform quality - both on the grid side and on the generator side - as well as their influence on power loss generation. Then, some aspects regarding component ratings and filter design are outlined and finally, to be used in a converter evaluation and converter comparison, the losses of the matrix converter are modeled.

4.1 Previous work

The fundamental ideas behind the matrix converter are quite old, indeed the first theoretical work was carried out during the 1920´s and 1930´s. Nevertheless, in almost any

literature concerning the matrix converter, the work done by Pelly and Gyugyi [23] is honoured as the invention of the matrix converter. At that time the lack of suitable switches with intrinsic turn-off capability had a restrictive influence on the further development within the field. Ten years after the publication of Pelly and Gyugyi´s work, only about ten papers have treated the matrix converter. Among these, especially the work carried out by Venturini and Alesina [57, 58] has contributed to the development of the matrix converter. In fact, the conventional matrix converter topology was introduced by Venturini in 1980 [57]. Fig. 4.1 shows the basic topology of the conventional matrix converter used in a doubly fed system. Each of the switches in Fig. 4.1 represents a bi-directional switch.

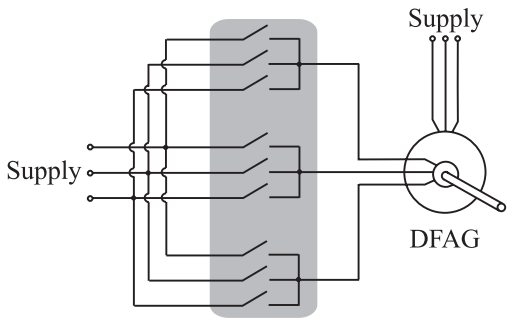


Figure 4.1: *Topology of the conventional matrix converter.*

Besides the problems concerning the switches, a major problem at this early stage was the restriction in the output voltage and the lacking ability of independent control of the input power factor. The output voltage was limited to half the input voltage and the input power factor was restricted to above the output power factor. To overcome these problems, a number of different conversion algorithms had been proposed, among others in [30, 35, 51]. A common drawback of these attempts was that the improved output performance was achieved at the expense of the input waveform and/or the converter complexity. In 1988 Alesina and Venturini [1, 2] presented a new conversion algorithm utilizing the theoretical maximum output voltage of $\sqrt{3}/2$ of the input voltage with sinusoidal input current. In addition full control of the power factor was achieved, however at the expense of the amplitude of the output voltage. Whether this publication was the breakthrough for the matrix converter is uncertain, but from about 1989 the amount of publications concerning the conventional matrix converter has increased significantly.

Today more than 400 papers concerning the matrix converter have been published, where the majority treats the matrix converter for implementation in a conventional three phase motor drive. Only about six publications have treated the matrix converter in a wind turbine application [3, 17, 22, 34, 67, 68], where the bi-directional power flow (almost) is a necessity. Regarding practical use, the 3MW Growian turbine erected in the early eighties was based on the cyclo-converter[1] [60].

[1]The cyclo-converter is based on the same principles as the matrix converter but without the possibility of force commutating the involved switches

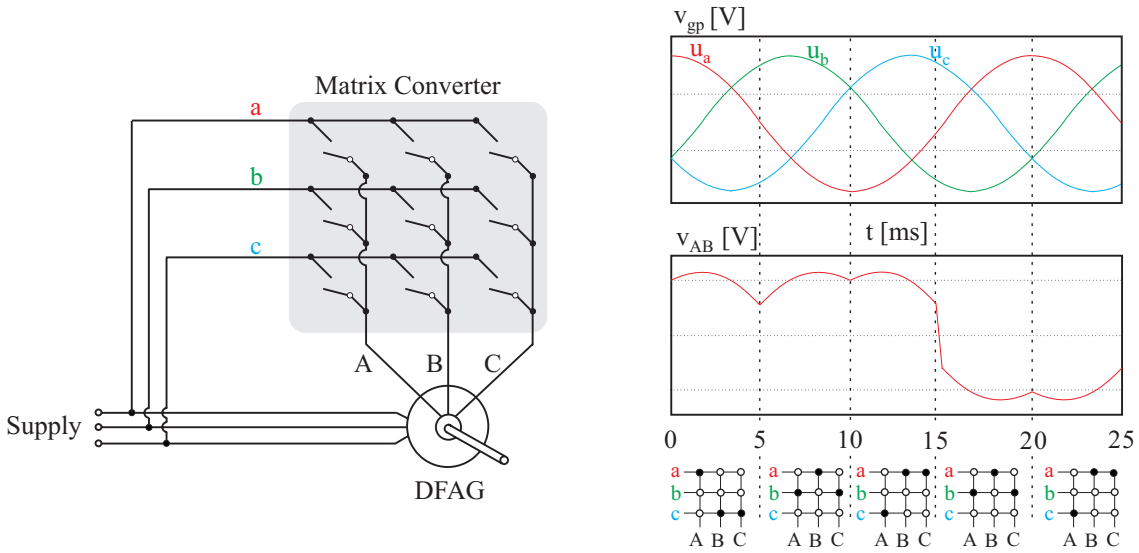


Figure 4.2: *Operation principles of the matrix converter.*

4.2 Operating principles

Compared to the operating principles of the back-to-back two-level voltage source converter which can be treated as two separate inverters, the operating principles of the matrix converter is rather complicated due to the fact that both input and output waveforms have to be shaped in the same conversion step. This section pursues to explain the basic operating principles of the matrix converter and to define the switch-state notation which will be used throughout the chapter. Besides the rather theoretical explanation of the basic operating principles the chapter includes a review on issues such as bi-directional switch realization, commutation strategies, unbalanced supply conditions and shut down procedures - issues necessary to consider if the matrix converter is to be operative.

4.2.1 Reference voltage and current generation

The aim for the matrix converter is to synthesize a rotor voltage that generates the desired generator active- and reactive power at the desired rotational speed and at the same time synthesize a sinusoidal input current matching the desired power factor demand on the grid side of the converter. Considering the generation of a rotor voltage reference, this task is equivalent to the case of the back-to-back two-level voltage source converter. Hence the control structure illustrated in Fig. 3.4 on page 49 may very well suit the purpose of generating a voltage reference for the matrix converter as well. At the grid side, the matrix converter is to be considered as a current source and hence one could expect that the control of the matrix converter would have to generate a current reference. However, due to the fact that the matrix converter does not include an energy storing element no active power can be stored and hence the active current generated to the grid will at any time have to represent the active power processed on the rotor side.

Hence the matrix converter is to be controlled without actually having an amplitude for a desired grid current. As will be shown in section 4.3 concerning the modulation of the matrix converter, the only references needed in order to control the grid current are the instantaneous angle of the voltage vector measured between the grid filter and the matrix converter and the desired power factor at the grid side of the input filter whereas the amplitude of the input current is inherently generated by controlling the switches of the matrix converter to generate the desired generator rotor voltage. The control of the grid side power factor may either be realized as an open loop control using the filter component values to calculate the phase shift across the grid filter or as a closed loop control using the currents measured at the grid side of the grid filter.

4.2.2 Voltage and current synthesizing

The basic idea of the matrix converter is, that a desired input current $i^{\star}_{gp}$, output voltage $v^{\star}_{rp}$ and output frequency $f^{\star}_{r}$ can be obtained by properly connecting the output terminals to the input terminals. Fig. 4.2 on the page before illustrates the operating principles for the matrix converter. The switching pattern in Fig. 4.2 serves only as illustration of the operating principles of the matrix converter. From Fig. 4.2 it appears that 2^9 different switch state combinations exist, although the most of these switch state combinations are invalid. In order to protect the converter, two basic control rules have to be obeyed:

Short circuit of the supply: From the matrix converter topology shown in Fig. 4.2 it is obvious that two switches in the same output leg are not allowed to be in a conducting state at the same time.

Braking an inductive current: Due to the inductive nature of the load of the matrix converter, all output phases have to be connected to an input phase.

Complying with these two control rules, the allowable switch state combinations are reduced to 27. Fig. 4.3 summarizes the allowed switch combinations. Each of these switch combinations are characterized by a three letters code, -one per rotor side phase, where each letter denotes to which grid phase the respective rotor phase is connected.

Since no internal energy storage is present, the relation between input quantities and output quantities is clear. From Fig. 4.2 the transfer matrix in eq. (4.1) can be obtained.

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} m_{Aa}\, m_{Ab}\, m_{Ac} \\ m_{Ba}\, m_{Bb}\, m_{Bc} \\ m_{Ca}\, m_{Cb}\, m_{Cc} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} m_{Aa}\, m_{Ba}\, m_{Ca} \\ m_{Ab}\, m_{Bb}\, m_{Cb} \\ m_{Ac}\, m_{Bc}\, m_{Cc} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{4.1}$$

where m_{xy} represents either the switch state at any instant of time or the duty-cycle for switch s_{xy} in a switching period. Complying with the two control rules above, the

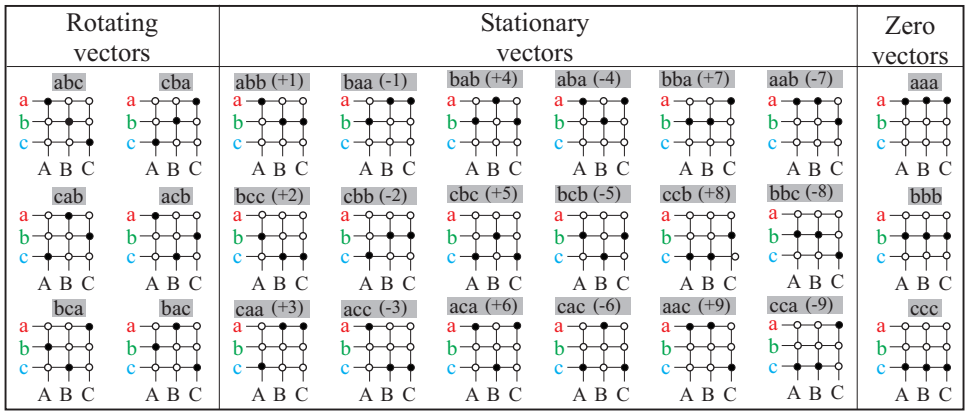


Figure 4.3: *The 27 allowed switch combinations.*

constraint in eq. (4.2) is derived.

$$\sum_{y=a}^{c} m_{xy} \equiv 1 \quad x \in [A, B, C] \tag{4.2}$$

The procedure for filling out the transfer matrix depends on the modulation strategy [48] and will be discussed in section 4.3.

4.2.3 Switch configuration

In the converter topology treated in the previous chapter only unidirectional switches were required. A unidirectional switch offers the opportunity of conducting bi-directional current and withstand unipolar voltage. For the matrix converter, the need for a switch which in addition can block bipolar voltages and control bi-directional current flow arises. Until recently (about 2003) a bidirectional switch had to be built up from several standard semiconductor devices. In [49] three different bidirectional switch configurations were presented. Fig. 4.4a-c show these configurations. Fig. 4.4d shows a bi-directional switch realized by use of a standard H-bridge transistor module.

The diode embedded switch shown in Fig. 4.4a consists of only one transistor and four diodes. In early papers dealing with the matrix converter this switch configuration was preferred because it only requires one active switch [5]. In a three-phase to three-phase matrix converter based upon the diode embedded switch a total number of transistors, diodes and gate drive supplies amounts to 9, 36 and 9 respectively. Whenever a diode embedded switch is conducting, the conducting path involves three semiconductors -the transistor and two diodes. Hence the on-state losses become relatively large compared to the other switch cell configurations. Since the diode embedded switch acts as a true bidirectional switch, the direction of the current cannot be controlled and every switching becomes a *hard-switching*. Because of the hard-switchings, the switching losses of the diode embedded switch becomes relatively large [63]. In addition, the property as a true bi-directional switch constitutes a problem for the commutation between two input

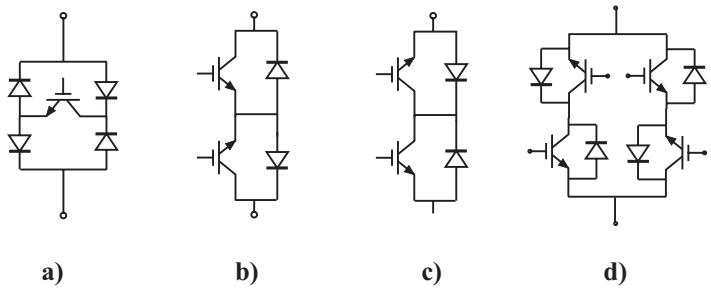


Figure 4.4: *Bi-directional switch topologies.* **a)** *Diode embedded switch.* **b)** *Anti parallel switch with common emitter.* **c)** *Anti parallel switch with common collector.* **d)** *Standard H-bridge module.*

phases. To deal with the commutation problem either a snubber circuit or additional line inductances have to be added. The commutation problem is treated in the next section.

The common emitter switch shown in Fig. 4.4b consists of two transistors and two diodes. The presence of the diodes ensures that the reverse voltages across the transistors are limited to the on-state voltage drop of the diodes. By use of the common emitter switch cell only one gate drive supply per cell is required. The total number of transistors, diodes and gate drive supplies for a three-phase to three-phase matrix converter amounts to 18, 18 and 9 respectively. The conducting path of the common emitter switch involves only one transistor and one diode. The common emitter switch cell does not act as a true bi-directional switch because the direction of the current is controllable. By use of this property, the commutation problems can be solved by a proper switching pattern, which is treated in the next section.

The characteristics of the common collector switch cell in Fig. 4.4c is to a great extent similar to the common emitter switch cell. Dependent on the number of input- and output lines of the matrix converter, the number of gate drive supplies can be reduced in comparison with the common emitter switch cell. In the case of a three-phase to three-phase matrix converter based upon the common collector switch, the number of gate drive supplies may ideally be reduced[2] to 6.

Fig. 4.4d shows a bi-directional switch, constructed from a standard H-bridge semiconductor device. By this arrangement a standard module forms two parallel bi-directional switches - one based on the common-emitter approach and one based on the common collector approach. By this switch realization, a three-phase to three-phase matrix converter can be realized by 9 standard H-bridge modules and 15 isolated gate drive supplies.

[2]In a high current application as discussed herein, the voltage drop across stray inductances will constitute a serious problem for the establishment of a common-emitter potential and hence the matrix converter in the present application may not benefit from this opportunity.

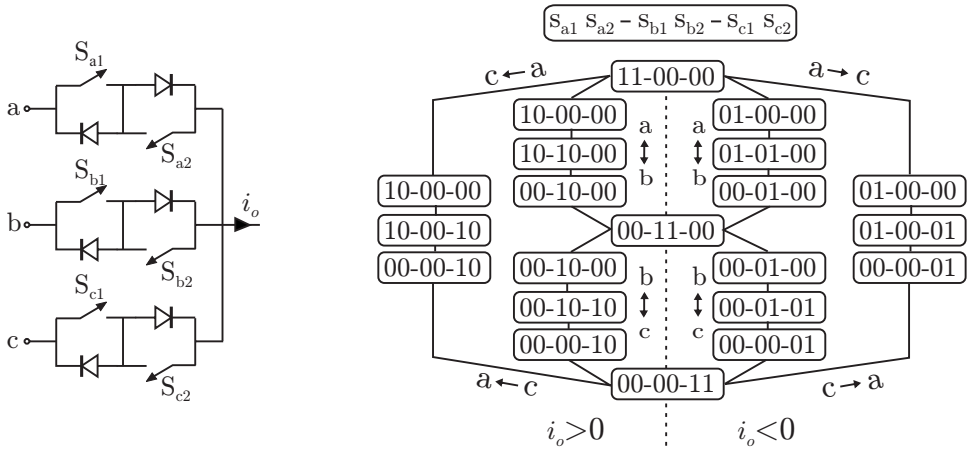


Figure 4.5: *Illustration of the semi-soft switching algorithm based upon the output current.*

In present semiconductor technology, a true bi-directional switch with current direction control is actually available [44] and clearly such a switch built into a phase-leg switch cell or even integrated as an embedded matrix converter will clearly increase the competitiveness of the matrix converter.

4.2.4 Commutation strategy

Since the switches of the matrix converter do not offer ideal switching characteristics, i.e. instantaneous turn-on and turn-off, the two basic control rules can not both be full filled. Hence a quandary of the matrix converter is the phase commutations. The commutation problem is treated in several of the papers concerning the matrix converter [51]. However, the proposed solutions to the commutation problem is only divided into five different strategies. Four of these strategies are briefly explained in the following. Furthermore current reversals may constitute a problem for the switch cells in Fig. 4.4b - 4.4d.

In [5] and [63] a phase commutation method termed *overlap current commutation* or *make before break* is discussed. In this method the incoming switch cell is fired before the outgoing switch cell is turned off. This causes a momentary short circuit of the supply. To avoid damaging over currents during the short circuit, inductors have to be added at the supply side of the converter. The presence of inductors of the supply side of the matrix converter demands snubber circuits to avoid overvoltages across the transistors. These additional components increases the losses of the matrix converter [19]. In the overlap current commutation, current reversals do not present a problem since all transistors in the switch cell are fired.

In [46] a *dead time* or *break before make* commutation strategy is mentioned. In this strategy the commutation problem is handled by introducing a delay between the turn

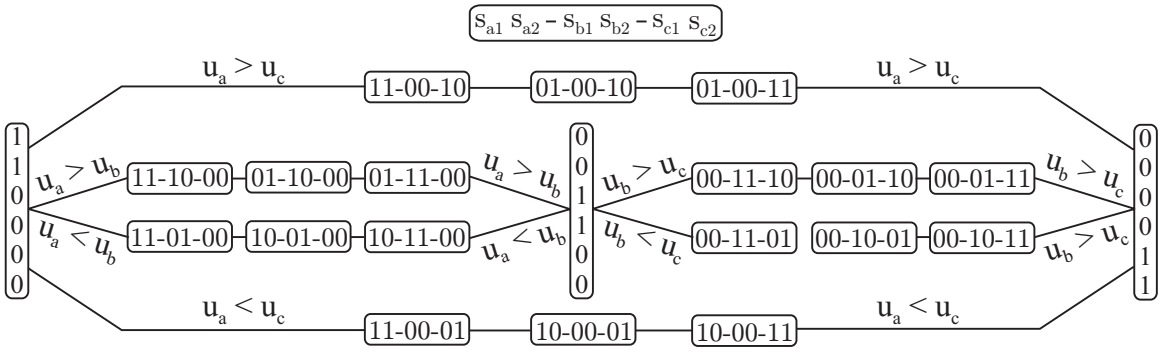


Figure 4.6: *Illustration of the semi-soft switching algorithm based upon the phase voltages.*

on of the incoming switch cell and the turn off of the outgoing switch cell. To avoid over voltages across the semiconductors caused by the inductive load current, a snubber network must be used to provide a current path. In [55] and [62] it is stated that this commutation strategy also introduces additional losses of the matrix converter. Since all transistors in a switch cell are fired in the *dead time* commutation strategy, this method does not present a current reversal problem either.

A third and more reliable commutation strategy, based on the switch cell configuration in Fig. 4.4b - Fig. 4.4d was proposed almost contemporary in [7, 29, 51], and subsequently treated in several papers. In this method the transistors in the switch cell are controlled independently. Current reversals are achieved by gating both transistors in the conducting cell. A phase commutation is achieved by turning off the non-conducting transistor in the outgoing cell before the right transistor in the incoming cell is fired. By this, the phase commutation becomes a four step process. This commutation process is shown in Fig. 4.5 on the preceding page. Because the half of the phase commutation will be natural commutations i.e. the potential of the incoming switch is higher than the outgoing switch, the switching losses might be reduced by use of this commutation strategy [4, 5, 63]. Due to this property, the commutation strategy is often termed the *semi-soft switching strategy*. A problem with the semi-soft switching strategy is the detection of the current direction at low current levels and at current reversal. These problems are treated in [18, 19].

Contrary to the semi-soft switching algorithm in Fig. 4.5 where the phase commutation depends on the current direction, [42] proposed a different semi-soft switching algorithm, where the phase commutation depends on the input phase voltage. This algorithm is illustrated in Fig. 4.6. The commutation strategy in Fig. 4.6 requires knowledge of the instantaneous phase voltages.

Finally, closely related to the commutation is the voltage error introduced by the time interval occupied by the commutation sequence. Especially at low output voltages

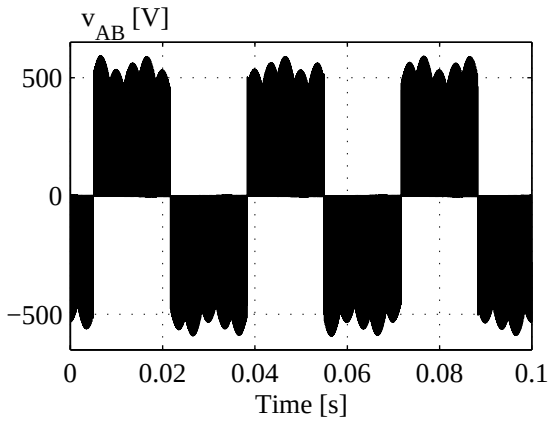


Figure 4.7: *Simulated output voltage V_{AB} under 6% unbalanced input voltage.*

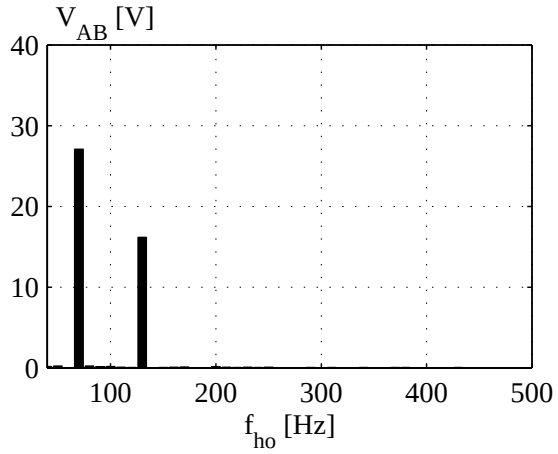


Figure 4.8: *Output voltage spectrum for the simulation in Fig. 4.7.*

(which actually are likely to be present in the doubly-fed system) the problems related to such an issue may be critical. Analysis and solutions of such problems are among others addressed in [24, 64, 65].

4.2.5 Unbalanced supply- and load conditions

The absent of the energy storing elements in the matrix converter causes that unbalanced or distorted conditions in the input voltage are transferred to the output of the matrix converter. In [20], the effects of unbalanced input conditions were analyzed, and it was found, that output harmonics f_{oh} appears from the following frequencies (if no compensation is performed):

$$f_{oh} = 2f_g \pm f_r; \tag{4.3}$$

where f_g is the input frequency and f_r is the desired output frequency. From eq. (4.3) it is evident that for output frequencies lower than the input frequency, the emitted output harmonics are higher than the fundamental of the output frequency, while for output frequencies higher than the input frequency subharmonics are introduced. Fig. 4.7 shows the simulated output voltage (phase-phase) of the matrix converter when the input voltage is 6% unbalanced and the desired output frequency f_r is 30 Hz. The imbalance ratio is determined in accordance with [10]. From eq. (4.3) the expected harmonics is at 70 Hz and 130 Hz. Fig. 4.8 shows the frequency spectrum from 40 Hz to 500 Hz. Similar, the input current of the matrix converter contains undesirable harmonics under unbalanced input voltages. Fig. 4.9 and Fig. 4.10 shows the simulated input current and input current spectrum respectively.

Because the instantaneous input power must equal the instantaneous output power, it is obvious that the matrix converter cannot be controlled to achieve both balanced sinusoidal input currents and balanced sinusoidal output voltages, when the input volt-

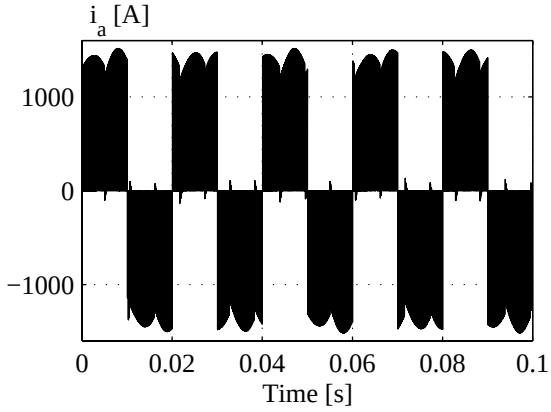


Figure 4.9: *Simulated input current i_a under 6% unbalanced input voltage.*

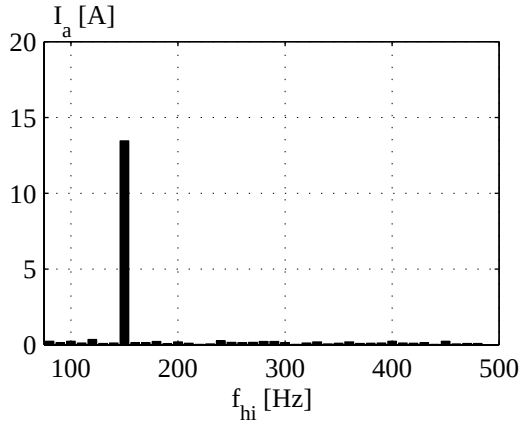


Figure 4.10: *Input current spectrum for the simulation in Fig. 4.9.*

age is unbalanced. In the literature, several compensation techniques are proposed [10, 11, 48, 50, 69], all achieving sinusoidal balanced output voltages. The difference between the proposed methods are the direction along which the input current is modulated while the difference between the performance of the compensation methods is the degree of distortion and the RMS value of the input current. In the following a brief presentation of the three proposed methods is given.

The first compensation method was proposed in [10] and the objective of this strategy was to achieve the minimum RMS input current for a given output power, thus achieving minimum line losses. Based upon measurements of the instantaneous input voltage the modulation index has to be recalculated in every switching period in order to achieve balanced output voltages and to keep the input current angel equal to the input voltage angel. In order to evaluate the compensation technique the emission of input current harmonics are calculated[3]. In [10] it was found that this compensation technique only gives rise to emission of positive odd harmonics with amplitudes given by:

$$I_{hk} = I_1 u^{(k-1)/2} \quad k = [3, 5..\infty] \tag{4.4}$$

where u is the degree of imbalance. Furthermore it was found that the total harmonic distortion THD_i of the input current is given by:

$$THD_i = \frac{u}{\sqrt{1-u^2}} \tag{4.5}$$

An extension to the work in [10] is given by [12] where the matrix converter operation is analyzed under unbalanced input voltage and unbalanced load. By the unbalanced

[3]The evaluation of current harmonics in a three phase unbalanced system is a *hard topic* because the harmonics may be balanced as well as unbalanced with regard to the three phases. In [21], the harmonics are evaluated in the complex space vector plane. By this the harmonics in the three phase system can be evaluated as positive and negative rotating space vectors. That is: the presence of both a positive and negative rotating space vector at a given frequency describes an unbalanced harmonic while the presence of only a positive or a negative vector describes a balanced harmonic.

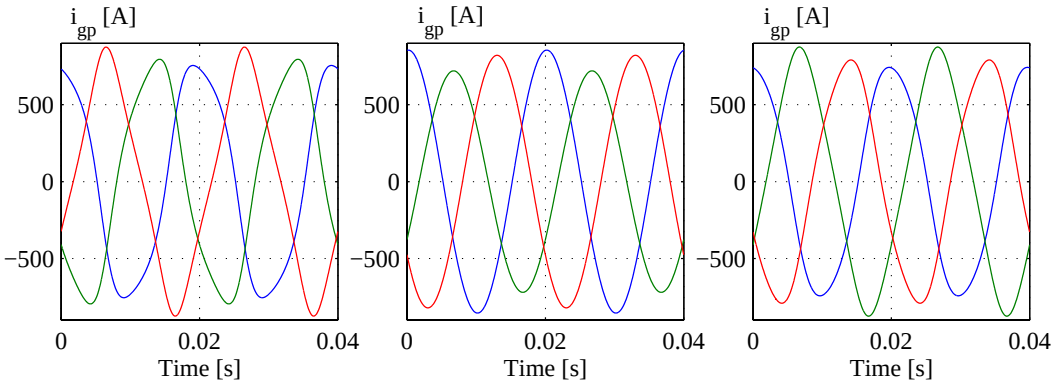


Figure 4.11: *Simulated input currents for the three compensation techniques. The unbalanced ratio u is 10%. From left, the method proposed by [10], the method proposed by [11] and the method proposed by [48].*

load several sub- as well as super harmonics are added to the harmonic content given in eq. (4.4).

In [11] a slightly different approach were considered. The main strategy in this technique is to achieve the minimum harmonic distortion of the input current, however at the expense of a higher and unbalanced RMS line current. By this method only the fundamental harmonic is represented but with a positive and a negative sequence. The amplitude of the negative sequence is given by:

$$I_{hk} = u \cdot I_1 \quad ; \quad k = -1 \tag{4.6}$$

Since the method in [11] does not emit higher harmonics, the total harmonic distortion of the input current equals zero.

A third compensation technique was proposed in [48] and [50]. The objective was to achieve a method for simple implementation. In [50] the current is simply modulated along one of the phase voltages (a, b or c). The performance of this method depends on both the unbalanced ratio u and upon the direction of imbalance[4]. However, in [48] it is stated that the performance of this method seems to be a compromise between the method proposed by [10] and the method proposed by [11]. The current waveform for each of the proposed compensation techniques is illustrated in Fig. 4.11. In [48], and [50] the three compensation techniques are explained in detail and a comparison is performed. It is stated that the first method ([10]) and the third method ([48]) is the most straight forward to implement, while the method by [11] takes more on-line computations.

In the three methods presented above, the displacement angel of the input current

[4]The direction of imbalance is the direction of the major ellipse axis in the complex space vector plane.

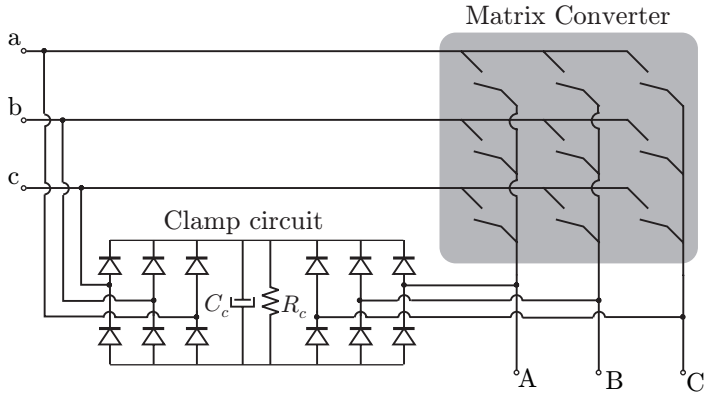


Figure 4.12: *The clamp circuit proposed by [2]*

is predetermined. A compensation technique was proposed by [53] where the input displacement angle was controllable, but the performance obtained by this method is not comparable to the results obtained by the other three methods. The presence of harmonic distorted and unbalanced input voltage is analyzed in [14]. Based upon analytical expressions, the major content of harmonics in the input current can be predicted, but no compensation technique was developed.

4.2.6 Protection and shut down

Another crucial problem of the matrix converter is the shut down. In a fault situation, a momentary shut down of the matrix converter may be unavoidable. In the basic topology, cf. Fig. 4.1 on page 90, such a shut down would cause over voltages across the switches due to the magnetic energy stored in the load. Adding the clamp circuit in Fig. 4.12, the stored energy in the load is transferred to the clamp capacitor C_c. The voltage across the switches during a shut down can then be controlled by the size of the clamp capacitor and the clamp resistor. In order to reduce the size of the clamp capacitor, and to eliminate the continuous power dissipation in the clamp resistor R_c, an active clamp circuit was proposed in [48]. In this configuration, a transistor is placed in series with the clamp resistor. The transistor is turned on whenever the voltage across the clamp capacitor is above the normal voltage level. In [48] it is suggested that the rectified voltage in the clamp circuit might be used for internal supply of the control- and driver circuits.

In [54], the shut down of the converter is actively controlled, thereby reducing the need for a clamp circuit. The philosophy in [54] is, that during a transitional phase, the load is de-magnetized by applying reverse biased voltages. (The technique is very similar to the shut down of a conventional PWM-VSI, where the free-wheeling diodes induces the de-magnetizing voltage.) When the load is de-magnetized, the control signals are removed.

4.3 Modulation

During the past, the modulation of the matrix converter has evolved from complicated modulation expressions based on transfer function approaches to modern space-vector modulation. Actually, the literature distinguish between the following modulation methods.

- **Direct transfer function approach:** In the early research phases of the matrix converter, the modulation was based on solving the nine equations in (4.1) and eq. (4.2) with a sinusoidal reference for the input current and the output voltage [57]. By this method the output voltage was restricted to 0.5 times the input voltage. In [1] the voltage transfer ratio was increased to 0.866 times the input voltage by adding a harmonic component to the output reference voltage. The direct transfer function approach comprehends all the desirable properties, i.e. maximum voltage transfer ratio, sinusoidal input/output, and adjustable power factor. However, the formulae for the duty cycle computation are complicated and require considerable computational power for real time implementation [66]. In addition the switching losses by this method are rather high due to a high number of switch commutations per switching cycle [61].

- **Indirect transfer function approach:** The indirect modulation was used in [37] and [46]. By this method, the matrix converter is separated in a rectifier part and an inversion part, which are modulated separately. Compared to the direct transfer function approach, the indirect transfer function approach requires less computational power [33].

- **Carrier based modulation:** From modulation of conventional converters, the carrier based modulation was adapted for use in matrix converters. The first attempts [36] and [56] mainly focused on the modulation of the output voltage, at which a relatively simple modulation was achieved. Extensions to the carrier based modulation was added by [52], where the modulation also included the input current.

- **Conventional space vector modulation:** The conventional space vector modulation [9, 28, 30], utilizes that all the switch combinations in the stationary vector group in Fig. 4.3 results in position-stationary vectors for both input current and output voltages when transformed to the complex space vector plane. By this, the normally known space vector approach can be used to modulate both the input current and the output voltage. In [45] a space vector modulator, which also utilizes the six rotating vectors of the matrix converter was proposed, by which the harmonic content was reduced.

- **Indirect space vector modulation:** Combining the principles of the indirect transfer function approach with the principles of space vector modulation leads to the indirect space vector modulation. In the indirect space vector modulation

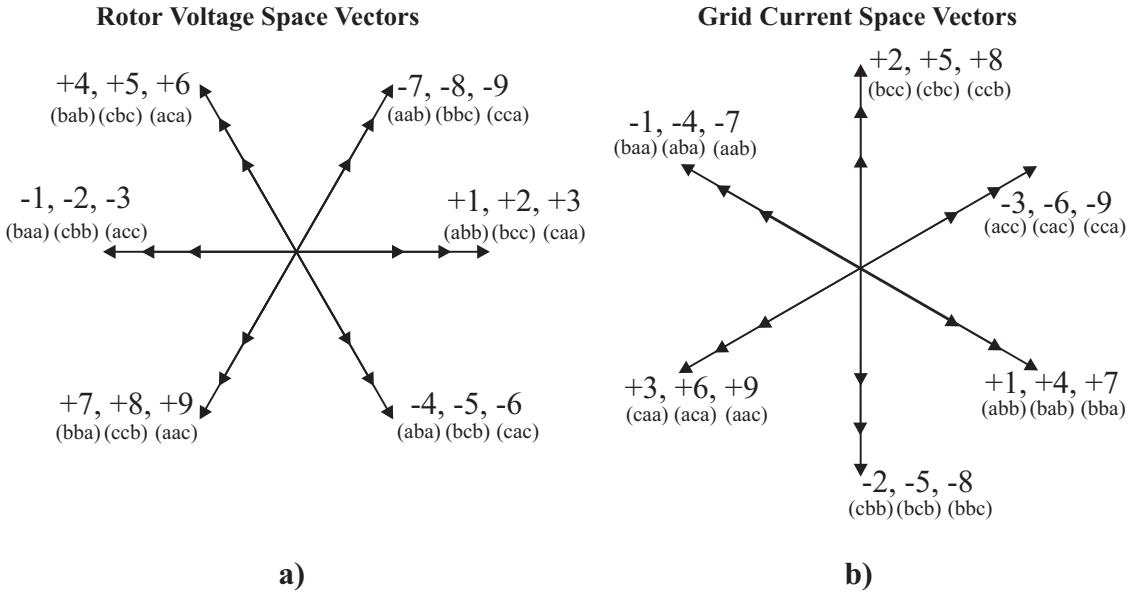


Figure 4.13: *The rotor voltage space vectors and the grid current space vectors for the active switch combinations, c.f. Fig. 4.3.*

the SVM is performed individually for the rectification and the inversion. The indirect modulation is among others treated in [31, 32, 33, 47]. In [48] the number of switchings in the indirect space vector modulation was optimized, achieving lower switching losses.

In [13], an approach is presented allowing a space-vector-like implementation of the earlier carrier based modulation schemes and thereby a straight forward comparison of the early and recent modulation schemes. In modern control of matrix converters, the first three modulation strategies are no longer of importance and only the latter two are used in recent papers. The difference between the conventional space vector modulation and the indirect space vector modulation is only a matter of abstraction level while the performance is completely identical. In this thesis, the conventional space vector modulation approach will be used.

4.3.1 Space vector representation for matrix converters

The space vector approach is based on the transformation of the time varying quantities into the complex space vector plane. For the space-vector modulation of the matrix converter it is appropriate to define the following four space vectors.

$$\underline{V}_{gp} = \frac{2}{3}(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{j\frac{4\pi}{3}}) \tag{4.7}$$

$$\underline{V}_{rp} = \frac{2}{3}(v_A + v_B e^{j\frac{2\pi}{3}} + v_C e^{j\frac{4\pi}{3}}) \tag{4.8}$$

$$\underline{I}_{gp} = \frac{2}{3}(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}}) \tag{4.9}$$

$$\underline{I}_{rp} = \frac{2}{3}(i_A + i_B e^{j\frac{2\pi}{3}} + i_C e^{j\frac{4\pi}{3}}) \tag{4.10}$$

where $\underline{V}_{gp}$ is the space-vector representation for the grid phase voltage, $\underline{V}_{rp}$ is the space-vector representation for the rotor phase voltage, $\underline{I}_{gp}$ is the space-vector representation for the grid current and $\underline{I}_{rp}$ is the space-vector representation for the rotor current. Applying eq. (4.8) on the active switch combinations shown in Fig. 4.3 on page 93 it turns out that all these combinations become stationary vectors in the space vector plane, however with time varying amplitudes. The rotor voltage vectors for the active switch combinations are shown in Fig. 4.13a. Similar, by utilizing eq. (4.9) it appears that the active switch combinations correspond to position stationary grid current vectors in the complex space vector plane. The grid current space vectors are shown in Fig. 4.13b. Due to these properties of the active switch combinations, the well known space vector modulation principles can be applied to the matrix converter, although the modulation has to consider both the grid current and the rotor voltage.

In the following, two different approaches are presented, one named the conventional space-vector modulation [9] and an alternative method named the modified space vector modulation [27].

4.3.2 Conventional space vector modulation

In the conventional space vector modulation, the sectors are defined as shown in Fig. 4.14. It should be noted that the amplitudes of both the rotor voltage vectors and the grid current vectors are varying, depending on the grid voltage angle, Δ_g, and the rotor current angle. (The rotor current angle is not defined in Fig. 4.14 because the modulation are to be independent of this angle, i.e. independent of the load). In the derivation of the space vector modulation, it is appropriate to define the angles Δ_g and Δ_r to be independent of, in which sector they are located. Hence the grid angle Δ_g used in the conventional space vector modulation is defined as:

$$\Delta_g = \mod\left(\omega_g t, \frac{\pi}{3}\right) \tag{4.11}$$

where $\omega_g t = 0$ is defined as the positive zero crossing of the phase a grid voltage ($v_a = \hat{v}_g \cdot \sin(\omega_g t)$) and the operator "mod" is the modulus after division. Similar, the rotor voltage angle Δ_r is defined as:

$$\Delta_r = \mod\left(\left(\omega_r t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \tag{4.12}$$

where $\omega_r t = 0$ is defined as the positive zero crossing of the phase A rotor reference voltage ($v_A^\star = \hat{v}_A \cdot \sin(\omega_r t)$). For an arbitrary sector location of the rotor voltage reference

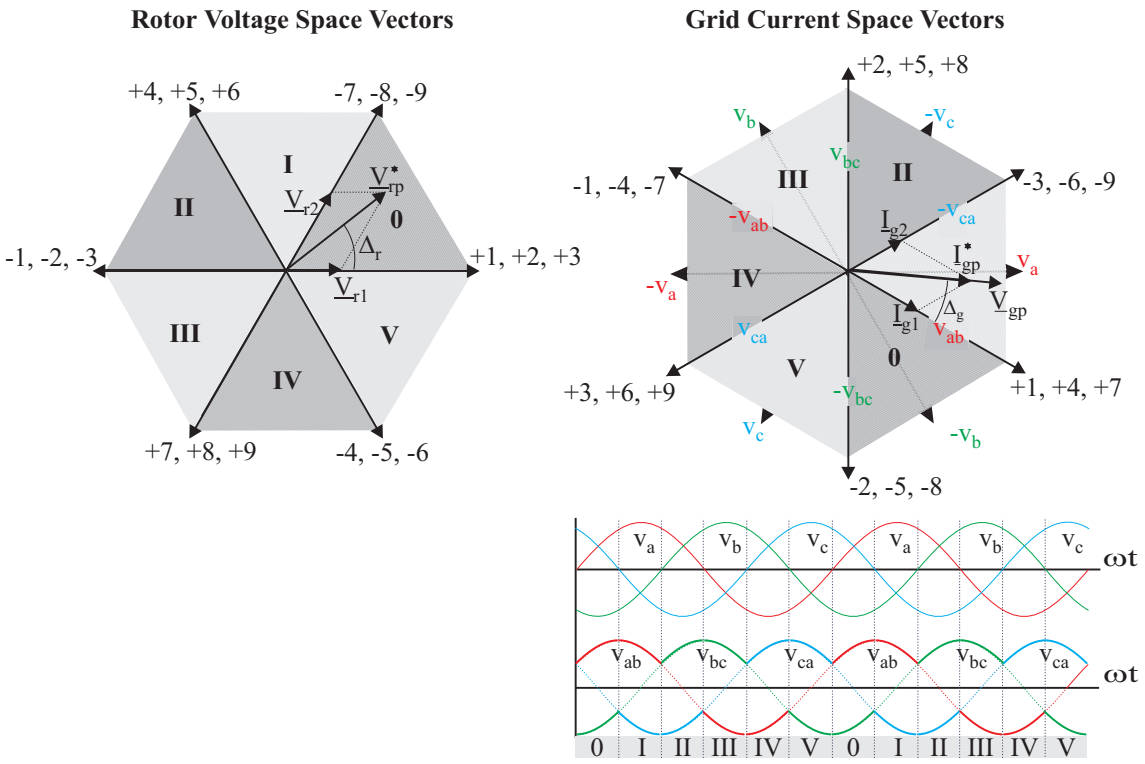


Figure 4.14: *Angle and sector definitions for the conventional space vector modulation.*

and the grid current reference, the following equations can be derived ($\underline{V}^{\star}_{rp} = \underline{V}_{r1} + \underline{V}_{r2}$):

$$\begin{aligned} \underline{V}_{r1} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot \cos\left(\Delta_g - \frac{\pi}{3}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \delta_2 \cdot \cos\left(\Delta_g - \pi\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{4.13}$$

$$\begin{aligned} \underline{V}_{r2} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_3 \cdot \cos\left(\Delta_g - \frac{\pi}{3}\right) \cdot |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot \cos\left(\Delta_g - \pi\right) \cdot |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{4.14}$$

where $\delta_{1..4}$ are the on-time duration for the four applied vectors in a switching period. In each input sector, only the two line-line voltages with the highest amplitudes are used. This is illustrated in the lower part of Fig. 4.14. By similar considerations the input current vectors can be calculated ($\underline{I}^{\star}_{gp} = \underline{I}_{g1} + \underline{I}_{g2}$):

$$\begin{aligned} \underline{I}_{g1} &= |\underline{I}^{\star}_{gp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_2 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{4.15}$$

$$\begin{aligned} \underline{I}_{g2} &= |\underline{I}^{\star}_{gp}| \cdot \sin\left(\Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_3 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{4.16}$$

where i_x and i_y are the instantaneous value of a rotor phase current. Assuming that the rotor currents are sinusoidal and symmetrical, the relation between i_x and i_y becomes:

$$\begin{cases} i_x &= \hat{i}_r \cdot \sin(\omega_r t) \\ i_y &= \hat{i}_r \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right) \end{cases}$$

$$\Downarrow$$

$$i_y = i_x \frac{\sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin(\omega_r t)} \tag{4.17}$$

Combining eq. (4.15), eq. (4.16) and eq. (4.17) and rearranging, the following rotor current position dependent expressions are obtained:

$$0 = \frac{\delta_2}{\sin\left(\frac{\pi}{3} - \Delta_g\right)} - \frac{\delta_4 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin(\omega_r t)} - \frac{\delta_1}{\sin(\Delta_g)} + \frac{\delta_3 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin(\omega_r t) \cdot \sin(\Delta_g)} \tag{4.18}$$

In order to achieve a solution for the modulation functions $\delta_{1..4}$ which is independent of the rotor current position, eq. (4.18) is separated into the following two equations:

$$0 = \frac{\delta_2}{\sin\left(\frac{\pi}{3} - \Delta_g\right)} - \frac{\delta_1}{\sin(\Delta_g)} \tag{4.19}$$

$$0 = \frac{\delta_3 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin(\omega_r t) \cdot \sin(\Delta_g)} - \frac{\delta_4 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin(\omega_r t)} \tag{4.20}$$

where the position of the rotor current can be eliminated. Solving the equations (4.13), (4.14), (4.19) and (4.20) for the modulation functions $\delta_{1..4}$ gives:

$$\begin{aligned} \delta_1 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \sin(\Delta_g) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_2 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_3 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \sin(\Delta_g) \cdot \sin(\Delta_r) \\ \delta_4 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin(\Delta_r) \\ \delta_0 &= 1 - (\delta_1 + \delta_2 + \delta_3 + \delta_4) \end{aligned} \tag{4.21}$$

It should however be noted that the modulation functions at any time instant are limited by the following constraint:

$$\delta_{0..4} \geq 0$$

Taking this constraint into account, it is found that the maximum reference voltage $|\underline{V}^\star_{rp}|$ are limited to $\frac{\sqrt{3}}{2}$ of the input voltage. Using only the two line-line voltages with maximum amplitudes (which was a precondition for the derivation of the duty-cycles in eq. (4.21)), the sector-dependent switch combination for each duty-cycle function $\delta_{1..4}$ are summarized in Table I. The sectors refer to the sector location in Fig. 4.14.

TABLE I: *Switching table for the conventional space vector modulation.*

→Rec	Sector 0				Sector I				Sector II				Sector III				Sector IV				Sector V			
↓Inv	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4
0	abb	cbb	aab	ccb	acc	abb	aac	aab	bcc	acc	bbc	aac	baa	bcc	bba	bbc	caa	baa	cca	bba	cbb	caa	ccb	cca
I	aab	ccb	bab	bcb	aac	aab	cac	bab	bbc	aac	cbc	cac	bba	bbc	aba	cbc	cca	bba	aca	aba	ccb	cca	bcb	aca
II	bab	bcb	baa	bcc	cac	bab	caa	baa	cbc	cac	cbb	caa	aba	cbc	abb	cbb	aca	aba	acc	abb	bcb	aca	bcc	acc
III	baa	bcc	bba	bbc	caa	baa	cca	bba	cbb	caa	ccb	cca	abb	cbb	aab	ccb	acc	abb	aac	aab	bcc	acc	bbc	aac
IV	bba	bbc	aba	cbc	cca	bba	aca	aba	ccb	cca	bcb	aca	aab	ccb	bab	bcb	aac	aab	cac	bab	bbc	aac	cbc	cac
V	aba	cbc	abb	cbb	aca	aba	acc	abb	bcb	aca	bcc	acc	bab	bcb	baa	bcc	cac	bab	caa	baa	cbc	cac	cbb	caa

4.3.3 Modified space vector modulation

The main idea in the modified space vector modulation is to make use of the minimum line-line-voltage (contrary to the conventional space vector modulation which utilizes the two maximum line-line voltages) whenever the rotor voltage reference is lesser than half of the grid voltage. The advantages of this new modulation strategy are that the harmonic content of the rotor side voltages are reduced and additionally the switching losses are decreased. A disadvantage of the proposed modulation strategy is that the harmonic current spectra on the grid side of the converter is slightly increased. Fig. 4.15 shows the modified space vector modulation approach. The line-line voltages used within each of the sectors are indicated by the increased linewidth. The procedure for deriving the duty-cycle functions for the modified space vector modulation approach is almost similar to the procedure in the conventional space vector modulation. However for completion of the modulation description, the derivation of the modified duty-cycle function are given below.

The grid angle Δ_g used in the modified space vector modulation is defined as[5]:

$$\Delta_g = \mod\left(\left(\omega_g t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \tag{4.22}$$

where $\omega_g t = 0$ is defined as the positive zero crossing of the phase a grid voltage ($v_a = \hat{v}_g \cdot \sin(\omega_g t)$). Similar, the rotor voltage angle Δ_r is defined:

$$\Delta_r = \mod\left(\left(\omega_r t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \tag{4.23}$$

For an arbitrary sector location of the rotor voltage reference and the grid current

[5]Please note that the grid side space vector hexagon by this definition is rotated $\pi/6$ compared to the conventional space vector approach.

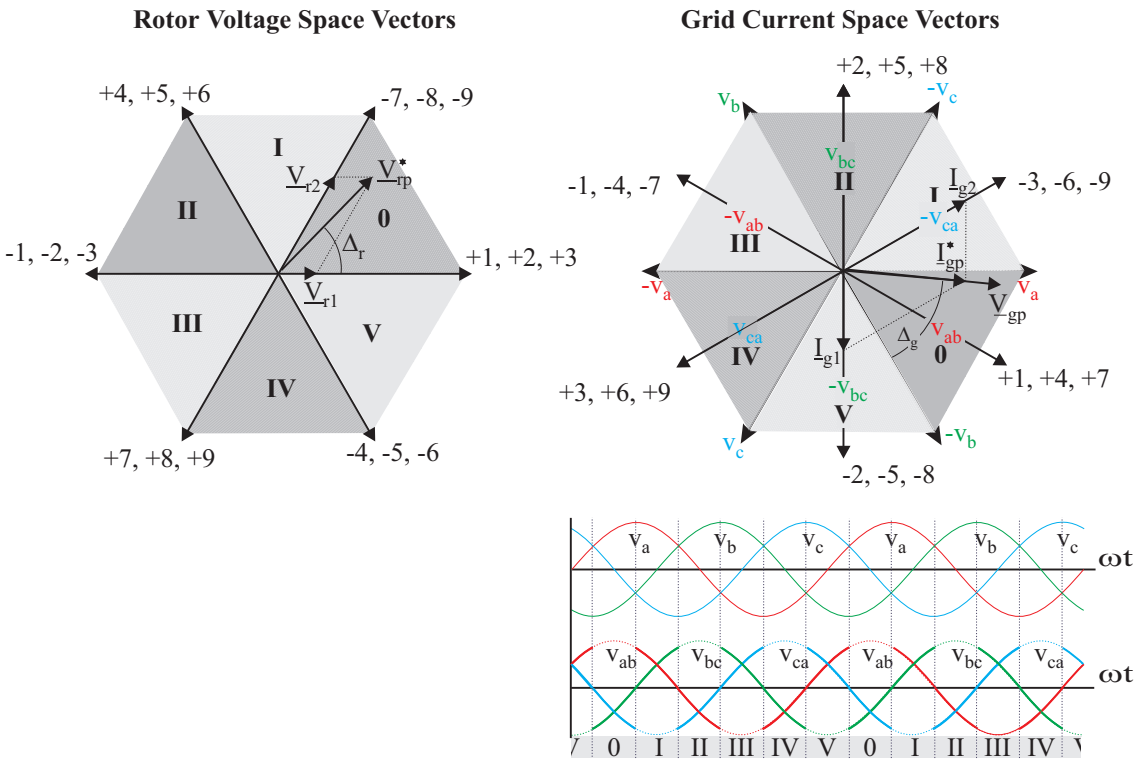


Figure 4.15: *Angle and sector definitions for the modified space vector modulation.*

reference, the following equations can be derived ($\underline{V}^*_{rp} = \underline{V}_{r1} + \underline{V}_{r2}$):

$$\begin{aligned}
\underline{V}_{r1} &= |\underline{V}^\star_{rp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\
&= -\delta_1 \cdot \cos\left(\Delta_g + \frac{\pi}{2}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \delta_2 \cdot \cos\left(\frac{5\pi}{6} - \Delta_g\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \qquad (4.24) \\
\underline{V}_{r2} &= |\underline{V}^\star_{rp}| \cdot \sin\left(\Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\
&= -\delta_3 \cdot \cos\left(\Delta_g + \frac{\pi}{2}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot \cos\left(\frac{5\pi}{6} - \Delta_g\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \qquad (4.25)
\end{aligned}$$

In each input sector, only the two line-line voltages with the lowest amplitudes are used. This is illustrated in the lower part of Fig. 4.15. By similar considerations the input current vectors can be calculated ($\underline{I}^\star_{gp} = \underline{I}_{g1} + \underline{I}_{g2}$):

$$\begin{aligned}
\underline{I}_{g1} &= |\underline{I}^\star_{gp}| \cdot \cos\left(\Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\
&= \delta_2 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot i_y \cdot \frac{2}{\sqrt{3}} \qquad (4.26) \\
\underline{I}_{g2} &= |\underline{I}^\star_{gp}| \cdot \cos\left(\frac{\pi}{3} - \Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\
&= \delta_1 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_3 \cdot i_y \cdot \frac{2}{\sqrt{3}} \qquad (4.27)
\end{aligned}$$

TABLE II: *Switching table for the modified space vector modulation.*

→Rec	Sector 0				Sector I				Sector II				Sector III				Sector IV				Sector V			
↓Inv	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4
0	acc	cbb	aac	ccb	bcc	abb	bbc	aab	baa	acc	bba	aac	caa	bcc	cca	bbc	cbb	baa	ccb	bba	abb	caa	aab	cca
I	aac	ccb	cac	bcb	bbc	aab	cbc	bab	bba	aac	aba	cac	cca	bbc	aca	cbc	ccb	bba	bcb	aba	aab	cca	bab	aca
II	cac	bcb	caa	bcc	cbc	bab	cbb	baa	aba	cac	abb	caa	aca	cbc	acc	cbb	bcb	aba	bcc	abb	bab	aca	baa	acc
III	caa	bcc	cca	bbc	cbb	baa	ccb	bba	abb	caa	aab	cca	acc	cbb	aac	ccb	bcc	abb	bbc	aab	baa	acc	bba	aac
IV	cca	bbc	aca	cbc	ccb	bba	bcb	aba	aab	cca	bab	aca	aac	ccb	cac	bcb	bbc	aab	cbc	bab	bba	aac	aba	cac
V	aca	cbc	acc	cbb	bcb	aba	bcc	abb	bab	aca	baa	acc	cac	bcb	caa	bcc	cbc	bab	cbb	baa	aba	cac	abb	caa

where i_x and i_y are the instantaneous value of a rotor phase current. By use of the relationship in eq. (4.17) and then separating eq. (4.26) into rotor current position independent expressions gives:

$$0 = \delta_2 \cdot \cos\left(\frac{\pi}{3} - \Delta_g\right) - \delta_1 \cdot \cos\left(\Delta_g\right) \tag{4.28}$$

$$0 = \delta_3 \cdot \cos\left(\Delta_g\right) - \delta_4 \cdot \cos\left(\frac{\pi}{3} - \Delta_g\right) \tag{4.29}$$

Solving the equations (4.24), (4.25), (4.28) and (4.29) for the modulation functions $\delta_{1..4}$:

$$\begin{aligned}
\delta_1 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\
\delta_2 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\Delta_g\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\
\delta_3 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\Delta_r\right) \\
\delta_4 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\Delta_g\right) \cdot \sin\left(\Delta_r\right) \\
\delta_0 &= 1 - (\delta_1 + \delta_2 + \delta_3 + \delta_4)
\end{aligned} \tag{4.30}$$

Also for the modified space vector modulation approach is should be noted that the modulation functions at any time instant are limited by the following constraint:

$$\delta_{0..4} >= 0$$

Taking this constraint into account, it is found that the maximum reference voltage $|V^{\star}_{rp}|$ are limited to half the input voltage. Table II summarizes the sector dependent switch combinations for each of the four active duty-cycle functions. The sectors in table II refers to the sector location in Fig. 4.15. The modified space vector approach were presented in the paper entitled *A novel loss reduced modulation strategy matrix converters* [27], c.f. Appendix D on page 335.

4.3.4 Modulation index

When comparing different modulation strategies for one type of converter, it is often convenient to normalize the output voltage to some reference voltage. This normalized voltage is named *Modulation index* M. The choice of reference voltage can be arbitrary and in the literature different choices exits which leads to some confusion. In this context however, the choice of reference voltage are to be done in accordance with the choice of modulation index definition for the other converters in order to be able to compare the different modulation methods for the different converters. Hence the modulation index for the matrix converter will be defined to be unity at the boundary between the linear and non-linear modulation region for the conventional space vector modulation. From eq. (4.21), the modulation index for the matrix converter becomes:

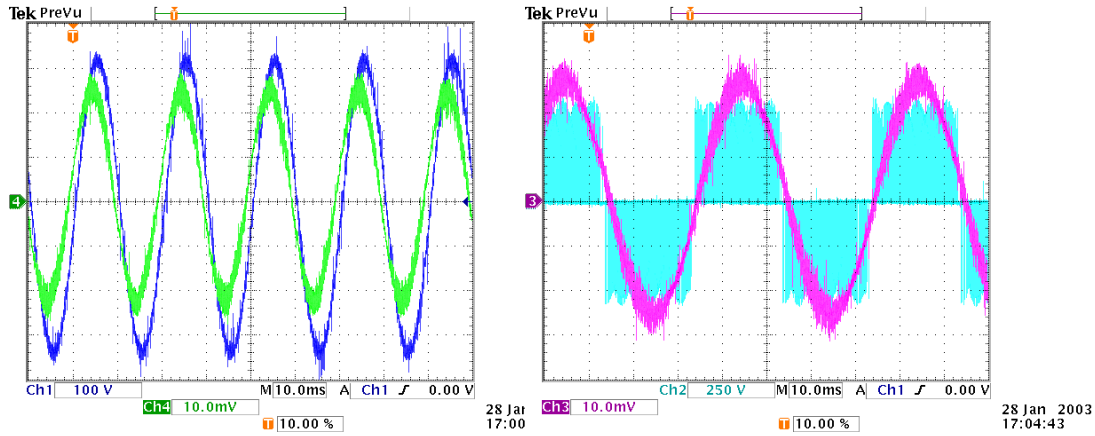
$$M = \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\widehat{\underline{V}}_{rp}|} \tag{4.31}$$

Further, for comparison, the input voltage of the matrix converter are to be designed such, that a given modulation index for the different converters correspond to the same rotor voltage.

4.3.5 Vector sequences

Like the modulation of the back-to-back voltage source converter, the vector sequences and the placement of the zero vectors have a high influence on the performance, efficiency and common-mode voltage generation of the matrix converter [16]. In the first papers concerning space vector modulation, single-sided modulation was used [9], but at the expense of only a slight increase in the number of branch switch over (BSO) per switching period, double sided modulation has become the prevalent method although a few recent papers [39, 38] have re-introduced the single sided modulation sequence. In double-sided modulation, the switching period is divided in two equal periods and in both these periods the four selected active vectors are applied. In the last of the two periods, the sequence order is reversed. The zero-vectors can be applied anywhere in the switching sequence. Due to the better harmonic performance at the grid side and at the rotor side, only double sided modulation is considered in this thesis. Specific, the following five double-sided modulation strategies will be treated:

- Conventional double sided modulation (8 BSO).
- Double sided modulation for the modified space-vector algorithm (8 BSO).
- Conventional double sided modulation with distributed zero vectors (10 BSO).
- Low distortion modulation method (8 BSO).
- Double sided modulation with distributed zero vectors for the modified space vector algorithm (10 BSO).



a) b)

Figure 4.16: *Measured waveforms for the conventional 8 BSO scheme. Left: Input current and input voltage. Right: Output current and output voltage.*

Conventional double sided modulation

In the conventional modulation presented in [47] the switching sequence for the conventional modulation was optimized with regards to the BSOs per switching fundamental, giving a minimum number of 8 BSO. Following this switching procedure, there is still one degree of freedom left and that is the position of the zero-vector within the switching sequence. The zero vector could either be applied in the beginning of the sequence or in the center of the sequence. Regarding the converter efficiency, the switched voltage when changing to/from the zero-vector can be used to determine the zero-vector placement, c.f. the lower part of Fig. 4.14. Hence, for even sector sums, the half of the switching sequence is:

$$\delta_0 \xrightarrow[v_{ab}]{i_C} \delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \qquad \text{when} \quad \Delta_g < \frac{\pi}{6} \tag{4.32}$$

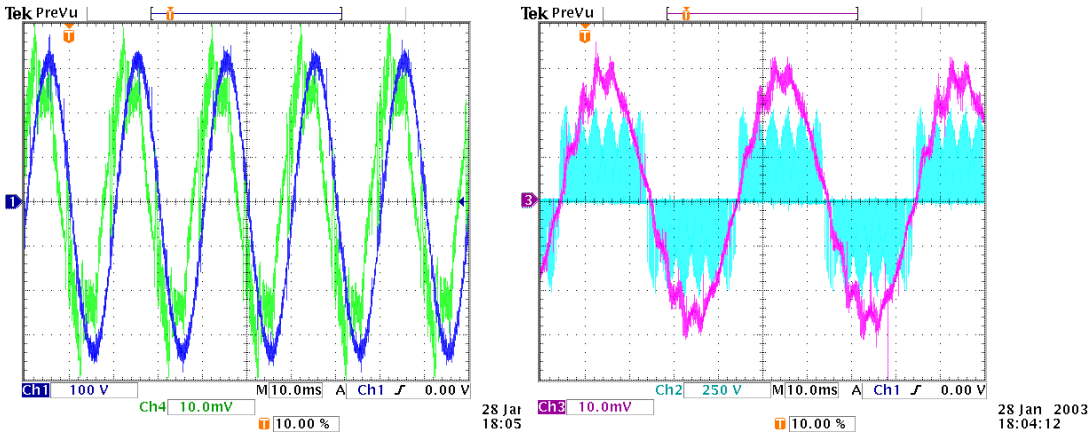
$$\delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \xrightarrow[v_{bc}]{i_C} \delta_0 \qquad \text{when} \quad \Delta_g > \frac{\pi}{6} \tag{4.33}$$

and for odd sector sums, the half of the switching sequence is:

$$\delta_0 \xrightarrow[v_{ca}]{i_A} \delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \qquad \text{when} \quad \Delta_g < \frac{\pi}{6} \tag{4.34}$$

$$\delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \xrightarrow[v_{ab}]{i_A} \delta_0 \qquad \text{when} \quad \Delta_g > \frac{\pi}{6} \tag{4.35}$$

For each BSO in eq. (4.32) to eq. (4.35) the switched current and the switched line-line voltage are shown, valid for sector 0_{rec}-0_{inv} and $I_{rec} - 0_{inv}$ respectively. By use of table I on page 106, the switched voltages and switched currents for an arbitrary sector location can be determined. This will be used when evaluating the switching losses of the different modulation methods. Fig. 4.16 show the measured current and voltage waveforms when using the conventional 8 BSO modulation method.



a) b)

Figure 4.17: *Measured waveforms for the modified 8 BSO scheme. Left: Input current and input voltage. Right: Output current and output voltage.*

Modified double sided modulation

By inspection of Table II it appears that the switching sequences of the modified modulation strategy are to be changed in order to obtain the minimum of 8 BSOs per switching fundamental. Hence, for even sector sums, the half of the switching sequence should be:

$$\delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \tag{4.36}$$

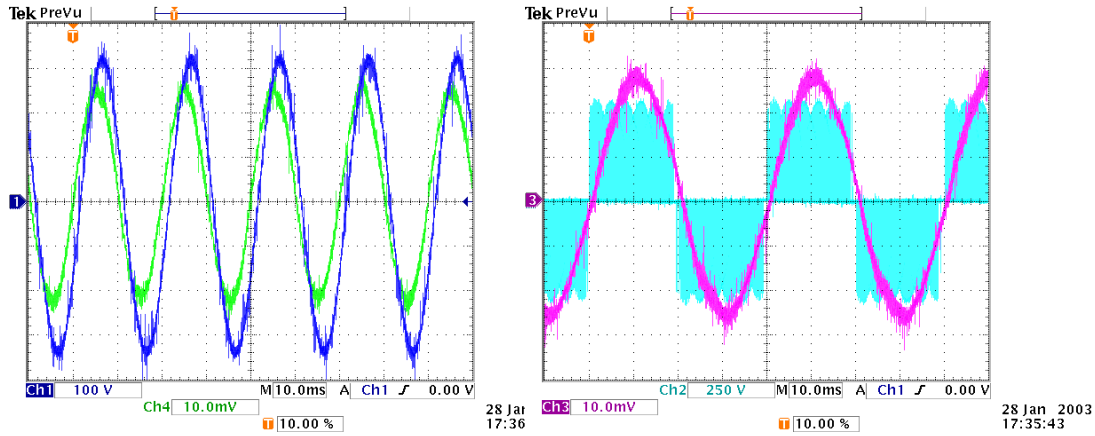
which assures 8 BSOs per switching fundamental. For odd sector sums, the half of the switching sequence should be:

$$\delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \tag{4.37}$$

Compared to the conventional method it appears that only the two minimum line-line voltages are switched which presumably decreases the switching losses. The switched currents and voltages listed in eq. (4.36) and eq. (4.37) are valid for sector 0_{rec}-0_{inv} and $I_{rec}-0_{inv}$ respectively. By use of table II on page 108 the switched voltages and currents can be determined for an arbitrary sector location of the rotor reference vector and the grid current vector. Fig. 4.17 shows the measured current and voltage waveforms when using the modified 8 BSO modulation method.

Conventional double sided modulation with distributed zero vectors

The third method to be treated takes advantages of that the switching sequence can be used to increase the switching frequency seen from the grid side, which is advantageous when considering the input filter design. However, this is achieved at the expense of a



a) b)

Figure 4.18: *Measured waveforms for the conventional 10 BSO scheme. Left: Input current and input voltage. Right: Output current and output voltage.*

higher number of BSOs per switching fundamental. In [41] different distributions of the zero vector were discussed and it was concluded that the most significant improvements are obtained by distributing the zero-vector at the beginning and in the center of the switching sequence. By this, the dominant switching frequency seen from the grid side is doubled at the expense of only two additional switchings per switching fundamental. With the constraint of only one BSO per switch-state shift, there is no degree of freedom left in the order of the switching sequence. According to [41], the half of the switching sequence for even sector sums is:

$$\delta_0 \xrightarrow[v_{ab}]{i_C} \delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \xrightarrow[v_{bc}]{i_C} \delta_0 \tag{4.38}$$

And for odd sector sums:

$$\delta_0 \xrightarrow[v_{ca}]{i_A} \delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \xrightarrow[v_{ab}]{i_A} \delta_0 \tag{4.39}$$

The switched currents and voltages listed in eq. (4.38) and eq. (4.39) are valid for sector 0_{rec}-0_{inv} and $I_{rec} - 0_{inv}$ respectively. Fig. 4.18 shows the measured current and voltage waveforms when using the conventional 10 BSO modulation method.

Low distortion modulation method

Inspired from the method proposed in [41] where the use of additional zero vectors were used to reduce the harmonic content, the "Low distortion modulation method" was developed [43]. Besides adding additional zero vectors, the proposed method aims to reduce the number of switchings per switching period from 10 to 8. For even sector sums, the half of the switching sequence should be realized by:

$$\delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ab}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \tag{4.40}$$

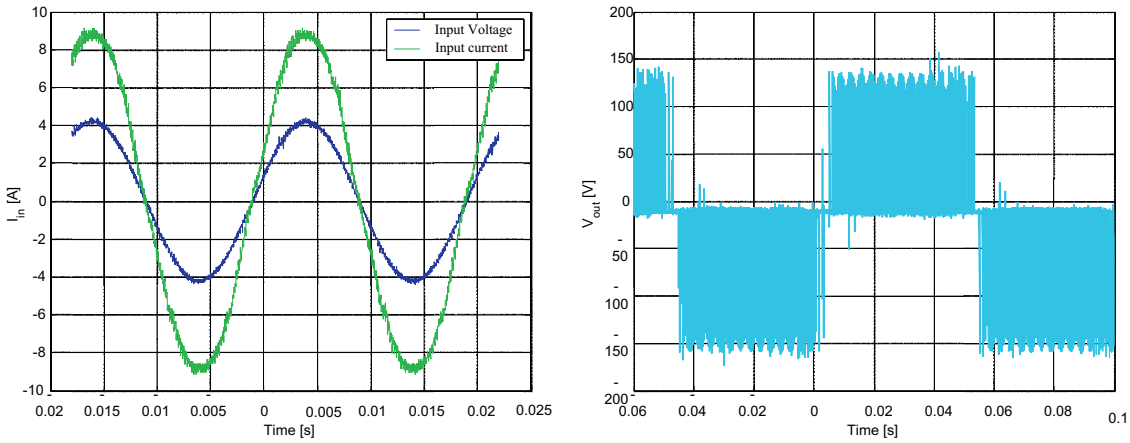


Figure 4.19: *Measured waveforms for the low distortion modulation scheme [43].*

and for odd sector sums, the half of the switching sequence is:

$$\delta_1 \xrightarrow[v_{ab}]{i_A} \delta_3 \xrightarrow[v_{ab}]{i_B} \delta_0 \xrightarrow[v_{bc}]{i_B} \delta_4 \xrightarrow[v_{bc}]{i_A} \delta_2 \tag{4.41}$$

The switched currents and voltages listed in eq. (4.40) and eq. (4.41) are valid for sector 0_{rec}-0_{inv} and $I_{rec} - 0_{inv}$ respectively. Fig. 4.19 shows the measured current and voltage waveforms when using the low distortion modulation method. The distortion approach were presented in the paper entitled *Analysis of Symmetrical Pulse Width Modulation Strategies for Matrix Converters* [43], c.f. Appendix I on page 383.

Double sided modulation with distributed zero vectors for the modified space vector algorithm

Adopting the method from [41] for use in the modified modulation approach is not as simple as for the conventional modulation due to a higher degree of freedom in the order of the switching sequence. According to the sequences in eq. (4.36) and eq. (4.37) the zero-vector could be applied in either the beginning of the sequence or in the center of the sequence. In order to explain the differences in the zero-vector placement, the half of the switching sequence for sector 0_{rec}-0_{inv} is listed in eq. (4.42) where the optional zero-vector placement is marked with the red and green δ_0 respectively.

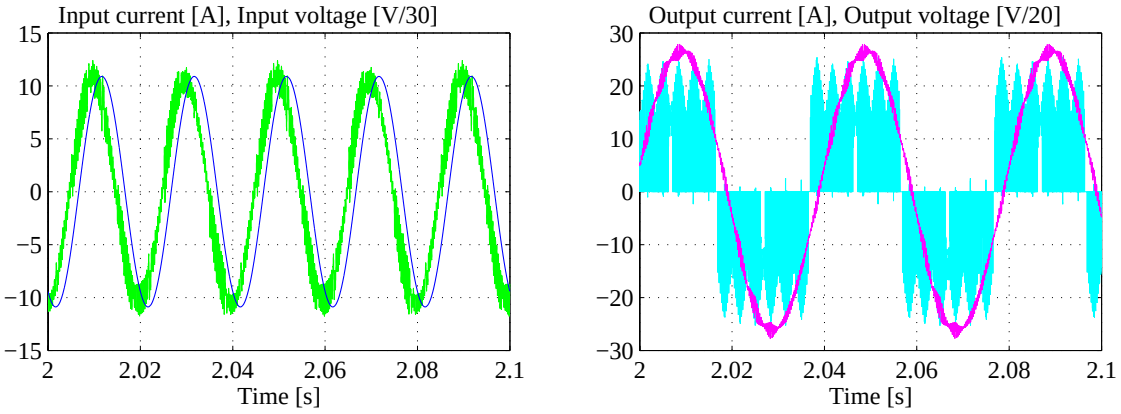
$$\delta_0 \xrightarrow[v_{ca}]{i_C} \delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \xrightarrow[v_{bc}]{i_A} \delta_0 \tag{4.42}$$

From eq. (4.42) it appears that the positioning of the zero-vector can be done either with regard to the switched current or with regard to the switched voltage.

Switched voltage: Regarding the switched voltage, it appears from the lower part of Fig. 4.15 on page 107 that the half of the switching sequence for even sectors should be:

$$\delta_0 \xrightarrow[v_{ca}]{i_C} \delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \qquad \text{when} \quad \Delta_g < \frac{\pi}{6} \tag{4.43}$$

$$\delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \xrightarrow[v_{bc}]{i_A} \delta_0 \qquad \text{when} \quad \Delta_g > \frac{\pi}{6} \tag{4.44}$$



a) b)

Figure 4.20: *Simulated current and voltage waveforms when using the modified modulation with distributed zero-vectors (SV). Left: Input current and input voltage. Right: Output current and output voltage.*

in order to assure that the lowest voltage is switched when applying the zero-vector. For odd sectors, the sequence should be:

$$\delta_0 \xrightarrow[v_{bc}]{i_A} \delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \qquad \text{when} \quad \Delta_g < \frac{\pi}{6} \tag{4.45}$$

$$\delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \xrightarrow[v_{ab}]{i_C} \delta_0 \qquad \text{when} \quad \Delta_g > \frac{\pi}{6} \tag{4.46}$$

The modulation method described by the sequences in eq. (4.43) - eq. (4.46) are in the further denoted *modified modulation with distributed zero-vectors (SV)*, where the abbreviation *SV* indicates that the modulation regards the switched voltage. Fig. 4.20 shows the simulated current and voltage waveforms when using the modified modulation with distributed zero-vectors (SV).

Switched Current: Regarding the switched current, the modified modulation with distributed zero-vectors can adopt some of the features from the discontinuous modulation strategies of the conventional voltage source inverter, c.f. section 3.3.3 on page 53. In other words, the placement of the zero-vector can be determined such that the minimum current is switched. By this, the optional placement of the zero-vector becomes dependent of the angle ϕ_r between rotor current and rotor voltage. This is illustrated in Fig. 4.21. Fig. 4.21 shows the rotor current and rotor phase voltage space vector diagram. For illustration purposes, the rotor voltage reference vector $\underline{V}^{\star}_{rp}$ is located in sector 0 and the angle between the rotor voltage reference and the rotor current is ϕ_r. In order to assure that the minimum rotor current is switched when switching to/from the zero-vector, the switching sequence in eq. (4.42) should be altered between the *red* and *green sequence* in accordance with the rotor current position in Fig. 4.21.

Generalizing to an arbitrary sector location of the rotor voltage vector the half of the

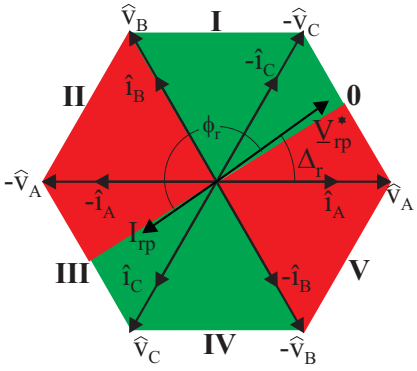


Figure 4.21: *Rotor current and rotor voltage space vector diagram.*

vector sequence for even sectors sums becomes:

$$\delta_0 \xrightarrow[v_{ca}]{i_C} \delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \quad \text{when} \quad \begin{cases} -\frac{\pi}{3} & < (\Delta_r + \phi_r) < \frac{\pi}{6} \\ \frac{2\pi}{3} & < (\Delta_r + \phi_r) < \frac{7\pi}{6} \end{cases} \tag{4.47}$$

$$\delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \xrightarrow[v_{bc}]{i_A} \delta_0 \quad \text{when} \quad \begin{cases} \frac{\pi}{6} & < (\Delta_r + \phi_r) < \frac{2\pi}{3} \\ \frac{7\pi}{6} & < (\Delta_r + \phi_r) < \frac{5\pi}{3} \end{cases} \tag{4.48}$$

and for odd sector sums the switching sequence becomes:

$$\delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \xrightarrow[v_{ab}]{i_C} \delta_0 \quad \text{when} \quad \begin{cases} -\frac{\pi}{3} & < (\Delta_r + \phi_r) < \frac{\pi}{6} \\ \frac{2\pi}{3} & < (\Delta_r + \phi_r) < \frac{7\pi}{6} \end{cases} \tag{4.49}$$

$$\delta_0 \xrightarrow[v_{bc}]{i_A} \delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \quad \text{when} \quad \begin{cases} \frac{\pi}{6} & < (\Delta_r + \phi_r) < \frac{2\pi}{3} \\ \frac{7\pi}{6} & < (\Delta_r + \phi_r) < \frac{5\pi}{3} \end{cases} \tag{4.50}$$

Following the switching sequences in eq. (4.47) - eq. (4.50), the modulator need information about the instantaneous angle between rotor voltage and rotor current. However, it is easily realized, that the angle ϕ_r can be pre-set to a fixed value representing the steady-state nominal value of the load angle.

The modulation method described by the sequences in eq. (4.47) - eq. (4.50) are in the further denoted *modified modulation with distributed zero-vectors (SC)*, where the abbreviation *SC* indicates that the modulation regards the switched current.

4.3.6 Evaluation of modulation methods

An evaluation of the modulation methods for the matrix converter has to consider both the quality of the generated generator voltage and the quality of the generated input current. An evaluation of the generated generator voltage is directly comparable with the voltage generated by the two-level inverter treated in chapter 3 and the three-level inverter to be treated in chapter 5 whereas an evaluation of the generated input current quality is only suitable for an internal comparison of the matrix converter modulation methods and can be used as a hint for determining the filter requirements and/or switching frequency requirements associated with the different modulation methods.

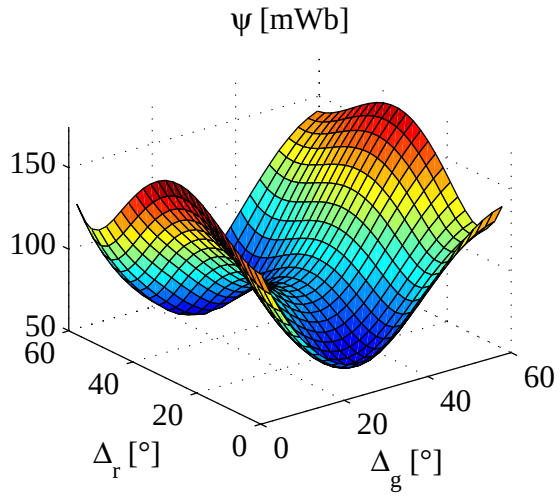


Figure 4.22: *The per-carrier cycle RMS value of the harmonic flux as a function of the input and output angle for the conventional modulation strategy.*

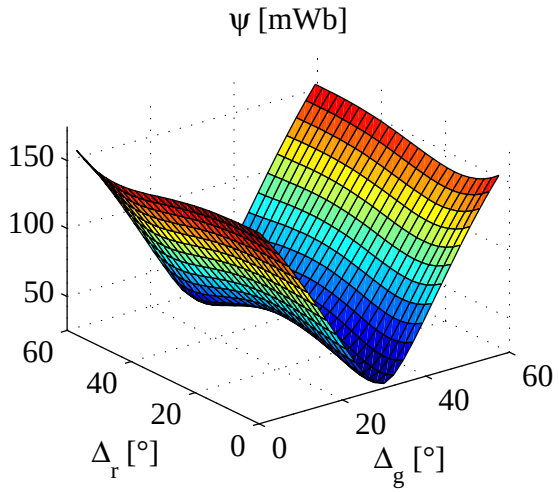


Figure 4.23: *The per-carrier cycle RMS value of the harmonic flux as a function of the input and output angle for the modified modulation strategy.*

Generator side harmonic performance

To evaluate the output voltage quality, the harmonic flux is considered [25]. In the N$^{\text{th}}$ carrier cycle the harmonic flux $\tilde{\psi}$ is calculated by:

$$\tilde{\psi} = \int_{NT_s}^{(N+1)T_s} (\underline{V}_{rp} - \underline{V}^{\star}_{rp}) dt \tag{4.51}$$

where $\underline{V}_{rp}$ is a stationary output vector. To be able to compare the different modulators for the different converters, the per carrier harmonic flux error $\tilde{\psi}$ in eq. (4.51),is normalized to the product of the maximum rotor voltage amplitude $|\underline{\hat{V}}_{rp}|$ and the switching period. That is:

$$\tilde{\psi}_n = \frac{2}{\sqrt{3} T_s |\underline{\hat{V}}_{rp}|} \cdot \tilde{\psi} \tag{4.52}$$

The normalized per-carrier cycle RMS value of the harmonic flux $\tilde{\psi}_{RMS,n}$ can be calculated by:

$$\langle \tilde{\psi}_{RMS,n} \rangle_{T_s} = \sqrt{\int_0^1 \left(\tilde{\psi}_n \cdot \tilde{\psi}_n^* \right) dt} \tag{4.53}$$

where $\tilde{\psi}_n^*$ is the complex conjugate of $\tilde{\psi}_n$. Fig. 4.22 and Fig. 4.23 shows the per-carrier cycle RMS value of the harmonic flux as a function of the input angle and the output angle. The figures are valid for conventional double sided modulation and the modified double sided modulation and are plotted for modulation indexes of 1 and 0.577 respectively. Evaluating for a general case, where input frequency and the output frequency has no common period time, the RMS value of the harmonic flux is obtained

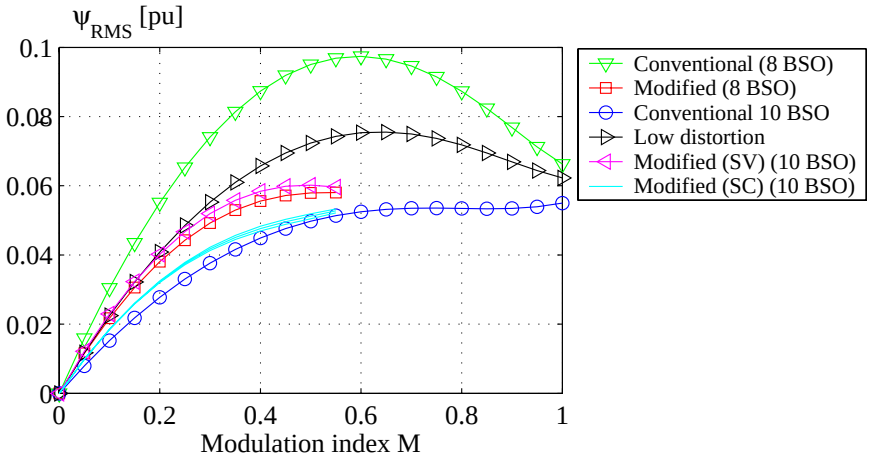


Figure 4.24: *The harmonic flux as a function of the modulation index, c.f. eq. (4.31)*

by integrating over the entire surface. The RMS value of the harmonic flux is calculated by:

$$\tilde{\psi}_{RMS,n} = \sqrt{\frac{9}{\pi^2}\int_0^{\frac{\pi}{3}}\int_0^{\frac{\pi}{3}}\left(\langle\tilde{\psi}_{RMS,n}\rangle_{T_s}\right)^2 d\Delta_g\, d\Delta_r} \tag{4.54}$$

Fig. 4.24 shows the RMS-value of the harmonic flux as a function of the modulation index. From Fig. 4.24 it appears that the conventional double sided modulation with distributed zero vectors shows the best output harmonic performance in the entire linear modulation range. The harmonic flux curves in Fig. 4.24 are directly comparable to the harmonic flux levels calculated for the two-level inverter, c.f. Fig. 3.11 on page 59. Finally, it should be noted that for $\cos(\phi_i) \neq 1$ at the input, all the curves in Fig. 4.24 would be changed.

Grid side harmonic performance

In principle, the evaluation of the input current follows the same procedure as for the output voltage, however the evaluation parameter is changed from harmonic flux to harmonic charge $\tilde{Q}$. Further, the evaluation of the input current becomes a little more complex than the evaluation of the output voltage due to the fact that the amplitudes of the stationary input current vectors are affected by the load angle ($\cos(\phi_r)$). Fig. 4.25 shows the normalized harmonic charge $\tilde{Q}_{RMS}$ vs. the modulation index M. In the calculation of the results in Fig. 4.25 the harmonic charge $\tilde{Q}$ is normalized by $\frac{T_s}{2}\frac{\sqrt{3}\hat{i}_r}{2}$.

The paper entitled *Evaluation of Modulation Schemes for Three-phase to Three-phase Matrix Converters* [26] provides a thorough explanation of the evaluation method discussed in this section along with a detailed comparison of selected modulation methods.

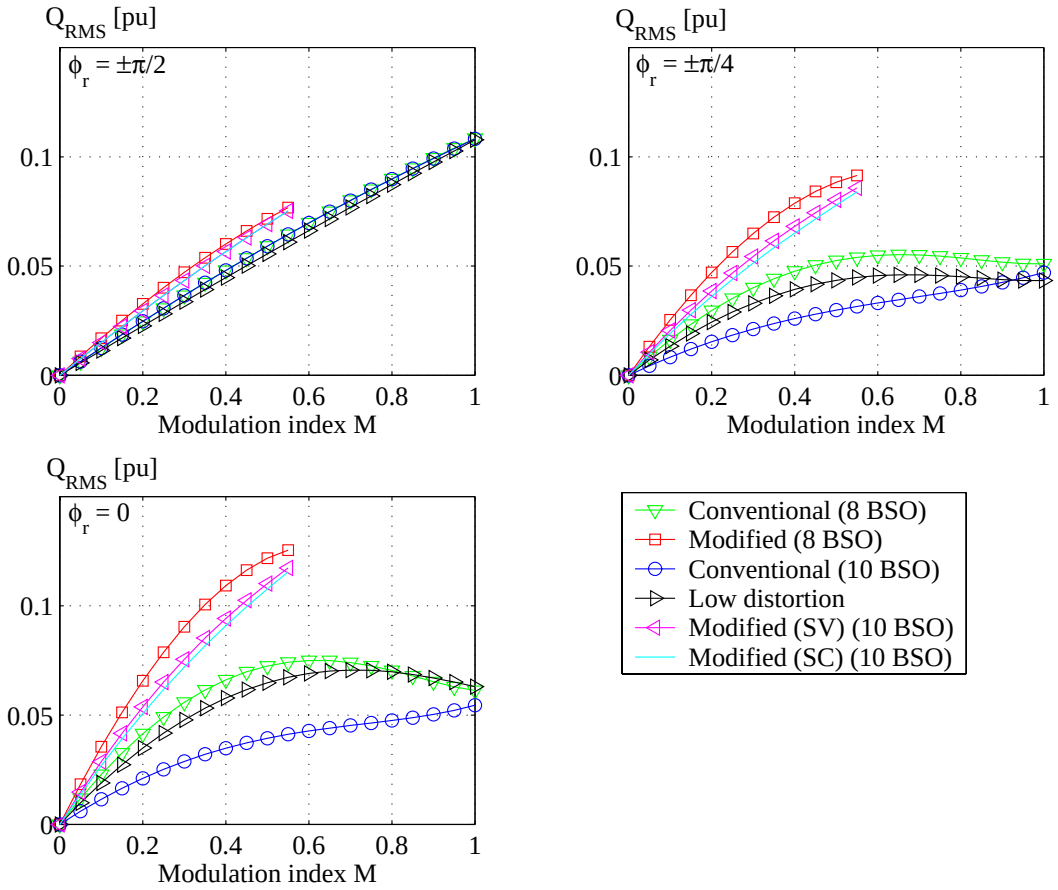


Figure 4.25: *The charge distortion as a function of the modulation index, c.f. eq. (4.31).*

4.4 Loss evaluation

With the purpose of obtaining a fast method for comparing the power losses generated by the matrix converter with the power losses generated by an alternative converter configuration, analytical expressions for the power losses within the matrix converter has to be derived. Considering the matrix converter, the power losses to be concerned with are the conducting losses and switching losses of the semiconductor devices as well as the losses dissipated by the input filter. As discussed in section 3.4.3, the temperature of the semiconductor devices has a significant influence on the generated losses and is crucial when evaluating a certain converter design. Hence the derivation of power losses has to take into consideration the temperature of the semiconductor devices. Hence, the purpose of this section is to derive analytical expressions for the losses generated by the matrix converter and based on these loss expressions to end up with some expressions relating the generated losses to the temperature of the semiconductor devices.

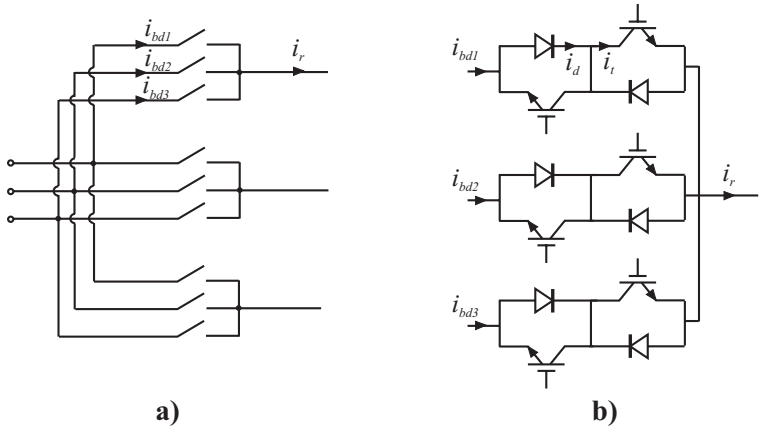


Figure 4.26: *Definition of the currents in the matrix converter.* **a)** *Current notation in the matrix converter.* **b)** *Current notation within a phase-leg of the matrix converter.*

4.4.1 Conducting losses of the switches

The conduction losses in the transistors and diodes of the matrix converter are approximated by:

$$P_{t,cond} = V_{t0}(T) \cdot I_{t,avg} + R_t(T) \cdot I_t^2 \tag{4.55}$$

$$P_{d,cond} = V_{d0}(T) \cdot I_{d,avg} + R_d(T) \cdot I_d^2 \tag{4.56}$$

where $I_{x,avg}$ is the average current through the considered component, I_x is the RMS current through the considered component, $V_{x0}(T)$ is the temperature dependent threshold voltage of the considered component and $R_{x0}(T)$ is the temperature dependent resistance of the considered component. The threshold voltage and on-resistance can either be found from data sheets or derived by the procedure described in Appendix A.

So far, every aspect treated for the matrix converter has seemed to be a little more complicated than for the previously considered back-to-back two-level voltage source converter. However, considering the derivation of the average- and RMS currents for the transistors and diodes within the matrix converter it turns out that these expressions are far more simple than the expressions derived in chapter 3 for the two-level inverter. Further, the expressions become independent of the modulation scheme and since the current through a diode at any time instant equals the current through a transistor, the following relations apply:

$$I_{d,avg} = I_{t,avg} \tag{4.57}$$

$$I_d = I_t \tag{4.58}$$

Fig. 4.26 defines the notation used when deriving the individual currents through the components. From eq. (4.57) and eq. (4.58) the only exercise left is to derive the expressions for the average- and RMS current through the transistor. The average

current $I_{bd,avg}$ through one of the bi-directional switches can be calculated by:

$$I_{bd,avg} = \frac{1}{T}\int_0^T i_{bd}dt \tag{4.59}$$

where T is a period time common for both the grid frequency and the rotor frequency. The output phase current i_r is at any instant of time the sum of the currents in an output leg. That is:

$$i_r = i_{bd1} + i_{bd2} + i_{bd3} \tag{4.60}$$

For symmetrical input and output conditions the average current through a switch cell can be calculated as [48]:

$$\begin{aligned} I_r &= \frac{\pi}{2\sqrt{2}}\sum_{x=1}^{3}\left(\frac{1}{T}\int_0^T i_{bd,x}dt\right) = \frac{3\pi}{2\sqrt{2}}\cdot I_{bd,avg} \\ &\Downarrow \\ I_{bd,avg} &= \frac{2\sqrt{2}}{3\pi}I_r \end{aligned} \tag{4.61}$$

Assuming that a bidirectional switch is realized as a full controllable bi-directional switch, c.f. Fig. 4.4b-d, the average current through the individual transistors is given by:

$$I_{t,avg} = \frac{\sqrt{2}}{3\pi}I_r \tag{4.62}$$

Considering the RMS current through one of the bi-directional switches, the same considerations apply:

$$I_{bd} = \sqrt{\frac{1}{T}\int_0^T i_{bd}^2 dt} \tag{4.63}$$

where T is a period time common for both the grid frequency and the rotor frequency. Using the information given by eq. (4.60), and assuming symmetrical input and output conditions the RMS current through a switch cell can be calculated as [48]:

$$\begin{aligned} I_r &= \sqrt{\sum_{x=1}^{3}\left(\frac{1}{T}\int_0^T i_{bd,x}^2 dt\right)} = \sqrt{3\cdot I_{bd}^2} \\ &\Downarrow \\ I_{bd} &= \frac{I_r}{\sqrt{3}} \end{aligned} \tag{4.64}$$

The RMS current through a transistor in a bi-directional switch realized by one of the configurations shown in Fig. 4.4b-d is then given by:

$$I_t = \frac{1}{\sqrt{6}}I_r \tag{4.65}$$

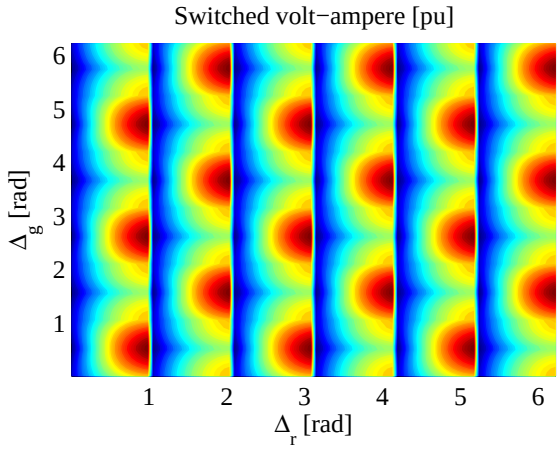


Figure 4.27: *Contour plot of the switching losses of the conventional modulation method for* $\phi_r = \pi/6$.

4.4.2 Switching losses

Assuming the switch devices of the matrix converter to have linear current and voltage turn-on and turn-off characteristics with respect to time and accounting only for the fundamental component of the rotor current, the per component switching energy dissipated by every hard commutated turn-on and turn-off[6] of the matrix converter can be analytically modeled as:

$$E_{sw,t} \propto |v_{sw}| \cdot |i_{sw}| \cdot E_{sw0,t}(T) \tag{4.66}$$

$$E_{sw,d} \propto |v_{sw}| \cdot |i_{sw}| \cdot E_{sw0,d}(T) \tag{4.67}$$

where $E_{t,sw0}$ is the sum of the per unit VA transistor turn-on and turn-off switching energy, $E_{d,sw0}$ is sum of the per unit VA diode turn on and turn off switching energy, v_{sw} is the instantaneous voltage switched by the considered component and i_{sw} is the instantaneous current switched by the considered component. The per unit VA switching energies can either be found from data sheets or derived by the procedure described in Appendix A. Since the switched current i_{sw} and switched voltage v_{sw} are un-correlated time varying functions, the exact average switching losses will depend on the specific working condition. To illustrate this *problem*, Fig. 4.27 shows the switched volt-amperes (hard-switched) as a function of the grid angle Δ_g and the rotor angle Δ_r when using the conventional double sided modulation. The switched volt-ampere surface in Fig. 4.27 is calculated for a rotor load angle of $\pi/6$. Clearly, from Fig. 4.27 it appears that the average switched volt-amperes depend on the actual course across the surface, i.e. input- and output frequency and the initial angle conditions. To avoid the need for initial angle conditions when calculating the average switched volt-amperes, a general case is assumed where the grid frequency and the rotor frequency have no common time period and hence the average switched volt-amperes can be calculated by integrating over the

[6]It appears that half of the switchings when using either the commutation procedure given in Fig. 4.5 or Fig. 4.6 are hard commutated while the latter switchings appear to be soft switchings.

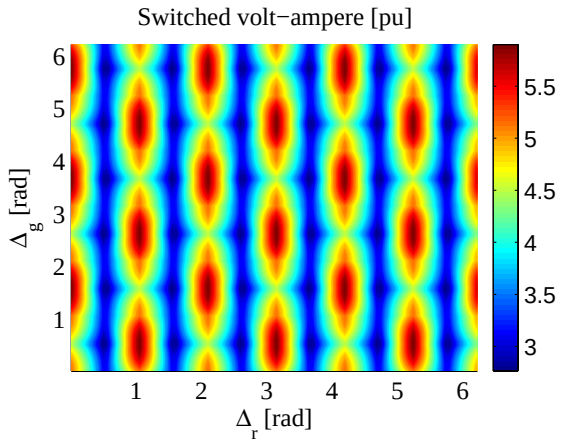


Figure 4.28: *Hard switched volt-amperes when using the conventional double sided modulation.*

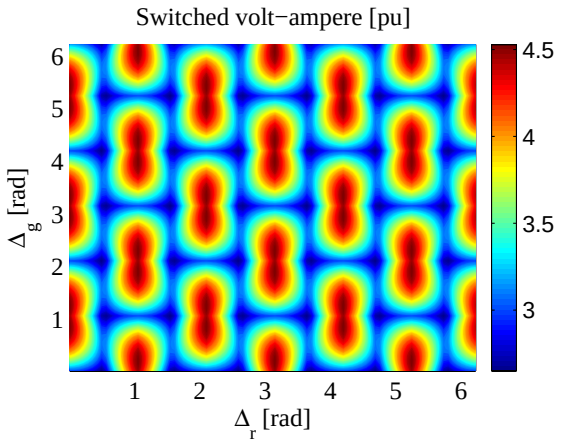


Figure 4.29: *Hard switched volt-amperes when using the modified double sided modulation.*

entire surface. Hence, to evaluate the different modulation methods with regards to the switching losses, the average switched volt-amperes will have to be calculated as a function of the rotor load angle[7]. The average switched volt-amperes $S_{sw,avg}$ can be calculated by:

$$S_{sw,avg} = \frac{1}{4\pi^2} \int_0^{2\pi} \int_0^{2\pi} (|u_{sw}| \cdot |i_{sw}|)\, d\Delta_g\, d\Delta_r \tag{4.68}$$

By use of eq. (4.68) analytical expressions for the average switching losses of the considered modulation method can be obtained:

$$P_{t,sw} = \frac{1}{18} S_{sw,avg} \cdot E_{sw0,t}(T) \cdot f_{sw} \tag{4.69}$$

$$P_{d,sw} = \frac{1}{18} S_{sw,avg} \cdot E_{sw0,d}(T) \cdot f_{sw} \tag{4.70}$$

where $P_{t,sw}$ is the average switching losses of a single transistor in the matrix converter and $P_{d,sw}$ is the average switching losses of a single diode in the matrix converter when the matrix converter is realized from 18 diodes and 18 transistors. Hence the only exercise left is to derive the analytical expressions for the average hard switched volt-amperes $S_{sw,avg}$.

Conventional double sided modulation

Considering the switching sequences of the conventional double sided modulation method as described on page 110, the hard switched volt-amperes can be calculated for every combination of input angle Δ_g and output angle Δ_r. Fig. 4.28 illustrates the switched volt-ampere surface when the load angle ϕ_r of the matrix converter is zero. Using the sequences given by eq. (4.32) - eq. (4.35) in combination with the information

[7]For simplicity, the input load angle is assumed to be unity.

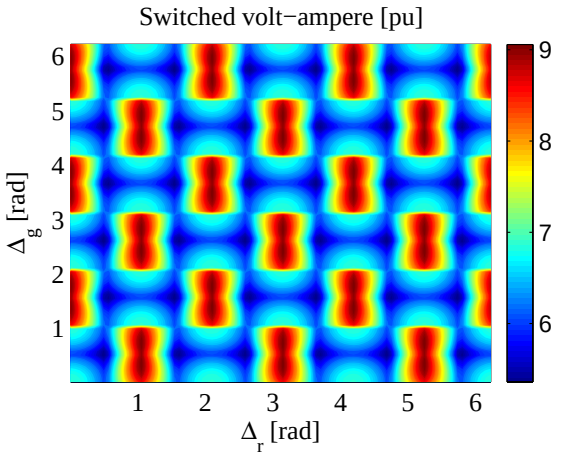


Figure 4.30: *Hard switched volt-amperes when using the conventional double sided modulation with distributed zero vectors.*

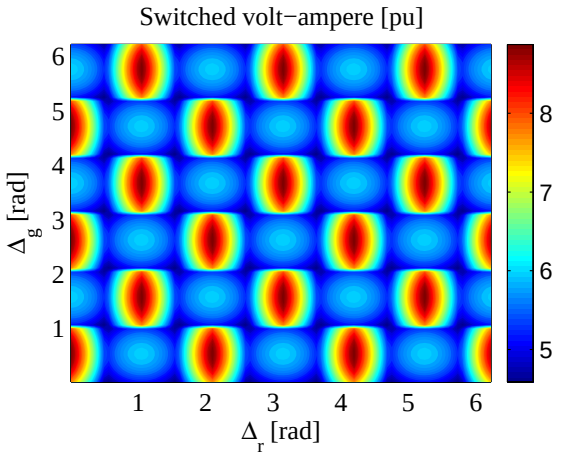


Figure 4.31: *Hard switched volt-amperes when using the low distortion modulation method.*

in Table I, analytical expression for the hard switched volt-amperes can be derived from eq. (4.68):

$$S_{sw,avg} = \begin{cases} 9\,\frac{\sqrt{3}\left(-6\,\cos(\phi_r)+\sqrt{3}\cos(\phi_r)+4\,\sqrt{3}\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| < \frac{\pi}{6} \\ 9\,\frac{\sqrt{3}\left(2-\sin(|\phi_r|)+2\,\sqrt{3}\sin(|\phi_r|)\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| \geq \frac{\pi}{6} \end{cases} \tag{4.71}$$

where V_{gp} is the RMS phase voltage at the input to the matrix converter and I_r is the RMS phase current at the output of the matrix converter.

Modified double sided modulation

Similarly, the hard-switched volt-amperes when using the modified double sided modulation method can be calculated. Fig. 4.29 shows an example of the hard switched volt-amperes as a function of the input angle Δ_g and output angle Δ_r when the load angle is zero. Evaluating eq. (4.68) with the sequences given by eq. (4.36) and eq. (4.37) in combination with the switch states in Table II, the analytical expressions for the hard switched volt-amperes $S_{sw,avg}$ when using the modified double sided modulation method can be derived:

$$S_{sw,avg} = \begin{cases} 9\,\frac{\sqrt{3}\left(4-\sqrt{3}\cos(\phi_r)\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| < \frac{\pi}{6} \\ 9\,\frac{\sqrt{3}\,(2+\sin(|\phi_r|))}{\pi^2} V_{gp}\cdot I_r & |\phi_r| \geq \frac{\pi}{6} \end{cases} \tag{4.72}$$

Conventional double sided modulation with distributed zero vectors

The conventional double sided modulation with distributed zero vectors added an additional zero-vector to the conventional double sided sequence whereby the number of

switchings per switching period was increased from 8 to 10, Hence it must be expected that the average switched volt-amperes will increase more or less correspondingly. Fig. 4.30 illustrates the hard-switched volt-amperes for a load angle of zero. Evaluating eq. (4.68) with the sequences given by eq. (4.38) and eq. (4.39) in combination with the switch states in Table I, the analytical expressions for the hard switched volt-amperes $S_{sw,avg}$ when using the conventional double sided modulation method with distributed zero vectors can be derived:

$$S_{sw,avg} = \begin{cases} 18\,\frac{\sqrt{3}\left(2\sqrt{3}+\sqrt{3}\cos(\phi_r)-3\,\cos(\phi_r)\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| < \frac{\pi}{6} \\ 18\,\frac{\sqrt{3}\left(\sqrt{3}\sin(|\phi_r|)+2-\sin(|\phi_r|)\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| \geq \frac{\pi}{6} \end{cases} \tag{4.73}$$

Low distortion modulation method

The idea of the low distortion modulation method was to improve the quality of the generated input current and output voltage by adding an additional zero-vector while still keeping the number of switchings per switching period at 8. Evaluating the switching sequence given by eq. (4.40) and eq. (4.41) with regard to the switched volt-amperes and with a load angle of zero, the surface in Fig. 4.31 is obtained. Averaging the surface in Fig. 4.31 by use of eq. (4.68) and calculating for arbitrary load angles, the following expression for the hard-switched volt-amperes is obtained:

$$S_{sw,avg} = \begin{cases} 9\,\frac{\sqrt{3}\left(-3\,\cos(\phi_r)+4\sqrt{3}\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| < \frac{\pi}{6} \\ 27\,\frac{(2+\sin(|\phi_r|))}{\pi^2} V_{gp}\cdot I_r & |\phi_r| \geq \frac{\pi}{6} \end{cases} \tag{4.74}$$

Double sided modulation with distributed zero vectors for modified space vector algorithm (SV)

Likewise, inspired from the conventional double sided modulation with distributed zero vectors, the harmonic content of the modified space-vector modulation approach was improved by adding an additional zero-vector to the switching sequence. As discussed in section 4.3.5 on page 113, the location of this additional zero-vector leave some degree of freedom and as discussed one way to choose the location is to look at the switched voltage associated with the location of the additional zero-vector and then select the location associated with the lowest switched voltage. This approach is given by the sequences in eq. (4.43) - eq. (4.46). Fig. 4.32 shows the hard switched volt-amperes as a function of the input angle Δ_g and output angle Δ_r when the load-angle is zero. Calculating the hard switched volt-amperes for arbitrary values of the load angle and evaluating the average switched volt-amperes by use of eq. (4.68) the following expression is obtained:

$$S_{sw,avg} = \begin{cases} 9\,\frac{\sqrt{3}\left(4+\sqrt{3}\cos(\phi_r)-3\,\cos(\phi_r)\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| < \frac{\pi}{6} \\ 9\,\frac{\sqrt{3}\left(6-2\sqrt{3}+\sqrt{3}\sin(|\phi_r|)-\sin(|\phi_r|)\right)}{\pi^2} V_{gp}\cdot I_r & |\phi_r| \geq \frac{\pi}{6} \end{cases} \tag{4.75}$$

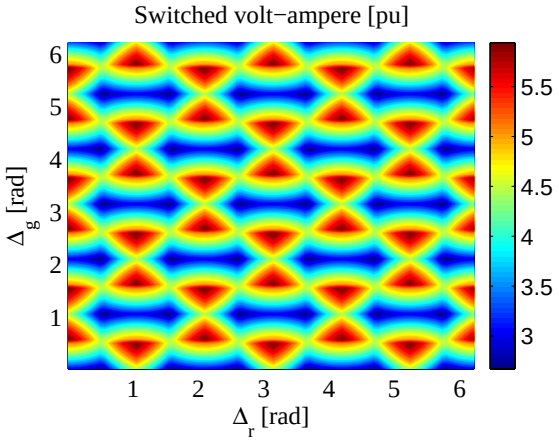


Figure 4.32: *Hard switched volt-amperes when using the double sided modulation with distributed zero vectors for modified space vector algorithm (SV).*

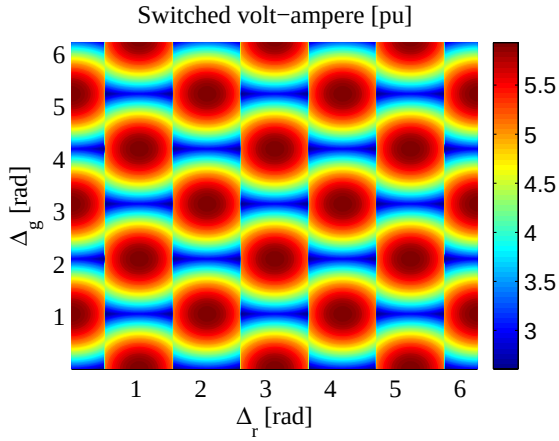


Figure 4.33: *Hard switched volt-amperes when using the double sided modulation with distributed zero vectors for modified space vector algorithm (SC).*

Double sided modulation with distributed zero vectors for modified space vector algorithm (SC)

Finally, considering the double sided modulation with distributed zero vectors for the modified space vector algorithm where the switching sequence is chosen in order to minimize the switched current, the switched volt-ampere surface for a load angle of zero will appear as illustrated in Fig. 4.33. Evaluating eq. (4.68) on the sequences given in eq. (4.47)- eq. (4.50) in combination with Table II the following expression for the hard switched volt-amperes is obtained:

$$S_{sw,avg} = \begin{cases} 27\,\frac{\sqrt{3}}{\pi^2} V_{gp} \cdot I_r & |\phi_r| \leq \frac{\pi}{6} \\ \frac{9}{2}\,\frac{\sqrt{3}\left(8-\sqrt{3}\cos(\phi_r)-\sin(|\phi_r|)\right)}{\pi^2} V_{gp} \cdot I_r & \frac{\pi}{6} < |\phi_r| \leq \frac{\pi}{3} \\ 9\,\frac{\sqrt{3}\left(4+\sin(|\phi_r|)-\sqrt{3}\right)}{\pi^2} V_{gp} \cdot I_r & |\phi_r| \geq \frac{\pi}{3} \end{cases} \tag{4.76}$$

By use of eq. (4.71)- eq. (4.76) the average hard switched volt-amperes (switched by the entire matrix converter) can be calculated and hence a measure of the switching losses associated with the different modulation methods can be obtained. Fig. 4.34 shows the hard switched volt-amperes as a function of the load angle ϕ_r evaluated for the different modulation methods.

4.4.3 Thermal modeling

The thermal modeling for calculating the temperature of the switches in the matrix converter very much depend on the switch configuration, c.f. Fig. 4.4. In the following, it is assumed that a bi-directional switch is realized from a standard H-bridge module as illustrated in Fig. 4.4d. The purpose of the thermal model of the matrix converter

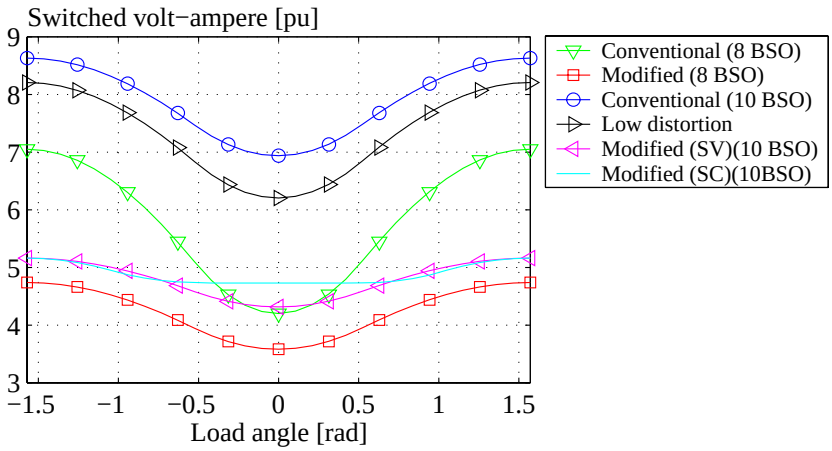


Figure 4.34: *The switching losses of the four different modulation functions for the matrix converter.*

is to calculate the diode and transistor average temperature in order to determine the temperature dependent component resistances and threshold voltages. To validate a certain matrix converter design, a secondary purpose of the thermal modeling is to be able to calculate the component peak temperature for a given load condition.

Fig. 4.35a illustrates a simple one dimensional approach to calculate the junction temperature of the semiconductor components in a full bridge module where the component notation follows the notation given in Fig. 4.35c. Each of the semiconductor power losses are modeled as a current source feeding into a thermal impedance denoted by Z_{thxx}. As illustrated in Fig. 4.35b, the thermal impedances can be composed of one or more parallel connected RC-elements. The temperature source $k \cdot T_{xx}$ represents a thermal coupling from other transistors and diodes and the temperature source T_{amb} makes it possible to offset the temperature estimation by the ambient temperature. Based on the thermal modeling approach in Fig. 4.35 the goal is to derive a method which enables estimation of the average and peak junction temperatures, only with information on the modulation dependent semiconductor losses calculated in section 4.4 and the thermal parameters in Fig. 4.35.

Average temperatures

Neglecting the thermal coupling between the components in the half bridge module, the average temperature of the individual components can simply be calculated by:

$$T_{tx} = P_{tx} \cdot \sum_{w=1}^{y} R_{thxw,t} + 4 \cdot (P_{tx} + P_{dx}) \cdot (R_{thch} + R_{thha}) + T_{amb} \tag{4.77}$$

$$T_{dx} = P_{dx} \cdot \sum_{w=1}^{y} R_{thxw,d} + 4 \cdot (P_{tx} + P_{dx}) \cdot (R_{thch} + R_{thha}) + T_{amb} \tag{4.78}$$

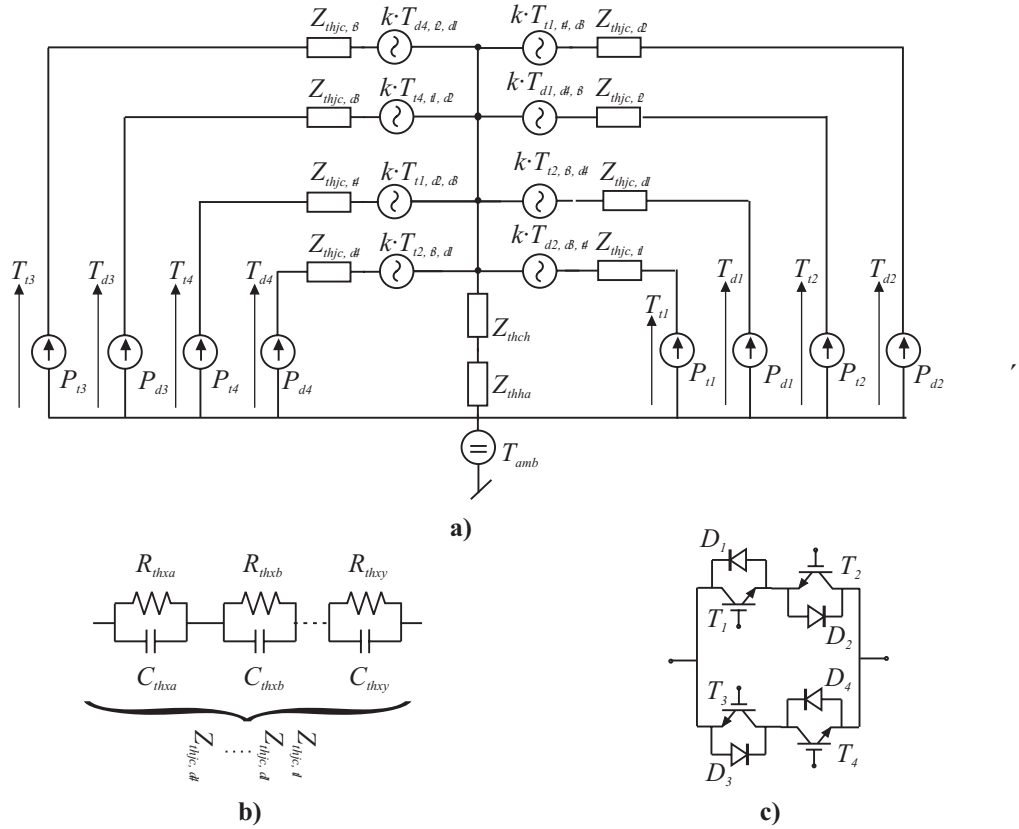


Figure 4.35: *Illustration of the simple thermal models used to estimate switch temperatures.* **a)** *Thermal model of a half bridge module.* **b)** *model of a thermal impedance Z_{th}.* **c)** *Component name notation.*

where T_{tx} is the average transistor temperature, T_{dx} is the average diode temperature, $R_{thxx,x}$ is the thermal resistances in the thermal model in Fig. 4.35 and P_{tx} and P_{dx} are the average transistor and diode losses derived form eq. (4.55), eq. (4.56), eq. (4.69) and eq. (4.70).

Peak temperatures

Estimation of the peak temperatures in the matrix converter is a little more complex than for the two-level converter treated in chapter 3. Actually, as the peak power loss experienced by the individual components depend on the input and output frequency, an exact prediction of the peak temperatures is not possible. For instance, Fig. 4.36 illustrates an example of the per switching period switched volt-amperes experienced by a transistor (or diode) in switch[8] S_{a1} when the load angle is $\pi/6$ and the switches are controlled according to the conventional 8 BSO modulation method. Correspondingly, Fig. 4.37 shows the per switching period RMS current through a transistor (or diode) in switch S_{a1}.

[8]The switch notation refer to the notation used in Fig. 4.5 on page 95.

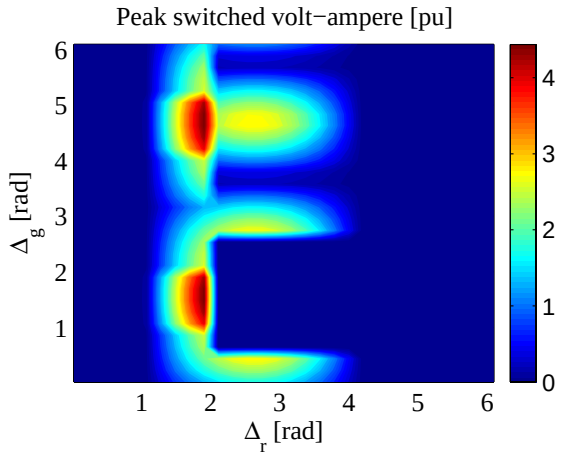


Figure 4.36: *The per switching period switched volt-amperes experienced by switch S_{a1} when the load angle is $\pi/6$ and the switches are controlled according to the conventional 8 BSO modulation method.*

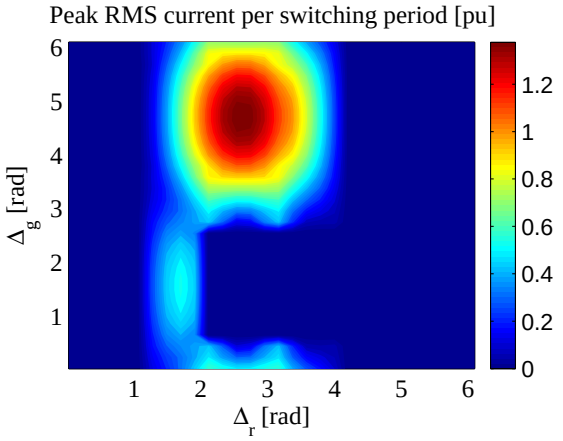


Figure 4.37: *the per switching period RMS current through switch S_{a1} when the load angle is $\pi/6$ and the switches are controlled according to the conventional 8 BSO modulation method.*

Besides the fact that the peak power losses experienced by one of the switches in the matrix converter depend on the actual course across the surface in Fig. 4.36 and Fig. 4.37 it appears that the peak of the switched volt-amperes and the peak of the conducted current are not necessarily located in the same position and furthermore, the locations are moving, depending on the load angle. Finally, it appears that for some of the modulation methods, the peak value of the switched volt-amperes (switched by the individual switches) depend on the load angle while the peak of the per switching period conducted current appears to be both modulation index dependent and load angle dependent.

Due to the above described complexity in calculating the peak power losses of the individual components in the matrix converter, a more pragmatic approach will be applied. The approach is to describe the time varying losses of the transistor, p_{tx}, and of the diode, p_{dx}, as sinusoidal functions given by:

$$p_{tx} = P_{tx} + (\langle \hat{P}_{t,sw} \rangle_{T_s} + \langle \hat{P}_{t,cond} \rangle_{T_s} - P_{tx}) \cdot \sin(\omega_g t) \quad (4.79)$$

$$p_{dx} = P_{dx} + (\langle \hat{P}_{d,sw} \rangle_{T_s} + \langle \hat{P}_{d,cond} \rangle_{T_s} - P_{dx}) \cdot \sin(\omega_g t) \quad (4.80)$$

where P_{tx} and P_{dx} are the average transistor- and diode losses , $\langle \hat{P}_{t,sw} \rangle_{T_s}$ and $\langle \hat{P}_{d,sw} \rangle_{T_s}$ are the peak switching losses of a transistor and diode, evaluated for each switching period while , $\langle \hat{P}_{t,cond} \rangle_{T_s}$ and $\langle \hat{P}_{d,cond} \rangle_{T_s}$ are the peak conducting losses of the transistor and diode, evaluated for each switching period. In the present approach, the peak switching

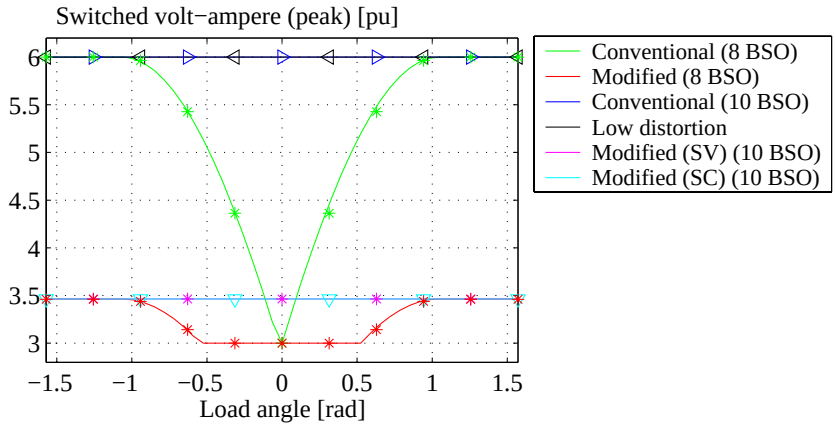


Figure 4.38: *The peak of the switched volt-amperes versus load angle when evaluated in each switching period.*

losses per switching fundamental is calculated by:

$$\langle \hat{P}_{t,sw} \rangle_{T_s} = \langle \hat{S}_{sw,Sa1} \rangle_{T_s} \cdot E_{sw0,t} \cdot f_{sw} \tag{4.81}$$

$$\langle \hat{P}_{d,sw} \rangle_{T_s} = \langle \hat{S}_{sw,Sa1} \rangle_{T_s} \cdot E_{sw0,d} \cdot f_{sw} \tag{4.82}$$

As discussed above, the per switching period switched volt-amperes depend on both the load angle and the modulation method. Fig. 4.38 shows the peak value of the per switching period switched volt-amperes as a function of the load angle. The peak value of the per switching period switched volt-amperes when using the conventional 8 BSO modulation method can be approximated by:

$$\langle \hat{S}_{sw,Sa1} \rangle_{T_s} \approx \begin{cases} 3 + 3 \cdot \left| \sin\left(\frac{3}{2} \cdot \phi_r\right) \right| V_{gp} \cdot I_r & |\phi_r| < \frac{\pi}{6} \\ 6 \cdot V_{gp} \cdot I_r & \frac{\pi}{6} \leq |\phi_r| \leq \frac{\pi}{2} \end{cases} \tag{4.83}$$

The peak value of the per switching period switched volt-amperes when using the modified 8 BSO modulation method can be approximated by:

$$\langle \hat{S}_{sw,Sa1} \rangle_{T_s} \approx \begin{cases} 3 \cdot V_{gp} \cdot I_r & |\phi_r| < \frac{\pi}{6} \\ \left(3 + 0.461 \cdot \left| \sin\left(3 \cdot \phi_r - \frac{\pi}{2}\right) \right|\right) V_{gp} \cdot I_r & \frac{\pi}{6} \leq |\phi_r| < \frac{\pi}{3} \\ 3.461 \cdot V_{gp} \cdot I_r & \frac{\pi}{3} \leq |\phi_r| \leq \frac{\pi}{2} \end{cases} \tag{4.84}$$

Considering the conventional 10 BSO modulation method and the low distortion modulation method, the peak value of the per switching period switched volt-amperes is constant and can be approximated by:

$$\langle \hat{S}_{sw,Sa1} \rangle_{T_s} \approx 6 \cdot V_{gp} \cdot I_r \tag{4.85}$$

Finally, for the modified modulation methods involving 10 BSO's the peak value of the per switching period switched volt-amperes can be approximated by:

$$\langle \hat{S}_{sw,Sa1} \rangle_{T_s} \approx 3.461 \cdot V_{gp} \cdot I_r \tag{4.86}$$

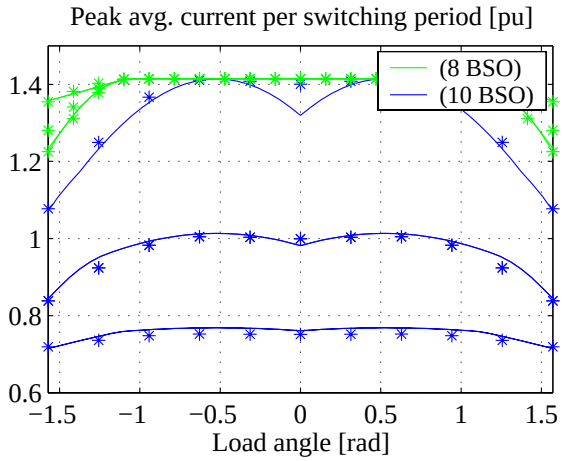


Figure 4.39: *The peak of the per switching period average current versus load angle.*

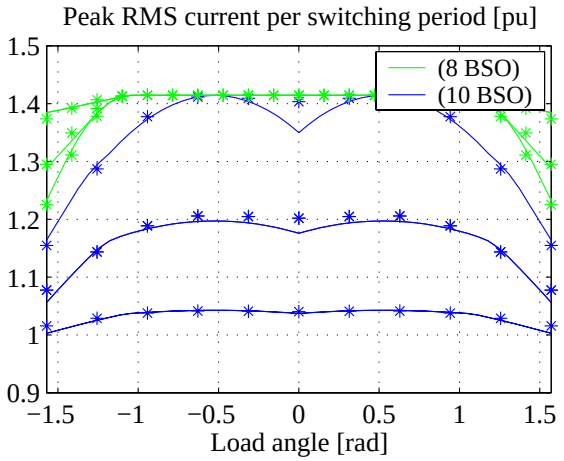


Figure 4.40: *The peak of the per switching period RMS current versus load angle.*

The solid lines in Fig. 4.38 are derived directly from surfaces lake that in Fig. 4.36 while the values marked with (*) represents the modeling of the peak value of the switched volt-amperes as given by eq. (4.83) - eq. (4.86).

The peak value of the per switching period conducting losses are derived by:

$$\langle \hat{P}_{t,cond} \rangle_{T_s} = V_{t0}(T) \cdot \langle \hat{I}_{t,avg} \rangle_{T_s} + R_t(T) \cdot \langle \hat{I}_t \rangle^2_{T_s} \quad (4.87)$$

$$\langle \hat{P}_{d,cond} \rangle_{T_s} = V_{d0}(T) \cdot \langle \hat{I}_{d,avg} \rangle_{T_s} + R_d(T) \cdot \langle \hat{I}_d \rangle^2_{T_s} \quad (4.88)$$

where $\langle \hat{I}_{x,avg} \rangle_{T_s}$ and $\langle \hat{I}_x \rangle_{T_s}$ are the maximum appearing value of the per switching period average and RMS current through the considered component. Fig. 4.39 shows the peak value of the per switching period average current through a transistor (and diode) while Fig. 4.40 shows the peak value of the per switching period RMS current through a transistor (and diode). As appear from Fig. 4.39 and Fig. 4.40 the peak value of the per switching period average transistor- and diode current is dependent on the load angle, the modulation index and the chosen modulation method.

For the modulation functions involving 8 BSO, the peak value of the per switching period average current can be approximated by:

$$\langle \hat{I}_{t,avg} \rangle_{T_s} \approx \begin{cases} \sqrt{2} \cdot I_r & |\phi_r| < \frac{\pi}{3} \\ \left(\sqrt{2} - 0.1892 \cdot \sqrt{M} |1 + \cos(3\phi_r)| \right) I_r & |\phi_r| \geq \frac{\pi}{3} \end{cases} \quad (4.89)$$

while for the modulation functions involving 10 BSO′s, the peak value of the per switching period average current can be approximated by:

$$\langle \hat{I}_{t,avg} \rangle_{T_s} \approx \left(\frac{1}{\sqrt{2}} + 0.37 M^{1.5} + 0.39 M \cdot \sin\left(\phi_r + \frac{\pi}{2}\right) + 0.065 M \cdot \sin\left(3\phi_r + \frac{\pi}{2}\right) \right) I_r \quad (4.90)$$

Similarly, approximations for the peak value of per switching period RMS current can be found. For the modulation functions involving 8 BSO, the peak RMS current is approximated by:

$$\langle \hat{I}_t \rangle_{T_s} \approx \begin{cases} \sqrt{2} \cdot I_r & |\phi_r| < \frac{\pi}{3} \\ \left(\sqrt{2} - 0.1892 \cdot M^{\frac{2}{3}} \cdot |1 + \cos(3 \cdot \phi_r)| \right) \cdot I_r & |\phi_r| \geq \frac{\pi}{3} \end{cases} \tag{4.91}$$

while for the modulation functions involving 10 BSO′s, the peak value of the per switching period RMS current can be approximated by:

$$\langle \hat{I}_t \rangle_{T_s} \approx \left(1 + \left(\frac{2}{\sqrt{3}} - 1 \right) M + 0.30M \cdot \sin\left(\phi_r + \frac{\pi}{2} \right) + 0.05M \cdot \sin\left(3\phi_r + \frac{\pi}{2} \right) \right) I_r \tag{4.92}$$

Assuming that the thermal capacitance of the case to ambient structure of the semiconductor module is sufficiently large to suppress temperature variations in the considered frequency range, the peak junction temperature of the transistor and diode can be estimated by:

$$\hat{T}_{tx} = P_{tx} \sum_{w=1}^{y} R_{thxw,t} + \left(\langle \hat{P}_{t,sw} \rangle_{T_s} + \langle \hat{P}_{t,cond} \rangle_{T_s} - P_{tx} \right) |Z_{thxw,t}(\omega_g)| + T_c \tag{4.93}$$

$$\hat{T}_{dx} = P_{dx} \sum_{w=1}^{y} R_{thxw,d} + \left(\langle \hat{P}_{d,sw} \rangle_{T_s} + \langle \hat{P}_{d,cond} \rangle_{T_s} - P_{dx} \right) |Z_{thxw,d}(\omega_g)| + T_c \tag{4.94}$$

With the assumption of sufficiently large thermal capacity of the case to ambient structure, the case temperature T_c is given by:

$$T_c = 4 \cdot (P_{tx} + P_{dx}) \cdot (R_{thch} + R_{thha}) + T_{amb} \tag{4.95}$$

To justify the above described rough approach for estimating the peak temperatures, it should be noted that according to Fig. 4.36 and Fig. 4.37 the peak power losses can never appear as a static value due to the high frequency on the grid side of the matrix converter and hence the peak temperature of the matrix converter components is not as crucial as for the switches of the back-to-back converter. This statement is very much supported by the results obtained in [8].

4.4.4 Filter power losses

In the modeling approach of the power losses within the grid filter for the matrix converter, it is assumed that only the inductor resistances are contributing significantly to the filter power losses. Further, it is assumed that any filter damping necessary for the functionality of the matrix converter can be achieved by active control, without sacrificing the quality of the generated waveforms to considerable extent. Hence the modeling approach for the power losses within matrix converter filter will follow the same procedure as for the back-to-back two-level converter as discussed in section 3.4.4.

The inductor power losses P_L are composed of copper losses, hysteresis losses and eddy current losses:

$$P_L = P_{cu} + P_{hy} + P_{ed} \tag{4.96}$$

Copper losses

The copper losses in the inductor are due to the effective resistance R_L of the windings.

$$P_{cu} = 3R_L I_L^2 \tag{4.97}$$

Where the effective resistance is a function of the inductor design, the inductor temperature and the frequency of the inductor current. For a given load current and a desired inductor value, Appendix B provides a detailed inductor design tool from which the effective resistance R_L of the inductor is extracted.

Hysteresis losses

The empirical Steinmetz equation expresses the specific hysteresis loss as an exponential function of the frequency f and the maximum flux density $\hat{B}_c$. Provided that the magnetizing current is purely sinusoidal, the hysteresis loss can be expressed by:

$$P_{hy} = M_L \cdot c_m \cdot f^{\alpha} \cdot \hat{B}_c^{\beta} \tag{4.98}$$

where M_L is the weight of the core material c_m, α and β are material property constants. Despite, the formula in (4.98) is a well established expression for the hysteresis losses, manufactures of iron cores rather provide graphical presentation of the loss characteristic than providing the material property constants. Appendix B provides a detailed description on the extraction of the material property constants c_m, α and β as well as a design procedure for determining core material mass, given the nominal current and the desired inductance value. The design values for the current and inductance are discussed in section 4.5.2.

Eddy current losses

To account for the eddy current losses the empirical Steinmetz equation is used:

$$P_{ed} = M_L \cdot \frac{\sigma_c \cdot \tau}{12\rho_c} \left(\frac{dB}{dt} \right)^2 \tag{4.99}$$

where σ_c is the conductivity of the core material, τ is the thickness of the lamination and ρ_c is the mass density of the iron. For a more detailed description on the modeling of the inductor power losses, see Appendix B.

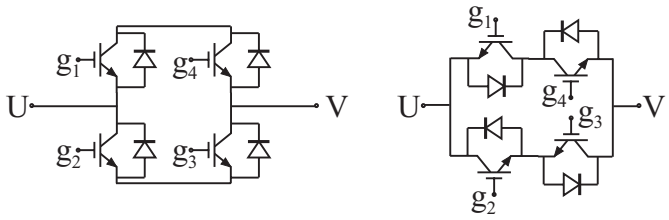


Figure 4.41: *Realization of a bi-directional switch from a standard full-bridge module.*

4.5 Design aspects

Based on the modeling approach described in the previous sections, especially section 4.4, the loading of individual components within the matrix converter can be estimated for a certain load profile. Hence, in many aspects, a rough design guideline for current- and voltage ratings of the matrix converter components can be obtained by combining the modeling approach of the surrounding turbine components as described in chapter 2 with the equations obtained from the loss modeling approach in section 4.4. Nevertheless, from an initial design point of view it may seem a little overwhelming and confusing to select and combine the necessary equations - equations which in some cases were derived for a slightly different purpose. Hence a short summary on the design aspects regarding selection of an appropriate switch will be provided. Then some guidelines regarding filter design will be outlined and finally some consideration regarding selection of switching frequency will be discussed.

4.5.1 Design of the bi-directional switches

As discussed in section 4.4.3, dealing with the thermal modeling approach, it is provided that the bi-directional switch is realized from a standard H-bridge module as shown in Fig. 4.41. Using an H-bridge module actually forms a bidirectional switch with two parallel branches - one branch consisting of a common collector bi-directional switch and another branch consisting of a common emitter bi-directional switch. Fig. 4.41 shows the realization of a bi-directional switch from a standard full-bridge module.

Current ratings

Provided that the power factor at the input of the matrix converter is restricted to unity, the RMS current loading of each transistor and diode in a bidirectional switch was derived in section 4.4.1 and given by:

$$I_t = \frac{1}{\sqrt{6}} I_r \tag{4.100}$$

However, to select an appropriate switch it is worthwhile to notice that the time period for which the RMS current is evaluated is a time period common for both the input side and output side. Since the frequency at the generator in the doubly-fed system is

rather low the design should take into account that the RMS current loading evaluated on a more *local basis* will be up to a factor of 2 higher than the value calculated by eq. (4.100). Using the simplified modeling approach of the generator, as discussed in section 2.4.4 on page 37 the RMS rotor current I_r, can then be estimated by:

$$\tilde{I}_r = \frac{1}{N_{gen}} \cdot \frac{\sqrt{\tilde{P}_r^2 + \tilde{Q}_r^2}}{3 \cdot s \cdot |\underline{V}_s|} \tag{4.101}$$

where the " ˜ " indicates that the quantity is an estimated value and s is the slip of the generator. Neglecting the generator power losses, the rotor power P_r is estimated by:

$$\tilde{P}_r = \frac{s(\omega_{gen} T_{gen})}{1+s} \tag{4.102}$$

where $\omega_{gen} T_{gen}$ is the power applied at the shaft of the generator[9]. The reactive rotor power Q_r is estimated by:

$$\tilde{Q}_r = s \cdot \left(Q_s^* + \frac{3|\underline{V}|_s^2}{\omega_s L_m} \right) \tag{4.103}$$

where Q_s^* is the desired reactive power to be generated from the stator.

Voltage ratings

Considering the voltage ratings of the matrix converter, the reduced voltage gain plays an important role. As discussed in section 4.3 the actual voltage gain of the matrix converter depend on the chosen modulation strategy but can never exceed $\sqrt{3}/2$ unless entering the non-linear over modulation range. Hence, to obtain the same operating speed range as for the two-level back-to-back voltage source converter two possibilities can be considered: 1) Selecting an appropriate input voltage, in order to obtain the same output voltage as for the 2-level back-to-back voltage source converter or 2) select a generator winding ration N_{gen} which is $2/\sqrt{3}$ lower than for the generator used in the 2-level back-to-back voltage source converter. The latter will clearly increase the rotor current by a factor of $2/\sqrt{3}$.

Neglecting the overvoltages arising from stray inductances between the input filter capacitors and the switches and overvoltages caused by oscillations in the input filter, the transistors and diodes within the matrix converter should be designed to withstand the phase-phase peak voltage at the input side of the matrix converter. The minimum required input voltage to the matrix converter $|\underline{V}'_{g3}|$ depends on the operating condition and is generally estimated by:

$$|\underline{V}'_{g3,min}| = \frac{2}{\sqrt{3}} \left(|\hat{s}| \cdot N_{gen} \cdot |\underline{V}_s| \right) \tag{4.104}$$

[9]Neglecting power losses in the system , the power applied at the shaft of the generator is equal to the turbine power.

where $|\hat{s}|$ is the maximum occurring slip. Assuming that the filter is realized by a 2-stage LC filter as shown in Fig. 4.42 and having the minimum required input voltage to the matrix converter, the required transformer voltage $|\underline{V}_{g3}|$ can be calculated from:

$$|\underline{V}_{g3}| = \left| \frac{Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d}{Z_b Z_d} \underline{V}'_{g3,min} + \frac{(Z_a Z_b Z_d + Z_a Z_c Z_d + Z_b Z_c Z_d)}{Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d} \underline{I}'_{g3} \right| \tag{4.105}$$

where the impedances $Z_a ... Z_d$ are given in accordance with Fig. 4.42:

$$Z_a = j \cdot \omega_g \cdot L_a \tag{4.106}$$

$$Z_b = R_b + \frac{1}{j \cdot \omega_g \cdot C_b} \tag{4.107}$$

$$Z_c = j \cdot \omega_g \cdot L_c \tag{4.108}$$

$$Z_d = R_d + \frac{1}{j \cdot \omega_g \cdot C_d} \tag{4.109}$$

The current from the matrix converter $|\underline{I}'_{g3}(s)|$ can be estimated by:

$$|\tilde{I}'_{g3}(s)| = \frac{\tilde{P}_r}{2 \cdot \sqrt{3} \cdot |s| \cdot |\underline{V}_s|} \tag{4.110}$$

Having the required transformer voltage from eq. (4.105) the load dependent voltage at the matrix converter terminals can be calculated by:

$$|\underline{V}'_{g3}| = \left| \frac{Z_b Z_d}{Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d} \underline{V}_{g3} + \frac{(Z_a Z_b Z_d + Z_a Z_c Z_d + Z_b Z_c Z_d)}{Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d} \underline{I}'_{g3} \right| \tag{4.111}$$

Hence the switches of the matrix converter should at least be capable of withstanding a voltage of $\sqrt{6} \cdot |\underline{V}'_{g3}|$ as given by eq. (4.111). However as was the case for the back-to-back two-level voltage source converter, the selection of appropriate switches should incorporate some design margin in order to cope with the transient voltage spikes occurring at each switching instant due to stray inductances and voltage oscillations in the input filter. As the stray inductances depend on the specific hardware layout it is not possible to come up with a *watertight* design rule but since the stray inductances in the matrix converter design inevitable will be larger than in the back-to-back two-level voltage source converter where the stray inductances can be clamped at the DC-terminals of the half-bridge module, the design margin should be larger than the corresponding design margin applied to the back-to-back two-level voltage source converter. The voltage margin design rule for the back-to-back two-level voltage source converter was based on common practice and was illustrated in Fig. 3.39 on page 76.

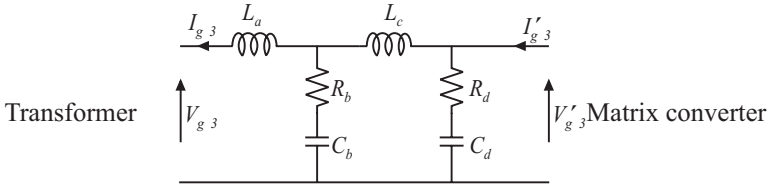


Figure 4.42: *Filter topology for the matrix converter.*

4.5.2 Filter design

As the matrix converter acts as a current source on the grid side, the matrix converter has to be connected to a *pure* voltage source in order to obtain a proper operation. Due to line impedance and stray inductances in the transformer, the grid itself can not be considered as a *pure* voltage source and hence the input filter has to provide this feature. Further, since the matrix converter itself generates a high amount of current harmonics the filter has to attenuate these current harmonics to an acceptable amount. Finally, considering the fundamental frequency, the filter design should take into account the reactive power consumption and the voltage drop across the filter. Fig. 4.42 shows the considered filter topology.

In the following, some guidelines regarding the filter design is provided [59]. Besides these general design guidelines, some practical filter issues regarding grid voltage distortions, filter resonance and power-up should be addressed [40]. However, these practical issues will not be treated in this thesis.

Fundamental frequency considerations

Due to a highly increased complexity in the calculation of losses and waveform quality, it was decided to restrict the controllable power factor at the input of the matrix converter to be unity. This implies that the current $\underline{I}'_{g3}$ is always in phase with the voltage $\underline{V}'_{g3}$, c.f. Fig. 4.42. This restriction further implies that the matrix converter is not able to compensate the reactive power absorption in the grid filter and hence this compensation has to be done through the generator. The reactive power absorbed by the filter depends on the operating conditions but in general is given by:

$$Q_g = 3 \cdot \Im m(\underline{V}_{g3} \cdot \underline{I}^{\star}_{g3}) \tag{4.112}$$

where the * denotes the complex conjugate. The current $\underline{I}_{g3}$ is given by:

$$\underline{I}_{g3} = \frac{(Z_a Z_b Z_d + Z_b^2 Z_d)\underline{I}'_{g3} - (Z_b^2 + Z_a Z_d + Z_b Z_d + Z_a Z_b + Z_a Z_c + Z_b Z_c)\underline{V}_{g3}}{(Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d)(Z_a + Z_b)} \tag{4.113}$$

To determine the actual orientation of the current $\underline{I}'_{g3}$, the voltage $\underline{V}'_{g3}$ has to be calculated. The voltage at the matrix converter side of the filter is given by:

$$\underline{V}'_{g3} = \frac{Z_b Z_d \underline{V}_{g3} + (Z_a Z_b Z_d + Z_a Z_c Z_d + Z_b Z_c Z_d)\underline{I}'_{g3}}{Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d} \tag{4.114}$$

Besides determining the orientation of the voltage $\underline{V}'_{g3}$, eq. (4.114) gives the voltage ratings for which the switches of the matrix converter has to be designed, c.f. section 4.5.1 on page 133.

Frequency analysis

Besides establishing a *pure* voltage source at the input of the matrix converter, the aim of the filter was to reduce the amount of current harmonics emitted to the supply grid. Considering the transfer function from converter harmonic current $\underline{I}'_{g3,h}$ to grid harmonic current $\underline{I}_{g3,h}$, this is given by:

$$\underline{I}_{g3,h} = \frac{Z_b Z_d}{Z_a Z_d + Z_a Z_c + Z_b Z_c + Z_a Z_b + Z_b Z_d} \underline{I}'_{g3,h} \tag{4.115}$$

where the impedances Z_a - Z_d is given by eq. (4.106) - eq. (4.109). Another important aspect when considering the filter design is the interaction with harmonics on the grid. Clearly, if harmonics are present in the grid voltage these harmonics will for a certain filter design be able to resonate with the LC-LC filter circuit. Hence an important aspect when designing the filter is to locate the resonance frequencies of the filter in a frequency range where 1: No harmonics are present in the grid voltage or 2) in a range where the matrix converter is able to actively damp the resonance. Alternatively (or in combination) The passive damping resistors can be designed to attenuate the resonance of the filter. Considering the relation between harmonic voltage on the grid $\underline{V}_{g3,h}$ and harmonic voltage present at the terminals of the matrix converter $\underline{V}'_{g3,h}$, this is given by:

$$\underline{V}'_{g3,h} = \frac{Z_b Z_d}{Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d} \underline{V}_{g3,h} \tag{4.116}$$

Finally, the current harmonics $\underline{I}'_{g3,h}$ fed from the matrix converter to the filter may cause resonance problems in the filter. Assuming ideal supply voltage, the relation between current harmonics and harmonic voltage present at the matrix converter terminals is given by:

$$\underline{V}'_{g3,h} = \frac{(Z_a Z_b Z_d + Z_a Z_c Z_d + Z_b Z_c Z_d)}{Z_a Z_b + Z_a Z_c + Z_a Z_d + Z_b Z_c + Z_b Z_d + Z_c Z_d} \underline{I}'_{g3,h} \tag{4.117}$$

4.5.3 Modulation strategy and switching frequency

To this stage, the different modulation methods have been evaluated with regard to harmonic performance and generated power losses, assuming the same switching frequency for all the modulation methods. However as it appeared when evaluating with regard to these criteria, the modulation methods behave quite different when evaluated over the operative modulation range and hence a fair comparison is not directly obtainable. Actually, in order to be able to compare the different modulation methods - and in a final stage compare different converters, one evaluation parameter has to form a common basis. In some prior art documents [25, 40], the number of switchings for the

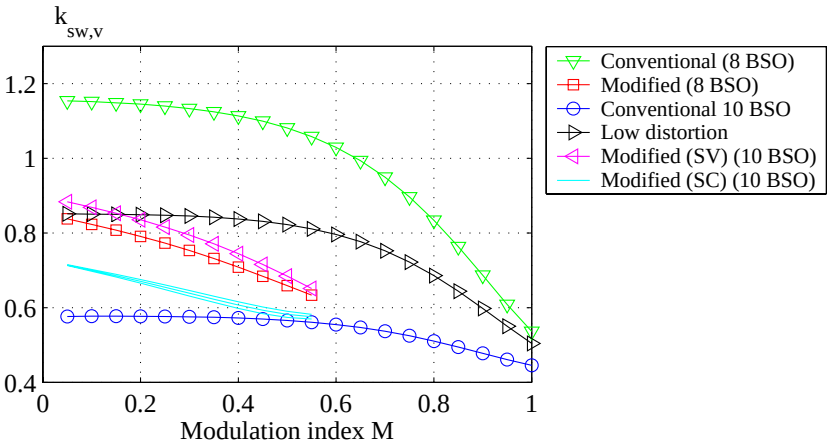


Figure 4.43: *The switching frequency correction factor where output voltage distortion is normalized to the suboptimal modulation method of the two-level voltage source inverter, c.f. section 3.3.3 on page 53.*

different modulation methods has been used to form a common basis for the comparison. Equaling the number of switchings seems however to be a strange common basis for a comparison as the number of switchings in it self is not an interesting parameter. In the previous chapter treating the back-to-back two-level voltage source converter, the common basis was formed by evaluating the generated harmonic distortion and then adjusting the switching frequency for the different modulation methods in order to obtain the same harmonic distortion in the entire modulation range. Considering the matrix converter, the selection of an appropriate switching frequency is a little more tricky as the switching frequency for the matrix converter influences both the quality of the generated generator voltage and the quality of the generated grid current. Hence, adopting the same ideas as used in chapter 3, two approaches appear. Either, the switching frequency for the different modulation methods can be adjusted to generate the same harmonic distortion in the generator voltage or adjusted to generate the same harmonic distortion in the grid current.

Using the generated harmonic voltage distortion as a common basis for the converter evaluation, the switching frequency for the different modulation methods has to be adjusted by a switching frequency correction factor $k_{sw,v}$. Fig. 4.43 shows the switching frequency correction factor as a function of the modulation index for the considered modulation methods where the switching frequency correction factor is adjusted to generate the same harmonic voltage distortion as generated by the suboptimal modulation scheme for the back-to-back two-level converter[10] , c.f. section 3.3.4. Having the modulation index M_0 for the nominal working condition, the switching frequency correction factor for the different modulation methods can be fitted by a polynomial. The switching frequency correction factor for the conventional double sided modulation method

[10]The harmonics are evaluated for the same output voltage capability.

can be approximated by:

$$k_{sw,v} = 3.333M_0^5 - 7.897M_0^4 + 5.769M_0^3 - 2.055M_0^2 + 0.239M_0 + 1.145 \quad (4.118)$$

where M_0 is the modulation index when operating at nominal conditions. Similarly, the switching frequency correction factor for the modified double sided modulation method can be approximated by:

$$k_{sw,v} = 1.002M_0^5 - 0.463M_0^4 - 0.341M_0^3 - 0.0570M_0^2 - 0.277M_0 + 0.852 \quad (4.119)$$

while the correction factor for the conventional double sided modulation method with distributed zero vectors becomes:

$$k_{sw,v} = 0.910M_0^5 - 2.137M_0^4 + 1.589M_0^3 - 0.578M_0^2 + 0.089M_0 + 0.573 \quad (4.120)$$

Considering the low distortion modulation method, the switching frequency correction factor can be approximated by:

$$k_{sw,v} = 1.883M_0^5 - 4.516M_0^4 + 3.253M_0^3 - 1.105M_0^2 + 0.142M_0 + 0.846 \quad (4.121)$$

The switching frequency correction factor for the modified double sided modulation method with distributed zero vectors when optimized for the switched voltage can be approximated by:

$$k_{sw,v} = 0.720M_0^5 - 0.476M_0^4 - 0.331M_0^3 - 0.113M_0^2 - 0.272M_0 + 0.897 \quad (4.122)$$

and finally the switching frequency correction factor for the modified double sided modulation method with distributed zero vectors and optimized for the switched current can be approximated by:

$$k_{sw,v} = 1.66M_0^5 - 0.695M_0^4 + 0.012M_0^3 - 0.094M_0^2 - 0.264M_0 + 0.727 \quad (4.123)$$

Alternatively, the switching frequency correction factor could be calculated to obtain comparable grid current harmonic distortion. Using this approach, the different modulation methods for the matrix converter is still comparable but a comparison with e.g. the two-level inverter is not directly obtainable. Fig. 4.44 shows the switching frequency correction factor as a function of the modulation index for the different modulation methods when the input current characteristics are used as a common basis. In Fig. 4.44 the conventional double sided modulation method is used as a reference. Having the modulation index M_0 for the nominal working condition, the switching frequency correction factor $k_{sw,c}$ for the different modulation methods can be polynomial-fitted. As the conventional double sided modulation method was chosen as basis, the switching frequency correction factor for this method simply becomes:

$$k_{sw,c} = 1 \quad (4.124)$$

The switching frequency correction factor for the modified double sided modulation method can be approximated by:

$$k_{sw,c} = -1.962M_0^5 + 2.042M_0^4 - 1.029M_0^3 + 0.372M_0^2 + 0.246M_0 + 1.527 \quad (4.125)$$

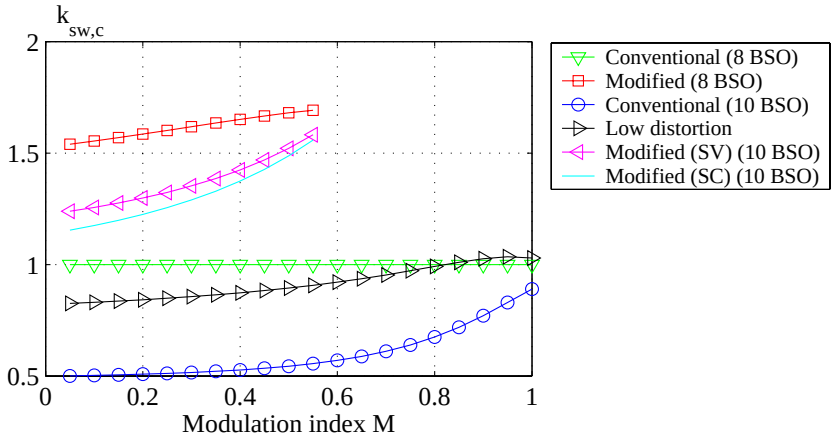


Figure 4.44: *The switching frequency correction factor where the input current distortion is normalized to the conventional double sided modulation method.*

while the correction factor for the conventional double sided modulation method with distributed zero vectors becomes:

$$k_{sw,c} = -1.066M_0^5 + 3.113M_0^4 - 2.529M_0^3 + 0.964M_0^2 - 0.094M_0 + 0.504 \quad (4.126)$$

Considering the low distortion modulation method, the switching frequency correction factor can be approximated by:

$$k_{sw,c} = -2.299M_0^5 + 5.004M_0^4 - 3.788M_0^3 + 1.381M_0^2 - 0.096M_0 + 0.829 \quad (4.127)$$

The correction factor for the modified double sided modulation method with distributed zero vectors when optimized for the switched voltage can be approximated by:

$$k_{sw,c} = 0.556M_0^5 + 0.281M_0^4 + 0.149M_0^3 + 0.417M_0^2 + 0.279M_0 + 1.224 \quad (4.128)$$

and finally the switching frequency correction factor for the modified double sided modulation method with distributed zero vectors and optimized for the switched current can be approximated by:

$$k_{sw,c} = 0.716M_0^5 + 0.110M_0^4 + 0.331M_0^3 + 0.437M_0^2 - 0.344M_0 + 1.136 \quad (4.129)$$

4.6 Model of the matrix converter

Input to the matrix converter model are given, both from the generator side and from the grid side, i.e. from the transformer. Input from the rotor side are the rotor voltage, rotor current, load angle and frequency, all given by the generator modeling approach described in section 2.4. Input from the grid side are the grid voltage, i.e. the voltage on the tertiary side of the transformer, c.f section 2.5 and the grid frequency. Based on these input, the converter model has to output the resulting grid current supplied to the tertiary transformer windings along with the converter losses.

4.6.1 Converter losses

Depending on the chosen modulation method, the total converter losses can be derived from the equations given in section 4.4. The power losses of the semiconductors within the matrix converter, P_{con}, is given by:

$$\begin{aligned} P_{con} &= 18\left(P_{t,cond} + P_{t,cond} + P_{t,sw} + P_{d,sw}\right) \\ &= 18\left(\left(V_{t0}(T) + V_{d0}(T)\right) \cdot I_{t,avg} + \left(R_t(T) + R_d(T)\right) \cdot I_t^2\right) + \\ &\quad S_{sw,avg}(E_{sw0,t} + E_{sw0,d}) \cdot f_{sw} \end{aligned} \tag{4.130}$$

The current quantities involved for calculating the conducting losses are independent of the chosen modulation method and can be calculated by eq. 4.62 and eq. 4.65 whereas the expression for the switched volt-amperes $S_{sw,avg}$ has to be calculated according to the chosen modulation method. The modulation method dependent expressions for the switched volt-amperes are given by eq. 4.71 - eq. 4.76. The grid inductor power losses P_L are calculated according to eq. (4.96) on page 132.

4.6.2 Power transferred to the transformer

According to eq. (2.47) on page 39 input to the transformer modeling approach is the grid inverter current $\underline{I}_{g3}$, the stator current I_s and the primary side voltage $\underline{V}_{g1}$. Hence, besides the converter losses, the only necessary output from the converter modeling is the grid inverter current.

$$\underline{I}_{g3} = \frac{(P_r - (P_{con} + P_L)) + j \cdot Q_g}{3 \cdot \underline{V}_{g3}} \tag{4.131}$$

where Q_g is the reactive power consumed by the filter of the matrix converter. The reactive power consumed by the grid filter can be calculated from eq. (4.112).

4.7 Summary

This chapter has treated the three-phase to three-phase matrix converter for use in a wind turbine application based on the doubly-fed induction generator. Specifically, the aim of the chapter was to be able to compare the matrix converter with the more matured back-to-back two-level converter conventionally used in said application. The chapter was introduced by a short review on previous work within the field of matrix converters but as the use of matrix converters in wind turbine applications appeared to be almost unknown, the survey has focused on matrix converters in general. The survey on previous work was followed up by an explanation of the basic working principles of the converter. The explanation of the basic working principles is a pure mathematical exercise and although complicated at a first glance, the real obstacles for the matrix converter occur due to non-ideal conditions. These non-ideal conditions involves considerations such as commutation strategy, bi-directional switch realization and operation

with unbalanced or faulty input- and output conditions. These working principle related issues are addressed in the major part of previous work. Closely related to the working principles are the modulation of the matrix converter which has to take into consideration both the generation of a sinusoidal input current and a sinusoidal output voltage and unlike the previously considered back-to-back two-level converter this has to be done without an intermediate energy storage. To obtain a fair comparison between the quite un-matured matrix converter and the conventionally used back-to-back two-level voltage source converter, a lot of efforts in this chapter was dedicated to develop new modulation methods for the matrix converter - modulation methods aiming to minimize the generated power losses [27] and/or the generated harmonic distortion [43]. To be able to compare the considered modulation methods internally as well as comparing the matrix converter with the other converter topologies, the modulation methods were evaluated with regard to harmonic performance [26] on both the grid side and generator side as well as with regard to the generated power losses. Regarding the power losses generated by the matrix converter, analytical expressions were derived taking into account the modulation method as well as the temperature of the considered components. Finally, to be able to design the matrix converter, some rules of thumb regarding switch current ratings, switch voltage ratings, choice of switching frequency and input filter design has been presented.

References

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Chapter 5

The back-to-back three-level voltage source converter

THE third and last power converter to be treated in this thesis is the back-to-back three-level voltage source converter. The configuration of the back-to-back three-level voltage source converter is in many aspects very similar to the back-to-back two-level voltage source converter treated in chapter 3 and hence the three-level converter adopts many of the nice features represented by the two-level counterpart. For instance the input side and output side of the converter are de-coupled and the converter control can be separated into a grid side inverter control and a rotor side inverter control working almost independently. Further, the voltage waveform synthesizing is better which may be used to decrease the switching frequency and/or reduce the size of the filters. This better voltage waveform is however obtained at the expense of a more complex hardware and control structure and problems such as voltage imbalance in the DC-link.

The chapter is introduced by a short review on the previous work in the field of three-level inverters followed by an explanation of the operating principles. Compared to the conventional two-level voltage source inverter, modulation schemes for use in three-level inverters are not as well exploited and hence a quite large part of the chapter is dedicated to the explanation of existing strategies and to the development of new modulation strategies. To be able to compare and in a final stage select an appropriate modulation method, the methods are evaluated with regard to their waveform quality, DC-link balancing capability, conducting losses, switching losses and influence on the switch temperature variation. Finally, to be used in a converter evaluation and converter comparison, the losses of the back-to-back three-level voltage source converter are modeled and some design aspects and design guidelines regarding component ratings are outlined.

5.1 Previous work

The three-level neutral point clamped (NPC) inverter was introduced by Nabae et. al. [24] in 1981 as an alternative to the conventional two-level voltage source inverter, offering high efficiency and improved harmonic performance. Fig. 5.1a shows one phase

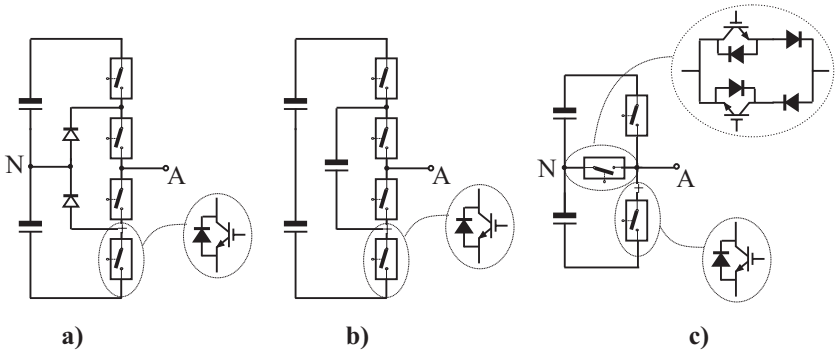


Figure 5.1: *Three-level structures (one phase-leg).* **a)** *Diode clamped inverter [24].* **b)** *Capacitor clamped inverter.* **c)** *Transistor clamped inverter [35].*

leg of the three-level NPC voltage source inverter. Since the introduction, the NPC inverter has been re-introduced in a couple of alternative configurations, diverging more or less from the original NPC-inverter. Fig. 5.1b and 5.1c show two of these configurations derived from the original NPC topology. The topology shown in Fig. 5.1b is called the three-level flying capacitor inverter and uses additional capacitors instead of diodes to provide a neutral level output voltage. The third alternative configuration, shown in Fig. 5.1c, was originally also proposed by Nabae et. al. back in 1981 but often the author of [35] is acknowledged as the inventor - maybe due to the fact that this author actually holds a US-patent (US4961129) specifically disclosing the present topology configuration. Besides the closely related converter topologies shown in Fig. 5.1, several topologies based on interconnection of conventional two-level inverters have been proposed, for instance such as those described in [5] and [26].

Originally, the NPC inverter was intended for high voltage- and low switching frequency power conversion applications but progressing advance in computational power processors and in solid state switching devices, such as the IGBT, has made the NPC inverter applicable also in low- and medium voltage high switching frequency applications [39, 41, 43]. Considering low switching frequency applications ($f_{sw} < 1$ kHz), a lot of research have been concerned about calculating optimal switching patterns to eliminate low order harmonics in the output voltage [8, 12, 23] but as the switching frequency increases, research on harmonic voltage elimination recedes while problems like e.g. reduction of switching losses becomes more urgent [6].

Another important issue regarding three-level inverters (and multi-level inverters in general) is the DC-link balancing problem. Without entering details at this point, it may appear from e.g. Fig. 5.1a that an unbalanced loading of the DC-link capacitors may occur due to:

- Unequal capacitor values due to manufacturing tolerances.

- Unequal loading of the capacitors due to un-intended switching delays.

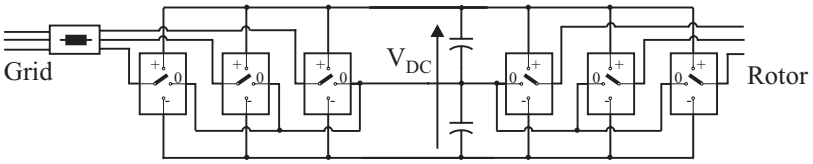


Figure 5.2: *Illustration of the back-to-back three-level voltage source converter.*

- Unequal loading of the capacitors due to e.g. non-linear loads containing even order harmonics [20].

Actually, a major part of papers concerning modulation of three-level inverters deals with the DC-link balancing issue, among these [4, 7, 18, 21, 25, 27, 29, 43, 46].

Along with the prevalent use of voltage source inverters and the enhancement of semiconductor devices a couple of secondary problems have appeared, among these an increasingly number of early bearing failures due to bearing currents. The bearing current arises from the voltage built up across the bearing due to electro-static couplings between machine windings and machine shaft/frame causing randomly appearing bearing current spikes. These bearing currents lead to bearing material erosion known as pitting and fluting and recent motor reliability studies have clarified that bearing failures account for about 40% of all motor failures [9]. Besides the steep voltage gradients and machine asymmetry, the inherent generation of common-mode voltages between the inverter neutral point and the motor neutral point is a certain cause of early bearing failures. With the purpose of reducing these early bearing failures in electrical machines, [31, 44] both proposed a modulation scheme for three-level NPC inverters with a complete elimination of the common-mode voltage. The elimination of common-mode voltage is however obtained at the expense of a reduced voltage gain of the three-level inverter but since it is likely to believe that the bearing current problem is even more severe in doubly-fed machines were the switched voltages are applied on the rotor windings, having much higher winding-shaft capacitance than the stator windings, the reduced inverter voltage gain may be justified by an extended bearing lifetime.

Although the three-level converter is widely used in applications such as traction and standard medium voltage converter applications the three-level converter is relatively untreated for wind turbine applications. Recently a few papers [28, 42] have been published concerning the back-to-back three-level converter for use in a wind turbine application while commercially, the Z72 2MW wind turbine from Harakosan (former Zephyros) is based on the ABB ACS1000 three-level converter [13, 37, 38].

5.2 Operating principles

As the name implies, the back-to-back three-level voltage source converter consists of two three-level inverters coupled in a back-to-back fashion as shown in Fig. 5.2. The two inverters of the back-to-back converter may be realized from any of the inverter legs

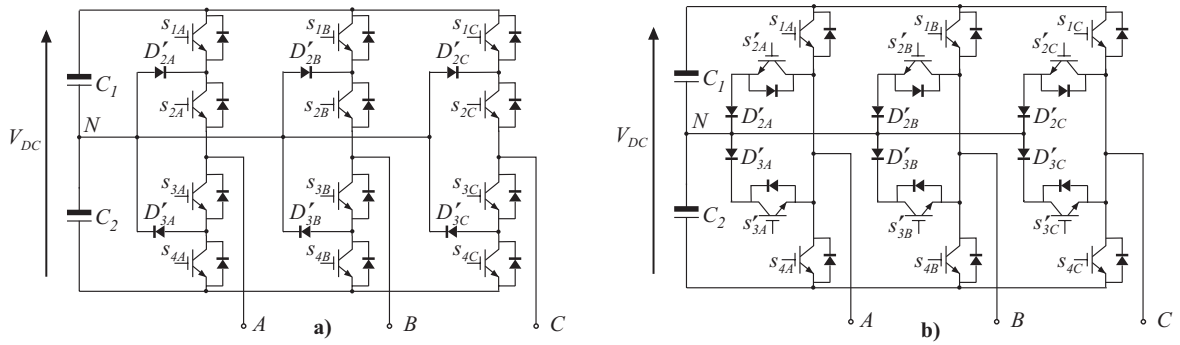


Figure 5.3: *The three-level NPC inverter.* **a)** *Diode clamped NPC inverter [24].* **b)** *Transistor clamped NPC inverter [35].*

shown in Fig. 5.1 but since the operating principles are a little different, at least for the flying capacitor topology in Fig. 5.1b, this chapter is limited to treat the topologies built on the inverter legs in Fig. 5.1a and Fig. 5.1c. Actually, these two inverter topologies are illustrated on Fig. 5.3. Fig. 5.3a shows the diode clamped three-level NPC inverter as proposed by [24] while Fig. 5.3b shows the transistor clamped NPC inverter. In the diode clamped NPC inverter topology, each of the switches $S_{1A}..S_{4C}$ and the diodes $D'_{2A}..D'_{3C}$ only have to block half the DC-link voltage and hence, the diode clamped NPC inverter is well suited for high voltage applications. Further, it appears that the diode clamped NPC inverter can be extended to an arbitrary number of voltage levels - still with the advantage that the individual switch only needs to block a voltage given by $(V_{DC}/(N_{levels}-1))$. As an alternative to the diode clamped NPC inverter, Fig. 5.3b shows the transistor clamped NPC inverter. It appears that the transistor clamped NPC inverter is built from the same number of components although the anti-parallel diodes in the neutral point clamping transistor, i.e. S_{2x} and S_{3x}, are of no use - at least with regard to the current flow. Like the diode clamped NPC inverter, the transistor clamped NPC inverter only switches half the DC-link voltage (if modulated properly), but concerning the voltage ratings of the switches it appears that the upper and lower switches (S_{1x} and S_{4x}) in the transistor clamped NPC inverter need the ability to block the full DC-link voltage. Hence, the transistor clamped NPC inverter is not as well suited for high voltage applications. Despite, the higher voltage ratings, a salient feature of the three-level transistor clamped NPC inverter is that only one semiconductor provides the conducting path to the upper and lower DC-bus thereby having the possibility of reducing the conducting losses, especially when a high modulation index is required (which typically is the case for the grid side inverter). This particular issue is treated in section 5.4.1. Finally, the transistor clamped NPC inverter can be extended to a higher number of voltage levels by adding diode clamped circuits for the additional levels.

5.2.1 Reference voltage generation

As in the case with the back-to-back two-level converter, the aim for the grid side inverter and the rotor side inverter in the back-to-back three-level converter is to synthesize a

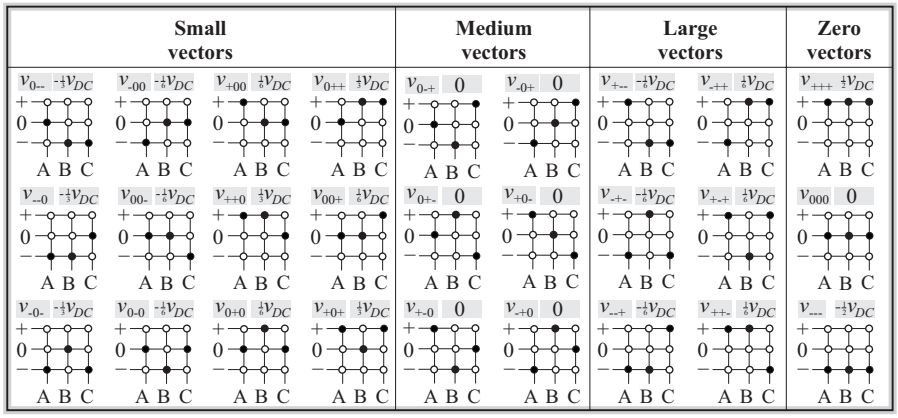


Figure 5.4: *The 27 possible switch configurations with the three level inverter.*

voltage that generates the desired grid current and rotor current respectively. Typically, the grid side inverter is operated to keep the DC-link voltage at a certain level while the rotor side inverter is operated to control the active and reactive power flow to/from the generator. Due to the similarities between the two-level and three-level converter, a more detailed explanation of the reference voltage generation is referred to section 3.2 on page 49.

5.2.2 Voltage synthesizing

As the two inverters of the back-to-back three-level converter are operated individually -at least with regards to the voltage synthesizing, the voltage synthesizing can be explained by inspection of only one of the inverters. With reference to Fig. 5.3 and with the restriction of not short circuiting the DC-link, the three-level inverter has 27 allowable and meaningful switch states. These switch states are shown in Fig. 5.4. Each of the illustrated switch states, are identified by a three letter code, representing the connection of phase leg A, B and C respectively. For instance, the code (+-0) represents a switch state where output phase A is connected to the positive DC-link, output phase B is connected to the negative DC-link and output phase C is connected to the center point. The switch states in Fig. 5.4 are categorized as "Small vectors", "Medium vectors" and "Large vectors", named after their location in the complex space vector plane, and as will be shown later, each vector category shows different properties with regard to the loading of the DC-link capacitors and with regards to common-mode voltage generation. By a proper control of the switch states in Fig. 5.4, the three-level inverter is able to synthesize the desired output voltage. The control of the switch states are known as modulation and will be treated in details in section 5.3.

5.2.3 DC-link imbalance

According to Fig. 5.3a an excessive high voltage may be applied to the switching devices if the neutral point N varies from the center potential of the DC-link. Further, both NPC

type inverters in Fig. 5.3 may be unable to synthesize the reference voltage if too large neutral point voltage variations occur. By inspection of Fig. 5.4 it appears that with regards to output voltage (phase-phase), several of these switch states are redundant (in pairs). For instance, the switch combinations v_{0--} and v_{+00} produce exactly the same output voltage (provided that the neutral point voltage is balanced) but with regards to the current flowing to/from the neutral point these two switch states behaves in the opposite manner. Hence, the selection among the redundant switch states has a vital influence on the neutral point potential and can actively be used to control/reestablish the neutral point voltage. An in-depth explanation of the DC-link balancing principles will be presented in section 5.3.5.

5.3 Modulation

As discussed above, an important feature of modulation schemes for three-level converters with split capacitor DC-link is the ability to control and stabilize the DC-link neutral point in case of an unbalanced loading condition. Unlike the two-level inverter where the redundancy in switching states v_{000} and v_{111}, c.f. section 3.3.3 on page 53, can be exclusively dedicated to e.g. switching loss reduction, the redundant switch states in the three-level inverter also have to be attributed to DC-link neutral potential stabilization [43]. In this section two basically different space vector approaches are presented. The first method is based on the conventional space vector approach while the latter is applicable to modulation with common mode voltage elimination. Since the vector sequences for both modulation methods can be altered resulting in different properties, the resulting amount of considered modulation strategies becomes about six. All the six modulation schemes are applicable for both of the inverters in Fig. 5.3 and with regard to harmonic performance and DC-link stabilizing ability both inverters behaves identical while with regards to conducting losses the two inverter topologies show different behaviour, depending on the chosen modulation method.

5.3.1 Conventional space vector approach

For the space vector approach, the following transformation of the time domain inverter output voltages is useful:

$$\underline{V_s^\star} = \frac{2}{3}\left(v_A^\star + v_B^\star \cdot e^{j\cdot\frac{2\pi}{3}} + v_C^\star \cdot e^{j\cdot\frac{4\pi}{3}}\right) \tag{5.1}$$

where $v_A^\star$, $v_B^\star$ and $v_C^\star$ are the three reference phase voltages given by:

$$\begin{aligned} v_A^\star &= \sqrt{2}V_A^\star \cdot \sin(\omega_s t) \\ v_B^\star &= \sqrt{2}V_B^\star \cdot \sin\left(\omega_s t - \frac{2\pi}{3}\right) \\ v_C^\star &= \sqrt{2}V_C^\star \cdot \sin\left(\omega_s t - \frac{4\pi}{3}\right) \end{aligned} \tag{5.2}$$

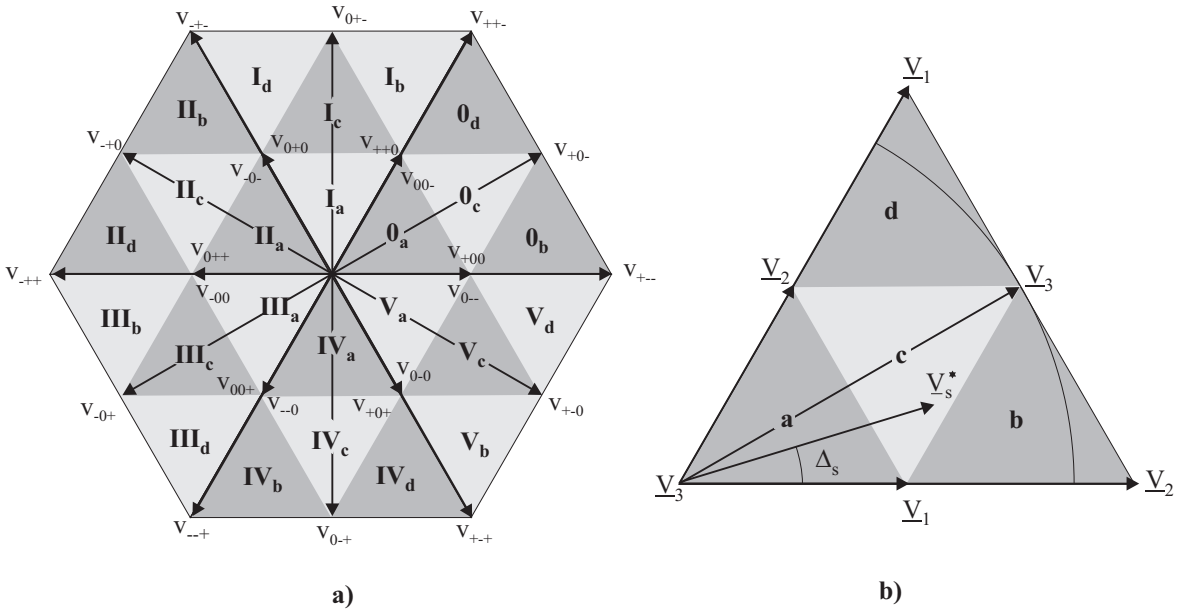


Figure 5.5: **a)** *The voltage space vectors for the three-level inverter.* **b)** *The definition of the segment independent angle* Δ_s.

By this transformation, the inverter output voltages become a vector with constant amplitude, rotating with a constant angular speed in the complex space vector plane.

Applying eq. (5.1) on the 27 possible switch combinations, c.f. Fig. 5.4, the space vector hexagon in Fig. 5.5a is obtained. With reference to Fig. 5.5b, which shows one of the main sectors in Fig. 5.5a, the reference voltage vector $\underline{V}_s^\star$ can be obtained by applying the three adjacent stationary vectors for an angle dependent time duration. For a given reference voltage vector $\underline{V}_s^\star$, the fractional on-times for the adjacent stationary vectors can be calculated and in general the following matrix equation has to be solved:

$$\begin{bmatrix} |\underline{V}_s^\star| \cdot \sin(\Delta_s) \\ |\underline{V}_s^\star| \cdot \cos(\Delta_s) \\ 1 \end{bmatrix} = \begin{bmatrix} Im(\underline{V}_1) & Im(\underline{V}_2) & Im(\underline{V}_3) \\ Re(\underline{V}_1) & Re(\underline{V}_2) & Re(\underline{V}_3) \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix} \tag{5.3}$$

where $\underline{V}_1$, $\underline{V}_2$ and $\underline{V}_3$ are the three stationary vectors closest to the reference vector and $\delta_{1..3}$ are the fractional on-time duration for the three stationary vectors. In order to solve eq. (5.3), the first step is to identify the sector location in order to determine the three adjacent vectors $\underline{V}_1$, $\underline{V}_2$ and $\underline{V}_3$.

Sector location

To establish expressions for the duty-cycles which are independent of, in which main sector **0-V** the voltage reference vector is located, the angle Δ_s is defined as:

$$\Delta_s = \mod\left(\omega_s t + \frac{\pi}{6}, \frac{\pi}{3}\right) \tag{5.4}$$

where $\omega_s t = 0$ is defined as the positive zero crossing of the phase A reference voltage ($v_A^\star = \sqrt{2} V_A \cdot \sin(\omega_s t)$). By this, the angle Δ_s is in the interval: $\Delta_s \in [0..\frac{\pi}{3}]$. Due to the

six fold symmetry and the angle definition in eq. (5.4) it is only necessary to monitor the six basic sectors **0-V** and then identify whether the sector location is **a**, **b**, **c** or **d**. Simply, by applying the law of sines, the following constrains are obtained:

$$Sector = \begin{cases} \mathbf{a} \text{ if } \left(M \leq \frac{1}{2\sin(2\pi/3-\Delta_s)}\right) \\ \mathbf{b} \text{ if } \left(M > \frac{1}{2\sin(\pi/3-\Delta_s)}\right) \\ \mathbf{c} \text{ if } \left(M > \frac{1}{2\sin(2\pi/3-\Delta_s)}\right) \wedge \left(M \leq \frac{1}{2\sin(\pi/3-\Delta_s)}\right) \wedge \left(M \leq \frac{1}{2\sin(\Delta_s)}\right) \\ \mathbf{d} \text{ if } \left(M > \frac{1}{2\sin(\Delta_s)}\right) \end{cases} \tag{5.5}$$

On-time duration

Based on the sector identification, the on-time ratios $\delta_{1..3}$ can be calculated. Basically, the on-time durations are found by solving eq. (5.3) but because the angles and amplitudes of the selected vectors, $\underline{V}_1 - \underline{V}_3$, depend on, in which sub-sector the reference voltage vector is located, the expressions for the on-times becomes sector dependent. Solving eq. (5.3) for the voltage reference vector located in sector X_a gives:

$$\begin{aligned} \delta_{1a} &= 2 \cdot \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin\left(\frac{\pi}{3} - \Delta_s\right) \\ \delta_{2a} &= 2 \cdot \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s) \\ \delta_{3a} &= 1 - \delta_1 - \delta_2 \end{aligned} \tag{5.6}$$

Solving for the reference vector located in sector X_b:

$$\begin{aligned} \delta_{1b} &= 2 - \frac{3|\underline{V}_s^\star|}{V_{DC}} \cdot \cos(\Delta_s) - \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s) \\ \delta_{2b} &= \frac{3|\underline{V}_s^\star|}{V_{DC}} \cos(\Delta_s) - \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s) - 1 \\ \delta_{3b} &= 2\frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s) \end{aligned} \tag{5.7}$$

Solving for the reference vector located in sector: X_c

$$\begin{aligned} \delta_{1c} &= (1 - 2 \cdot \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s)) \\ \delta_{2c} &= (2 \cdot \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin\left(\Delta_s - \frac{\pi}{3}\right) + 1) \\ \delta_{3c} &= (2 \cdot \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin\left(\Delta_s + \frac{\pi}{3}\right) - 1) \end{aligned} \tag{5.8}$$

And finally, solving for the reference vector located in sector X_d:

$$\begin{aligned} \delta_{1d} &= (2 \cdot \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s) - 1) \\ \delta_{2d} &= (2 - \frac{3|\underline{V}_s^\star|}{V_{DC}} \cos(\Delta_s) - \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s)) \\ \delta_{3d} &= (\frac{3|\underline{V}_s^\star|}{V_{DC}} \cdot \cos(\Delta_s) - \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s)) \end{aligned} \tag{5.9}$$

The duty-cycle expressions in eq. (5.6) - eq. (5.9) are at any instant of time limited by the following two constrains:

$$\sum_{n=1}^{3} \delta_{nj} \triangleq 1 \tag{5.10}$$

$$\delta_{nj} \geq 0 \qquad j \in [a, b, c, d] \tag{5.11}$$

To comply with the constrains above, the maximum obtainable reference space vector is given by:

$$|\hat{\underline{V}}_s^*| = \frac{V_{DC}}{\sqrt{3}} \tag{5.12}$$

5.3.2 Space vector modulation with common-mode voltage elimination

In the conventional modulation of the three level inverters and in fact all modulation schemes for the matrix converter and the two-level voltage source inverter treated in the two preceding chapters, a common-mode voltage is injected, both between the center point of the converter and the center point of the rotor circuit and between the center point of the converter and the center point of the grid side transformer. As discussed earlier this applied common mode voltage may cause generator shaft voltages and premature bearing failures [45]. In fact, [30] has shown that the bearing damaging common-mode voltage is twice as severe in a regenerative converter, eg. a back-to-back converter as in a non-regenerative converter. Further, the reasonable assumption, that the bearing current problem is even more severe in doubly-fed machines may justify to look for a method to reduce the common-mode voltage problems.

A salient feature of the three-level inverter is the possibility to reduce [17] or to eliminate [14] the common-mode voltage by use of a proper modulation scheme. Defining the common-mode voltage as:

$$v_0 = \frac{1}{3}(v_{AN} + v_{BN} + v_{CN}) \tag{5.13}$$

where N refers to the DC-link center point of the inverter, c.f. Fig. 5.3. It appears, that among the 27 allowable switch states in Fig. 5.4, only 7 of these switch states result in zero common-mode voltage [14, 44]. These switch states are: (+0-), (0+-), (-+0), (-0+), (0-+), (+-0) and (000) where the first six of these vectors are those categorized as *"medium vectors"*, cf. Fig. 5.4 and the latter is a zero vector. Restricting the modulation strategy to concern only these 7 switching states, the resulting space-vector hexagon is reduced to the hexagon shown in Fig. 5.6. The reference space vector voltage $\underline{V}_s^*$ is obtained in the same way as for the conventional space vector approach, c.f. eq. (5.1) on page 154, implying the steps of determining the sector location and then calculating the on-time durations.

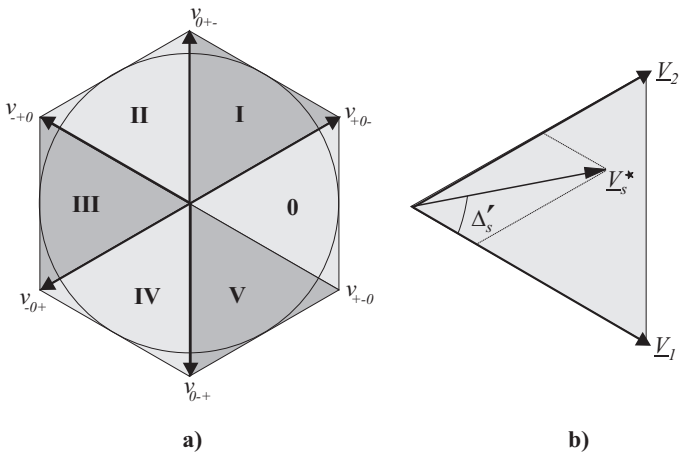


Figure 5.6: a) *The voltage space vectors for the space-vector modulation with common-mode voltage elimination.* **b)** *The definition of the segment independent angle* Δ'_s.

Sector location

To obtain duty-cycle expressions which are independent of the sector location, the angle Δ'_s is defined as:

$$\Delta'_s = \mod\left(\omega_s t, \frac{\pi}{3}\right) \tag{5.14}$$

where $\omega_s t = 0$ is defined as the positive zero crossing of the phase A reference voltage $v_A^\star = \sqrt{2}V_s \sin(\omega_s t)$. The apostrophe is used to indicate the difference between the conventional space vector approach and the present approach.

On-time duration

The sector independent duty-cycle expressions can then be derived by use of simple trigonometric considerations, c.f. Fig. 5.6:

$$\begin{aligned} \delta'_1 &= \frac{2|\underline{V}_s^\star|}{V_{DC}} \cdot \sin\left(\frac{\pi}{3} - \Delta'_s\right) \\ \delta'_2 &= \frac{2|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta'_s) \\ \delta'_0 &= 1 - \delta'_1 - \delta'_2 \end{aligned} \tag{5.15}$$

At all time instant the duty-cycle functions in eq. (5.15) are limited by:

$$0 \leq \delta'_x \leq 1 \qquad \text{where} \qquad x = [0, 1, 2] \tag{5.16}$$

From eq. (5.15) and eq. (5.16) it appears that the penalty to be paid for the elimination of the zero-sequence is, that the maximum output voltage is limited to half the DC-link voltage or $\frac{\sqrt{3}}{2}$ the output voltage of the conventional space vector modulation schemes.

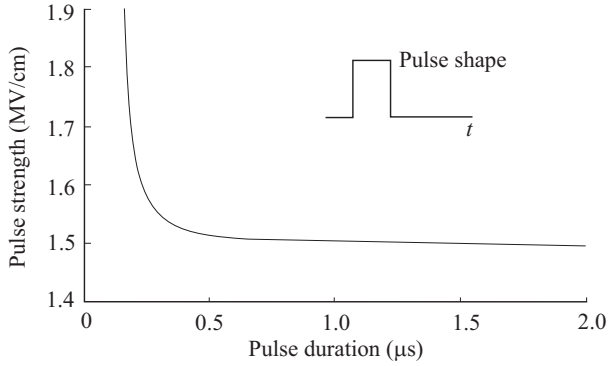


Figure 5.7: *Illustration of the field strength of a bearing lubricant film as a function of the pulse width [1].*

Transient common mode voltage effects

According to Fig. 5.6a each change in switch state, say from v_{+0-} to v_{0+-}, involves two branch switch over (BSO). If a slight mismatch of the switchings occur due to e.g. different delays in the gate drivers, a short common-mode voltage pulse is introduced at the motor terminals. Fortunately, regarding the break down voltage of bearing lubricant oil, the fields strength increases as the pulse width decreases [1], c.f. Fig. 5.7. Alternatively, the transient common-mode voltage can be eliminated by a snubber-circuit as described in [31] or by a common-mode voltage filter as described in [30, 32], but this clearly adds to the complexity of the system.

5.3.3 Modulation index

As in the case with the two-level voltage source inverter, the modulation index M for the three-level inverter is defined to be unity at the boundary where the conventional space vector modulation enters overmodulation. This boundary is shown as the circle in Fig. 5.5b. By this definition, the magnitude of the space vector voltage $|\underline{V}_s|$ is related to the modulation index by:

$$M = \frac{\sqrt{3}|\underline{V}_s^*|}{V_{DC}} \tag{5.17}$$

From the constrains given in eq. (5.16) it should be noted that the modulation index for the common-mode elimination method is limited to $\sqrt{3}/2$.

From the definition of the space vector voltage, c.f. eq. (5.1), the inverter RMS output phase voltage V_A^* is related to the modulation index by:

$$V_A^* = \frac{M}{\sqrt{6}} V_{DC} \tag{5.18}$$

TABLE I: *Switching table for modulation method 1 (Inner sectors).*

→Sector	a				
↓Even	δ_1	δ_2	δ_3	δ_1'	δ_2'
0	0−−	00−	000	+00	++0
II	−0−	−00	000	0+0	0++
IV	−−0	0−0	000	00+	+0+
↓Odd	δ_2'	δ_1	δ_3	δ_2	δ_1'
I	−0−	00−	000	0+0	++0
III	−−0	−00	000	00+	0++
V	0−−	0−0	000	+00	+0+

5.3.4 Vector sequences

Having the fractional on-times for the identified voltage vectors, there is still one degree of freedom left and that is the composition of the voltage vector sequence. The composition of the vector sequence can be done in an arbitrary number of ways and as the case with the two-level voltage source inverter and the matrix converter, a *clever* arrangement of the vector sequence may result in different salient properties such as reduced switching losses or improved harmonic performance.

In the following, six different vector sequences are described. The first five vector sequences are applicable for the conventional modulation method, while the last one can be applied on the modulation method with common-mode voltage elimination. All the discussed vector sequences are distributed symmetrically around the center of the switching period and for the vector sequences applicable for the conventional modulation method, any shift between switch states are only allowed to involve one branch switch over. The last restriction can however not be accomplished for the vector sequence with common-mode voltage elimination.

Finally, since the modulation methods for use with the three-level inverter is not matured to the same extent as in the case with the two-level voltage source inverter, there exists no common naming convention for the different vector sequences and hence the naming convention used in this thesis can in general not be referred to any prior art material.

Space vector modulation method 1 (SVPWM1)

The first vector sequence, named SVPWM1, is applicable for the conventional space vector approach and utilizes all possible switch states representing the three adjacent stationary vectors, in each switching cycle, e.g. none of the redundant switching states are omitted. As an example, considering sector $\mathbf{0_a}$ in Fig. 5.5a, the half of the switching sequence is given by:

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{000} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+00} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++0} \tag{5.19}$$

TABLE II: *Switching table for modulation method 1 (Outer sectors).*

→Sector	b				c					d			
↓Even	δ_1	δ_2	δ_3	δ'_1	δ_1	δ_2	δ_3	δ'_1	δ'_2	δ_2	δ_3	δ_1	δ'_2
0	0−−	+−−	+0−	+00	0−−	00−	+0−	+00	++0	00−	+0−	++−	++0
II	−0−	−+−	−+0	0+0	−0−	−00	−+0	0+0	0++	−00	−+0	−++	0++
IV	−−0	−−+	0−+	00+	−−0	0−0	0−+	00+	+0+	0−0	0−+	+−+	+0+
↓Odd	δ_1	δ_3	δ_2	δ'_1	δ_2	δ_1	δ_3	δ'_2	δ'_1	δ_2	δ_1	δ_3	δ'_2
I	00−	0+−	++−	++0	−0−	00−	0+−	0+0	++0	−0−	−+−	0+−	0+0
III	−00	−0+	−++	0++	−−0	−00	−0+	00+	0++	−−0	−−+	−0+	00+
V	0−0	+−0	+−+	+0+	0−−	0−0	+−0	+00	+0+	0−−	+−+	+−0	+00

Considering sector $\mathbf{0_b}$, the half of the switching sequence is given by:

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \tag{5.20}$$

Considering sector $\mathbf{0_c}$, the half of the switching sequence is given by :

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++0} \tag{5.21}$$

And finally for sector $\mathbf{0_d}$, the half of the switching sequence is given by:

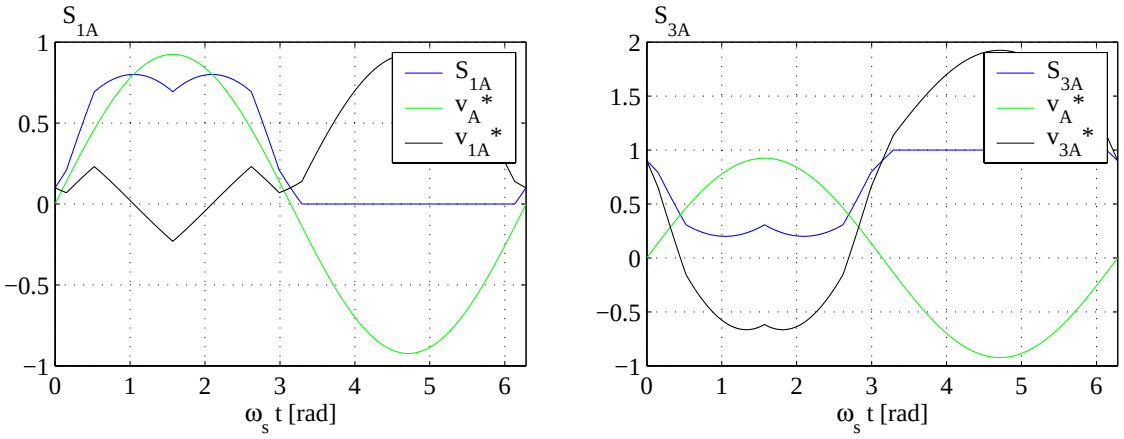
$$v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{++0} \tag{5.22}$$

For each of the switch state shifts above, the switched current and switched voltage are listed. Table I and Table II summarizes the sector dependent switch states where the switch states colored in red and green indicates the redundant switch states. An inspection of the table further indicates that the switch states colored in green load the DC-link in an opposite manner than the switch states colored in red. This property will be used in order to stabilize the DC-link neutral potential, c.f. section 5.3.5.

Although, the modulation scheme SVPWM1 can be implemented from the information in Table I and Table II along with eq. (5.5) - eq. (5.9), and analytical expressions for e.g. the current through the individual switches can be established, it may for some purposes be convenient to have analytical expressions of the modulation functions. Considering the modulation scheme SVPWM1, the modulation function for the upper switch S_{1A} is given by:

$$S_{1A} = \frac{\sqrt{2}}{\sqrt{3}} \frac{v_A^*}{V_A^*} M + v_{1A}^* \tag{5.23}$$

It should be noted that unlike the modulation functions for the two-level inverter, the signal v_{1A}^* is not a common-mode signal in an ordinary sense. For the purpose of deriving an analytical expression for the signal v_{1A}^* it is convenient to define the following six



a) b)

Figure 5.8: *Modulation function ($M = 0.8$) for the SVPWM1 method.* **a)** *Modulation function for the upper switch S_{1A}.* **b)** *Modulation function for the center switch S_{3A}.*

signals:

$$v^*_{Am} = \frac{1}{2V_{DC}} v^*_A \qquad v^*_{Bm} = \frac{1}{2V_{DC}} v^*_B \qquad v^*_{Cm} = \frac{1}{2V_{DC}} v^*_C \tag{5.24}$$

$$v^*_{min} = \min \begin{pmatrix} v^*_{Am} \\ v^*_{Bm} \\ v^*_{Cm} \end{pmatrix} \qquad v^*_{max} = \max \begin{pmatrix} v^*_{Am} \\ v^*_{Bm} \\ v^*_{Cm} \end{pmatrix} \qquad v^*_{mid} = -v^*_{min} - v^*_{max} \tag{5.25}$$

If the modulation index M is less than $1/2$, the signal v^*_{1A} can be obtained from:

$$v^*_{1A} = \max \begin{pmatrix} v^*_{Bm} \\ v^*_{Cm} \\ -2v^*_{Am} \end{pmatrix} \tag{5.26}$$

On the other hand, if the modulation index exceeds $1/2$, the signal v^*_{1A} is composed by:

$$v^*_{1A} = \max \begin{pmatrix} v^*_{mid} \\ \min \begin{pmatrix} -\min \begin{pmatrix} -v^*_{Bm} \\ -v^*_{Cm} \end{pmatrix} \\ \min \begin{pmatrix} v^*_{Bm} \\ v^*_{Cm} \end{pmatrix} + \frac{1}{2} \end{pmatrix} \\ -2v^*_{Am} \end{pmatrix} \tag{5.27}$$

The modulation function S_{3A} is given by:

$$S_{3A} = \overline{S}_{1A} \tag{5.28}$$

Finally, the modulation function for the switches S_{2A} and S_{4A} can be derived by multiplying the reference signals v^*_{Am}, v^*_{Bm} and v^*_{Cm} by -1. Fig. 5.8a and Fig. 5.8b shows an example of the modulation functions S_{1A} and S_{3A} when the modulation index equals 0.8. More precisely, Fig. 5.8a and Fig. 5.8b is an illustration of eq. (5.27) and eq. (5.28) respectively.

TABLE III: *Switching table for modulation method 2 (Inner sectors).*

→Sector	$\mathbf{a}_1$				$\mathbf{a}_2$			
↓Even	δ_1	δ_2	δ_3	δ_1'	δ_2	δ_3	δ_1	δ_2'
0	0−−	00−	000	+00	00−	000	+00	++0
II	−0−	−00	000	0+0	−00	000	0+0	0++
IV	−−0	0−0	000	00+	0−0	000	00+	+0+
↓Odd	δ_1	δ_3	δ_2	δ_1'	δ_2	δ_1	δ_3	δ_2'
I	00−	000	0+0	++0	−0−	00−	000	0+0
III	−00	000	00+	0++	−−0	−00	000	00+
V	0−0	000	+00	+0+	0−−	0−0	000	+00

Space vector modulation method 2 (SVPWM2)

The second vector sequence, in this context named SVPWM2, is also applicable for the conventional space vector approach but contrary to the SVPWM1 method discussed above, the present sequence only utilizes one of the redundant switch states within a switching period [22, 47]. Considering sector $\mathbf{0_a}$, the half of the switching sequence is given by:

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{000} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+00} \quad \text{for} \quad \Delta_s < \frac{\pi}{6} \tag{5.29}$$

$$v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{000} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+00} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++0} \quad \text{for} \quad \Delta_s \geq \frac{\pi}{6} \tag{5.30}$$

Considering sector $\mathbf{0_b}$, the half of the switching sequence is given by:

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \tag{5.31}$$

Considering sector $\mathbf{0_c}$, the half of the switching sequence is given by:

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \quad \text{for} \quad \Delta_s < \frac{\pi}{6} \tag{5.32}$$

$$v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++0} \quad \text{for} \quad \Delta_s \geq \frac{\pi}{6} \tag{5.33}$$

And finally for sector $\mathbf{0_d}$, the half of the switching sequence is given by:

$$v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{++0} \tag{5.34}$$

Table III and Table IV summarize the sector- and angle dependent switch states. Sector **a** and sector **c** are divided into two sub-sectors, the first sub-sector being valid for the first half of the sector and the other being valid for the last half of the sector.

For some purposes an analytical expression for the modulation function is convenient and in general, the modulation function for the upper switch is given by eq. (5.23). However, the signal v_{1A}^* has to be shaped in a different way than signal generation applied for the

TABLE IV: *Switching table for modulation method 2 (Outer sectors).*

→Sector	b				c_1				c_2				d			
↓Even	δ_1	δ_2	δ_3	δ'_1	δ_1	δ_2	δ_3	δ'_1	δ_2	δ_3	δ_1	δ'_2	δ_2	δ_3	δ_1	δ'_2
0	0−−	+−−	+0−	+00	0−−	00−	+0−	+00	00−	+0−	+00	++0	00−	+0−	++−	++0
II	−0−	−+−	−+0	0+0	−0−	−00	−+0	0+0	−00	−+0	0+0	0++	−00	−+0	−++	0++
IV	−−0	−−+	0−+	00+	−−0	0−0	0−+	00+	0−0	0−+	00+	+0+	0−0	0−+	+−+	+0+
↓Odd	δ_1	δ_3	δ_2	δ'_1	δ_1	δ_3	δ_2	δ'_1	δ_2	δ_1	δ_3	δ'_2	δ_2	δ_1	δ_3	δ'_2
I	00−	0+−	++−	++0	00−	0+−	0+0	++0	−0−	00−	0+−	0+0	−0−	−+−	0+−	0+0
III	−00	−0+	−++	0++	−00	−0+	00+	0++	−−0	−00	−0+	00+	−−0	−−+	−0+	00+
V	0−0	+−0	+−+	+0+	0−0	+−0	+00	+0+	0−−	0−0	+−0	+00	0−−	+−−	+−0	+00

SVPWM1 method, c.f. eq. (5.26) and eq. (5.27). In case the modulation index M is less than $1/\sqrt{3}$, the signal v^*_{1A} is given by:

$$v^*_{1A} = \max\left(\begin{array}{c} \operatorname{sign}(3\omega_s t)\cdot\min\left(\begin{array}{c} \min\left(\begin{array}{c} -|v^*_{Am}| \\ -|v^*_{Bm}| \\ -|v^*_{Cm}| \end{array}\right) + \frac{1}{2} \\ v^*_{max} \\ -v^*_{min} \end{array}\right) \\ -2v^*_{Am} \end{array}\right) \tag{5.35}$$

while in case the modulation index M exceeds $1/\sqrt{3}$, the signal v^*_{1A} is given by:

$$v^*_{1A} = \max\left(\begin{array}{c} \operatorname{sign}(3\omega_s t)\cdot\max\left(\begin{array}{c} \left|\min\left(\begin{array}{c} -|v^*_{Am}| \\ -|v^*_{Bm}| \\ -|v^*_{Cm}| \end{array}\right) + \frac{1}{2}\right| \\ |v^*_{mid}| \end{array}\right) \\ -2v^*_{Am} \end{array}\right) \tag{5.36}$$

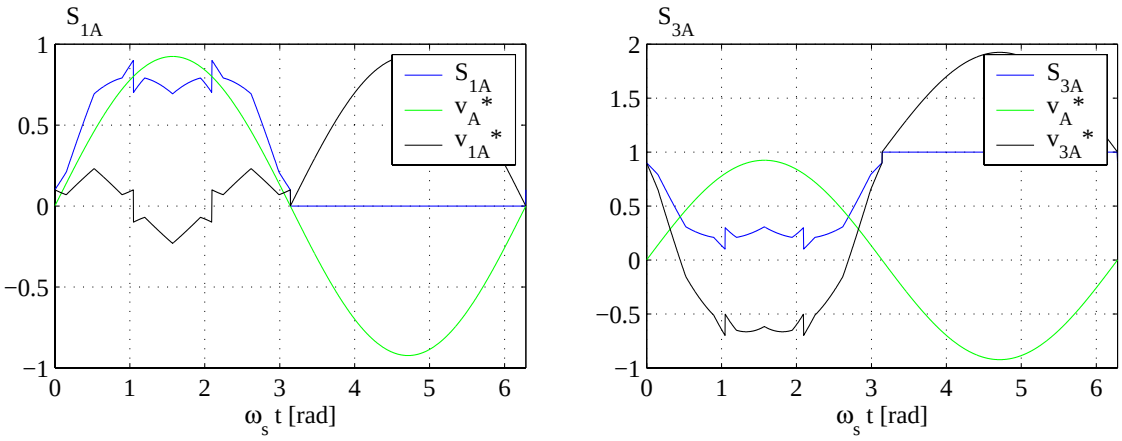
The modulation function S_{3A} is given by:

$$S_{3A} = \overline{S}_{1A} \tag{5.37}$$

Fig. 5.9a and Fig. 5.9b shows an example of the modulation functions S_{1A} and S_{3A} when the modulation index equals 0.8, i.e. Fig. 5.9a and Fig. 5.9b is an illustration of eq. (5.36) and eq. (5.37) respectively. Actually it turns out, that the space-vector approach given by the above described modulation method (SVPWM2) turns out to be identical with the carrier based modulation method discussed in [36].

Symmetrical flat top modulation (DPWM1)

Like for the two-level voltage source inverter, the redundant switching states can be used to omit switchings in one phase leg for a certain period [3]. To obtain this feature, each switching period has to prevent the use of redundant switch states. Unfortunately,



a) b)

Figure 5.9: *Modulation function ($M = 0.8$) for the SVPWM2 method.* **a)** *Modulation function for the upper switch S_{1A}.* **b)** *Modulation function for the center switch S_{3A}.*

as discussed in section 5.2.3, the three-level voltage source inverter may have a problem of a drifting DC-link neutral potential and normally this problem is solved by cleverly controlling the redundant switch states. However, at the present stage, ideal conditions are assumed, i.e. no drifting DC-link neutral potential, and the issue regarding DC-link balancing is left for section 5.3.5. The present modulation strategy clamps each phase leg around the peak of the phase voltage reference and hence, the present method can be used to minimize the switching losses when reference voltage and load current are in phase (or counter phase). The modulation method is applicable for the conventional space vector modulation approach. Considering sector $\mathbf{0_a}$, the half of the switching sequence is given by:

$$v_{+++} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{++0} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+00} \quad \text{for} \quad \Delta_s < \frac{\pi}{6} \tag{5.38}$$

$$v_{---} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{00-} \quad \text{for} \quad \Delta_s \geq \frac{\pi}{6} \tag{5.39}$$

Considering sector $\mathbf{0_b}$, the half of the switching sequence is given by:

$$v_{+--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \quad \text{for} \quad \Delta_s < \frac{\pi}{6} \tag{5.40}$$

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+0-} \quad \text{for} \quad \Delta_s \geq \frac{\pi}{6} \tag{5.41}$$

Considering sector $\mathbf{0_c}$, the half of the switching sequence is given by:

$$v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++0} \quad \text{for} \quad \Delta_s < \frac{\pi}{6} \tag{5.42}$$

$$v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+0-} \quad \text{for} \quad \Delta_s \geq \frac{\pi}{6} \tag{5.43}$$

And finally for sector $\mathbf{0_d}$, the half of the switching sequence is given by:

$$v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{++0} \quad \text{for} \quad \Delta_s < \frac{\pi}{6} \tag{5.44}$$

$$v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++-} \quad \text{for} \quad \Delta_s \geq \frac{\pi}{6} \tag{5.45}$$

Table V on page 170 summarizes the sector and angle dependent switching states for the symmetrical flat top modulation method. Since Table V is a general table valid for all the discontinuous modulation schemes, the angle ϕ'_s actually defines the type of discontinuous modulation. To obtain the symmetrical flat top modulation, the angle ϕ'_s equals zero. Table V further specify the DC-link balancing angle ϕ_c, but since the considerations so far assumes ideal conditions, this angle is zero. The DC-link balancing angle will be discussed in section 5.3.5.

For some implementation purposes as well as illustrative purposes it is convenient to have an analytical expression of the modulation function for the switches. In general, the modulation function S_{1A} for the upper switch is given by eq. (5.23) where the signal v^*_{1A} in the entire modulation range is given by:

$$v^*_{1A} = \max \begin{pmatrix} -2 \cdot \text{sign}(\sin(3\omega_s t)) \cdot \min \begin{pmatrix} -|v^*_{Am}| \\ -|v^*_{Bm}| \\ -|v^*_{Cm}| \end{pmatrix} + 1 \\ -2v^*_{Am} \end{pmatrix} \tag{5.46}$$

The modulation function for the center switch S_{3A} is given by:

$$S_{3A} = \overline{S}_{1A} \tag{5.47}$$

Fig. 5.10a and Fig. 5.10b illustrates the modulation signals for the upper switch S_{1A} and the center switch S_{3A} respectively, when the modulation index M is 0.8.

Asymmetrical shifted left flat top modulation (DPWM0)

Depending on the nature of the load (capacitive or inductive) the clamping interval can be moved forth and back compared to the symmetrical flat top modulation, thereby obtaining a further switching loss reduction. For a capacitive (or leading) current, the clamping interval will have to be moved to the left compared to the symmetrical flat top modulation - whereby the asymmetrical shifted left flat top modulation is obtained. The asymmetrical shifted left flat top modulation is applicable for the conventional space vector modulation. To exemplify the switching sequence for the asymmetrical shifted left flat top modulation, the half of the sequence for sector $\mathbf{0_a}$ is given by:

$$v_{+++} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{++0} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+00} \tag{5.48}$$

while the half of the switching sequence for sector $\mathbf{0_b}$, is given by:

$$v_{+--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \tag{5.49}$$

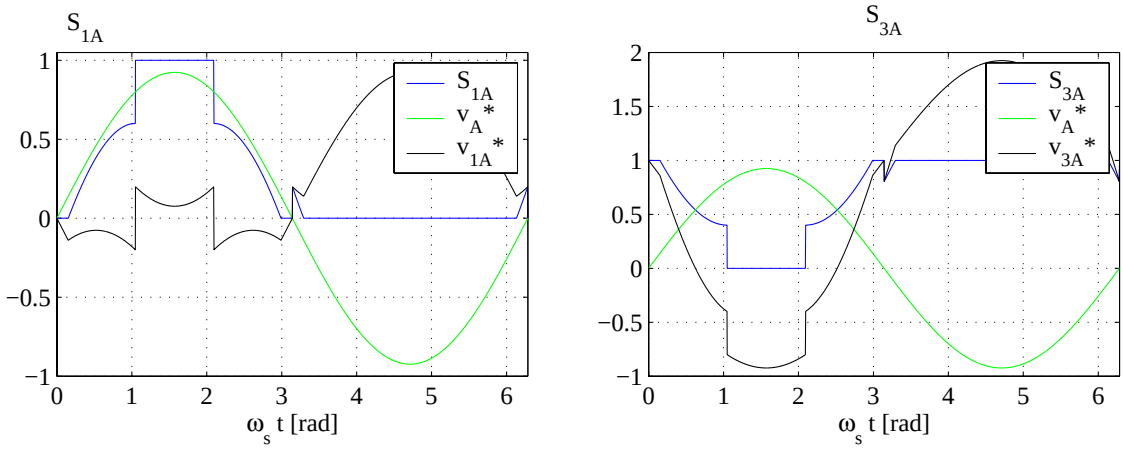


Figure 5.10: *Modulation function ($M = 0.8$) for the DPWM1 method.* **a)** *Modulation function for the upper switch S_{1A}.* **b)** *Modulation function for the center switch S_{3A}.*

Considering sector $\mathbf{0_c}$, the half of the switching sequence is given by:

$$v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{+00} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++0} \tag{5.50}$$

and finally for sector $\mathbf{0_d}$, the half of the switching sequence is given by:

$$v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{++-} \xrightarrow[\frac{1}{2}V_{DC}]{i_C} v_{++0} \tag{5.51}$$

Table V shows the switching sequences to be used in each of the sectors in the space vector hexagon, c.f. Fig. 5.5. Since Table V is a general table, common for all the discontinuous modulation methods, the parameter ϕ' (which actually determines the position of the clamping interval) has to be $\pi/6$ in order to obtain the asymmetrical shifted left flat top modulation.

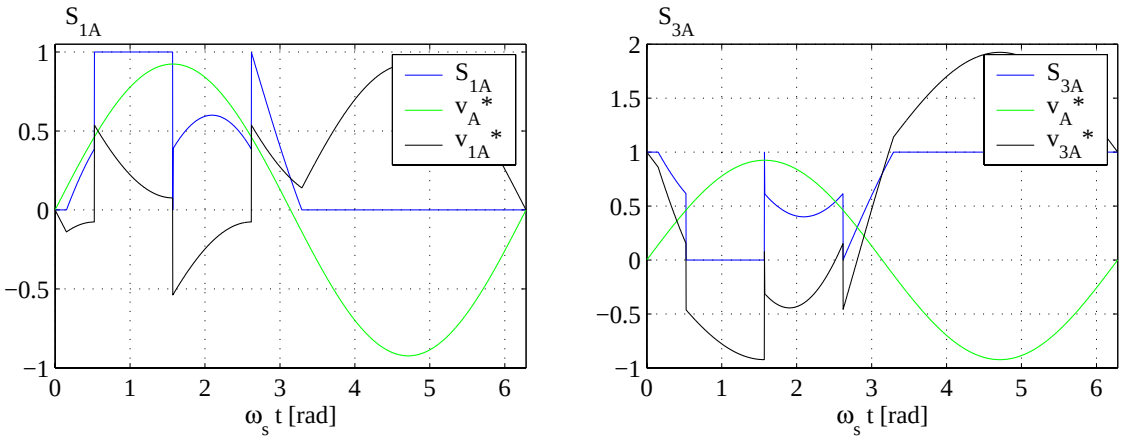
As for the previously discussed modulation methods, the carrier based version of the asymmetrical shifted left flat top modulation is simply given by eq. (5.23) but with the signal v_{1A}^* generated by:

$$v_{1A}^* = \max \left(\begin{array}{c} -2 \cdot \text{sign}(\sin(3\omega_s t)) \cdot \left(\begin{array}{c} v_{Cm}^* \text{ if } |v_{Am}^*| > |v_{Bm}^*| < |v_{Cm}^*| \\ v_{Am}^* \text{ if } |v_{Am}^*| > |v_{Cm}^*| < |v_{Bm}^*| \\ v_{Bm}^* \text{ if } |v_{Bm}^*| > |v_{Am}^*| < |v_{Cm}^*| \end{array} \right) \\ -2v_{Am}^* \end{array} \right) \tag{5.52}$$

The modulation function S_{3A} for the center switch is then given by:

$$S_{3A} = \overline{S}_{1A} \tag{5.53}$$

Fig. 5.11a and Fig. 5.11b illustrates the modulation signals for the upper switch S_{1A} and the center switch S_{3A} respectively, when the modulation index M is 0.8.



a) b)

Figure 5.11: *Modulation function ($M = 0.8$) for the DPWM0 method.* **a)** *Modulation function for the upper switch S_{1A}.* **b)** *Modulation function for the center switch S_{3A}.*

Asymmetrical shifted right flat top modulation (DPWM2)

The last discontinuous modulation method to be treated in this section is the method named asymmetrical shifted right flat top modulation. As the name implies, the clamping interval is shifted to the right making this modulation method suitable for an inductive load, i.e. a lagging current. The asymmetrical shifted right modulation method is applicable for the conventional space vector modulation. Considering the half of the vector sequence for sector $\mathbf{0_a}$:

$$v_{---} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{0--} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{00-} \tag{5.54}$$

while the half of the switching sequence for sector $\mathbf{0_b}$, is given by:

$$v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+--} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{0--} \tag{5.55}$$

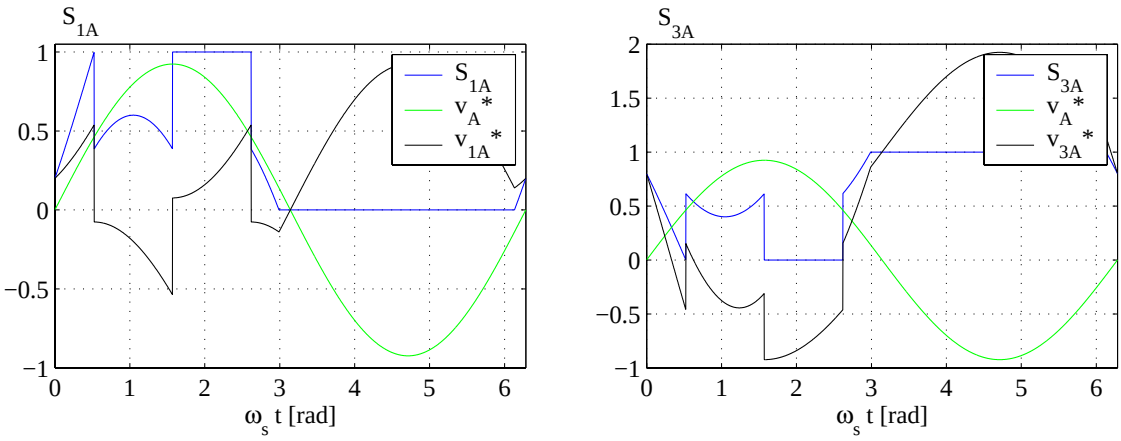
Considering sector $\mathbf{0_c}$, the half of the switching sequence is given by:

$$v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{00-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{0--} \tag{5.56}$$

And finally for sector $\mathbf{0_d}$, the half of the switching sequence is given by:

$$v_{++-} \xrightarrow[\frac{1}{2}V_{DC}]{i_B} v_{+0-} \xrightarrow[\frac{1}{2}V_{DC}]{i_A} v_{00-} \tag{5.57}$$

Table V shows the switching sequences to be used in each of the sectors in the space vector hexagon, c.f. Fig. 5.5. Since Table V is a general table, common for all the discontinuous modulation methods, the parameter ϕ' (which actually determines the position of the clamping interval) has to be $-\pi/6$ in order to obtain the asymmetrical shifted right flat top modulation.



a) b)

Figure 5.12: *Modulation function ($M = 0.8$) for the DPWM2 method.* **a)** *Modulation function for the upper switch S_{1A}.* **b)** *Modulation function for the center switch S_{3A}.*

The signal v^*_{1A} for the asymmetrical shifted right flat top modulation is generated by:

$$v^*_{1A} = \max \left(\begin{array}{c} -2 \cdot \text{sign}(\sin(3\omega_s t)) \cdot \left(\begin{array}{c} v^*_{Bm} \text{ if } |v^*_{Am}| > |v^*_{Bm}| < |v^*_{Cm}| \\ v^*_{Cm} \text{ if } |v^*_{Am}| > |v^*_{Cm}| < |v^*_{Bm}| \\ v^*_{Am} \text{ if } |v^*_{Bm}| > |v^*_{Am}| < |v^*_{Cm}| \end{array} \right) \\ -2v^*_{Am} \end{array} \right) \tag{5.58}$$

and the modulation function for the middle switch S_{3A} is then given by:

$$S_{3A} = \overline{S}_{1A} \tag{5.59}$$

Fig. 5.12a and Fig. 5.12b illustrates the modulation signals for the upper switch S_{1A} and the center switch S_{3A} respectively, when the modulation index M is 0.8.

The latter three modulation methods - known as the discontinuous modulation methods can be generalized in such a way that the clamping interval continuously tracks the current amplitude in order to minimize the switching losses [15, 16]. Further, this generalized method and its ability to balance the DC-link is discussed in the publication *"Generalized Discontinuous DC-link Balancing Modulation Strategy for Three-level Inverters"* [11], c.f. Enclosure F.

Vector sequence for common mode voltage elimination (CMPWM)

The last vector sequence to be treated for the three level inverter is a vector sequence applicable for the space vector modulation with common mode voltage elimination. According to the space vector hexagon in Fig. 5.6 and the switching vectors forming the hexagon, there is no *smart* way to arrange the switching vectors in order to minimize the number of switchings. Actually in each of the six sectors, a shift between any of the three adjacent vectors involve two switchings and hence the ordering of the switching

TABLE V: *Switching table for the discontinuous modulation methods.*

→**Sub sector**	**a**			**b**			**c**			**d**		
↓ **if** $\Delta_s \leq \frac{\pi}{6}+\phi'+n\cdot\phi_c$	δ_3	δ_1	δ_2	δ_2	δ_3	δ_1	δ_3	δ_1	δ_2	δ_3	δ_1	δ_2
Sector 0	+++	+00	++0	+−−	+0−	+00	+0−	+00	++0	+0−	++−	++0
Sector I	−−−	00−	−0−	++−	0+−	00−	0+−	00−	−0−	0+−	−+−	−0−
Sector II	+++	0+0	0++	−+−	−+0	0+0	−+0	0+0	0++	−+0	−++	0++
Sector III	−−−	−00	−−0	−++	−0+	−00	−0+	−00	−−0	−0+	−−+	−−0
Sector IV	+++	00+	+0+	−−+	0−+	00+	0−+	00+	+0+	0−+	+−+	+0+
Sector V	−−−	0−0	0−−	+−+	+−0	0−0	+−0	0−0	0−−	+−0	+−−	0−−
↓ **if** $\Delta_s > \frac{\pi}{6}+\phi'+n\cdot\phi_c$	δ_3	δ_2	δ_1	δ_3	δ_2	δ_1	δ_3	δ_2	δ_1	δ_1	δ_3	δ_2
Sector 0	−−−	00−	0−−	+0−	+−−	0−−	+0−	00−	0−−	++−	+0−	00−
Sector I	+++	0+0	++0	0+−	++−	++0	0+−	0+0	++0	−0−	0+−	0+0
Sector II	−−−	−00	−0−	−+0	−+−	−0−	−+0	−00	−0−	−++	−+0	−00
Sector III	+++	00+	0++	−0+	−++	0++	−0+	00+	0++	−−+	−0+	00+
Sector IV	−−−	0−0	−−0	0−+	−−+	−−0	0−+	0−0	−−0	+−+	0−+	0−0
Sector V	+++	+00	+0+	+−0	+−+	+0+	+−0	+00	+0+	+−−	+−0	+00

TABLE VI: *Switching table for modulation method with common-mode voltage elimination.*

↓**Even**	δ_1	δ_2	δ_3
0	+−0	+0−	000
I	+0−	0+−	000
II	0+−	−+0	000
III	−+0	−0+	000
IV	−0+	0−+	000
V	0−+	+−0	000

sequence with regard to switching losses does not matter very much. The half of the switching sequence for sector **0** is:

$$v_{000} \longrightarrow v_{+-0} \longrightarrow v_{+0-} \longrightarrow v_{000} \tag{5.60}$$

Table VI summarizes the sector dependent switching sequences. To obtain the carrier based modulation method with common-mode voltage elimination is a little more tricky than the preceding methods as each transition between switch states involves two switchings. A method for handling this particular issue was proposed in [44] using two intermediate reference signals to generate modulation signals for one phase. These two intermediate reference signals are in fact the sine wave reference signals for the two remaining phases shifted by $\pi/2$. The intermediate reference signals are then compared to the triangular carrier and finally the two obtained intermediate PWM signals are then subtracted by which the gate signals for considered phase is obtained. For further explanation, see [44].

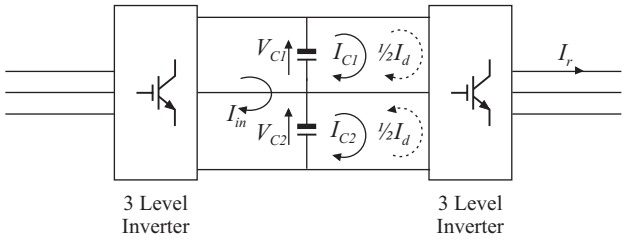


Figure 5.13: *Definitions of the currents and voltages used for DC-link balancing.*

5.3.5 DC-link balancing techniques

As discussed previously, the balance of the DC-link can either be performed by a hardware modification or by making use of the redundant switch states. In this thesis only the latter method will be treated. This actually implies a slight modification of the modulation schemes discussed so far. For the purpose of explaining the DC-link balancing approaches Fig. 5.13 illustrates the loading of the DC-link when considering only one of the inverters in the back-to-back three-level converter. Using the current definitions in Fig. 5.13, it appears that DC-link voltage equilibrium is obtained when the following condition is satisfied:

$$\begin{aligned} \langle I_{C1}\rangle_{T_0} + \frac{1}{2}\langle I_d\rangle_{T_0} &= \langle I_{C2}\rangle_{T_0} - \frac{1}{2}\langle I_d\rangle_{T_0} \\ \Downarrow & \\ \langle I_d\rangle_{T_0} &= \langle I_{C2}\rangle_{T_0} - \langle I_{C1}\rangle_{T_0} \end{aligned} \tag{5.61}$$

where I_{C1} and I_{C2} are the DC-link currents originating from the linear balanced load of the three level inverter and I_d represents the unbalanced loading of the inverter. The notation $\langle X\rangle_{T_0}$ indicates that the quantity is averaged over a time period T_0. From eq. (5.61) it appears that an imbalance may be compensated by adjusting the ratio between $\langle I_{C1}\rangle_{T_0}$ and $\langle I_{C2}\rangle_{T_0}$. However, dependent on the considered modulation method there are major differences in the way such DC-link balancing feature can be implemented. Actually three different approaches have to be considered, one for the continuous modulation methods, another for the discontinuous methods and finally a third approach for the method with common mode voltage elimination.

Continuous modulation schemes

Considering the continuous modulation schemes. i.e. the space vector modulation method 1 (SVPWM1) and the space vector modulation method 2 (SVPWM2) it appears that within each switching cycle, the modulation schemes are able to perform a balancing action by adjusting the ratio between the different redundant switch vectors, i.e. the ratio between the switch states marked in green and red respectively in Table I - Table IV. Referring to Table I - Table IV the DC-link balancing can be implemented by:

$$\underline{V}_s = k_1 \cdot (\delta_1 \cdot \underline{V}_1 + \delta_2 \cdot \underline{V}_2)) + k_2 \cdot (\delta_1' \cdot \underline{V}_1 + \delta_2' \cdot \underline{V}_2)) + \delta_3 \underline{V}_3 \tag{5.62}$$

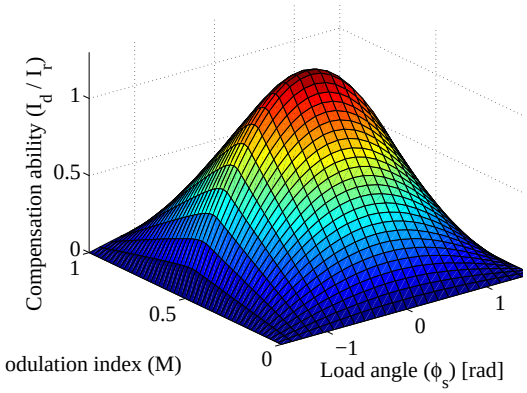


Figure 5.14: *DC-link load imbalance for which the modulation scheme SVPWM1 is able to compensate.*

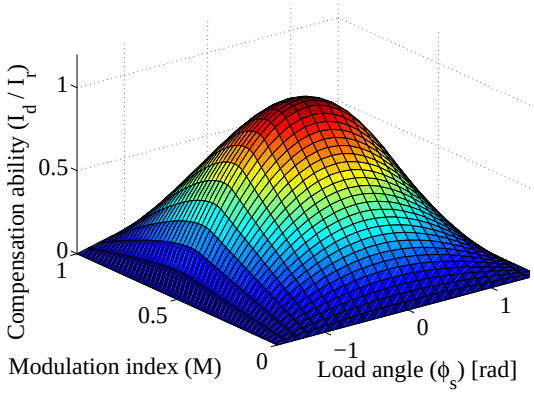


Figure 5.15: *DC-link load imbalance for which the modulation scheme SVPWM2 is able to compensate.*

In a physical implementation, a PI-controller may be used to adjust the ratio between k_1 and k_2 based on the degree of imbalance [20].

To evaluate the ability of the above explained DC-link balancing technique, the current through capacitor C_1 and C_2 have to be calculated for the extreme situation where k_1 equals 1 and k_2 equals 0 (or vice versa). Eq. (5.65) is only formulated for modulation method SVPWM1 with the voltage reference vector located in sector $\mathbf{0_a}$:

$$\begin{aligned} \langle I_{C1}\rangle_{T0} &= \frac{1}{2\pi}\left(k_2\int_0^{\frac{\pi}{3}}(\delta_1\cdot i_A-\delta_2\cdot i_C)d\Delta_s+....\right. \\ \langle I_{C2}\rangle_{T0} &= \frac{1}{2\pi}\left(k_1\int_0^{\frac{\pi}{3}}(\delta_1\cdot i_A-\delta_2\cdot i_C)d\Delta_s+....\right. \end{aligned} \tag{5.63}$$

Extending eq. (5.63) to arbitrary values of the modulation index M, the maximum imbalance, for which the continuous modulation schemes are able to compensate can be calculated. Fig. 5.14 shows the ability of the SVPWM1 modulation scheme to compensate DC-link imbalance. Similar, Fig. 5.15 shows the ability of the SVPWM2 modulation scheme to compensate DC-link imbalance. In Fig. 5.14 and Fig. 5.15 the unbalanced current I_d is normalized to the output current I_r originating from the linear loading of the inverter and plotted against the modulation index M and load angle ϕ. In terms of DC-link balancing ability it appears that the SVPWM1 method has up to 30% better performance compared to the SVPWM2 method due to the use of double redundant switch states in sector **a** and sector **c**.

Discontinuous modulation schemes

Unlike the continuous modulation methods, i.e. SVPWM1 and SVPWM2, the discontinuous modulation methods do not allow the use of redundant switch states within a

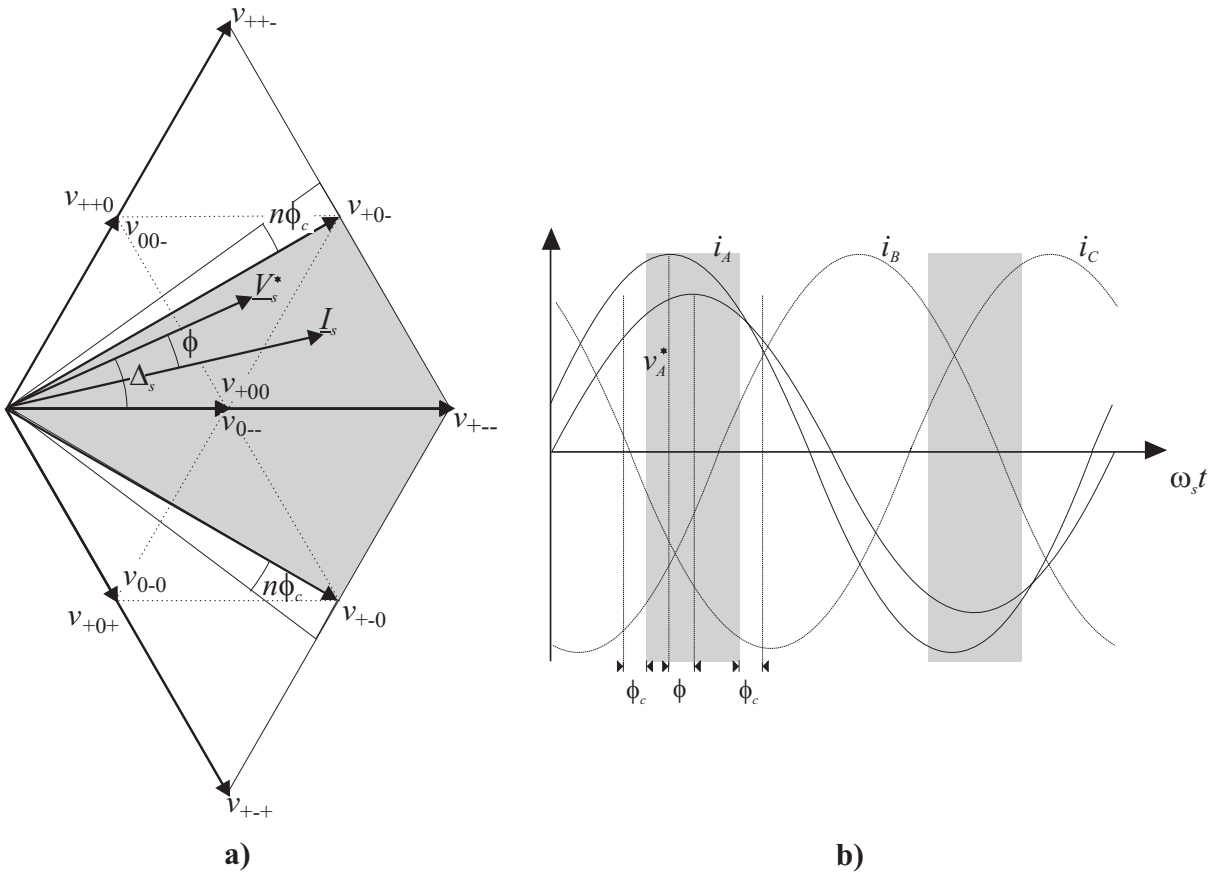


Figure 5.16: *Definitions of the DC-link balancing angle ϕ_c.* **a)** *in the complex space vector domain.* **b)** *in the time domain.*

TABLE VII: *Definition of the sign operator n.*

	a	**b**	**c**	**d**
Even Sec.	-Sign(P_o)	Sign(P_o)	Sign(P_o)	Sign(P_o)
Odd Sec.	Sign(P_o)	-Sign(P_o)	-Sign(P_o)	-Sign(P_o)

switching period and hence the DC-link cannot be stabilized during a switching period. As an alternative, the length of the clamping interval may be used to alter the loading of the upper and lower DC-link capacitors. For this purpose, the angle $n \cdot \phi_c$ is introduced, c.f. Fig. 5.16, where the sign operator n is defined in accordance with Table VII and ϕ_c is defined in the interval $\phi_c \in [-\frac{\pi}{6}..\frac{\pi}{6}]$. From Fig. 5.16, Table V and Table VII it appears that by increasing/decreasing the angle ϕ_c, the load on capacitor C_1 can be increased/decreased. Hence, the angle ϕ_c can be used to compensate unbalanced loading of the DC-link. Adjusting the clamping interval according to Fig. 5.16 makes it necessary also to adjust the angle ϕ' defining the center of the clamping interval - at

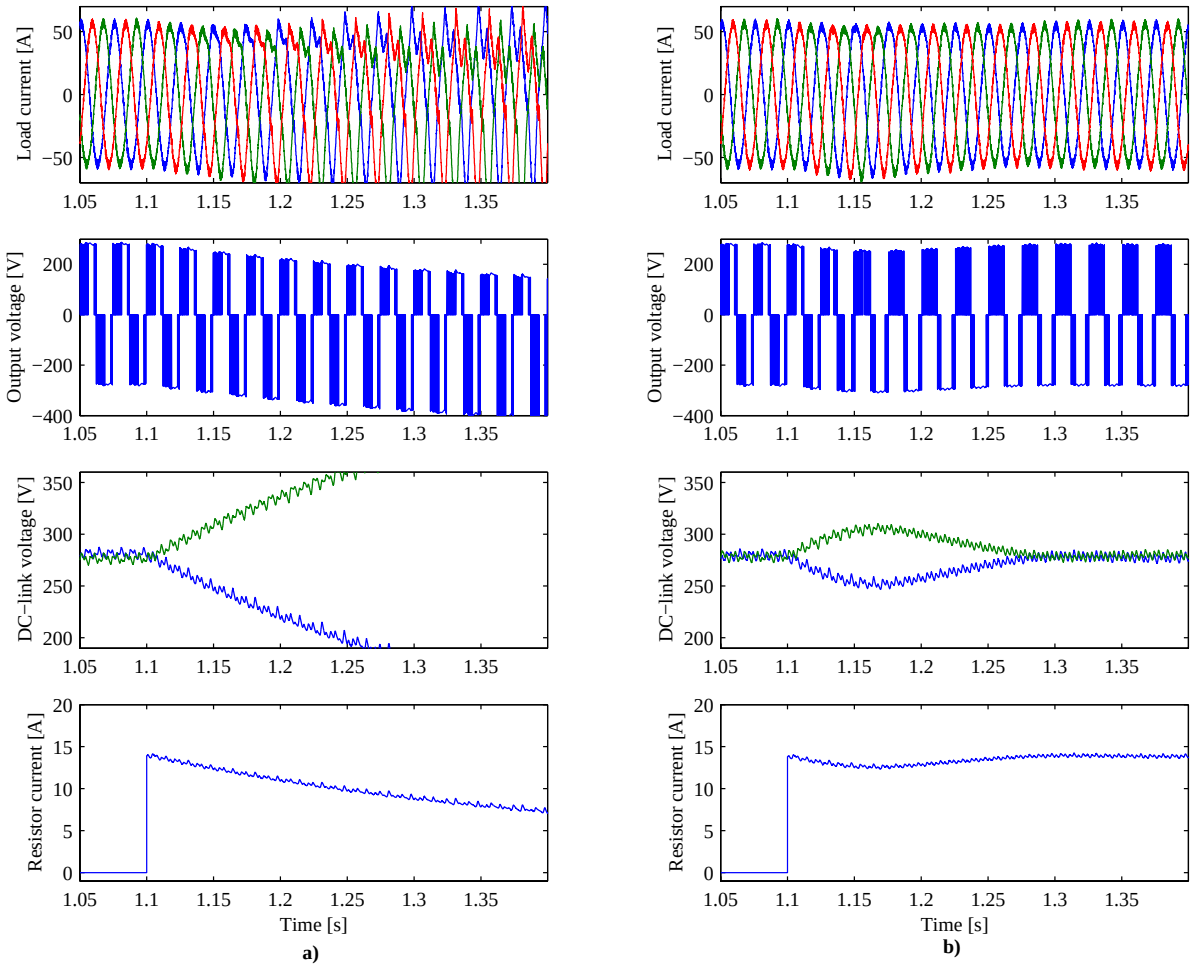


Figure 5.17: *Simulation results.* **a)** *Simulation results without DC-link compensation.* **b)** *Simulation results with the DC-link balancing technique applied.*

least for the asymmetrical modulation methods. The angle ϕ' is given by:

$$\phi' = \begin{cases} \frac{\pi}{6} - \phi_c & \text{For DPWM0} \\ 0 & \text{For DPWM1} \\ -\frac{\pi}{6} + \phi_c & \text{For DPWM2} \end{cases} \tag{5.64}$$

To demonstrate the functionality of the proposed DC-link balancing method for the discontinuous modulation methods the three-level inverter was simulated. Fig. 5.17a shows a simulation of the effect of an unbalanced loading of the DC-link without compensating the imbalance. At time ($t = 1.1$), an unbalanced loading is introduced. Due to the unbalanced load between capacitor C_1 and C_2, the voltage at the center point N starts to drift towards the voltage of the positive bus-bar. The upper plot in Fig. 5.17a shows the phase current, the upper middle plot shows the voltage v_{aN}, the lower middle plot shows the voltages across capacitor C_1 and capacitor C_2 while the lower plot shows the current through the resistor used to establish the imbalance. Applying the proposed modulation technique for DC-link balancing, the voltage in the center-point N can be

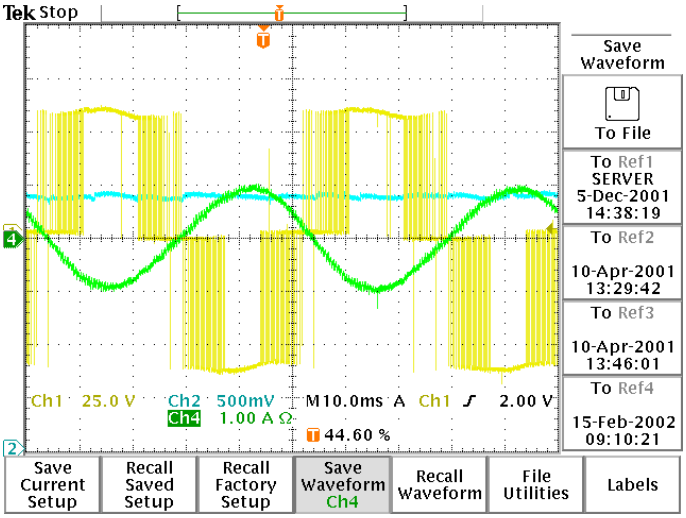


Figure 5.18: *Measured waveforms for the proposed DC-link balancing method applicable for the discontinuous modulation schemes.*

re-established. Fig 5.17b shows the effects of an unbalanced loading, similar to the case in Fig. 5.17a, where the proposed balancing technique is applied. From Fig. 5.17b it clearly appears that the clamping interval of the upper and lower transistors are changed and the DC-link neutral point is re-established despite the heavy unbalanced loading of the DC-link. To further demonstrate the proposed DC-link balancing method, the scheme was implemented in an experimental test setup. Fig. 5.18 shows the measured phase voltage (-), the inverter load current (-) and the DC-link voltage (-) when an unbalanced loading of the DC-link capacitors was introduced, i.e. a resistor loading the lower DC-link capacitor. From Fig. 5.18 it also appears that the clamping interval of the upper and lower transistors are different in order to compensate the DC-link imbalance.

To evaluate the ability of the proposed DC-link balancing technique, the current through capacitor C_1 and C_2 have to be calculated. Eq. (5.65) is only formulated for sector $\mathbf{0_a}$ and further it is provided that the modulation index is below 0.5:

$$\begin{aligned} \langle I_{C1}\rangle_{T0} &= \frac{1}{2\pi}\left(\int_{\frac{\pi}{6}+\phi'+n\phi_c}^{\frac{\pi}{6}} (\delta_1 \cdot i_A - \delta_2 \cdot i_C) d\Delta_s + ... \right. \\ \langle I_{C2}\rangle_{T0} &= \frac{1}{2\pi}\left(\int_{0}^{\frac{\pi}{6}+\phi'+n\phi_c} (\delta_1 \cdot i_A - \delta_2 \cdot i_C) d\Delta_s + ... \right. \end{aligned} \tag{5.65}$$

Extending 5.65 to arbitrary values of the modulation index M, and calculating for $\phi_c = \pm\frac{\pi}{6}$ the maximum imbalance, for which the modulation scheme is able to compensate may be calculated. Fig. 5.19 shows the ability of the proposed modulation scheme to compensate DC-link imbalance. In Fig. 5.19 the unbalanced current I_d is normalized to the output current I_r originating from the linear loading of the inverter and plotted

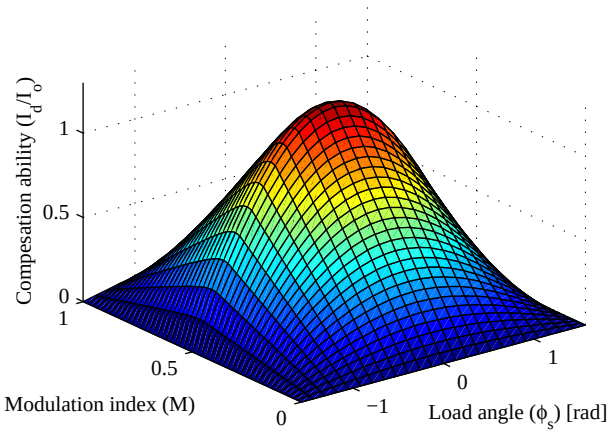


Figure 5.19: *DC-link load imbalance for which the discontinuous modulation schemes are able to compensate.*

against the modulation index M and load angle ϕ. For a more detailed explanation of the DC-link balancing strategy for discontinuous modulation methods, is referred to the paper *"Generalized Discontinuous DC-link Balancing Modulation Strategy for Three-level Inverters"* [11], c.f. Enclosure F.

Modulation scheme with common mode elimination

So far the modulation scheme with common mode voltage elimination is equal to the modulation scheme described by [31] and [44] but since no redundant switch states are used within a switching period, DC-link balancing can not be obtained by adjusting the on-times for such redundant switch states. Instead, a kind of redundancy can be introduced by using three active vectors to form the reference vector $\underline{V}_s$. This is illustrated in Fig. 5.20. By use of three vectors the freedom to choose either vector $\underline{V}'_3$ or vector $\underline{V}''_3$ is obtained. By inspection of Fig. 5.6 it appears that the voltage vectors $\underline{V}'_3$ and $\underline{V}''_3$ for all sectors charges the DC-link capacitors in opposite manners. By this, the use of either $\underline{V}'_3$ or $\underline{V}''_3$ can be used to control the DC-link voltages. According to Fig. 5.20 the reference vector $\underline{V}^\star_s$ is synthesized by:

$$\underline{V}^\star_s = \delta_1 \cdot \underline{V}_1 + \delta_2 \cdot \underline{V}_2 + \delta_3 \cdot \underline{V}_3 + \delta_0 \cdot \underline{V}_0 \tag{5.66}$$

where $\underline{V}_3$ can be either $\underline{V}'_3$ or $\underline{V}''_3$. Independent of the choice of vector $\underline{V}'_3$ or $\underline{V}''_3$ the on-time ratio δ_3 is calculated by:

$$\delta_3 \;=\; k \cdot (1 - \delta'_1 - \delta'_2) \tag{5.67}$$

where k is a constant proportional to the degree of imbalance. The calculations of the duty-cycles δ_1 and δ_2 depends on the choice of vector $\underline{V}_3$. If $\underline{V}'_3$ is be used to compensate

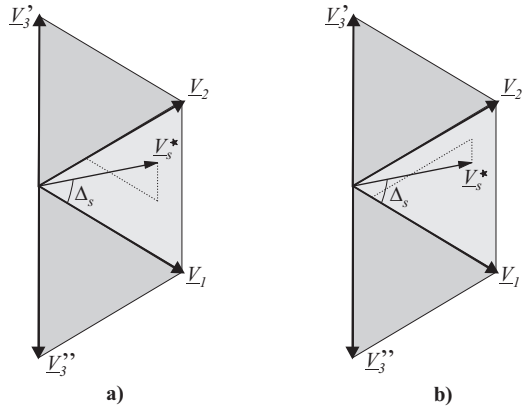


Figure 5.20: *Illustration of the proposed DC-balancing technique.* **a)** *Using voltage vector* $\underline{V}_3'$. **b)** *Using voltage vector* $\underline{V}_3''$.

DC-link imbalance, the duty-cycles δ_1 and δ_2 becomes:

$$\begin{aligned} \delta_1 &= \delta_1' + \delta_3 \\ \delta_2 &= \delta_2' - \delta_3 \end{aligned} \tag{5.68}$$

where δ_1' and δ_2' refer to the duty-cycles calculated without considering any unbalanced conditions, c.f. section 5.3.2. Complying with the restriction in (5.16) the limit for k becomes dependent of the modulation depth M and the angular position of the voltage reference vector. Combining (5.15) and (5.67) the limit for k when using voltage vector $\underline{V}_3'$ becomes:

$$1 \geq \hat{k} \leq \frac{M \cdot \sin(\Delta_s')}{1 - M \cdot \left(\sin\left(\frac{\pi}{3} - \Delta_s'\right) + \sin(\Delta_s')\right)} \tag{5.69}$$

If the unbalanced condition requires voltage vector $\underline{V}_3''$ to be used, the duty-cycles δ_1 and δ_2 becomes:

$$\begin{aligned} \delta_1 &= \delta_1' - \delta_3 \\ \delta_2 &= \delta_2' + \delta_3 \end{aligned} \tag{5.70}$$

Again, complying with the restriction in (5.16) the limit for k becomes:

$$1 \geq \hat{k} \leq \frac{M \cdot \sin\left(\frac{\pi}{3} - \Delta_s'\right)}{1 - M \cdot \left(\sin\left(\frac{\pi}{3} - \Delta_s'\right) + \sin(\Delta_s')\right)} \tag{5.71}$$

The on-time ratio for the zero vector is finally calculated by:

$$\delta_0 = 1 - \delta_1 - \delta_2 - \delta_3 \tag{5.72}$$

By the restrictions on k formulated in (5.69) and (5.71) the voltage gain ratio of the proposed modulation scheme is not further reduced and the DC-link voltage can be

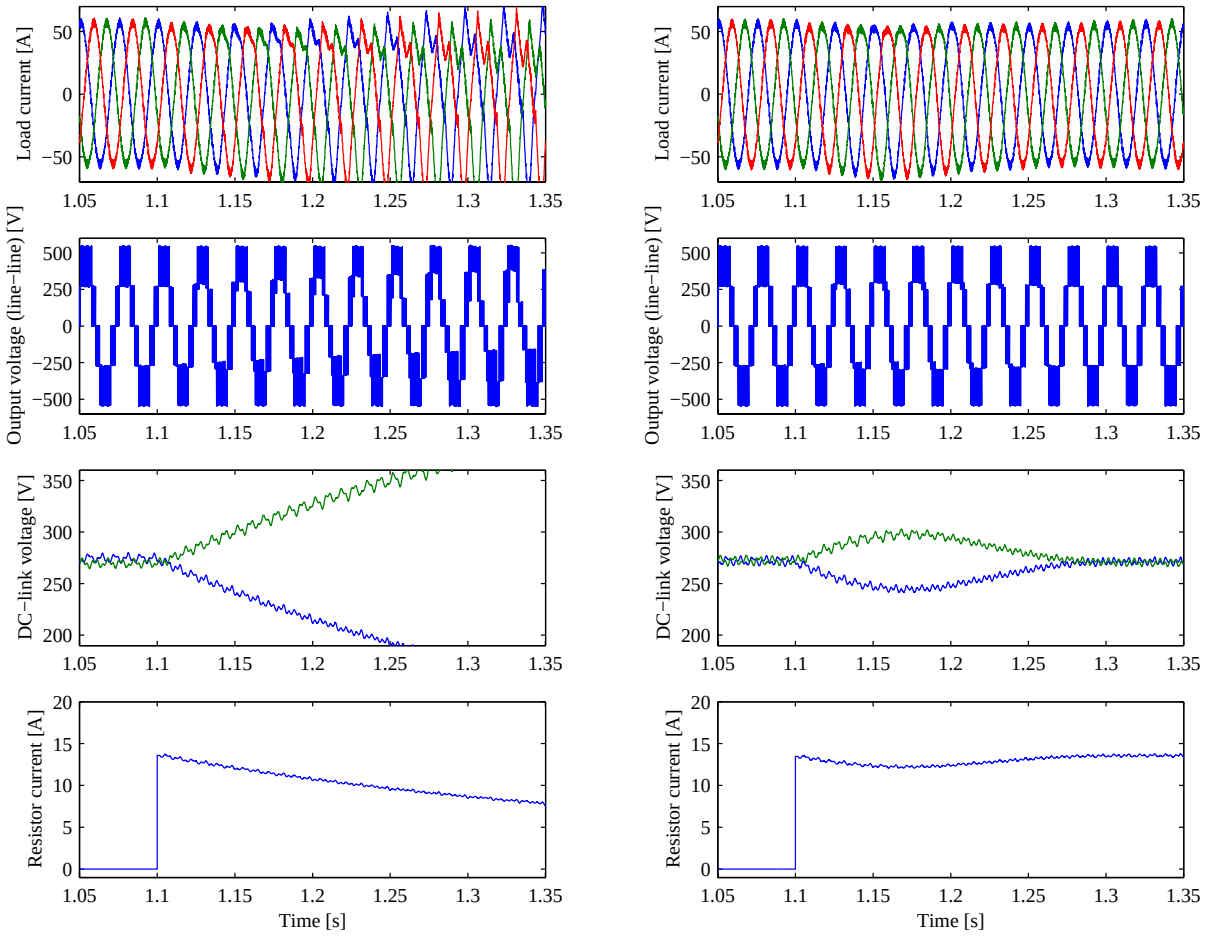


Figure 5.21: *Simulation results.* **a)** *Simulation results without DC-link compensation.* **b)** *Simulation results with the DC-link balancing technique applied.*

balanced, even if an un-balanced loading of the DC-link capacitors occur. Fig. 5.21a shows the effect of an unbalanced loading of the DC-link without compensating the unbalance. At time ($t = 1.1$), a resistor is connected across capacitor C_1. Due to the unbalanced load between capacitor C_1 and C_2, the voltage at the center point N starts to drift towards the voltage of the positive bus-bar. The upper plot in Fig. 5.21a shows the phase current, the upper middle plot shows the voltage v_{ab}, lower middle plot shows the voltages across capacitor C_1 and capacitor C_2 while the lower plot shows the current through the resistor used to establish the DC-link imbalance. Applying the proposed modulation technique for DC-link balancing, the voltage in the center-point N can be re-established. Fig 5.21b shows the effects of an unbalanced loading, similar to the case in Fig. 5.21a, where the proposed balancing technique is applied.

To evaluate the ability of the proposed DC-link balancing technique, the current through capacitor C_1 and C_2 have to be calculated. Eq. (5.73) is only formulated for sector 0

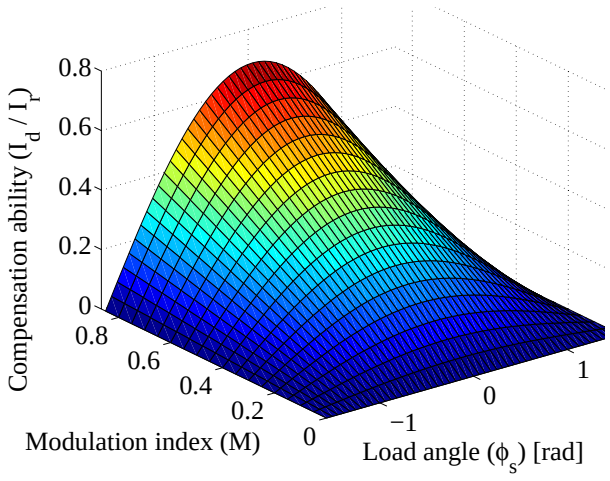


Figure 5.22: *DC-link load imbalance for which the CMPWM modulation scheme is able to compensate.*

and only valid when using voltage vector V_3' for DC-link balancing:

$$\begin{aligned} \langle I_{C1}\rangle_{T0} &= \frac{1}{2\pi}\left(\int_0^{\frac{\pi}{3}}(\delta_1\cdot i_A+\delta_2\cdot i_A+d_3\cdot i_B)d\Delta_s'+....\right. \\ \langle I_{C2}\rangle_{T0} &= \frac{1}{2\pi}\left(\int_0^{\frac{\pi}{3}}(\delta_1\cdot i_C+\delta_2\cdot i_B+d_3\cdot I_A)d\Delta_s'+....\right. \end{aligned} \tag{5.73}$$

Extending eq. (5.73) to include all six sectors the maximum imbalance, for which the modulation scheme is able to compensate can be calculated. Fig. 5.22 shows the ability of the proposed modulation scheme to compensate DC-link imbalance. In Fig. 5.22 the unbalanced current I_d is normalized to the output current I_r originating from the linear loading of the inverter and plotted against the modulation index M and load angle ϕ. For a more detailed explanation of the DC-link balancing strategy for the modulation method with common mode voltage elimination, is referred to the paper *"Modulation Scheme with Common Mode-Voltage Elimination and DC-link Balancing for Three-Level Inverters"*, c.f. Enclosure G.

5.3.6 Evaluation of the modulation methods

From the preceding sections, it appears that the discussed modulation methods involve different numbers of switch states in each switching period and hence it is likely to expect that the modulation methods have different salient properties. When considering modulation methods for the three-level voltage source inverter the following four properties are important, - the harmonic performance, the switching losses, the conducting losses and the DC-link balancing capability. In this section, the harmonic content for the different modulation methods are evaluated in order to be able to select a switching frequency which for a certain modulation method generates an acceptable harmonic content. The switching losses and conducting losses and their relation to the selected

modulation method are discussed in section 5.4 while the DC-link balancing capability were discussed in section 5.3.5.

Harmonic performance

When modulating the three-level converter in order to synthesize a desired output voltage, harmonics are introduced at integer multiples of the switching frequency and at the side bands of all these frequencies. The harmonic content depends on the chosen modulation scheme and since this undesirable frequency content causes torque ripple and additional copper losses in the generator (or any other load connected thereto), it is convenient to have a method to compare the harmonic behavior of different modulation schemes. In general, harmonic analysis can be done by either FFT or harmonic flux distortion (HFD). For a quantitative analysis, HFD is most suitable and hence the proposed modulation scheme is evaluated with regards to the HFD.

In the N$^{\text{th}}$ carrier cycle the harmonic flux $\tilde{\psi}$ is calculated by:

$$\tilde{\psi} = \int_{NT_s}^{(N+1)T_s} (\underline{V}_s - \underline{V}_s^{\star}) dt \tag{5.74}$$

where $\underline{V}_s$ is a stationary output voltage vector. To generalize the performance characterization, the per carrier harmonic flux error $\tilde{\psi}$ in eq. (5.74), is normalized to the product of the nominal output voltage amplitude $|\underline{\hat{V}}_s^*|$ and the switching period T_s. That is:

$$\tilde{\psi}_n = \frac{1}{T_s|\underline{\hat{V}}_s^*|} \cdot \tilde{\psi} \tag{5.75}$$

The normalized per-carrier cycle RMS value of the harmonic flux $\tilde{\psi}_{RMS,n}$ can now be calculated by:

$$\langle \tilde{\psi}_{RMS,n} \rangle_{T_s} = \sqrt{\int_0^1 \left(\tilde{\psi}_n \cdot \tilde{\psi}_n^* \right) dt} \tag{5.76}$$

where $\tilde{\psi}_n^*$ is the complex conjugate of $\tilde{\psi}_n$. Due to the six fold symmetry of the space-vector modulation, the per fundamental RMS harmonic flux may be calculated by:

$$\tilde{\psi}_{RMS,n} = \sqrt{\frac{3}{\pi} \int_0^{\frac{\pi}{3}} \left(\langle \tilde{\psi}_{RMS,n} \rangle_{T_s} \right)^2 d\Delta_s} \tag{5.77}$$

Fig. 5.23 shows the RMS-value of the harmonic flux as a function of the modulation index for the different modulation methods. It is worthwhile to notice, that the harmonic flux levels in Fig. 5.23 is directly comparable with the calculated harmonic flux levels of the back-to-back two-level voltage source converter shown in Fig. 3.11 on page 59 and the harmonic flux levels of the matrix converter shown in Fig. 4.22 on page 116. For instance, the dotted line in Fig. 5.23 indicates the harmonic flux distortion for the two-level inverter when using the suboptimal modulation method. The evaluated harmonic flux distortions in Fig. 5.23 can be used to decide an appropriate switching frequency dependent on the chosen modulation method and nominal modulation index. This issue is discussed in section 5.5.4.

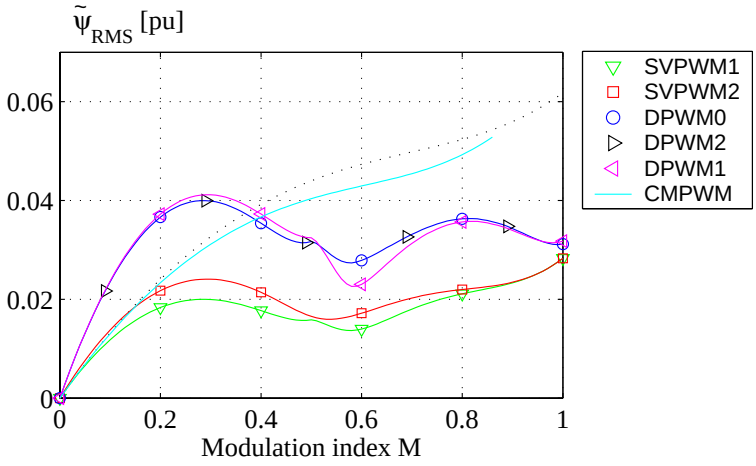


Figure 5.23: *Evaluation of the modulation methods for the multi-level converter.*

5.4 Loss evaluation

As it appeared from the discussion of the different modulation methods, the converter losses and to some extent the loss distribution over time depends on the chosen modulation strategy, the modulation index M and the load angle ϕ. In order to be able to evaluate this dependency in an RMS value model, analytical expressions have to be established for both the conducting losses and the switching losses. The purpose of this section is to derive these analytical expressions.

5.4.1 Conducting losses of the switches

Like for the previously considered converter topologies, the conducting losses of a semiconductor device, i.e. transistor or diode, are simply modeled by [40]:

$$P_{t,cond} = V_{t0}(T) \cdot I_{t,avg} + R_t(T) \cdot I_t^2 \tag{5.78}$$

$$P_{d,cond} = V_{d0}(T) \cdot I_{d,avg} + R_d(T) \cdot I_d^2 \tag{5.79}$$

where $I_{x,avg}$ is the average current through the considered component, I_x is the RMS current through the considered component, $V_{x0}(T)$ is the temperature dependent threshold voltage of the considered component and $R_{x0}(T)$ is the temperature dependent resistance of the considered component. The threshold voltage and on-resistance can either be found from data sheets or derived by the procedure described in Appendix A.

Since both the RMS current and the average current through each individual switch (transistor and diode) depends on the chosen modulation method as well as modulation index and load angle, the calculation of these currents are rather complex. Actually, the calculations involve piecewise integration with modulation index dependent integration limits as can be derived from eq. (5.5) as well as load angle dependent integration limits. However, for the purpose of avoiding time consuming simulations it is worth-

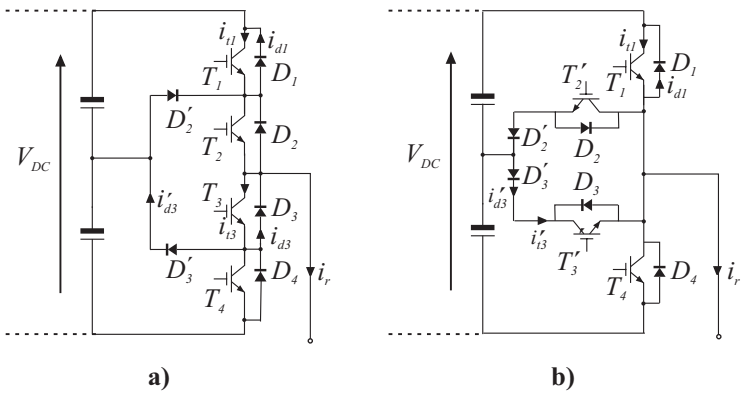


Figure 5.24: *Current definitions for the considered three-level inverter topologies.* **a)** *Inverter leg of the diode clamped three-level inverter.* **b)** *Inverter leg of the transistor clamped three-level inverter.*

while to derive these closed form expression for the average current and the RMS current.

Considering the modulation function for each individual component it is possible to derive the independent expressions for all the involved components. However inspection of the considered three-level inverter topologies reveals some simple relationships. For instance, since all the considered modulation methods assures an equal loading of the upper and lower part of the three level inverter, it is only necessary to calculate the current through the components in the upper (or lower) part[1]. Further, considering the topology redrawn in Fig. 5.24a and using the current definition hereof, it appears that the current i_{d3} through the center diode, at any time is equal to the current through diode D_4 and hence when evaluated for a fundamental, equal to the current i_{d1} through the top diode. Hence the average current $I_{d3,avg}$ and the RMS current I_{d3} simply becomes:

$$I_{d3,avg} = I_{d1,avg} \tag{5.80}$$

$$I_{d3} = I_{d1} \tag{5.81}$$

Moreover, considering the current i_{t3} through the center transistor it appears that during the negative half period of the output current i_r, the transistor current is given by: $i_{t3} = i_r - i_{d2}$ while equaling zero during the positive half period of the output current. Hence, the average- and RMS current through the center transistor can be calculated by:

$$I_{t3,avg} = \frac{\sqrt{2}}{\pi} I_r - I_{d1,avg} \tag{5.82}$$

$$I_{t3} = \sqrt{\frac{1}{2} I_r^2 - I_{d1}^2} \tag{5.83}$$

Further, the current i'_{d3} through the clamping diodes in Fig. 5.24a is at any time instant given by: $i'_{d3} = i_{t3} - i_{t1}$. By this and by using the relationship in eq. (5.82) and eq.

[1]Like for the two level inverter it is possible to establish modulation methods which have an unequal loading of the upper and lower inverter parts. In such case, the current through each individual switch should be calculated separately.

(5.83) the average diode current $I'_{d3,avg}$ and the RMS diode current I'_{d3} can be derived as:

$$I'_{d3,avg} = \frac{\sqrt{2}}{\pi} I_r - (I_{d1,avg} + I_{t1,avg}) \tag{5.84}$$

$$I'_{d3} = \sqrt{\frac{1}{2} I_r^2 - (I_{t1}^2 + I_{d1}^2)} \tag{5.85}$$

The expressions in eq. (5.84) and eq. (5.85) are also valid for the diodes connected to the center point in the topology shown in Fig. 5.24b. Finally, it is easily recognized that the current i'_{t3} through the center transistor in the topology shown in Fig. 5.24b is equal to the diode current i'_{d3}. That is:

$$I'_{t3,avg} = I'_{d3,avg} \tag{5.86}$$

$$I'_{t3} = I'_{d3} \tag{5.87}$$

By these relationships, and by recognizing that the current through the top (and bottom) transistors i_{t1} and diodes i_{d1} are equal for both of the topologies in Fig. 5.24, it is only necessary to derive the analytical expressions for these currents. However, this has to be done for each of the considered modulation methods. Before entering the analytical derivations of the remaining currents, it is appropriate to define the following six integration limits which are commonly used during the derivations.

$$\theta_1 = \frac{\pi}{2} - \sin^{-1}\left(\frac{1}{2M}\right) \tag{5.88}$$

$$\theta_2 = \sin^{-1}\left(\frac{1}{2M}\right) - \frac{\pi}{6} \tag{5.89}$$

$$\theta_3 = \frac{5\pi}{6} - \sin^{-1}\left(\frac{1}{2M}\right) \tag{5.90}$$

$$\theta_4 = \sin^{-1}\left(\frac{1}{2M}\right) - \frac{\pi}{6} \tag{5.91}$$

$$\theta_5 = \pi - \sin^{-1}\left(\frac{1}{2M}\right) \tag{5.92}$$

$$\theta_6 = \sin^{-1}\left(\frac{1}{2M}\right) + \frac{\pi}{6} \tag{5.93}$$

Actually, these integration limits represents the angle at which the space vector makes a transition between the sub-sectors, c.f. Fig. 5.4 on page 153. Finally, it is important to note that the expressions being derived in the following sections are valid for power flowing out of the inverter while for power entering the inverter, the diode and transistor current expressions have to be exchanged.

Space vector modulation method 1 (SVPWM1)

Using the switching pattern for the space vector modulation method 1, cf. Table I and Table II and the modulation functions given by eq. (5.6) - eq. (5.9) the average current through the top (and bottom) transistors and diodes can be calculated by piecewise integration. The average current $I_{d1,avg}$ through the top diode is given by:

$$I_{d1,avg} = I_{t1,avg} - \left(\frac{\sqrt{6}}{6} M \cos(\phi)\right) I_r \tag{5.94}$$

while the expression for the average current $I_{t1,avg}$ through the top transistor are to be calculated by either eq. (5.95), eq. (5.96) or eq. (5.98), depending on the modulation index.

Modulation index lower than 1/2: If the modulation index is lower than 1/2, the average currents through the top transistor can be derived by:

$$I_{t1,avg} = \begin{cases} \frac{M\sqrt{2}\left(\left(2+\pi\sqrt{3}\right)\cos(\phi)+2|\phi|\sin(|\phi|)\right)}{8\pi} I_r & |\phi| \leq \frac{\pi}{6} \\ \frac{M\sqrt{2}\left(\left(6+7\,\pi\,\sqrt{3}-6\,|\phi|\,\sqrt{3}\right)\cos(\phi)+\left(\pi+6\,|\phi|+6\,\sqrt{3}\right)\sin(|\phi|)\right)}{48\pi} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.95}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between 1/2 and $1/\sqrt{3}$, the average current $I_{t1,avg}$ through the top (and bottom) transistor is given by:

$$I_{t1,avg} = \begin{cases} \frac{\left(M^2\pi\,\sqrt{3}-2\,M^2-1\right)\cos(\phi)-2\,M^2|\phi|\,\sin(|\phi|)+4\,M}{\sqrt{32}M\pi} I_r & |\phi| \leq \theta_1 \\ \frac{M\left(2+\sqrt{3}\pi\right)\cos(\phi)+\left(\sqrt{\frac{4\,M^2-1}{M^2}}+2\,M(|\phi|-\pi+2\theta_D)\right)\sin(|\phi|)}{\sqrt{32}\pi} I_r & \theta_1 < |\phi| \leq \frac{\pi}{6} \\ \frac{M\left(1+\sqrt{3}\left(\frac{7\pi}{6}-|\phi|\right)\right)\cos(\phi)}{\sqrt{32}\pi} + & \\ \frac{\left(\sqrt{\frac{4M^2-1}{M^2}}+M\left(\sqrt{3}-\frac{11}{6}\pi+|\phi|+4\theta_D\right)\right)\sin(|\phi|)}{\sqrt{32}\pi} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.96}$$

where the angle θ_D is defined by:

$$\theta_D = \sin^{-1}\left(\frac{1}{2M}\right) \tag{5.97}$$

and the angle θ_1 is given by eq. (5.88).

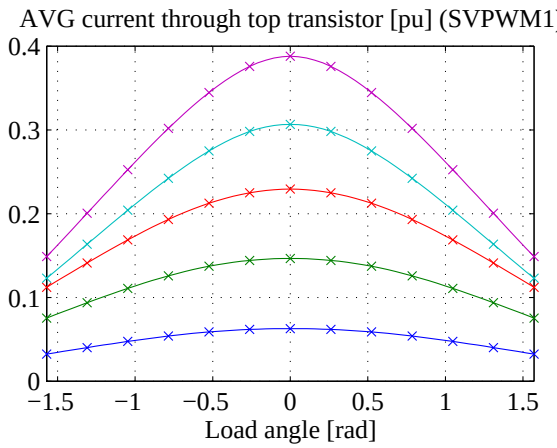


Figure 5.25: *Per unit average current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

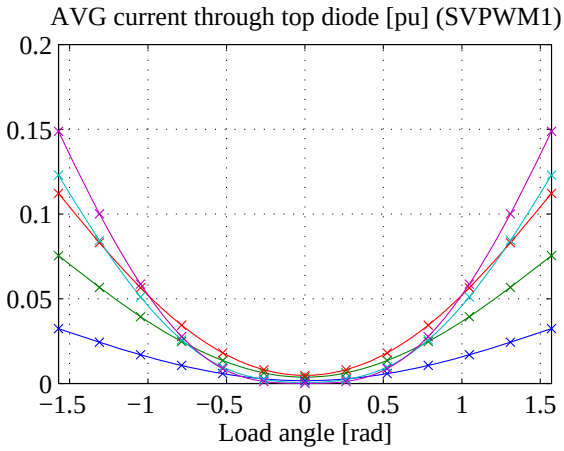


Figure 5.26: *Per unit average current through top diode as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

Modulation index higher than $1/\sqrt{3}$: Finally if the modulation index is above $1/\sqrt{3}$ the average current $I_{t1,avg}$ through the top transistor becomes:

$$I_{t1,avg} = \begin{cases} \frac{\left(\sqrt{3}M^2\left(\frac{5\pi}{6}-\frac{1}{\sqrt{3}}-\theta_D\right)-\sqrt{\frac{12M^2-3}{16M^2}}M-\frac{1}{4}\right)\cos(\phi)+M(2-M|\phi|\sin(|\phi|))}{2\sqrt{8}M\pi} I_r & |\phi| \leq \theta_4 \\ \frac{M^2\left(\frac{2\pi}{\sqrt{3}}-|\phi|\sqrt{3}\right)\cos(\phi)+\left(M^2\left(\frac{\pi}{6}-\theta_D+\sqrt{3}\right)-\sqrt{\frac{4M^2-1}{16M^2}}M+\frac{\sqrt{3}}{4}\right)\sin(|\phi|)}{2\sqrt{32}\pi M} I_r & \theta_4 < |\phi| \leq \frac{\pi}{6} \\ \frac{\left(M^2\left(\frac{\pi}{6}-2\theta_D+\sqrt{3}+|\phi|\right)-\sqrt{\frac{4M^2-1}{4M^2}}M+\frac{\sqrt{3}}{2}\right)\sin(|\phi|)}{\sqrt{32}\pi M}+ & \\ \frac{\sqrt{3}M^2\left(\frac{1}{\sqrt{3}}-|\phi|+\frac{7\pi}{6}\right)\cos(\phi)}{\sqrt{32}\pi M} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{2} \end{cases} \quad (5.98)$$

where the angle θ_4 is given by eq. (5.91). Fig. 5.25 shows the average current $I_{t1,avg}$ through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.95), (5.96) and (5.98). The currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. Similarly, Fig. 5.26 shows the average current $I_{d1,avg}$ through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.94). To validate the closed form expressions, the transistor- and diode current has been obtained from numerical simulations. These results are shown by the marks in Fig. 5.25 and Fig. 5.26.

By use of the expressions for currents trough the top (and bottom) transistor and diode, the average current $I_{t3,avg}$ through the center transistor can be calculated from eq. (5.82). Fig. 5.27 shows the average current $I_{t3,avg}$ through the center transistors as a function of the load angle. Similarly, the current $I'_{d3,avg}$ through the clamping diode can be calculated by use of eq. (5.84). Fig. 5.28 shows the average current $I'_{t3,avg}$ through the clamping diode as a function of the load angle. In both figures, the currents are

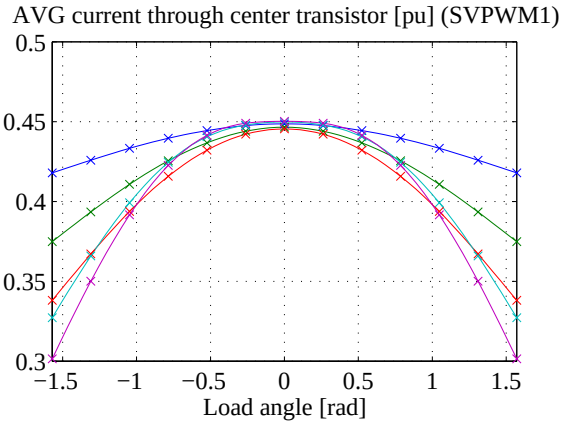


Figure 5.27: *Per unit average current through center transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

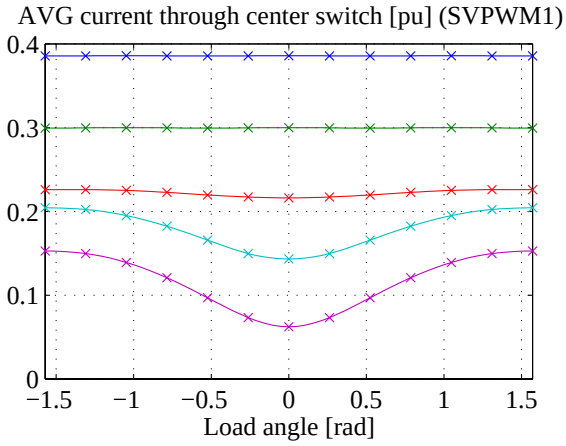


Figure 5.28: *Per unit average current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

Similarly to the average currents through the top (and bottom) transistors and diodes, the expressions for the RMS values can be derived.

Modulation index lower than 1/2: For instance, if the modulation index is less than 1/2, the RMS current through the top transistor and diode becomes:

$$I_{t1} = \begin{cases} \sqrt{\frac{M\left(2-\cos(\phi)^2+2\sqrt{3}\cos(\phi)\right)}{3\pi}} I_r & |\phi| \leq \frac{\pi}{6} \\ \sqrt{\frac{M\left(13-2\cos(\phi)^2+\sqrt{3}\sin(2|\phi|)+4\sqrt{3}\cos(\phi)-4\sin(|\phi|)\right)}{12\pi}} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.99}$$

$$I_{d1} = \sqrt{\frac{3M}{2\pi} I_r^2 - I_{t1}^2} \tag{5.100}$$

Modulation index between than 1/2 and $1/\sqrt{3}$: If the modulation index is between 1/2 and $1/\sqrt{3}$, the RMS current through the top (and bottom) transistor I_{t1} and diode I_{d1} is given by:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(4M^2-1\right)\cos(\phi)^2-8M^2+\frac{1}{2}\right)}{12\pi M} + \right. \\ \left. \frac{4M^2\left(2-\cos(\phi)^2+2\sqrt{3}\cos(\phi)\right)+3M(\pi-2\theta_D)}{12\pi M} \right)^{\frac{1}{2}} I_r & |\phi| \leq \frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(4M^2-1\right)\cos(\phi)^2-8M^2+\frac{1}{2}\right)+3M(\pi-2\theta_D)}{12\pi M} + \right. \\ \left. \frac{M^2\left(4\sqrt{3}\cos(\phi)+\sqrt{3}\sin(2|\phi|)-2(\cos\phi)^2-4\sin(|\phi|)+13\right)}{12\pi M} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.101}$$

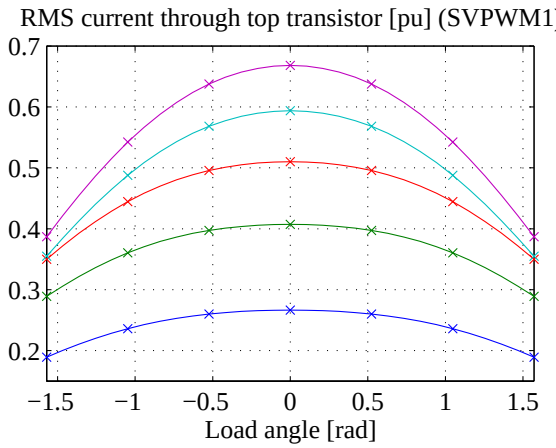


Figure 5.29: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

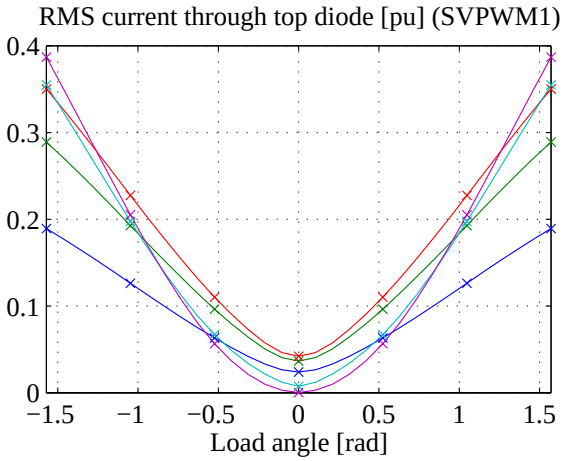


Figure 5.30: *Per unit RMS current through top diode as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

$$I_{d1} = \sqrt{\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(1+8M^2\cos(\phi)^2-16M^2-2\cos(\phi)^2\right)+18M^2+6M\pi-12\theta_D M}{12\pi M}\right) I_r^2 - I_{t1}^2} \tag{5.102}$$

Modulation index higher than $1/\sqrt{3}$: Finally if the modulation index is above $1/\sqrt{3}$ the current through the top (and bottom) transistor I_{t1} and diode I_{d1} becomes:

$$I_{t1} = \begin{cases} \left(\frac{M^2\left(12\sqrt{3}\cos(\phi)^2+24\theta_D-4\pi-6\sqrt{3}\right)+8M^3\left(4\sqrt{3}\cos(\phi)-4\cos(\phi)^2-1\right)}{48\pi M^2}+\right. & \\ \left.\frac{\sqrt{3}-2\sqrt{3}\cos(\phi)^2+\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(4M^3-M\right)\cos(\phi)^2+20M^3+M\right)}{48\pi M^2}\right)^{\frac{1}{2}} I_r & |\phi| \le \frac{\pi}{6} \\ \left(\frac{M^2\left(24\theta_D-4\pi-6\sqrt{3}+12\sqrt{3}\cos(\phi)^2\right)}{48\pi M^2}+\right. & \\ \frac{4M^3\left(\sqrt{3}\sin(2|\phi|)+4\sqrt{3}\cos(\phi)-6\cos(\phi)^2-4\sin(|\phi|)+3\right)}{48\pi M^2}+ & \frac{\pi}{6} < |\phi| \le \frac{\pi}{2} \\ \left.\frac{\sqrt{3}-2\sqrt{3}\cos(\phi)^2+\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(4M^3-M\right)\cos(\phi)^2+20M^3\right)+M}{48\pi M^2}\right)^{\frac{1}{2}} I_r & \end{cases} \tag{5.103}$$

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}M\left(1+20M^2+\left(8M^2-2\right)\cos(\phi)^2\right)-M^3\left(4+16\cos(\phi)^2\right)}{24\pi M^2}+\right.\right. \\ \left.\left.\frac{M^2\left(12\sqrt{3}\cos(\phi)^2-4\pi+24\theta_D-6\sqrt{3}\right)+\sqrt{3}-2\sqrt{3}\cos(\phi)^2}{24\pi M^2}\right) I_r^2 - I_{t1}^2\right)^{\frac{1}{2}} \tag{5.104}$$

Fig. 5.29 shows the RMS current I_{t1} through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.99), (5.101) and (5.103). Similarly, Fig. 5.30 shows the RMS current I_{d1} through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.100), (5.102) and (5.104). In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest value of

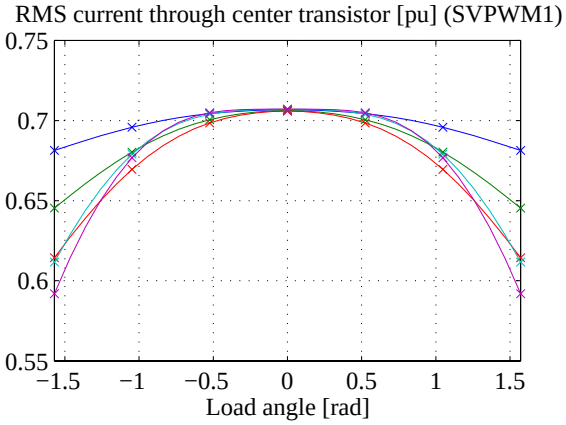


Figure 5.31: *Per unit RMS current through center transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

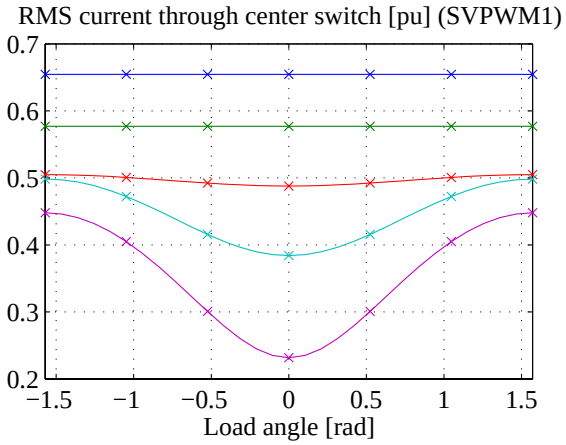


Figure 5.32: *Per unit RMS current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

the modulation index. To validate the closed form expressions, the transistor- and diode current was obtained from numerical simulations. These results are shown by the marks in Fig 5.29 and Fig. 5.30.

By use of the expressions for RMS currents through the top (and bottom) transistor and diode, the RMS current I_{t3} through the center transistor can be calculated from eq. (5.83). Fig. 5.31 shows the RMS current I_{t3} through the center transistors as a function of the load angle. Similarly, the current I'_{d3} through the clamping diode can be calculated by use of eq. (5.85). Fig. 5.32 shows the RMS current I'_{d3} through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

Space vector modulation method 2 (SVPWM2)

Using the switching pattern for the space vector modulation method 2 (SVPWM2), cf. Table III and Table IV and the modulation functions given by eq. (5.6) - eq. (5.9) the average current through the top (and bottom) transistors and diodes can be calculated by piecewise integration. For the entire modulation index range, the average current $I_{d1,avg}$ through the top diodes are given by:

$$I_{d1,avg} = I_{t1,avg} - \left(\frac{\sqrt{6}}{6} M \cos(\phi) \right) I_r \tag{5.105}$$

while the expression for the average current $I_{t1,avg}$ through the top transistor are to be calculated for three different modulation index ranges.

Modulation index lower than 1/2: If the modulation index is lower than 1/2, the average currents through the top transistor can be derived by:

$$I_{t1,avg} = \begin{cases} \frac{M\left(\sqrt{3}(4\pi-3|\phi|)\cos(\phi)+3\left(\sqrt{3}+|\phi|\right)\sin(|\phi|)\right)}{12\sqrt{2}\pi} I_r & |\phi| \leq \frac{\pi}{6} \\ \frac{M\left(\left(9\sqrt{3}\pi-6-12\sqrt{3}|\phi|\right)\cos(\phi)+\left(12\sqrt{3}+\pi\right)\sin(|\phi|)\right)}{24\sqrt{2}\pi} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{3} \\ \frac{M\left(\left(7\sqrt{3}\pi-6-6|\phi|\sqrt{3}\right)\cos(\phi)+\left(3\pi-6|\phi|+12\sqrt{3}\right)\sin(|\phi|)\right)}{24\sqrt{2}\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.106}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between 1/2 and $1/\sqrt{3}$, the average current through the top (and bottom) transistor $I_{t1,avg}$ is given by:

$$I_{t1,avg} = \begin{cases} \frac{\left(3M\left(\sqrt{3}-|\phi|\right)\sin(|\phi|)+\left(4\sqrt{3}M\pi-6-3\sqrt{3}M|\phi|\right)\cos(\phi)+6\right)}{12\sqrt{2}\pi} I_r & |\phi| \leq \theta_1 \\ \frac{\left(M^2\left(|\phi|+2\theta_D-\pi+\sqrt{3}\right)+\sqrt{\frac{4M^2-1}{4M^2}}M\right)\sin(|\phi|)}{4\sqrt{2}\pi M} + & \\ \frac{\left(M^2\left(2+\frac{4\pi}{\sqrt{3}}-\sqrt{3}|\phi|\right)-2M+\frac{1}{2}\right)\cos(\phi)}{4\sqrt{2}\pi M} I_r & \theta_1 < |\phi| \leq \frac{\pi}{6} \\ \frac{\left(M^2\left(4\theta_D-\frac{5\pi}{3}+4\sqrt{3}\right)+\sqrt{\frac{4M^2-1}{M^2}}M\right)\sin(|\phi|)}{8\sqrt{2}\pi M} + & \\ \frac{\left(M^2\left(2+3\sqrt{3}\pi-4\sqrt{3}|\phi|\right)-4M+1\right)\cos(\phi)}{8\sqrt{2}\pi M} I_r & \frac{\pi}{6} < |\phi| \leq \theta_2 \\ \frac{\left(4M^2\left(3\theta_D-|\phi|-\pi+\sqrt{3}\right)+3\sqrt{\frac{4M^2-1}{M^2}}M-\sqrt{3}\right)\sin(|\phi|)}{16\sqrt{2}\pi M} + & \\ \frac{\left(4M^2\left(\frac{4\pi}{\sqrt{3}}-|\phi|\sqrt{3}-\sqrt{3}\theta_D\right)-M\left(\sqrt{\frac{4M^2-1}{M^2}}\sqrt{3}+8\right)+1\right)\cos(\phi)+8M}{16\sqrt{2}\pi M} I_r & \theta_2 < |\phi| \leq \frac{\pi}{3} \\ \frac{\left(M^2\left(12\theta_D-\frac{16\pi}{3}+4\sqrt{3}\right)+M\left(3\sqrt{\frac{4M^2-1}{M^2}}+8\sqrt{3}\right)-\sqrt{3}\right)\sin(|\phi|)}{16\sqrt{2}\pi M} + & \\ \frac{\left(4\sqrt{3}M^2(2\pi-2|\phi|-\theta_D)-\sqrt{\frac{4M^2-1}{M^2}}\sqrt{3}M+1\right)\cos(\phi)-8M}{16\sqrt{2}\pi M} I_r & \frac{\pi}{3} < |\phi| \leq \theta_3 \\ \frac{\left(M^2(4\theta_D-\pi-2|\phi|)+M\left(4\sqrt{3}+\sqrt{\frac{4M^2-1}{M^2}}\right)-\sqrt{3}\right)\sin(|\phi|)}{8\sqrt{2}\pi M} + & \\ \frac{M^2\left(\frac{7\pi}{\sqrt{3}}-2-2\sqrt{3}|\phi|\right)\cos(\phi)}{8\sqrt{2}\pi M} I_r & \theta_3 < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.107}$$

where the angles θ_1 - θ_3 are given by eq. (5.88) - eq. (5.90).

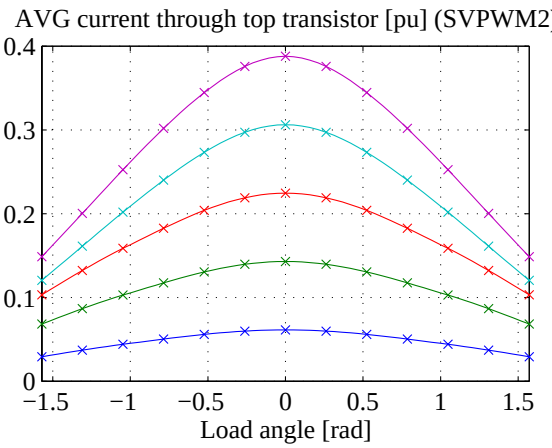


Figure 5.33: *Per unit average current through top transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

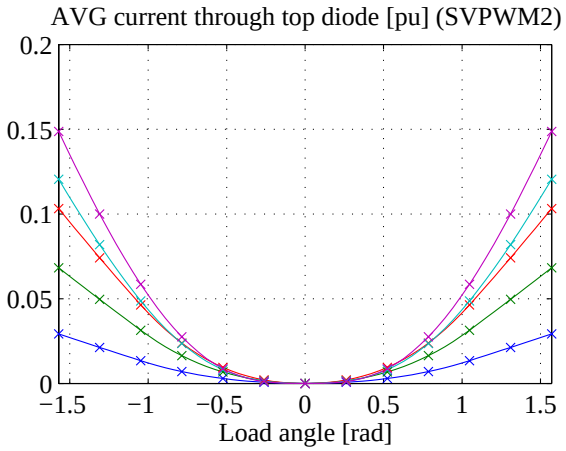


Figure 5.34: *Per unit average current through top diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

Modulation index higher than $1/\sqrt{3}$: Finally if the modulation index is above $1/\sqrt{3}$ the average current through the top (and bottom) transistor $I_{t1,avg}$ becomes:

$$I_{t1,avg} = \begin{cases} \frac{\left(\sqrt{3}M(4\pi-3|\phi|)-6\right)\cos(\phi)+3\,M\left(\sqrt{3}-|\phi|\right)\sin(|\phi|)+6}{12\sqrt{2}\pi} I_r & |\phi| \le \theta_4 \\ \frac{\left(4M^2\left(\sqrt{3}\frac{7\pi}{6}+1-2\sqrt{3}|\phi|+\theta_D\right)+\sqrt{\frac{4\,M^2-1}{M^2}}\sqrt{3}M-8\,M+1\right)\cos(\phi)}{16\sqrt{2}\pi M}+ & \\ \frac{\left(M^2\left(8\sqrt{3}-4\theta_D+\frac{2\pi}{3}\right)+\sqrt{3}-\sqrt{\frac{4\,M^2-1}{M^2}}M\right)\sin(|\phi|)}{16\sqrt{2}\pi M} I_r & \theta_4 < |\phi| \le \frac{\pi}{6} \\ \frac{\left(M^2\left(4\pi\sqrt{3}+8-4\sqrt{3}(|\phi|-\theta_D)\right)+M\left(\sqrt{\frac{4\,M^2-1}{M^2}}\sqrt{3}-8\right)+1\right)\cos(\phi)}{16\sqrt{2}\pi M}+ & \\ \frac{4\,M^2\left(\sqrt{3}-\theta_D+|\phi|\right)\sin(|\phi|)-\sqrt{\frac{4\,M^2-1}{M^2}}M+\sqrt{3}}{16\sqrt{2}\pi M} I_r & \frac{\pi}{6} < |\phi| \le \theta_5 \\ \frac{\left(4\sqrt{3}M^2(\pi+\theta_D-|\phi|)+M\left(\sqrt{\frac{4\,M^2-1}{M^2}}\sqrt{3}-8\right)-1\right)\cos(\phi)}{16\sqrt{2}\pi M}+ & \\ \frac{\left(4M^2\left(\sqrt{3}-3\theta_D+\pi-|\phi|\right)-3\sqrt{\frac{4\,M^2-1}{M^2}}M+\sqrt{3}\right)\sin(|\phi|)+8\,M}{16\sqrt{2}\pi M} I_r & \theta_5 < |\phi| \le \frac{\pi}{3} \\ \frac{\left(\frac{4}{\sqrt{3}}M^2(4\pi-6|\phi|+3\theta_D)+\sqrt{\frac{4\,M^2-1}{M^2}}\sqrt{3}M-1\right)\cos(\phi)}{16\sqrt{2}\pi M}+ & \\ \frac{\left(4M^2\left(\sqrt{3}-3\theta_D+\frac{2\pi}{3}\right)+M\left(8\,M\sqrt{3}-3\sqrt{\frac{4\,M^2-1}{M^2}}\right)+\sqrt{3}\right)\sin(|\phi|)-8\,M}{16\sqrt{2}\pi M} I_r & \frac{\pi}{3} < |\phi| \le \theta_6 \\ \frac{\sqrt{3}M\left(\frac{7}{6}\pi+\frac{1}{\sqrt{3}}-\phi\right)\cos(\phi)+\left(M\left(\frac{\pi}{2}-4\theta_D+\phi\right)-\sqrt{\frac{4M^2-1}{M^2}}+2\sqrt{3}\right)\sin(|\phi|)}{4\sqrt{2}\pi} I_r & \theta_6 < |\phi| \le \frac{\pi}{2} \end{cases} \quad (5.108)$$

where the angles θ_4 - θ_6 are given by eq. (5.91) - eq. (5.93). Fig. 5.33 shows the average current $I_{t1,avg}$ through the top (and bottom) transistors as a function of the load angle,

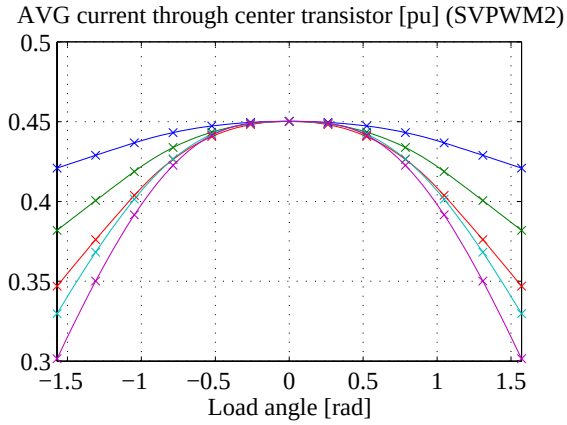


Figure 5.35: *Per unit average current through center transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

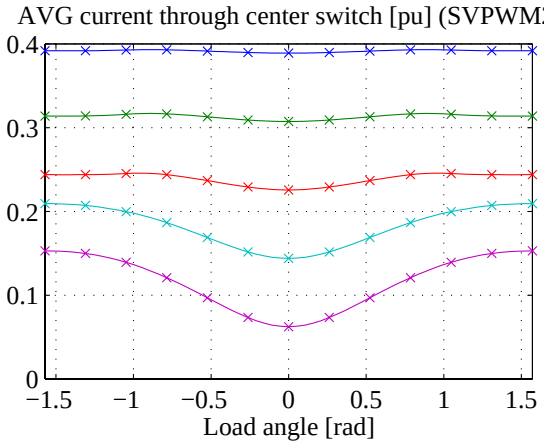


Figure 5.36: *Per unit average current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

i.e. the current calculated by the expressions given by eq. (5.106), (5.107) and (5.108). The currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. Similarly, Fig. 5.34 shows the average current $I_{d1,avg}$ through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.105). To validate the closed form expressions, the transistor- and diode current was derived from numerical simulations. These results are shown by the marks in Fig. 5.33 and Fig. 5.34.

By use of the expressions for currents trough the top (and bottom) transistor and diode, the average current $I_{t3,avg}$ through the center transistor can be calculated from eq. (5.82). Fig. 5.35 shows the average current $I_{t3,avg}$ through the center transistors as a function of the load angle. Similarly, the current $I'_{d3,avg}$ through the clamping diode can be calculated by use of eq. (5.84). Fig. 5.36 shows the average current $I'_{t3,avg}$ through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

As in the case for the average currents, the RMS values are to be derived for three different modulation index ranges.

Modulation index lower than 1/2: For instance, if the modulation index is less than 1/2, the RMS current through the top transistor becomes:

$$I_{t1} = \begin{cases} \frac{\sqrt{M\left(\sin(|2\phi|)-3\sqrt{3}\cos(\phi)^2+3\sqrt{3}+1-2\sin(|\phi|)+4\cos(\phi)^2+2\sqrt{3}\cos(\phi)\right)}}{\sqrt{6\pi}} I_r & |\phi| \leq \frac{\pi}{6} \\ \frac{\sqrt{M\left(\left(6-6\sqrt{3}\right)\cos(\phi)^2+2\sin(|2\phi|)+6\sqrt{3}-3-\sqrt{3}\sin(|2\phi|)+8\sqrt{3}\cos(\phi)\right)}}{\sqrt{12\pi}} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{3} \\ \frac{\sqrt{M\left(2\left(3-\sqrt{3}\right)\cos(\phi)^2-3+\left(2-\sqrt{3}\right)\sin(|2\phi|)+4\left(\sqrt{3}\cos(\phi)+\sin(|\phi|)+\sqrt{3}\right)\right)}}{\sqrt{12\pi}} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \quad (5.109)$$

while the RMS current I_{d1} through the top diode is given by:

$$I_{d1} = \sqrt{\frac{M\left(\left(2-\sqrt{3}\right)\cos(\phi)^2+2\sqrt{3}+\frac{1}{2}\right)}{3\pi} I_r^2 - I_{t1}^2} \tag{5.110}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between 1/2 and $1/\sqrt{3}$, the RMS current through the transistors in the top (and bottom) switch becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(4M^3-M\right)\cos(\phi)^2-16M^3+M\right)+2\sqrt{3}\cos(\phi)^2-\sqrt{3}}{24\pi M^2} + \right. \\ \frac{3M^2\left(2\pi-8\sqrt{3}\cos(\phi)^2-4\theta_D+4\sqrt{3}+\sin(|2\phi|)-2|\phi|\right)}{24\pi M^2} + \\ \left. \frac{4M^3\left(1-\sqrt{3}+2\sqrt{3}\cos(\phi)+\left(4+5\sqrt{3}\right)\cos(\phi)^2-\sin(|2\phi|)+2\sin(|\phi|)\right)}{24\pi M^2} \right)^{\frac{1}{2}} I_r & |\phi| \le \theta_1 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(4M^3-M\right)\cos(\phi)^2-16M^3+M\right)-\sin(|2\phi|)+4\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \right. \\ \frac{6M^2\left(\pi-2\theta_D+4\sqrt{3}-8\sqrt{3}\cos(\phi)^2+4\sin(|\phi|)\cos(\phi)\right)-2\sqrt{3}}{48\pi M^2} + \\ \left. \frac{8M^3\left(1-\sqrt{3}+2\sqrt{3}\cos(\phi)+\left(4+5\sqrt{3}\right)\cos(\phi)^2-\sin(|2\phi|)-2\sin(|\phi|)\right)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & \theta_1 < |\phi| \le \frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(4M^3-M\right)\cos(\phi)^2-16M^3+M\right)-\sin(|2\phi|)-2\sqrt{3}}{48\pi M^2} + \right. \\ \frac{6M^2\left(\pi-2\theta_D+4\sqrt{3}-8\sqrt{3}\cos(\phi)^2+2\sin(|2\phi|)\right)+4\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \\ \left. \frac{4M^3\left(8\sqrt{3}\cos(\phi)+\left(6+10\sqrt{3}\right)\cos(\phi)^2-3-2\sqrt{3}-\left(2+\sqrt{3}\right)\sin(|2\phi|)\right)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < |\phi| \le \theta_2 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(\sqrt{3}M-4M^3\sqrt{3}\right)\sin(|2\phi|)+6\left(4M^3-M\right)\cos(\phi)^2+3M-12M^3\right)}{96\pi M^2} + \right. \\ \frac{M^2\left(8\pi+42\sqrt{3}-84\sqrt{3}\cos(\phi)^2-24|\phi|+30\sin(|2\phi|)\right)-3\sin(|2\phi|)+6\sqrt{3}\cos(\phi)^2-3\sqrt{3}}{96\pi M^2} + \\ \left. \frac{M^3\left(8\left(4\sin(|\phi|)-2\sqrt{3}+4\sqrt{3}\cos(\phi)-3\right)-8\left(\sqrt{3}-2\right)\sin(|2\phi|)+8\left(6+10\sqrt{3}\right)\cos(\phi)^2\right)}{96\pi M^2} \right)^{\frac{1}{2}} I_r & \theta_2 < |\phi| \le \frac{\pi}{3} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\sqrt{3}\left(M-4M^3\right)\sin(|2\phi|)+6\left(4M^3-M\right)\cos(\phi)^2-12M^3+3M\right)}{96\pi M^2} + \right. \\ \frac{M^2\left(24|\phi|-8\pi+30\sqrt{3}-60\sqrt{3}\cos(\phi)^2+42\sin(|2\phi|)\right)-3\sin(|2\phi|)+6\sqrt{3}\cos(\phi)^2}{96\pi M^2} + \\ \left. \frac{8M^3\left(8\sqrt{3}\cos(\phi)-\left(\sqrt{3}+4\right)\sin(|2\phi|)+\left(6+6\sqrt{3}\right)\cos(\phi)^2-3\right)-3\sqrt{3}}{96\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{3} < |\phi| \le \theta_3 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(4M^3-M\right)\cos(\phi)^2-16M^3+M\right)+2\sqrt{3}\cos(\phi)^2-\sqrt{3}-2\sin(|2\phi|)}{48\pi M^2} + \right. \\ \frac{M^2\left(6\pi+12\sqrt{3}-12\theta_D-24\sqrt{3}\cos(\phi)^2+24\sin(|2\phi|)\right)}{48\pi M^2} + \\ \left. \frac{4M^3\left(4\sin(|\phi|)+4\sqrt{3}\cos(\phi)-\left(\sqrt{3}+4\right)\sin(|2\phi|)+6\left(\sqrt{3}+1\right)\cos(\phi)^2-3\right)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & \theta_3 < |\phi| \le \frac{\pi}{2} \end{cases} \tag{5.111}$$

where the angles θ_1 - θ_3 are given by eq. (5.88) - eq. (5.90). The RMS diode current

I_{d1} becomes:

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4\,M^2-1}{M^2}}\left(2\left(4\,M^3-M\right)\cos(\phi)^2-16M^3+M\right)+4M^3\left(\left(6\sqrt{3}+4\right)\cos(\phi)^2+1\right)}{24\pi M^2} + \frac{6M^2\left(2\,\sqrt{3}+\pi-2\theta_D-4\,\sqrt{3}\cos(\phi)^2\right)2\,\sqrt{3}\cos(\phi)^2-\sqrt{3}}{24\pi M^2} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \tag{5.112}$$

Modulation index higher than $1/\sqrt{3}$: If the modulation index is above $1/\sqrt{3}$, the RMS current through the transistors in the top and bottom switch becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(M-4M^3\right)\cos(\phi)^2+16M^3-M\right)}{24\pi M^2} + \frac{M^2\left(3\sin(|2\phi|)-2\pi+12\sin^{-1}\left(\frac{1}{2M}\right)-6|\phi|\right)-2\sqrt{3}\cos(\phi)^2+\sqrt{3}}{24\pi M^2} + \frac{4M^3\left(\left(5\sqrt{3}-4\right)\cos(\phi)^2+2\sin(|\phi|)-\sin(|2\phi|)+2\sqrt{3}\cos(\phi)-\sqrt{3}-1\right)}{24\pi M^2} \right)^{\frac{1}{2}} I_r & |\phi| \leq \theta_4 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(10M-40M^3\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+44M^3-5M\right)}{96\pi M^2} + \frac{8M^3\left(\left(10\sqrt{3}-8\right)\cos(\phi)^2-2\sin(|2\phi|)+8\sqrt{3}\cos(\phi)-2\sqrt{3}-2\right)+\sin(|2\phi|)+3\sqrt{3}}{96\pi M^2} + \frac{M^2\left(6\sin(|2\phi|)-12\sqrt{3}\cos(\phi)^2+6\sqrt{3}-4\pi+24\sin^{-1}\left(\frac{1}{2M}\right)\right)-6\sqrt{3}\cos(\phi)^2}{96\pi M^2} \right)^{\frac{1}{2}} I_r & \theta_4 < |\phi| \leq \frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(10M-40M^3\right)\cos(\phi)^2+\left(4M^3-M\sqrt{3}\right)\sin(|2\phi|)+44M^3-5M\right)+\sin(|2\phi|)}{96\pi M^2} + \frac{8M^3\left(\left(10\sqrt{3}-6\right)\cos(\phi)^2+\left(\sqrt{3}-2\right)\sin(|2\phi|)+4\sqrt{3}\cos(\phi)-4\sin(|\phi|)-2\sqrt{3}+3\right)}{96\pi M^2} + \frac{M^2\left(6\sin(|2\phi|)-12\sqrt{3}\cos(\phi)^2+6\sqrt{3}-4\pi+24\sin^{-1}\left(\frac{1}{2M}\right)\right)-6\sqrt{3}\cos(\phi)^2+3\sqrt{3}}{96\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < |\phi| \leq \theta_5 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(6\left(M-4M^3\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)-3M+12M^3\right)}{96\pi M^2} + \frac{M^3\left(8\left(10\sqrt{3}-6\right)\cos(\phi)^2+8\left(\sqrt{3}-2\right)\sin(|2\phi|)+32\left(\sqrt{3}\cos(\phi)+\sin(|\phi|)\right)-16\sqrt{3}+24\right)}{96\pi M^2} + \frac{2M^2\left(4\pi-6\sqrt{3}\cos(\phi)^2-3\sin(|2\phi|)+3\sqrt{3}-12|\phi|\right)-6\sqrt{3}\cos(\phi)^2+3\sin(|2\phi|)+3\sqrt{3}}{96\pi M^2} \right)^{\frac{1}{2}} I_r & \theta_5 < |\phi| \leq \frac{\pi}{3} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(6\left(M-4M^3\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+12M^3-3M\right)}{96\pi M^2} + \frac{8M^3\left(6\left(\sqrt{3}-1\right)\cos(\phi)^2+\left(\sqrt{3}-4\right)\sin(|2\phi|)+8\sqrt{3}\cos(\phi)+3\right)-6\sqrt{3}\cos(\phi)^2}{96\pi M^2} + \frac{2M^2\left(+3\sin(|2\phi|)+6\sqrt{3}\cos(\phi)^2-3\sqrt{3}-4\pi+12|\phi|\right)+3\sin(|2\phi|)+3\sqrt{3}}{96\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{3} < |\phi| \leq \theta_6 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(+2\left(M-4M^3\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+16M^3-M\right)}{48\pi M^2} + \frac{M^3\left(24\left(\sqrt{3}-1\right)\cos(\phi)^2+\left(4\sqrt{3}M^3-16\right)\sin(|2\phi|)+16\sqrt{3}\cos(\phi)+12-16\sin(|\phi|)\right)}{48\pi M^2} + \frac{2M^2\left(3\sin(|2\phi|)M^2+6\sin^{-1}\left(\frac{1}{2M}\right)M^2-\pi M^2\right)-2\sqrt{3}\cos(\phi)^2+\sqrt{3}+\sin(|2\phi|)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & \theta_6 < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.113}$$

where the angles θ_4 - θ_6 are given by eq. (5.91) - eq. (5.93). The current through the top diode then becomes:

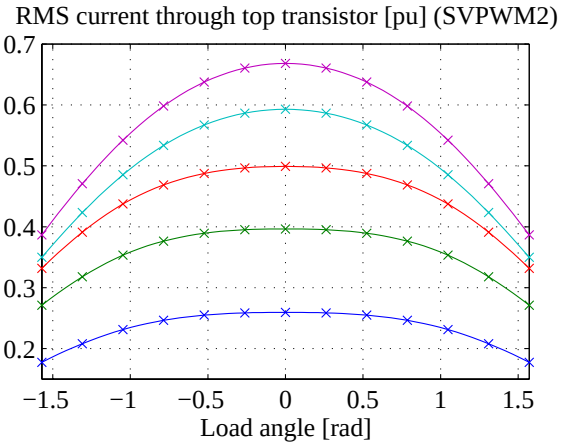


Figure 5.37: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

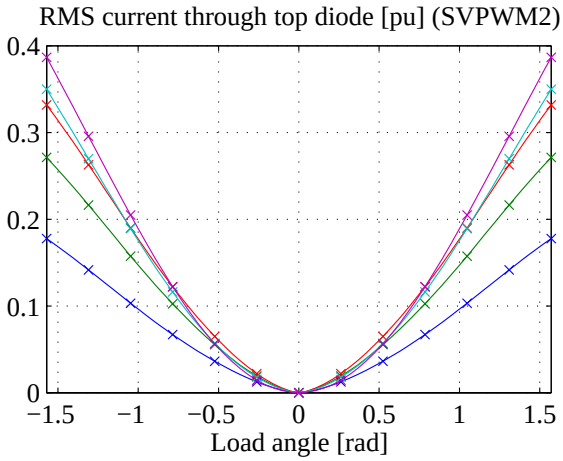


Figure 5.38: *Per unit RMS current through top diode as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(2\left(M-4M^3\right)\cos(\phi)^2+16M^3-M\right)+4M^3\left(\left(6\sqrt{3}-4\right)\cos(\phi)^2-1\right)}{24\pi M^2} + \frac{2M^2(6\theta_D-\pi)+\sqrt{3}-2\sqrt{3}\cos(\phi)^2}{24\pi M^2} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \tag{5.114}$$

Fig. 5.37 shows the RMS current I_{t1} through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.109), (5.111) and (5.113). Similarly, Fig. 5.38 shows the RMS current I_{d1} through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.110), (5.112) and (5.114). In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. To validate the closed form expressions the transistor- and diode current was derived from numerical simulations. These results are shown by the marks in Fig 5.37 and Fig. 5.38.

By use of the expressions for RMS currents through the top (and bottom) transistor and diode, the RMS current I_{t3} through the center transistor can be calculated from eq. (5.83). Fig. 5.39 shows the RMS current I_{t3} through the center transistors as a function of the load angle. Similarly, the current I'_{d3} through the clamping diode can be calculated by use of eq. (5.85). Fig. 5.40 shows the RMS current I'_{d3} through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

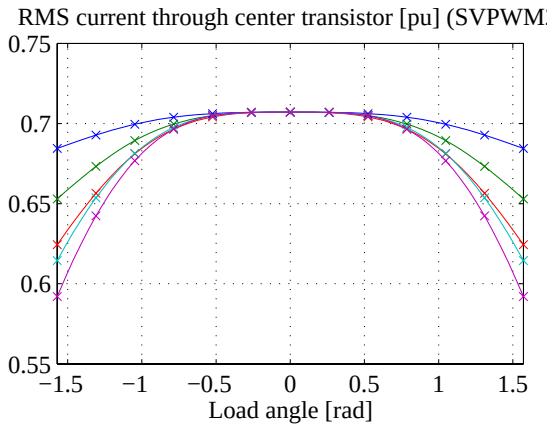


Figure 5.39: *Per unit RMS current through center transistor as a function of the load angle. $M \in [0.15, 0.35 ...0.95]$.*

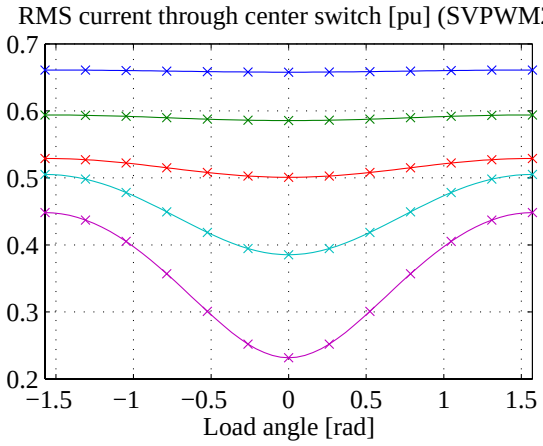


Figure 5.40: *Per unit RMS current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 ...0.95]$.*

Asymmetrical shifted left flat top modulation (DPWM0)

Considering the asymmetrical shifted left flat top modulation given by the upper part of Table V, the average current through the top diode is given by:

$$I_{d1,avg} = I_{t1,avg} - \left(\frac{\sqrt{6}}{6} M \cos(\phi)\right) I_r \tag{5.115}$$

while the average current through the top transistor has to be calculated separately for three different modulation index ranges.

Modulation index less than 1/2: If the modulation index is less than 1/2, the average current $I_{t1,avg}$ can be calculated by:

$$I_{t1,avg} = \begin{cases} \frac{M\left(2\sqrt{3}\pi-9\right)\cos(\phi)-M\left(2\pi+3\sqrt{3}\right)\sin(|\phi|)+12}{12\sqrt{2}\pi} I_r & -\frac{\pi}{2} \le \phi \le -\frac{\pi}{6} \\ \frac{M\left(\sqrt{3}\pi+6\sqrt{3}|\phi|-6\right)\cos(\phi)-M\left(6\sqrt{3}+\pi+6|\phi|\right)\sin(|\phi|)+12}{12\sqrt{2}\pi} I_r & -\frac{\pi}{6} < \phi \le 0 \\ \frac{\sqrt{2}\left(M\left(\pi\sqrt{3}-6|\phi|\sqrt{3}-6\right)\cos(\phi)+M\left(\pi+6\sqrt{3}-6|\phi|\right)\sin(|\phi|)+12\right)}{24\pi} I_r & 0 < \phi \le \frac{\pi}{6} \\ \frac{\sqrt{2}\left(M\left(3-\pi\sqrt{3}+6|\phi|\sqrt{3}\right)\cos(\phi)+M\left(\pi-6|\phi|-3\sqrt{3}\right)\sin(|\phi|)+12\right)}{24\pi} I_r & \frac{\pi}{6} < \phi \le \frac{\pi}{2} \end{cases} \tag{5.116}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between 1/2 and $1/\sqrt{3}$, the average current through the transistors in the top (and bottom)

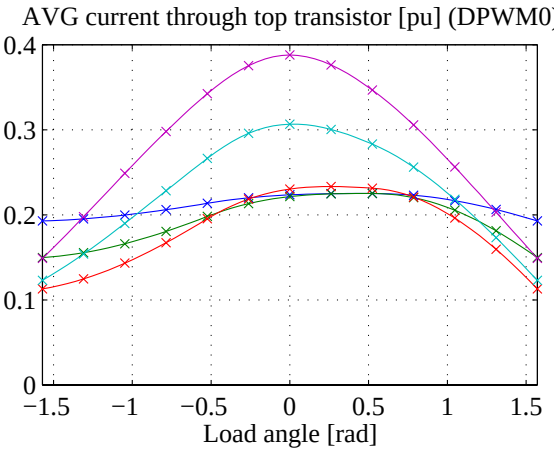


Figure 5.41: *Per unit average current through top transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

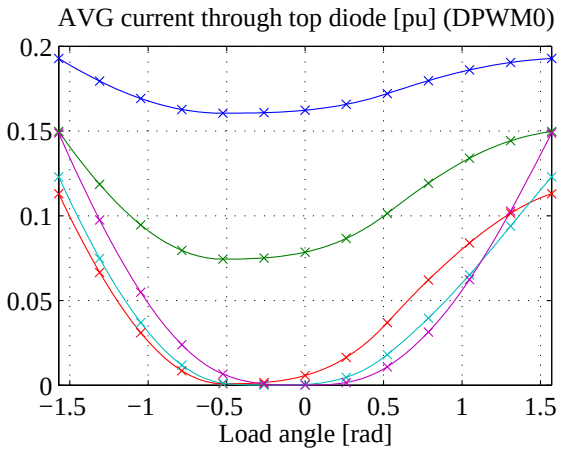


Figure 5.42: *Per unit average current through the top diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

switch becomes:

$$
I_{t1,avg} = \begin{cases}
\dfrac{M\left(4\pi-12\theta_D-3\sqrt{\frac{4M^2-1}{M^4}}-3\sqrt{3}\right)\sin(|\phi|)}{12\sqrt{2}\pi}+ & \\
\dfrac{M\left(8\pi\sqrt{3}-3\sqrt{3}\sqrt{\frac{4M^2-1}{M^4}}-12\theta_D\sqrt{3}-9\right)\cos(\phi)+12}{12\sqrt{2}\pi}I_r & -\frac{\pi}{2} \le \phi \le -\frac{\pi}{6} \\
\dfrac{M\left(\frac{5\pi}{6}-\sqrt{3}-\sqrt{\frac{4M^2-1}{4M^4}}-2\theta_D-|\phi|\right)\sin(|\phi|)}{2\sqrt{2}\pi}+ & \\
\dfrac{\sqrt{3}M\left(\frac{7\pi}{6}-\sqrt{\frac{4M^2-1}{4M^4}}-2\theta_D-\frac{1}{\sqrt{3}}+|\phi|\right)\cos(\phi)+2}{2\sqrt{2}\pi}I_r & -\frac{\pi}{6} < \phi \le 0 \\
\dfrac{\sqrt{6}\left(7M\pi-3\sqrt{\frac{4M^2-1}{M^2}}-12M\theta_D-6M|\phi|-\frac{6}{\sqrt{3}}M\right)\cos(\phi)}{24\pi}+ & \\
\dfrac{\sqrt{2}\left(6M\sqrt{3}-5M\pi+3\sqrt{\frac{4M^2-1}{M^2}}+12M\theta_D-6M|\phi|\right)\sin(|\phi|)+12\sqrt{2}}{24\pi}I_r & 0 < \phi \le \frac{\pi}{6} \\
\dfrac{\sqrt{6}\left(5M\pi-3\sqrt{\frac{4M^2-1}{M^2}}-12M\theta_D+\sqrt{3}M+6M|\phi|\right)\cos(\phi)}{24\pi}+ & \\
\dfrac{\sqrt{2}\left(3\sqrt{\frac{4M^2-1}{M^2}}-5M\pi+12M\theta_D-6M|\phi|-3M\sqrt{3}\right)\sin(|\phi|)+12\sqrt{2}}{24\pi}I_r & \frac{\pi}{6} < \phi \le \theta_2 \\
\dfrac{\sqrt{6}\left(\frac{1}{\sqrt{3}}+M^2\left(\frac{5}{\sqrt{3}}+\pi-2|\phi|\right)\right)\cos(\phi)}{8\pi M}+ & \\
\dfrac{\sqrt{6}\left(1+M^2\left(\frac{2}{\sqrt{3}}|\phi|-\frac{\pi}{\sqrt{3}}+3\right)\right)\sin(|\phi|)-4\sqrt{2}M}{8M\pi}I_r & \theta_2 < \phi \le \theta_3 \\
\dfrac{\sqrt{6}\left(\sqrt{3}M+3\sqrt{\frac{4M^2-1}{M^2}}-7M\pi+12M\theta_D+6M|\phi|\right)\cos(\phi)}{24\pi}+ & \\
\dfrac{\sqrt{2}\left(7M\pi-3\sqrt{\frac{4M^2-1}{M^2}}-12M\theta_D-3M\sqrt{3}-6M|\phi|\right)\sin(|\phi|)+12\sqrt{2}}{24\pi}I_r & \theta_3 < \phi \le \frac{\pi}{2}
\end{cases} \tag{5.117}
$$

Modulation index higher than $1/\sqrt{3}$: If the modulation index is higher than $1/\sqrt{3}$, the average current through the transistors in the top (and bottom) switch becomes:

$$I_{t1,avg} = \begin{cases} \frac{\left(M^2\left(6\sqrt{3}+4\pi-12\theta_D\right)-24\,M-3\,\sqrt{\frac{4\,M^2-1}{M^2}})M+3\,\sqrt{3}\right)\sin(|\phi|)}{24\sqrt{2}\pi M}+ \\ \frac{\left(M^2\left(18+4\pi\,\sqrt{3}+12\theta_D\sqrt{3}\right)+3\,\sqrt{\frac{4\,M^2-1}{M^2}}\sqrt{3}M-24\,M\sqrt{3}+3\right)\cos(\phi)+24\,M}{24\sqrt{2}\pi M} I_r & -\frac{\pi}{2} \le \phi \le -\frac{\pi}{6} \\ \frac{\left(12\,M^2\left(|\phi|+\frac{\pi}{6}-\theta_D+\sqrt{3}\right)-3\sqrt{\frac{4\,M^2-1}{M^2}}M+3\sqrt{3}\right)\sin(|\phi|)}{24\sqrt{2}\pi M}+ \\ \frac{\left(12\,M^2\left(\theta_D\sqrt{3}-|\phi|\sqrt{3}+\frac{\pi}{2}\,\sqrt{3}+1\right)+3\sqrt{\frac{4\,M^2-1}{M^2}}\sqrt{3}M+3\right)\cos(\phi)-24M}{24\sqrt{2}\pi M} I_r & -\frac{\pi}{6} < \phi \le -\theta_1 \\ \frac{\left(4M^2\left(\theta_D-|\phi|-\sqrt{3}-\frac{\pi}{6}\right)+\sqrt{\frac{4\,M^2-1}{M^2}}M-\sqrt{3}\right)\sin(|\phi|)}{8\sqrt{2}\pi M}+ \\ \frac{\left(4\sqrt{3}M^2\left(|\phi|-\theta_D-\frac{1}{\sqrt{3}}+\frac{5\pi}{6}\right)-\sqrt{3}\sqrt{\frac{4\,M^2-1}{M^2}}M-1\right)\cos(\phi)+8M}{8\sqrt{2}\pi M} I_r & -\theta_1 < \phi \le 0 \\ \frac{\sqrt{3}\left(M^2\left(10\pi-\frac{12}{\sqrt{3}}-12|\phi|-12\theta_D\right)-3\,\sqrt{\frac{4\,M^2-1}{M^2}}M-\sqrt{3}\right)\cos(\phi)}{12\sqrt{2}\pi M}+ \\ \frac{\left(M^2\left(12\sqrt{3}-12|\phi|+2\pi-12\theta_D\right)-3\,\sqrt{\frac{4\,M^2-1}{M^2}}M+3\,\sqrt{3}\right)\sin(|\phi|)+24M}{12\sqrt{2}\pi M} I_r & 0 < \phi \le \frac{\pi}{6} \\ \frac{\left(M^2\left(10\pi\,\sqrt{3}-6-12|\phi|\,\sqrt{3}-12\theta_D\sqrt{3}\right)-3\,\sqrt{\frac{4\,M^2-1}{M^2}}\sqrt{3}M+24\,M\sqrt{3}-3\right)\cos(\phi)}{12\sqrt{2}\pi M}+ \\ \frac{\left(M^2\left(12|\phi|-2\pi-12\theta_D+6\sqrt{3}\right)+24\,M-3\,\sqrt{\frac{4\,M^2-1}{M^2}}M+3\,\sqrt{3}\right)\sin(|\phi|)-24\,M}{12\sqrt{2}\pi M} I_r & \frac{\pi}{6} < \phi \le \frac{\pi}{2} \end{cases} \tag{5.118}$$

Fig. 5.41 shows the average current $I_{t1,avg}$ through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.116), (5.117) and (5.118). The currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. Similarly, Fig. 5.42 shows the average current $I_{d1,avg}$ through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.115). To validate the closed form expressions, the transistor- and diode current has been obtained from numerical simulations. These results are shown by the marks in Fig.5.41 and Fig. 5.42.

By use of the expressions for currents trough the top (and bottom) transistor and diode, the average current $I_{t3,avg}$ through the center transistor can be calculated from eq. (5.82). Fig. 5.43 shows the average current $I_{t3,avg}$ through the center transistors as a function of the load angle. Similarly, the current $I'_{d3,avg}$ through the clamping diode can be calculated by use of eq. (5.84). Fig. 5.44 shows the average current $I'_{t3,avg}$ through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents

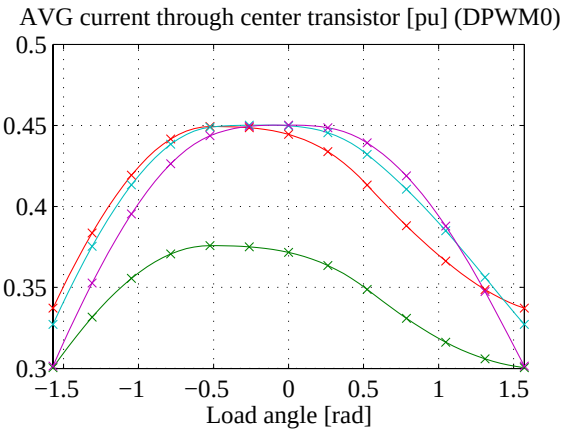


Figure 5.43: *Per unit average current through center transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

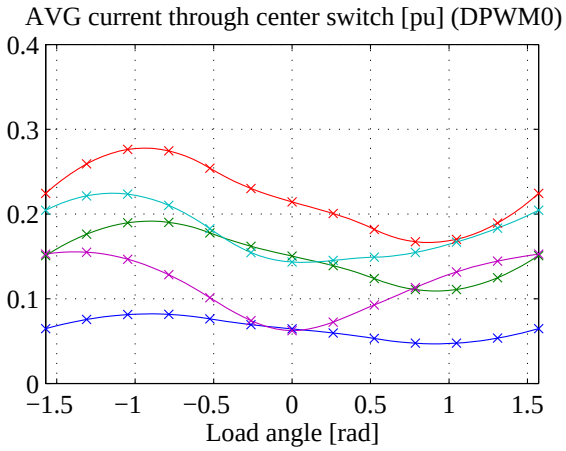


Figure 5.44: *Per unit average current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

the lowest modulation index.

Considering the RMS currents when using the asymmetrical shifted left flat top modulation method, the calculations are to be carried out for three different modulation index ranges.

Modulation index less than 1/2: The RMS current through the top (and bottom) transistors when the modulation index is below 0.5 is given by:

$$I_{t1} = \begin{cases} \sqrt{\frac{\left(10\,M-6\,\sqrt{3}\right)\cos(\phi)^2+\left(M\sqrt{3}-3\right)\sin(|2\phi|)+5\,\pi-6|\phi|+3\,\sqrt{3}-11M}{12\sqrt{3}\pi}}I_r & -\frac{\pi}{2}\leq\phi\leq-\frac{\pi}{6} \\ \sqrt{\frac{\left(\sqrt{3}M-3\right)\sin(|2\phi|)-2M\cos(\phi)^2+4M\sqrt{3}\cos(\phi)-4M\sin(|\phi|)+\frac{3\pi}{2}+3|\phi|-5M}{6\sqrt{3}\pi}}I_r & -\frac{\pi}{6}<\phi\leq 0 \\ \sqrt{\frac{\left(6-2\,M\sqrt{3}\right)\sin(|2\phi|)-4\,M\cos(\phi)^2+8\,M\sqrt{3}\cos(\phi)+8\,M\sin(|\phi|)-10\,M+3\,\pi-6|\phi|}{12\pi}}I_r & 0<\phi\leq\frac{\pi}{6} \\ \sqrt{\frac{\left(6-\frac{14}{\sqrt{3}}M\right)\cos(\phi)^2+\left(\frac{1}{\sqrt{3}}+M\right)\sin(|2\phi|)+8M\left(\cos(\phi)-\frac{1}{\sqrt{3}}\sin(|\phi|)\right)-3+\frac{\pi+6|\phi|+M}{\sqrt{3}}}{4\sqrt{3}\pi}}I_r & \frac{\pi}{6}<\phi\leq\frac{\pi}{2} \end{cases} \tag{5.119}$$

while the RMS current through the top (and bottom) diodes can be calculated by:

$$I_{d1} = \sqrt{\frac{3\pi - 9M + 2\sqrt{3}M\sin(|2\phi|)}{6\pi}I_r^2 - I_{t1}^2} \tag{5.120}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between $1/2$ and $1/\sqrt{3}$ and when using the asymmetrical shifted left flat top modulation method,

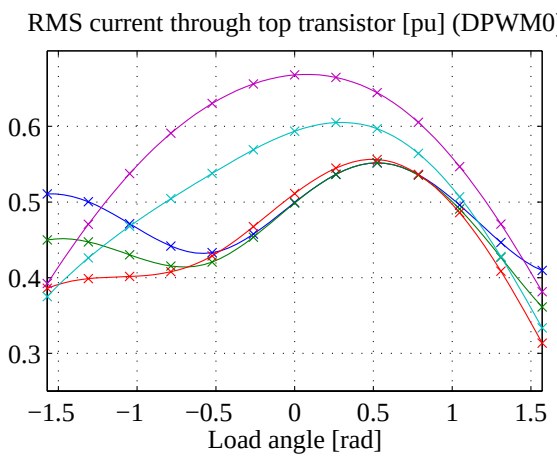


Figure 5.45: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

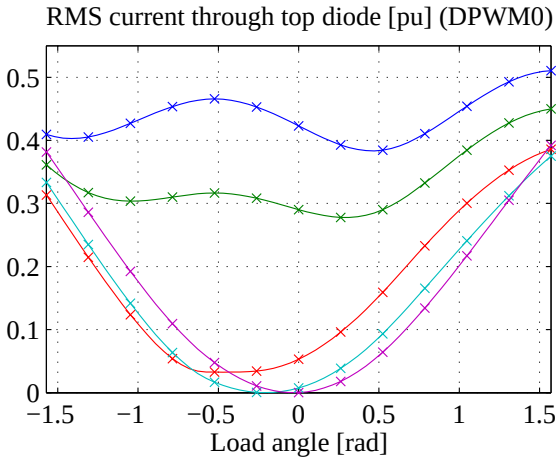


Figure 5.46: *Per unit RMS current through top diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

the RMS current through the transistors in the top (and bottom) switch becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(4M^2-1\right)\cos(\phi)^2+\sqrt{3}\left(2M^2-\frac{1}{2}\right)\sin(|2\phi|)+10M^2+\frac{1}{2}\right)}{12\pi M} + \right. \\ \left. \frac{M^2\left(10\cos(\phi)^2+\sqrt{3}\sin(|2\phi|)-11\right)+6M\left(2\theta_D-\frac{\pi}{6}-\sqrt{3}\cos(\phi)^2+\frac{\sqrt{3}}{2}-|\phi|-\frac{1}{2}\sin(|2\phi|)\right)}{12\pi M} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} \le \phi \le -\frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(M^2\left(\sqrt{3}\sin(|2\phi|)+2\cos(\phi)^2+5\right)-\frac{\sqrt{3}}{4}\sin(|2\phi|)-\frac{1}{2}\cos(\phi)^2+\frac{1}{4}\right)}{6\pi M} + \right. \\ \left. \frac{M^2\left(\sqrt{3}\sin(|2\phi|)-2\cos(\phi)^2-5+4\sqrt{3}\cos(\phi)-4\sin(|\phi|)\right)+3M\left(2\theta_D+|\phi|-\frac{\pi}{2}-\sin(|2\phi|)\right)}{6\pi M} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi \le 0 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\sqrt{3}\left(1-4M^2\right)\sin(|2\phi|)+\left(8M^2-2\right)\cos(\phi)^2+20M^2+1\right)+6M(4\theta_D-\pi)}{24\pi M} + \right. \\ \left. \frac{4M^2\left(4\sqrt{3}\cos(\phi)+4\sin(|\phi|)-\sqrt{3}\sin(|2\phi|)-2\cos(\phi)^2-5\right)+12M(\sin(|2\phi|)-|\phi|)}{24\pi M} \right)^{\frac{1}{2}} I_r & 0 < \phi \le \frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^2-2\right)\cos(\phi)^2+\left(\sqrt{3}-4M^2\right)\sin(|2\phi|)+20M^2+1\right)}{24\pi M} + \right. \\ \frac{2M^2\left(\sqrt{3}\sin(|2\phi|)-14\cos(\phi)^2-8\sin(|\phi|)+8\sqrt{3}\cos(\phi)+1\right)}{24\pi M} + \\ \left. \frac{2M\left(6\sqrt{3}\cos(\phi)^2+3\sin(|2\phi|)-3\sqrt{3}+12\theta_D-5\pi+6|\phi|\right)}{24\pi M} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < \phi \le \frac{\pi}{2} \end{cases} \tag{5.121}$$

while the RMS current through the top (and bottom) diode becomes:

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^2-2\right)\cos(\phi)^2+\left(\sqrt{3}-4M^2\right)\sin(|2\phi|)+20M^2+1\right)}{12\pi M} + \right. \right. \\ \left. \left. \frac{M^2\left(4\sqrt{3}\sin(|2\phi|)-18\right)+6M(4\theta_D-\pi)}{12\pi M} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \tag{5.122}$$

Modulation index higher than $1/\sqrt{3}$: If the modulation index is above $1/\sqrt{3}$, the

RMS current through the transistors and diodes in the top and bottom switch becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2\sqrt{3}\left(M-4M^3\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{M^3\left(28\sqrt{3}\sin(|2\phi|)+24\cos(\phi)^2-12\right)-\sin(|2\phi|)+\sqrt{3}-2\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \\ \left. \frac{M^2\left(24\theta_D-24\phi+6\sqrt{3}-30\sin(|2\phi|)+4\pi-12\sqrt{3}\cos(\phi)^2\right)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} \le \phi \le -\frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(M-4M^3\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{8M^3\left(4\sqrt{3}\sin(|2\phi|)+4\sqrt{3}\cos(\phi)-4\cos(\phi)^2-1-4\sin(|\phi|)\right)-2\sqrt{3}\cos(\phi)^2+\sqrt{3}}{48\pi M^2} + \\ \left. \frac{M^2\left(24\phi-6\sqrt{3}+12\sqrt{3}\cos(\phi)^2-42\sin(|2\phi|)-4\pi+24\theta_D\right)-\sin(|2\phi|)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi \le 0 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{32M^3\left(\sqrt{3}\cos(\phi)+\sin(|\phi|)-\frac{1}{4}-\sqrt{3}\sin(|2\phi|)-\cos(\phi)^2\right)-2\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \\ \left. \frac{M^2\left(12\sqrt{3}\cos(\phi)^2+42\sin(|2\phi|)+24\theta_D-4\pi-24|\phi|-6\sqrt{3}\right)+\sin(|2\phi|)+\sqrt{3}}{48\pi M^2} \right)^{\frac{1}{2}} I_r & 0 < \phi \le \frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{4M^3\left(9-5\sqrt{3}\sin(|2\phi|)-18\cos(\phi)^2+8\sqrt{3}\cos(\phi)-8\sin(|\phi|)\right)-2\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \\ \left. \frac{6M^2\left(4\theta_D-3\sqrt{3}-2\pi+4\sqrt{3}\cos(\phi)^2+6\phi+5\sin(|2\phi|)\right)+\sin(|2\phi|)+\sqrt{3}}{48\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < \phi \le \frac{\pi}{2} \end{cases} \tag{5.123}$$

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+20M^3+M\right)}{24\pi M^2} + \right. \right. \\ \frac{-4M^3\left(4\cos(\phi)^2+4\sqrt{3}\sin(|2\phi|)+1\right)-2\sqrt{3}\cos(\phi)^2+\sin(|2\phi|)+\sqrt{3}}{24\pi M^2} + \\ \left. \left. \frac{4M^2\left(6\theta_D+3\sqrt{3}\cos(\phi)^2+9\sin(|2\phi|)-1\pi-\frac{2}{3}\sqrt{3}\right)}{24\pi M^2} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \tag{5.124}$$

Fig. 5.45 shows the RMS current I_{t1} through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.119), (5.121) and (5.123). Similarly, Fig. 5.46 shows the RMS current I_{d1} through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.120), (5.122) and (5.124). In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. To validate the closed form expressions, the transistor- and diode current was derived from numerical simulations. These results are shown by the marks in Fig 5.45 and Fig. 5.46.

By use of the expressions for RMS currents through the top (and bottom) transistor and diode, the RMS current I_{t3} through the center transistor can be calculated from eq. (5.83). Fig. 5.47 shows the RMS current I_{t3} through the center transistors as a

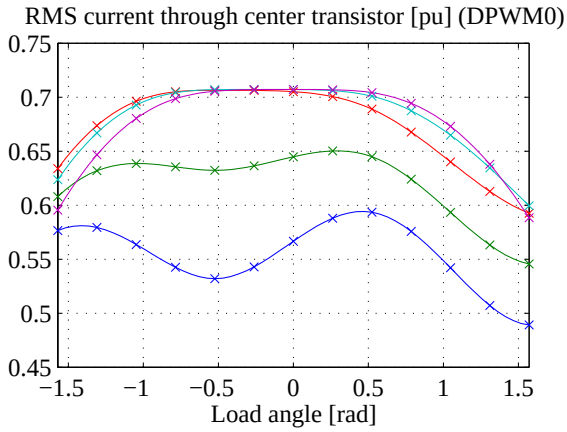


Figure 5.47: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

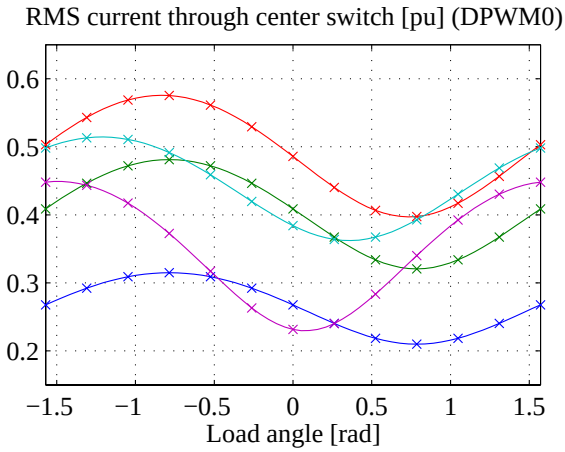


Figure 5.48: *Per unit RMS current through center transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

function of the load angle. Similarly, the current I'_{d3} through the clamping diode can be calculated by use of eq. (5.85). Fig. 5.48 shows the RMS current I'_{d3} through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

Symmetrical flat top modulation (DPWM1)

Using the switching pattern for the symmetrical flat top modulation, cf. Table V and the modulation functions given by eq. (5.6) - eq. (5.9) the average current through the top (and bottom) transistors and diodes can be calculated by piecewise integration. The average current $I_{d1,avg}$ through the top diode is given by:

$$I_{d1,avg} = I_{t1,avg} - \left(\frac{\sqrt{6}}{6} M \cos(\phi)\right) I_r \tag{5.125}$$

while the expression for the average current $I_{t1,avg}$ through the top transistor are to be calculated by either eq. (5.126), eq. (5.127) or eq. (5.128), depending on the modulation index.

Modulation index lower than 1/2: If the modulation index is lower than 1/2, the average currents through the top transistor can be derived by:

$$I_{t1,avg} = \begin{cases} \frac{\sqrt{2}\left(2+M\phi\sqrt{3}\cos(\phi)-M\left(\phi+\sqrt{3}\right)\sin(|\phi|)\right)}{4\pi} I_r & |\phi| \leq \frac{\pi}{3} \\ \frac{\sqrt{2}\left(6+M\pi\sqrt{3}\cos(\phi)-M\left(\pi+3\sqrt{3}\right)\sin(|\phi|)\right)}{12\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.126}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between $1/2$ and $1/\sqrt{3}$, the average currents through the top transistor can be derived by:

$$I_{t1,avg} = \begin{cases} \frac{2\sqrt{3}M^2\left(\left(\pi-2\theta_D+|\phi|-\frac{2}{\sqrt{3}}\right)\cos(\phi)-\left(1+\frac{2}{\sqrt{3}}|\phi|\right)\sin(|\phi|)\right)}{4\sqrt{2}\pi M}+ & \\ \frac{M\left(\left(4-\sqrt{\frac{4M^2-1}{M^2}}\sqrt{3}\right)\cos(\phi)+4\right)-\cos(\phi)}{4\sqrt{2}\pi M}I_r & |\phi| \leq \theta_2 \\ \frac{2M^2\left(\sqrt{3}(2\pi-3|\phi|)\cos(\phi)+\left(\pi+3\sqrt{3}-6\theta_D+3\phi\right)\sin(|\phi|)\right)}{12\sqrt{2}\pi M}+ & \\ \frac{M\left(12\cos(\phi)-3\sqrt{\frac{4M^2-1}{M^2}}\sin(|\phi|)-12\right)+3\sqrt{3}\sin(|\phi|)}{12\sqrt{2}\pi M}I_r & \theta_2 < |\phi| \leq \frac{\pi}{3} \\ \frac{2M^2\left(\frac{\pi}{\sqrt{3}}\cos(\phi)+\left(\sqrt{3}-2\theta_D+\frac{2}{3}\pi\right)\sin(|\phi|)\right)}{4\sqrt{2}\pi M}+ & \\ \frac{M\left(4-\left(\sqrt{\frac{4M^2-1}{M^2}}+4\sqrt{3}\right)\sin(|\phi|)\right)+\sqrt{3}\sin(|\phi|)}{4\sqrt{2}\pi M}I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.127}$$

Modulation index higher than $1/\sqrt{3}$: If the modulation index higher than and $1/\sqrt{3}$, the average currents through the top transistor can be derived by:

$$I_{t1,avg} = \begin{cases} \frac{2M^2\left(\left(\sqrt{3}\pi-2\sqrt{3}\theta_D+\sqrt{3}|\phi|-2\right)\cos(\phi)-\left(|\phi|+\sqrt{3}\right)\sin(|\phi|)\right)}{4\sqrt{2}\pi M}+ & \\ \frac{M\left(\left(4-\sqrt{\frac{4M^2-1}{M^2}}\sqrt{3}\right)\cos(\phi)+4\right)-\cos(\phi)}{4\sqrt{2}\pi M}I_r & |\phi| \leq \theta_1 \\ \frac{2M^2\left(\sqrt{3}(2\pi-3|\phi|)\cos(\phi)+3\left(|\phi|-2\theta_D+\sqrt{3}+\frac{\pi}{3}\right)\sin(|\phi|)\right)}{12\sqrt{2}\pi M}+ & \\ \frac{M\left(12\cos(\phi)-3\sqrt{\frac{4M^2-1}{M^2}}\sin(|\phi|)-12\right)+3\sqrt{3}\sin(|\phi|)}{12\sqrt{2}\pi M}I_r & \theta_1 < |\phi| \leq \frac{\pi}{3} \\ \frac{2M^2\left(\pi\sqrt{3}\cos(\phi)+\left(3\sqrt{3}-6\theta_D+2\pi\right)\sin(|\phi|)\right)}{12\sqrt{2}\pi M}+ & \\ \frac{M\left(12-\left(12\sqrt{3}+-3\sqrt{\frac{4M^2-1}{M^2}}\right)\sin(|\phi|)\right)+3\sqrt{3}\sin(|\phi|)}{12\sqrt{2}\pi M}I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.128}$$

Fig. 5.49 shows the average current $I_{t1,avg}$ through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.126), (5.127) and (5.128). The currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. Similarly, Fig. 5.50 shows the average current $I_{d1,avg}$ through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.125). To validate the closed form expressions, the transistor- and diode current has been obtained from numerical simulations. These results are shown by the marks in Fig.5.49 and Fig. 5.50.

By use of the expressions for currents trough the top (and bottom) transistor and diode, the average current $I_{t3,avg}$ through the center transistor can be calculated from

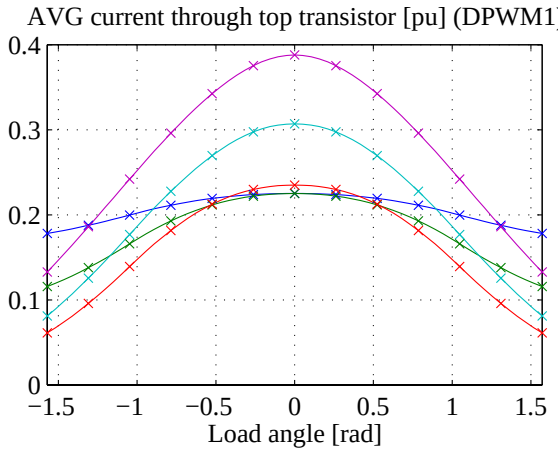


Figure 5.49: *Per unit average current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

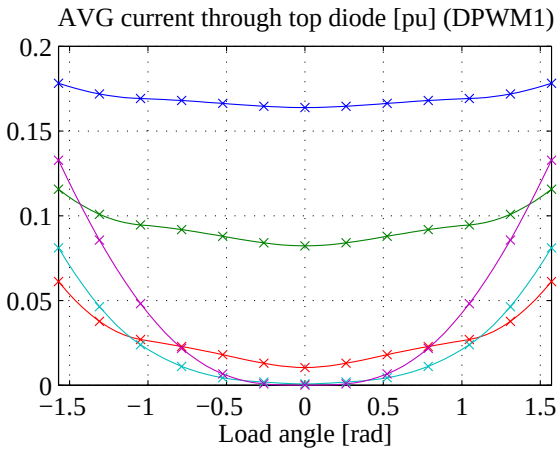


Figure 5.50: *Per unit average current through top diode as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

eq. (5.82). Fig. 5.51 shows the average current $I_{t3,avg}$ through the center transistors as a function of the load angle. Similarly, the current $I'_{d3,avg}$ through the clamping diode can be calculated by use of eq. (5.84). Fig. 5.52 shows the average current $I'_{t3,avg}$ through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

Similarly to the average currents through the top (and bottom) transistors and diodes, the RMS values can be derived.

Modulation index lower than 1/2: For instance, if the modulation index is less than 1/2, the RMS current through the top transistor and diode becomes:

$$I_{t1} = \begin{cases} \sqrt{\frac{(6-4M)\cos(\phi)^2+\frac{4M-1}{\sqrt{3}}\sin(|2\phi|)+4M\left(2\cos(\phi)-\frac{2}{\sqrt{3}}\sin(|\phi|)-1\right)+\frac{6|\phi|+2\pi}{\sqrt{3}}-3}{12\pi}}\, I_r & |\phi| \leq \frac{\pi}{3} \\ \sqrt{\frac{2\,M\sqrt{3}\cos(\phi)^2+(4\,M-3)\sin(|2\phi|)-4\,M\sqrt{3}+3\,\pi-3|\phi|}{6\sqrt{6}\pi}}\, I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.129}$$

$$I_{d1} = \sqrt{\left(\frac{3\,\pi-8\,M\sqrt{3}+4\,M\sqrt{3}\cos(\phi)^2}{6\pi}\right) I_r^2 - I_{t1}^2} \tag{5.130}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between 1/2 and $1/\sqrt{3}$, the RMS current through the transistors in the top and bottom switch

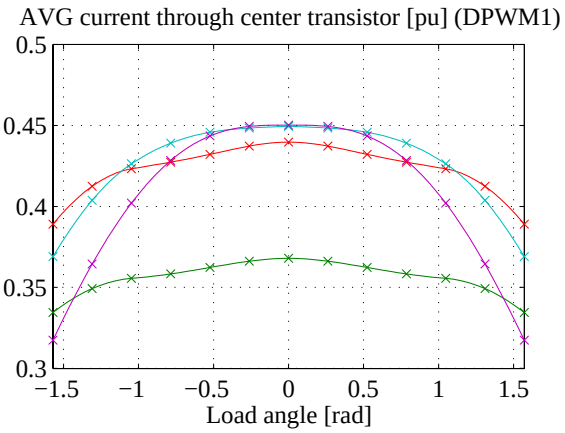


Figure 5.51: *Per unit average current through center transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

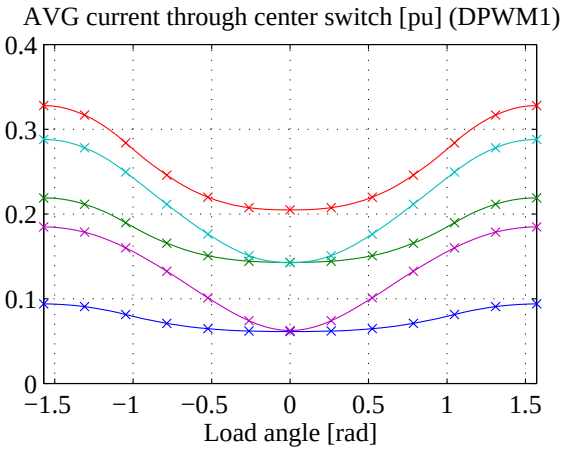


Figure 5.52: *Per unit average current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+20M^3+M\right)}{24\sqrt{6}\pi M^2} + \right. \\ \frac{8M^3\left(\sin(|2\phi|)-5\sqrt{3}\cos(\phi)^2-2\sin(|\phi|)+2\sqrt{3}\cos(\phi)+\sqrt{3}\right)}{24\sqrt{6}\pi M^2} + \\ \left. \frac{M^2\left(36\sqrt{3}\cos(\phi)^2-6\sin(|2\phi|)+24\theta_D-8\pi-18\sqrt{3}+12|\phi|\right)-2\sqrt{3}\cos(\phi)^2+\sqrt{3}}{24\sqrt{6}\pi M^2} \right)^{\frac{1}{2}} I_r & |\phi| \leq \frac{\pi}{3} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+20M^3+M\right)+8M^3\left(2\sin(|2\phi|)-3\sqrt{3}\cos(\phi)^2\right)}{24\sqrt{6}\pi M^2} + \right. \\ \left. \frac{12M^2\left(2\sqrt{3}\cos(\phi)^2-\sin(|2\phi|)-|\phi|+2\theta_D-\sqrt{3}\right)-2\sqrt{3}(\cos(\phi))^2+\sqrt{3}}{24\sqrt{6}\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \quad (5.131)$$

while the diode current through the top (and bottom) diode becomes:

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(M-4M^3\right)\cos(\phi)^2-10M^3-\frac{M}{2}\right)+12M^3\sqrt{3}\cos(\phi)^2}{6\pi M^2} + \right. \right. \\ \left. \left. \frac{3M^2\left(\pi+2\sqrt{3}-4\theta_D-4\sqrt{3}\cos(\phi)^2\right)+\sqrt{3}\cos(\phi)^2-\frac{\sqrt{3}}{2}}{6\pi M^2} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \quad (5.132)$$

Modulation index higher than $1/\sqrt{3}$: If the modulation index is above $1/\sqrt{3}$, the

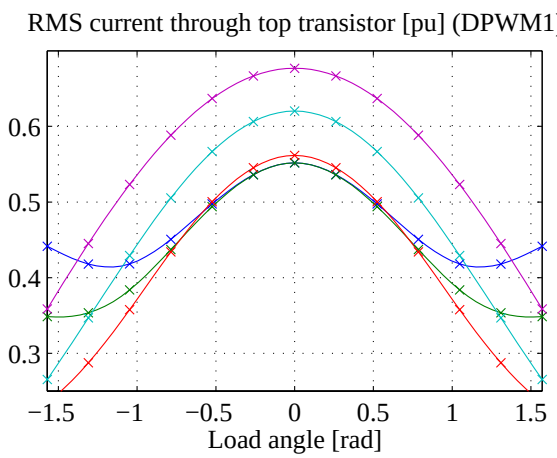


Figure 5.53: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15,\ 0.35\ ...0.95]$.*

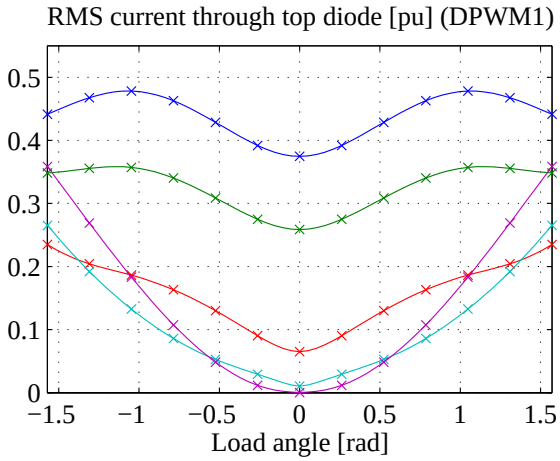


Figure 5.54: *Per unit RMS current through top diode as a function of the load angle. $M \in [0.15,\ 0.35\ ...0.95]$.*

RMS current through the transistors in the top and bottom switch becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+20M^3+M\right)+\sqrt{3}-2\sqrt{3}\cos(\phi)^2}{24\sqrt{6}\pi M^2} + \right. & \\ \frac{8M^3\left(\sin(|2\phi|)-5\sqrt{3}\cos(\phi)^2-2\sin(|\phi|)+2\sqrt{3}\cos(\phi)+\sqrt{3}\right)}{24\sqrt{6}\pi M^2} + & \\ \left. \frac{2M^2\left(18\sqrt{3}\cos(\phi)^2-3\sin(|2\phi|)+12\theta_D-4\pi+6|\phi|-9\sqrt{3}\right)}{24\sqrt{6}\pi M^2} \right)^{\frac{1}{2}} I_r & |\phi| \leq \frac{\pi}{3} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+20M^3+M\right)+8M^3\left(2\sin(|2\phi|)-3\sqrt{3}\cos(\phi)^2\right)}{24\sqrt{6}\pi M^2} + \right. & \\ \left. \frac{12M^2\left(2\sqrt{3}\cos(\phi)^2-\sin(|2\phi|)-|\phi|+2\theta_D-\sqrt{3}\right)-2\sqrt{3}\cos(\phi)^2+\sqrt{3}}{24\sqrt{6}\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \quad (5.133)$$

while the diode current through the top (and bottom) diode becomes:

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+20M^3+M\right)-24M^3\sqrt{3}\cos(\phi)^2}{12\pi M^2} + \right. \right. \\ \left. \left. \frac{6M^2\left(4\theta_D-\pi-2\sqrt{3}+4\sqrt{3}\cos(\phi)^2\right)-2\sqrt{3}\cos(\phi)^2+\sqrt{3}}{12\pi M^2} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \quad (5.134)$$

Fig. 5.53 shows the RMS current I_{t1} through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.129), (5.131) and (5.133). Similarly, Fig. 5.54 shows the RMS current I_{d1} through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.130), (5.132) and (5.134). In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. To validate the closed form expressions, the transistor- and diode current was derived from numerical simulations. These results are shown by the marks in Fig 5.53 and Fig. 5.54.

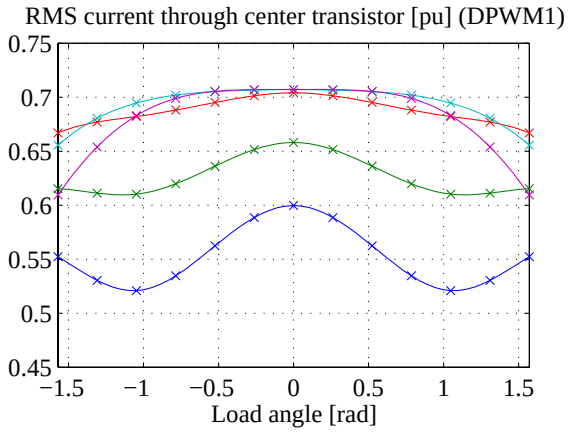


Figure 5.55: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ...0.95]$.*

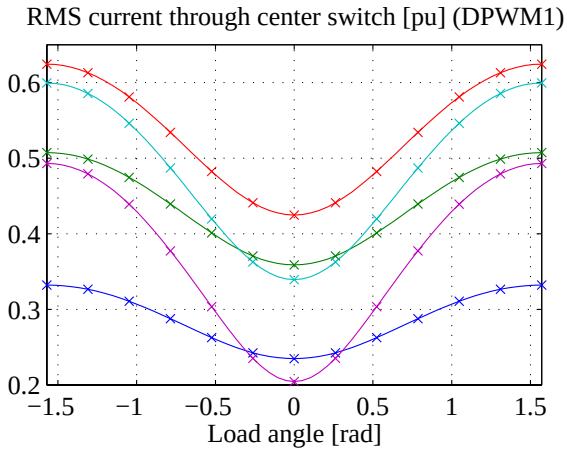


Figure 5.56: *Per unit RMS current through center transistor as a function of the load angle. $M \in [0.15, 0.35 ...0.95]$.*

By use of the expressions for RMS currents through the top (and bottom) transistor and diode, the RMS current I_{t3} through the center transistor can be calculated from eq. (5.83). Fig. 5.55 shows the RMS current I_{t3} through the center transistors as a function of the load angle. Similarly, the current I'_{d3} through the clamping diode can be calculated by use of eq. (5.85). Fig. 5.56 shows the RMS current I'_{d3} through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

Asymmetrical shifted right flat top modulation (DPWM2)

Considering the asymmetrical shifted right flat top modulation given by the lower part of Table V, the average current through the top diode is given by:

$$I_{d1,avg} = I_{t1,avg} - \left(\frac{\sqrt{6}}{6} M \cos(\phi)\right) I_r \tag{5.135}$$

while the average current through the top diode has to be calculated separately for three different modulation index ranges.

Modulation index less than 1/2: If the modulation index is less than 1/2, the average current $I_{t1,avg}$ can be calculated by:

$$I_{t1,avg} = \begin{cases} \frac{\sqrt{2}\left(M\left(3-\pi\sqrt{3}+6|\phi|\sqrt{3}\right)\cos(\phi)+M\left(\pi-6|\phi|-3\sqrt{3}\right)\sin(|\phi|)+12\right)}{24\pi} I_r & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \\ \frac{\sqrt{2}\left(M\left(\pi\sqrt{3}-6|\phi|\sqrt{3}-6\right)\cos(\phi)+M\left(\pi+6\sqrt{3}-6|\phi|\right)\sin(|\phi|)+12\right)}{24\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ \frac{M\left(\sqrt{3}\pi+6\sqrt{3}|\phi|-6\right)\cos(\phi)-M\left(6\sqrt{3}+\pi+6|\phi|\right)\sin(|\phi|)+12}{12\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{M\left(2\sqrt{3}\pi-9\right)\cos(\phi)-M\left(2\pi+3\sqrt{3}\right)\sin(|\phi|)+12}{12\sqrt{2}\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.136}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between 1/2 and $1/\sqrt{3}$, the average current through the transistors in the top (and bottom) switch becomes:

$$I_{t1,avg} = \begin{cases} \frac{\sqrt{6}\left(\sqrt{3}M+3\sqrt{\frac{4M^2-1}{M^2}}-7M\pi+12M\theta_D+6M|\phi|\right)\cos(\phi)}{24\pi}+ \\ \frac{\sqrt{2}\left(7M\pi-3\sqrt{\frac{4M^2-1}{M^2}}-12M\theta_D-3M\sqrt{3}-6M|\phi|\right)\sin(|\phi|)+12\sqrt{2}}{24\pi} I_r & -\frac{\pi}{2} < \phi \leq -\theta_3 \\ \frac{\sqrt{6}\left(\frac{1}{\sqrt{3}}+M^2\left(\frac{5}{\sqrt{3}}+\pi-2|\phi|\right)\right)\cos(\phi)}{8\pi M}+ \\ \frac{\sqrt{6}\left(1+M^2\left(\frac{2}{\sqrt{3}}|\phi|-\frac{\pi}{\sqrt{3}}+3\right)\right)\sin(|\phi|)-4\sqrt{2}M}{8M\pi} I_r & -\theta_3 < \phi \leq -\theta_2 \\ \frac{\sqrt{6}\left(5M\pi-3\sqrt{\frac{4M^2-1}{M^2}}-12M\theta_D+\sqrt{3}M+6M|\phi|\right)\cos(\phi)}{24\pi}+ \\ \frac{\sqrt{2}\left(3\sqrt{\frac{4M^2-1}{M^2}}-5M\pi+12M\theta_D-6M|\phi|-3M\sqrt{3}\right)\sin(|\phi|)+12\sqrt{2}}{24\pi} I_r & -\theta_2 < \phi \leq -\frac{\pi}{6} \\ \frac{\sqrt{6}\left(7M\pi-3\sqrt{\frac{4M^2-1}{M^2}}-12M\theta_D-6M|\phi|-\frac{6}{\sqrt{3}}M\right)\cos(\phi)}{24\pi}+ \\ \frac{\sqrt{2}\left(6M\sqrt{3}-5M\pi+3\sqrt{\frac{4M^2-1}{M^2}}+12M\theta_D-6M|\phi|\right)\sin(|\phi|)+12\sqrt{2}}{24\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ \frac{M\left(\frac{5\pi}{6}-\sqrt{3}-\sqrt{\frac{4M^2-1}{4M^4}}-2\theta_D-|\phi|\right)\sin(|\phi|)}{2\sqrt{2}\pi}+ \\ \frac{\sqrt{3}M\left(\frac{7\pi}{6}-\sqrt{\frac{4M^2-1}{4M^4}}-2\theta_D-\frac{1}{\sqrt{3}}+|\phi|\right)\cos(\phi)+2}{2\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{M\left(4\pi-12\theta_D-3\sqrt{\frac{4M^2-1}{M^4}}-3\sqrt{3}\right)\sin(|\phi|)}{12\sqrt{2}\pi}+ \\ \frac{M\left(8\pi\sqrt{3}-3\sqrt{3}\sqrt{\frac{4M^2-1}{M^4}}-12\theta_D\sqrt{3}-9\right)\cos(\phi)+12}{12\sqrt{2}\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.137}$$

Modulation index higher than $1/\sqrt{3}$: If the modulation index is higher than $1/\sqrt{3}$,

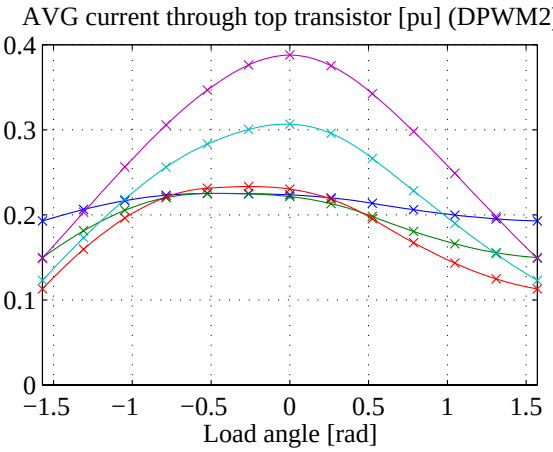


Figure 5.57: *Per unit average current through top transistor as a function of the load angle. $M \in [0.15,\ 0.35\ ...0.95]$.*

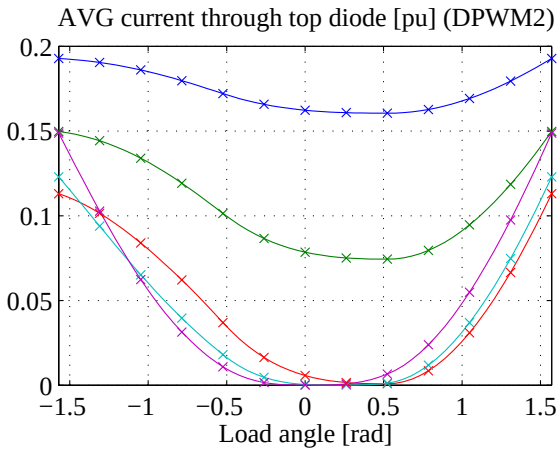


Figure 5.58: *Per unit average current through the top diode as a function of the load angle. $M \in [0.15,\ 0.35\ ...0.95]$.*

the average current through the transistors in the top (and bottom) switch becomes:

$$I_{t1,avg} = \begin{cases} \frac{\left(M^2\left(10\pi\sqrt{3}-6-12\phi\sqrt{3}-12\theta_D\sqrt{3}\right)-3\sqrt{\frac{4M^2-1}{M^2}}\sqrt{3}M+24M\sqrt{3}-3\right)\cos(\phi)}{12\sqrt{2}\pi M}+ \\ \frac{\left(M^2\left(12\phi-2\pi-12\theta_D+6\sqrt{3}\right)+24M-3\sqrt{\frac{4M^2-1}{M^2}}M+3\sqrt{3}\right)\sin(|\phi|)-24M}{12\sqrt{2}\pi M}I_r & -\frac{\pi}{2} \le \phi \le -\frac{\pi}{6} \\ \frac{\sqrt{3}\left(M^2\left(10\pi-\frac{12}{\sqrt{3}}-12|\phi|-12\theta_D\right)-3\sqrt{\frac{4M^2-1}{M^2}}M-\sqrt{3}\right)\cos(\phi)}{12\sqrt{2}\pi M}+ \\ \frac{\left(M^2\left(12\sqrt{3}-12|\phi|+2\pi-12\theta_D\right)-3\sqrt{\frac{4M^2-1}{M^2}}M+3\sqrt{3}\right)\sin(|\phi|)+24M}{12\sqrt{2}\pi M}I_r & -\frac{\pi}{6} < \phi \le 0 \\ \frac{\left(4M^2\left(\theta_D-|\phi|-\sqrt{3}-\frac{\pi}{6}\right)+\sqrt{\frac{4M^2-1}{M^2}}M-\sqrt{3}\right)\sin(|\phi|)}{8\sqrt{2}\pi M}+ \\ \frac{\left(4\sqrt{3}M^2\left(|\phi|-\theta_D-\frac{1}{\sqrt{3}}+\frac{5\pi}{6}\right)-\sqrt{3}\sqrt{\frac{4M^2-1}{M^2}}M-1\right)\cos(\phi)+8M}{8\sqrt{2}\pi M}I_r & 0 < \phi \le \theta_1 \\ \frac{\left(12M^2\left(|\phi|+\frac{\pi}{6}-\theta_D+\sqrt{3}\right)-3\sqrt{\frac{4M^2-1}{M^2}}M+3\sqrt{3}\right)\sin(|\phi|)}{24\sqrt{2}\pi M}+ \\ \frac{\left(12M^2\left(\theta_D\sqrt{3}-|\phi|\sqrt{3}+\frac{\pi}{2}\sqrt{3}+1\right)+3\sqrt{\frac{4M^2-1}{M^2}}\sqrt{3}M+3\right)\cos(\phi)-24M}{24\sqrt{2}\pi M}I_r & \theta_1 < \phi \le \frac{\pi}{6} \\ \frac{\left(M^2\left(6\sqrt{3}+4\pi-12\theta_D\right)-24M-3\sqrt{\frac{4M^2-1}{M^2}})M+3\sqrt{3}\right)\sin(|\phi|)}{24\sqrt{2}\pi M}+ \\ \frac{\left(M^2\left(18+4\pi\sqrt{3}+12\theta_D\sqrt{3}\right)+3\sqrt{\frac{4M^2-1}{M^2}}\sqrt{3}M-24M\sqrt{3}+3\right)\cos(\phi)+24M}{24\sqrt{2}\pi M}I_r & \frac{\pi}{6} < \phi \le \frac{\pi}{2} \end{cases} \quad (5.138)$$

Fig. 5.57 shows the average current $I_{t1,avg}$ through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.136), (5.137) and (5.138). The currents are shown for different values of the

modulation index M where the blue curve represents the lowest value of the modulation index. Similarly, Fig. 5.58 shows the average current $I_{d1,avg}$ through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.135). To validate the closed form expressions, the transistor- and diode current has been obtained from numerical simulations. These results are shown by the marks in Fig. 5.57 and Fig. 5.58.

By use of the expressions for the currents trough the top (and bottom) transistor and diode, the average current $I_{t3,avg}$ through the center transistor can be calculated from eq. (5.82). Fig. 5.59 shows the average current $I_{t3,avg}$ through the center transistors as a function of the load angle. Similarly, the current $I'_{d3,avg}$ through the clamping diode can be calculated by use of eq. (5.84). Fig. 5.60 shows the average current $I'_{t3,avg}$ through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

Considering the RMS currents when using the asymmetrical shifted right flat top modulation method, the calculations are to be carried out for three different modulation index ranges.

Modulation index less than 1/2: The RMS current through the top (and bottom) transistors when the modulation index is below 0.5 is given by:

$$I_{t1} = \begin{cases} \sqrt{\frac{\left(6-\frac{14}{\sqrt{3}}M\right)\cos(\phi)^2+\left(\frac{1}{\sqrt{3}}+M\right)\sin(|2\phi|)+8M\left(\cos(\phi)-\frac{1}{\sqrt{3}}\sin(|\phi|)\right)-3+\frac{\pi+6|\phi|+M}{\sqrt{3}}}{4\sqrt{3}\pi}}I_r & -\frac{\pi}{2}\leq\phi\leq-\frac{\pi}{6} \\ \sqrt{\frac{\left(6-2\,M\sqrt{3}\right)\sin(|2\phi|)-4\,M\cos(\phi)^2+8\,M\sqrt{3}\cos(\phi)+8\,M\sin(|\phi|)-10\,M+3\,\pi-6|\phi|}{12\pi}}I_r & -\frac{\pi}{6}<\phi\leq 0 \\ \sqrt{\frac{\left(\sqrt{3}M-3\right)\sin(|2\phi|)-2M\cos(\phi)^2+4M\sqrt{3}\cos(\phi)-4M\sin(|\phi|)+\frac{3\pi}{2}+3|\phi|-5M}{6\sqrt{3}\pi}}I_r & 0<\phi\leq\frac{\pi}{6} \\ \sqrt{\frac{\left(10\,M-6\,\sqrt{3}\right)\cos(\phi)^2+\left(M\sqrt{3}-3\right)\sin(|2\phi|)+5\,\pi-6|\phi|+3\,\sqrt{3}-11M}{12\sqrt{3}\pi}}I_r & \frac{\pi}{6}<\phi\leq\frac{\pi}{2} \end{cases} \tag{5.139}$$

while the RMS current through the top (and bottom) diode can be calculated by:

$$I_{d1} = \sqrt{\frac{3\,\pi-9\,M-2\,M\sqrt{3}\sin(|2\phi|)}{6\pi}I_r^2 - I_{t1}^2} \tag{5.140}$$

Modulation index between 1/2 and $1/\sqrt{3}$: If the modulation index is between $1/2$ and $1/\sqrt{3}$, the RMS current through the transistors in the top and bottom switch

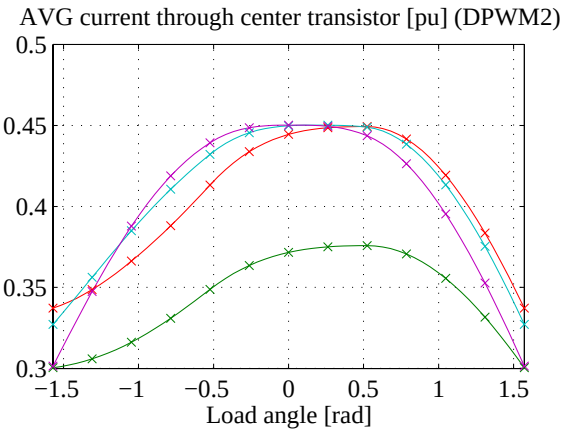


Figure 5.59: *Per unit average current through center transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

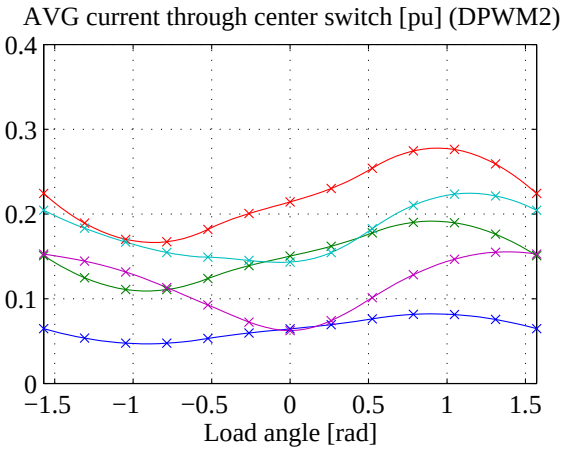


Figure 5.60: *Per unit average current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.95]$.*

becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^2-2\right)\cos(\phi)^2+\left(\sqrt{3}-4M^2\right)\sin(|2\phi|)+20M^2+1\right)}{24\pi M} + \right. \\ \frac{2M^2\left(\sqrt{3}\sin(|2\phi|)-14\cos(\phi)^2-8\sin(|\phi|)+8\sqrt{3}\cos(\phi)+1\right)}{24\pi M} + \\ \left. \frac{2M\left(6\sqrt{3}\cos(\phi)^2+3\sin(|2\phi|)-3\sqrt{3}+12\theta_D-5\pi+6|\phi|\right)}{24\pi M} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} \le \phi \le -\frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\sqrt{3}\left(1-4M^2\right)\sin(|2\phi|)+\left(8M^2-2\right)\cos(\phi)^2+20M^2+1\right)+6M(4\theta_D-\pi)}{24\pi M} + \right. \\ \left. \frac{4M^2\left(4\sqrt{3}\cos(\phi)+4\sin(|\phi|)-\sqrt{3}\sin(|2\phi|)-2\cos(\phi)^2-5\right)+12M(\sin(|2\phi|)-|\phi|)}{24\pi M} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi \le 0 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(M^2\left(\sqrt{3}\sin(|2\phi|)+2\cos(\phi)^2+5\right)-\frac{\sqrt{3}}{4}\sin(|2\phi|)-\frac{1}{2}\cos(\phi)^2+\frac{1}{4}\right)}{6\pi M} + \right. \\ \left. \frac{M^2\left(\sqrt{3}\sin(|2\phi|)-2\cos(\phi)^2-5+4\sqrt{3}\cos(\phi)-4\sin(|\phi|)\right)+3M\left(2\theta_D+|\phi|-\frac{\pi}{2}-\sin(|2\phi|)\right)}{6\pi M} \right)^{\frac{1}{2}} I_r & 0 < \phi \le \frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(4M^2-1\right)\cos(\phi)^2+\sqrt{3}\left(2M^2-\frac{1}{2}\right)\sin(|2\phi|)+10M^2+\frac{1}{2}\right)}{12\pi M} + \right. \\ \left. \frac{M^2\left(10\cos(\phi)^2+\sqrt{3}\sin(|2\phi|)-11\right)+6M\left(2\theta_D-\frac{\pi}{6}-\sqrt{3}\cos(\phi)^2+\frac{\sqrt{3}}{2}-|\phi|-\frac{1}{2}\sin(|2\phi|)\right)}{12\pi M} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < |\phi| \le \frac{\pi}{2} \end{cases} \tag{5.141}$$

and the RMS current through the top diode becomes:

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^2-2\right)\cos(\phi)^2+\left(\sqrt{3}+4M^2\right)\sin(|2\phi|)+20M^2+1\right)}{12\pi M} + \right. \right. \\ \left. \left. \frac{M^2\left(-4\sqrt{3}\sin(|2\phi|)-18\right)+6M(4\theta_D-\pi)}{12\pi M} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \tag{5.142}$$

Modulation higher than $1/\sqrt{3}$: If the modulation index is above $1/\sqrt{3}$, the RMS

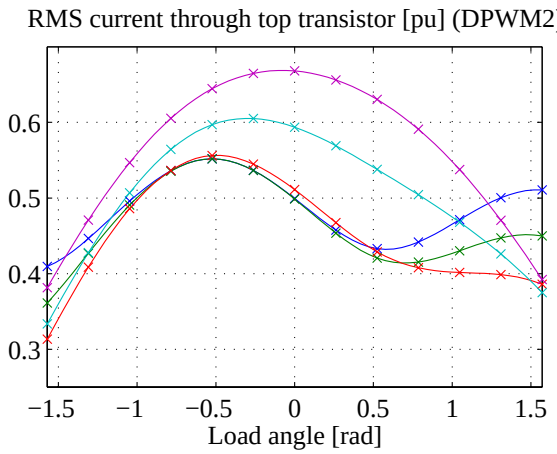


Figure 5.61: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15,\ 0.35\ ...0.95]$.*

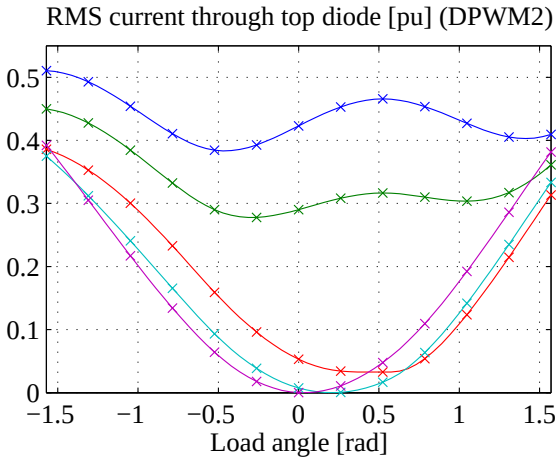


Figure 5.62: *Per unit RMS current through top diode as a function of the load angle. $M \in [0.15,\ 0.35\ ...0.95]$.*

current through the transistors in the top and bottom switch becomes:

$$I_{t1} = \begin{cases} \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{4M^3\left(9-5\sqrt{3}\sin(|2\phi|)-18\cos(\phi)^2+8\sqrt{3}\cos(\phi)-8\sin(|\phi|)\right)-2\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \\ \left. \frac{6M^2\left(4\theta_D-3\sqrt{3}-2\pi+4\sqrt{3}\cos(\phi)^2+6\phi+5\sin(|2\phi|)\right)+\sin(|2\phi|)+\sqrt{3}}{48\pi M^2} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{2} < \phi \le -\frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(4M^3-M\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{32M^3\left(\sqrt{3}\cos(\phi)+\sin(|\phi|)-\frac{1}{4}-\sqrt{3}\sin(|2\phi|)-\cos(\phi)^2\right)-2\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \\ \left. \frac{M^2\left(12\sqrt{3}\cos(\phi)^2+42\sin(|2\phi|)+24\theta_D-4\pi-24|\phi|-6\sqrt{3}\right)+\sin(|2\phi|)+\sqrt{3}}{48\pi M^2} \right)^{\frac{1}{2}} I_r & -\frac{\pi}{6} < \phi \le 0 \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(M-4M^3\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{8M^3\left(4\sqrt{3}\sin(|2\phi|)+4\sqrt{3}\cos(\phi)-4\cos(\phi)^2-1-4\sin(|\phi|)\right)-2\sqrt{3}\cos(\phi)^2+\sqrt{3}}{48\pi M^2} + \\ \left. \frac{M^2\left(24\phi-6\sqrt{3}+12\sqrt{3}\cos(\phi)^2-42\sin(|2\phi|)-4\pi+24\theta_D\right)-\sin(|2\phi|)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & 0 < \phi \le \frac{\pi}{6} \\ \left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2\sqrt{3}\left(M-4M^3\right)\sin(|2\phi|)+20M^3+M\right)}{48\pi M^2} + \right. \\ \frac{M^3\left(28\sqrt{3}\sin(|2\phi|)+24\cos(\phi)^2-12\right)-\sin(|2\phi|)+\sqrt{3}-2\sqrt{3}\cos(\phi)^2}{48\pi M^2} + \\ \left. \frac{M^2\left(24\theta_D-24\phi+6\sqrt{3}-30\sin(|2\phi|)+4\pi-12\sqrt{3}\cos(\phi)^2\right)}{48\pi M^2} \right)^{\frac{1}{2}} I_r & \frac{\pi}{6} < \phi \le \frac{\pi}{2} \end{cases} \tag{5.143}$$

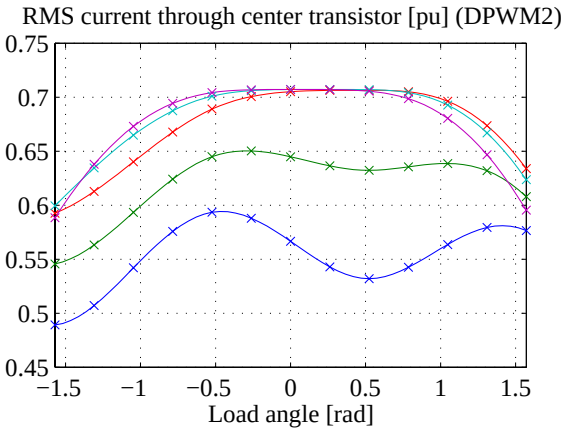


Figure 5.63: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

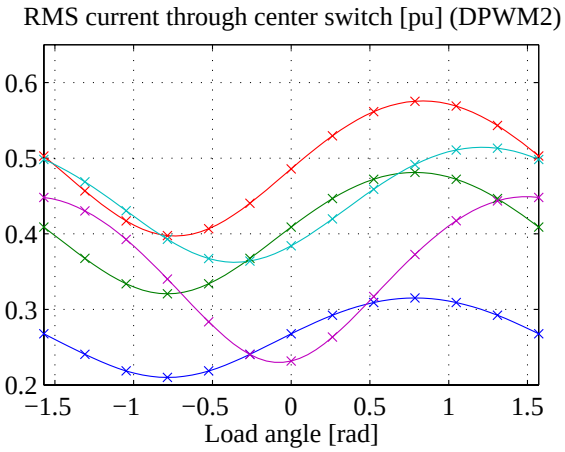


Figure 5.64: *Per unit RMS current through center transistor as a function of the load angle. $M \in [0.15, 0.35 ... 0.95]$.*

The RMS current through the top diode becomes:

$$I_{d1} = \left(\left(\frac{\sqrt{\frac{4M^2-1}{M^2}}\left(\left(8M^3-2M\right)\cos(\phi)^2+\sqrt{3}\left(M-4M^3\right)\sin(|2\phi|)+20M^3+M\right)}{24\pi M^2} + \frac{M^3\left(16\sqrt{3}\sin(|2\phi|)-16\cos(\phi)^2-4\right)-2\sqrt{3}\cos(\phi)^2-\sin(|2\phi|)+\sqrt{3}}{24\pi M^2} + \frac{M^2\left(12\sqrt{3}\cos(\phi)^2-4\pi+24\theta_D-18\sin(|2\phi|)-6\sqrt{3}\right)}{24\pi M^2} \right) I_r^2 - I_{t1}^2 \right)^{\frac{1}{2}} \tag{5.144}$$

Fig. 5.61 shows the RMS current I_{t1} through the top (and bottom) transistors as a function of the load angle, i.e. the current calculated by the expressions given by eq. (5.139), (5.141) and (5.143). Similarly, Fig. 5.62 shows the RMS current I_{d1} through the top (and bottom) diode as a function of the load angle, i.e. the current calculated by eq. (5.140), (5.142) and (5.144). In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest value of the modulation index. To validate the closed form expressions, the transistor- and diode current was derived from numerical simulations. These results are shown by the marks in Fig. 5.61 and Fig. 5.62.

By use of the expressions for the RMS currents through the top (and bottom) transistor and diode, the RMS current I_{t3} through the center transistor can be calculated from eq. (5.83). Fig. 5.63 shows the RMS current I_{t3} through the center transistors as a function of the load angle. Similarly, the current I'_{d3} through the clamping diode can be calculated by use of eq. (5.85). Fig. 5.64 shows the RMS current I'_{d3} through the clamping diode as a function of the load angle. In both figures, the currents are shown for different values of the modulation index M where the blue curve represents the lowest modulation index.

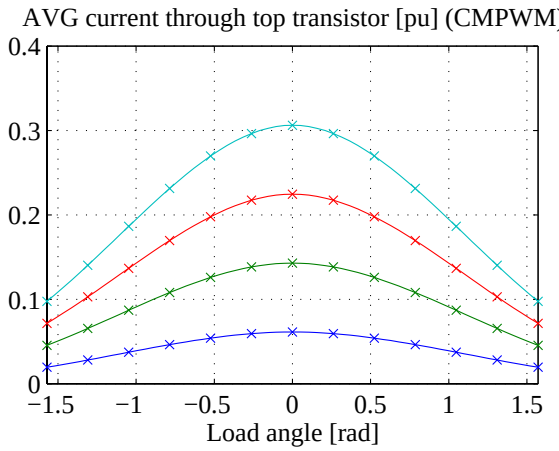


Figure 5.65: *Per unit average current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ...0.75]$.*

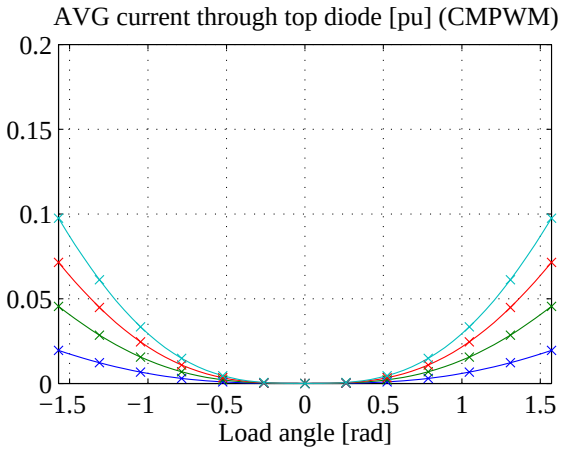


Figure 5.66: *Per unit average current through top diode as a function of the load angle. $M \in [0.15, 0.35 ...0.75]$.*

Common mode voltage elimination modulation (CMPWM)

As the modulation scheme with common-mode voltage elimination only operates with six active vectors and one zero vector, the derivation of the currents through the individual switches becomes far more simple compared to the previously discussed modulation strategies. Although the present modulation strategy in many aspects are very different from the conventional methods, the relations given by eq. (5.80) - eq. (5.87) between currents through the different switches are still valid and hence the only expressions to be derived are those describing the currents through the top transistor T_1 and top diode D_1. The average current $I_{t1,avg}$ through the top transistor is given by:

$$I_{t1,avg} = \frac{\sqrt{3}M\sqrt{2}\left(\sin\left(|\phi|\right) + \cos\left(\phi\right)\pi - \cos\left(\phi\right)|\phi|\right)}{6\pi} \tag{5.145}$$

while the average current $I_{d1,avg}$ through the top diode is given by:

$$I_{d1,avg} = \frac{\sqrt{3}M\sqrt{2}\left(\sin\left(|\phi|\right) - \cos\left(\phi\right)|\phi|\right)}{6\pi} \tag{5.146}$$

Like for the modulation schemes based on the conventional space vector approach, the expressions in eq. (5.145) and eq. (5.146) are only valid when active power flows from the DC-link and out of the inverter. For a power flow entering the inverter, the expressions in eq. (5.145) and eq. (5.146) are to be exchanged. Fig. 5.65 shows the average current $I_{t1,avg}$ through the top transistor as a function of the load angle and plotted for different modulation indexes. The continuous line represents the current values calculated by eq. (5.145) while the values presented by marks are derived from numerical simulations of the three-level inverter. Similarly, Fig. 5.66 shows the average current through the top diode. Using the expressions given by eq. (5.80), (5.82), (5.84) and (5.86) the average current through the remaining switches can be calculated. Fig. 5.67 shows the average current through the center transistor T_3 when using the diode

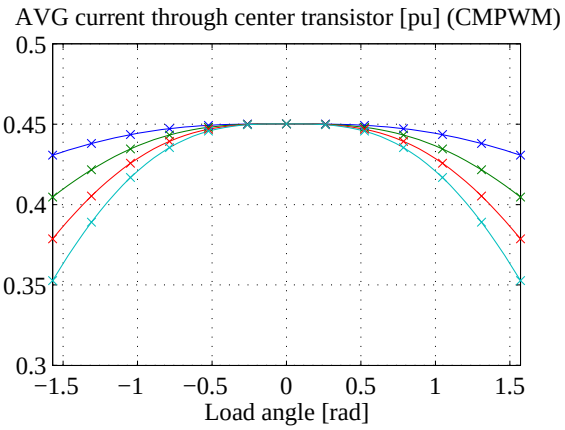


Figure 5.67: *Per unit average current through center transistor as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.75]$.*

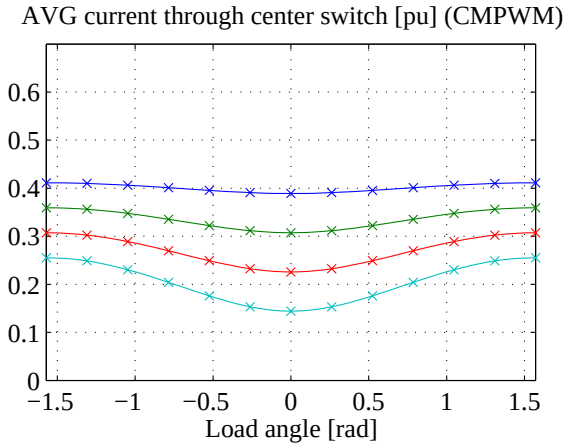


Figure 5.68: *Per unit average current through clamping diode as a function of the load angle. $M \in [0.15, 0.35 \ldots 0.75]$.*

clamped topology whereas Fig. 5.68 shows the average current through the clamping diode D_3'. Considering the RMS current through the top transistor when using the modulation scheme with common-mode voltage elimination, this is given by:

$$I_{t1} = \frac{\sqrt{2}\sqrt[4]{3}\sqrt{M\left(\cos\left(\phi\right)+1\right)^2}}{3\sqrt{\pi}} \tag{5.147}$$

whereas the RMS current through the top diode is given by:

$$I_{d1} = \frac{\sqrt{2}\sqrt[4]{3}\sqrt{M\left(\cos\left(\phi\right)-1\right)^2}}{\sqrt{3\pi}} \tag{5.148}$$

Using eq. (5.147) and eq. (5.148) to calculate the RMS currents, Fig. 5.69 and Fig. 5.70 shows the RMS currents through the top transistor and top diode as a function of the load angle. The values plotted by marks are derived from a numerical simulation of the three-level inverter and is used to validate the derived expressions. Similarly, Fig. 5.71 shows the RMS currents through the center transistor T_3 of the diode clamped topology. Fig. 5.72 shows the RMS current through the clamping diode D_3'

5.4.2 Switching losses

Assuming the switching devices of the NPC inverter to have linear current and voltage turn-on and turn-off characteristics with respect to time and accounting only for the fundamental component of the output current, the switching losses of the NPC inverter can be analytically modeled for any given modulation strategy. The transistor and diode switching losses per fundamental can be evaluated by:

$$P_{t,sw} = \frac{1}{2} V_{DC} \cdot E_{sw0,t}(T) \cdot f_{sw} \cdot I_{t,swavg} \tag{5.149}$$

$$P_{d,sw} = \frac{1}{2} V_{DC} \cdot E_{sw0,t}(T) \cdot f_{sw} \cdot I_{d,swavg} \tag{5.150}$$

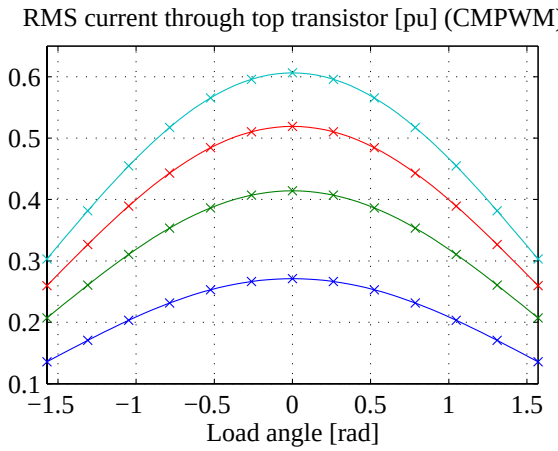


Figure 5.69: *Per unit RMS current through top transistor as a function of the load angle. $M \in [0.15, 0.35 ...0.75]$.*

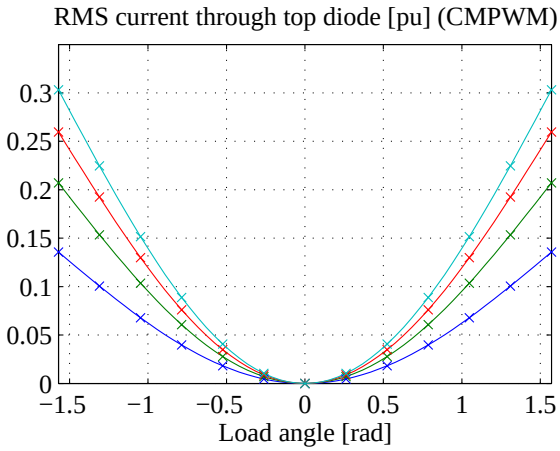


Figure 5.70: *Per unit RMS current through top diode as a function of the load angle. $M \in [0.15, 0.35 ...0.75]$.*

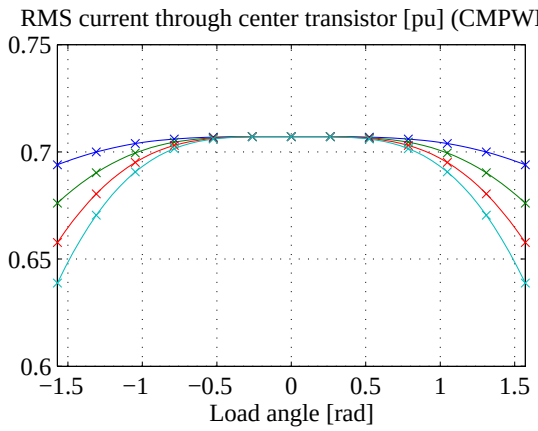


Figure 5.71: *Per unit RMS current through center transistor as a function of the load angle. $M \in [0.15, 0.35 ...0.75]$.*

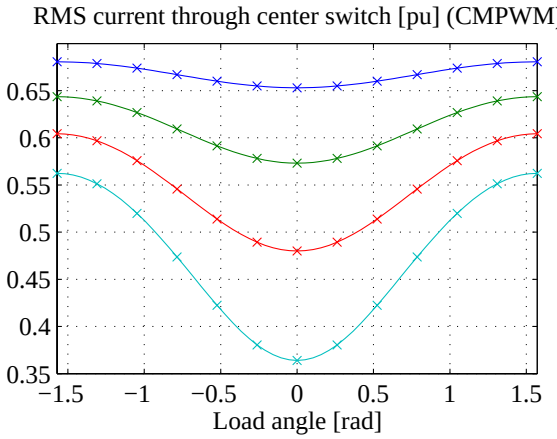


Figure 5.72: *Per unit RMS current through center transistor as a function of the load angle. $M \in [0.15, 0.35 ...0.75]$.*

where $E_{t,sw0}$ is the sum of the per unit VA transistor turn on and turn off switching energy, $E_{d,sw0}$ is sum of the per unit VA diode turn on and turn off switching energy, V_{DC} is the DC-link voltage, f_{sw} is the switching frequency, $I_{t,swavg}$ is the average switched transistor current and $I_{d,swavg}$ is the average switched diode current. The per unit VA switching energies can either be found from data sheets or derived by the procedure described in Appendix A. The average switched device current is given by:

$$I_{sw,avg} = \frac{1}{2\pi}\int_0^{2\pi} \tilde{i}_{sw}(\theta)d\theta \tag{5.151}$$

where $\tilde{i}_{sw}(\theta)$ is the switching current function The switching current function equals zero in the intervals where modulation function for the considered component ceases, c.f. the graphical illustrations of the modulation functions in section 5.3.4, and the absolute

value of the corresponding phase current value elsewhere. To obtain a closed form expression for the switching losses, the switching current function has to be evaluated for the different modulation methods. However, it turns out that a common trade for all the modulation methods is, that the average switched current of the center switches has the following properties:

$$I_{d3,swavg} = 0 \tag{5.152}$$

$$I_{t3,swavg} = I'_{t3,swavg} = I_{d1,swavg} \tag{5.153}$$

$$I'_{d3,swavg} = I_{t1,swavg} \tag{5.154}$$

where the indices refer to Fig. 5.24 on page 182. Hence the only exercise left is to derive the switched current $I_{t1,swavg}$ through the top transistor and $I_{d1,swavg}$ through the top diode. As a final remark, it is important to note that all the derived expressions for the average switched current are valid when active power flows out of the inverter. If active power is entering the inverter, the expressions for transistor and diode switched current have to be exchanged.

Space vector modulation method 1 (SVPWM1)

Evaluating eq. (5.151) for the space vector modulation method 1 (SVPWM1) it turns out that the switching current function for both top transistor and top diode becomes modulation index dependent as well as load angle dependent. If the modulation index M is less than $1/\sqrt{3}$ the average switched current through the top transistor becomes:

$$I_{t1,swavg} = \begin{cases} \frac{\sqrt{2}}{\pi} I_r & |\phi| \leq \frac{\pi}{6} \\ \frac{\sqrt{2}\left(\sin(|\phi|)+2+\sqrt{3}\cos(\phi)\right)}{4\pi} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.155}$$

while the average current switched by the top diode becomes:

$$I_{d1,swavg} = \begin{cases} \frac{\sqrt{2}\left(2-\sqrt{3}\cos(\phi)\right)}{2\pi} I_r & |\phi| \leq \frac{\pi}{6} \\ \frac{\sqrt{2}\left(2+\sin(|\phi|)-\sqrt{3}\cos(\phi)\right)}{4\pi} I_r & \frac{\pi}{6} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.156}$$

If the modulation index M is more than $1/\sqrt{3}$ the average current switched by the top transistor becomes:

$$I_{t1,swavg} = \begin{cases} \frac{\sqrt{2}}{\pi} I_r & |\phi| \leq \theta_1 \\ \frac{\sqrt{2}\left(\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)+1\right)}{2\pi} I_r & \theta_1 < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.157}$$

where the angle θ_1 is give by eq. (5.88) and the angle θ_D is given by eq. (5.97). The average current switched by the top diode when the modulation index is above $1/\sqrt{3}$ can be calculated by:

$$I_{d1,swavg} = \begin{cases} \frac{\sqrt{2}\left(2-\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)-\cos\left(\frac{\pi}{6}-|\phi|-\theta_D\right)\right)}{2\pi} I_r & |\phi| \leq \theta_1 \\ \frac{\sqrt{2}\left(1-\cos\left(\frac{\pi}{6}-|\phi|-\theta_D\right)\right)}{2\pi} I_r & \theta_1 < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.158}$$

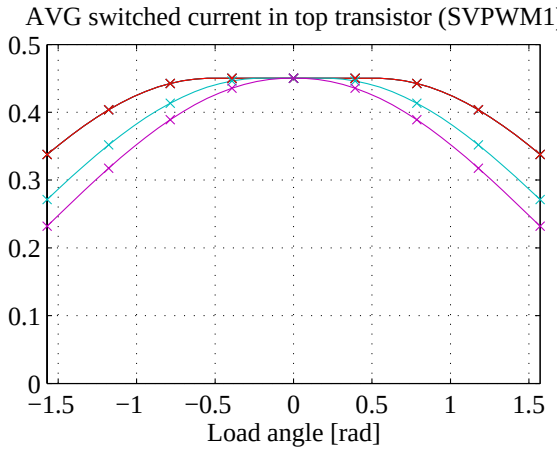


Figure 5.73: *Average switched current in top transistor when using SVPWM1.*

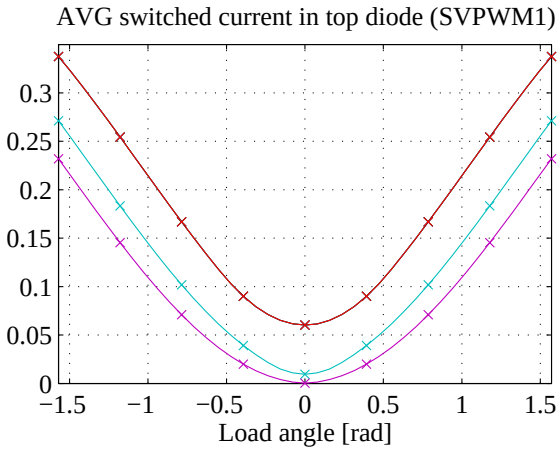


Figure 5.74: *Average switched current in top diode when using SVPWM1.*

Fig. 5.73 shows the average current $I_{t1,swavg}$ switched by the top transistor while Fig. 5.74 shows the current $I_{d1,swavg}$ switched by the top diode. The results represented by marks are obtained from numerical simulation and validates the analytical expressions for the average switched currents.

Space vector modulation method 2 (SVPWM2)

Using the space vector modulation method 2 (SVPWM2), the switchings of each device are clamped during half of the fundamental period. This in turn results in a load angle dependent switching current function while being independent of the modulation index. The switching current function $I_{t1,swavg}$ for the upper (and lower) transistors are given by:

$$I_{t1,swavg} = \frac{\sqrt{2}}{2}\left(\frac{1+\cos(\phi)}{\pi}\right) I_r \tag{5.159}$$

while the switching current function $I_{d1,swavg}$ for the upper (and lower) diodes are given by:

$$I_{d1,swavg} = \frac{\sqrt{2}}{2}\left(\frac{1-\cos(\phi)}{\pi}\right) I_r \tag{5.160}$$

Fig. 5.75 shows the average current $I_{t1,swavg}$ switched by the top transistor while Fig. 5.76 shows the current $I_{d1,swavg}$ switched by the top diode. The results represented by marks are obtained from numerical simulation and validates the analytical expressions for the average switched currents.

Asymmetrical shifted left flat top modulation (DPWM0)

Considering the asymmetrical shifted left flat top modulation (DPWM0) the average switched current depends on both the modulation index and the load angle. If the modulation index is lower than 1/2, the average switched current through the top transistor

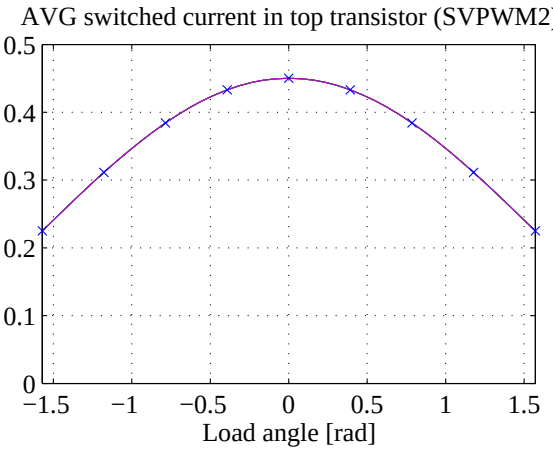


Figure 5.75: *Average switched current in top transistor when using SVPWM2.*

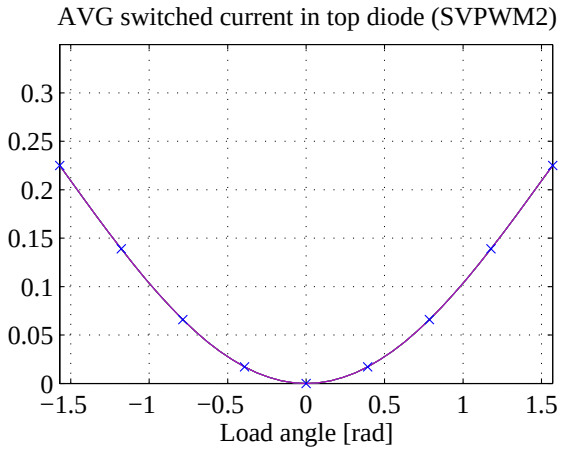


Figure 5.76: *Average switched current in top diode when using SVPWM2.*

can be calculated by:

$$I_{t1,swavg} = \begin{cases} \frac{\sqrt{2}\left(\sqrt{3}\cos(\phi)+\sin(|\phi|)-2\right)}{4\pi} I_r & -\frac{\pi}{2} \leq \phi \leq 0 \\ \frac{\sqrt{2}\left(2-\cos(\phi)\sqrt{3}+\sin(|\phi|)\right)}{4\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{\sqrt{2}\sin(|\phi|)}{2\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.161}$$

while the switched current through the top diode can be calculated by:

$$I_{d1,swavg} = \begin{cases} \frac{\sqrt{2}}{2\pi} I_r & -\frac{\pi}{2} \leq \phi \leq 0 \\ \frac{\sqrt{2}}{2\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{\sqrt{2}\left(\cos(\phi)\sqrt{3}+\sin(|\phi|)\right)}{4\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.162}$$

If the modulation index is in the range between $1/2$ and $1/\sqrt{3}$, the switched current through the top transistor can be derived as:

$$I_{t1,swavg} = \begin{cases} \frac{-\sqrt{3}\cos(\phi)-\sin(|\phi|)+2+2\cos\left(\frac{\pi}{6}+\theta_D+|\phi|\right)+2\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq 0 \\ \frac{2\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)+2\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)+2-\cos(\phi)\sqrt{3}+\sin(|\phi|)}{2\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)+\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)+\sin(|\phi|)}{\sqrt{2}\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.163}$$

and the diode current as:

$$I_{d1,swavg} = \begin{cases} \frac{1-\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)-\cos\left(\frac{\pi}{6}+\theta_D+|\phi|\right)}{\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq 0 \\ \frac{1-\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)-\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)}{\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{-2\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)+\sin(|\phi|)+\cos(\phi)\sqrt{3}-2\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)}{2\sqrt{2}\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.164}$$

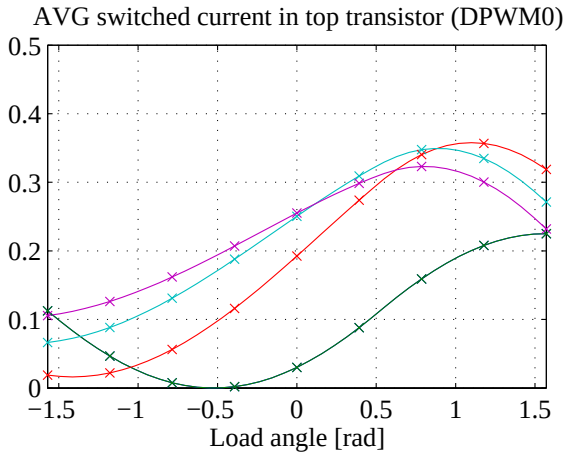


Figure 5.77: *Average switched current in top transistor when using DPWM0.*

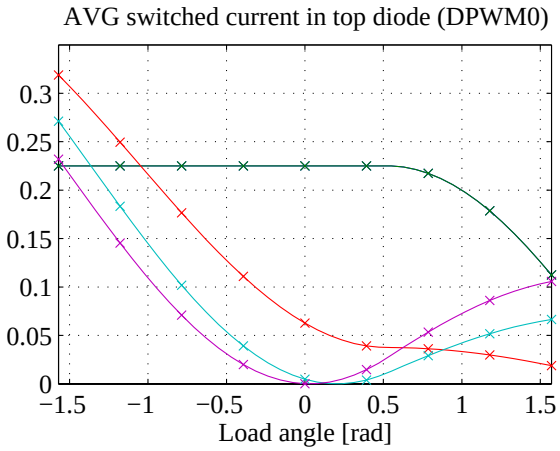


Figure 5.78: *Average switched current in top diode when using DPWM0.*

Finally, if the modulation index is above $1/\sqrt{3}$, the switched transistor current $I_{t1,swavg}$ and switched diode current $I_{d1,swavg}$ can be calculated by:

$$I_{t1,swavg} = \begin{cases} \frac{-\sqrt{3}\cos(\phi)-\sin(|\phi|)+2+2\,\sin\left(\frac{\pi}{3}+\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq 0 \\ \frac{-\cos(\phi)\sqrt{3}+\sin(|\phi|)+2\,\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)+2}{2\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{\sin(|\phi|)+\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)}{\sqrt{2}\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.165}$$

$$I_{d1,swavg} = \begin{cases} -\frac{-1+\sin\left(\frac{\pi}{3}+\theta_D+|\phi|\right)}{\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq 0 \\ -\frac{-1+\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)}{\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{6} \\ \frac{\cos(\phi)\sqrt{3}+\sin(|\phi|)-2\,\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)}{2\sqrt{2}\pi} I_r & \frac{\pi}{6} < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.166}$$

Fig. 5.77 shows the switched current through the top transistor when using the asymmetrical shifted left flat top modulation (DPWM0) where the green curve is valid for a modulation index below 1/2, the red curve represents the current switching function when the modulation index is 0.55 while the cyan and magenta curves represent the switching current function for a modulation index of 0.75 and 0.95 respectively. Similarly, Fig. 5.78 shows the switched current through the top diode when using the asymmetrical shifted left flat top modulation (DPWM0). The marks in the figures represent results obtained from numerical simulations and are used to validate the derived expressions.

Symmetrical flat top modulation (DPWM1)

Using the symmetrical flat top modulation (DPWM1) the average switched currents have to be calculated for three different modulation index ranges. Whenever the modulation index is lower than 1/2, the average switched current through the top transistor

is given by:

$$I_{t1,swavg} = \begin{cases} \frac{1-\cos(\phi)}{\sqrt{2}\pi} I_r & |\phi| \leq \frac{\pi}{3} \\ \frac{\sqrt{3}\sin(|\phi|)-\cos(\phi)}{2\sqrt{2}\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.167}$$

while the average switched top diode current can be calculated by:

$$I_{d1,swavg} = \begin{cases} \frac{\sqrt{2}}{2\pi} I_r & |\phi| \leq \frac{\pi}{3} \\ \frac{\cos(\phi)+\sqrt{3}\sin(|\phi|)}{2\sqrt{2}\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.168}$$

In case the modulation index is between $1/2$ and $1/\sqrt{3}$, the average switched current through the top transistor can be calculated by:

$$I_{t1,swavg} = \begin{cases} -\frac{2\cos(\phi)-\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)-\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)-1}{\sqrt{2}\pi} I_r & |\phi| \leq \frac{\pi}{3} \\ \frac{2\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)-3\cos(\phi)+\sin(|\phi|)\sqrt{3}+2\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.169}$$

and for the top diode, the corresponding average switched current becomes:

$$I_{d1,swavg} = \begin{cases} \frac{1-\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)-\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)+\cos(\phi)}{\sqrt{2}\pi} I_r & |\phi| \leq \frac{\pi}{3} \\ \frac{-2\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)+3\cos(\phi)+\sin(|\phi|)\sqrt{3}-2\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.170}$$

Finally if the modulation index is above $1/\sqrt{3}$, the average switched top transistor current can be calculated by:

$$I_{t1,swavg} = \begin{cases} \frac{-2\cos(\phi)+\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)+\sin\left(\frac{\pi}{3}+\theta_D+|\phi|\right)+1}{\sqrt{2}\pi} I_r & |\phi| \leq \frac{\pi}{3} \\ -\frac{-2\sin\left(\frac{\pi}{3}+\theta_D+|\phi|\right)+3\cos(\phi)-\sqrt{3}\sin(|\phi|)-2\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.171}$$

while the average switched top diode current can be calculated by:

$$I_{d1,swavg} = \begin{cases} \frac{1-\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)-\sin\left(\frac{\pi}{3}+\theta_D+|\phi|\right)+\cos(\phi)}{\sqrt{2}\pi} I_r & |\phi| \leq \frac{\pi}{3} \\ \frac{-2\sin\left(\frac{\pi}{3}+\theta_D+|\phi|\right)+3\cos(\phi)+\sqrt{3}\sin(|\phi|)-2\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & \frac{\pi}{3} < |\phi| \leq \frac{\pi}{2} \end{cases} \tag{5.172}$$

Fig. 5.79 shows the average current $I_{t1,swavg}$ switched by the top transistor when using the symmetrical flat top modulation method while Fig. 5.80 shows the current $I_{d1,swavg}$ switched by the top diode. The results represented by marks are obtained from numerical simulation and validates the analytical expressions for the average switched currents.

Asymmetrical shifted right flat top modulation (DPWM2)

As was the case for the asymmetrical shifted left flat top modulation, the average switched current functions for the asymmetrical shifted right flat top modulation are not symmetrically distributed across the considered load angle range. Actually the expressions for these asymmetrical modulation methods are very much equal although

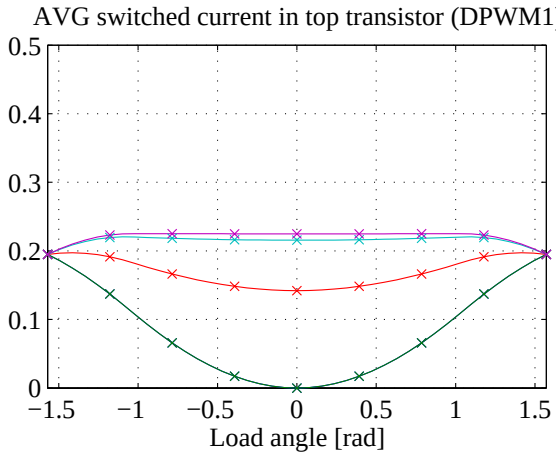


Figure 5.79: *Average switched current in top transistor when using DPWM1.*

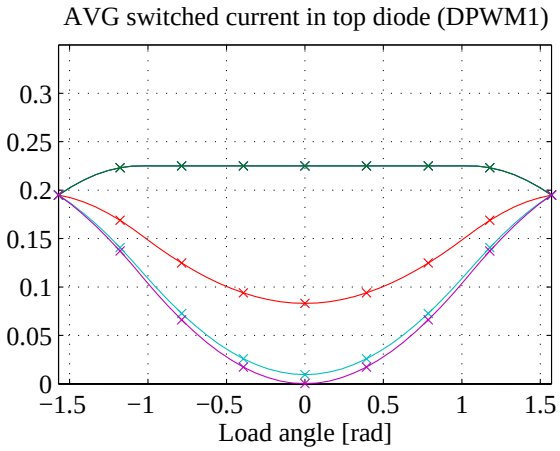


Figure 5.80: *Average switched current in top diode when using DPWM1.*

mirrored through a load angle of zero. As for the previously discussed modulation methods, the average switched currents are modulation index independent as long as the modulation index is below 1/2. In such case, the average switched top transistor current becomes:

$$I_{t1,swavg} = \begin{cases} \frac{\sqrt{2}\sin(|\phi|)}{2\pi} I_r & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \\ -\frac{\sqrt{2}\left(-2+\cos(\phi)\sqrt{3}-\sin(|\phi|)\right)}{4\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ -\frac{\sqrt{2}\left(\sqrt{3}\cos(\phi)+\sin(|\phi|)-2\right)}{4\pi} I_r & 0 < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.173}$$

and the average switched top diode current becomes:

$$I_{d1,swavg} = \begin{cases} \frac{\sqrt{2}\left(\cos(\phi)\sqrt{3}+\sin(|\phi|)\right)}{4\pi} I_r & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \\ \frac{\sqrt{2}}{2\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ \frac{\sqrt{2}}{2\pi} I_r & 0 < \phi \leq \frac{\pi}{2} \end{cases} \tag{5.174}$$

When the modulation index exceeds 1/2, the average switched currents becomes modulation index dependent as the intersections from one sub-sector to another depends on the modulation index. When the modulation index is between 1/2 and $1/\sqrt{3}$ the space vector are located in both sub-sector a and sub-sector c and since the switching sequences within these sub-sectors are not equal the average switched current becomes dependent of the modulation index. This modulation index dependency actually reflects the intersection between sub-sector a and sub-sector c and is represented by the angle θ_D, c.f. eq. (5.97). The average switched current through the top transistor can be

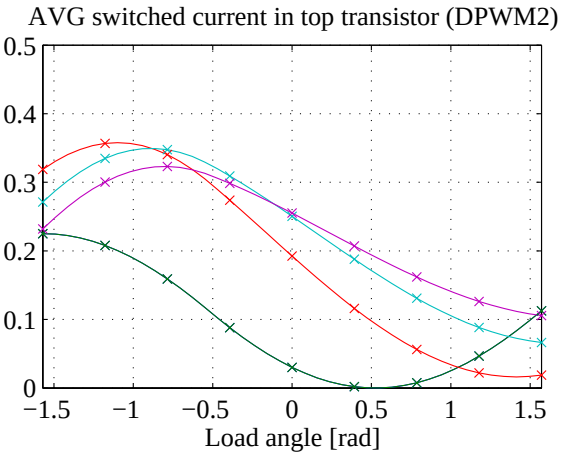


Figure 5.81: *Average switched current in top transistor when using DPWM1.*

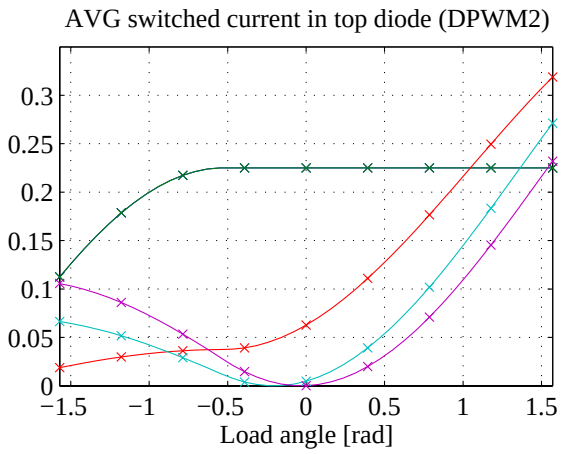


Figure 5.82: *Average switched current in top diode when using DPWM2.*

derived as:

$$I_{t1,swavg} = \begin{cases} \frac{\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)+\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)+\sin(|\phi|)}{\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \\ -\frac{-2\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)-2\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)-2+\cos(\phi)\sqrt{3}-\sin(|\phi|)}{2\sqrt{2}\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ \frac{-\sqrt{3}\cos(\phi)-\sin(|\phi|)+2+2\cos\left(\frac{\pi}{6}+\theta_D+|\phi|\right)+2\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{2} \end{cases} \quad (5.175)$$

while the average switched top diode current can be calculated by:

$$I_{d1,swavg} = \begin{cases} \frac{-2\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)+\sin(|\phi|)+\cos(\phi)\sqrt{3}-2\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)}{2\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \\ -\frac{-1+\sin\left(\frac{\pi}{3}-\theta_D+|\phi|\right)+\cos\left(\frac{\pi}{6}-\theta_D-|\phi|\right)}{\sqrt{2}\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ -\frac{\cos\left(\frac{\pi}{6}-\theta_D+|\phi|\right)+\cos\left(\frac{\pi}{6}+\theta_D+|\phi|\right)-1}{\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{2} \end{cases} \quad (5.176)$$

In case the modulation index is above $1/\sqrt{3}$ the average switched current through the top transistor can be calculated by:

$$I_{t1,swavg} = \begin{cases} \frac{\sin(\phi)+\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)}{\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \\ \frac{-\cos(\phi)\sqrt{3}+\sin(|\phi|)+2\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)+2}{2\sqrt{2}\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ \frac{-\sqrt{3}\cos(\phi)-\sin(|\phi|)+2+2\sin\left(\frac{\pi}{6}+\theta_D+|\phi|\right)}{2\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{2} \end{cases} \quad (5.177)$$

while the average switched diode current through the top diode can be calculated by:

$$I_{d1,swavg} = \begin{cases} \frac{\cos(\phi)\sqrt{3}+\sin(|\phi|)-2\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)}{2\sqrt{2}\pi} I_r & -\frac{\pi}{2} \leq \phi \leq -\frac{\pi}{6} \\ -\frac{-1+\sin\left(\theta_D+\frac{\pi}{3}-|\phi|\right)}{\sqrt{2}\pi} I_r & -\frac{\pi}{6} < \phi \leq 0 \\ -\frac{-1+\sin\left(\frac{\pi}{3}+\theta_D+|\phi|\right)}{\sqrt{2}\pi} I_r & 0 < \phi \leq \frac{\pi}{2} \end{cases} \quad (5.178)$$

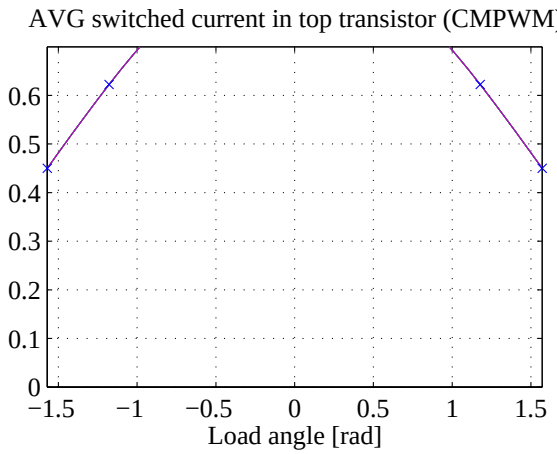


Figure 5.83: *Average switched current in top transistor when using CMPWM.*

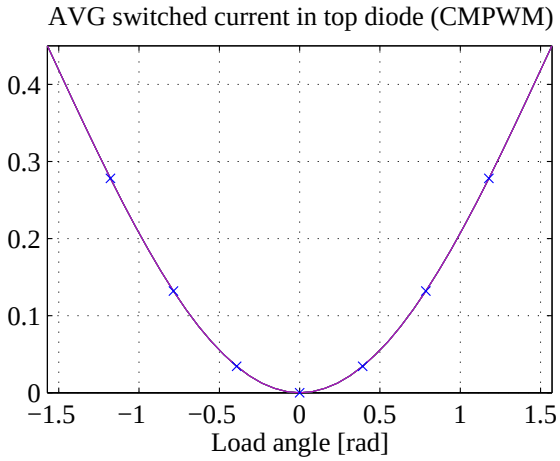


Figure 5.84: *Average switched current in top diode when using CMPWM.*

Fig. 5.81 shows the switched current through the top transistor when using the asymmetrical shifted right flat top modulation (DPWM2) where the green curve is valid for a modulation index below 1/2, the red curve represents the current switching function when the modulation index is 0.55 while the cyan and magenta curves represent the switching current function for a modulation index of 0.75 and 0.95 respectively. Similarly, Fig. 5.82 shows the switched current through the top diode when using the asymmetrical shifted right flat top modulation (DPWM2). The marks in the figures represent results obtained from numerical simulations and are used to validate the derived expressions.

Common mode voltage elimination modulation (CMPWM)

Unlike the switched current functions for the other considered modulation methods, the average switched current when using the common mode voltage elimination modulation (CMPWM) becomes only load angle dependent while being independent of the modulation index. Evaluating eq. (5.151) with respect to the switching sequences given by Table VI gives the following average switched current for the top transistors.

$$I_{t1,swavg} = \frac{\sqrt{2}\left(1+\cos\left(\phi\right)\right)}{\pi} \tag{5.179}$$

Similarly, the average switched current for the top diode becomes:

$$I_{d1,swavg} = \frac{\sqrt{2}\left(1-\cos\left(\phi\right)\right)}{\pi} \tag{5.180}$$

Fig. 5.83 shows the average current switched by the top transistor when the load angle is between $\pm\frac{\pi}{2}$ while Fig. 5.84 shows the averaged switched current through the top diode.

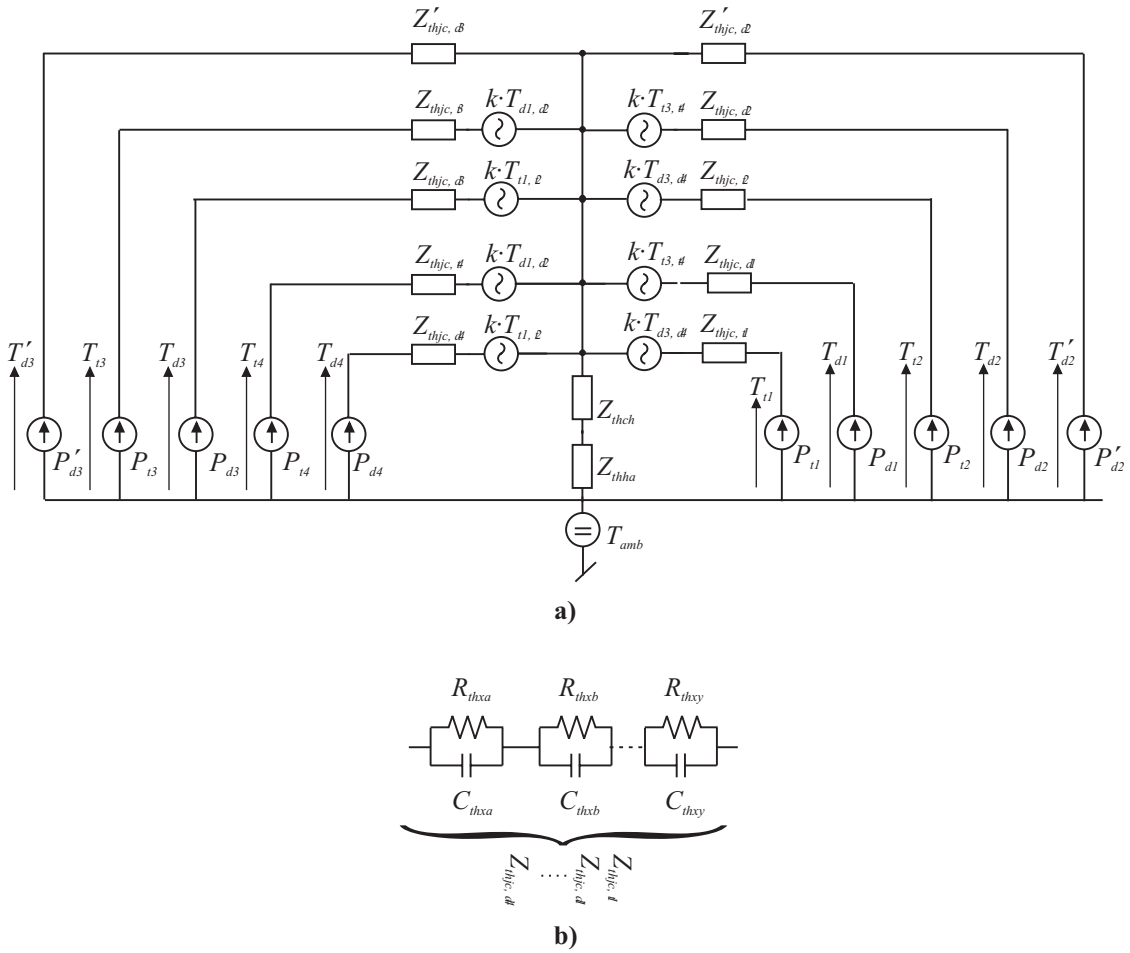


Figure 5.85: *Illustration of the simple thermal model used to estimate switch temperatures in the three-level inverter.* **a)** *Thermal model of a half bridge module.* **b)** *Model of a thermal impedance* Z_{th}.

5.4.3 Thermal modeling

The thermal modeling of the switches for use in the three-level inverter is in many aspects very similar to the modeling approach described for the two-level inverter. However as the thermal model for the three-level inverter are based on some crucial assumptions - assumptions not as present for the two-level inverter - the thermal modeling approach for the switches in the three-level inverter will be discussed in the same details as was the case in chapter 3.

The thermal modeling of the switches has two purposes:

1. To calculate the per fundamental average temperature in order to derive the correct values for resistances and on-state voltage drops under the actual temperature conditions[2].

[2]Assuming the resistances and on-state voltage drops to be linear dependent on the component temperature, this approach will generate the correct per fundamental power losses.

2. To calculate the peak temperature within a fundamental period in order to validate a certain converter design[3].

Fig. 5.85a illustrates a simple one dimensional approach to calculate the junction temperature of the semiconductor components in a three-level inverter leg module, where the index notation of the power losses, e.g. P_{t1}, follows the notation in Fig. 5.24 on page 182. The simple approach described by Fig. 5.85a relies on the assumption that an inverter phase leg is realized in a single module[4] mounted on a heatsink with sufficiently high thermal capacitance to suppress temperature variations due power loss variations within a fundamental cycle and with sufficient heat conducting properties to suppress local hotspots on the heatsink due to the loss cycle within the individual components.

Considering Fig. 5.85 each of the semiconductor power losses are modeled as a current source feeding into a thermal impedance denoted by Z_{thxx}. As illustrated in Fig. 5.85b, the thermal impedances can be composed of one or more series connected RC-elements. The temperature source $k \cdot T_{xx}$ illustrates a thermal coupling between components having current conduction in the same half period of a fundamental and finally the temperature source T_{amb} makes it possible to offset the temperature estimation by the ambient temperature. Based on the thermal modeling approach in Fig. 5.85 the goal is to derive a method which enables estimation of the average and peak junction temperatures, only with information on the modulation dependent average semiconductor losses calculated by the expressions derived in section 5.4 and the thermal parameters in Fig. 5.85.

Average temperatures

Neglecting the thermal coupling between the components in the half bridge module, the average temperature of the individual components can simply be calculated by:

$$T_{tx} = P_{tx} \cdot \sum_{w=1}^{y} R_{thxw,t} + 2 \cdot (P_{t1} + P_{d1} + P_{t3} + P_{d3} + P'_{d3}) \cdot (R_{thch} + R_{thha}) + T_{amb} \tag{5.181}$$

$$T_{dx} = P_{dx} \cdot \sum_{w=1}^{y} R_{thxw,d} + 2 \cdot (P_{t1} + P_{d1} + P_{t3} + P_{d3} + P'_{d3}) \cdot (R_{thch} + R_{thha}) + T_{amb} \tag{5.182}$$

where T_{tx} is the average temperature of the considered transistor, T_{dx} is the average temperature of the considered diode and $R_{thxx,x}$ is the thermal resistances in the thermal model as given in Fig. 5.85.

[3] Especially in the doubly-fed system, this seems to be a very important issue due to the low fundamental frequency of the rotor inverter. Due to the low frequency, very high temperature variations within a fundamental period can be expected.

[4] This assumption is fictitious as no such module is available on the marked. However, since the conventional half bridge module is very much optimized for use in the two-level inverter a similar module should be developed for the inverter leg of the three-level inverter in order to obtain a fair comparison.

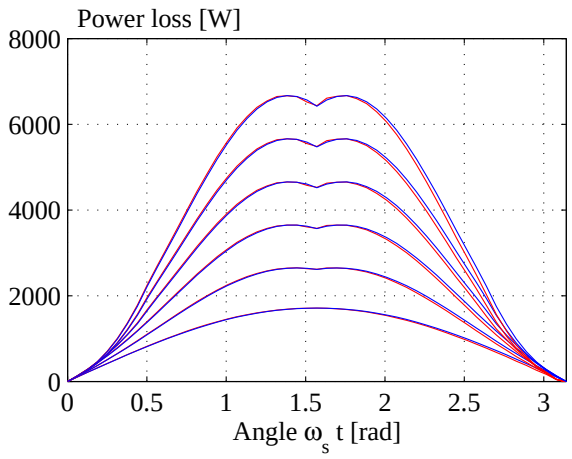


Figure 5.86: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using the SVPWM1 modulation.*

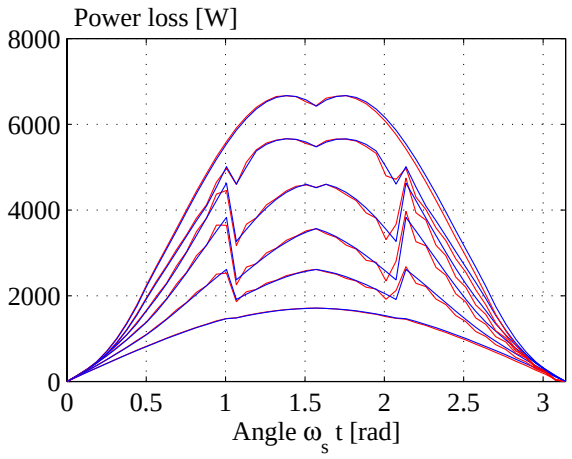


Figure 5.87: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using the SVPWM2 modulation.*

Peak temperatures

During operation at low frequencies ($f_s < 10 - 20$ Hz) the temporal variability of the power losses within a fundamental causes similar junction temperature variations. As the peak temperature during operation at very low frequencies may vary quite much from the average temperature and since such temperature variations will have a very high influence on the lifetime of the semiconductors[5] it is important to be able to estimate the peak temperatures. As discussed in chapter 3 several approaches exist to estimate the temperature within a semiconductor but in order to suit the goal for the present calculation tool, the approach has to be very simple and only acquire knowledge of the most fundamental component properties.

The approach considered in this context is based on the one-dimensional thermal model illustrated in Fig. 5.85, and the approach is to model the losses as sinusoidal functions with a DC-offset representing the average losses. By this approach, the thermal problem is reduced from a complex numerical iteration task to simple scalar expressions. By the present approach, the transistor losses $\tilde{p}_{tx}$ and diode losses $\tilde{p}_{dx}$ are estimated by:

$$\tilde{p}_{tx}(t) = P_{tx} + \sum_{n=1}^{\infty} \left(p_{t,an} \cdot \cos\left(n \cdot \omega_s \cdot t\right) + p_{t,bn} \cdot \sin\left(n \cdot \omega_s \cdot t\right) \right) \tag{5.183}$$

$$\tilde{p}_{dx}(t) = P_{dx} + \sum_{n=1}^{\infty} \left(p_{d,an} \cdot \cos\left(n \cdot \omega_s \cdot t\right) + p_{d,bn} \cdot \sin\left(n \cdot \omega_s \cdot t\right) \right) \tag{5.184}$$

[5]Thermal cycling and power cycling represents structural stresses on the different materials used to built the module. These effects are crucial mechanisms when considering the life time of a module.

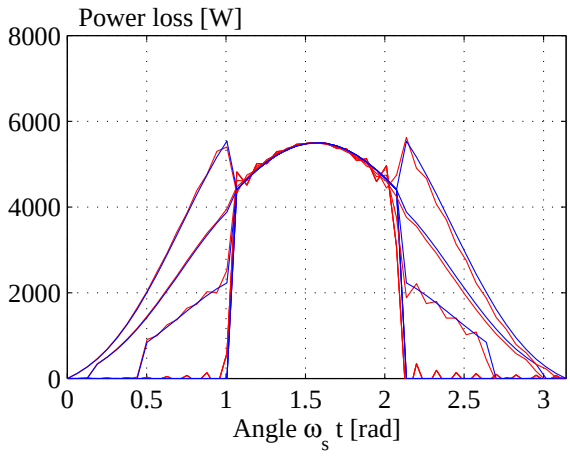


Figure 5.88: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using the DPWM1 modulation.*

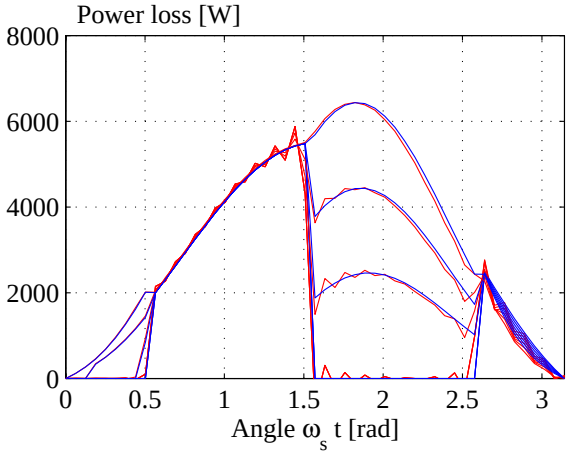


Figure 5.89: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using the DPWM0 modulation.*

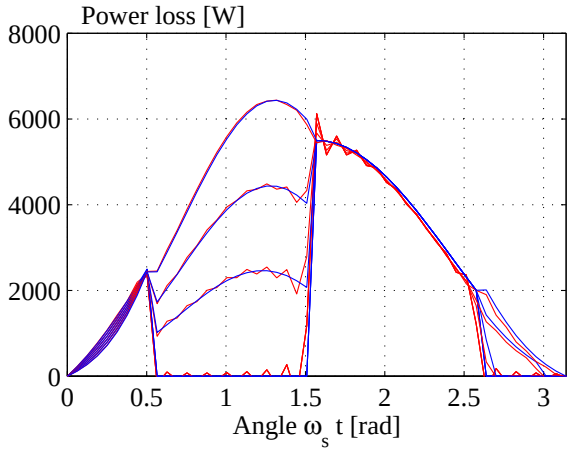


Figure 5.90: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using the DPWM2 modulation.*

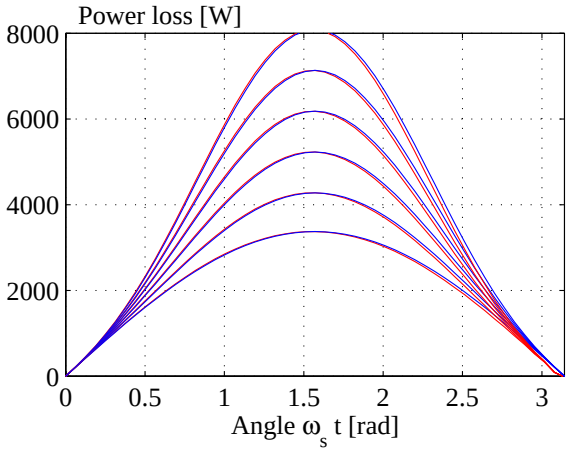


Figure 5.91: *Example of estimated (-) and simulated (-) IGBT losses as a function of the modulation angle, using the CMPWM modulation.*

where the coefficients $p_{t,an}$, $p_{t,bn}$, $p_{d,an}$ and $p_{d,bn}$ are found from a Fourier analysis of the actual transistor losses and diode losses. The actual transistor- and diode losses where derived in section 5.4 and are given by:

$$p_{tx}(\theta) = \left(V_{DC} \cdot E_{sw0,t}(T) \cdot f_{sw} \cdot \tilde{i}_{sw,t}(\theta) + S_{xA}\left(V_{t0}(T) \cdot i_t(\theta) + R_t \cdot i_t^2(\theta)\right)\right) \quad (5.185)$$

$$p_{dx}(\theta) = \left(V_{DC} \cdot E_{sw0,d}(T) \cdot f_{sw} \cdot \tilde{i}_{sw,d}(\theta) + S_{xA}\left(V_{d0}(T) \cdot i_d(\theta) + R_d \cdot i_d^2(\theta)\right)\right) \quad (5.186)$$

Fig. 5.86 - Fig. 5.91 illustrates the present approach calculated for the top transistor T_1 when applied on the six considered modulation strategies. The blue curves show the real losses derived from a numerical simulation whereas the red curves show

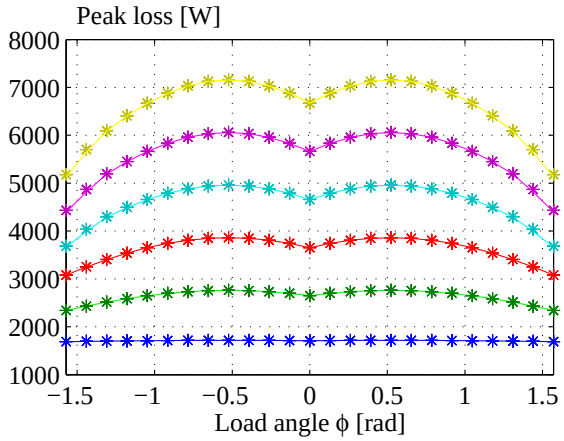


Figure 5.92: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using the SVPWM1 modulation.*

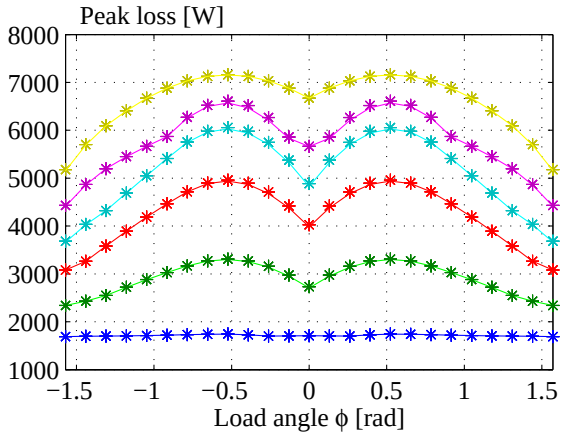


Figure 5.93: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using the SVPWM2 modulation.*

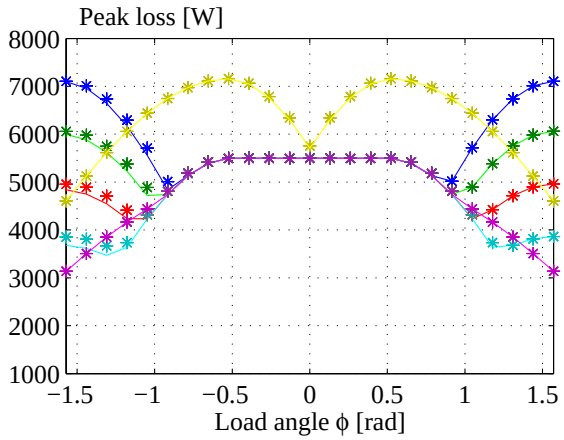


Figure 5.94: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using the DPWM1 modulation.*

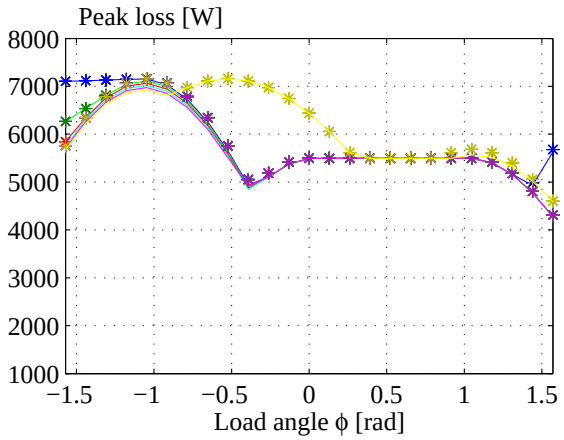


Figure 5.95: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using the DPWM0 modulation.*

the losses calculated from eq. (5.183) - eq. (5.186) when the number of harmonics n is limited to 25. The different curves correspond to different modulation indexes. To further demonstrate the strength of the present approach, Fig. 5.92 - Fig. 5.97 shows the peak power losses in a transistor. The peak power losses are calculated as a function of the load angle ϕ and shown for different values of the modulation index. The power losses marked with (*) are simulated losses using a numerical simulation model while peak powers calculated by the present approach are shown by solid lines.

Assuming that the thermal capacitance of the case to ambient structure of the semiconductor module is sufficiently large to suppress temperature variations in the considered

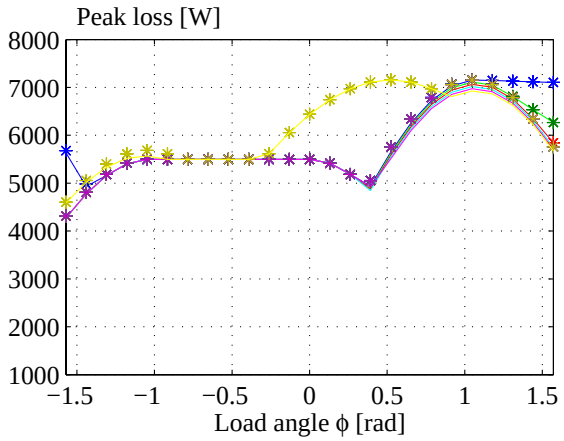


Figure 5.96: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using the DPWM2 modulation.*

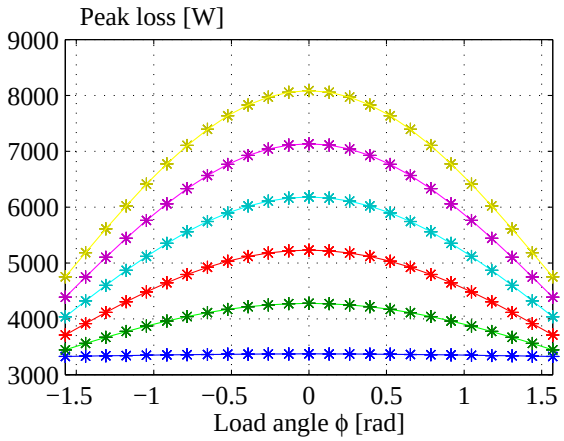


Figure 5.97: *Example of calculated (-) and simulated (*) peak power losses as a function of the load angle, using the CMPWM modulation.*

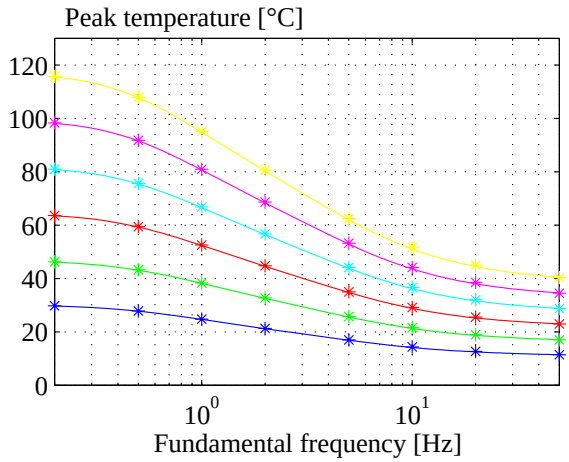


Figure 5.98: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using the SVPWM1 modulation.*

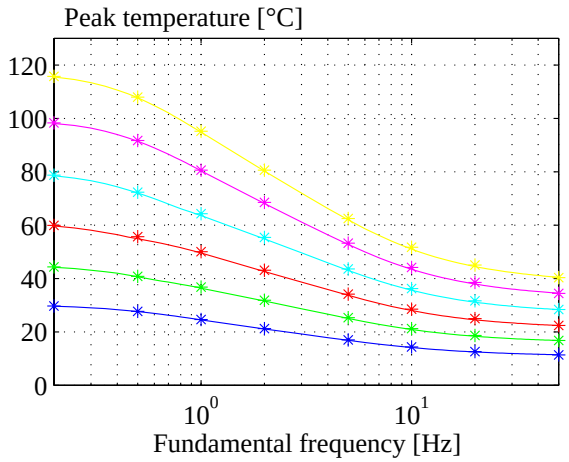


Figure 5.99: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using the SVPWM2 modulation.*

frequency range, the peak junction temperature of the transistor and diode can be estimated by:

$$\tilde{T}_{tx} = T_{tx} + \sum_{n=1}^{\infty} \left(\left(p_{t,an} \cdot \cos\left(n \cdot \omega_s \cdot t\right) + p_{t,bn} \cdot \sin\left(n \cdot \omega_s \cdot t\right) \right) \sum_{w=1}^{y} Z_{thxw}(n \cdot \omega_s) \right) \quad (5.187)$$

$$\tilde{T}_{dx} = T_{dx} + \sum_{n=1}^{\infty} \left(\left(p_{d,an} \cdot \cos\left(n \cdot \omega_s \cdot t\right) + p_{d,bn} \cdot \sin\left(n \cdot \omega_s \cdot t\right) \right) \sum_{w=1}^{y} Z_{thxw}(n \cdot \omega_s) \right) \quad (5.188)$$

where T_{tx} and T_{dx} are the average component temperature calculated by the expressions

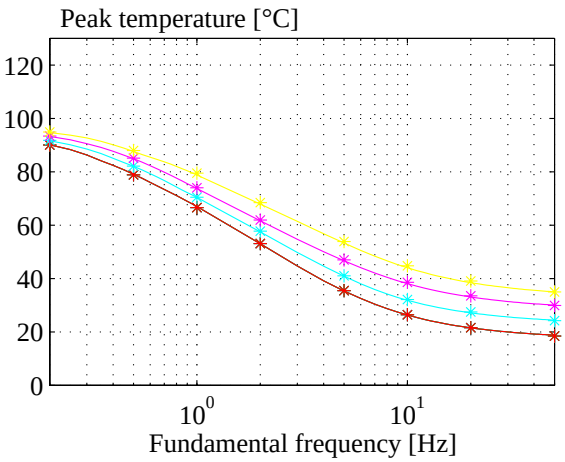


Figure 5.100: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using the DPWM1 modulation.*

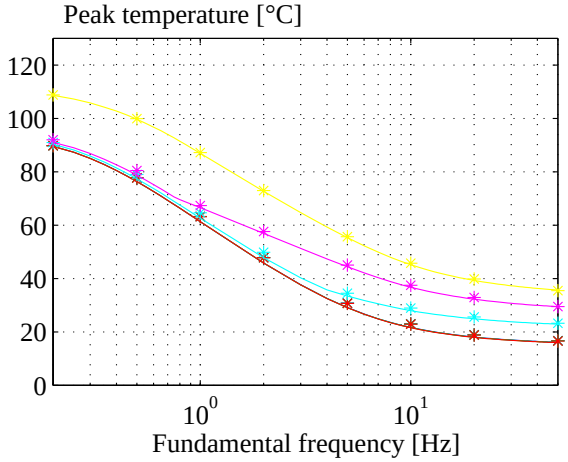


Figure 5.101: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using the DPWM0 modulation.*

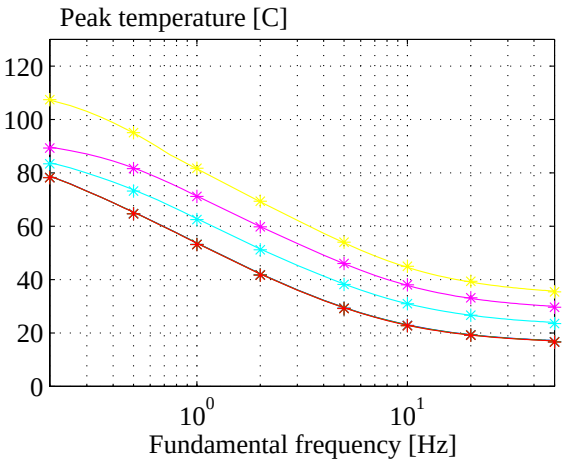


Figure 5.102: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using the DPWM2 modulation.*

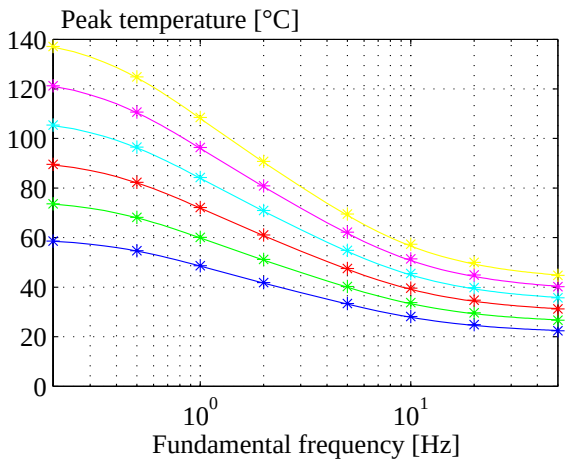


Figure 5.103: *Example of calculated (-) and simulated (*) IGBT junction temperatures as a function of the fundamental frequency, using CMPWM modulation.*

given in eq. (5.181) and eq. (5.182). Fig. 5.98 - Fig. 5.103 demonstrate the present approach for calculating peak junction temperature. The junction temperatures are calculated as a function of the fundamental frequency and shown for different values of the modulation index. The temperatures marked with (*) are simulated temperatures using the real loss distribution on a thermal model as shown in Fig. 5.85 while temperatures calculated by the approach given in eq. (5.187) and eq. (5.188) are shown by unbroken lines.

The thermal parameters used to exemplify the peak temperature estimation approach

TABLE VIII: *Thermal parameters used in the example of Fig. 5.98 - Fig. 5.103.*

Symbol	Value	Unit	Symbol	Value	Unit
$R_{thjc1,t}$	3.4	[K/kW]	$C_{thjc1,t}$	107	[K/mWs]
$R_{thjc2,t}$	9.6	[K/kW]	$C_{thjc2,t}$	18.8	[K/Ws]
$R_{thjc3,t}$	7.0	[K/kW]	$C_{thjc3,t}$	5.7	[K/Ws]
R_{thca}	11	[K/kW]	C_{thca}	$--$	[K/Ws]

are listed in Table VIII.

5.4.4 Inductor power losses

In principle, the modeling of the inductor power losses for the three-level inverter is equivalent to the modeling approach described in chapter 3 concerning the inductor power losses for the two-level inverter although the design and hereby the loss coefficients will differ. However, for completeness of the treatment of the back-to-back three-level converter the loss-modeling is repeated. The inductor power losses P_L are composed of three loss components - copper losses, hysteresis losses and eddy current losses:

$$P_L = P_{cu} + P_{hy} + P_{ed} \tag{5.189}$$

where each of the loss components P_{cu}, P_{hy} and P_{ed} may be estimated as described below.

Copper losses

The copper losses in the inductor are due to the effective resistance R_L of the windings and given by.

$$P_{cu} = 3R_L I_L^2 \tag{5.190}$$

where the effective resistance is a function of the inductor design, the inductor temperature and the frequency components of the inductor current. For a given load current and a desired inductor value, Appendix B provides a detailed inductor design tool from which the effective resistance R_L of the inductor can be extracted.

Hysteresis losses

The empirical Steinmetz equation expresses the specific hysteresis loss as an exponential function of the frequency f and the maximum flux density $\hat{B}_c$. Provided that the magnetizing current is purely sinusoidal, the hysteresis loss can be expressed by:

$$P_{hy} = M_L \cdot c_m \cdot f^{\alpha} \cdot \hat{B}_c^{\beta} \tag{5.191}$$

where M_L is the weight of the core material c_m, α and β are material property constants. Despite, the formula in (5.191) is a well established expression for the hysteresis losses,

manufactures of iron cores rather provide graphical presentation of the loss characteristic than providing the material property constants. Appendix B provides a detailed description on the extraction of the material property constants c_m, α and β as well as a design procedure for determining core material mass, given the nominal current and the desired inductance value. The design values for the current and inductance are discussed in section 5.5.2.

Eddy current losses

To account for the eddy current losses the empirical Steinmetz equation is used:

$$P_{ed} = M_L \cdot \frac{\sigma_c \cdot \tau}{12\rho_c} \left(\frac{dB}{dt} \right)^2 \tag{5.192}$$

where σ_c is the conductivity of the core material, τ is the thickness of the lamination and ρ_c is the mass density of the iron. For a more detailed description on the modeling of the inductor power losses, see Appendix B.

5.5 Design aspects

Although the modeling approach concerning component losses, described in the preceding sections, in some sense has provided most of the equations for use in the converter design it may be difficult to extract the essential parts and for that reason it may be convenient to have some less complex design guidelines, at least for an initial design approach. This section is aimed to provide such design guidelines for the components in the back-to-back three-level voltage source converter. Having this rough converter design, the loss- and temperature modeling approach described in the previous sections of this chapter can then be used to evaluate whether the rough converter design complies with the specified performance specification.

5.5.1 Design of switches

The aspects regarding the switch design describes some rough current rating estimations based on the ideal generator model discussed on page 37 and the current loading of the individual switches as calculated in section 5.4.1. Further, some rules of thumb regarding choice of switch for a given DC-link voltage is provided. Regarding the latter aspect it is important to note that the voltage design margin very much depend on the specific power layout - especially the presence of stray inductances. As no switches are optimized for use in the three-level inverter[6] this aspect is very crucial for the three-level inverter design and may de-rate the switch voltage rating.

[6]Regarding stray inductances, the half bridge modules very much favours the two-level inverter as the voltage across the module can be clamped at the terminals of the module and hence the only stray inductances to be concerned with are the well defined stray inductances within the module.

Current ratings

As a fast but quite accurate estimation of the rotor current, the following expression can be used:

$$|\underline{\tilde{I}}_r| = \frac{\sqrt{\tilde{P}_r^2 + \tilde{Q}_r^2}}{3 \cdot N_{gen} \cdot |s| \cdot |\underline{V}_s|} \tag{5.193}$$

where N_{gen} is the winding ratio between rotor and stator, P_r is the active rotor power, Q_r is the reactive rotor power, s is the slip[7] and $|\underline{V}_s|$ is the RMS stator phase voltage. Neglecting the generator losses, the active power P_r to be handled by the back-to-back three-level rotor inverter is given by:

$$\tilde{P}_r = \frac{s(\omega_{gen} T_{gen})}{1+s} \tag{5.194}$$

where ω_{gen} is the angular velocity of the generator shaft and T_{gen} is the torque applied on the generator shaft. Further, the reactive power $\tilde{Q}_r$ to be handled by the rotor inverter can be estimated by:

$$\tilde{Q}_r = |s| \cdot \left(Q_s^* + \frac{3|\underline{V}_s|^2}{\omega_s L_m} \right) \tag{5.195}$$

where Q_s^* is the desired reactive power to be generated from the stator, and L_m is the magnetizing inductance of the generator. Neglecting the converter losses, the power to be handled by the grid side inverter equals the rotor power $\tilde{P}_r$. Hence the grid inverter current $\tilde{I}_{g3}$ can the be estimated by:

$$|\underline{\tilde{I}}_{g3}| = \frac{\sqrt{\tilde{P}_r^2 + (Q_{g3}^*)^2}}{3 \cdot |\underline{V}_{g3}|} \tag{5.196}$$

where Q_{g3}^* is the reactive power generated to the grid by the grid side inverter. As was shown in Fig. 3.38 in chapter 3, these simple relations calculates the output current to be handled with an inaccuracy of less than 5%. From the calculations of the current through the individual switches in the 3-level inverter, c.f. section 5.4.1, it appeared that for specific operation conditions, i.e. a specific power factor, a specific modulation index and a specific modulation method, the individual switches in the three-level inverter may be designed for different current ratings[8]. This is in particular interesting for the grid side inverter which is operating at a high and nearly constant modulation index. For the rotor side inverter, the situation is quite different as the entire modulation range is to be used and the power factor is varying with the load conditions of the generator. Hence, for the rotor side inverter it appears that all switches are loaded almost equally

[7] Please note that the definition of slip is positive for super synchronous speed - a definition contrary to the definition normally used in text books concerning electrical machinery. The slip was defined in eq. (2.16) on page 33.

[8] Alternatively, the loss balancing control method suggested in [2] although the control method is applied at the expense of additional switches in the clamp circuit.

and hence all the switches should have the same current ratings. Further, compared to the two-level inverter, the currents through the switches in the three-level inverter is somewhat comparable. However, since the switching losses of the individual switches in the three-level inverter may be assumed to be less than for the two-level counterpart, the switches for use in the three-level inverter may have 10-25% lower current ratings than those selected for the two-level inverter. Finally, as was the case for the two-level inverter, the current ratings of the switches in the back-to-back three-level converter should be able to handle a bi-directional power flow and hence the diodes and transistors have to be rated for almost the same current[9].

Voltage ratings

In order to be able to control the generated power in a certain slip range, the rotor side inverter has to be able to generate voltages higher than the voltage appearing on the rotor terminal of the generator. Assuming an ideal generator, the voltage at the rotor terminals of the generator can be approximated by:

$$|\tilde{\underline{V}}_r(s)| = s \cdot |\underline{V}_s| \cdot N_{gen} \tag{5.197}$$

Further to control the power flow to/from the grid, the grid side inverter has to be capable of generating voltages higher than the grid voltage. The necessary grid inverter phase voltage V_{gc} can be approximated by:

$$|\tilde{\underline{V}}_{gc}| = |\underline{V}_{g3} + j \cdot \omega_s \cdot L_g \cdot \tilde{\underline{I}}_{g3}(\hat{s})| \tag{5.198}$$

where $|\underline{V}_{g3}|$ is the transformer phase voltage at the grid side of the inverter and $\tilde{\underline{I}}_{g3}(\hat{s})$ is the grid current appearing at the maximum slip. Hence the DC-link voltage of the back-to-back two-level voltage source converter has to obey the following constrains:

$$V_{DC} > |\hat{s}| \cdot \sqrt{6}|\underline{V}_s| \cdot N_{gen} \tag{5.199}$$

$$\wedge$$

$$V_{DC} > \sqrt{6}|\underline{V}_{g3} + j \cdot \omega_s \cdot L_g \cdot \tilde{\underline{I}}_{g3}(\hat{s})| \tag{5.200}$$

The grid side voltage $|\underline{V}_{g3}|$ should be the maximum appearing value for which the turbine is expected to be in normal operation, c.f. section 2.6.2.

The selection of a switch for a certain DC-link voltage has to incorporate some voltage margin to cope with the transient voltage spikes occurring at each switching instant due to stray inductances, both inside the switch and in the surrounding DC-link circuit. This voltage design margin especially has to include the overvoltages arising from the turn-off transients in case of short circuit failures. In Fig. 3.39 on page 76 typical relations between maximum output inverter voltage and voltage ratings of an applicable switch for the two-level inverter topology was shown. As a rough estimate, the switch

[9] In conventional drives and in wind turbines based on full-scale converters the power flow is normally uni-directional and hence the current shear between transistor and diodes is unequal.

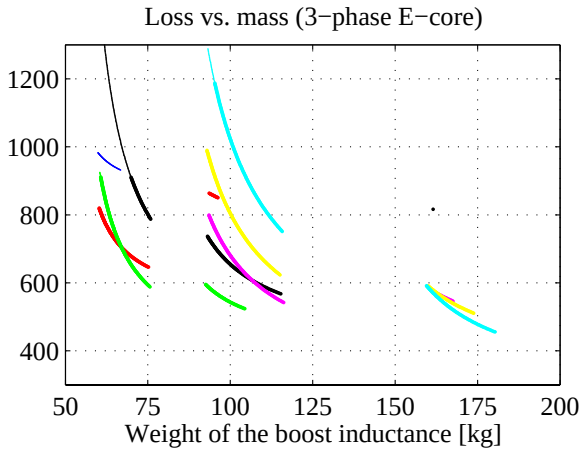


Figure 5.104: *Core designs. Losses vs. mass of the three-phase inductor plotted for current densities between 1.5 - 8 A/mm^2.*

voltage ratings for the diode clamped inverter should be half the ratings in Fig. 3.39. Considering the transistor clamped inverter, the voltage ratings for the two switches connected to the upper and lower DC-link should be the same as for the two-level counterpart.

5.5.2 Design of boost inductance

In order to be able to design the boost inductance, the necessary inductance value and inductance current rating have to be found. Once having the desired inductance and the current rating, the boost inductance can be designed in accordance with the procedure described in Appendix B. Further, from the design procedure the loss parameters necessary for the loss calculations can be derived.

Inductance value

In dynamic operation, i.e. when the rotational speed varies up to the maximum specified slip $\hat{s}$, the grid inverter still has to be able to control the power to/from the DC-link. From eq. (5.200) it appears that the maximum inductance value depends on the DC-link voltage and the grid voltage. Rearranging eq. (5.200) the following constrain regarding the boost inductance is obtained:

$$L_g \leq \frac{-\hat{Q}^*_{g3} + \sqrt{9|\hat{\underline{V}}_{gc}|^2|\hat{\underline{I}}_{g3}|^2 - \hat{P}_r^2 - 2\hat{P}_r\hat{Q}^*_{g3}}}{\omega_g|\hat{\underline{I}}_{g3}|^2} \tag{5.201}$$

where $|\hat{\underline{V}}_{gc}|$ and $|\hat{\underline{I}}_{g3}|$ are the maximum necessary grid inverter voltage and current given by eq. (5.198) and eq. (5.196) respectively.

Current rating

The current ratings of the boost inductance has to be designed for the current given by eq. (5.196).

By use of the iterative design procedure described in Appendix B, it is possible to design an inductor complying with the specifications. Fig. 5.104 shows an example of the outcome of the present design procedure when using the SVPWM1 modulation method[10]. In Fig. 5.104 the inductor losses are calculated for 7 different inductor designs and shown as a function of the corresponding mass of the inductor design[11] (0.1mH to 0.4mH stepped by 50μH). The calculations are repeated for different current densities (1.5 A/mm^2 to 8 A/mm^2). The bold lines correspond to core designs where the temperature is kept below the maximum allowable temperature while thin lines correspond to designs which do not comply with the temperature specifications.

5.5.3 Design of DC-link

As was the case for the two-level converter the design of the DC-link for the three-level converter is not a necessary task for the loss calculation approach. However, as it is a general issue in the converter design and involves some non-trivial considerations, the current loading for which the DC-link needs to be designed will be derived. As discussed in section 3.5.3 when treating the DC-link design for the two-level converter the presence of the two active inverters feeding harmonic currents into the DC-link capacitors make the DC-link design a little more complex than the DC-link design of conventional uni-directional drives. Further due to the presence of the DC-link neutral connection, the calculation of the DC-link current stress seems to be even more complicated than for the two-level counterpart - at least from an initial point of view.

In general, the DC-link design include the following considerations [19]:

- Harmonic current ratings in steady-state operation.
- Peak-voltage suppression in case of a grid failure.
- Suppress the effect of a transient power mismatch between grid side inverter and rotor side inverter.

In this context, only the design considerations regarding the steady state operation are discussed. In the harmonic current calculation, the current definitions in Fig. 5.105 are used.

[10] As the current ripple is taken into consideration in the core design procedure described in Appendix B the calculated losses may slightly vary for different modulation methods.

[11] In the present example, the product of the inductance and the switching frequency is kept constant at 2.0.

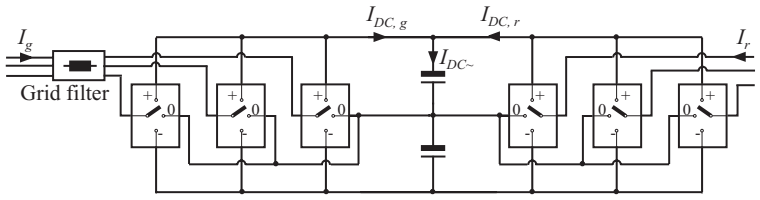


Figure 5.105: *Definition of the DC-link currents.*

Current contribution from the three-level rotor side inverter

The current fed from the rotor side to the DC-link $I_{DC,r}$ can be calculated from the switch states presented in section 5.3. Equation (5.202) below is valid for modulation method SVPWM1 and partly written for sector $\mathbf{0_a}$

$$I_{DCr} = \sqrt{\frac{1}{2\pi}\int_0^{\pi/3}(\frac{1}{2}\delta_1 \cdot i_A^2 + \frac{1}{2}\delta_2(-i_C)^2 + ...)d\Delta_s} \tag{5.202}$$

where the duty-cycle functions δ_1 and δ_2 is given by eq. (5.6) - (5.9) when considering the conventional modulation method and by eq. (5.15) when considering the modulation method with common mode voltage elimination. Evaluating the current originating from the rotor side inverter in the three-level inverter, it turns out that all the modulation schemes based on the conventional space vector modulation approach generates the same amount of DC-link current. The entire DC-link current $I_{DC,r}$ when considering the conventional modulation schemes is given by:

$$I_{DCr} = I_r\sqrt{\frac{M_r}{\pi}(1 + 4\cos^2(\phi_r))} \tag{5.203}$$

whereas for the modulation method with common mode voltage elimination, the DC-link current $I_{DC,r}$ is given by:

$$I_{DCr} = \frac{2}{3}\frac{3^{\frac{3}{4}}\sqrt{M_r\left(1 + (\cos(\phi_r))^2\right)}}{\sqrt{\pi}} \tag{5.204}$$

Fig. 5.106 shows the RMS DC-link current from the rotor side inverter as a function of the load angle ϕ_r and the modulation index M_r when using the conventional modulation methods. Similarly, Fig. 5.107 shows the RMS DC-link current from the rotor side inverter as a function of the load angle ϕ_r and the modulation index M_r when using the modulation method with common mode elimination. The DC-link current $I_{DC,r}$ calculated by eq. (5.203) and eq. (5.204) can be considered as being composed of an average value $I_{DC,r=}$ and a ripple current $I_{DC,r\tilde{}}$ related by:

$$I_{DC,r} = \sqrt{I_{DC,r=}^2 + I_{DC,r\tilde{}}^2} \tag{5.205}$$

The average current $I_{DC,r=}$ fed from the rotor circuit to the DC-link is independent of the modulation method and is given by:

$$I_{DC,r=} = \frac{6}{2\pi}\int_0^{\frac{\pi}{3}}(\delta_1 \cdot i_A + \delta_2(-i_C))d\Delta_s \tag{5.206}$$

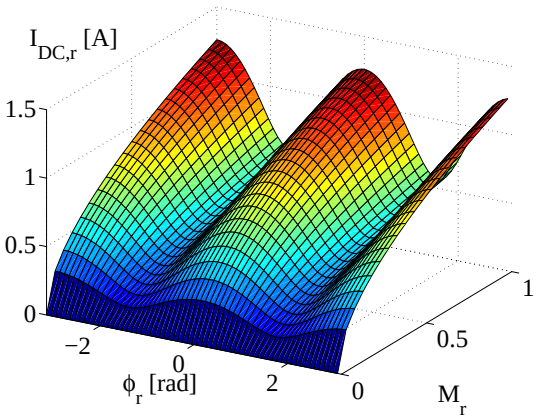


Figure 5.106: *The DC-link current $I_{DC,r}$ (RMS) due to the switching operation of the rotor inverter when using the conventional modulation methods.*

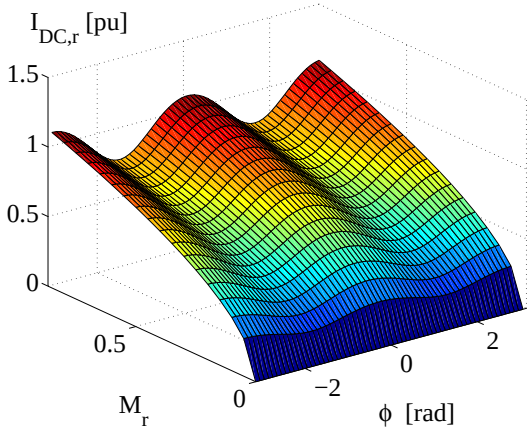


Figure 5.107: *The DC-link current $I_{DC,r}$ (RMS) due to the switching operation of the rotor inverter when using the modulation method with common mode elimination.*

On a closed for, the average current $I_{DC,r=}$ becomes:

$$I_{DC,r=} = \frac{\sqrt{6}}{2} M_r \cdot \cos(\phi_r) \cdot I_r \tag{5.207}$$

Since the current through the DC-link capacitors do not contain any DC-component, the current through the capacitors can be derived from eq. (5.205). For the modulation schemes based on the conventional modulation approach, the RMS-current through the capacitors is given by:

$$I_{DC,\tilde{r}} = \frac{1}{2} I_r \sqrt{\left(\frac{16}{\pi} - 6M_r\right) M_r \cdot \cos(\phi_r)^2 + \frac{4}{\pi} M_r} \tag{5.208}$$

Considering the RMS current through the capacitors when using the modulation method with common-mode voltage elimination the expression is given by:

$$I_{DC,\tilde{r}} = I_r \sqrt{\frac{M_r \left(8\sqrt{3}\left(1 + \cos\left(\phi_r\right)^2\right) - 9\, M_r \pi\, \cos\left(\phi_r\right)^2\right)}{6\pi}} \tag{5.209}$$

Fig. 5.108 and Fig. 5.109 show the harmonic DC-link capacitor current originating from the rotor side inverter as a function of the load angle ϕ_r and the modulation index M_r.

Current contribution from the three-level grid side inverter

The current contribution from the grid side inverter is derived similar to the derivation of the current contribution from the rotor side inverter. The RMS capacitor current originating from the grid side inverter when using the modulation schemes based on the conventional space vector approach is given by:

$$I_{DC,\tilde{g}} = \frac{1}{2} I_g \sqrt{\left(\frac{16}{\pi} - 6M_g\right) M_g \cdot \cos^2(\phi_g) + \frac{4}{\pi} M_g} \tag{5.210}$$

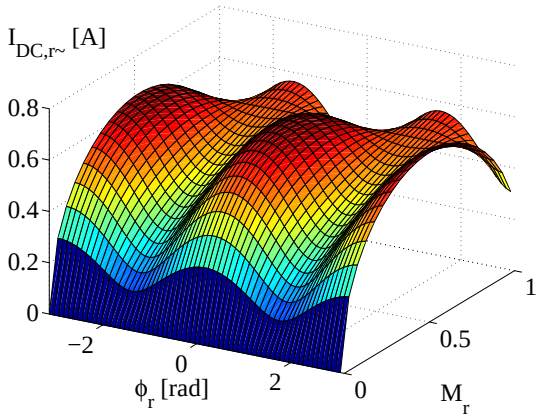


Figure 5.108: *The DC-link capacitor current $I_{DC,\tilde{r}}$ (RMS) due to the switching operation of the rotor inverter when using the conventional modulation schemes.*

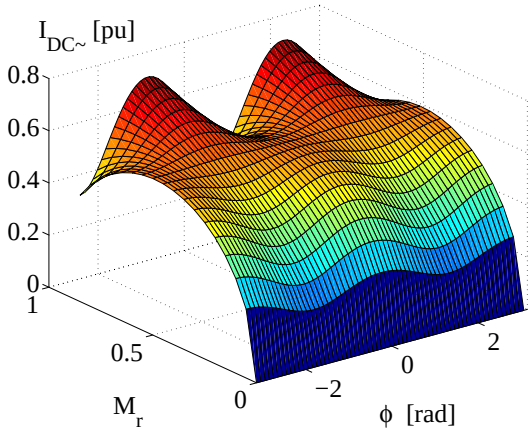


Figure 5.109: *The DC-link capacitor current $I_{DC,\tilde{r}}$ (RMS) due to the switching operation of the rotor inverter when using the modulation method with common mode voltage elimination.*

where ϕ_g is the angle between the grid inverter reference voltage and the grid current and M_g is the modulation index of the grid side inverter. Using the modulation method with common-mode voltage elimination, the RMS capacitor current originating from the grid side inverter becomes:

$$I_{DC,\tilde{g}} = I_g \sqrt{\frac{M_g \left(8\sqrt{3}\left(1+\cos\left(\phi_g\right)^2\right) - 9\,M_g\pi\,\left(\cos\left(\phi_g\right)\right)^2\right)}{6\pi}} \tag{5.211}$$

Current stresses on the DC-link capacitors

Although having the current contribution from both the grid side inverter and the rotor side inverter, the current stress on the DC-link is still quite complex to derive. Actually, in the general form, each harmonic component (h) of the grid- and rotor side inverter has to be added vectorially. That is [33, 34]:

$$\begin{aligned} I_{DC\tilde{}}^2 &= \sum_{h=1}^{\infty} (\underline{I}_{DC,\tilde{g}}(h) + \underline{I}_{DC,\tilde{r}}(h))^2 \\ &= \sum_{h=1}^{\infty} (I_{DC,\tilde{g}}^2(h) + I_{DC,\tilde{r}}^2(h) + 2 \cdot I_{DC,\tilde{g}}(h) \cdot I_{DC,\tilde{r}}(h) \cos(\theta_g(h) - \theta_r(h)) \end{aligned} \tag{5.212}$$

where $\theta_g(h)$ and $\theta_r(h)$ is the angle of the individual harmonic. The angle of the harmonics depend on the synchronization of the grid side modulator and rotor side modulator. Clearly, the expression of the DC-link harmonic current, involving the need for a harmonic analysis is of limited value in a rough DC-link design. However, with the assumption that the grid side inverter and rotor side inverter are operated at different switching frequencies and in addition, contains no common higher harmonics, the current

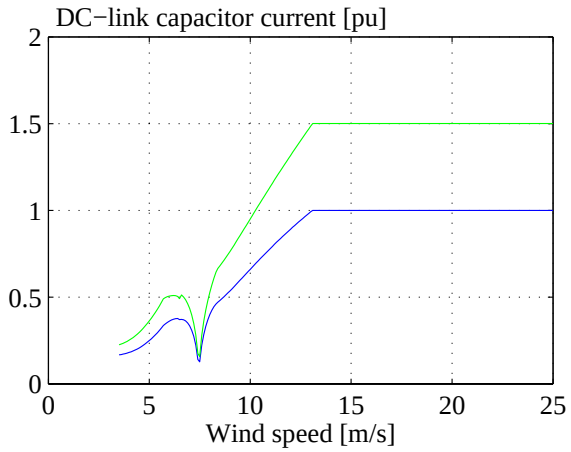


Figure 5.110: *The current through the DC-link capacitors as a function of the wind speed in a typical wind turbine application.*

stress on the DC-link capacitors can be approximated by:

$$I_{DC} = \sqrt{I_{DC,\tilde{g}}^2 + I_{DC,\tilde{r}}^2} \tag{5.213}$$

From eq. (5.212) it appears that selecting the switching frequencies of the grid side inverter and rotor side inverter with an integer multipla in difference and further synchronizing the modulators the DC-link capacitor current may be reduced from the values obtained by the expression in eq. (5.213). Fig. 5.110 shows an example of the DC-link capacitor current as a function of the wind speed for a typical wind turbine application. The blue curve shows the DC-link RMS current when using the conventional space vector approach while the green curve shows the DC-link RMS current when using the modulation scheme with common mode voltage elimination. Both curves are normalized to the DC-link current in nominal operation when using the conventional modulation method.

5.5.4 Modulation strategy and switching frequency

As it appeared from the evaluation of the harmonic distortion, c.f. section 5.3.6, the modulation methods for the three-level inverter behave quite different and varies with the modulation index. To obtain a fair comparison between the modulation methods -including a comparison of modulation methods between different converters - one of the evaluation parameters has to form a common basis for the comparison. Using the harmonic performance as a comparison basis, the switching frequency of the different modulation methods are to be adjusted for obtaining the same evaluation basis. Using the suboptimal modulation method for the two-level inverter as the basis, the switching frequency for the three-level inverter modulation schemes have to be adjusted according to Fig. 5.111. Fig. 5.111 shows the switching frequency correction factor $k_{sw,v}$ as a function of the modulation index M. Having the modulation index M_0 for the nominal working condition, the switching frequency correction factor for the different modulation

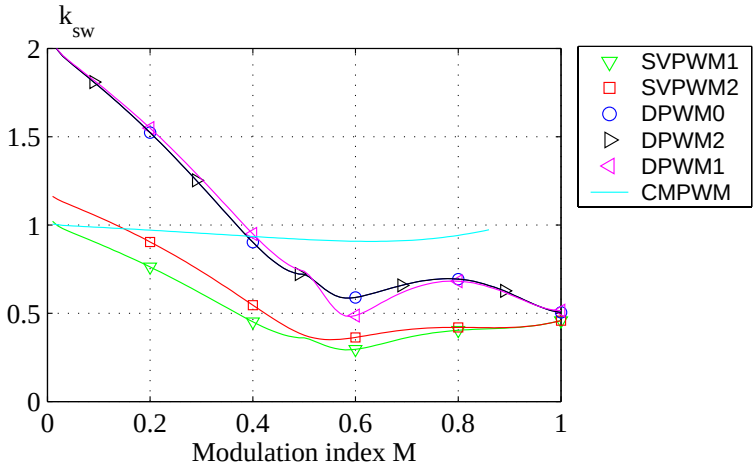


Figure 5.111: *The switching frequency correction factor normalized to the suboptimal modulation method of the two-level voltage source inverter, c.f. section 3.3.3 on page 53.*

methods can be polynomial-fitted. The switching correction factor for the SVPWM1 method can be approximated by:

$$k_{sw,v} = 45.40M_0^6 - 139.0M_0^5 + 155.27M_0^4 - 75.41M_0^3 + 15.74M_0^2 - 2.57M_0 + 1.06 \quad (5.214)$$

where M_0 is the modulation index when operating in nominal conditions. Similarly, switching correction factor for the SVPWM2 modulation method can be approximated by:

$$k_{sw,v} = 68.4M_0^6 - 205.7M_0^5 + 226.4M_0^4 - 108.9M_0^3 + 22.07M_0^2 - 3.01M_0 + 1.21 \quad (5.215)$$

while the correction factor for the DPWM0 and DPWM2 method becomes:

$$k_{sw,v} = 82.67M_0^6 - 254.1M_0^5 + 282.7M_0^4 - 135.9M_0^3 + 27.86M_0^2 - 4.80M_0 + 2.09 \quad (5.216)$$

The correction factor for the DPWM1 method are approximated by:

$$k_{sw,v} = 89.92M_0^6 - 290.2M_0^5 + 342.6M_0^4 - 178.6M_0^3 + 40.63M_0^2 - 6.08M_0 + 2.12 \quad (5.217)$$

and finally, for the CMPWM, the switching frequency correction factor can be approximated by:

$$k_{sw,v} = -0.532M_0^6 - 1.02M_0^5 + 0.46M_0^4 - 1.00M_0^3 + 0.36M_0^2 - 0.211M_0 + 1.01 \quad (5.218)$$

5.6 Model of the back-to-back three-level voltage source converter

Input to the converter model are given, both from the generator side and from the grid side, i.e. from the transformer. Input to the rotor side inverter are the rotor voltage,

rotor current, load angle and frequency, all given by the generator modeling approach described in section 2.4. Input to the grid side inverter are the grid voltage, i.e. the voltage on the tertiary side of the transformer, c.f section 2.5, the grid frequency and the desired reactive power generation from the grid side inverter. Based on these input, the converter model has to output the resulting grid current supplied to the tertiary transformer windings along with the converter losses and internal temperatures.

5.6.1 Converter losses

Depending on the chosen modulation method (can be selected differently for the grid side inverter and the rotor side inverter), the total converter losses can be derived from the equations given in section 5.4. The losses of the rotor side inverter, $P_{inv,r}$, is given by:

$$\begin{aligned} P_{inv,r} &= 6\big(P_{cond,t1r} + P_{cond,d1r} + P_{cond,t3r} + P_{cond,d3r} + P'_{cond,d3r} + \\ &\quad P_{sw,t1r} + P_{sw,d1r} + P_{sw,t3r} + P_{sw,d3r} + P'_{sw,d3r}\big) \\ &= 6\big(V_{tr0}(T)\cdot I_{t1r,avg} + R_{tr}(T)\cdot I_{t1r}^2 + V_{dr0}(T)\cdot I_{d1r,avg} + R_{dr}(T)\cdot I_{d1r}^2 + \\ &\quad V_{tr0}(T)\cdot I_{t3r,avg} + R_{tr}(T)\cdot I_{t3r}^2 + V_{dr0}(T)\cdot I_{d3r,avg} + R_{dr}(T)\cdot I_{d3r}^2 + \\ &\quad V_{dr0}(T)\cdot I'_{d3r,avg} + R_{dr}(T)\cdot I'^2_{d3r} + \\ &\quad \frac{V_{DC}}{2}\cdot f_{swr}\cdot\big(E_{sw0,tr}(T)\cdot I_{t1r,swavg} + E_{sw0,dr}(T)\cdot I_{d1r,swavg} + \\ &\quad E_{sw0,tr}(T)\cdot I_{t3r,swavg} + E_{sw0,dr}(T)\cdot I_{d3r,swavg} + E_{sw0,dr}(T)\cdot I'_{d3r,swavg}\big)\big) \end{aligned} \tag{5.219}$$

The current quantities in eq. (5.219) has to be evaluated according to the chosen modulation strategy. The modulation method dependent expression for the current quantities are derived in section 5.4.

Similarly, the grid side inverter losses may be evaluated:

$$\begin{aligned} P_{inv,g} &= 6\big(P_{cond,t1g} + P_{cond,d1g} + P_{cond,t3g} + P_{cond,d3g} + P'_{cond,d3g} + \\ &\quad P_{sw,t1g} + P_{sw,d1g} + P_{sw,t3g} + P_{sw,d3g} + P'_{sw,d3g}\big) \\ &= 6\big(V_{tg0}(T)\cdot I_{t1g,avg} + R_{tg}(T)\cdot I_{t1g}^2 + V_{dg0}(T)\cdot I_{d1g,avg} + R_{dg}(T)\cdot I_{d1g}^2 + \\ &\quad V_{tg0}(T)\cdot I_{t3g,avg} + R_{tg}(T)\cdot I_{t3g}^2 + V_{dg0}(T)\cdot I_{d3g,avg} + R_{dg}(T)\cdot I_{d3g}^2 + \\ &\quad V_{dg0}(T)\cdot I'_{d3g,avg} + R_{dg}(T)\cdot I'^2_{d3g} + \\ &\quad \frac{V_{DC}}{2}\cdot f_{swg}\cdot\big(E_{sw0,tg}(T)\cdot I_{t1g,swavg} + E_{sw0,dg}(T)\cdot I_{d1g,swavg} + \\ &\quad E_{sw0,tg}(T)\cdot I_{t3g,swavg} + E_{sw0,dg}(T)\cdot I_{d3g,swavg} + E_{sw0,dg}(T)\cdot I'_{d3g,swavg}\big)\big) \end{aligned} \tag{5.220}$$

The grid inductor power losses P_L are calculated according to eq. (5.189) on page 231.

5.6.2 Power transferred to the transformer

According to eq. (2.47) on page 39 input to the transformer modeling approach is the grid inverter current $\underline{I}_{g3}$, the stator current I_s and the primary side voltage $\underline{V}_{g1}$. Hence,

besides the converter losses, the only necessary output from the converter modeling is the grid inverter current. The grid inverter current is given by:

$$\underline{I}_{g3} = \frac{(P_r - (P_{inv,r} + P_{inv,g} + P_L)) + j \cdot Q_g^*}{3 \cdot \underline{V}_{g3}} \tag{5.221}$$

5.7 Summary

The aim of this chapter was to establish a foundation for a fair and direct comparison of the three level voltage source inverter with the more matured two-level voltage source inverter. Although an inverter with three-level properties can be realized by several topologies, the chapter has focused on only two three-level inverter topologies, namely the diode clamped three-level inverter and the transistor clamped three-level inverter. The chapter was introduced by a brief survey on previous work, trends and focus areas in the field of three level inverters. However, as three-level inverters are relatively unknown in wind turbine applications the survey covered activities within other technical areas. Then the basic working principles was discussed followed by a thorough explanation of the modulation principles especially with focus on the space vector approach[12]. As the modulation schemes for the three-level inverters are not as matured as the corresponding modulation schemes for the two-level inverter, a lot of efforts have been dedicated to the development of modulation schemes comparable to the schemes for the two-level counterpart. The developed modulation schemes included discontinuous schemes [11] and schemes with complete common-mode voltage elimination [10]. As the DC-link balance is a major issue for three-level inverters, all the developed schemes included active DC-link balancing capabilities. As discussed in chapter 3 one criteria for comparison is the harmonic distortion of the generated output voltage and hence the discussed modulation schemes were evaluated with respect to this distortion. Further, in order to use an RMS model for the purpose of comparing the different modulation methods as well as the different topologies the inverter losses were to be calculated. This involved derivation of analytical expressions for both RMS current and average current through each individual component - expressions which turned out to be modulation method dependent, load angle dependent as well as modulation index dependent. For the purpose of including the switch temperature in the converter loss evaluation, analytical expressions for the average switch temperature has been derived. Further, due to the fact that the rotor inverter in the doubly-fed system is operated at variable but low frequencies the peak temperature deviate quite much from the average temperature. Hence for the purpose of a fast validation of a certain converter design, some analytical approximations for the peak temperature has been proposed. Finally, to be able to predimension the back-to-back three-level voltage source converter, some rules of thumb regarding switch current ratings, switch voltage ratings, DC-link design and inductor design has been presented.

[12]For completeness, the carrier based modulation functions of the considered modulation methods were also derived.

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Chapter 6

The wind turbine comparison tool D′rives

SO far all efforts have been dedicated to the derivation of suitable models describing the individual wind turbine components. Although the purpose of the modeling approach was to obtain a fast and simple calculation tool, it turned out that the number of equations and parameters involved are quite high. To obtain a usable calculation tool it seems necessary to have a graphical interface providing a well-arranged overview of the involved parameters and at the same time linking the right equations depending on the chosen turbine configuration and control method. The purpose of this chapter is to describe the simulation tool D′rives which is a simulation package with a graphical user interface linking the turbine models derived in chapter 2-5. In many aspects the functionality of D′rives is comparable to existing simulation tools such as MELCOSIM [1, 2] and SEMISEL [3, 4] provided by Mitsubishi and Semikron respectively. However MELCOSIM and SEMISEL both require converter loading conditions which require time consuming and potential erroneously pre-calculations whereas D′rives calculates all converter loading from the equations describing the surrounding components. Even though the D′rives program takes into account all the main components of the wind turbine, the simulation speed is still very high due to the explicit analytical expressions for the component loadings and component losses. For instance, a simulation of peak temperatures of the semiconductors in a converter design calculated for the entire power/speed operating range has been reduced from a day-long simulation task into a simulation time of few seconds.

As the D′rives is considered as a property of Vestas Wind Systems A/S, the program is not publicly available and hence some aspects of the chapter may be of limited interest for readers not employed by Vestas. Nevertheless, besides providing a "*Getting started*" manual, the chapter provides an overview on the flexibility and facilities in D′rives - facilities used for the converter comparison in chapter 7.

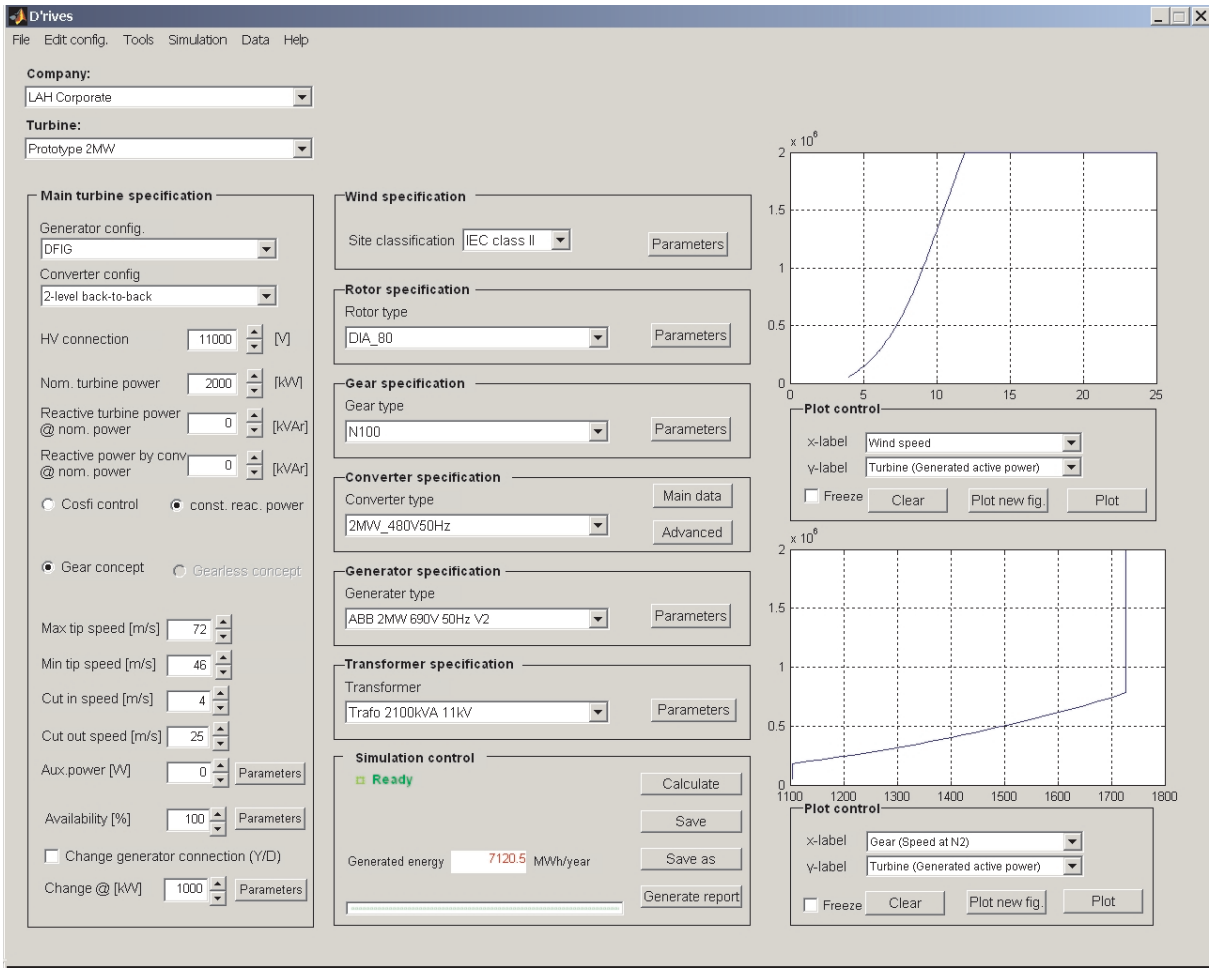

Figure 6.1: *User interface of the wind turbine comparison tool.*

6.1 Main user interface in D′rives

Fig. 6.1 shows the main user interface of the comparison tool "D′rives". Considering the user interface, the left part concerns the main turbine characteristics, the center part concerns the individual turbine components and the right part provides a graphical representation of the obtained results.

6.1.1 Menu

The top menu contains the following items: File, Edit config, Tools, Simulation, Data and Help. The content of the menu items are shown in Fig. 6.2. In the File menu the following actions are available:

File||New company: Create your own library for your own turbine models. A library contains one ore more turbines (or turbine models). For instance, one library could contain the Vestas turbine portfolio while another library could be created by a user and used for investigation of customized turbines/future turbines. A library

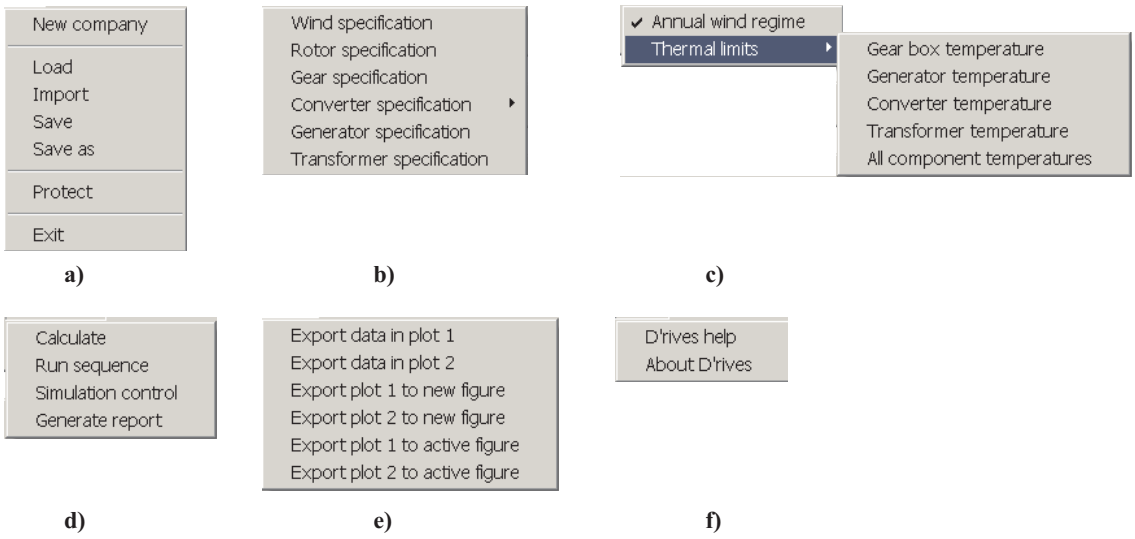

Figure 6.2: *The content of the menu items.* **a)** *The File menu.* **b)** *The Edit config menu.* **c)** *The Tools menu.* **d)** *The Simulation menu.* **e)** *The Data menu.* **f)** *The Help menu.*

can be password protected to avoid unauthorized editing. However the password do not protect the library from being used by others or from being imported to other users libraries.

File‖Load: Load a new turbine library. Be aware that libraries of other users may be password protected preventing unauthorized editing in turbine models. The load command actually performs the same action as obtained by selecting a new company from the company popup menu, c.f. Fig 6.1.

File‖Import: The import function allows the user to import a turbine model from another turbine library. This action is allowed despite the imported turbine model is located in a password protected library.

File‖Save: The save function save the changes made to the main turbine, i.e changes made from the main page shown in Fig. 6.1. All changes made in the user interfaces for the individual components have to be saved from the individual component user interfaces, c.f. section 6.2. Saving may require a password if the current turbine library is password protected. The save action can also be performed by pushing the save button.

File‖Save as: The ”save as” function save the changes made to the main turbine as a new turbine into the current library. Only changes made from the main page shown in Fig. 6.1 are saved whereas all changes made in the user interfaces for the individual components have to be saved from the individual component user interfaces. The saving action may require a password if the current turbine library is password protected. The ”save as” action can also be performed by pushing the button ”Save as”, c.f. Fig 6.1.

File‖Protect: Allows the user to password protect the current library (company).

File‖Exit: Terminates the Drives program. If changes have been made without saving the user is prompted for a saving action.

In the Edit config menu, the following actions are available:

Edit‖Wind specification: Opens the wind parameter specification dialog. This action corresponds to the action obtained by pushing the parameter button in the wind specification box and will be discussed further in section 6.2.1.

Edit‖Rotor specification: Opens the rotor parameter specification dialog. This action corresponds to the action obtained by pushing the parameter button in the rotor specification box and will be discussed further in section 6.2.2.

Edit‖Gear specification: Opens the gear parameter specification dialog. This action corresponds to the action obtained by pushing the parameter button in the gear specification box and will be discussed further in section 6.2.3.

Edit‖Converter specification: Opens the converter parameter specification dialog. This action corresponds to the action obtained by pushing the parameter button in the converter specification box and will be discussed further in section 6.2.6.

Edit‖Generator specification: Opens the generator parameter specification dialog. This action corresponds to the action obtained by pushing the parameter button in the generator specification box and will be discussed further in section 6.2.4.

Edit‖Transformer specification: Opens the transformer parameter specification dialog. This action corresponds to the action obtained by pushing the parameter button in the transformer specification box and will be discussed further in section 6.2.5.

In the Tools menu, the following actions are available:

Tools‖Annual wind regime: In this mode, the simulation programme performs a sweep for the specified wind speed range and calculates the loading on the individual components. This mode allows calculation of annual energy production.

Tools‖Thermal limits: In this mode the specified wind speed range is disregarded and the simulation program performs a sweep within the specified speed range and then determines the power capability of the considered component. The speed range is determined by the minimum allowed tip speed and the maximum allowed tip speed. In fact this mode can be used to calculate the power limits of the turbine due to e.g. the converter design and hence determining the safety margin of the actual design. Actually, as shown in Fig. 6.2b, the power capability determined by any of the main components can be calculated, although the validity of the obtained results are dependent on the thermal model of the considered component. During

simulations of the power capability determined by one of the main components, the simulator suggests that all other models are calculated without considering the thermal calculations. This suggestion is due to the fact that challenging one components power capability in the entire speed range may very well force other components to be operated in a range where their thermal model is no longer valid, i.e. corresponding to a physical break down of the component.

In the Simulation menu, the following actions are available:

Simulation‖Calculate: This action starts the calculation. This action can also be activated by pushing the calculation button.

Simulation‖Run sequence: This action allows a sequential calculation of different designs and/or different operation conditions. The sequences to be calculated are loaded from a text file. Before entering a sequential calculation, the results to be shown in the graphical part has to be chosen. Once a sequence has been run any change in the graphical interface will only display the result from the last run in the sequence.

Simulation‖Simulation control: This action opens a dialog enabling the user to modify the aggressiveness of the solver and to set the acceptable tolerance on the simulation result. This may speed up/slow down the simulation time. This action can also be used in cases where the actual simulation seems troublesome for the solver. Besides tolerances, the simulation control dialog is used to limit the number of iterations and/or the limit the maximum allowed simulation time. Further, the number of data to be exported along with the data format is controlled from this dialog box. Finally, the filenames used for error log file, default export data file and net list file is specified from the Simulation control dialog.

Simulation‖Generate report: The generate report action creates a net list of the parameters and configurations used in the last simulation. This net list can be used for later reference. The file name for the net list is specified in the simulation control dialog, c.f. item above.

In the Data menu, the following actions are available:

Data‖Export data in plot 1: Exports the content of plot #1 to a fixed space delimited text file. The number of data and the data format are specified in the simulation control dialog. The first column of the text file contains the x-axis data whereas the remaining columns contains the y-axis data. The export data action will prompt the user for a filename to be used. The default appearing filename is specified in the simulation control dialog. If the data to be exported are distinct, i.e. the x-data are in an increasing order, the data are curve fitted in order to obtain an equal spacing between the exported data. For non-distinct data the export function picks out the necessary number of data.

Data‖Export data in plot 2: Exports the content of plot #2 to a fixed space delimited text file. The number of data and the data format are specified in the simulation control dialog. The first column of the text file contains the x-axis data whereas the remaining columns contains the y-axis data. The export data action will prompt the user for a filename to be used. The default appearing filename is specified in the simulation control dialog. If the data to be exported are distinct, i.e. the x-data are in an increasing order, the data are curve fitted in order to obtain an equal spacing between the exported data. For non-distinct data the export function picks out the necessary number of data.

Data‖Export plot 1 to new figure: Opens a new external figure and reprints the content of plot #1 into this figure. The new figure contains a legend explaining the different plots.

Data‖Export plot 2 to new figure: Opens a new external figure and reprints the content of plot #2 into this figure. The new figure contains a legend explaining the different plots.

Data‖Export plot 1 to active figure: If a figure is open this action reprints the content of plot #1 into this figure. If more figures are open, the last activated figure will receive the data from plot #1. If no figure is open, this action correspond to the "Data—Export plot 1 to new figure" action.

Data‖Export plot 2 to active figure: If a figure is open this action reprints the content of plot #2 into this figure. If more figures are open, the last activated figure will receive the data from plot #2. If no figure is open, this action correspond to the "Data—Export plot 2 to new figure" action.

In the Help menu, the following actions are available:

Help‖D′rives help: Provides a functional description of the D′rives programme. The description corresponds to the content of this chapter.

Help‖About D′rives: Displays the actual version of the programme D′rives.

6.1.2 Main turbine specification

The main turbine specification area (left part of the main user interface) allows the user to change the main characteristics of the considered wind turbine including change of generator[1]- and converter topology, connection condition such as voltage level, nominal active and reactive power production. Further, the main turbine specification includes control parameters such as cut-in and cut-out wind speed, maximum and minimum tip speed, including noise limiting operating conditions and Y-Δ connection control of

[1]Since only the doubly-fed induction generator is treated in this report, this description will not contain the remaining generator topologies.

the generator. Finally, the main turbine specification includes change of parameters impacting on the availability of the turbine and specification of the auxiliary power consumption. The auxiliary power consumption includes several auxiliary components with separate specification of their operation condition dependent power consumption.

Generator config.: The program support the following generator topologies, doubly-fed induction generator, induction generator, synchronous generator, permanent synchronous generator and variable rotor resistor induction generator. The modeling of the generator is described in section 2.4.

Converter config.: The program supports the following converter topologies: 2-level back-to-back voltage source converter, three-level back-to-back voltage source converter, matrix converter, 2-level voltage source converter with passive generator side inverter, 2-level voltage source converter with passive grid side inverter and without any power converter. The modeling of the power converter is described in chapter 3 - chapter 5.

6.2 Model of the wind turbine components

In the center part of the main user interface, the main components of the turbine can be changed and parameters of the existing models can be modified. At this stage it is important to note that any change made within the parameters describing the individual main components will affect all turbines using the particular component. If a parameter change is only to affect one single turbine, the component for which the parameters were changed has to be saved as a new component and then to be included in the particular turbine.

6.2.1 Wind parameters

Entering the dialog box for the wind conditions allows the user to modify the wind distribution. More specific the dialog allows specification of the parameters a and c in the Weibull distribution, c.f. eq. (2.4) on page 25. The programme includes four standard annual wind distributions "IEC class I" - "IEC class IV" having the parameters given i Table I on page 26.

6.2.2 Blade parameters

The popup menu in the rotor specification box allows the user to select among the available blade designs by pushing the popup menu. Entering the blade parameter wizard by pushing the parameter button provides a graphical view of the power performance profile of the selected blade. Alternatively, the user can specify a user defined power performance profile versus tip speed ratio and indicate whether the profile is pitchable. The blade specification dialog is shown in Fig. 6.3.

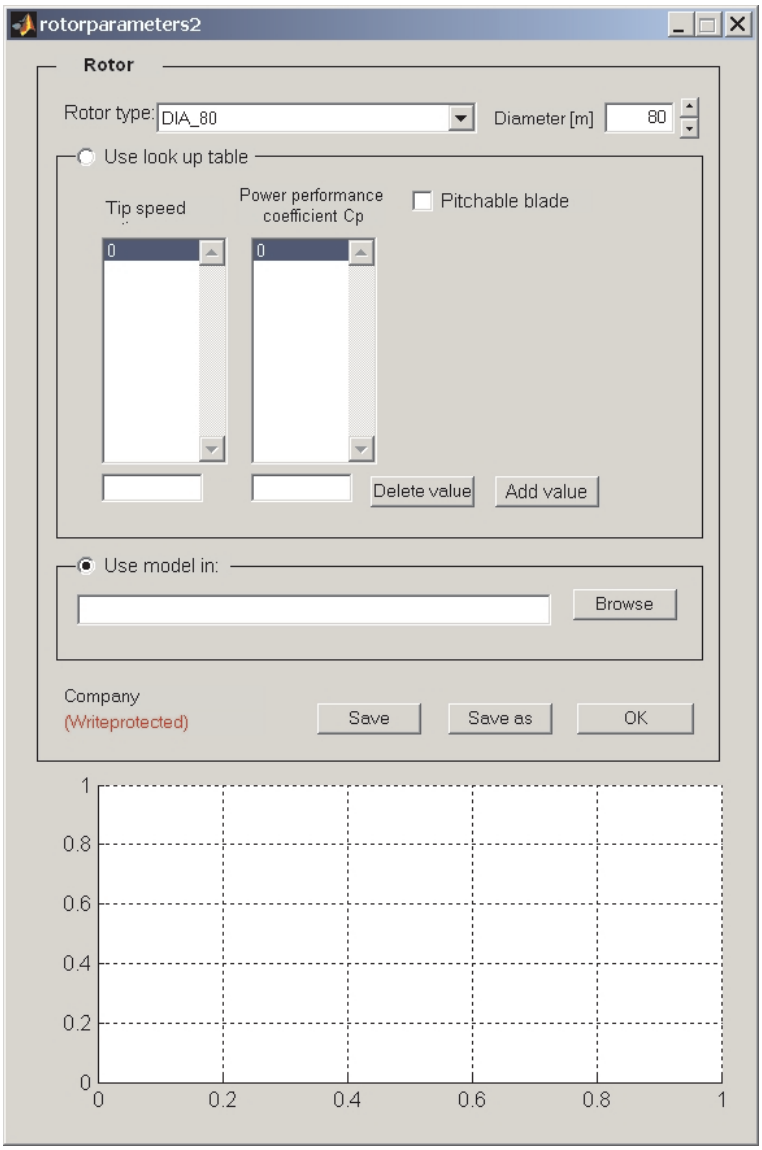

Figure 6.3: *Rotor parameter wizard.*

6.2.3 Gear parameters

From the main menu, the choice of gear type can be altered by pushing the popup menu in the gear parameter box. This action allows the user to select a gear type from a list of available gear boxes. Modification of gear parameters or establishment of a new gear model are to be done from the gear box parameter wizard. The gear box parameter wizard is entered by pushing the parameter button in the gear specification box or alternatively from the menu "Edit config||Gear specification". The gear box parameter wizard is shown in Fig. 6.4. In the gear box parameter wizard the user can choose another gear box from the list, change the gear ratio and select an appropriate gear loss model. Actually, the user can opt to use the standard equation given by eq. 2.9 on page 29, make use of a look up table or alternatively make use of a self made model, provided that this model respect the required input and output interface.

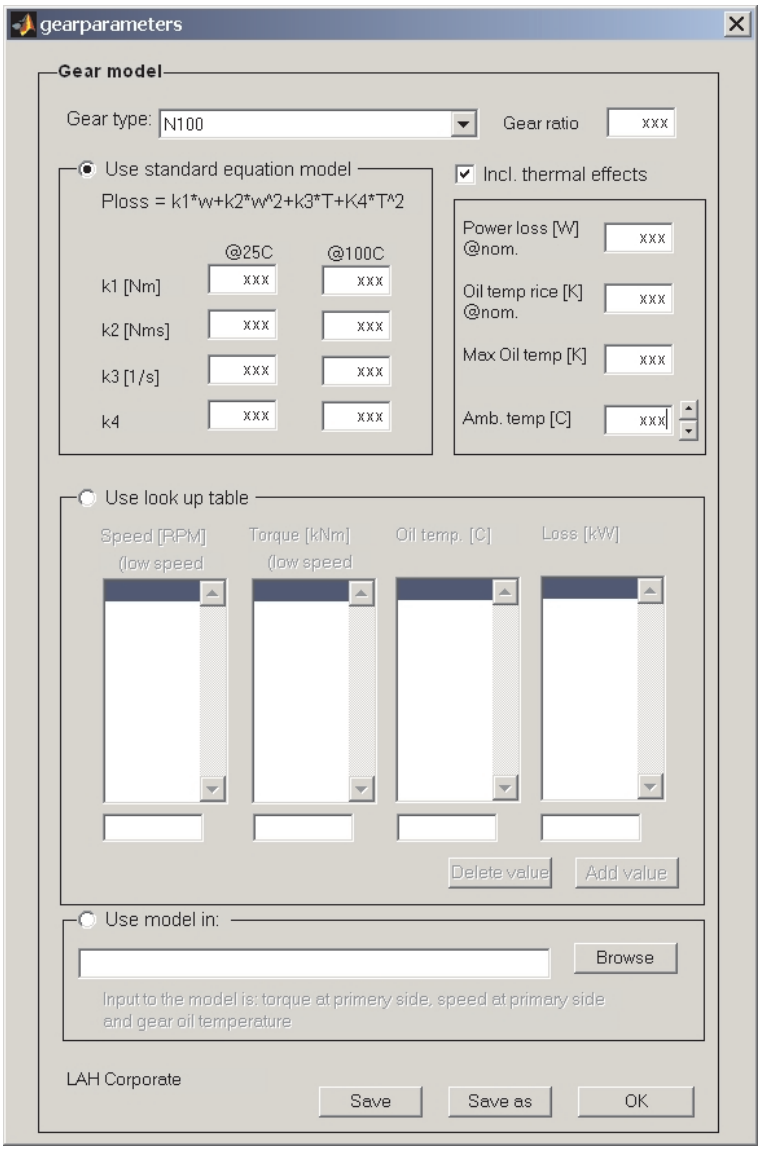

Figure 6.4: *Gear box parameter wizard.*

Enabling the gear box model to include thermal effects, the model based on the standard loss equation simply uses a one dimensional thermal model where the thermal resistance is calculated from the gear losses at nominal operating conditions and the corresponding temperature rice. The parameter "Max oil temp" is used to specify the maximum allowed gear oil temperature and a simulation of conditions where this temperature is exceeded will generate a warning to the user.

On exit the user can choose to save the changes to the existing gear type by pushing the "save" button. This action will overwrite existing data for the particular gear type without any notification. Alternatively the user can choose to push the "Save as" button. By this action, the user will be prompted for a name for the new gear box whereupon the gear box model is added to the working library. It should be noted that

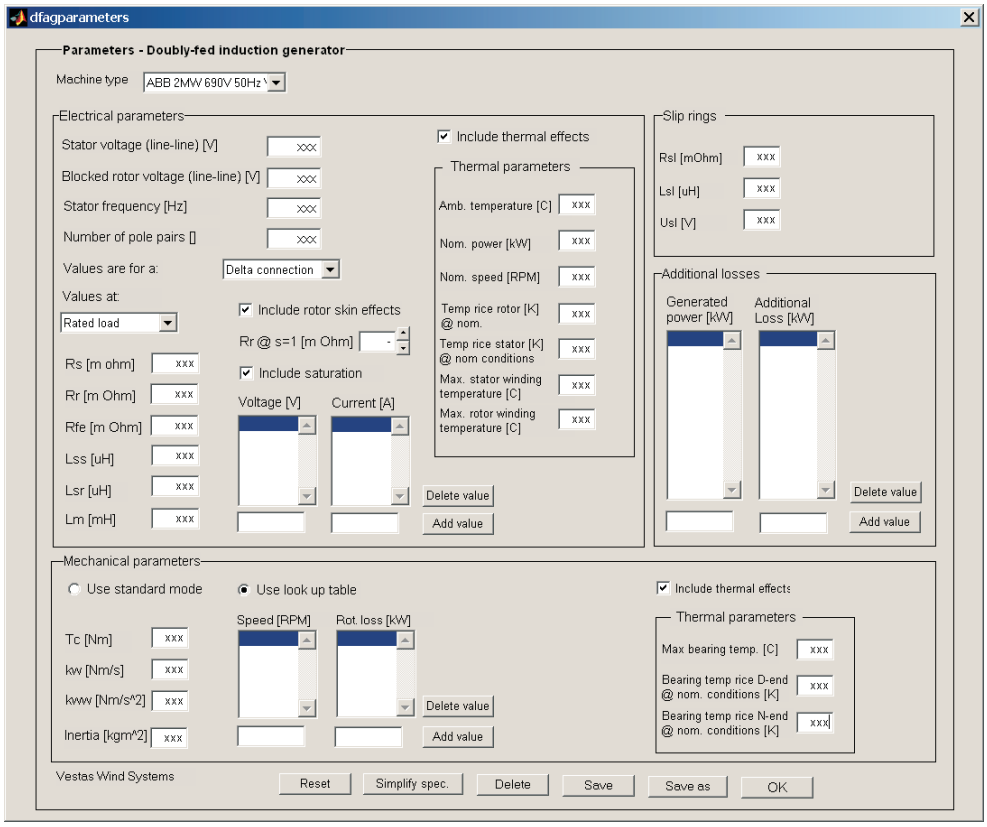

Figure 6.5: *Generator parameter wizard for the DFIG.*

if the current working library is password protected, the save and save as action is not possible. Pushing the "OK" button generates a temporary gear box model (prototype model) which will be used for the next simulation. It must be noted that any action in the main menu forcing the simulator to reload gear data will overwrite this temporary file with the gear data store in the working library. Such actions include change of company, change of turbine, change of gear type and entrance of the gear box wizard. Pushing the "OK" button automatically closes the gear box wizard.

6.2.4 Generator parameters

From the main user interface, the user can select a new generator from the list in the popup menu whereas change of generator parameters or registration of a new generator is to be done by entering the generator parameter wizard. The generator parameter wizard for the doubly-fed induction generator is shown in Fig. 6.5. The generator parameter wizard for the doubly-fed induction generator is divided into four main groups, one group relating to the electrical model of the generator, another group relating the mechanical modeling a third group relating to the slip rings and finally a group where additional power losses of the generator can be entered.

In the group "Electrical parameters" all parameters relating to the equations in sec-

tion 2.4 on page 30 are to be entered. The check box "Include rotor skin effects" forces the simulator to take eq. (2.32) on page 35 into account whereas the check box "Include saturation" varies the magnetizing inductance in accordance with the calculated magnetizing current. Applying the thermal calculations of the stator and rotor temperature by checking the "Include thermal effects", the simulator makes use of the simple one-dimensional approach given by eq. (2.33) and eq. (2.34) on page 36. The thermal impedances α_s and α_r are derived from the temperature rice in stator and rotor at nominal conditions. Specifying a maximum allowed temperature for the stator- and rotor winding will generate a warning message if a simulated condition generates a temperature exceeding the specified values.

In the group "Mechanical parameters" the parameters describing the rotational losses are to be entered. Two approaches are available, either the use of the standard equation for the rotational losses given by eq. (2.12) on page 31 or an approach based on a simple look up table. Applying the thermal calculation by checking the "Include thermal effects" the bearing temperatures are calculated. The calculations of the bearing temperatures are based on the same simple one-dimensional model as described for the calculation of winding temperatures and uses the temperature rice at nominal conditions to determine the thermal impedance of the bearings.

The third box "Slip rings" include the parameters determining the voltage drop and power losses of the slip rings.

Since generators in this size typically requires internal and/or external cooling means, the forth group "Additional losses" can be used to enter power losses related to such cooling means. The additional losses are based on a two dimensional look-up table using the generated power to determine the additional losses. It could be argued that since the additional losses may be used to describe the ventilation losses of an internal cooling fan the look-up table should be three-dimensional where the third dimension should represent the rotational speed of the generator. In the present approach, these additional ventilation losses are to be added in the mechanical parameters describing the rotational losses.

On exit the user can choose to save the changes to the present generator type by pushing the "save" button hereby overwriting existing data or alternatively save the changes to a new generator type. The latter action will add a new generator type to the list of available generator types in the actual company library. The "save as" action will prompt the user for a name for the new generator. In case the working library is password protected, the save and save as buttons are not available. Omitting the "save" and "save as" and simply just pushing the "OK" button on exit will generate a temporary file for the generator model. This temporary file is used in the simulations as long as no action forces the simulator to reload generator data. Such actions include change/reload

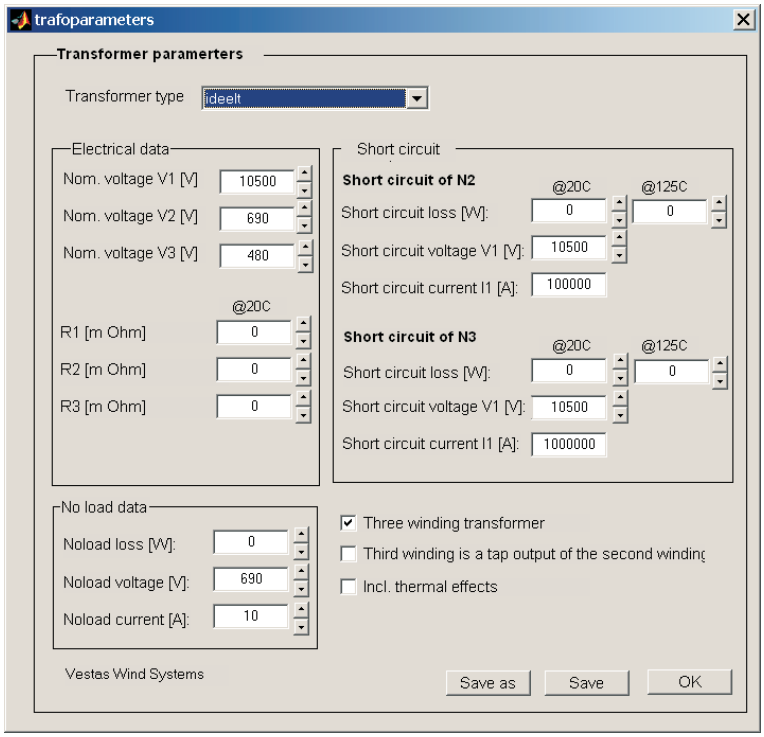

Figure 6.6: *Transformer parameter wizard.*

of company and turbine, change of generator and generator configuration and finally entrance of the generator wizard.

6.2.5 Transformer parameters

In the transformer specification box, the user can select any of the transformers appearing in the transformer popup menu. If changing the type of transformer, it is important to note that the transformer terminal voltages should match the HV-voltage setting, the generator stator voltage setting and the converter voltage setting. Any mismatch between the HV voltage settings in the left part of the main user interface and the primary voltage settings for the transformer will produce simulation results representing a steady state over- or under voltage situation. Entering the transformer parameter wizard, the user interface shown in Fig. 6.6 appears. As discussed in chapter 2 the model of the transformer is based on the equivalent circuit in Fig. 2.16 on page 38 and requires parameters such as inductances and resistances. However typical data sheets for transformers implies short circuit conditions and no-load conditions rather than equivalent circuit parameters. Hence the transformer parameter wizard prompt for such data and then subsequently calculates the equivalent circuit parameters from these inputs. Regarding the resistances to be entered it is important to note that all values are physical per phase values measured at the considered tap, i.e. no transformation from one side to the other is needed.

On exit the user can choose to save changes to the existing transformer type by pushing

the "save" button. This action will overwrite existing data for the particular transformer type without any notification. Alternatively the user can choose to push the "Save as" button. By this action, the user will be prompted for a name for the new transformer type whereupon the transformer type is added to the working library. Pushing the "OK" button generates a temporary transformer model (prototype model) which will be used for the next simulation. It must be noted that any action in the main menu forcing the simulator to reload transformer data will overwrite this temporary file with transformer data stored in the working library. Such actions include change of company, change of turbine, change of transformer type and entrance of the transformer parameter wizard. Pushing the "OK" button automatically closes the parameter wizard for the transformer.

6.2.6 Converter parameters

The actual converter wizard appearing when pressing the parameter button in the converter specification box depend on the converter topology chosen in the left part of the main user interface. In the succeeding sections follow a description of the parameter wizards applicable for the topologies treated in this thesis, i.e. the back-to-back two-level converter, the matrix converter and the back-to-back three-level converter. The latter incorporates both the diode-clamped topology and the transistor clamped topology.

Parameters for back-to-back two-level voltage source converter

The parameter wizard for the back-to-back two-level voltage source converter is shown in Fig. 6.7. Besides some general settings such as DC-ink voltage, DC-link voltage control and choice of method for the thermal calculations, the wizard for the back-to-back two-level converter is divided into a grid inverter part (upper left part of the user interface), a generator inverter part (lower left part of the user interface), a grid inductor part (upper right part) and a rotor inductor part (lower right part). The user interface for the two inverters are identical and allows the user to specify switching frequency, modulation method, semiconductor component and/or semiconductor component characteristics along with the thermal characteristics hereof. In the present version of D′rives, only the thermal resistances are available for modification whereas the data determining the transient thermal characteristics are to be read from the data file containing the semiconductor characteristics.

In the right part of the user interface, it is possible to specify a grid side and a rotor side inductor. The thermal modeling of the inductors are based on a simple one-dimension approach using the nominal losses and temperature rice to calculate an equivalent thermal impedance of the inductors.

Besides the transient thermal characteristics of the semiconductors, the user interface illustrated in Fig. 6.7 contains all the information needed for the modeling approach

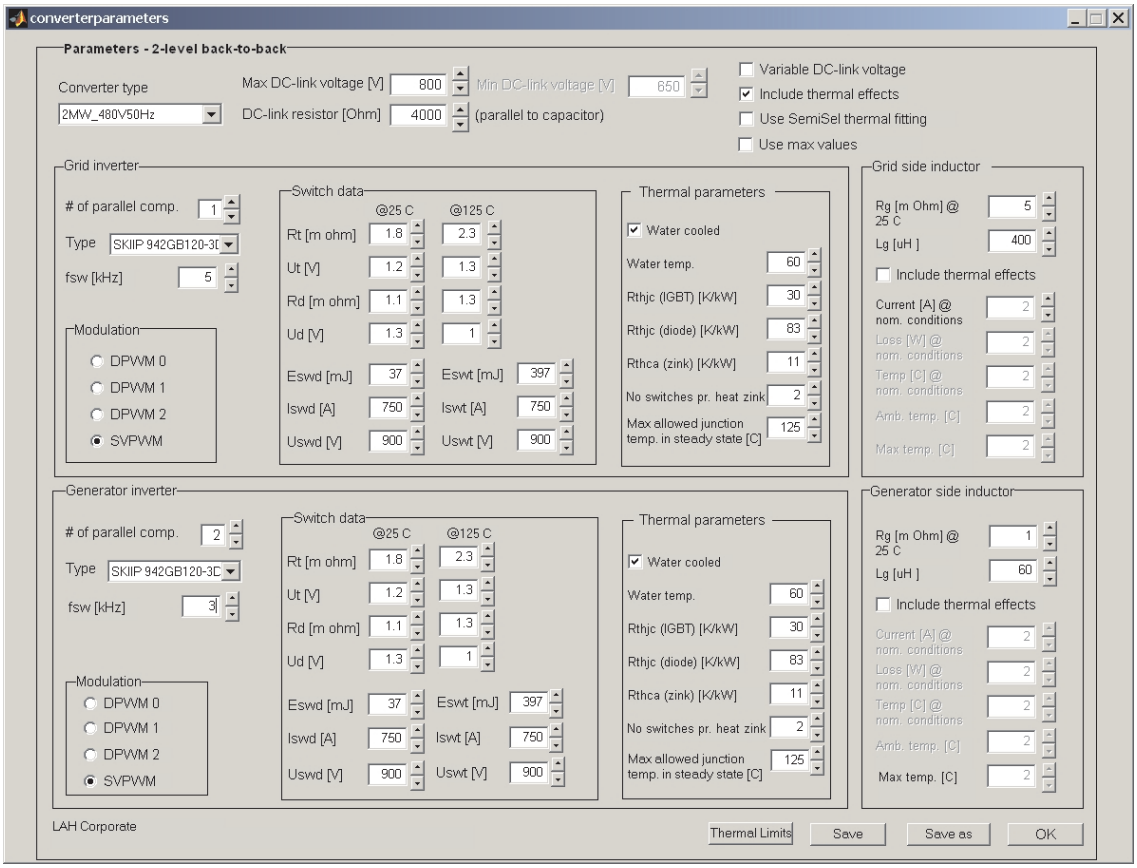

Figure 6.7: *Back-to-back two-level voltage source converter wizard.*

described in chapter 3.

On exit, the user can choose to save modifications in the existing converter identification name by pushing the ”save” button thereby overwriting existing data without further notification. It should be noted that any changes saved by the save-action applies to all turbines in the present working library using the particular converter type. Alternatively the user can create a new converter type by pushing the ”save as” button. This action adds a new two-level converter topology to the list of available converters in the active company directory. By this action, the changes only affects the present turbine while other turbine types are unaffected by the changes. Pushing the ”OK” button closes the back-to-back two-level converter wizard. This action, without previous save- or save-as action, generates a temporary converter design file which will be used in the further simulations until the simulator is forced to reload converter data. The following actions force the simulator to reload converter data: Change of company library, change of turbine, change (or reload) of converter topology, change (or reload) of converter type and opening of the converter wizard. On opening of the converter wizard, the temporary converter data is lost and the data presented in the user interface corresponds to the last-saved data for the particular converter type within the working library.

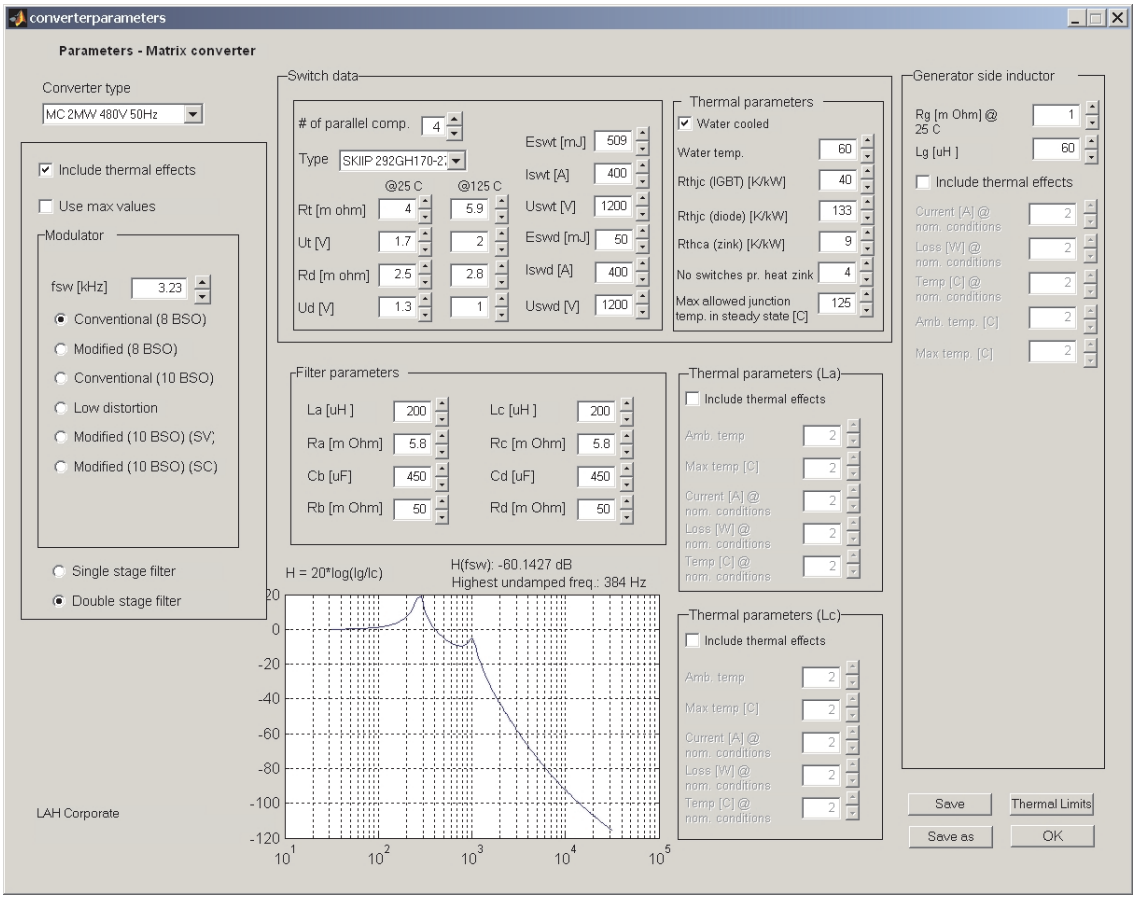

Figure 6.8: *Matrix converter wizard.*

Parameters for matrix converter

Selecting the matrix converter from the list of available converter topologies in the left part of the main user interface, c.f. Fig. 6.1, the parameter wizard in Fig. 6.8 will appear when pushing the parameter button on the converter specification field. The parameter wizard for the matrix converter is divided in four parts. The left concerns main data such as modulation method, switching frequency and input filter type, whereas the upper center part concerns switch characteristics such as number of parallel switches, switch type and switch type characteristics. Regarding the number of parallel components it should be noted that a bi-directional switch realized from a standard H-bridge as discussed in section 4.2.3 on page 93 inherently will imply two parallel components. Further the parameter wizard only allows the user to modify the static thermal characteristics of the semiconductors whereas the parameters determining the transient thermal behaviour are loaded directly from the data file containing the switch data. Changing or reloading the switch type by pushing the switch type-popup menu will overwrite any switch data modified by the user.

The lower center part concerns the input filter. Depending of the chosen number of filter stages the user has to enter filter parameters for one or two LCR circuits including

the resistance of the inductor(s). Changes of the filter parameters are immediately reflected in the transfer function depicted in the plot window and given by eq. (4.115) on page 137. Along with the electrical filter parameters it is possible to enter the thermal characteristics for the inductor(s) in the input filter. The thermal approach is simply based on a steady-state one dimensional approach using nominal losses and nominal temperature rise. The right part of the matrix converter wizard is dedicated for the generator side inductor (if any).

Besides the transient thermal characteristics of the semiconductors, the user interface illustrated in Fig. 6.8 contains all the information needed for the modeling approach described in chapter 4.

As for all the previously discussed parameter wizards the user has three possibilities when leaving the parameter wizard for the matrix converter. Either use the "save" button, the "save as" button or the "OK" button. The "save" action overwrites existing parameters for the particular matrix converter type without any notification whereas the "save as"action adds a new converter type to the list of available matrix converters in the working library. Pushing the "save as" button, the user will be prompted for a new converter type name. The "OK" button closes the matrix converter parameter wizard and saves any changes made to a temporary converter file which are used in simulations as long as the simulator is not forced to reload converter data. Actions forcing the simulator to reload converter data include change/reload of company, change/reload of turbine type, change/reload of converter topology, change/reload of converter type and finally entrance to the converter parameter wizard.

Parameters for back-to-back three-level voltage source converter

The parameter wizard for the three-level converter topology - valid for both the diode-clamped and the transistor-clamped topology - is shown in Fig. 6.9. The left part of the parameter wizard is a static part containing data such as DC-link-voltage, DC-link voltage control, choice of thermal calculation method and type of three-level converter topology (diode-clamped or transistor clamped). The fields to the right of the static part contain inverter parameters. However, due to the high number of parameters involved (compared to the previously discussed converter topologies) the parameter wizard for the back-to-back three-level converter is split into two parts where only one part is visible at the time. One part concerns the grid side inverter and one concerns the generator side inverter. To change between viewing grid inverter parameters and generator inverter parameters, the two upper radiobuttons in the main part is used.
The structure for the grid inverter wizard and the generator inverter wizard is completely identical and contains a section describing characteristics for the upper (and lower) switches, a section for the center switches and finally a part containing data for the clamping diodes. It should be noted that in the present version of D′rives only the static thermal characteristics can be modified from the user interface whereas the

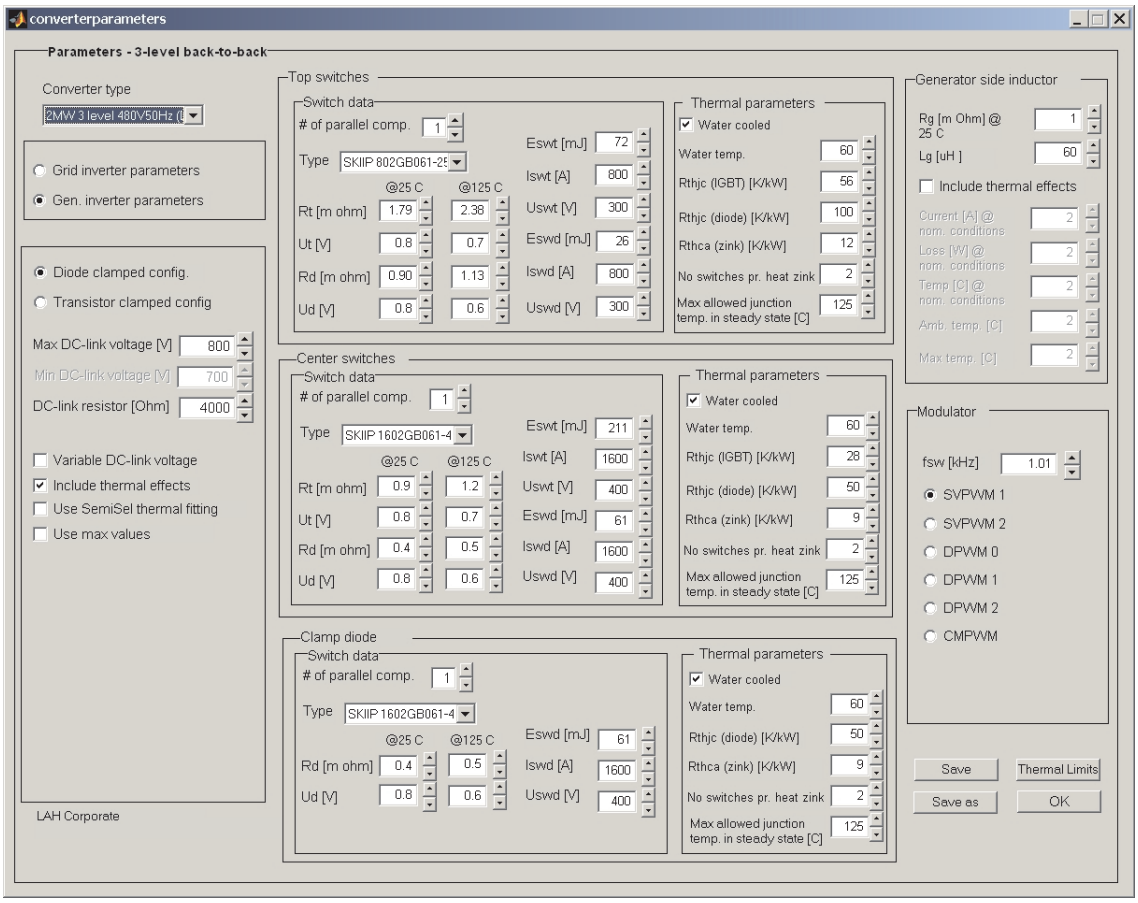

Figure 6.9: *Back-to-back three-level voltage source converter wizard.*

data determining the transient thermal behaviour are to be modified in the data file containing the switch data.

Tabulating between the grid inverter page and the generator inverter page saves data from the closing page into a temporary file. On re-entrance these data are reloaded into the user interface. On exit the user can choose to save changes to the existing back-to-back three-level converter type by pushing the "save" button. This action will overwrite existing data for the particular converter type, both data from the grid side inverter and the generator side inverter. Data are overwritten without any notification. Alternatively the user can choose to push the "Save as" button. By this action, the user will be prompted for a name for the new back-to-back three-level converter whereupon the converter type is added to the working library. Pushing the "OK" button generates a temporary converter type (prototype model) which will be used for the next simulations. It must be noted that any action in the main menu forcing the simulator to reload converter data will overwrite this temporary file with converter data store in the working library. Such actions include change of company, change of turbine, change of converter topology/type and entrance of the converter parameter wizard. Pushing the "OK" button automatically closes the parameter wizard for the back-to-back three-level

converter.

6.3 Data representation

Returning to the main page, c.f. Fig. 6.1, the right part is dedicated to presentation of simulation results and contains two identical plot areas. In each plot area, the user can plot almost any internal simulation variables against another, simply by use of the popup menus below the plot windows. Checking the check box "Freeze" allows the user to plot several variables in the same plot. However, a change of the x-axis variable will reset the current plot. Data can be exported to external figures by use of the buttons "Plot" and "Plot new fig.". Using the "Plot" button plots the current content of the plot window in the last activated external figure (if any). If no external figure is present, a new external figure is created and data is exported to this figure. The "Plot new fig." creates a new external figure and exports data into this figure. The "Clear" button simply deletes the content of the current plot window.

6.4 Summary

This chapter has provided an introduction to the wind turbine simulation tool *D′rives* or at least to that part of the tool concerning the models described in this thesis. In summary, *D′rives* is a package with a graphical interface linking all the modeling approaches described throughout this report in a user-friendly and well-arranged manner. The simulation tool provides easy access for changing the topology configuration and change of main characteristics such as power-speed curve, star-delta connection and active/reactive power generation. Further, each of the main components, i.e. blades, gear box, generator, converter and transformer have a separate page allowing change of all the parameters involved in the modeling approaches described in chapter 2 - chapter5. The representation of simulation results is very flexible as most internal simulation variables can be plotted against each other. As a final remark, it should be noted that due to the explicit analytical expressions for component currents and component losses, the simulation speed of the *D′rives* program is extremely high. For instance, a simulation of peak temperatures of the semiconductors in a converter design calculated for the entire power/speed operating range has been reduced from a day-long simulation task into a simulation time of about 2 seconds.

References

[1] P. Bhalerao and Eugen Stumpf. Selection, Power Loss Calculation and Temperature Rise Analysis. *Bodo′s Power Systems*, pages pp. 24–27, November 2006.

[2] http://www.mitsubishichips.com. Homepage of Mitsubishi. 2006.

[3] http://www.semikron.de. Homepage of Semikron. 2006.

[4] Peter R. W. Martin, Ulrich Nicolai, Jürgen Petzoldt, and Josef Lutz. *Semikron innovation+servive - Application manual power modules.* ISLE, ISBN : 3-932633-46-6, April 2000.

Part III

Comparison and conclusion

Chapter 7

Topology comparison

AS discussed previously, the result of a comparison between different converter topologies may vary depending on the specific application. To handle this uncertainty, the main components of the wind turbine were modeled throughout chapter 2. However, even for a specific application such as the wind turbine application equipped with a doubly-fed induction generator, the result may vary depending on the choice of the surrounding components, e.g. generator voltage level, gear ratio, choice of semiconductor component etc. Hence this chapter will not end up by recommending a specific converter topology but rather demonstrate the functionality of the program D′rives linking all the modeling approaches described in this thesis.

In this chapter, the four converter topologies discussed until now will be designed for a 2 MW wind turbine and compared in a wind turbine application. The chapter begins with a specification example for a 2 MW turbine, defining the main characteristics of the interfacing components. Based on this specification, an initial design of the considered converters are carried out using the design guidelines presented throughout the thesis. Each of the designs are validated by calculating the turbine power limits set by the actual converter design and the limiting components are identified within the considered speed range. Finally, the four converters are compared in terms of power losses, system efficiency, power capability, component count and switch utilization.

7.1 Turbine specification - an example

For the present design example, the surrounding turbine components, i.e. blades, gear box, generator and transformer will be selected without entering a discussion on the actual choices. Further, although the reader - based on the content of chapter 2 - could expect a detailed presentation of the loss models used in the considered design example, such a presentation is omitted. The reason for this omission is, that most of the specific material related to the modeling of component losses are to be considered as confidential information. Accordingly, the loss modeling which could be presented in this chapter would have to be normalized and hence it would not contain further details than already presented in chapter 2. Nevertheless, the calculations of system power capability, energy

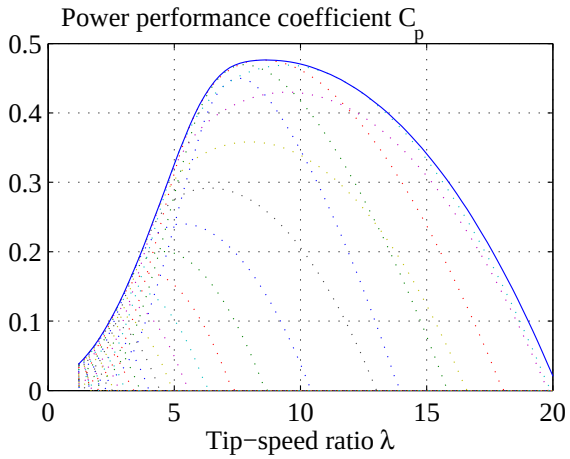

Figure 7.1: *Power performance coefficient C_p for the chosen blade as a function of the tip speed ratio λ.*

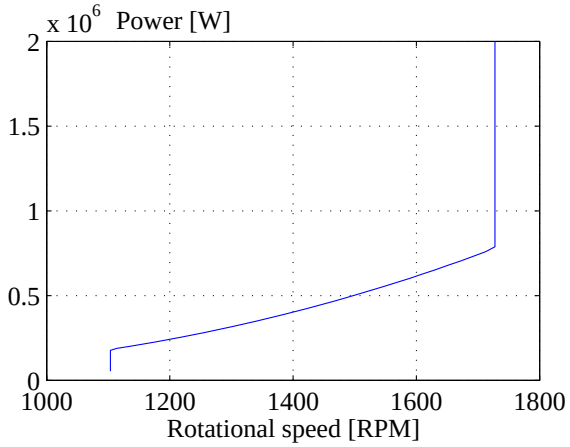

Figure 7.2: *Power speed curve for the turbine designs.*

production etc. include the power losses generated by the individual components.

7.1.1 Turbine blades

In the present example, the turbine is equipped with three 39m long pitch controlled blades corresponding to those used in the Vestas V80 2 MW turbine. Fig. 7.1 shows the power performance coefficient C_p versus tip speed ratio λ, plotted for different pitch angles. The solid line shows the maximum achievable blade efficiency which is to be used as long as the turbine operates in partial load. In full load operation, the blades are pitched out of the wind corresponding to a C_p curve shown by the dotted lines.

7.1.2 Gear ratio and speed operating range

As discussed in chapter 1 and chapter 2, the most efficient energy capture for a certain blade design is obtained by keeping a constant tip-speed ratio, c.f. Fig. 7.1. However, in a practical design several issues are constraining the allowable speed range and thereby the range where the turbine can achieve maximum aerodynamic efficiency. These constrains are given by issues such as:

- Emitted noise.
- Tear and wear on the blades edges due to hail and other airborne particles.
- Tear and wear on turbine structure.

Hence in a turbine design a trade off has to be made. In the present example the maximum steady state tip speed is limited to 72 m/s whereas the turbine design should allow transient tip speeds of 80 m/s due to turbulence. For a specific blade layout, the gear box ratio combined with the restrictions concerning maximum tip speed actually

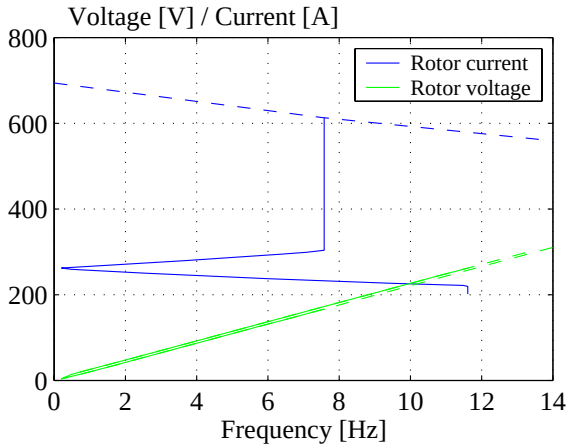

Figure 7.3: *Rotor voltage and rotor current when following the power-speed curve in Fig. 7.2.*

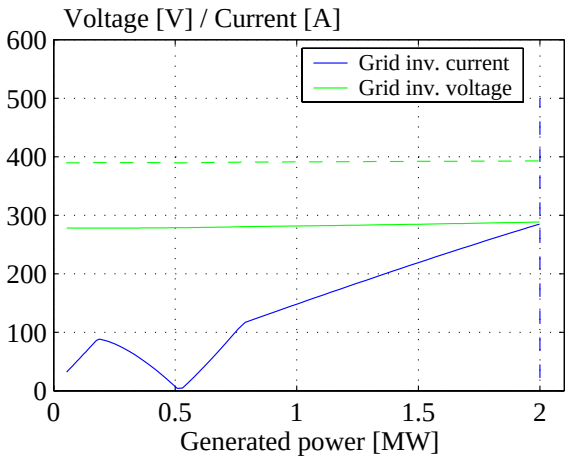

Figure 7.4: *Grid inverter voltage and grid inverter current when following the power-speed curve in Fig. 7.2.*

defines the speed range in which the generator of the turbine will have to operate. For the present example, a gear box ratio of 1:100 is chosen by which the nominal speed for the generator becomes 1719 RPM. Using the chosen maximum steady state tip speed, the selected gear ratio and the chosen blade profile, the turbine power-speed curve can be obtained. Fig. 7.2 shows the power speed curve for which the turbine in this example should be designed.

7.1.3 Generator interface

In section 2.4 a quite detailed model of the generator was derived. For the initial converter design however, the only necessary characteristics are the nominal stator voltage V_s the generator winding ratio N_{gen} and the pole number N_p which in combination defines the voltage, current and frequency for which the converters are to be designed. The generator used in this design example is a 2MW 4 pole doubly-fed induction generator from ABB with a winding ratio[1] of 2.6 and a nominal stator phase voltage of 400 V. Combining these generator characteristics with the power-speed curve in Fig. 7.2, the rotor current and rotor voltage can be found as a function of the rotor frequency. Fig. 7.3 shows the generator rotor current (-) and generator rotor voltage (-) as a function of the applied frequency, for which the considered converters will have to be designed. The dashed line in Fig. 7.3 represent an expectable transient overload current which may occur due to turbulence - a current for which the converters should be designed.

[1]The true winding ratio is actually 1.5 but since the generator is operated in a Δ-Y connection the winding ratio has been transformed to an equivalent Y-Y connection

7.1.4 Transformer interface

The transformer used in the present design example is a three-winding transformer for connection on an 11 kV supply grid. The secondary winding phase voltage is 400 V in order to match the chosen generator. For the back-to-back two-level converter and the back-to-back three-level converter, the tertiary winding voltage (phase) is 277 V whereas for the matrix converter, the tertiary winding voltage (phase) is 380 V. The latter voltage choice is due to the reduced voltage gain inherently connected with the use of the matrix converter. Fig. 7.4 shows the grid voltage and grid current for which the converters are to be designed. The solid green line represents the grid voltage for the back-to-back two-level converter and the back-to-back three-level converter while the dashed green line represents the grid voltage for the matrix converter. The blue curve shows the corresponding grid current for which the grid side inverters in the back-to-back two-level converter and the back-to-back three-level converter must be designed. The dashed line in Fig. 7.4 represent an expectable transient overload current which may occur due to turbulence - a current for which the grid side inverters should be designed.

7.2 Design of the back-to-back two-level converter

The design of the back-to-back two-level voltage source converter follows the rough design guide line provided in section 3.5 on page 74. Having the rough converter design the more comprehensive modeling approach along with the chosen operating conditions will be used to determine the present design margin and to investigate to what extent the choice of modulation method actually influences the design margin. Based on this investigation, this section is concluded by a finalized pre-design of the back-two-back two-level converter which will be used in the comparison with the other converter candidates.

TABLE I: *Converter ratings.*

	Grid inverter	Generator inverter
Nom. current [A]	314	593
Max. current [A]	518[a]	673[b]
Nom. frequency [Hz]	50	7.5
DC-link voltage [V]	> 697	> 695
Inductance [mH]	< 3.2[c]	-

[a]Current calculated at full power and 27.4% slip.
[b]Current calculated at full power and 0.1% slip.
[c]Provided a DC-link voltage of 800V.

TABLE II: *Switching frequencies in [kHz].*

	Subopt.	Sft	Aslft	Asrft
Grid inverter	5	6.4	5.75	5.75
Generator inverter	3	5.5	5.34	5.34

7.2.1 Component ratings

To be able to select suitable switches for the back-to-back two-level voltage source converter, the necessary current and voltage ratings have to be determined. Following the rough design approach given in section 3.5 on page 74 along with the specification of the interfacing component characteristics, the necessary current and voltage ratings can be determined. Table I summarizes the calculated component ratings.

7.2.2 Selection of switching frequencies

When selecting a switching frequency for the two inverters in the back-to-back two-level converter, several practical issues should be considered. For instance control band width, sampling of signals and emission of switching harmonics are issues to be concerned with when selecting switching frequencies. Further, for comparison purposes a focus area of this thesis has been to be able to select switching frequencies making different converter designs and even different converter topologies comparable in terms of harmonic distortion. Only the latter aspect will be considered in this design example as the purpose is to demonstrate the evaluation tool rather than ending up with a functional design taking all practical issues into consideration.

In the present approach, all the modulation methods for all the converter topologies have been evaluated with regard to the associated harmonic voltage distortion and to obtain comparable performance, a switching frequency correction factor $k_{sw,v}$ has been introduced. Hence choosing switching frequency for one specific converter design actually defines the switching frequency for all the other designs. In the design example for the back-to-back two-level voltage source converter using the sub-optimal modulation method in both inverters, a switching frequency of 5 kHz is to be used in the grid side inverter whereas a switching frequency of 3 kHz is to be used in the generator side inverter. Using eq. (3.76) and eq. (3.77) on page 82, the switching frequencies for the three discontinuous modulation methods can be found. Table II shows the switching frequencies to be used for the different modulation methods in order to obtain the same harmonic distortion as for the suboptimal modulation method.

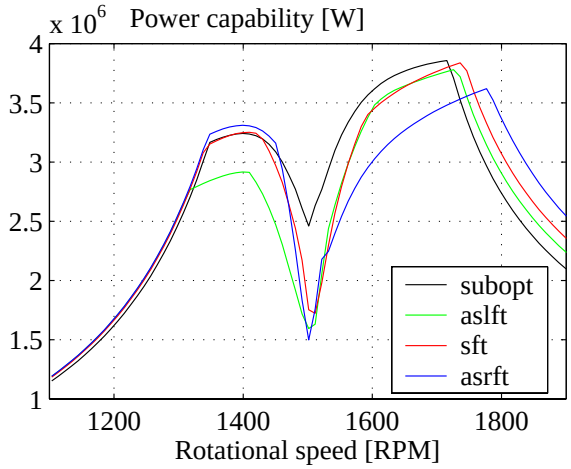

Figure 7.5: *Power capability of the system when considering the limits determined by the converter design.*

7.2.3 Power capability

As discussed previously, the doubly-fed system is a quite unusual system when considering the loading conditions of the converter. For instance, operation near synchronous speed puts a quite heavy load - both in terms of frequency and current level - on the rotor side inverter while the grid side inverter is nearly unloaded. On the other hand, increasing the speed above synchronous speed relieves the stress level on the rotor side inverter while increasing the load on the grid side inverter. For a certain converter design these properties clearly will changes the overall turbine power capability depending on the operating conditions and choice of modulation method. Fig. 7.5 shows the turbine power capability when considering the limits determined by the present converter design. Especially near synchronous speed the discontinuous modulation methods "fail" due to the relatively low fundamental frequency on the rotor inverter combined with the fact that these modulation methods clamps a phase-leg for one-sixth of the fundamental period. Besides operation near synchronous speed, the present converter designs seem to provide a sufficient design margin.

Having the system power limits set out by the converter design, another important investigation concerns the origin of the power limits - an origin which is not directly readable from Fig. 7.5. In fact, a proper design of the back-to-back two-level converter should assure that not only one component defines the power limit in the entire operating range. Fig. 7.6 to Fig. 7.9 shows the limiting component when applying the four considered modulation methods. As expected, the rotor side inverter components are the limiting components when operating around synchronous speed whereas for an increasing slip (sub- and super synchronous speed) the grid inverter becomes the limiting component. Whether, the diode or the IGBT turns out to be the limiting factor depend on the power factor, the power flow direction and the thermal characteristics of the diode and IGBT respectively.

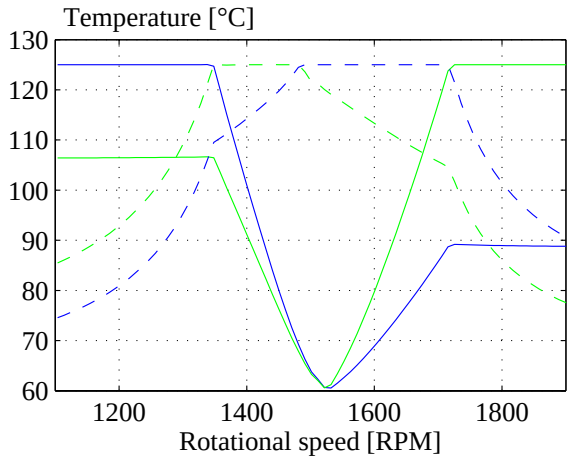

Figure 7.6: *Limiting components when using the SVPWM modulation method. Grid diode: (-), Grid IGBT: (-), Gen. diode: (- -) and Gen. IGBT: (- -).*

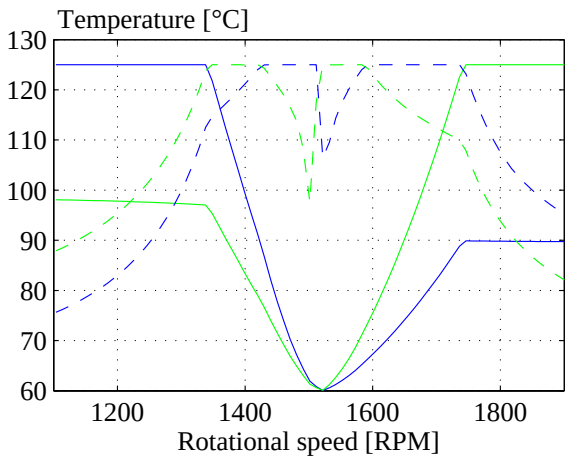

Figure 7.7: *Limiting components when using the DPWM1 modulation method. Grid diode: (-), Grid IGBT: (-), Gen. diode: (- -) and Gen. IGBT: (- -).*

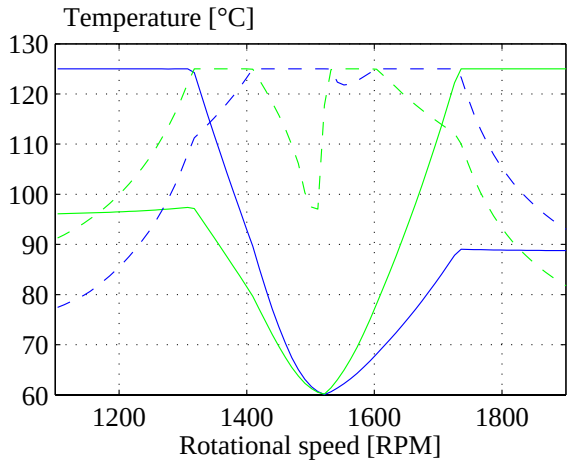

Figure 7.8: *Limiting components when using the DPWM0 modulation method. Grid diode: (-), Grid IGBT: (-), Gen. diode: (- -) and Gen. IGBT: (- -).*

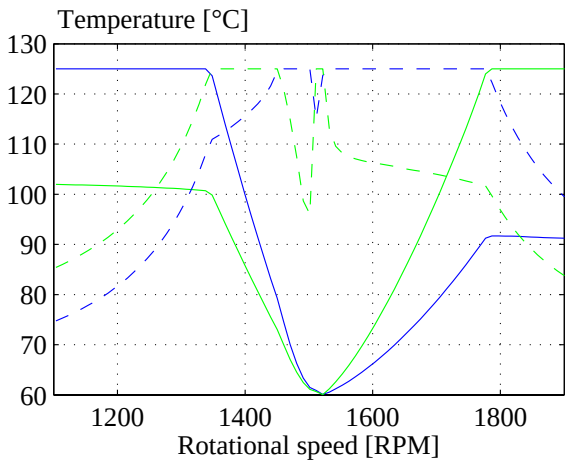

Figure 7.9: *Limiting components when using the DPWM2 modulation method. Grid diode: (-), Grid IGBT: (-), Gen. diode: (- -) and Gen. IGBT: (- -).*

7.2.4 Power losses

Finally, besides the power capability set out by the converter design, the absolute power losses are an important aspect when choosing the modulation method. Fig. 7.10 shows the converter losses as a function of the wind speed when the turbine follows the power speed curve given by Fig. 7.2. In the calculation of the converter power losses in Fig. 7.10 it is provided that both the grid side inverter and the rotor side inverter are using the same modulation methods. To achieve a more detailed "picture" of the losses and to have a better foundation for the selection of modulation methods, Fig. 7.11 and

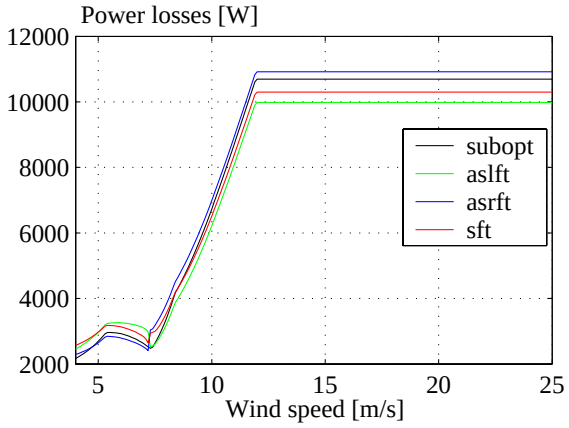

Figure 7.10: *Total converter power losses as a function of the wind speed for the considered modulation methods.*

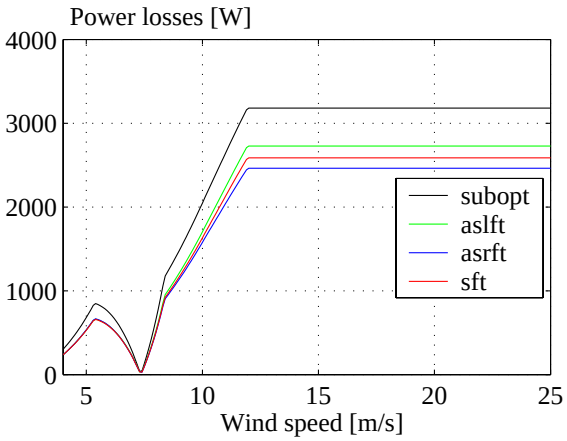

Figure 7.11: *Grid inverter power losses (semiconductors only) as a function of the wind speed for the considered modulation methods.*

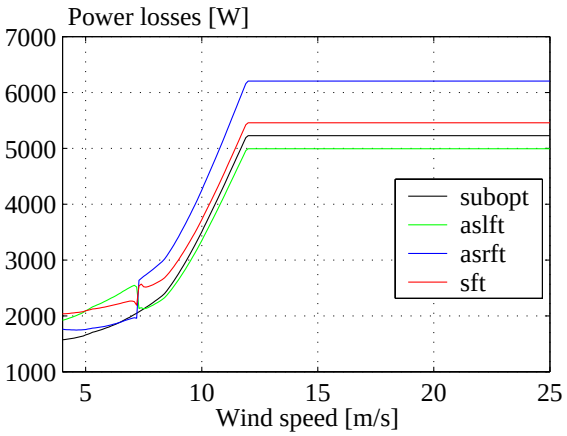

Figure 7.12: *Generator inverter power losses (semiconductors only) as a function of the wind speed for the considered modulation methods.*

Fig. 7.12 shows the grid inverter losses and rotor inverter losses associated with the use of the considered modulation methods. Combining the information on converter power capability read out from Fig. 7.5 with the inverter losses in Fig. 7.12 the rotor inverter in the present design example should make use of the sub-optimal modulation method due to quite good power loss properties and the good thermal distribution properties associated with this modulation method. On the other hand, since the grid inverter operates at 50 Hz the selection of modulation method can be made based on the calculated inverter losses without looking at the turbine power capability. Hence, according to Fig 7.11 the grid inverter in the back-to-back two-level voltage source inverter should make use of the asymmetrical shifted right flat top modulation method.

TABLE III: *Pre-design of the two-level converter.*

	Grid inverter	Generator inverter
Switch type	SkiiP 942GB120	SkiiP 942GB120
# of parallel modules	1	2
Inductor [μH]	400	60
Modulation method	Asrft	Subopt
Switching frequency [kHz]	5.75	3
DC-link voltage [V]	800	800

7.2.5 Selection of converter components

Based on the loss evaluation and the evaluation of power capability, the main characteristics of the pre-designed back-to-back two-level converter are listed in Table III and will be used for the turbine comparison presented in section 7.5.

7.3 Design of the matrix converter

The pre-design of the matrix converter generally concerns the selection of suitable switches matching the loading conditions discussed in section 7.1 and selection of a switching frequency matching the harmonic distortion obtained by the two-level converter. Further, since the grid side filter is a crucial part of the matrix converter, a proposal for a filter design is presented. Having the pre-designs, the power capability of the designed matrix converters are evaluated and the power losses associated by using the matrix converter in the wind turbine example is calculated. Based on the power capability and converter power losses, a design for the matrix converter is chosen for the further comparison.

TABLE IV: *Converter ratings.*

	Matrix converter
Nom. current (generator) [A]	593
Max. current (generator) [A]	673[a]
Nom. frequency (grid/generator) [Hz]	50 / 7.5
Grid voltage [V]	380
Grid side PF[b]	1

[a] Current calculated at full power and 0.1% slip.

[b] The power factor reference is evaluated at the input terminals of the matrix converter switches and hence the reactive power consumed by the input filter will have to be compensated by the generator reactive power control.

TABLE V: *Switching frequencies in [kHz].*

Con 8 BSO	Mod 8 BSO	Con 10 BSO	Ld	Mod 8 BSO (SV)	Mod 10 BSO (SC)
3.23	1.97	1.70	2.46	2.04	1.74

7.3.1 Component ratings

To be able to select suitable switches for the matrix converter, the necessary current and voltage ratings are to be determined. Following the rough design approach given in section 4.5.1 along with the interfacing component characteristics the necessary current and voltage ratings can be determined. Table IV summarizes the roughly performed design.

7.3.2 Selection of switching frequency

As discussed previously, a crucial aspect of the converter comparison is the selection of switching frequencies assuring comparable harmonic distortion from the considered converter topologies and modulation methods. In fact, determining the switching frequency for one particular converter design actually determines the switching frequencies to be used for the remaining converters and modulation strategies. For the matrix converter, eq. (4.118) - eq. (4.123) on page 139, can be used to scale the switching frequency for the matrix converter modulation methods in order to obtain the same harmonic distortion as obtained by the two-level converter using the sub-optimal modulation method. Applying eq. (4.118) - eq. (4.123) the switching frequencies for the six considered modulation schemes applicable for the matrix converter can be found. Table V shows the switching frequencies to be used for the different modulation methods in order to obtain the same harmonic distortion as for the suboptimal modulation method applicable for the two-level converter.

7.3.3 Design of grid side filters

The design procedure for the grid filter, applicable for the matrix converter were discussed in section 4.5.2. All filters in this section have been designed to have 60dB attenuation at the switching frequencies and no positive amplification at frequencies higher than one tenth of the switching frequency. Hence due to the selection of different switching frequencies for the different modulation schemes, different filter characteristics are necessary. Table VI shows the filter parameters used in order to realize the filters for the different modulation methods. Fig. 7.13 shows the attenuation characteristics of the designed grid side filters for use with the matrix converter.

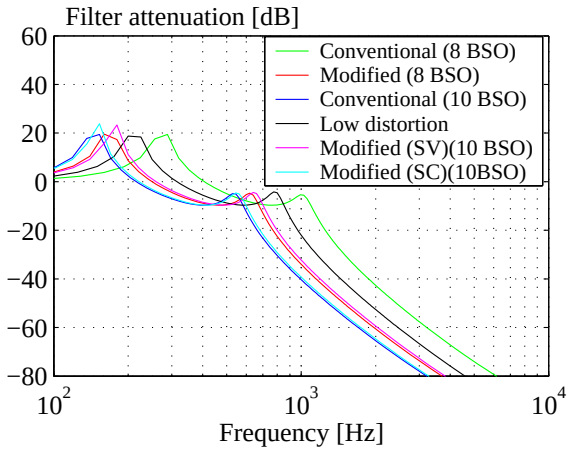

Figure 7.13: *Characteristics of the filters for the matrix converter designs.*

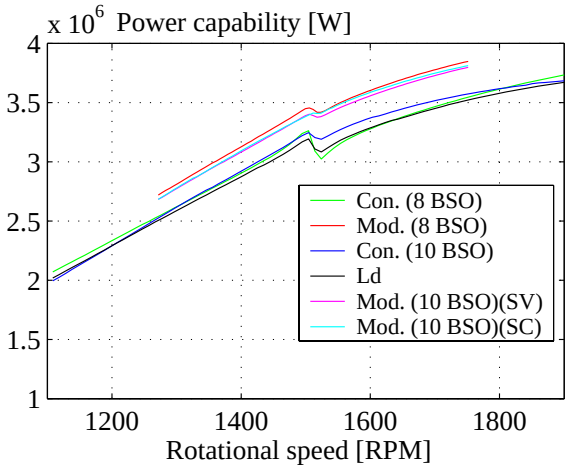

Figure 7.14: *Power capability of the system when considering the limits determined by the matrix converter design.*

7.3.4 Power capability

When evaluating the converter capability of the wind turbine equipped with the matrix converter, it is important to note that all the modified modulation schemes are not able to operate in the considered speed range due to the limited voltage gain of 0.5. Fig. 7.14 shows the turbine power capability determined by the matrix converter layout. An interesting, but at the same time expectable property of the matrix converter is the imperviousity against the low frequency operation at the generator side. Actually, the slight decrease in power capability near synchronous speed is merely due to the change in generator power factor than due to the low frequency operation.

Considering the limiting component of the matrix converter it is reasonable to expect that the limiting component remains the same in the entire speed range. In fact it turns out that for the present switch selection, the diodes are the limiting component in the entire operating speed range. Fig. 7.15 - Fig. 7.20 show the temperature of the diodes (-) and IGBT′s (-) versus generator speed when operating the turbine at the power

TABLE VI: *Grid filter components.*

	L_a [μH]	L_c [μH]	C_b [μF]	C_d [μF]	R_b [mΩ]	R_d [mΩ]
Con. (8 BSO)	200	200	450	450	50	50
Mod. (8 BSO)	350	350	680	680	50	50
Con. (10 BSO)	400	400	800	800	50	50
Ld. (8BSO)	300	300	500	500	50	50
Mod. (10 BSO)(SV)	350	350	630	630	50	50
Mod. (10 BSO)(SC)	400	400	760	760	50	50

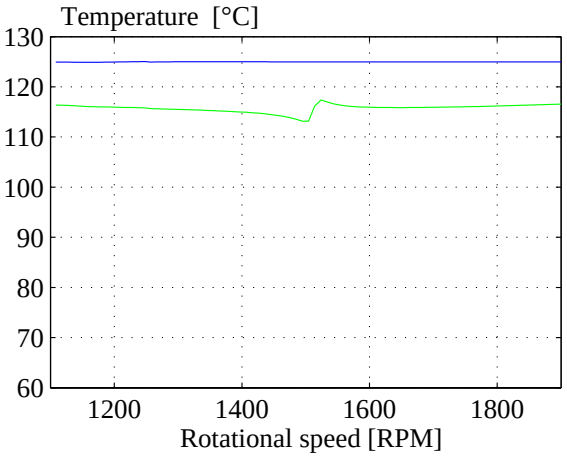

Figure 7.15: *Limiting components when using the conventional 8 BSO modulation method. Diode: (-), IGBT: (-).*

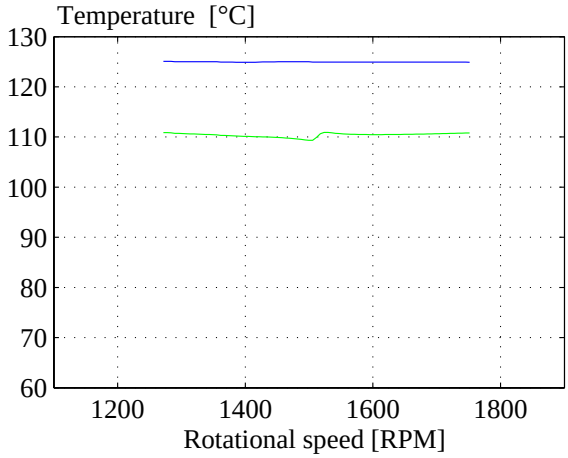

Figure 7.16: *Limiting components when using the modified 8 BSO modulation method. Diode: (-), IGBT: (-).*

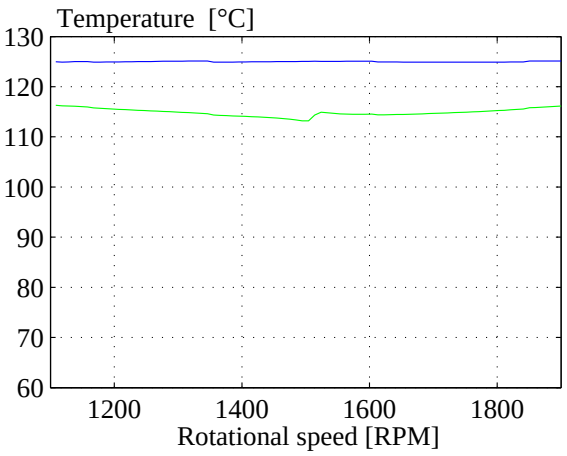

Figure 7.17: *Limiting components when using the conventional 10 BSO modulation method. Diode: (-), IGBT: (-).*

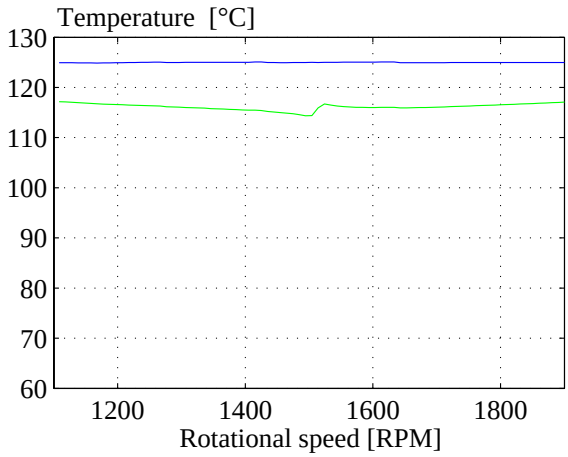

Figure 7.18: *Limiting components when using the Low distortion modulation method. Diode: (-), IGBT: (-).*

limits set out by the matrix converter design.

7.3.5 Power losses

Besides the limited speed operating range for all the modified modulation methods - a property that actually may disqualify these modulation schemes for the present design example - the evaluation of the system power capability did not provide convincing arguments for selection of one particular modulation method. Hence the power losses of the matrix converter will have to be the major criteria for selecting a modulation method for the further study. To evaluate the power losses generated by the semiconductors in the matrix converter, the analytical expressions derived in section 4.4 can be used. Fig.

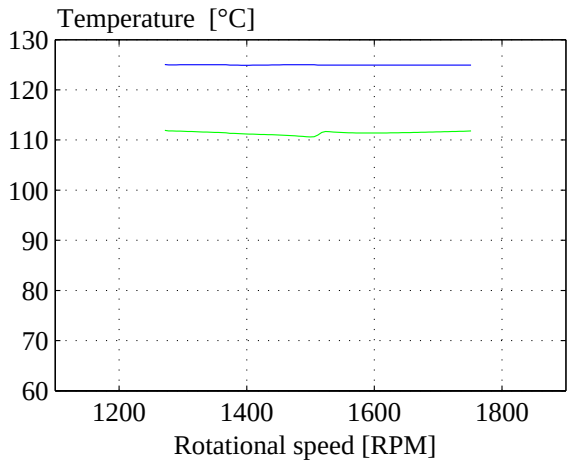

Figure 7.19: *Limiting components when using the modified 10 BSO modulation method (SV). Diode: (-), IGBT: (-).*

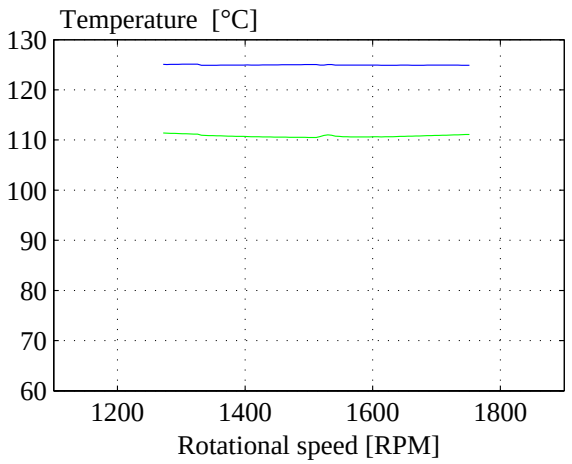

Figure 7.20: *Limiting components when using the modified 10 BSO modulation method (SC). Diode: (-), IGBT: (-).*

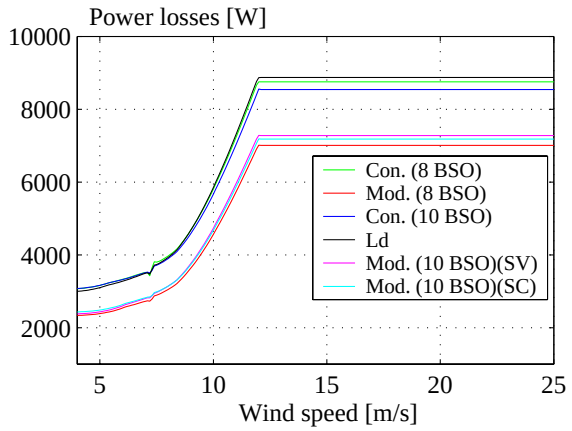

Figure 7.21: *Total Semiconductor power losses as a function of the wind speed for the considered modulation methods.*

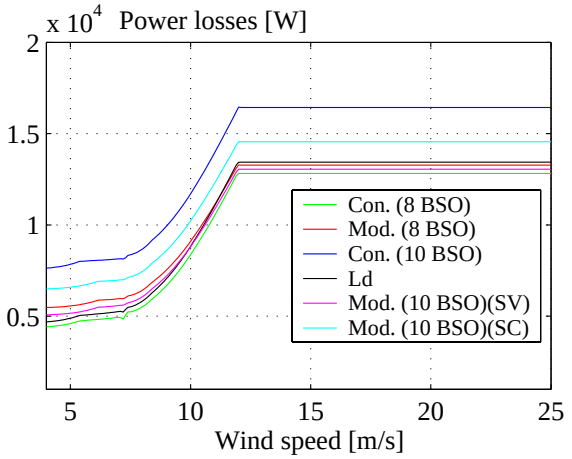

Figure 7.22: *Total converter power losses as a function of the wind speed for the considered modulation methods.*

7.21 shows the power losses generated by the semiconductor components of the matrix converter. As expected, the modified modulation methods all have a significantly reduced power loss level due to the lower switching losses. However, inclusion of the power losses associated with the filters designed for the different modulation methods actually changes the picture significantly. Fig. 7.22 shows the losses of the entire converter, including power losses of the filter components and based on this loss evaluation the conventionally 8 BSO modulation method is selected for the further study.

7.3.6 Selection of converter components

Based on the loss evaluation, the main characteristics of the pre-designed matrix converter are listed in Table VII and will be used for the turbine comparison presented in section 7.5.

7.4 Design of the back-to-back three-level voltage source converter

The pre-design of the back-to-back three-level voltage source converter actually involves design of two three-level converters, namely a design for the diode-clamped topology and a design for the transistor clamped topology.

7.4.1 Component ratings

To be able to select suitable switches for the back-to-back three-level voltage source converters, the necessary current and voltage ratings have to be determined. Following the rough design approach given in section 5.5 on page 232 along with interfacing component characteristics, the necessary current and voltage ratings can be determined. Table VIII summarizes the outcome from roughly performed pre-design.

7.4.2 Selection of switching frequencies

Both the transistor clamped three-level converter and the diode clamped three-level converter show equal harmonic properties when evaluated according to the procedure described in section 5.3.6 and hence both the topologies should operate at the same switching frequency. Using eq. (5.214) - eq. (5.218) on page 241, the switching frequencies for the six considered modulation methods can be found. Table IX summarizes the switching frequencies to be used for the different modulation methods in order to obtain

TABLE VII: *Pre-design of the matrix converter.*

Switch type[a]	SkiiP 292GH170
# of parallel modules	2[b]
Modulation method	Con. (8 BSO)
Grid filter[c]	2-stage,
Switching frequency [kHz]	3.23
Grid phase voltage [V]	380

[a]Note that this component is obsolete.
[b]This actually corresponds to 4 parallel bi-directional switches.
[c]Specific component values, can be found in Table VI on page 281

TABLE VIII: *Converter semiconductor components.*

	Grid inverter	Generator inverter
Nom. current [A]	314	593
Max. current [A]	518[a]	673[b]
Nom. frequency [Hz]	50	7.5
DC-link voltage [V]	> 697	> 695
Inductance [mH]	< 3.2[c]	-

[a]Current calculated at full power and 27.4% slip.
[b]Current calculated at full power and 0.1% slip.
[c]Provided a DC-link voltage of 800V.

the same harmonic distortion as for the suboptimal modulation method usable for the two-level converter. Due to the limited voltage gain of the modulation method with common mode voltage elimination, this scheme is not applicable for the grid inverter in the present design example.

TABLE IX: *Switching frequencies in [kHz].*

	SVPWM1	SVPWM2	DPWM0	DPWM1	DPWM2	CMPWM
Grid inv.	2.09	2.09	3.19	3.15	3.19	-
Gen. inv.	1.01	1.05	2.14	2.18	2.14	2.75

7.4.3 Power capability

To determine whether the present three-level converter designs actually suits the present turbine application, the system power capability set out by the converter design is an important evaluation criteria. Fig. 7.23 shows the turbine power capability when considering the limits determined by the diode clamped converter design. As appears from Fig. 7.23, the three-level diode clamped topology is highly affected by the low frequency operation - even more affected than the two-level topology. Especially, the discontinuous modulation schemes, i.e. DPWM0, DPWM1 and DPWM2 appears to "fail" in the low frequency operating range. Considering the transistor clamped topology, the power capability of the present design is shown in Fig. 7.24. From Fig. 7.24 it appears that transistor clamped topology suffers from the same low frequency properties as the diode-clamped counter part. If found necessary, the low frequency properties of the two three-level converter designs could be improved by identifying the limiting components and then performing a redesign of the particular components. Further identifying the limiting components may give a hint about the "quality" of the design. In fact, for the present designs not only one component should determine the system power capability

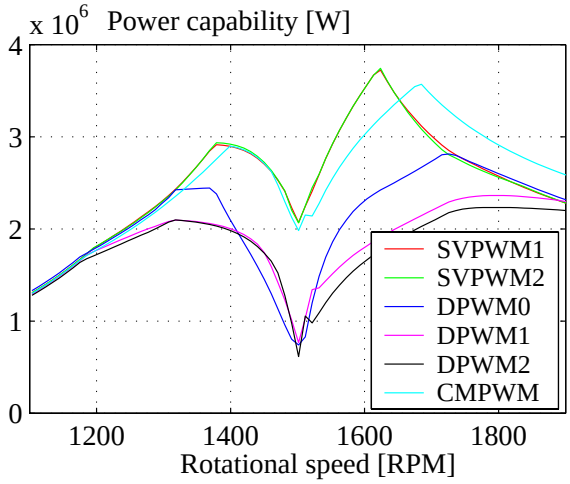

Figure 7.23: *Power capability of the system when considering the limits determined by the diode clamped converter design.*

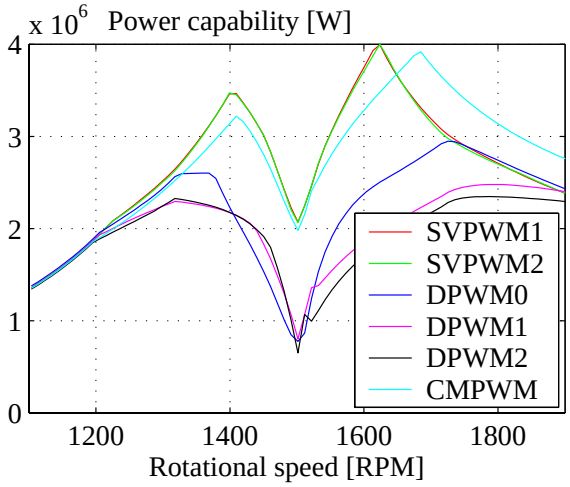

Figure 7.24: *Power capability of the system when considering the limits determined by the transistor clamped converter design.*

in the entire operating range. Fig. 7.25 to Fig. 7.30 show the limiting component when applying the six considered modulation methods in the diode clamped configuration. Due to the limited available space in Fig. 7.25 to Fig. 7.30 no legend is included inside the figures. However, for all the six figures, the below listed color codes apply:

— Grid inverter top IGBT. - - Gen. inverter top IGBT.

— Grid inverter top diode. - - Gen. inverter top diode.

— Grid inverter center IGBT. - - Gen. inverter center IGBT.

— Grid inverter center diode. - - Gen. inverter center diode.

— Grid inverter clamp diode. - - Gen. inverter clamp diode.

Considering the limiting components of the present diode-clamped design, shown in Fig. 7.25 to Fig. 7.30, it appears that the continuous modulation schemes, i.e. SVPWM1 and SVPWM2, have a quite good load distribution in the considered operating range. For instance, at sub-synchronous speed, the center diode (-) and almost the top diode (-) of the grid side inverter are the limiting component. From about 1200 RPM the top transistor of the generator inverter takes the position as the limiting component (- -). Subsequently follows the center transistor (- -), the clamping diode (- -) and then again the center transistor. Finally, the top diode of the generator inverter becomes the limiting component (- -). For the discontinuous modulation schemes, the situation is quite different. Actually, for the present designs the discontinuous modulation methods puts a quite high stress on the top diodes and top IGBT in the generator inverter

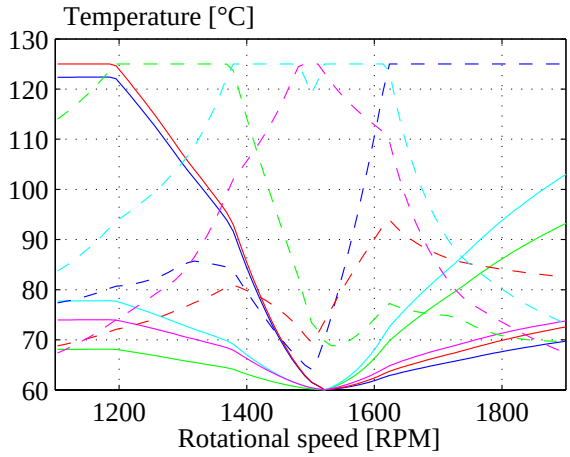

Figure 7.25: *Limiting components when using the SVPWM1 modulation method in the diode clamped configuration.*

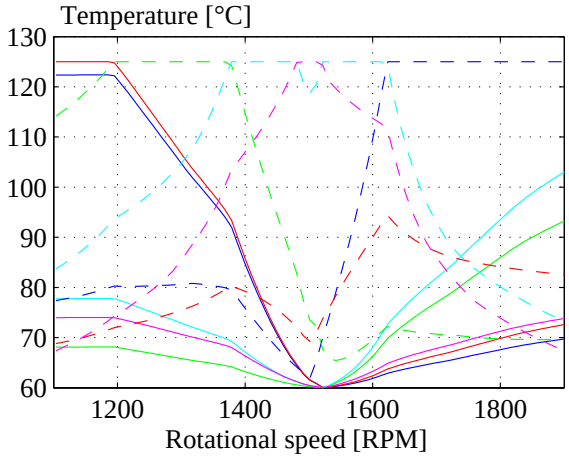

Figure 7.26: *Limiting components when using the SVPWM2 modulation method in the diode clamped configuration.*

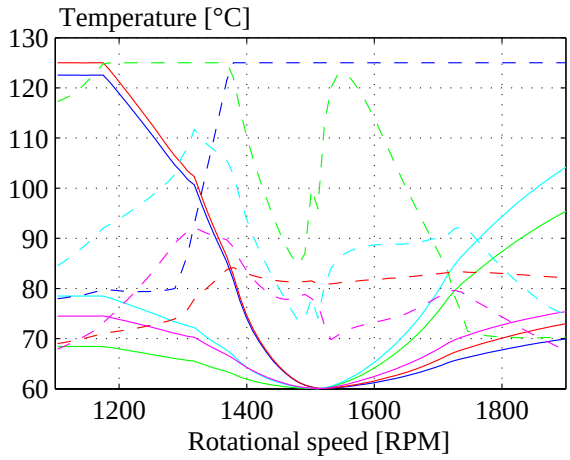

Figure 7.27: *Limiting components when using the DPWM0 modulation method in the diode clamped configuration.*

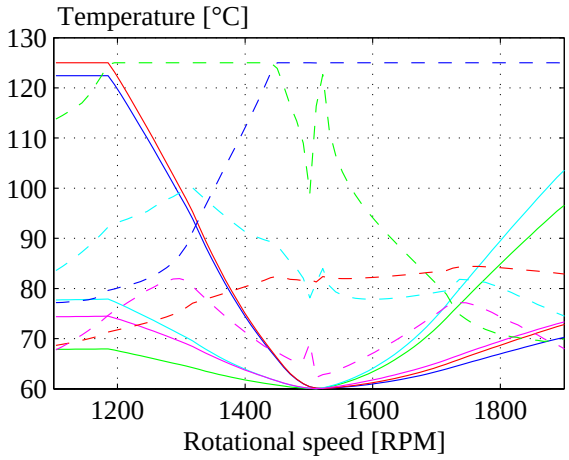

Figure 7.28: *Limiting components when using the DPWM1 modulation method in the diode clamped configuration.*

and as shown the top transistor (- -) and top diode (- -) are the limiting component in most of the operating range. Compared to the continuous modulation schemes, i.e. SVPWM1 and SVPWM2, the high stress when applying the discontinuous modulation methods is due to the selection of zero vectors in the clamping intervals. Based on Fig. 7.27 to Fig. 7.29 one could argue that the present design of the top-switch in the generator inverter should be changed when applying the discontinuous modulation schemes.

Considering the transistor clamped configuration, it appears that the operation dependent loading of the individual components are equal to the loading of the diode clamped

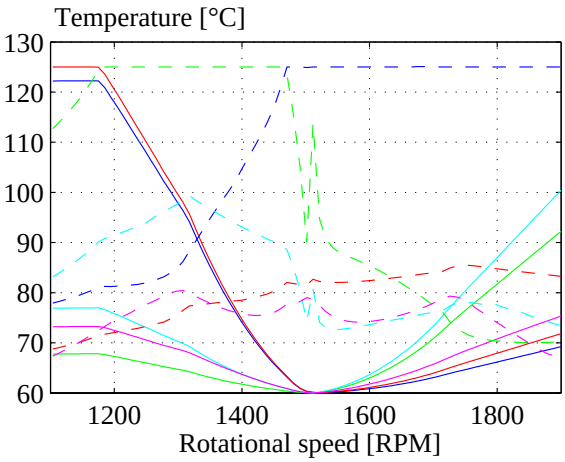

Figure 7.29: *Limiting components when using the DPWM2 modulation method in the diode clamped configuration.*

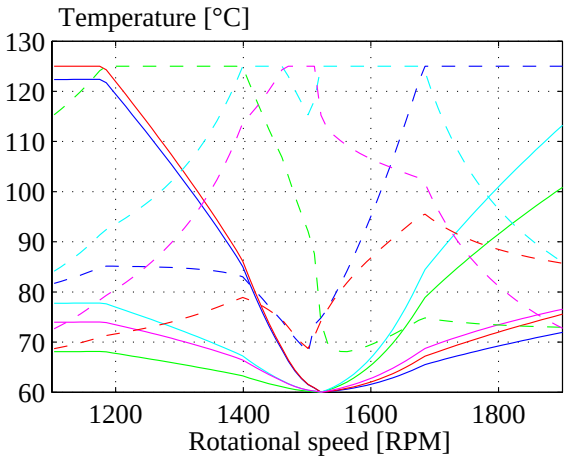

Figure 7.30: *Limiting components when using the CMPWM modulation method in the diode clamped configuration.*

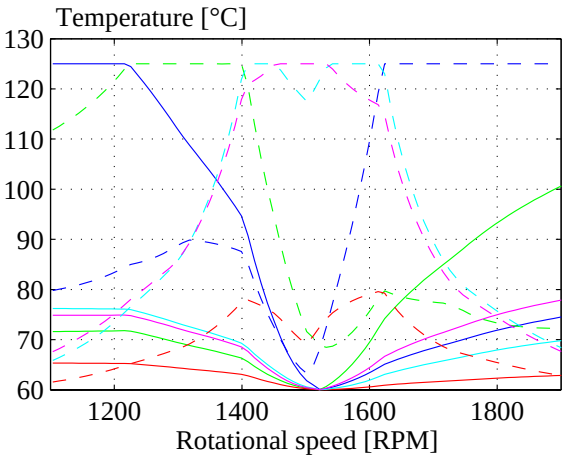

Figure 7.31: *Limiting components when using the SVPWM1 modulation method in the transistor clamped configuration.*

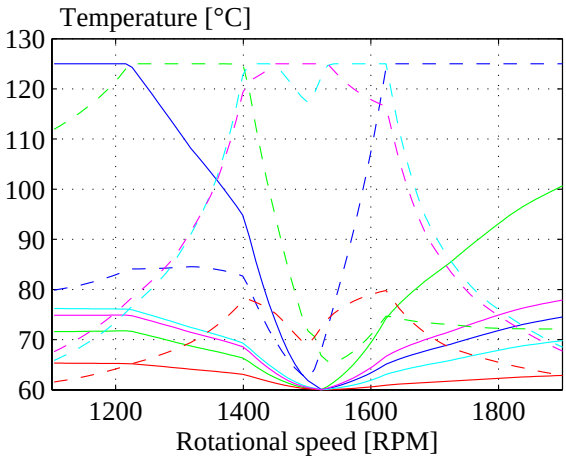

Figure 7.32: *Limiting components when using the SVPWM2 modulation method in the transistor clamped configuration.*

configuration. The only exception seems to be the load on the center diode (plotted by the red curve) which for the transistor clamped configuration is heavily relieved. Fig. 7.31 to Fig. 7.36 show the limiting components of the transistor clamped configuration. The color codes used in Fig. 7.31 - Fig. 7.36 correspond to those used for the diode clamped configuration and are explained on page 286.

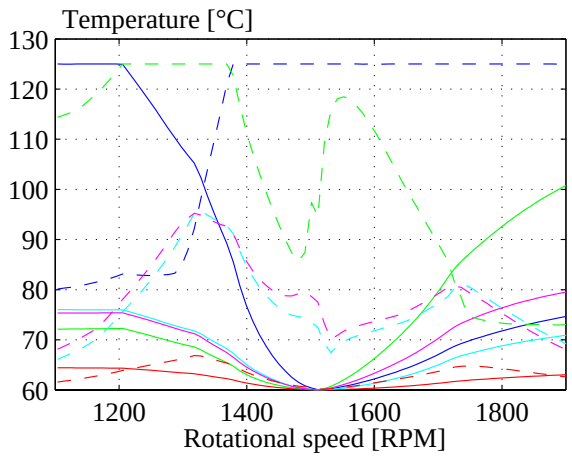

Figure 7.33: *Limiting components when using the DPWM0 modulation method in the transistor clamped configuration.*

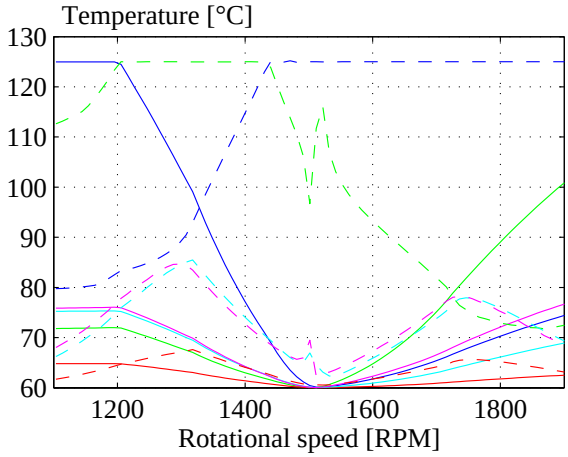

Figure 7.34: *Limiting components when using the DPWM1 modulation method in the transistor clamped configuration.*

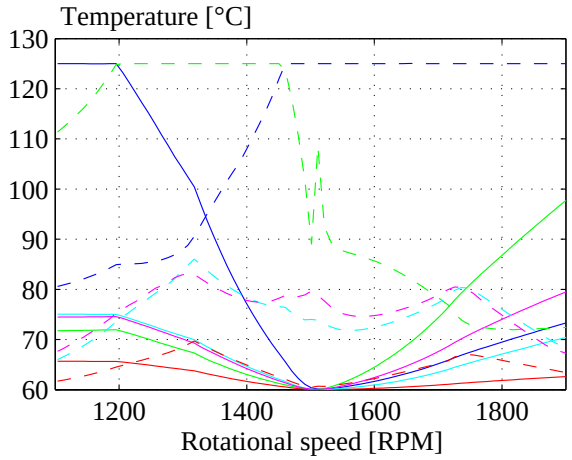

Figure 7.35: *Limiting components when using the DPWM2 modulation method in the transistor clamped configuration.*

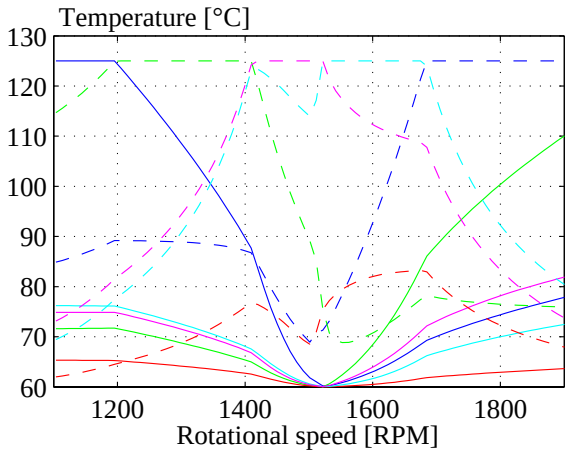

Figure 7.36: *Limiting components when using the CMPWM modulation method in the transistor clamped configuration.*

7.4.4 Power losses

Finally, besides the power capability set out by the converter design, the absolute power losses are an important aspect when choosing the modulation methods. Fig. 7.37 shows the converter losses of the diode clamped converter topology as a function of the wind speed when the turbine follows the power speed curve given by Fig. 7.2. Similarly, 7.38 shows the converter losses of the transistor clamped converter configuration. In the calculation of the converter power losses in Fig. 7.37 and Fig. 7.38 it is provided that both the grid side inverter and the rotor side inverter are using the same modulation methods. To achieve a more detailed "picture" of the losses and to have a better

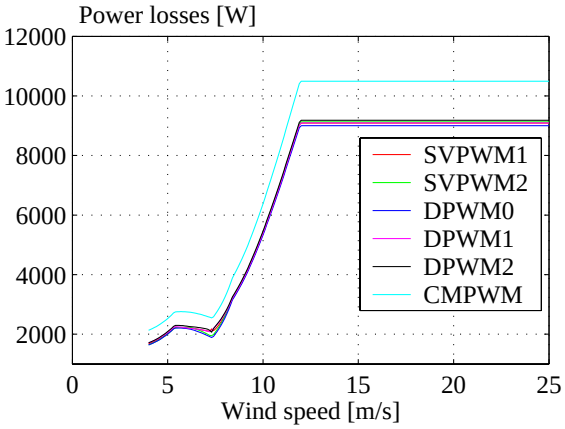

Figure 7.37: *Total converter power losses for the diode clamped configuration as a function of the wind speed for the considered modulation methods.*

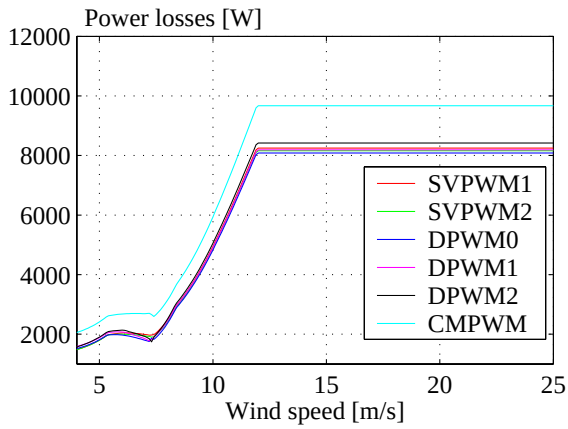

Figure 7.38: *Total converter power losses for the transistor clamped configuration as a function of the wind speed for the considered modulation methods.*

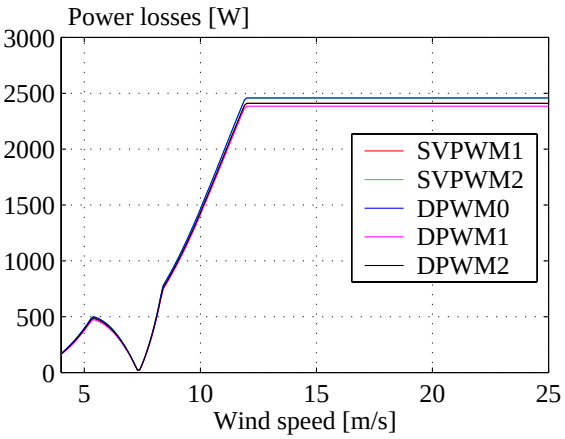

Figure 7.39: *Total grid inverter power losses for the diode clamped configuration as a function of the wind speed for the considered modulation methods.*

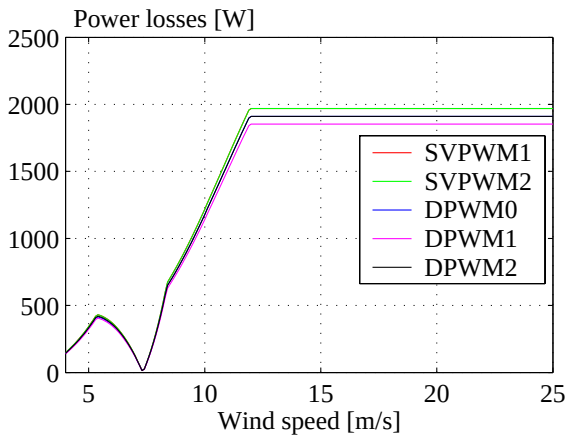

Figure 7.40: *Total grid inverter power losses for the transistor clamped configuration as a function of the wind speed for the considered modulation methods.*

foundation for the selection of modulation methods, Fig. 7.39 and Fig. 7.40 show the grid inverter losses of the two considered three-level topologies whereas Fig. 7.41 and Fig. 7.42 show the rotor inverter losses. Combining the information on converter capability read out from Fig. 7.23 and Fig. 7.24 with the inverter losses in Fig. 7.41 and 7.42 the rotor inverter of both the diode clamped configuration and the transistor clamped configuration in the present design examples should make use of the SVPWM2 modulation method due to good power loss properties and the quite good thermal distribution properties associated with this modulation method. On the other hand, selection of a modulation method for the grid inverter can be done without considering the power capability and hence according to Fig. 7.39 and Fig. 7.40 both the diode

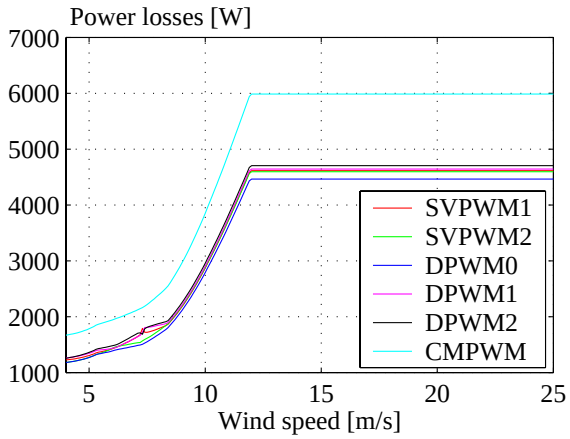

Figure 7.41: *Total generator inverter power losses for the diode clamped configuration as a function of the wind speed for the considered modulation methods.*

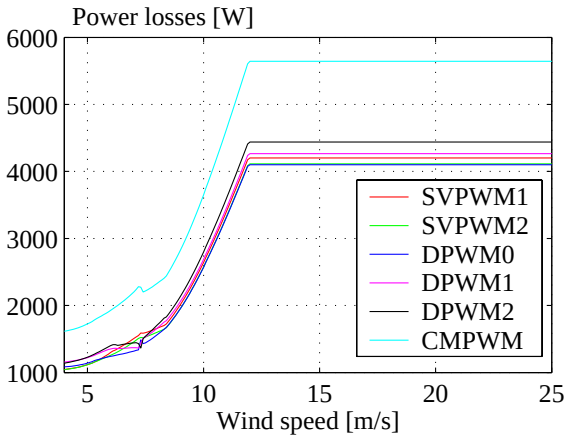

Figure 7.42: *Total generator inverter power losses for the transistor clamped configuration as a function of the wind speed for the considered modulation methods.*

TABLE X: *Converter components for the diode clamped topology.*

	Grid inverter	Generator inverter
Top switch type S_1	SkiiP 802GB060	SkiiP 802GB060
Center switch type S_3	SkiiP 802GB060	SkiiP 1602GB060
Clamp switch type S_1	SkiiP 802GB060	SkiiP 1602GB060
Inductor [μH]	400	60
Modulation method	DPWM1	SVPWM2
Switching frequency [kHz]	3.15	1.05
DC-link voltage [V]	800	800

clamped topology and the transistor clamped topology should make use of the DPWM1 modulation method.

7.4.5 Selection of converter components

Based on the loss evaluation and the evaluation of power capability, the main characteristics of the pre-designed back-to-back diode clamped three-level converter are listed in Table X. Similarly, the main characteristics of the pre-designed back-to-back transistor clamped three-level converter are listed in Table XI. The designs listed in Table X and Table XI will be used for the turbine comparison presented in the following section.

7.5 Converter comparison

In this section, the four considered converters will be evaluated with regard to the following measures:

- Component count.
- Switch utilization.
- Converter losses.
- Annual energy production.

7.5.1 Component count

As discussed in chapter 1 the turbine reliability is a major issue in a turbine design. A prediction of the system reliability however requires a detailed investigation. Actually, such an investigation should include a system level analysis to determine the degree of redundancy and inherent fault accelerators such as power cycling and thermal cycling as well as a component level analysis to determine individual component FIT-rates[2]. Such an investigation is clearly outside the scope of this thesis. However, if applying a pragmatic approach assuming that reliability to some extent is related to the number of involved semiconductor components - that is assuming equal FIT rates, no fault accelerators and ideal auxiliary components - the considered converter topologies are easily compared. Table XII shows the comparison of the considered converters listing the number of involved components. The first number represents the ideal component count whereas the number in parenthesis represents the actual component count in the present design example. Evaluating the component count, it appears that the conventional back-to-back two-level converter is clearly the best choice both when considering the ideal component count and for the actual design example.

[2]Failure in time

TABLE XI: *Converter components for the transistor clamped topology.*

	Grid inverter	Generator inverter
Top switch type S_1	SkiiP 942GB120	SkiiP 942GB120
Center switch type S_3	SkiiP 802GB060	SkiiP 1602GB060
Clamp switch type S_1	SkiiP 802GB060	SkiiP 1602GB060
Inductor [μH]	400	60
Modulation method	DPWM1	SVPWM2
Switching frequency [kHz]	3.15	1.05
DC-link voltage [V]	800	800

7.5.2 Switch utilization

Combined with the number of switching devices, the switch utilization can provide an indirect measure of the converter cost. Several approaches can be applied for calculating the switch utilization factor and in this context two approaches will be applied. The first approach simply gives a measure of the ratio between turbine nominal power and installed converter volt-amperes:

$$\nu = \frac{P_{tur}}{\sum V_T \cdot I_T + V_D \cdot I_D} \tag{7.1}$$

The approach in eq. (7.1) gives a single number for each of the considered topologies and can be calculated quite easily. However, by this simple approach one converter may be favored over another, simply by the lucky punch that present semiconductor ratings suits one converter better than another. Further, since the special application of the doubly-fed induction machine involves quite low frequency operation at the generator side the above mentioned simple switch utilization approach lacks information about the present converter topologies ability to handle these frequencies. Hence a more sophisticated approach can be applied where the actual turbine power capability is evaluated in relation to the totally installed volt-amperes:

$$\nu = \frac{\hat{P}_{tur}}{\sum V_T \cdot I_T + V_D \cdot I_D} \tag{7.2}$$

where $\hat{P}_{tur}$ is the turbine power to be generated in order to reach the thermal limits of the converter, $V_T \cdot I_T$ is the VA-rating for the individual transistors and $V_D \cdot I_D$ is the VA-rating for the individual diodes. Fig. 7.43 shows the utilization factor ν. The utilization factors calculated by the expression in eq. (7.1) are shown by the dashed lines whereas the utilization factors calculated by eq. (7.2) are shown by the solid lines. For both approaches, the matrix converter and the transistor clamped three-level voltage source converter appears to utilize the semiconductor components in the most efficient way.

TABLE XII: *Component counts.*

	# of diodes	# of transistors
Two-level	12 (54)	12 (54)
Matrix	18 (72)	18 (72)
Three-level (DC)	36 (96)	24 (60)
Three-level (TC)[a]	24 (60)	24 (60)

[a] In the component count for the transistor clamped three-level topology, the inactive diode connected in parallel with the center switch is not included.

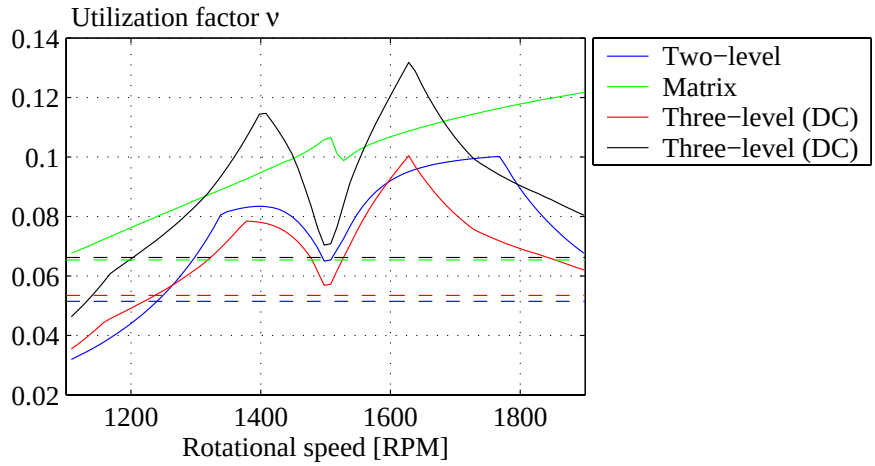

Figure 7.43: *The switch utilization factor for the considered converter topologies. Dashed lines are calculated by eq. (7.1) and solid lines are calculated by eq. (7.2).*

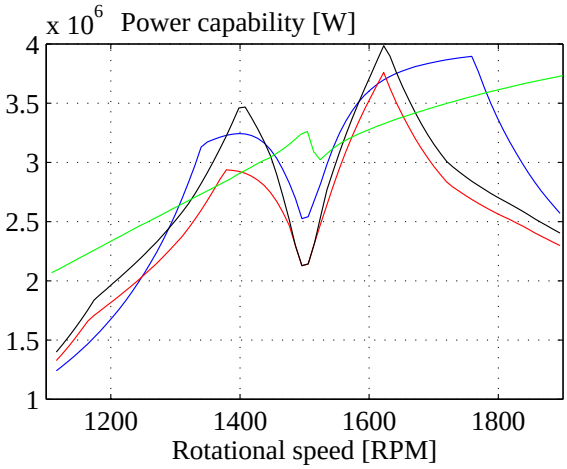

Figure 7.44: *Power capability of the system when considering the limits determined by the considered converter designs.*

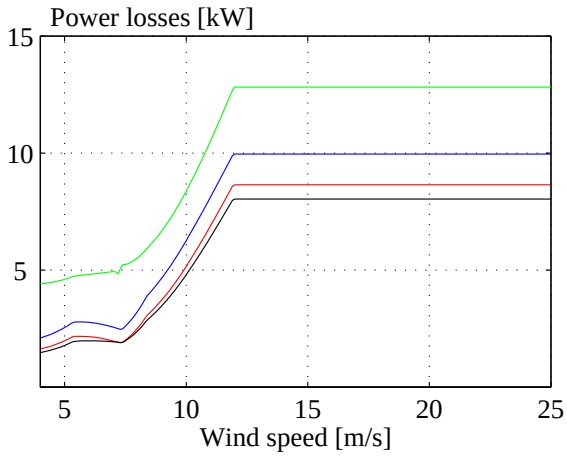

Figure 7.45: *Converter losses as a function of the wind speed for the different converter designs.*

7.5.3 Converter losses

The converter losses of the considered converter designs when operating in the normal operating range defined by the power speed curve in Fig. 7.2 is shown in Fig. 7.45. The blue curve represents the calculated losses for the back-to-back two-level voltage source converter, the green curve represents the losses for the matrix converter while the red and black curve represents the converter losses for the three-level diode clamped and transistor clamped converter topologies respectively. From the evaluation of converter power losses for the present converter lay-outs, the transistor clamped topology seems to be the best choice.

TABLE XIII: *Annual generated energy [pu] for different sites.*

	IEC I	IEC II	IEC III	IEC IV
Two-level	100.0	100.0	100.0	100.0
Matrix	99.7	99.5	99.5	99.2
Three-level (DC)	100.0	100.0	100.0	100.1
Three-level (TC)	100.0	100.1	100.1	100.1

7.5.4 Annual energy generation

Besides the reduced cooling needs, the converter losses will influence the annual energy production. Using standard wind distribution functions like those discussed in section 2.1 the annual energy production for the present turbine examples can be calculated. Table XIII shows the annual energy production for the considered turbine designs normalized to the expected production for the system based on the conventional two-level converter. Despite the large difference in converter power losses, the expected annual energy production is only affected insignificantly. The reason for this insignificant improvement is two-fold: firstly, the system based on the doubly-fed system does not "reward" the gained converter efficiency due to the fact that only 15-20% of the generated power is actually processed by the converter. Secondly, unlike other applications efficiency only count in partial load since in full-load operation all the excess of wind power is "dissipated" by pitching the blades out of the wind.

7.6 Summary

The purposes of this chapter has been to exemplify the developed comparison tool on some converter design examples. To perform the comparison, four converter designs were carried out - one for each of the considered converters. In order to obtain a fair comparison, each of the designs were evaluated with regards to the power capability determined by the converter design - an evaluation securing that each of the converter designs include more or less the same design margin. Considering the power losses of three converter design examples under the given operating conditions, the three-level transistor clamped converter is the best choice. However considering the gain in annual captured energy for a typical site (IEC II), the difference between the considered converter designs are in the order of 0.1-0.5% which is an insignificant improvement and within the uncertainty on the modeling approaches. As a final remark on the comparison it should be noted that a comparison on wind turbine with full power conversion through the power converter may give a more significant difference between the considered converters.

Chapter 8

Conclusion

ON the preceding 295 pages, this report has strictly focused on describing and developing models for a simulation tool suitable for a fast comparison of converter topologies for use in a wind turbine based on the doubly-fed induction machine. However, especially during the maturing efforts carried out on the considered converter topologies, the treatment has entered into very detailed levels and of course an entrance into such detailed explanations is done at the risk of loosing the continuity. For the purpose of remedying this particular issue, a brief summary of the individual chapters will be outlined. Then, since the present report is submitted as a part of fulfilling the requirements for the Ph.D-degree in electrical engineering and hence is to be judged on its contributions, the summary is followed by a list of topics considered to be contributions. Finally, as the normal outcome when digging into one particular problem seems to be that two new problems arise, the chapter is closed by pointing out areas for further investigation - areas closely related to the contributions of the present work.

8.1 Summary

As a general summary, this thesis has described the development of a tool suitable for comparing different converter topologies for use in a wind turbine application based on the doubly-fed induction generator. Specifically, the report treated four converter topologies, namely the back-to-back two level voltage source converter, the matrix converter, the back-to-back diode clamped three-level voltage source converter and the back-to-back transistor clamped three-level voltage source converter. Actually the *backbone* of the report is the modeling and maturing efforts of these four converters whereas the remaining chapters describing e.g. the modeling of the components interfacing to the converter is to be considered as a secondary contribution. The report include 7 chapters (apart from the present chapter) and the content of each chapter is briefly summarized below:

Chapter 1 on pages 3-21 "Introduction": This chapter presented some factual trends showing the progress in the wind energy sector as well as national programmes

and objectives initiated to promote wind energy even further in the future. Then the salient features of a variable speed wind turbine compared to a constant speed wind turbine were discussed and a brief overview of different variable speed wind turbine topologies were outlined - an overview which included topologies proposed by the academia as well as topologies used by the industry. Then the problem statement was presented and finally the outline for the thesis was discussed, including a short list of focus areas to which the main efforts in the present work has been dedicated.

Chapter 2 on pages 23-44 "Modeling of wind turbine system": This chapter was dedicated to develop and describe the modeling approaches used to model the individual turbine components interfacing directly or indirectly to the power converter. The purpose of the modeling has been: 1) to identify the power flow and thereby identify the current and voltage ratings for the considered converter and 2) to calculate the losses of the different components in order to evaluate the annual energy production. The loss models for the gear box and generator were based on measured data whereas the parameters for the transformer model were based on a standard data sheet information. Finally, since the upcoming national grid codes have a high impact on the necessary converter rating, the last section of this chapter summarized some of the most important steady state grid code requirements.

Chapter 3 on pages 47-87 "The back-to-back two-level voltage source converter": This chapter has provided a comprehensive overview of the back-to-back two-level voltage source converter, conventionally used in variable speed wind turbines. The section was introduced by an explanation of the operating principles followed by a detailed description of the most commonly used modulation methods. For the considered modulation methods, harmonic performance were evaluated in order to be able to select a switching frequency with comparable harmonic distortion. Further, closed form analytical expressions for the modulation method dependent conducting losses and switching losses have been derived. For the purpose of including the switch temperature in the converter loss evaluation, analytical expressions for the average switch temperature has been derived. Further, due to the fact that the rotor inverter in the doubly-fed system is operated at low frequencies the peak temperature deviate quite much from the average temperature. Hence for the purpose of a fast validation of a certain converter design, some analytical approximations have been proposed. Finally, to be able to pre-dimension the back-to-back two-level voltage source converter, some rules of thumb regarding switch current ratings, switch voltage ratings, DC-link design and inductor design have been presented.

Chapter 4 on page 89-148 "The matrix converter": This chapter has treated the three-phase to three-phase matrix converter for use in a wind turbine application based on the doubly-fed induction generator. Specifically, the aim of the chapter was to be able to compare the matrix converter with the more matured back-to-back two-level

converter conventionally used in said application. The chapter was introduced by a short review on previous work within the field of matrix converters but as the use of matrix converters in wind turbine applications appeared to be almost unknown, the survey has focused on matrix converters in general. The survey on previous work was followed up by an explanation of the basic working principles of the converter. The explanation of the basic working principles is a pure mathematical exercise and although complicated at a first glance, the real obstacles for the matrix converter occur due to non-ideal conditions. These non-ideal conditions involves considerations such as commutation strategy, bi-directional switch realization and operation with unbalanced or faulty input- and output conditions. These working principle related issues are addressed in the major part of previous work. Closely related to the working principles are the modulation of the matrix converter which has to take into consideration both the generation of a sinusoidal input current and a sinusoidal output voltage and unlike the previously considered back-to-back two-level converter this has to be done without an intermediate energy storage. To obtain a fair comparison between the quite un-matured matrix converter and the conventionally used back-to-back two-level voltage source converter, a lot of efforts in this chapter were dedicated to develop new modulation methods for the matrix converter - modulation methods aiming to minimize the generated power losses [7] and/or the generated harmonic distortion [8]. To be able to compare the considered modulation methods internally as well as comparing the matrix converter with the other converter topologies, the modulation methods were evaluated with regard to harmonic performance [5] on both the grid side and generator side as well as with regard to the generated power losses. Regarding the power losses generated by the matrix converter, analytical expressions were derived taking into account the modulation method as well as the temperature of the considered components. Finally, to be able to pre-design the matrix converter, some rules of thumb regarding switch current ratings, switch voltage ratings, choice of switching frequency and input filter design have been presented.

Chapter 5 on pages 149-248 "The back-to-back three-level voltage source converter": The aim of this chapter was to establish a foundation for a fair and direct comparison of the three level voltage source inverter with the more matured two-level voltage source inverter. Although an inverter with three-level properties can be realized by several topologies, the chapter has focused on the diode clamped three-level inverter and the transistor clamped three-level inverter. The chapter was introduced by a brief survey on previous work, trends and focus areas in the field of three level inverters. However, as three-level inverters are relatively unknown in wind turbine applications the survey covered activities within other technical areas. Then the basic working principles were discussed followed by a thorough explanation of the modulation principles especially with focus on the space vector approach. As the modulation schemes for the three-level inverters are not as matured as the corresponding modulation schemes for the two-level inverter, a lot of efforts have been dedicated to the development of modulation schemes comparable to the schemes for the two-level counterpart. The developed mod-

ulation schemes included discontinuous schemes and a scheme with complete common-mode voltage elimination [4]. As the DC-link balance is a major issue for three-level inverters, all the developed schemes included active DC-link balancing capabilities. All the considered modulation methods, were evaluated with respect to their harmonic performance in order to be able to select a switching frequency with comparable harmonic distortion. In order to use an RMS model for the purpose of comparing the different modulation methods as well as the different topologies the inverter losses were to be calculated. This involved derivation of analytical expressions for both RMS current and average current through each individual component - expressions which turned out to be modulation method dependent, load angle dependent as well as modulation index dependent. For the purpose of including the switch temperature in the converter loss evaluation, analytical expressions for the average switch temperature have been derived. Further, due to the fact that the rotor inverter in the doubly-fed system is operated at variable but low frequencies the peak temperature deviate quite much from the average temperature. Hence for the purpose of a fast validation of a certain converter design, some analytical approximations for the peak temperature has been proposed. Finally, to be able to pre-dimension the back-to-back three-level voltage source converters, some rules of thumb regarding switch current ratings, switch voltage ratings, DC-link design and inductor design have been presented.

Chapter 6 on pages 249-267 "Wind turbine comparison tool": This chapter has provided an introduction to the wind turbine simulation tool *D'rives* or at least to that part of the tool concerning the models described in this thesis. In summary, *D'rives* is a package with a graphical interface linking all the modeling approaches described throughout this report in a user-friendly and well-arranged manner. The simulation tool provides easy access for changing the topology configuration and change of main characteristics such as power-speed curve, star-delta connection and active/reactive power generation. Further, each of the main components, i.e. blades, gear box, generator, converter and transformer have a separate page allowing change of all the parameters involved in the modeling approaches described in chapter 2 - chapter 5. The representation of simulation results is very flexible as most internal simulation variables can be plotted against each other. As a final remark, it should be noted that due to the explicit analytical expressions for component currents and component losses, the simulation speed of the *D'rives* program is extremely high. For instance, a simulation of peak temperatures of the semiconductors in a converter design calculated for the entire power/speed operating range has been reduced from a day-long simulation task into a simulation time of about 2 seconds.

Chapter 7 on pages 271-295 "Topology comparison": The purposes of this chapter has been to exemplify the developed comparison tool on some converter design examples. To perform the comparison, four converter designs were carried out - one for each of the considered converters. In order to obtain a fair comparison, each of the designs

were evaluated with regards to the power capability determined by the converter design - an evaluation securing that each of the converter designs include more or less the same design margin. Considering the power losses of three converter design examples under the given operating conditions, the three-level transistor clamped converter is the best choice. However considering the gain in annual captured energy for a typical site (IEC II), the difference between the considered converter designs are in the order of 0.1-0.5% which is an insignificant improvement and within the uncertainty on the modeling approaches. As a final remark on the comparison it should be noted that a comparison on wind turbine with full power conversion through the power converter may give a more significant difference between the considered converters.

8.2 Contributions

Although the preparation of this report aimed to present all the contributions arising from the executed work some aspects may have been lost or suppressed in the entirety. Especially, contributions from the present work published elsewhere may have been skipped or simply just referred by a citation. Below follows a list of publications published or co-published by the author.

Comparison of different converter topologies: Comparison of different converter topologies for use in a variable speed wind turbine based on the doubly-fed induction generator [3]

New modulation strategies for the matrix converter : In the efforts on maturing the matrix converter, one task was to investigate and develop new modulation strategies having better harmonic properties and/or lower switching losses compared to existing strategies. Some of these efforts are described in [7, 8].

Tools for evaluating different modulation strategies: Besides developing new modulation strategies, a survey on the literature covering matrix converters revealed that unlike for the two- and three-level inverters, no methods existed for evaluating modulation strategies for the matrix converter. It was found worthwhile to spend some efforts developing a comparison method similar to those for two- and three-level inverters. The comparison tool is described in [5].

New modulation strategies for the three-level converter: As for the matrix converter, the study on three-level converters (and multi-level inverters in general) revealed that the maturing process for the three-level inverters needed a little injection with regards to modulation strategies. Hence, some efforts were also dedicated to develop new modulation strategies for the three-level converter, especially with focus on harmonic properties, switching losses and DC-link balancing [4, 6].

The citations mentioned above are all enclosed in Appendix C-I. Besides the work documented in this thesis and in the publications cited above, the intensive work in

converter topologies for the doubly-fed induction machine has made it possible to partly contribute to the following work:

Patent WO 01/91279 A1 [10]: The patent entitled "Variable Speed Wind Turbine having a Matrix Converter", International publication number WO 01/91279 A1 was partly initiated by the work described in chapter 4 of the this thesis. The content of the patent was formulated in co-operation with Anders V. Rebsdorf a former colleague at Vestas Wind Systems.

The book "Control in Power Electronics" [9]: Chapter 13 of the book *"Control in Power Electronics"*, covering wind turbine systems was written, based on knowledge obtained during the Ph.D.-programme. The chapter is a general survey over different wind turbine concepts, including some control aspects and was written in co-operation with Frede Blaabjerg.

The technical report "Risø-R-1205(EN)" [2] .Chapter 3 of the technical report *"Risø-R-1205(EN)"*, entitled *"Conceptual survey of Generators and Power Electronics for Wind Turbines"* covers different converter topologies for use in variable speed wind turbines and was based on a preliminary survey report written in the early stage of the Ph.D-programme.

Finally, apart from the publications etc. listed above, especially the work carried out to derive the current loading of the individual components as well as the peak temperature estimation methods are considered to have some novelty over prior art.

8.3 Perspectives

Approaching the end of the thesis the final task left for completing the report is to point out areas left for further investigation. From the very beginning of project, the scope of the research was three-fold:

1. Evaluate selected converter topologies for use in wind turbines based on the doubly-fed induction generator.

2. Design the selected converter.

3. Develop a control scheme for the selected converter, usable in a wind turbine application.

During the initial work it became clear that fulfilling these three tasks on a sufficiently detailed level was an overwhelming task. Especially the latter two subjects seemed to involve tasks already being handled by engineers within the wind industry and hence the fulfillment of these tasks seemed to be an unfair competition between a Ph.D student with novice skills in specific wind turbine technology and several experienced wind turbine engineers whereas the converter evaluation and to some extent design issues related

to the specific converters seemed to be a more *virginal* area. Hence the introductory part was rewritten to match the reduced content of the thesis.

Pointing out tasks left for further investigation it would be easy to direct such tasks to the remaining objectives of the original scope of the project. However, with the changed and limited scope of the thesis and with the present content of the report in mind several topics seems quite more obvious to tackle. The following lists these topics and the expected advantages obtained by solving these issues.

Investigate whether the modulation scheme with common-mode voltage elimination reduces the bearing currents in a doubly-fed induction generator. Although it is uncertain whether the problems regarding bearing currents is more severe for doubly-fed machines it is likely to believe that this is the case as the winding-to-shaft capacitance is much larger for the rotor than for the stator. It could be investigated to what extent the proposed modulation scheme is able to lower the bearing current level.

Harmonic content During the evaluation of the modulation schemes for the different converters and the selection of an appropriate switching frequency, only the harmonic distortion factor was considered. For sufficiently high frequencies this approach may be adequate but for the present application and especially when considering wind turbine applications with full scale power conversion the specific harmonic content is of interest and may very well favor one particular modulation. Hence the comparison tool could/should be extended in order to be able to predict the harmonic content emitted to the grid.

Converter design margin due to speed variations: With an unpredictable power source such as the wind no such steady-state condition exists and hence the speed and thereby the rotor inverter frequency will have to vary in order to keep the output power constant. Presently the modeling approach has concerned steady-state operation, although with the possibility of calculating the per-fundamental temperature variation in the semiconductor devices. In a practical design the temperature variations due to a certain rotor speed profile will have to be considered as well and hence without deviating from the purpose of having a fast model based on analytical expressions the modeling approach from a converter design point of view would have to be considered.

Estimation of semiconductor lifetime: As pointed out in [1], a potential problem for wind turbines based on the doubly-fed induction generator is the very low frequency at which the generator inverter is operated. Depending on the converter design, this low-frequency operation may cause high temperature variations within the semiconductor devices of the generator inverter leading to premature failures due to power cycling and thermal cycling. Extending the evaluation tool to incorporate analysis of a varying rotor speed profile, the calculation of semiconductor temperatures could be used as input to

tools able to calculate semiconductor lifetime.

References

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[9] F. Blaabjerg M.P. Kazmierkowski, R. Krishnan. *Control in Power Electronics*. Academic Press, ISBN : 0-12-402772-5, 2002.

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Part IV

Appendices

Appendix A

Extraction of switch parameters

IN the efforts of determining the switching losses of the different converter topologies, it was chosen to use a method based on a simplified switch model of the converter combined with parameters obtainable from datasheets. In cases where the data sheet informations are not sufficient, the parameters can be derived from measured/simulated loss data. This appendix describes a method usable to derive the necessary switch parameters. It should be noticed that the loss values used to exemplify the method in this appendix is calculated from a program supplied by the semiconductor manufacture `SEMIKRON`. However the algorithm used to derive the parameters can as well be applied to measured data.

The appendix is introduced with a description of the modeling approach, followed by a description of the derivation of the switch parameters.

A.1 Modeling approach

The losses in the switches (transistors and diodes) are modeled by:

$$P_{dx} = V_{d0}(T_{dj}) \cdot I_{d,avg} + R_d(T_{dj}) \cdot I_d^2 + E_{sw0,d}(T_{dj}) \cdot f_{sw} \cdot I_{sw,avg} \quad \text{(A.1)}$$

$$P_{dx} = V_{t0}(T_{tj}) \cdot I_{t,avg} + R_t(T_{tj}) \cdot I_t^2 + E_{sw0,t}(T_{tj}) \cdot f_{sw} \cdot I_{sw,avg} \quad \text{(A.2)}$$

where $I_{d,avg}$ and $I_{t,avg}$ are the average current through the diode and transistor, I_d and I_t are the RMS currents and $I_{sw,avg}$ is the average switched current which is equal for both the diode and the transistor.

A.2 Switch losses

This section describes a procedure for deriving the switch parameters V_{d0}, R_d, $E_{sw0,d}$, V_{t0}, R_t and $E_{sw0,t}$ by use of the SEMISEL program supplied by `SEMIKRON` [1]. Fig. A.1 shows the converter topology used to derive the switch parameters.
Knowing the modulation function for one phase leg of the full bridge arrangement in Fig. A.1 the RMS current and the average current can be calculated as a function of the

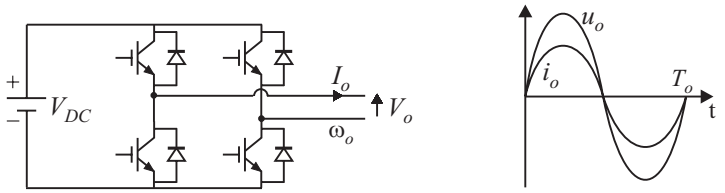

Figure A.1: *Test topology for deriving the switch parameters.*

output current i_{out} and the modulation index M. The modulation function δ is given by:

$$\delta = \frac{1}{2}(1 + M\sin(\omega_o t)) \tag{A.3}$$

where M is $\frac{\sqrt{2}V_o}{V_{DC}}$. The average current through the switch $I_{t,avg}$ is:

$$\begin{aligned}
\langle I_{t,avg}\rangle_{T_o} &= \frac{1}{T_o}\int_0^{\frac{T_o}{2}} (\delta \cdot \hat{i}_o \cdot \sin(\omega_o t))dt \\
&= \frac{1}{T_o}\int_0^{\frac{T_o}{2}} \left(\frac{1}{2}(1 + M\sin(\omega_o t)) \cdot \hat{i}_o \cdot \sin(\omega_o t)\right) dt \\
&= \frac{1}{8\pi}\left(4 + M\pi\right)\hat{i}_o
\end{aligned} \tag{A.4}$$

The RMS current through the switch is determined by:

$$\begin{aligned}
\langle I_t\rangle_{T_o} &= \sqrt{\frac{1}{T_o}\int_0^{\frac{T_o}{2}} (\delta \cdot \hat{i}_o^2)dt} \\
&= \sqrt{\frac{1}{T_o}\int_0^{\frac{T_o}{2}} \left(\frac{1}{2}(1 + M\sin(\omega_o t)) \cdot (\hat{i}_o \cdot \sin(\omega_o t))^2\right) dt} \\
&= \sqrt{\frac{1}{24\pi}\left((3\pi + 8M)\hat{i}_o^2\right)}
\end{aligned} \tag{A.5}$$

Similarly, the average current for the diode is derived:

$$\begin{aligned}
\langle I_{d,avg}\rangle_{T_o} &= \frac{1}{T_o}\int_{\frac{T_o}{2}}^{T_o} ((1 - \delta) \cdot \hat{i}_o \cdot \sin(\omega_o t))dt \\
&= \frac{1}{T_o}\int_{\frac{T_o}{2}}^{T_o} \left(\frac{1}{2}(1 - M\sin(\omega_o t)) \cdot \hat{i}_o \cdot \sin(\omega_o t)\right) dt \\
&= \frac{1}{8\pi}\left(4 - M\pi\right)\hat{i}_o
\end{aligned} \tag{A.6}$$

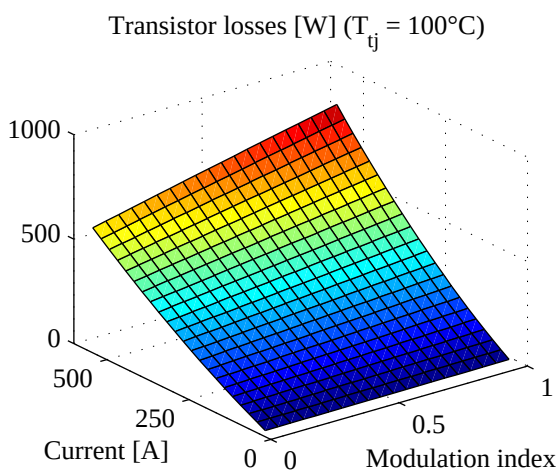

Figure A.2: *Simulated transistor losses (T_{tj}=100° C)*

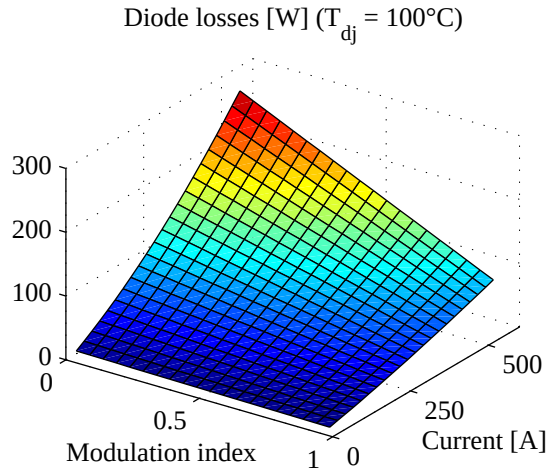

Figure A.3: *Simulated diode losses (T_{dj}=100° C)*

The RMS current through the diode is determined by:

$$\begin{aligned}\langle I_d\rangle_{T_o} &= \sqrt{\frac{1}{T_o}\int_{\frac{T_o}{2}}^{T_o}((1-\delta)\hat{i}_o^2)dt} \\ &= \sqrt{\frac{1}{T_o}\int_{\frac{T_o}{2}}^{T_o}\left(\frac{1}{2}(1-M\sin(\omega_o t))\cdot(\hat{i}_o\cdot\sin(\omega_o t))^2\right)dt} \\ &= \sqrt{\frac{1}{24\pi}\left((3\pi-8M)\hat{i}_o^2\right)} \end{aligned} \tag{A.7}$$

The average switching current is:

$$\begin{aligned}\langle I_{sw,avg}\rangle_{T_o} &= \frac{1}{T_o}\int_0^{\frac{T_o}{2}}(\hat{i}_o\sin(\omega_o t))dt \\ &= \frac{2}{\pi}\hat{i}_o \end{aligned} \tag{A.8}$$

Using eq. (A.4) - eq. (A.8) the transistor- and diode current can be calculated for any given output current I_o and output voltage V_o. Fig. A.2 and Fig. A.3 shows the simulated losses in the a transistor and a diode as a function of the duty-cycle, i.e output voltage and the output current.

A.3 Parameter extraction

Regardless of the method used to derive the loss data of the transistor and the diode, the algorithm used to derive the parameters $V_{d0}(T)$, $R_d(T)$, $E_{sw0,d}(T)$, $V_{t0}(T)$, $R_t(T)$ and $E_{sw0,t}(T)$ is based on a least square regression model [2]. The algorithm used to

derive the parameters is shown below.

for $k = 1 : N$
  $\underline{\phi} = [I_{d,avg}(k) \;\; I_d^2(k) \;\; f_{sw} V_{DC} I_{sw,avg}(k)\,]^T$
  $\underline{\underline{G}} = \underline{\underline{G}} + \underline{\phi} P_D$
  $\underline{\underline{R}} = \underline{\underline{R}} + \underline{\phi}\,\underline{\phi}^T$
  if $\det(\underline{\underline{R}}) \neq 0$
  | $\theta = \underline{\underline{R}}^{-1} \underline{\underline{G}}$
  end
end
$V_{d0} = \theta(1)$
$R_d = \theta(2)$
$E_{sw0,d} = \theta(3)$

Fig. A.4 and A.5 on the next page shows the convergence of the parameter extraction for the transistors and for the diodes respectively.

Repeating the procedure for different junction temperatures, following expressions for the switch parameters are derived:

$$\begin{aligned} U_{t0} &= 2.012 \cdot 10^{-3} \cdot T_{Tj} + 1.243 && [\mathrm{V}] \\ R_t &= 3.242 \cdot 10^{-6} \cdot T_{Tj} + 1.722 \cdot 10^{-3} && [\Omega] \\ E_{sw0,t} &= 1.616 \cdot 10^{-9} \cdot T_{Tj} + 8.628 \cdot 10^{-7} && [\mathrm{s}] \end{aligned} \tag{A.9}$$

$$\begin{aligned} U_{d0} &= -3.203 \cdot 10^{-3} \cdot T_{Tj} + 1.404 && [\mathrm{V}] \\ R_d &= 7.913 \cdot 10^{-7} \cdot T_{Tj} + 1.246 \cdot 10^{-3} && [\Omega] \\ E_{sw0,d} &= 11.038 \cdot 10^{-11} \cdot T_{Tj} + 5.363 \cdot 10^{-8} && [\mathrm{s}] \end{aligned} \tag{A.10}$$

References

[1] http://www.semikron.de. Homepage of Semikron. 2006.

[2] Karl Johan Åström and Björn Wittermark. *Adaptive control*. Addison-Wesley Publishing Company, Inc, ISBN : 0-201-55866-1, 1995.

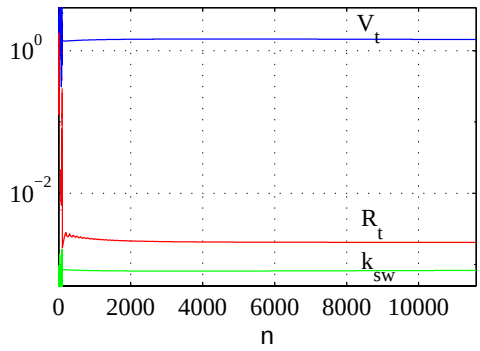

Figure A.4: *Convergence for the transistor parameters.*

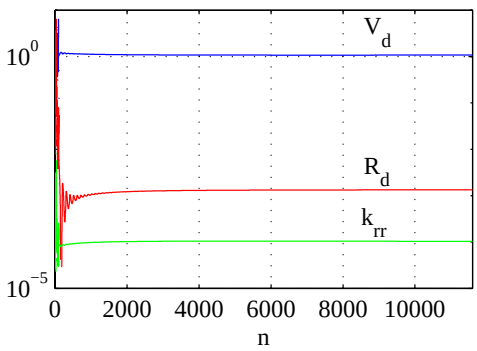

Figure A.5: *Convergence for the diode parameters.*

Appendix B

Inductor design

THIS appendix provides a procedure usable for designing the filter inductors used in the different converters. Output from the design procedure is, besides the inductor layout in terms of materials , windings and weights, the equivalent loss describing resistance and the thermal properties of the design. The loss describing resistance incorporates both copper losses, hysteresis losses and iron losses.

B.1 Design parameters

The following parameters are input to the inductor design procedure:

- The nominal inductance L
- The maximum flux density $\hat{B}$
- The maximum nominal inductor current $\hat{I}$, the corresponding current density $\hat{J}$ and the maximum transient current $\hat{I}_{max}$
- Available cores, including dimensions and magnetic properties
- Maximum allowable inductor temperature and ambient temperature
- The copper fill factor k_{cu} and the stacking factor k_{st}

B.2 Prerequisites and definitions

In order to limit the degree of freedom in the inductor design and reduce the complexity of the design algorithm, a few simplifications are introduced and the choice of core configurations are limited.

B.2.1 Assumptions

In the present inductor design approach, the following assumptions are made in order to simplify the calculations.

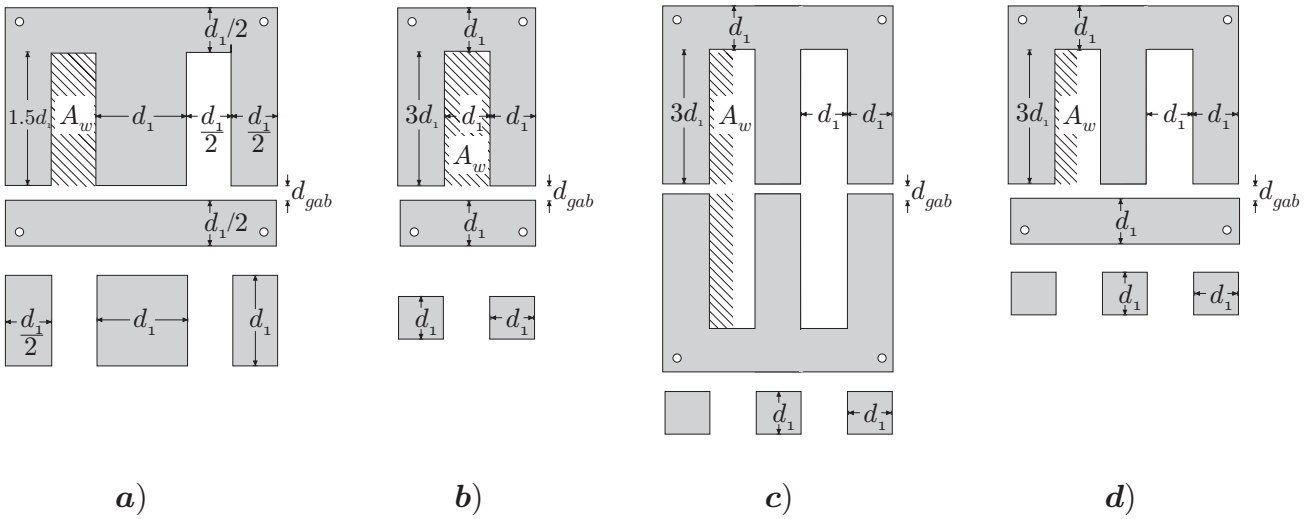

Figure B.1: *Standard core configurations.* **a)** *Single phase EI-core.* **b)** *Single-phase UI core.* **c)** *Three-phase EE core.* **d)** *Three-phase EI-core.*

Homogeneous temperature throughout the inductor: In steady state conditions, the temperature throughout the inductor is assumed to be uniform.

Linear magnetic properties: In the design procedure, the magnetic properties of the core material are assumed to be linear. Depending on the chosen value for the design parameter $\hat{B}$, the corresponding parameter $\hat{I}_{max}$ and the chosen magnetic core material, this assumption might be crucial.

No leakage flux exists: In the design algorithm it is assumed that flux lines follow the magnetic path defined by the core. Reflecting on this assumption, it appears that the designed inductance will be slightly lesser than desired due to the fact that the leakage flux reduces the flux linkage $N_t\phi$ and decreases the reluctance in the magnetic path.

B.2.2 Core configurations

The analysis and design are limited to standard cores defined by the properties in Fig. B.1 [3]. The dimension parameter d_1 is the so-called form-factor.
Besides limiting the inductor design to the standard cores defined on Fig. B.1, only cores having quadratic cross-sectional area are considered, i.e. the stack width equals the form-factor d_1. Further, the lamination thickness is fixed to 0.3 mm, although laminations thickness is available in a large range.

B.3 Design approach

Basically, from Amperes Law:

$$\oint Hdl = N_t \cdot i \tag{B.1}$$

Using $B = \mu H$, the continuity of flux lines and the assumption that no leakage flux exists, eq. (B.1) may be rewritten in the form:

$$\begin{aligned} \phi \oint \frac{dl}{\mu A} &= N_t \cdot i \\ &= \phi \cdot \Re \end{aligned} \tag{B.2}$$

where A is the cross-sectional area of the circuit at the point under consideration, μ is property constant depending on the medium in which the magnetic field H propagates and ϕ is the flux through the area A. In the actual case, where the magnetic path l is formed by a core (with an air g) which in turn consist of a number homogeneous pieces, both with respect to material and cross section, the reluctance $\Re$ can be approximated by:

$$\Re = \sum_j \frac{l_j}{\mu_j A_j} \tag{B.3}$$

Relating the above stated equations to the self inductance, Faradays Law is used:

$$e = N_t \frac{d\phi}{dt} \tag{B.4}$$

Assuming that the only flux linking the considered inductor, is the flux produced by the current in the inductor and that the flux is linearly dependent on the flux producing current, then eq. (B.4) can be rewritten:

$$\begin{aligned} e &= -N_t \frac{d\phi}{dt} \\ &= -N_t \frac{d\phi}{di}\frac{di}{dt} \\ &= -L\frac{di}{dt} \end{aligned} \tag{B.5}$$

For a constant relationship between current changes $\frac{di}{dt}$ and flux changes $\frac{d\phi}{dt}$, i.e. linear magnetic circuit, eq. (B.2) and eq. (B.5) reveal that:

$$L = \frac{N_t^2}{\Re} \tag{B.6}$$

The basic equations in eq. (B.1) - eq. (B.6) form the foundation for the inductor design procedure described in this section.

B.3.1 Geometric constraints

Considering the geometric dimensions of the cores in Fig. B.1 it appears that the maximum number of turns $\hat{N}_t$ is limited by:

$$\hat{N}_t = k_{cu} \cdot A_w \frac{\hat{J}}{\hat{I}} \tag{B.7}$$

where A_w is the winding window of the considered core. The winding window of the four considered cores is defined on Fig. B.1 as the hatched area. Combining eq. (B.2), eq. (B.6) and eq. (B.7) and assuming that the flux density inside the core B_c is uniform and given by $B_c = \frac{\phi}{A_c}$, the following inequality is obtained:

$$\begin{aligned} N_t &\leq \hat{N}_t \\ L \cdot \hat{I} \cdot \hat{I}_{max}\sqrt{2} &\leq k_{cu} A_w A_c \hat{B} J \end{aligned} \tag{B.8}$$

From eq. (B.8), the minimum applicable core size, with respect to magnetic properties, is found.

B.3.2 Air g

The purpose of the air-g is to increase the reluctance of the magnetic path in order to assure that the designed inductor is operated in the linear range, i.e. the flux density is kept below the design parameter $\hat{B}$ when the inductor carries the current $\hat{I}_{max}$. The air g d_g is defined on Fig. B.1. The reluctance of the air g $\Re_g$ is calculated by:

$$\Re_g = \frac{l_g}{\mu_0 \cdot A_g} \tag{B.9}$$

where l_g is the length of the air g and A_g is the cross-sectional area of the air g. To account for the fringing phenomena, the resultant cross-sectional area of the air-g becomes larger than the area of the core, reducing the flux-density in the air-g . Empirically, the cross-sectional area A_g of the air-g is determined by [4]:

$$A_g = (d_x + d_g)(d_y + d_g) \tag{B.10}$$

where d_x and d_y are the core dimensions and d_g is the length of the air-g. From eq. (B.2):

$$\Re = \frac{N_t \sqrt{2} \hat{I}_{max}}{A_c \hat{B}_c} \tag{B.11}$$

Single phase EI-core

Considering the single-phase EI-core, the reluctance of the center-leg air g $\Re_{g1}$, the outer-leg air gs $\Re_{g2}$ and the iron path reluctances $\Re_1$ and $\Re_2$ are defined by:

$$\begin{aligned}
\Re_{g1} &= \frac{d_g}{\mu_0(d_1+d_g)^2} \\
\Re_{g2} &= \frac{d_g}{\mu_0(d_1+d_g)(0.5d_1+d_g)} \\
\Re_1 &= \frac{2d_1}{\mu_c d_1^2} \\
\Re_2 &= \frac{4.5\cdot d_1}{\mu_c 0.5 d_1^2}
\end{aligned}$$

The total reluctance $\Re_{E1}$ of the single phase E-core is given by:

$$\Re_{E1} = \Re_1 + \Re_{g1} + 0.5(\Re_2 + \Re_{g2}) \tag{B.12}$$

Inserting eq. (B.12) and eq. (B.12) into eq. (B.11), and solving for the air-g gives a third-order equation having the following three solutions:

$$\begin{aligned}
d_{g,1} &= S + T - \frac{2.5d_1 - \frac{1.5}{k_1}}{3} \\
d_{g,2} &= -\frac{1}{2}(S+T) - \frac{2.5d_1 - \frac{1.5}{k_1}}{3} + j\frac{\sqrt{3}}{2}(S-T) \\
d_{g,3} &= -\frac{1}{2}(S+T) - \frac{2.5d_1 - \frac{1.5}{k_1}}{3} - j\frac{\sqrt{3}}{2}(S-T)
\end{aligned} \tag{B.13}$$

where the constants k_1, Q, R, S and T are given by:

$$\begin{aligned}
k_1 &= \frac{\mu_0 N_t \sqrt{2}\hat{I} - 6.5 d_1 \hat{B}_c \frac{\mu_0}{\mu_c}}{d_1^2 \hat{B}_c} \\
Q &= \frac{6d_1^2 - \frac{3d_1}{k_1}}{9} \\
R &= \frac{9\left(\left(2.5d_1 - \frac{1.5}{k_1}\right)\left(2d_1^2 - \frac{d_1}{k_1}\right)\right) - 27\left(\frac{d_1^3}{2}\right) - 2\left(2.5d_1 - \frac{1.5}{k_1}\right)^3}{54} \\
S &= \sqrt[3]{R + \sqrt{Q^3 + R^2}} \\
T &= \sqrt[3]{R - \sqrt{Q^3 + R^2}}
\end{aligned}$$

Single phase UI-core

For the single phase UI-core, the reluctance of the air g $\Re_{g1}$ and the iron path reluctance $\Re_1$ is given by:

$$\begin{aligned}
\Re_{g1} &= \frac{d_g}{\mu_0(d_1+d_g)^2} \\
\Re_1 &= \frac{12d_1}{\mu_c d_1^2}
\end{aligned} \tag{B.14}$$

The total reluctance $\Re_{U1}$ of the single phase UI-core is given by:

$$\Re_{U1} = \Re_1 + 2\Re_{g1} \tag{B.15}$$

Substituting eq. (B.14) and eq. (B.15) into eq. (B.11) and solving for air-g length gives:

$$d_g = \frac{-\left(2d_1 - \frac{2}{k_1}\right) \pm \sqrt{\left(2d_1 - \frac{2}{k_1}\right)^2 - 4d_1^2}}{2} \tag{B.16}$$

where k_1 is given by:

$$k_1 = \frac{\mu_0 N_t \hat{I} - \left(\frac{\sqrt{72}\mu_0 d_1 \hat{B}_c}{\mu_c}\right)}{\sqrt{2} d_1^2 \hat{B}_c} \tag{B.17}$$

Three phase EI-core

Assuming that the reluctance in the yoke is negligible ($\Re_y = 0$) the three phase EI-core can be considered as three single phase UI-cores having the reluctances defined as:

$$\begin{aligned} \Re_1 &= \frac{4d_1}{\mu_c d_1^2} \\ \Re_{g1} &= \frac{d_g}{\mu_0 (d_1 + d_g)^2} \end{aligned} \tag{B.18}$$

$$d_g = \frac{-\left(2d_1 - \frac{1}{k_1}\right) \pm \sqrt{\left(2d_1 - \frac{1}{k_1}\right)^2 - 4d_1^2}}{2} \tag{B.19}$$

where k_1 is given by:

$$k_1 = \frac{\mu_0 N_t \hat{I}\sqrt{2} - \left(\frac{4\mu_0 d_1 \hat{B}_c}{\mu_c}\right)}{d_1^2 \hat{B}_c} \tag{B.20}$$

Three phase EE-core

Assuming that the reluctance in the yoke is negligible ($\Re_y = 0$) the three phase EI-core can be considered as three single phase UI-cores having the reluctances defined as:

$$\begin{aligned} \Re_1 &= \frac{8d_1}{\mu_c d_1^2} \\ \Re_{g1} &= \frac{d_g}{\mu_0 (d_1 + d_g)^2} \end{aligned} \tag{B.21}$$

$$d_g = \frac{-\left(2d_1 - \frac{1}{k_1}\right) \pm \sqrt{\left(2d_1 - \frac{1}{k_1}\right)^2 - 4d_1^2}}{2} \tag{B.22}$$

where k_1 is given by:

$$k_1 = \frac{\mu_0 N_t \hat{I}\sqrt{2} - \left(\frac{8\mu_0 d_1 \hat{B}_c}{\mu_c}\right)}{d_1^2 \hat{B}_c} \tag{B.23}$$

B.3.3 Number of turns

Having the reluctance of the considered core (which in turn involves the number of turns), the number of turns N_t: can be calculated, c.f. eq. (B.6):

$$N_t = \sqrt{L \cdot \Re} \tag{B.24}$$

where $\Re$ is the reluctance of the magnetic flux path. The reluctance of a magnetic flux path is given by:

$$\Re = \frac{l}{\mu A} \tag{B.25}$$

where μ is property constant of the considered medium l is the length of the flux path and A is the equivalent cross-sectional area of the flux path.

B.3.4 Loss mechanisms

In the recursive inductor design procedure it is crucial to determine the losses of a given design. The following losses are included in the design procedure:

- Copper losses
- Hysteresis losses (major and minor loops)
- Eddy current losses

Hence the total inductor losses P_L are modeled by:

$$P_L = P_{cu} + P_{hy} + P_{ed} \tag{B.26}$$

where P_{cu} is the copper losses, P_{hy} are the hysteresis losses, and P_{ed} represent the eddy-current losses. The succeeding three sections presents the modeling of the three considered loss mechanisms.

Copper losses

The copper losses in the inductor are due to the effective resistance R_L of the windings.

$$P_{cu} = R_L I^2 \tag{B.27}$$

At DC-considerations, the resistance of the winding is determined by:

$$R_{cu} = \frac{l_{cu}}{\sigma_{cu} \cdot A_{cu}} \tag{B.28}$$

where l_{cu} is the length of the copper winding and A_{cu} is the cross-sectional area of the winding. However, the conductivity σ_{cu} is a temperature dependent material property factor which for copper is given by [2]:

$$\sigma_{cu} = \frac{\sigma_{cu,20}}{(1 + 0.00393(T - 20))} \qquad [1/(\Omega\text{m})] \tag{B.29}$$

where T is the actual winding temperature in degrees Celsius. Further complications occur when the inductor current becomes time varying. The time-varying currents produces an alternating magnetic field which in turn generates eddy currents in the winding which tends to shield the interior of the winding from the carrying current, resulting in an increased current density at the exterior of the winding [5]. the skin depth δ_{skin} is used. The skin depth is defined by:

$$\delta_{skin} = \sqrt{\frac{1}{\pi \cdot f \cdot \mu_{cu} \cdot \sigma_{cu}}} \tag{B.30}$$

where μ_{cu} is the permeability of copper[1] and f is the frequency of the inductor current. Considering only the fundamental of the inductor current, the skin depth becomes 10.6 mm. For rectangular conductors with a thickness d_{cu} the consequences of the skin effect can be neglected if the following inequality is satisfied [5]:

$$d_{cu} \leq 2 \cdot \delta_{skin} \tag{B.31}$$

In the actual inductor design, conductors which satisfy eq. (B.31) will be used and hence the skin effect can be omitted in the calculation of the effective winding resistance. Hence the copper losses in the actual inductor design is calculated by eq. (B.27), eq. (B.28) and eq. (B.29).

Hysteresis losses

The empirical Steinmetz equation expresses the specific hysteresis loss as an exponential function of the frequency f and the maximum flux density $\hat{B}_c$. Provided that the magnetizing current is purely sinusoidal the hysteresis loss can be expressed by:

$$P_{hy} = c_m \cdot f^{\alpha} \cdot \hat{B}_c^{\beta} \tag{B.32}$$

where c_m, α and β are material property constants. Despite, the formula in eq. (B.32) is a well established expression for the hysteresis losses, manufactures of iron cores rather provide graphical presentation of the loss characteristic than providing the material property constants. Further, eq. (B.32) only applies for a sinusoidal magnetizing current at a given core temperature[2]. Hence the calculation of the hysteresis losses in the inductor involves the following two steps:

- Extraction of the parameters c_m, α and β.

[1]The permeability of copper is [7]: $\mu_{cu} = \mu_0(1 - 0.98e^{-5})$.

[2]Due to insufficient data sheet information, the temperature dependence of the core losses is neglected.

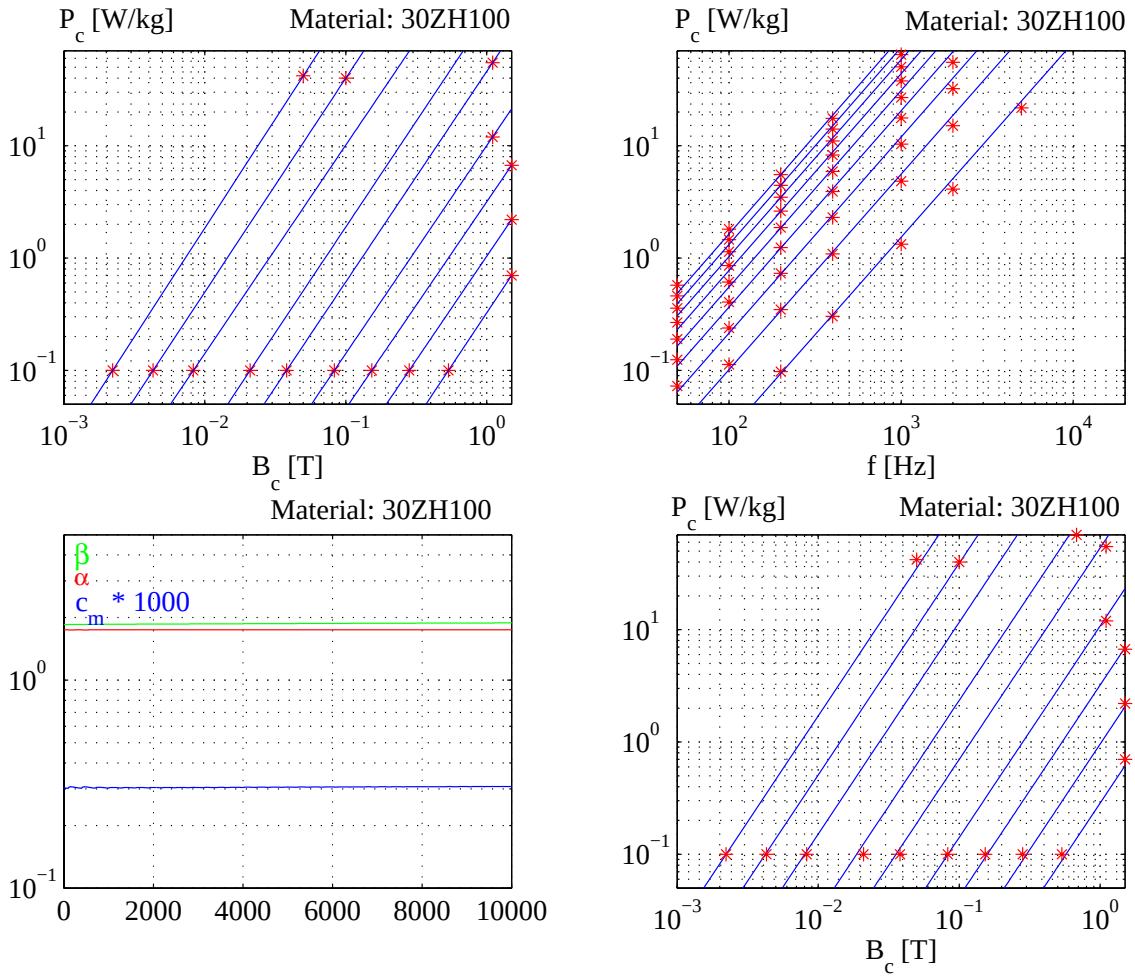

Figure B.2: *Extraction of hysteresis loss parameters.* **a)** *Reproduction of data sheet information. Losses vs. induction* **b)** *Reproduction of data sheet information. Losses vs. frequency.* **c)** *Convergence of the parameters c_m, α and β using the least square regression model.* **d)** *Model validation.*

- Extension of eq. (B.32) to account for arbitrary magnetizing currents.

The extraction of the three material property constants is based on the approach described in [6] while the extension of basic Steinmetz equation is described in [1].

Fig. B.2a shows a reproduction of the specific core loss as a function of the induction, plotted for the frequency range 50 Hz to 20 kHz.
Using the least square regression method [8], on the data in Fig. B.2a and Fig. B.2b the values for c_m, α and β can be extracted. The convergence of the least square regression method is depicted in Fig. B.2c.

$$P_{hy} = 3.026e^{-4} \cdot f^{1.749} \cdot \hat{B}_c^{1.891} \tag{B.33}$$

Fig. B.2 shows the hysteresis losses calculated by the extracted model (-) along with the data from the data sheet (*).

The core loss model given by eq. (B.33) only applies for sinusoidal exitation currents and to account for non-sinusoidal waveforms and sub-hysteresis loops, the model has to be extended. Based on the actual shape of the flux density, [6] suggests to determine an equivalent frequency $f_{sin,eq}$, given rise to the same hysteresis losses as obtained by the original signal. The equivalent frequency is determined by:

$$f_{sin,eq} = \frac{2}{\pi^2} \sum_{n=2}^{N} \left(\frac{B(n) - B(n-1)}{B_{max} - B_{min}} \right)^2 \cdot \frac{1}{t(n) - t(n-1)} \tag{B.34}$$

Thus the specific hysteresis power losses for an arbitrary magnetizing current becomes:

$$P_{hy} = \frac{1}{T} c_m \cdot f_{sin,eq}^{\alpha-1} \cdot B^{\beta} \tag{B.35}$$

where T is the time period of the original signal.

Eddy current losses

To account for the eddy current losses the empirical Steinmetz equation is used:

$$P_{ed} = \frac{\sigma_c \cdot \tau}{12\rho_c} \left(\frac{dB}{dt} \right)^2 \qquad [W/kg] \tag{B.36}$$

where σ_c is the conductivity of the core material, τ is the thickness of the lamination and ρ_c is the mass density of the iron.

B.3.5 Temperature considerations

At steady state temperature considerations, the relation between the power losses in the inductor and the inductor-to-ambient temperature ΔT can be expressed by:

$$\Delta T = R_{\Theta ia} P_c \tag{B.37}$$

where $R_{\Theta ia}$ is the inductor to ambient heat transfer resistance. Unfortunately, the heat transfer resistance is a quite complex function, depending on temperature, cooling method, surface area and surface characteristics. Hence the main difficulty of this approach is to determine a reasonable expression for the heat transfer resistance. In this inductor design, a relatively simple approach is used where it is assumed that the inductor is cooled only by convective and radiative heat transfer, i.e. the air circulation around the inductor is only due to natural air circulation caused by the heating of the air in proximity of the inductor. Further, it is assumed that the inductor is a homogeneous body with a smooth, closed, and black[3] surface.

[3] In the design of the inductor, emissivity constant is assumed to be 0.9 which holds for a black body [5]

Convective heat transfer

The convective heat transfer is modeled by [3]:

$$P_{conv} = 13.5 \cdot A_s \Delta T \tag{B.38}$$

where ΔT is the difference between the inductor temperature and the ambient temperature and A_s is the surface area of the designed inductor For design purposes the thermal resistance $R_{\Theta conv}$ due to convective heat transfer is found by combining eq. (B.37) and eq. (B.38):

$$R_{\Theta conv} = \frac{1}{13.5 \cdot A_s} \tag{B.39}$$

Radiative heat transfer

The power P_{rad} emitted by radiation is modeled by the Stefan-Boltzmann law [5]:

$$P_{rad} = 5.7 \cdot E \cdot A_s \left(\left(\frac{T_c}{100} \right)^4 - \left(\frac{T_a}{100} \right)^4 \right) \tag{B.40}$$

where E is the emissivity of the surface, T_s and T_a is the conductor temperature and the ambient temperature measured in Kelvin. Combining eq. (B.37) and eq. (B.40), the thermal resistance $R_{\Theta rad}$ due to radiative heat transfer becomes:

$$R_{\Theta rad} = \frac{1}{5.7 \cdot E \cdot A_s \left(\left(\frac{T_c}{100} \right)^4 - \left(\frac{T_a}{100} \right)^4 \right)} \tag{B.41}$$

Thermal resistance

By the approach described above, the total thermal resistance $R_{\Theta ia}$ including both the radiative and the convective heat transfer is determined by:

$$R_{\Theta ia} = \frac{R_{\Theta conv} \cdot R_{\Theta rad}}{R_{\Theta conv} + R_{\Theta rad}} \tag{B.42}$$

B.4 Iterative design algorithm

Fig. B.3 shows the algorithm used to design the inductances. For each calculation step in the algorithm, the actual equation is cited.

B.5 Core- and wire characteristics

Table I lists the core- and wire characteristics used in the design procedure.

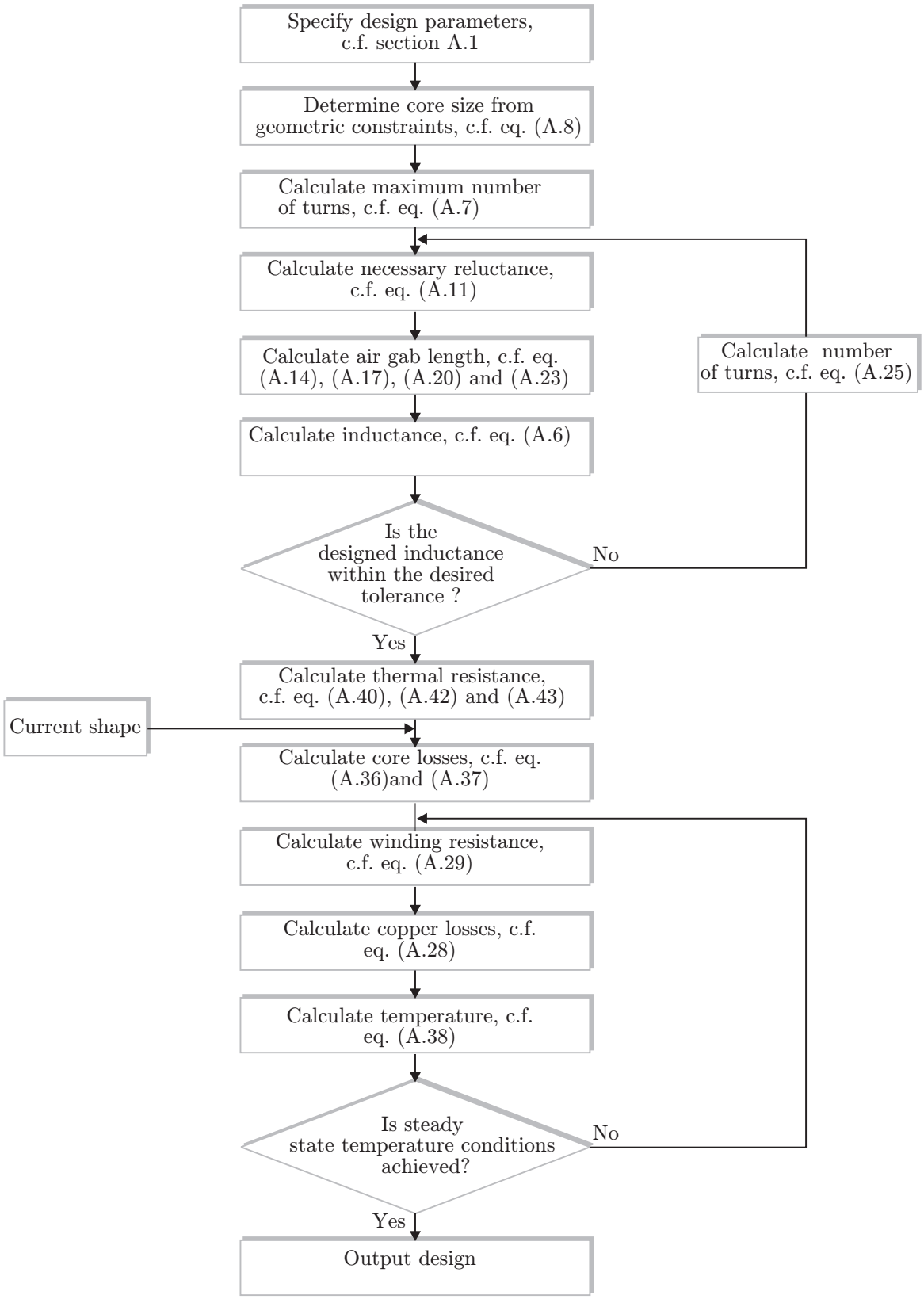

Figure B.3: *Algorithm for inductor design.*

TABLE I: *Design constants*

Description	*Symbol*	*Value*	*Unit*
Permeability of air	μ_0	$4\pi \cdot 10^{-7}$	[H/m]
Permeability of core material	μ_c	0.04	[H/m]
Permeability of copper	μ_{cu}	$\mu_0(1 - 0.98 \cdot 10^{-5})$	[H/m]
Conductivity of copper at 20°C	$\sigma_{cu,20}$	$5.797 \cdot 10^7$	[1/(Ωm)]
Conductivity of core material at 20°C	σ_c	$2 \cdot 10^6$	[1/(Ωm)]
Mass density of core material	ρ_c	7650	[kg/m^3]
Thickness of lamination	τ	$3 \cdot 10^{-4}$	[m]
	c_m	$3.0261 \cdot 10^{-4}$	
	α	1.7492	
	β	1.8910	

B.6 Design results

By use of the above described iterative design procedure, it is possible to design an inductor complying the specifications. Fig. B.4 shows calculated losses for 7 different inductances (0.3mH to 0.6mH stepped by 50μH) as a function of the mass of the inductor. The calculations are repeated for different current densities (1.5 A/mm^2 to 8 A/mm^2). The bold lines corresponds to core designs where the temperature is kept below the maximum allowable temperature while thin lines corresponds to designs which does not comply with the temperature specifications.

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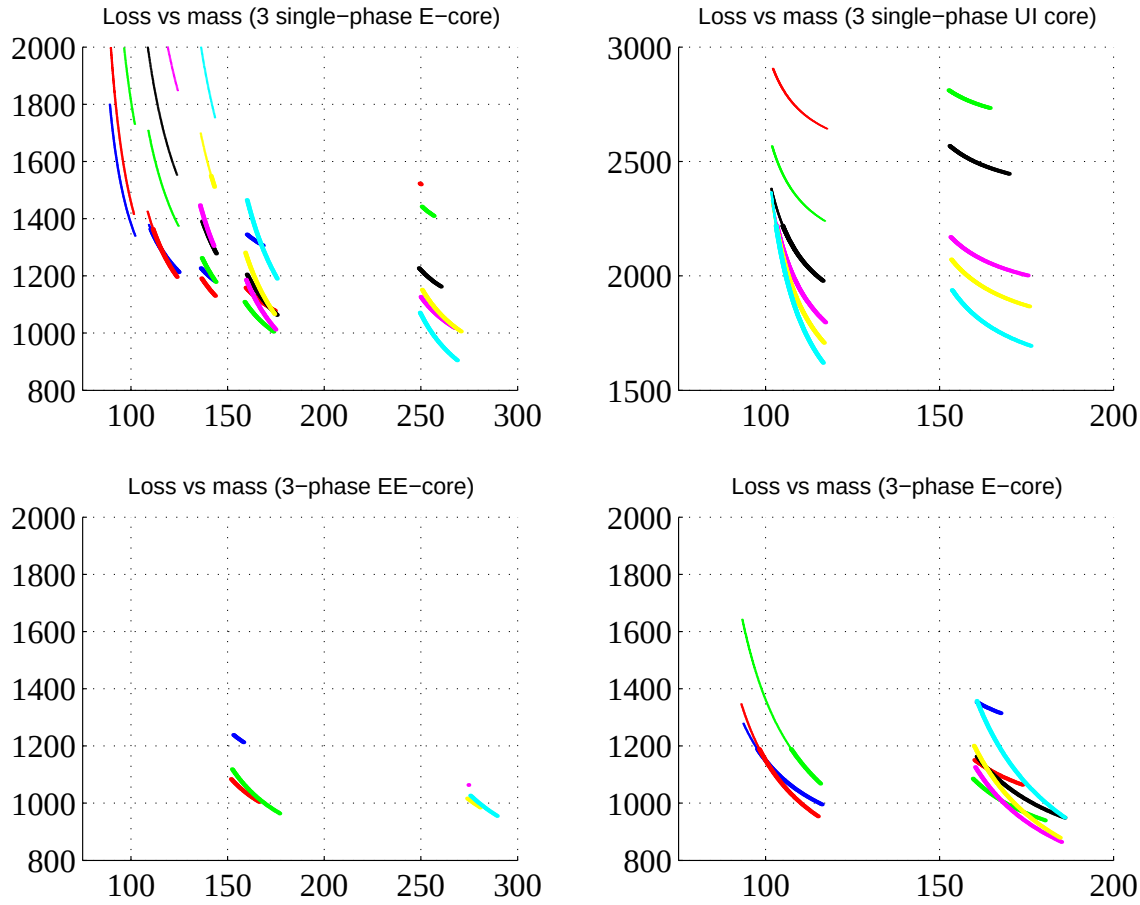

Figure B.4: *Core designs. Losses vs. mass of the three-phase inductor plotted for current densities between 1.5 - 8 A/mm^2.*

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Appendix C

Comparison of Converter Efficiency in Large Variable Speed Wind Turbines, APEC 2001

Comparison of Converter Efficiency in Large Variable Speed Wind Turbines

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Abstract— **This paper presents a new and fast method for evaluating the efficiency of different converter topologies in variable speed wind turbine applications. The method involves an accurate model of the considered generator while the converter models are based on ideal switches. The converter losses are modeled by analytical expressions of the switches, and the description of the losses incorporate both temperature, blocking voltage and switched current. The method is used to evaluate two converter topologies, a two-level back-to-back voltage source inverter (VSI), and a three-level back-to-back VSI for use in a 2MW wind turbine system based on a doubly-fed induction generator (DFIG). From this evaluation it appears that with regards to the efficiency, the two-level VSI is the most suitable solution for the rotor side inverter while at the grid side, both inverter topologies show approximately the same efficiency. The evaluation method is validated by experimental results.**

I. Introduction

Since the mid eighties the world-wide installed wind turbine power has increased dramatically and several international forecasts expect the growth to continue. Supporting these forecasts are a number of national energy programmes which proclaim a high utilization of wind power [1]. So far, the constant speed wind turbine, using the induction generator, has been widely used [2]. However as the ratings of the wind turbines are getting higher and the wind turbines are getting more widespread, a couple of problems with the constant speed wind turbine occurs, which make variable speed constant frequency systems more attractive.

A. Constant speed wind turbines

A.1 Energy capture: A problem concerning the design of a constant speed wind turbine is the choice of a nominal wind speed at which the wind turbine produces its rated power. In general the power transmitted to the hub shaft of the wind turbine is expressed as [3]:

$$P_{tur} = \frac{1}{2} C_p \rho A_v v_{wind}^3 \tag{1}$$

where A_v is the area swept out by the turbine blades, ρ is the air density, v_{wind} is the velocity of the wind and C_p is the power performance coefficient. The power performance coefficient varies considerably for various designs, but in general it is a function of the blade tip speed ratio λ. The problem concerning the energy capture from constant speed wind turbines is visualized in Fig. 1, where the power transmitted to the hub shaft versus rotor speed is plotted for different wind speeds, $v_1 ... v_4$. From Fig. 1 it appears, that at wind speeds above and below the rated wind speed, the energy capture does not reach the maximum available value.

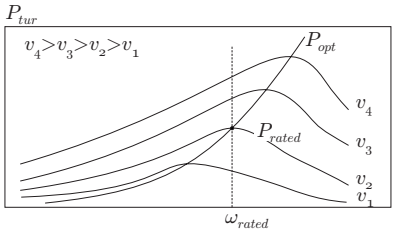

Fig. 1. The power transmitted to the hub shaft at different wind speeds.

A.2 Mechanical stress: Another problem concerning the fixed speed wind turbine is the design of the mechanical system. Due to the almost fixed speed of the wind turbine every fluctuations in the wind power is converted to torque pulsations which cause mechanical stresses. To avoid breakdowns, the drive train and gear-box of a fixed speed turbine must be able to withstand the absolute peak loading conditions and consequently additional safety factors need to be incorporated into the design [4,5].

A.3 Power quality The power generated from a fixed speed wind turbine is sensitive to fluctuations in the wind. Due to the steep speed-torque characteristics of an induction generator, any change in the wind speed is transmitted through the drive train on to the grid [4]. The rapidly changing wind power may create an objectionable voltage flicker. Another power quality problem of the fixed speed wind turbine is the reactive power consumption. To improve the power quality of wind turbines, large reactive components, active as well as passive, are often used to compensate for the reactive power consumption [6].

B. Variable speed wind turbines

Initiated by the disadvantages in the use of constant speed wind turbines described above, the trend in modern wind energy conversion is doubtlessly towards variable speed constant frequency (VSCF) generating systems. However, as the induction generator seems to be the *"defacto standard"* in constant speed wind turbines, no variable speed wind turbine solutions occupy this position at the moment. For example, the German company ENERCON count on a solution based on a direct driven synchronous generator while the Danish company VESTAS uses a doubly-fed induction generator (DFIG). Besides the choice of generator concept, another challenge

in the design of a variable speed wind turbine, is the selection of the most suitable converter topology. One goal for this selection should be, that the gained utilization of the wind energy is not lost in converter losses. This paper evaluates the efficiency of two power converters for use in the doubly-fed induction generator system. The considered power converters are: A two level back-to-back VSI and a three-level back-to-back VSI.

II. The doubly-fed induction generator system

Fig. 2 shows the considered doubly-fed induction generator system along with the definitions of power flow direction. In the system, the converter topology (including the grid filter) is the general design parameter while the characteristics of the generator, the transformer and the rotor side filter are predetermined values. The specifications for the wind turbine system are listed in Table I. A common trait of a converter for use in the doubly-fed induction generator system is, that it has to handle the generated active and reactive rotor power under the conditions specified in Table I.

A. Ratings for the converter

The power transmitted to the utility grid P_{sys} is the sum of the stator power P_s and the rotor power P_r, provided that the converter is loss less, i.e. $P_g = P_r$:

$$P_{sys} = P_s + P_r \tag{2}$$

Similar, the reactive power transmitted to the utility grid is the sum of the reactive power generated by the stator Q_s and the reactive power generated by the grid inverter Q_g:

$$Q_{sys} = Q_s + Q_g = 0 \tag{3}$$

As indicated in (3) the generated reactive power is controlled to zero and in steady-state operation, the two components Q_s and Q_g both equals zero. The only control parameter available to satisfy (3) is the rotor voltage. To determine the rotor voltage, the equation set for the electrical part of the generator is used. By a power invariant transformation of the phase quantities of the DFIG into the stationary two-axis frame the following equation set is obtained.

$$\begin{bmatrix} v_s \\ v_r \end{bmatrix} = \begin{bmatrix} -R_s - pL_s & -pL_m \\ (\omega_r - p)L_m & -R_r + (\omega_r - p)L_r \end{bmatrix} \begin{bmatrix} i_s \\ i_r \end{bmatrix} \tag{4}$$

where p is the time derivative operator, R_s is the stator resistance, R_r is the rotor resistance, L_m is the magnetizing inductance, L_r is the rotor inductance, L_s is the stator inductance and ω_r is the rotational speed in electrical

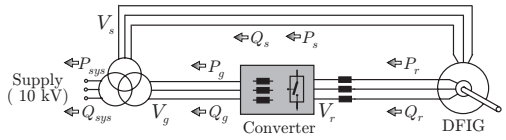

Fig. 2. The considered doubly-fed system.

TABLE I
Ratings for the system.

Nom. Speed	$\omega_{r,nom}$	1500 ± 12%	[rpm]
Dyn. slip[1]	s_{dyn}	30%	
Nom. power	P_{sys}	2.0	[MW]
Stator phase voltage	V_s	398	[V]
Grid phase voltage	V_g	277	[V]
Rotor side filter	L_r	60	[μH]
Gen. wind. ratio	n	2.63	

[1] Only for super synchronous speed.

measure. Hence, the active and reactive power equals:

$$P_s = \Re e(v_s \cdot i_s^*) \tag{5}$$
$$Q_s = \Im m(v_s \cdot i_s^*) \tag{6}$$
$$P_r = \Re e(v_r \cdot i_r^*) \tag{7}$$
$$Q_r = \Im m(v_r \cdot i_r^*) \tag{8}$$

where i_x^* denotes the complex conjugate of the quantity i_x. The $\Re e(\cdot)$ and $\Im m(\cdot)$ represents the real and imaginary part of the argument. Solving (2), (3) and (4) in steady-state conditions for a total power, P_{sys}, of 2 MW it is found that the converter have to be designed to the following conditions:

$$\hat{V}_r = 324 \text{ V} \tag{9}$$
$$\hat{I}_r = 774 \text{ [A]} \tag{10}$$
$$\hat{I}_g = 328 \text{ [A]} \quad (555 \text{ [A] for 1 minute}) \tag{11}$$

where $\hat{V}_r$ is the demanded rotor phase voltage (RMS) at 30% super-synchronous speed, $\hat{I}_r$ is the maximum rotor phase current (RMS) occurring at 12% sub-synchronous speed and $\hat{I}_g$ is the maximum RMS grid current occurring at 12% sub-synchronous speed.

B. Converter harmonic performance

In the design of the grid inverter for the doubly-fed induction generator the total harmonic current distortion THD_i, defined by:

$$THD_i = \sqrt{\sum_{h \neq 1} \left(\frac{I_h^2}{I_1^2} \right)} \tag{12}$$

will be limited to 5% at full load steady state. By this, the allowable harmonic RMS current becomes 16.4 A. Since the harmonic flux distortion $\tilde{\psi}_{RMS}$ [7] rather than the harmonic current is used as a design parameter for the grid side inverter, the design guide lines for the grid side inverter becomes:

$$\tilde{\psi}_{RMS} = \frac{I_h}{L_g} \tag{13}$$

where L_g is the inductance of the grid side filter. At the rotor side of the converter, a harmonic flux distortion of maximum 14 [mWb] will be allowed.

III. Power converter topologies

Fig. 3 shows the two considered power converters, the two-level back-to-back VSI and the three-level back-to-back VSI. In order to evaluate the efficiency of the two

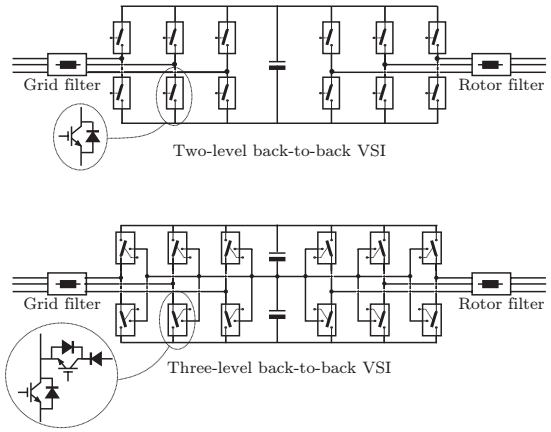

Fig. 3. The considered converter topologies.

converter topologies when used in the considered wind turbine system, some preliminary design considerations are to be made concerning the components which are believed to influence the losses of the converter system. The considered components are:

- Switching devices.
- Filters.
- Modulation strategies.

In the evaluation, the losses due to the series resistance of the DC-link capacitor(s) is neglected.

A. Back-to-back VSI

A.1 Design: From the design criteria specified in (9) the DC-link voltage of the two-level back-to-back VSI is fixed to 800 V (in this choice it is presumed that the converter are able to utilize the full DC-link voltage). Further, at this DC-link voltage, the grid filter inductance L_g is limited by the magnitude of the maximum grid current, c.f (11), given by:

$$L_g \leq \sqrt{\frac{\hat{V}_{gi}^2 - V_g^2}{(\omega_g \cdot I_g)^2}} \tag{14}$$

where $\hat{V}_{gi}$ is the maximum RMS grid inverter voltage. At a 10% increased grid voltage, a total power of 2MW and a speed 30% above synchronous speed the grid inductor is limited to a value below 0.7 mH. In the present case study, a 0.4 mH grid inductance is to be used. Regarding the switches of the two-level back-to-back VSI, the selection is limited to switches based on the SKiiP®-technology provided by `SEMIKRON`. For each leg in the two-level rotor side inverter two paralleled single phase bridges of type `SkiiP942GB120` is used. At the grid side, a single module, type `SkiiP942GB120`, per phase ensures the current capability specified by (11).

A.2 Modulation strategies and switching frequencies: Among the modulation schemes presented in the literature during the past, the following four are considered for use in the two-level grid side inverter and the two-level rotor side inverter.

- Space vector PWM (SVPWM) [8].

TABLE II
Designed switching frequencies for the two-level back-to-back VSI

	Grid side inv. ($0.84 < M_i < 1$)	Rotor side inv. ($0 < M_i < 0.4$)
SVPWM	4300 [Hz]	1300 [Hz]
DPWM0	4900 [Hz]	2450 [Hz]
DPWM1	5000 [Hz]	2500 [Hz]
DPWM2	4900 [Hz]	2450 [Hz]

- Discontinuous shifted left PWM (DPWM0) [10].
- Discontinuous centered PWM (DPWM1) [9].
- Discontinuous shifted right PWM (DPWM2) [10].

Evaluating these four modulation methods with regards to the RMS harmonic flux distortion $\tilde{\psi}_{RMS}$ and designing the switching frequency to meet the specified harmonic demands, the switching frequencies listed in Table II is obtained. Then, evaluating the switching losses of the different modulation methods (at the designed switching frequencies) it is possible to choose the most efficient modulation method. As example, regarding the two-level rotor inverter: With reference to Fig. 4, considering the switching losses as a function of the inverter load angle ϕ_r and comparing with the actual load angles for the rotor circuit of the generator it appears, that in general, the SVPWM is the most suitable modulation strategy with regards to the switching losses of the rotor inverter. The right part of Fig. 4 shows the normalized switching losses P_{sw} of the different modulation strategies as a function of the load angle ϕ_r (normalized to the switching losses of the continuous modulator (SVPWM)). The left part of Fig. 4 shows the load angles of the rotor inverter plotted against the absolute slip value. The different load angle curves correspond to different levels of total power (the load angle approaches -90° as the total power decreases). Applying the same procedure for the grid inverter, it appears that the discontinuous modulation scheme DPWM1 is the most applicable among the considered modulation schemes.

B. Three-level back-to-back VSI

From Fig. 3 it appears that the preferred switch configuration for the three-level converter suffers from the advantage of normal multi-level structures in which the voltage ratings for all the switches can be derated. In the considered topology, the switches connected to the upper and lower DC-bus have to be rated to the full DC-link voltage while the switches connected to the DC-link cen-

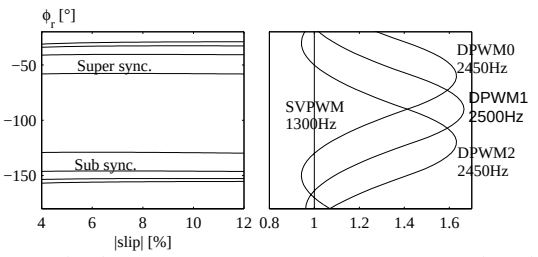

Fig. 4. (Left) The load angle for the rotor side inverter. (Right) The normalized losses of the considered modulation strategies as a function of the load angle

TABLE III
DESIGNED SWITCHING FREQUENCIES FOR THE THREE-LEVEL BACK-TO-BACK VSI

	Grid side inv. $(0.84 < M_i < 1)$	Rotor side inv. $(0 < M_i < 0.4)$
SVPWM1	2000 [Hz]	650 [Hz]
SVPWM2	2000 [Hz]	750 [Hz]

ter point can be rated to half the DC-link voltage. An advantages of the present topology is that only one switch is in the current path whenever the output of the converter is clamped to either the upper or the lower DC-bus (contrary to the conventional diode clamped three-level converter [11] where two switches form the conducting path). Another salient feature of the three-level topology in Fig. 3 is that the single phase `SkiiPPACK` modules from `SEMIKRON` are applicable (these modules include a complete gate drive circuit).

B.1 Design: For the three-level converter, the same conditions as for the two-level converter apply with regard to the magnitude of the DC-link voltage and the size of the grid inductance. Hence the total DC-link voltage is fixed to 800 V and the grid filter inductance is chosen to 0.4 mH. For the rotor side inverter, 12 half bridge-modules (two in parallel), type `SKiiP942GB120` along with 18 additional diodes, type `SKKD90F06` ensures the current capability in (10) while six modules, type `SKiiP642GB120` along with 12 diodes, type `SKKD90F06` form the three-level grid inverter.

B.2 Modulation strategies and switching frequencies: Unlike the two-level back-to-back VSI, where the redundancy of the zero vectors can be dedicated to switching loss reduction (the discontinuous modulators), the redundancy of the switch-states in the three-level converter has to be attributed to DC-link neutral potential stabilization. For the present application, only modulation strategies which are able to stabilize the DC-link voltage in each switching cycle are considered. Actually, those to be treated are:

- Space vector PWM1 (SVPWM1)[1].
- Space vector PWM2 (SVPWM2)[1] [12].

Designing both modulation methods to meet the prerequested harmonic performance criteria, the switching frequencies can be calculated to the values in Table III. Similar to the procedure for the two-level converter, the switching losses of the two modulation schemes are calculated for the actual load conditions, and the most efficient modulator is chosen. For both the grid side inverter and the rotor side inverter, the method denoted SVPWM2 is the most efficient, although the SVPWM1 method allows lower switching frequency in the rotor inverter, c.f. Table III

[1]Due to some confusion in the names of modulation schemes for the three-level converter, appendix II is dedicated to a brief presentation of the two methods in order to clarify the differences.

IV. LOSS MODELING

A. Semiconductor loss description:

In the efforts of determining the converter efficiencies, an appropriate transistor loss model are to be used. Several approaches are described in the literature [13-16], ranging from simple conducting loss models to complex and simulation time consuming semiconductor models. In this paper it is chosen to use a method based on an analytical formulation of the losses. It is assumed that the semiconductor losses can be modeled by [17]:

$$p_T = u_{Th,T}(T_j, u_T) \cdot i_T + R_T(T_j, u_T) \cdot i_T^2 + k_{sw}(T_j, u_{sw}) \cdot \bar{i}_{sw} \cdot \tilde{f}_{sw} \quad (15)$$

$$p_D = u_{Th,D}(T_j, u_D) \cdot i_D + R_D(T_j, u_D) \cdot i_D^2 + k_{rr}(T_j, u_{sw}) \cdot \bar{i}_{sw} \cdot \tilde{f}_{sw} \quad (16)$$

where $u_{Th,x}$ is the threshold voltage for the transistor and diode as a function of the device junction temperature T_j and blocking voltage u_x, R_x is the device resistance, k_{xx} is a switching loss function, i_x is the device current, $\bar{i}_{sw}$ is the switched current and $\tilde{f}_{sw}$ is the number of switchings per second for the considered device.

A.1 Parameter extraction: One method for deriving the parameters in (15) and (16) is to use the test system described in [14]. However, in this paper it is chosen to limit the considered switches to the `SkiiPPACK` modules from `SEMIKRON`, and hence the designing tool `SKiiPselect` provided by the manufacturer can be used to derive the parameters. As example, Fig. 5 shows the derived losses (per switch) in an H-bridge equipped with the module `SkiiP642GB120`. The junction temperature is kept at 100°C and the DC-link voltage is 400 V. The losses in Fig. 5 is shown as a function of modulation function m and the output current I_o from the H-bridge. From the loss modeling approaches described by (15) and (16) and by use of a least square regression model [18], the model parameters can be extracted from the losses in Fig. 5. Repeating the procedure for other combinations of the DC-link voltage and device junction temperature, a temperature- and blocking voltage dependent switch model is obtained.

A.2 Device parameters: Applying the least square regression model, c.f. appendix I, on the derived loss arrays, the model parameters are derived. Table IV lists the derived transistor parameters and Table V the corresponding diode parameters. For the additional diodes in the three-level structure, the data sheet loss parameters are used.

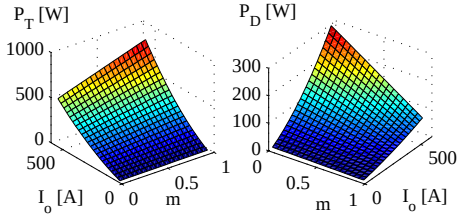

Fig. 5. Transistor- and diode losses.

TABLE IV

SEMICONDUCTOR LOSS MODELS (TRANSISTORS).

	942GB120[1]	942GB120[2]	642GB120[3]
$U_{th,T}$ [V]	$2.0e^{-3}T_j+1.24$	1.44	1.44
R_T [mΩ]	$3.2e^{-3}T_j+1.72$	2.0	3.08
k_{sw} [μs]	$0.65T_j+350$	$1.9e^{-4}u_T^2+0.37u_T$	179

TABLE V

SEMICONDUCTOR LOSS MODELS (DIODES).

	942GB120[1]	942GB120[2]	642GB120[3]
$U_{th,D}$ [V]	$-3.2e^{-3}T_j+1.40$	1.08	1.08
R_D [mΩ]	$7.9e^{-4}T_j+1.25$	1.32	1.97
k_{rr} [μs]	$8.8e^{-2}T_j+4.29$	$0.66u_T-2.3e^{-6}u_T^2$	26.5

[1] Temperature dependent model, Blocking voltage equals 800 V.

[2] Voltage dependent model, junction temperature equals 100°.

[3] Blocking voltage at 400 V, and junction temperature at 100°.

B. Filter loss description

The losses in the filters (grid side and rotor side inductance) are modeled by an equivalent series resistance. The resistance value for the two considered inductors are calculated by

$$R_L = \frac{P_{RL}}{\sum(I_h^2)} \tag{17}$$

where P_{RL} is the inductor losses specified by the manufacturer at a given harmonic current spectra I_h.

V. SIMULATION MODEL

The method used to simulate the losses of the different converter systems is illustrated on Fig. 6. The method is based on a dynamic model of the doubly-fed induction generator, an ideal model of the converter (including grid filter and modulator(s)) and the switch model(s). The simulation platform used in the presented approach is `PSIM` provided by `PowerSimTech`.

VI. RESULTS

A. Verification of the loss prediction method

To validate the loss prediction method, measurements were performed on a 2 MW test-setup based on a two-level back-to-back VSI. The measurements were obtained by use of a `NORMA D61000` power analyzer measuring the power at both the grid side and the rotor side of the converter simultaneously, (The measurements include the losses of the rotor filter and the grid filter). Fig. 7 shows the measured losses of the 2 MW test-setup (indicated with marks △ and ▷). In order to be able to simulate the converter at the same operating conditions, the switching device temperature along with the grid voltage was recorded for each of the measurements. Supporting the developed simulation model with the characteristics of the test setup (modulation strategies, switching frequencies, switching device characteristics, grid voltages, device temperatures and filter characteristics), the losses of the test setup were simulated. The solid lines in Fig. 7 represents the simulated losses of the converter.

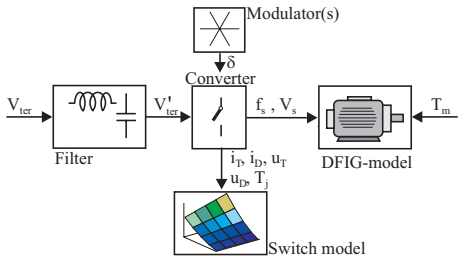

Fig. 6. Illustration of the simulation method.

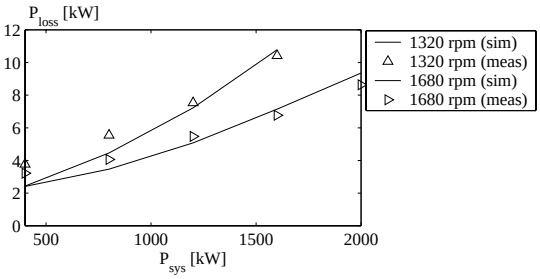

Fig. 7. Measured and simulated losses for a 2 MW test setup.

B. Simulated losses in the two-level back-to-back VSI

Fig. 8 shows the simulated losses of the grid side two-level VSI. The upper left part (UL) shows the switching losses of the grid inverter and the upper right part (UR) shows the conducting losses of the grid inverter. The lower left part (LL) shows the losses in the grid side filter and the lower right part (LR) shows the total grid inverter losses (including filter losses). Fig. 9 shows the simulated losses associated with the operation of the rotor side inverter of the two-level back-to-back VSI. The (UL) shows the total switching losses in the rotor side inverter, (UR) shows the conducting losses of the rotor side inverter and (LL) shows the losses in the rotor side filter. The total losses of the

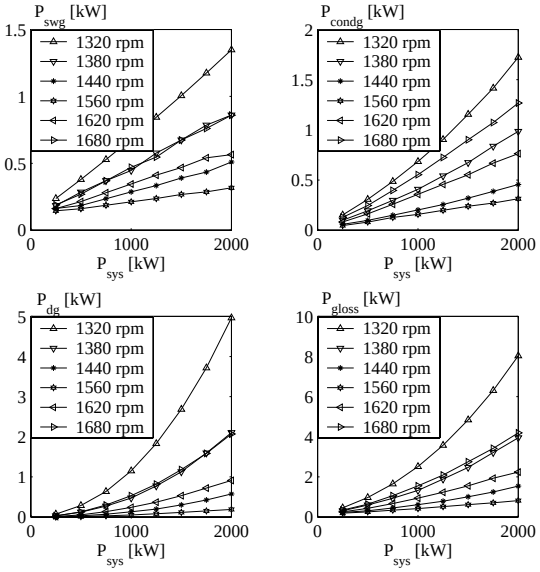

Fig. 8. Simulated losses of the grid inverter of the two-level back-to-back VSI.

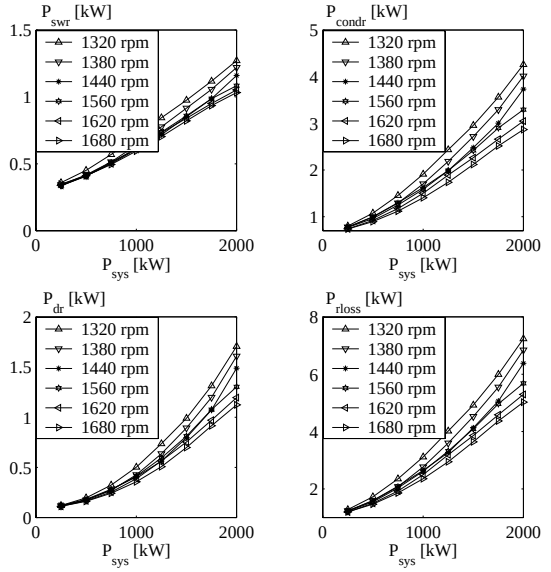

Fig. 9. Simulated losses of the rotor inverter of the two-level back-to-back VSI.

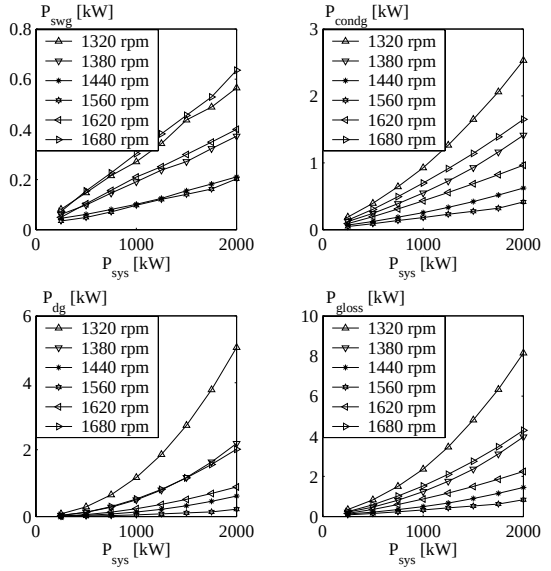

Fig. 10. Simulated losses of the grid inverter of the three-level back-to-back VSI.

rotor side two-level VSI is shown in the (LR) of Fig. 9.

C. Simulated losses in the three-level converter

Fig. 10 shows the simulated losses of the grid side three-level VSI. The (UL) shows the total switching losses of the grid inverter and the (UR) shows conducting losses. The (LL) shows the losses in the grid side filter and (LR) shows the total grid inverter losses of the three-level structure (including filter losses). Fig. 11 shows the simulated losses associated with the operation of the rotor side inverter of the three-level back-to-back VSI. The (UL) shows the switching total losses of switches in the rotor side inverter, (UR) shows the conducting losses of the rotor side inverter

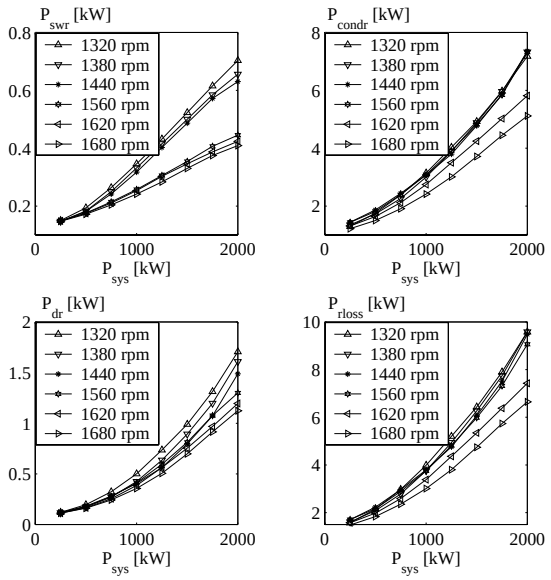

Fig. 11. Simulated losses of the rotor inverter of the three-level back-to-back VSI.

and (LL) shows the losses in the rotor side filter. The total losses of the rotor side three-level VSI is shown in the (LR) of Fig. 11.

VII. Discussion

Comparing the simulated results for the converter losses of the two-level back-to-back VSI and the three level back-to-back VSI it appears that the back-to-back VSI, totally considered, has the lowest losses. A more detailed study of the losses gives, that the switching losses of the three-level converter is lower than the two-level back-to-back VSI but the conducting losses are very dominant. Comparing the grid inverters and the rotor inverters of the two considered topologies independently, it appears that the two-level rotor inverter is significantly more efficient that the three-level rotor inverter. However, comparing the grid side inverters, it appears that the total losses are more or less equal and that the dominant loss contribution for both inverters arises from the grid filter. Since the switching losses of the three-level structure are quite small, it is believed that the total grid inverter losses could be reduced by increasing the switching frequency and then reduce the grid filter inductor.Hence from the analysis performed in this paper it is proposed to use a combination of the two- and three-level structure, i.e. a three-level structure at the grid side and a two-level structure at the rotor side.

VIII. Conclusion

This paper has presented a method for evaluating the power losses of converter topologies for use in variable speed wind turbines. The method is based on a switch model of the converter using ideal switches, an analytical (or a look up-table) description of the device losses, a generator model and modulator(s) for the converter. The loss prediction method is validated by measurements

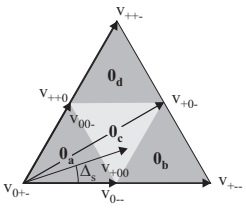

Fig. 12. Segment 0 of the space vector hexagon for the three level converter.

on a 2MW test setup, and it is concluded that the loss-prediction method shows quite good accuracy. In the present work, the loss prediction method is used to evaluate the efficiency of two converter topologies for use in a system based on the doubly-fed induction generator. The considered converter topologies are a two-level back-to-back VSI, and a three-level back-to-back VSI. It is found that the back-to-back VSI, totally considered, is the most efficient among the two topologies.

IX. Acknowledgment

The authors would like to thank Vestas Wind System A/S, Denmark for providing the necessary test equipment and facilities. In particular, thanks to Björn Andresen (Vestas Wind Systems, Denmark) for his kindly support during the experimental measurements.

Appendix

I. Least Square regression model for switch model parameters

As an example, the least square regression model for deriving the diode parameters is shown below. Input to the regression model is, besides the diode loss model, the diode losses P_D, the diode RMS conducting current I_D, the diode average conducting current $\overline{I}_D$, the average switched current $\overline{i}_{sw}$ and the number of switchings per fundamental $\tilde{f}_{sw}$.

for $k = 1 : N$

$\quad \underline{\phi} = \begin{bmatrix} \overline{I}_D(k) & I_D^2(k) & \tilde{f}_{sw}\overline{i}_{sw} \end{bmatrix}^T$

$\quad \underline{\underline{G}} = \underline{\underline{G}} + \underline{\phi} P_D$

$\quad \underline{\underline{R}} = \underline{\underline{R}} + \underline{\phi}\,\underline{\phi}^T$

$\quad$ **if** $det(\underline{\underline{R}}) \neq 0$

$\quad\quad \theta = \underline{\underline{R}}^{-1}\underline{\underline{G}}$

$\quad$ **end**

end

$U_D = \theta(1) \quad R_D = \theta(2) \quad k_{rr} = \theta(3)$

II. Modulation strategies for the three-level converter.

The half of the sector dependent switching sequence for the SVPWM1 is shown in (18) - (21)

$$\mathbf{0_a} \quad v_{0--} \longrightarrow v_{00-} \longrightarrow v_{000} \longrightarrow v_{+00} \longrightarrow v_{++0} \tag{18}$$

$$\mathbf{0_b} \quad v_{0--} \longrightarrow v_{+--} \longrightarrow v_{+0-} \longrightarrow v_{+00} \tag{19}$$

$$\mathbf{0_c} \quad v_{0--} \longrightarrow v_{00-} \longrightarrow v_{+0-} \longrightarrow v_{+00} \longrightarrow v_{++0} \tag{20}$$

$$\mathbf{0_d} \quad v_{00-} \longrightarrow v_{+0-} \longrightarrow v_{++-} \longrightarrow v_{++0} \tag{21}$$

For the method SVPWM2, the corresponding sequences are:

$$\mathbf{0_a} \quad \begin{cases} v_{+00} \longrightarrow v_{000} \longrightarrow v_{00-} \longrightarrow v_{0--} & \text{for} \quad \Delta_s < \frac{\pi}{6} \\ v_{00-} \longrightarrow v_{000} \longrightarrow v_{+00} \longrightarrow v_{++0} & \text{for} \quad \Delta_s \geq \frac{\pi}{6} \end{cases} \tag{22}$$

$$\mathbf{0_b} \quad v_{0--} \longrightarrow v_{+--} \longrightarrow v_{+0-} \longrightarrow v_{+00} \tag{23}$$

$$\mathbf{0_c} \quad \begin{cases} v_{+00} \longrightarrow v_{+0-} \longrightarrow v_{00-} \longrightarrow v_{0--} & \text{for} \quad \Delta_s < \frac{\pi}{6} \\ v_{00-} \longrightarrow v_{+0-} \longrightarrow v_{+00} \longrightarrow v_{++0} & \text{for} \quad \Delta_s \geq \frac{\pi}{6} \end{cases} \tag{24}$$

$$\mathbf{0_d} \quad v_{00-} \longrightarrow v_{+0-} \longrightarrow v_{++-} \longrightarrow v_{++0} \tag{25}$$

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Appendix D

A Novel Loss Reduced Modulation Strategy for Matrix Converters, PESC 2001

A Novel Loss Reduced Modulation Strategy for Matrix Converters

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Abstract— **This paper presents a new modulation strategy for three-phase to three-phase matrix converters. The new modulation strategy is applicable whenever the output voltage reference is below half the input voltage. By applying this new modulation method, the switching losses are reduced by 15-35% compared to the conventional modulation scheme. The waveform quality of the new modulation strategy is evaluated with regard to both output flux harmonic distortion and input charge harmonic distortion.**

I. Introduction

In recent years, matrix converters for use in induction motor drives have received considerable attention as a competitor to the normally used pulse width modulated voltage source inverter (PWM-VSI). The matrix converter topology is shown in Fig. 1, where each of the nine switches are bi-directional configurations. Compared to the PWM-VSI with diode rectification stage at the input, the matrix converter provides sinusoidal input and output waveforms, bi-directional power flow, controllable input power factor and more compact design [1]. On the other hand, the matrix converter can only be linearly modulated to an output voltage equal to 0.866 times the input voltage [2]. Further, the filter design issues are complex and decoupling between input and output distortions are to some extent limited due to the absent of the DC-link capacitor [3-5]. Regarding the converter efficiency, [6] and [7] have performed some general considerations, concluding that at low switching frequencies, the VSI are the most efficient, while at higher switching frequencies, the matrix converter becomes superior. A realistic efficiency comparison (if at all possible) should however include a number of design considerations, among these a selection of modulation strategy for both converters. Unfortunately, with regard to modulation strategies, the field of VSI modulation seems quite better explored [8] than the corresponding field for matrix converters. Regarding the VSI, different discontinues modulators can be applied by which the switching losses are reduced by up to 50% compared to the normally used continuous modulation schemes [9].

Loss reduction in matrix converters have mainly been focused on reducing the number of switchings [10] and on hardware considerations [11]. This paper presents a new loss reduced modulation strategy with no demands for additional hardware. Further, to evaluate this new modulation strategy, an evaluation method is established which corresponds to the already known evaluation method for VSI modulation schemes [8].

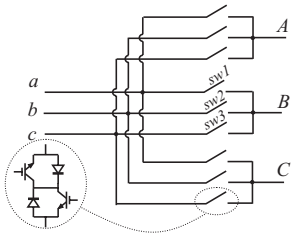

Fig. 1. The matrix converter topology.

II. Vector analysis of the switching combinations

Since the matrix converter is supplied by voltage sources the input phases must never be shorted and due to the inductive nature of the load, the output phases must not be left open. Complying with these two basic control rules, only 27 switch combinations are valid. These combinations are shown in Fig. 2. For the space-vector modulation of the matrix converter it is convenient to define the following four space vectors [12]:

$$\underline{V}_{gp} = \frac{2}{3}(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{j\frac{4\pi}{3}}) \quad (1)$$

$$\underline{V}_{rp} = \frac{2}{3}(v_A + v_B e^{j\frac{2\pi}{3}} + v_C e^{j\frac{4\pi}{3}}) \quad (2)$$

$$\underline{I}_{gp} = \frac{2}{3}(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}}) \quad (3)$$

$$\underline{I}_{rp} = \frac{2}{3}(i_A + i_B e^{j\frac{2\pi}{3}} + i_C e^{j\frac{4\pi}{3}}) \quad (4)$$

where $\underline{V}_{gp}$ is the space-vector representation for the input phase voltage, $\underline{V}_{rp}$ is the space-vector representation for the output phase voltage, $\underline{I}_{gp}$ is the space-vector representation for the input phase current and $\underline{I}_{rp}$ is the space-vector representation for the output phase current. Applying (2) on the active switch combinations shown in Fig. 2 it turns out that all these combinations become stationary vectors in the space vector plane, however with time varying amplitudes. The output voltage vectors for the active switch combinations are shown in the left part of Fig. 3. Similar, by utilizing (3) it appears that the active switch combinations correspond to stationary input current vectors in the complex space vector plane. Due to these properties of the active switch combinations, the well known space vector modulation principles can be applied to the matrix converter, although the modulation both has to consider the input current and the output voltage in the same step.

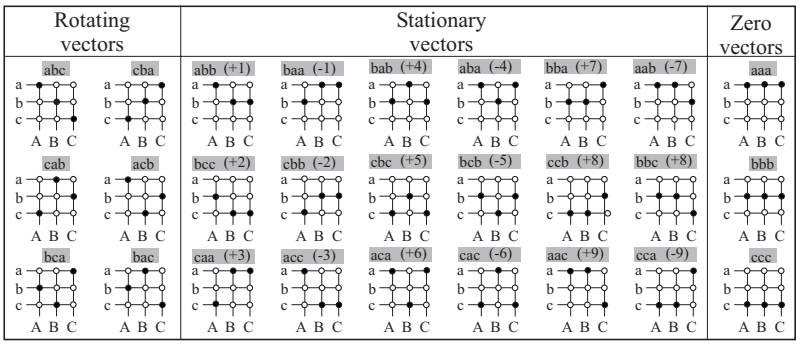

Fig. 2. The 27 allowed switch combinations.

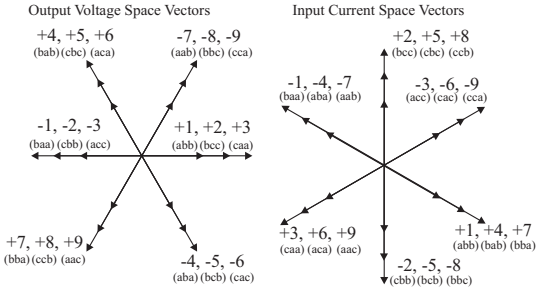

Fig. 3. The output voltage space vectors and the input current space vectors for the active switch combinations, c.f. Fig. 2.

III. Conventional space vector modulation

A. Vector time intervals

In the conventional space vector modulation, the sectors are defined as shown in Fig. 4. The input angle Δ_g used in the conventional space vector modulation is defined as:

$$\Delta_g = \mod\left(\omega_g t\ ,\ \frac{\pi}{3}\right) \tag{5}$$

where $\omega_g t = 0$ is defined as the positive zero crossing of the phase a input voltage ($v_a = \hat{v}_g \cdot \sin(\omega_g t)$). Similar, the output voltage angle Δ_r is defined as:

$$\Delta_r = \mod\left(\omega_r t + \frac{\pi}{6}\ ,\ \frac{\pi}{3}\right) \tag{6}$$

where ω_r is the angular speed of the output voltage vector. For an arbitrary sector location of the output voltage reference $\underline{V}^{\star}_{rp}$ and the input voltage vector $\underline{V}_{gp}$, the following equations can be derived using that $\underline{V}^{\star}_{rp} = \underline{V}_{r1} + \underline{V}_{r2}$:

$$\begin{aligned} V_{r1} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot \cos\left(\Delta_g - \frac{\pi}{3}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_2 \cdot \cos\left(\Delta_g - \pi\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{7}$$

$$\begin{aligned} V_{r2} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_3 \cdot \cos\left(\Delta_g - \frac{\pi}{3}\right) \cdot |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_4 \cdot \cos\left(\Delta_g - \pi\right) \cdot |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \end{aligned}$$

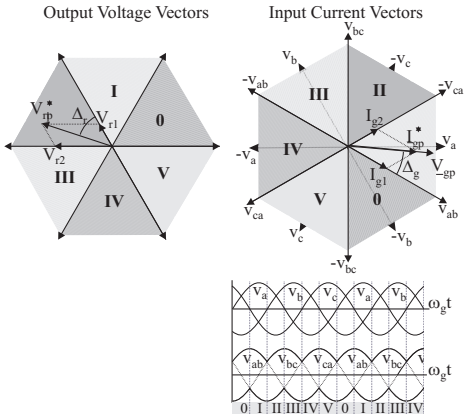

Fig. 4. Angle and sector definitions for the conventional space vector modulation.

where $\delta_{1..4}$ are the on-time durations for the four applied vectors. In each input sector, only the two line-line voltages with the highest amplitudes are used. This is illustrated in the lower part of Fig. 4. By similar considerations the input current vectors are calculated ($\underline{I}^{\star}_{gp} = \underline{I}_{g1} + \underline{I}_{g2}$):

$$\begin{aligned} I_{g1} &= |\underline{I}^{\star}_{gp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_2 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{8}$$

$$\begin{aligned} I_{g2} &= |\underline{I}^{\star}_{gp}| \cdot \sin\left(\Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_3 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned}$$

where i_x and i_y are the instantaneous value of an output phase current. Assuming that the output currents are sinusoidal and symmetrical distributed, the relation between i_x and i_y are:

$$\left\{ \begin{array}{lcl} i_x &=& \hat{i}_{rp} \cdot \sin(\omega_r t) \\ i_y &=& \hat{i}_{rp} \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right) \end{array} \right.$$

$$\Downarrow$$

$$i_y = i_x \cdot \frac{\sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin(\omega_r t)} \tag{9}$$

TABLE I

Switching table for the conventional space vector modulation

→Rec	Sector 0				Sector I				Sector II				Sector III				Sector IV				Sector V			
↓Inv	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4
0	abb	cbb	aab	ccb	acc	abb	aac	aab	bcc	acc	bbc	aac	baa	bcc	bba	bbc	caa	baa	cca	bba	cbb	caa	ccb	cca
I	aab	ccb	bab	bcb	aac	aab	cac	bab	bbc	aac	cbc	cac	bba	bbc	aba	cbc	cca	bba	aca	aba	ccb	cca	bcb	aca
II	bab	bcb	baa	bcc	cac	bab	caa	baa	cbc	cac	cbb	caa	aba	cbc	abb	cbb	aca	aba	acc	abb	bcb	aca	bcc	acc
III	baa	bcc	bba	bbc	caa	baa	cca	bba	cbb	caa	ccb	cca	abb	cbb	aab	ccb	acc	abb	aac	aab	bcc	acc	bbc	aac
IV	bba	bbc	aba	cbc	cca	bba	aca	aba	ccb	cca	bcb	aca	aab	ccb	bab	bcb	aac	aab	cac	bab	bbc	aac	cbc	cac
V	aba	cbc	abb	cbb	aca	aba	acc	abb	bcb	aca	bcc	acc	bab	bcb	baa	bcc	cac	bab	caa	baa	cbc	cac	cbb	caa

Combining (8) and (9):

$$0 = -\frac{\delta_1}{\sin(\Delta_g)} - \frac{\delta_4 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin(\omega_r t)} + \frac{\delta_2}{\sin\left(\frac{\pi}{3} - \Delta_g\right)} + \frac{\delta_3 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin(\omega_r t) \cdot \sin(\Delta_g)} \quad (10)$$

In order to achieve a solution for the modulation functions $\delta_{1..4}$ which are independent of the output current position, (10) can be separated into the following two equations:

$$\begin{aligned} 0 &= \delta_2 \cdot \sin(\Delta_g) - \delta_1 \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \\ 0 &= \delta_3 \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) - \delta_4 \cdot \sin(\Delta_g) \end{aligned} \quad (11)$$

Solving (7) and (11) for the modulation functions $\delta_{0..4}$ gives:

$$\begin{aligned} \delta_1 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin(\Delta_g) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_2 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_3 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin(\Delta_g) \cdot \sin(\Delta_r) \\ \delta_4 &= \frac{2 \cdot |\underline{V}^\star_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin(\Delta_r) \\ \delta_0 &= 1 - (\delta_1 + \delta_2 + \delta_3 + \delta_4) \end{aligned} \quad (12)$$

It should however be noted that the modulation functions at any time instant are limited by the following constraint:

$$\delta_{0..4} >= 0 \quad (13)$$

Taking this constraint into account, it is found that the maximum reference voltage $|V^\star_{rp}|$ are limited to $\sqrt{3}/2$ of the input phase voltage. Using only the two line-line voltages with maximum amplitudes, the sector-dependent switch combination for each duty-cycle function $\delta_{1..4}$ are summarized in Table I. The sector notation in Table I refers to the sector location in Fig. 4.

B. Switching sequences

In order to assure the minimum number of branch-switch-over (BSO) per switching period, which is 8 for double sided modulation [10], the following switching sequences are used: For even sector sums, the half of the switching sequence is:

$$\begin{aligned} &\delta_0 \xrightarrow[v_{ab}]{i_C} \delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 ... \quad \text{when} \quad \Delta_g < \frac{\pi}{6} \\ &\delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \xrightarrow[v_{bc}]{i_C} \delta_0 ... \quad \text{when} \quad \Delta_g > \frac{\pi}{6} \end{aligned} \quad (14)$$

and for odd sector sums, the half of the switching sequence is:

$$\begin{aligned} &\delta_0 \xrightarrow[v_{ca}]{i_A} \delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \quad \text{when} \quad \Delta_g < \frac{\pi}{6} \\ &\delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \xrightarrow[v_{ab}]{i_A} \delta_0 ... \quad \text{when} \quad \Delta_g > \frac{\pi}{6} \end{aligned} \quad (15)$$

Besides the number of BSOs per switching period, also the amplitude of the switched voltage and current influences the switching losses. As example (14) shows the switched voltages for sector combination $0_{rec}, 0_{inv}$, and similar (15) shows the switched voltages for sector combination $I_{rec}, 0_{inv}$.

IV. Modified space vector modulation

The main idea of the modified space vector modulation is to make use of the minimum line-line-voltage (contrary to the conventional space vector modulation which utilizes the two maximum line-line voltages) whenever the output voltage reference is less than half of the input voltage. The advantages of this new modulation strategy are that the harmonic content of the output voltages are reduced and additionally the switching losses are decreased. A disadvantage of the proposed modulation strategy is that the harmonic current spectra on the input side of the converter deteriorates.

A. Vector time intervals

Fig. 5 shows the modified space vector modulation approach. The line-line voltages used within each of the sectors are indicated by the increased line width in the lower part of Fig. 5 . The procedure for deriving the duty-cycle functions for the modified space vector modulation approach is almost similar to the procedure in the conventional space vector modulation. However for completion of the modulation description, the derivation of the modified duty-cycle function are given below.
The input angle Δ_g used in the modified space vector modulation is defined as, c.f. Fig 5:

$$\Delta_g = \mod\left(\left(\omega_g t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \quad (16)$$

TABLE II

SWITCHING TABLE FOR THE MODIFIED SPACE VECTOR MODULATION

→Rec	Sector 0				Sector I				Sector II				Sector III				Sector IV				Sector V			
↓Inv	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4
0	acc	cbb	aac	ccb	bcc	abb	bbc	aab	baa	acc	bba	aac	caa	bcc	cca	bbc	cbb	baa	ccb	bba	abb	caa	aab	cca
I	aac	ccb	cac	bcb	bbc	aab	cbc	bab	bba	aac	aba	cac	cca	bbc	aca	cbc	ccb	bba	bcb	aba	aab	cca	bab	aca
II	cac	bcb	caa	bcc	cbc	bab	cbb	baa	aba	cac	abb	caa	aca	cbc	acc	cbb	bcb	aba	bcc	abb	bab	aca	baa	acc
III	caa	bcc	cca	bbc	cbb	baa	ccb	bba	abb	caa	aab	cca	acc	cbb	aac	ccb	bcc	abb	bbc	aab	baa	acc	bba	aac
IV	cca	bbc	aca	cbc	ccb	bba	bcb	aba	aab	cca	bab	aca	aac	ccb	cac	bcb	bbc	aab	cbc	bab	bba	aac	aba	cac
V	aca	cbc	acc	cbb	bcb	aba	bcc	abb	bab	aca	baa	acc	cac	bcb	caa	bcc	cbc	bab	cbb	baa	aba	cac	abb	caa

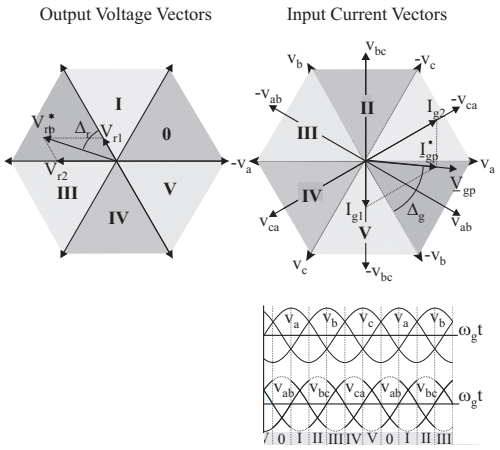

Fig. 5. Angle and sector definitions for the modified space vector modulation.

where $\omega_g t = 0$ is defined as the positive zero crossing of the phase a input voltage ($v_a = \hat{v}_g \cdot \sin(\omega_g t)$). The output voltage angle Δ_r is defined:

$$\Delta_r = \mod\left(\left(\omega_r t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \tag{17}$$

For an arbitrary sector location of the output voltage reference and the input voltage, the following equations can be derived:

$$\begin{aligned} V_{r1} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= -\delta_1 \cdot \cos\left(\Delta_g + \frac{\pi}{2}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_2 \cdot \cos\left(\frac{5\pi}{6} - \Delta_g\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{18}$$

$$\begin{aligned} V_{r2} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= -\delta_3 \cdot \cos\left(\Delta_g + \frac{\pi}{2}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_4 \cdot \cos\left(\frac{5\pi}{6} - \Delta_g\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{19}$$

Similar, the current reference $|\underline{I}^{\star}_{gp}|$ can be obtained by:

$$\begin{aligned} I_{g1} &= |\underline{I}^{\star}_{gp}| \cdot \cos\left(\Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_2 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{20}$$

$$\begin{aligned} I_{g2} &= |\underline{I}^{\star}_{gp}| \cdot \cos\left(\frac{\pi}{3} - \Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_3 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{21}$$

By use of the relation in (9), the modulation functions $\delta_{0..4}$ for the modified modulation approach can be derived:

$$\begin{aligned} \delta_1 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_2 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\Delta_g\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_3 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\Delta_r\right) \\ \delta_4 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cos\left(\Delta_g\right) \cdot \sin\left(\Delta_r\right) \\ \delta_0 &= 1 - (\delta_1 + \delta_2 + \delta_3 + \delta_4) \end{aligned} \tag{22}$$

It should be noted that the modulation functions at any time instant are limited by the constraint in (13): Taking this constraint into account, it is found that the maximum reference voltage $|V^{\star}_{rp}|$ are limited to half the input voltage. Table II shows the sector dependent switch combinations for the modified modulation. The sectors refer to the sector location in Fig. 5.

B. Switching sequences

By inspection of Table II it appears that the switching sequences have to be changed in the modified modulation strategy in order to obtain the minimum BSOs. For even sector sums, the half of the switching sequence should be:

$$\delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \tag{23}$$

and for odd sector sums, the half of the switching sequence should be:

$$\delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \tag{24}$$

V. SWITCHING LOSSES

Assuming the switch devices of the matrix converter to have linear current and voltage turn-on and turn-off characteristics with respect to time and counting only for the fundamental component of the output current, the switching losses of the matrix converter can be analytically modeled as [13]:

$$p_{sw} \propto v_{sw} \cdot i_{sw} \cdot (T_{on} + T_{off}) \cdot f_{sw} \tag{25}$$

Using the different switching sequences (14), (15), (23) and (24), the normalized per carrier switching losses may

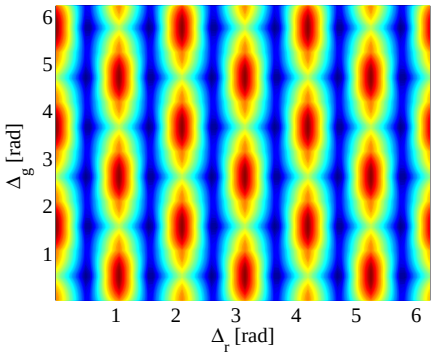

Fig. 6. Contour plot of the switching losses of the conventional modulation method for $\phi_r = 0$.

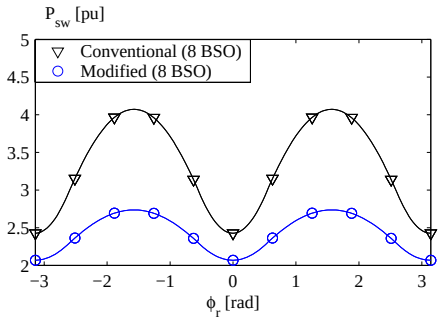

Fig. 7. The switching losses of the four different modulation functions for the matrix converter.

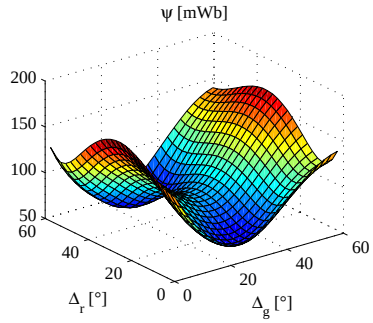

Fig. 8. The per-carrier cycle RMS value of the harmonic flux as a function of the input and output angle for the conventional modulation strategy.

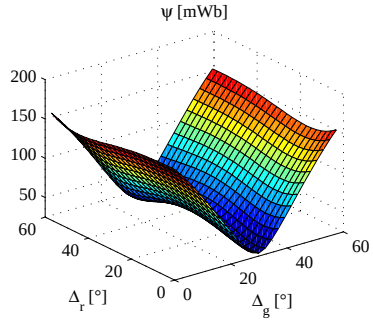

Fig. 9. The per-carrier cycle RMS value of the harmonic flux as a function of the input and output angle for the modified modulation strategy.

be calculated for arbitrary sector locations of the output voltage reference vector, the input current reference vector and the output current vector (it is provided that input current is in phase with the input phase voltage). Figure 6 shows the normalized switching losses for the conventional modulation method when the output current and output phase voltage are in phase. From figure 6 it appears that the switching losses averaged over a common period time for the input frequency and the output frequency, depends on the actual course over the surface. However, considering a general case, where the input frequency and the output frequency have no common time period, the average switching losses are calculated by integrating over the entire surface. Hence, to evaluate the different modulation methods with regards to the switching losses the following switching loss function is defined:

$$\bar{p}_{sw} \propto \frac{1}{4\pi^2}\int_0^{2\pi}\int_0^{2\pi}(p_{sw})d\Delta_g d\Delta_r \tag{26}$$

By use of (26) the switching loss functions of the two modulation schemes can be calculated for different load cases, i.e different angles ϕ_r between output phase voltage and output current. Figure 7 shows the switching loss functions for the modulations schemes as a function of the angle ϕ_r.

VI. Harmonic performance

A. Output voltage

To evaluate the output voltage quality, the harmonic flux is considered [8]. In the N^{th} carrier cycle the harmonic flux $\tilde{\psi}$ is calculated by:

$$\tilde{\psi} = \int_{NT_s}^{(N+1)T_s}(\underline{V}_{rp} - \underline{V}^{\star}_{rp})dt \tag{27}$$

where $\underline{V}_{rp}$ is a stationary output vector. The per-carrier cycle RMS value of the harmonic flux $\tilde{\psi}_{RMS}$ can be calculated by:

$$\langle\tilde{\psi}_{RMS}\rangle_{T_s} = \sqrt{\frac{1}{T_s}\int_0^{T_s}\left(\tilde{\psi}\cdot\tilde{\psi}^*\right)dt} \tag{28}$$

where $\tilde{\psi}^*$ is the complex conjugate of $\tilde{\psi}$ Fig. 8 and Fig. 9 shows the per-carrier cycle RMS value of the harmonic flux as a function of the input angle and the output angle. The figures are plotted for modulation indexes of 1 and 0.577 respectively and the harmonic flux is normalized by $\frac{T_s}{2}\frac{\sqrt{3}\hat{u}_{gp}}{2}$. Evaluating for a general case, where input frequency and the output frequency has no common period time, the RMS value of the harmonic flux is obtained by integrating over the entire surface. The RMS value of the harmonic flux is calculated by:

$$\tilde{\psi}_{RMS} = \sqrt{\frac{9}{\pi^2}\int_0^{\frac{\pi}{3}}\int_0^{\frac{\pi}{3}}\left(\langle\tilde{\psi}_{RMS}\rangle_{T_s}\right)^2 d\Delta_g\, d\Delta_r} \tag{29}$$

Fig. 10 shows the RMS-value of the harmonic flux as a function of the modulation index where the modulation index is given by (cf. (12) and (22)):

$$M = \frac{2\cdot|\underline{V}^{\star}_{rp}|}{\sqrt{3}\cdot|\underline{V}_{rp}|} \tag{30}$$

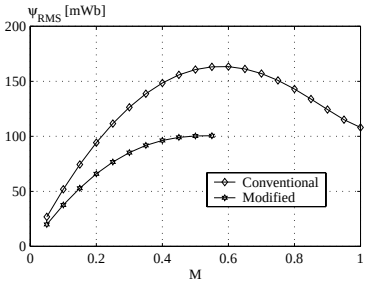

Fig. 10. The harmonic flux as a function of the modulation index, c.f. (30)

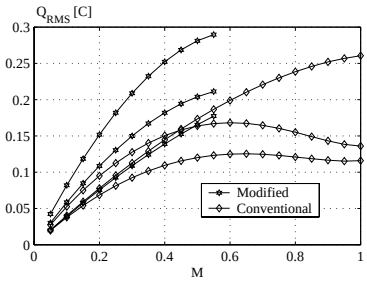

Fig. 11. The charge distortion as a function of the modulation index, c.f. (30). The different curves correspond to different output load angles.

From Fig. 10 it appears that the modified modulation strategy shows better output harmonic performance in the entire linear modulation range. It should be noted that for $\cos(\phi_i) \neq 1$ at the input, both curves in Fig. 10 would be changed.

B. Input current

In principle, the evaluation of the input current follows the same procedure as for the output voltage, however the evaluation parameter is changed from harmonic flux to harmonic charge $\tilde{Q}$. Further, the evaluation of the input current becomes a little more complex than the evaluation of the output voltage due to the fact that the amplitudes of the stationary input current vectors are affected by the load angle ϕ_r. Fig. 11 shows the harmonic charge $\tilde{Q}_{RMS}$ vs. the modulation index. The lowest curve for both the modified modulation algorithm and the conventional modulation algorithm corresponds to $\cos(\phi_o) = 1$ while the the middle curve and the upper curve corresponds to $\cos(\phi_o) = 0.71$ and $\cos(\phi_o) = 0$ respectively. In the calculation of the results in Fig. 11 the harmonic charge $\tilde{Q}$ is normalized by $\frac{T_s}{2}\frac{\sqrt{3}i_r}{2}$.

VII. Results

Fig. 12 show a simulation of the matrix converter which illustrates the improved output performance by using the modified space vector modulation at output voltages lower than half the input voltage.

VIII. Conclusion

This paper has presented a new modulation strategy for matrix converters. The modulation strategy can be used whenever the output reference is lower than half the input voltage. It is shown by analytical expressions that the proposed modulation strategy reduces the switching losses of the matrix converter by 15-35%, depending on the output load angle. An evaluation tool similar to that proposed for VSIs [8], is developed. This tool is used to compare the new modulation strategy with the conventional, both with regard to output waveforms and input waveforms. It turns out that the new modulation strategy shows better output waveforms than the conventional modulation strategy in the whole linear modulation range while at the input, the conventional modulation strategy seems superior. The developed evaluation tool are also applicable to compare the matrix converter with the VSI.

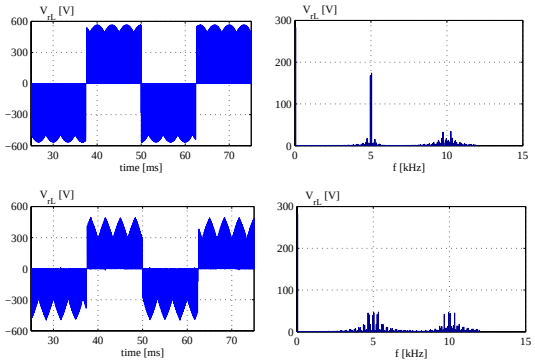

Fig. 12. The upper plot shows the output side voltage using conventional modulation ($M = 0.577$), while the lower plot shows the output side voltage using the modified modulation ($M = 0.577$).

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Appendix E

Evaluation of Modulation Schemes for Three-phase to Three-phase Matrix Converters. IEEE Transaction on Industrial Electronics 2002

Evaluation of Modulation Schemes for Three-phase to Three-phase Matrix Converters

Lars Helle, Kim B. Larsen, Allan H. Jørgensen, Stig Munk-Nielsen and Frede Blaabjerg

Abstract— **This paper presents a method for evaluating different modulation schemes employed with three-phase to three-phase matrix converters. The evaluation method addresses three important modulator characteristics - the output waveform quality, the input waveform quality and the switching losses associated with the modulation schemes. The method is used to evaluate four different modulation strategies, all based on the direct space vector modulation approach. Further, regarding the switching losses, the paper proposes a new space vector approach by which the switching losses can be reduced by 15-35%, depending on the output load angle. This new modulation approach is applicable whenever the output voltage reference is below half the input voltage and the output voltage quality is then superior to that of the conventional space vector modulation scheme. The functionality of the new modulation scheme is validated by both simulations and experimental results and compared to waveforms obtained by using exiting space vector modulation schemes. The output voltage of the proposed scheme turns out to be comparable to the best of the conventional schemes while the input current is more distorted.**

I. Introduction

In recent years, matrix converters for use in induction motor drives have received considerable attention as a competitor to the normally used pulse width modulated voltage source inverter (PWM-VSI). The matrix converter topology is shown in Fig. 1, where each of the nine switches represents a bi-directional configuration. Compared to the PWM-VSI with diode rectification stage at the input, the matrix converter provides sinusoidal input and output waveforms, bi-directional power flow, controllable input power factor and more compact design [1]. On the other hand, the matrix converter can only be linearly modulated to an output voltage equal to 0.866 times the input voltage [2]. Further, the filter design issues are complex and a de-coupling between input and output distortions is to some extent limited due to the absent of the DC-link capacitor [3-5]. Regarding the converter efficiency, [6] and [7] have performed some general considerations, concluding that at low switching frequencies, the VSI are the most efficient, while at higher switching frequencies, the matrix converter becomes superior. A realistic comparison (if at all possible) should however include a number of design considerations, among these a selection of modulation strategy for both converters. Unfortunately, with regard to modulation strategies, the field of VSI modulation seems quite better explored [8] than the corresponding field of matrix converters. Regarding the VSI, different modulators can be applied by which the switching loss is reduced by up to 50% compared to the normally used modulation schemes [9]. Loss reduction in matrix converters has mainly been focused on reducing the number of switchings [10] and on hardware considerations [11]. Moreover, like the performance evaluation of PWM-VSI modulation schemes presented in [8], no similar approach exists for modulation schemes applicable to the matrix converter. The purposes of this paper are:

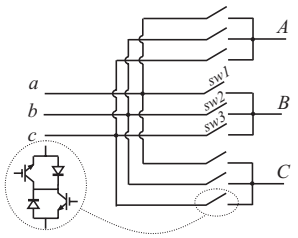

Fig. 1. The matrix converter topology.

1. Presentation of a new loss reduced space vector modulation approach that is applicable whenever the output voltage reference is below half the input voltage [12].

2. Presentation of a performance evaluation method for three-phase to three-phase matrix converter modulation schemes, regarding switching losses, input waveform quality and output waveform quality.

First the paper reviews the space vector analysis applied for three-phase to three-phase matrix converters. Then the conventional space vector modulation theory for matrix converters is reviewed using the direct approach. From the theory of the conventional direct space vector modulation, the new switching loss reduced space vector approach is derived. Some important aspects regarding the switching sequence and the placement of the zero-vectors are also discussed for both the conventional scheme and the new reduced switching loss space vector approach. The remaining part of the paper is dedicated to the development of a tool usable for performance analysis of modulation schemes for matrix converters. The performance analysis is divided into three parts concerning the switching losses, the input performance and the output performance of the different modulation schemes. Finally, in order to show the functionality of the proposed switching loss reduced space vector modulation method and in order to compare the different modulation methods in the time domain, the paper contains simulated and experimental results of different modulation schemes.

II. Vector analysis of the switching combinations

From Fig. 1 it appears that the control of the matrix converter involves 2^9 different switch states. However, since the matrix converter is supplied by voltage sources, the input phases must never be shorted and due to the inductive nature of the load, the output phases must not be

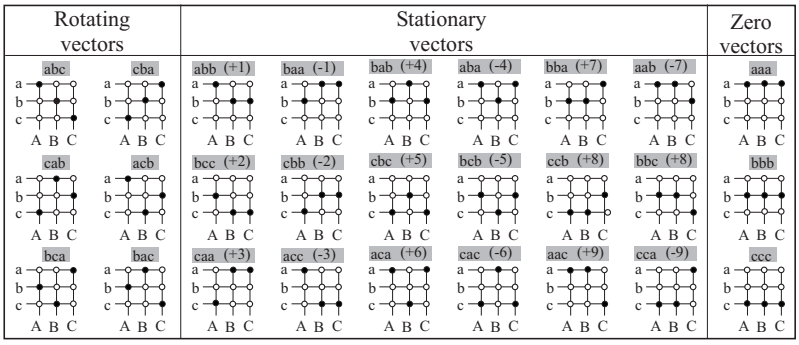

Fig. 2. The 27 allowed switch combinations in a matrix converter.

left open. Complying with these two basic control rules, only 27 switch combinations are valid. These combinations are shown in Fig. 2. For the space-vector modulation of the matrix converter it is convenient to define the following four space vectors [13]:

$$\underline{V}_{gp} = \frac{2}{3}(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{j\frac{4\pi}{3}}) \quad (1)$$

$$\underline{V}_{rp} = \frac{2}{3}(v_A + v_B e^{j\frac{2\pi}{3}} + v_C e^{j\frac{4\pi}{3}}) \quad (2)$$

$$\underline{I}_{gp} = \frac{2}{3}(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{4\pi}{3}}) \quad (3)$$

$$\underline{I}_{rp} = \frac{2}{3}(i_A + i_B e^{j\frac{2\pi}{3}} + i_C e^{j\frac{4\pi}{3}}) \quad (4)$$

where $\underline{V}_{gp}$ is the space-vector representation for the input phase voltage, $\underline{V}_{rp}$ is the space-vector representation for the output phase voltage, $\underline{I}_{gp}$ is the space-vector representation for the input phase current and $\underline{I}_{rp}$ is the space-vector representation for the output phase current. Applying (2) on the active switch combinations shown in Fig. 2 it turns out that all these combinations become stationary vectors in the complex space vector plane, but with time varying amplitudes. The output voltage vectors for the active switch combinations are shown in the left part of Fig. 3. Similarly by using (3) it appears that the active switch combinations correspond to stationary input current vectors in the complex space vector plane. Due to these properties of the active switch combinations, the well known space vector modulation principle can be applied to the matrix converter, although the modulation both has to consider the input current and the output voltage in the same step.

III. Conventional space vector modulation

A. Vector time intervals

In the conventional direct space vector modulation approach, the sectors are defined as shown in Fig. 4. The input angle Δ_g used in the conventional space vector modulation is defined as:

$$\Delta_g = \mod(\omega_g t\ ,\ \frac{\pi}{3}) \quad (5)$$

where $\omega_g t = 0$ is defined as the positive zero crossing of the phase a input voltage ($v_a = \hat{v}_g \cdot \sin(\omega_g t)$). Similar, the

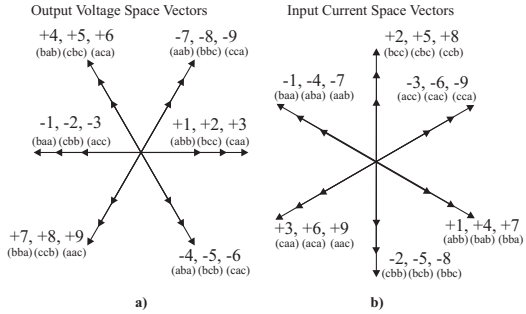

Fig. 3. Space vector hexagons for the active switch combinations, c.f. Fig. 2. **a)** Output voltage. **b)** Input current.

output voltage angle Δ_r is defined:

$$\Delta_r = \mod(\omega_r t + \frac{\pi}{6}\ ,\ \frac{\pi}{3}) \quad (6)$$

where ω_r is the angular speed of the output voltage reference vector and $\omega_r t = 0$ is defined as the positive zero crossing of the phase A output voltage ($v_A^\star = \hat{v}_r^\star \cdot \sin(\omega_r t)$). For an arbitrary sector location of the output voltage reference $\underline{V}_{rp}^\star$ and the input voltage vector $\underline{V}_{gp}$, the following equations can be derived using that $\underline{V}_{rp}^\star = \underline{V}_{r1} + \underline{V}_{r2}$:

$$\begin{aligned}\underline{V}_{r1} &= |\underline{V}_{rp}^\star| \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot \cos\left(\Delta_g - \frac{\pi}{3}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_2 \cdot \cos(\Delta_g - \pi)\, |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}}\end{aligned} \quad (7)$$

$$\begin{aligned}\underline{V}_{r2} &= |\underline{V}_{rp}^\star| \cdot \sin(\Delta_r) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_3 \cdot \cos\left(\Delta_g - \frac{\pi}{3}\right) \cdot |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_4 \cdot \cos(\Delta_g - \pi) \cdot |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}}\end{aligned}$$

where $\delta_{1..4}$ are the on-time durations for the four applied vectors. In each input sector, only the two line-line voltages with the highest amplitudes are used. This is illustrated in the lower part of Fig. 4. By similar considerations the input current vectors are calculated, using that

TABLE I

SWITCHING TABLE FOR THE CONVENTIONAL SPACE VECTOR MODULATION.

→Rec	Sector 0				Sector I				Sector II				Sector III				Sector IV				Sector V			
↓Inv	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4
0	abb	cbb	aab	ccb	acc	abb	aac	aab	bcc	acc	bbc	aac	baa	bcc	bba	bbc	caa	baa	cca	bba	cbb	caa	ccb	cca
I	aab	ccb	bab	bcb	aac	aab	cac	bab	bbc	aac	cbc	cac	bba	bbc	aba	cbc	cca	bba	aca	aba	ccb	cca	bcb	aca
II	bab	bcb	baa	bcc	cac	bab	caa	baa	cbc	cac	cbb	caa	aba	cbc	abb	cbb	aca	aba	acc	abb	bcb	aca	bcc	acc
III	baa	bcc	bba	bbc	caa	baa	cca	bba	cbb	caa	ccb	cca	abb	cbb	aab	ccb	acc	abb	aac	aab	bcc	acc	bbc	aac
IV	bba	bbc	aba	cbc	cca	bba	aca	aba	ccb	cca	bcb	aca	aab	ccb	bab	bcb	aac	aab	cac	bab	bbc	aac	cbc	cac
V	aba	cbc	abb	cbb	aca	aba	acc	abb	bcb	aca	bcc	acc	bab	bcb	baa	bcc	cac	bab	caa	baa	cbc	cac	cbb	caa

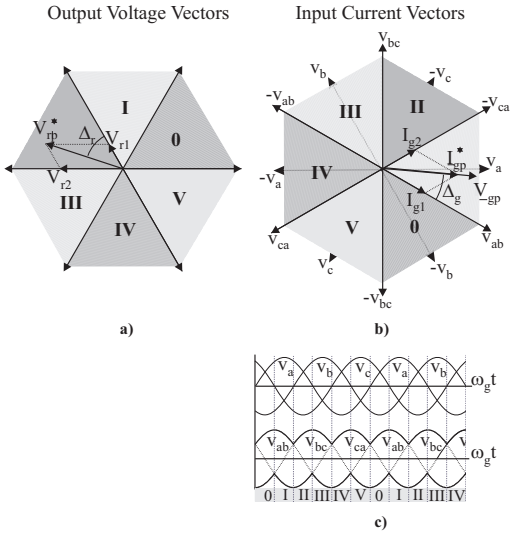

Fig. 4. Angle and sector definitions for the conventional space vector modulation. **a)** Output voltage. **b)** Input current. **c)** Input sector definition in time domain.

$(\underline{I}^{\star}_{gp} = \underline{I}_{g1} + \underline{I}_{g2})$:

$$\begin{aligned} \underline{I}_{g1} &= |\underline{I}^{\star}_{gp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_2 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot i_y \cdot \frac{2}{\sqrt{3}} \\ \underline{I}_{g2} &= |\underline{I}^{\star}_{gp}| \cdot \sin\left(\Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_3 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{8}$$

where i_x and i_y are the instantaneous values of two output phase currents. Assuming that the output currents are sinusoidal and symmetrical distributed, the relation between i_x and i_y are:

$$\left\{ \begin{array}{rcl} i_x &=& \hat{i}_{rp} \cdot \sin(\omega_r t) \\ i_y &=& \hat{i}_{rp} \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right) \end{array} \right.$$

$$\Downarrow$$

$$i_y = i_x \cdot \frac{\sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin(\omega_r t)} \tag{9}$$

Combining (8) and (9) and rearranging, the following output current dependent expression is obtained:

$$\begin{aligned} 0 = &-\frac{\delta_1}{\sin(\Delta_g)} - \frac{\delta_4 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin(\omega_r t)} + \\ &\frac{\delta_2}{\sin\left(\frac{\pi}{3} - \Delta_g\right)} + \frac{\delta_3 \cdot \sin\left(\omega_r t \pm \frac{2\pi}{3}\right)}{\sin(\omega_r t) \cdot \sin(\Delta_g)} \end{aligned} \tag{10}$$

In order to achieve solutions for the modulation functions $\delta_{1..4}$ which are independent of the output current position, (10) can be separated into the following two equations:

$$\begin{aligned} 0 &= \delta_2 \cdot \sin(\Delta_g) - \delta_1 \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \\ 0 &= \delta_3 \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) - \delta_4 \cdot \sin(\Delta_g) \end{aligned} \tag{11}$$

Solving (7) and (11) for the modulation functions $\delta_{0..4}$ gives:

$$\begin{aligned} \delta_1 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin(\Delta_g) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_2 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \\ \delta_3 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin(\Delta_g) \cdot \sin\left(\Delta_r\right) \\ \delta_4 &= \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \cdot \sin\left(\frac{\pi}{3} - \Delta_g\right) \cdot \sin\left(\Delta_r\right) \\ \delta_0 &= 1 - (\delta_1 + \delta_2 + \delta_3 + \delta_4) \end{aligned} \tag{12}$$

It should however be noted that the modulation functions at any time instant are limited by the following constraint:

$$\delta_{0..4} >= 0 \tag{13}$$

Using only the two line-line voltages with maximum amplitudes, the sector-dependent switch combination for each duty-cycle function $\delta_{1..4}$ are summarized in Table I. The sector notation in Table I refers to the sector location in Fig. 4.

B. Modulation index

When comparing different modulation strategies for one type of converter, it is often convenient to normalize the output voltage to some reference voltage. This normalized voltage quantity is termed the modulation index M. The choice of reference voltage can be arbitrary and in the literature different choices exist which lead to some confusion. In this context, the choice of reference voltage is chosen in such a way that the modulation index

TABLE II

SWITCHING TABLE FOR THE MODIFIED SPACE VECTOR MODULATION.

→Rec	Sector 0				Sector I				Sector II				Sector III				Sector IV				Sector V			
↓Inv	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4	δ_1	δ_2	δ_3	δ_4
0	acc	cbb	aac	ccb	bcc	abb	bbc	aab	baa	acc	bba	aac	caa	bcc	cca	bbc	cbb	baa	ccb	bba	abb	caa	aab	cca
I	aac	ccb	cac	bcb	bbc	aab	cbc	bab	bba	aac	aba	cac	cca	bbc	aca	cbc	ccb	bba	bcb	aba	aab	cca	bab	aca
II	cac	bcb	caa	bcc	cbc	bab	cbb	baa	aba	cac	abb	caa	aca	cbc	acc	cbb	bcb	aba	bcc	abb	bab	aca	baa	acc
III	caa	bcc	cca	bbc	cbb	baa	ccb	bba	abb	caa	aab	cca	acc	cbb	aac	ccb	bcc	abb	bbc	aab	baa	acc	bba	aac
IV	cca	bbc	aca	cbc	ccb	bba	bcb	aba	aab	cca	bab	aca	aac	ccb	cac	bcb	bbc	aab	cbc	bab	bba	aac	aba	cac
V	aca	cbc	acc	cbb	bcb	aba	bcc	abb	bab	aca	baa	acc	cac	bcb	caa	bcc	cbc	bab	cbb	baa	aba	cac	abb	caa

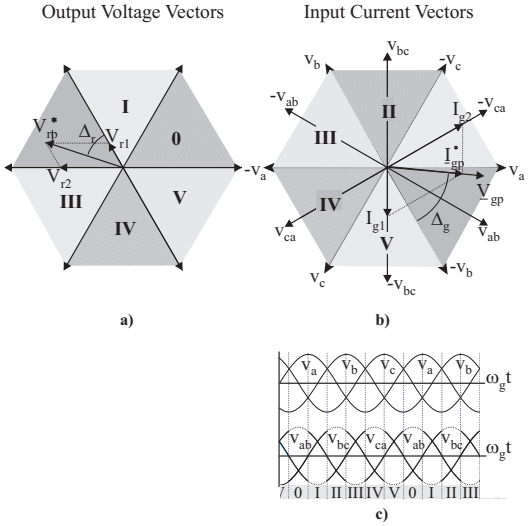

Fig. 5. Angle and sector definitions for the modified space vector modulation. **a)** Output voltage. **b)** Input current. **c)** Input sector definition in time domain.

becomes unity at the boundary between the linear modulation range and over modulation for the conventional modulation method. Hence, from (12) and (13) the modulation index becomes:

$$M = \frac{2 \cdot |\underline{V}^{\star}_{rp}|}{\sqrt{3} \cdot |\underline{V}_{gp}|} \tag{14}$$

From (14) it appears that the maximum output reference voltage $|\widehat{V}^{\star}_{rp}|$ is limited to $\sqrt{3}/2$ of the input phase voltage.

IV. Modified space vector modulation

The main idea of the modified space vector modulation [12] is to make use of the minimum line-line voltage (contrary to the conventional space vector modulation which utilizes the two maximum line-line voltages) whenever the output voltage reference is less than half of the input voltage. The advantages of this new modulation strategy are that the harmonic content of the output voltages are reduced and additionally the switching losses are decreased. A disadvantage of the proposed modulation strategy is that the harmonic current spectrum on the input side of the converter is changed.

A. Vector time intervals

Fig. 5 shows the output hexagons and the input hexagons for the modified space vector modulation approach. The line-line voltages used within each of the sectors are indicated by the increased line width in the lower part of Fig. 5. The procedure for deriving the duty-cycle functions for the modified space vector modulation approach is almost similar to the procedure in the conventional space vector modulation. However, for completion of the modulation description, the derivation of the modified duty-cycle function is given below.

The input angle Δ_g used in the modified space vector modulation is defined as, c.f. Fig. 5:

$$\Delta_g = \mod\left(\left(\omega_g t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \tag{15}$$

where $\omega_g t = 0$ is defined as the positive zero crossing of the phase a input voltage ($v_a = \hat{v}_g \cdot \sin(\omega_g t)$). The output voltage angle Δ_r is defined as:

$$\Delta_r = \mod\left(\left(\omega_r t + \frac{\pi}{6}\right), \frac{\pi}{3}\right) \tag{16}$$

For an arbitrary sector location of the output voltage reference and the input voltage, the following equations can be derived:

$$\begin{aligned} V_{r1} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\frac{\pi}{3} - \Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= -\delta_1 \cdot \cos\left(\Delta_g + \frac{\pi}{2}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_2 \cdot \cos\left(\frac{5\pi}{6} - \Delta_g\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \\ V_{r2} &= |\underline{V}^{\star}_{rp}| \cdot \sin\left(\Delta_r\right) \cdot \frac{2}{\sqrt{3}} \\ &= -\delta_3 \cdot \cos\left(\Delta_g + \frac{\pi}{2}\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} - \\ &\quad \delta_4 \cdot \cos\left(\frac{5\pi}{6} - \Delta_g\right) |\underline{V}_{gp}| \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{17}$$

Similar, the current reference $|\underline{I}^{\star}_{gp}|$ can be obtained by:

$$\begin{aligned} I_{g1} &= |\underline{I}^{\star}_{gp}| \cdot \cos\left(\Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_2 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_4 \cdot i_y \cdot \frac{2}{\sqrt{3}} \\ I_{g2} &= |\underline{I}^{\star}_{gp}| \cdot \cos\left(\frac{\pi}{3} - \Delta_g\right) \cdot \frac{2}{\sqrt{3}} \\ &= \delta_1 \cdot i_x \cdot \frac{2}{\sqrt{3}} - \delta_3 \cdot i_y \cdot \frac{2}{\sqrt{3}} \end{aligned} \tag{18}$$

Using the relation in (9), the modulation functions $\delta_{0..4}$ for the modified modulation approach can be derived:

$$\begin{aligned}
\delta_1 &= \frac{2\cdot|\underline{V}^{\star}_{rp}|}{\sqrt{3}\cdot|\underline{V}_{gp}|}\cos\left(\frac{\pi}{3}-\Delta_g\right)\cdot\sin\left(\frac{\pi}{3}-\Delta_r\right)\\
\delta_2 &= \frac{2\cdot|\underline{V}^{\star}_{rp}|}{\sqrt{3}\cdot|\underline{V}_{gp}|}\cos\left(\Delta_g\right)\cdot\sin\left(\frac{\pi}{3}-\Delta_r\right)\\
\delta_3 &= \frac{2\cdot|\underline{V}^{\star}_{rp}|}{\sqrt{3}\cdot|\underline{V}_{gp}|}\cos\left(\frac{\pi}{3}-\Delta_g\right)\cdot\sin\left(\Delta_r\right) \qquad (19)\\
\delta_4 &= \frac{2\cdot|\underline{V}^{\star}_{rp}|}{\sqrt{3}\cdot|\underline{V}_{gp}|}\cos\left(\Delta_g\right)\cdot\sin\left(\Delta_r\right)\\
\delta_0 &= 1-(\delta_1+\delta_2+\delta_3+\delta_4)
\end{aligned}$$

It should be noted that the modulation functions at any time instant are limited by the constraint in (13). Table II shows the sector dependent switch combinations for the modified modulation approach. The sector notation in Table II refers to the sector location in Fig. 5.

B. Modulation index

For comparison it is convenient to retain the modulation index expression defined in (14). Taking the constraint in (13) into account, it is found that the boundary between linear modulation and over modulation occurs at a modulation index of 0.577. Hence, the maximum output reference voltage $|V^{\star}_{rp}|$ is limited to half the input voltage in the modified space vector approach.

V. Double-sided vector sequences

Like the modulation of the VSI, the vector sequences and the placement of the zero vectors have a high influence on the performance and the efficiency of the matrix converter. In the first papers concerning space vector modulation, single-sided modulation was used [14], but at the expense of only a slight increase in the number of branch switch over (BSO) per switching period, double-sided modulation has become the preferred method. In double-sided modulation, the switching period is divided into two equal periods and in both these periods the four selected active vectors are applied. In the last of the two periods, the sequence order is reversed. The zero-vectors can be applied anywhere in the switching sequence. Due to the better harmonic performance at the input side and at the output side, only double-sided modulation is considered in this paper. Specific, the following four double-sided modulation strategies will be treated:

- Conventional double-sided modulation (8 BSO) [15].
- Double-sided modulation for the modified space-vector algorithm (8 BSO) [12].
- Conventional double-sided modulation with distributed zero vectors (10 BSO) [16].
- Double-sided modulation with distributed zero vectors for the modified space vector algorithm (10 BSO).

A. Conventional modulation (8 BSO)

In the conventional modulation presented in [15] the switching sequence for the conventional modulation was optimized with regards to the BSO per switching fundamental, giving a minimum number of 8 BSO. Following this switching procedure, there is still one degree of freedom left and that is the position of the zero-vector within the switching sequence. The zero vector could either be applied in the beginning of the sequence or in the center of the sequence. Regarding the converter efficiency (and the emission of common-mode voltage [17]), the amplitude of the switched voltage, when changing to/from the zero-vector state can be used to determine the zero-vector placement, c.f. the lower part of Fig. 4. Hence, for even sector sums, the half of the switching sequence is:

$$\delta_0 \xrightarrow[v_{ab}]{i_C} \delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \ldots \quad \text{if} \quad \Delta_g < \frac{\pi}{6} \qquad (20)$$

$$\delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \xrightarrow[v_{bc}]{i_C} \delta_0 \ldots \quad \text{if} \quad \Delta_g > \frac{\pi}{6} \qquad (21)$$

and for odd sector sums, the half of the switching sequence is:

$$\delta_0 \xrightarrow[v_{ca}]{i_A} \delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \ldots \quad \text{if} \quad \Delta_g < \frac{\pi}{6} \qquad (22)$$

$$\delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \xrightarrow[v_{ab}]{i_A} \delta_0 \ldots \quad \text{if} \quad \Delta_g > \frac{\pi}{6} \qquad (23)$$

For each BSO in (20) to (23) the switched current and the switched line-line voltage are shown, valid for sector 0_{rec}-0_{inv} and $I_{rec}-0_{inv}$ respectively. By use of Table I, the switched voltages and switched currents for an arbitrary sector location can be determined. This will be used when evaluating the switching losses of the conventional double-sided modulation method.

B. Modified space-vector modulation (8BSO)

By inspection of Table II it appears that the switching sequences of the modified modulation strategy are to be changed in order to obtain the minimum of 8 BSO per switching fundamental. Hence, for even sector sums, the half of the switching sequence should be:

$$\delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \ldots \qquad (24)$$

which assures 8 BSO per switching fundamental. For odd sector sums, the half of the switching sequence should be:

$$\delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \ldots \qquad (25)$$

Compared to the conventional method it appears that only the two minimum line-line voltages are switched, which presumably decreases the switching losses. The switched currents and voltages listed in (24) and (25) are valid for sector 0_{rec}-0_{inv} and $I_{rec}-0_{inv}$ respectively. By the use of Table II the switched voltages and currents can be determined for an arbitrary sector location of the output reference vector and the input current vector.

C. Conventional modulation with distributed zero vectors (10 BSO)

The third method takes advantage of that the switching sequence order can be used to increase the switching frequency seen from the input side by distributing the zero vectors throughout the switching period. This is especially advantageous when considering the input filter design. However, this is achieved at the expense of a higher number of BSO per switching fundamental. In [16] different distributions of the zero vector are discussed and it is

concluded that the most significant improvements are obtained by distributing the zero-vector at the beginning and in the center of the switching sequence. This doubles the dominant switching frequency seen from the input side at the expense of only two additional switchings per switching fundamental. With the constraint of only one BSO per switch-state shift, there is no degree of freedom left in the order of the switching sequence. According to [16], the half of the switching sequence for even sector sums is:

$$\delta_0 \xrightarrow[v_{ab}]{i_C} \delta_3 \xrightarrow[v_{ab}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_2 \xrightarrow[v_{bc}]{i_B} \delta_4 \xrightarrow[v_{bc}]{i_C} \delta_0 ... \tag{26}$$

And for odd sector sums:

$$\delta_0 \xrightarrow[v_{ca}]{i_A} \delta_1 \xrightarrow[v_{ca}]{i_B} \delta_3 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{ab}]{i_B} \delta_2 \xrightarrow[v_{ab}]{i_A} \delta_0 ... \tag{27}$$

The switched currents and voltages listed in (26) and (27) are valid for sector 0_{rec}-0_{inv} and $I_{rec} - 0_{inv}$ respectively.

D. *Modified space vector modulation with distributed zero vectors (10 BSO)*

Adopting the method from [16] for use in the modified modulation approach is not as simple as for the conventional modulation due to a higher degree of freedom when ordering the switching sequence. According to the sequences in (24) and (25) the additional zero-vector could be applied in either the beginning of the sequence or in the center of the sequence. In order to explain the differences in the zero-vector placement, the half of the switching sequence for sector 0_{rec}-0_{inv} is listed in (28) where the optional zero-vector placement is marked with the δ_0' and δ_0'' respectively.

$$\delta_0' \xrightarrow[v_{ca}]{i_C} \delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \xrightarrow[v_{bc}]{i_A} \delta_0'' ... \tag{28}$$

From (28) it appears that the positioning of the zero-vector can be done either with regard to the switched current or with regard to the switched voltage.

D.1 Switched voltage

Regarding the switched voltage, it appears from the lower part of Fig. 5 that the half of the switching sequence for even sectors should be:

$$\delta_0 \xrightarrow[v_{ca}]{i_C} \delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 ... \quad \text{if } \Delta_g < \frac{\pi}{6} \tag{29}$$

$$\delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \xrightarrow[v_{bc}]{i_A} \delta_0 ... \quad \text{if } \Delta_g > \frac{\pi}{6} \tag{30}$$

in order to assure that the lowest voltage is switched when applying the zero-vector. For odd sectors, the sequence should be:

$$\delta_0 \xrightarrow[v_{bc}]{i_A} \delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 ... \quad \text{if } \Delta_g < \frac{\pi}{6} \tag{31}$$

$$\delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \xrightarrow[v_{ab}]{i_C} \delta_0 ... \quad \text{if } \Delta_g > \frac{\pi}{6} \tag{32}$$

The modulation method described by the sequences in (29) to (32) is in the further denoted *modified modulation (10 BSO) with distributed zero-vectors (SV)*, where the abbreviation *SV* indicates that the modulation regards the switched voltage.

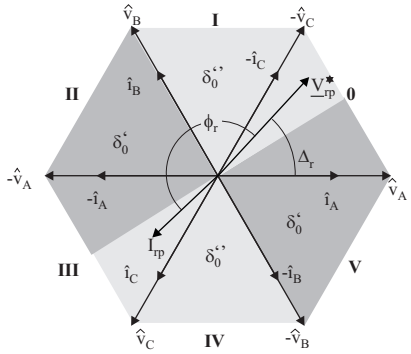

Fig. 6. Output current and output voltage space vector diagram.

D.2 Switched Current

Regarding the switched current, the modified modulation with distributed zero-vectors can adopt some of the features from the discontinuous modulation strategies of the VSI. In other words, the placement of the zero-vector can be determined such that the minimum current is switched. By this, the optional placement of the zero-vector becomes dependent of the angle ϕ_r between output current and output voltage. This is illustrated in Fig. 6. where the output current and output phase voltage space vector diagram are shown. For illustration purposes, the output voltage reference vector $\underline{V}^\star_{rp}$ is located in sector 0 and the angle between the output voltage reference and the output current is ϕ_r. In order to assure that the minimum output current is switched when switching to/from the zero-vector state, the switching sequence in (28) should be altered between the δ_0' and the δ_0'' sequence in accordance with the output current position in Fig. 6.

Generalizing to an arbitrary sector location of the output current vector the half of the vector sequence for even sector sums becomes:

$$\delta_0 \xrightarrow[v_{ca}]{i_C} \delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \text{ if } \begin{cases} -\frac{\pi}{3} < (\Delta_r + \phi_r) < \frac{\pi}{6} \\ \frac{2\pi}{3} < (\Delta_r + \phi_r) < \frac{7\pi}{6} \end{cases} \tag{33}$$

$$\delta_3 \xrightarrow[v_{ca}]{i_B} \delta_1 \xrightarrow[v_{ca}]{i_A} \delta_0 \xrightarrow[v_{bc}]{i_C} \delta_4 \xrightarrow[v_{bc}]{i_B} \delta_2 \xrightarrow[v_{bc}]{i_A} \delta_0 \text{ if } \begin{cases} \frac{\pi}{6} < (\Delta_r + \phi_r) < \frac{2\pi}{3} \\ \frac{7\pi}{6} < (\Delta_r + \phi_r) < \frac{5\pi}{3} \end{cases} \tag{34}$$

and for odd sector sums the switching sequence becomes:

$$\delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \xrightarrow[v_{ab}]{i_C} \delta_0 \text{ if } \begin{cases} -\frac{\pi}{3} < (\Delta_r + \phi_r) < \frac{\pi}{6} \\ \frac{2\pi}{3} < (\Delta_r + \phi_r) < \frac{7\pi}{6} \end{cases} \tag{35}$$

$$\delta_0 \xrightarrow[v_{bc}]{i_A} \delta_1 \xrightarrow[v_{bc}]{i_B} \delta_3 \xrightarrow[v_{ab}]{i_C} \delta_0 \xrightarrow[v_{bc}]{i_A} \delta_2 \xrightarrow[v_{ab}]{i_B} \delta_4 \text{ if } \begin{cases} \frac{\pi}{6} < (\Delta_r + \phi_r) < \frac{2\pi}{3} \\ \frac{7\pi}{6} < (\Delta_r + \phi_r) < \frac{5\pi}{3} \end{cases} \tag{36}$$

Following the switching sequences in (33) to (36), the modulator needs information about the instantaneous angle between output voltage and output current. However, it is easily realized, that the angle ϕ_r can be pre-set to a fixed value representing the steady-state nominal value of the load angle.

The modulation method described by the sequences in (33) to (36) is in the further denoted *modified modulation (10 BSO) with distributed zero-vectors (SC)*, where the abbreviation *SC* indicates that the modulation regards the switched current.

VI. Switching losses

Assuming the switching devices of the matrix converter to have a linear current and voltage turn-on and turn-

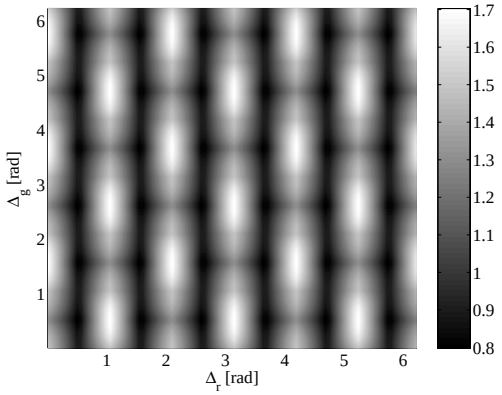

Fig. 7. Contour plot of the per carrier switching losses of the conventional modulation method for $\phi_r = 0$. The losses are plotted against the angles Δ_g and Δ_r.

off characteristic with respect to time and counting only for the fundamental component of the output current, the switching losses p_{sw} of the matrix converter can be analytically modeled as [18]:

$$p_{sw} \quad \propto \quad v_{sw} \cdot i_{sw} \cdot (T_{on} + T_{off}) \cdot f_{sw} \tag{37}$$

where v_{sw} is the switched voltage, i_{sw} is the switched current, f_{sw} is the switching frequency and T_{on} and T_{off} is the turn-on and turn-off times for the switching devices. For further simplification, (37) is normalized to the product of the peak output current $\hat{i}_r$, the peak value of the switched voltage v_{gL} (which is the peak line-line voltage at the supply grid), the switching frequency and the device characteristics. The normalized switching loss function $p_{sw,n}$ yields:

$$p_{sw,n} \quad \propto \quad \frac{p_{sw}}{\hat{v}_{gL} \cdot \hat{i}_r \cdot (T_{on} + T_{off}) \cdot f_{sw}} \tag{38}$$

Using the different switching sequences, the normalized per-carrier switching losses may be calculated for arbitrary sector locations of the output voltage reference vector, the input current reference vector and the output current vector (it is provided that the input current vector and the input voltage vector are synchronized, i.e. the input current is in phase with the input voltage). Fig. 7 shows the normalized switching losses for the conventional modulation method, c.f. (20) to (23) when the output current and output voltage are in phase. From Fig. 7 it appears that the switching losses averaged over a common time period for the input frequency and the output frequency, depends on the actual course over the surface. However, considering a general case, where the input frequency and the output frequency have no common time period, the average switching losses are calculated by integrating over the entire surface. Hence, to evaluate the different modulation methods with regards to the switching losses the following normalized switching loss function is defined:

$$\bar{p}_{sw,n} \quad \propto \quad \frac{1}{4\pi^2} \int_0^{2\pi} \int_0^{2\pi} (p_{sw,n}) d\Delta_g d\Delta_r \tag{39}$$

By the use of (39) the switching loss functions of the different modulators can be calculated for different load cases,

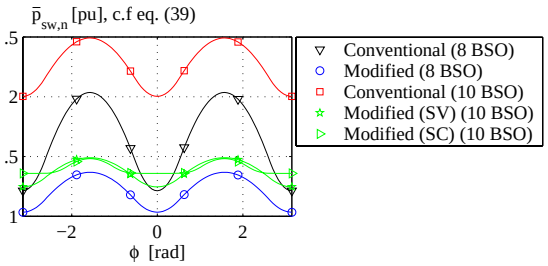

Fig. 8. The switching losses of the four different modulation functions for the matrix converter.

i.e. different angle ϕ_r between output voltage and output current. Fig. 8 shows the normalized switching loss functions for the different modulators as a function of the angle ϕ_r.

VII. Harmonic performance

When modulating the matrix converter in order to synthesize a desired output voltage and input current, harmonics are introduced at integer multiples of the switching frequency and at the side bands of all these frequencies. The harmonic content depends on the chosen modulation scheme and since this undesired frequency content causes torque ripple and additional copper losses in e.g. a motor load and increases the demands to the input filter, it is convenient to have a method to compare the harmonic behavior of different modulation schemes.

A. Output voltage

To evaluate the output voltage quality, the harmonic flux is considered [8]. In the N^{th} carrier cycle the harmonic flux $\tilde{\psi}$ is calculated by:

$$\tilde{\psi} = \int_{NT_{sw}}^{(N+1)T_{sw}} (\underline{V}_{rp} - \underline{V}^{\star}_{rp}) dt \tag{40}$$

where $\underline{V}_{rp}$ is a stationary output voltage vector and T_{sw} is the carrier period. To generalize the performance characterization, the per carrier harmonic flux error $\tilde{\psi}$ in (40), is normalized to the product of the nominal output voltage amplitude $|\underline{\hat{V}}_{rp}|$ and half the carrier period. That is:

$$\tilde{\psi}_n = \frac{2}{T_{sw}|\underline{\hat{V}}_{rp}|} \cdot \tilde{\psi} \tag{41}$$

The normalized per-carrier cycle RMS value of the harmonic flux $\tilde{\psi}_{RMS,n}$ can now be calculated by:

$$\langle \tilde{\psi}_{RMS,n} \rangle_{T_{sw}} = \sqrt{\int_0^1 \left(\tilde{\psi}_n \cdot \tilde{\psi}^*_n \right) dt} \tag{42}$$

where $\tilde{\psi}^*_n$ is the complex conjugate of $\tilde{\psi}_n$. Fig. 9 illustrates the harmonic flux trajectory for the conventional (8 BSO) modulation. Fig. 10 shows the per-carrier cycle RMS value of the harmonic flux as a function of the input angle Δ_g and the output angle Δ_r. The harmonic flux is plotted for a modulation index of 1. Evaluating for a general case, where the input frequency and the output frequency have no common time period, the RMS value of the harmonic flux is obtained by integrating over the

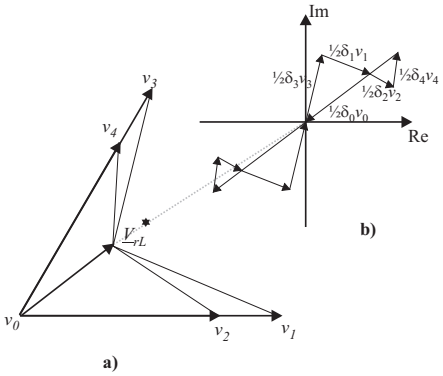

Fig. 9. Illustration of the per carrier harmonic flux trajectory. **a)** Output voltage hexagon (first segment). **b)** Resulting harmonic flux trajectory (conventional 8 BSO modulation scheme).

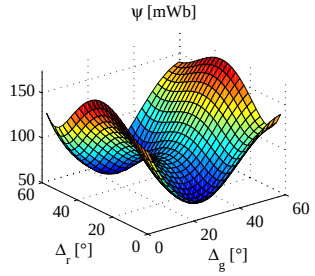

Fig. 10. The per-carrier cycle RMS value of the harmonic flux as a function of the input- and output angle for the conventional 8 BSO modulation strategy.

entire surface. The RMS value of the harmonic flux is calculated by:

$$\tilde{\psi}_{RMS,n} = \sqrt{\frac{1}{4\pi^2}\int_0^{2\pi}\int_0^{2\pi}\left(\langle\tilde{\psi}_{RMS,n}\rangle_{T_{sw}}\right)^2 d\Delta_g\, d\Delta_r} \qquad (43)$$

Fig. 11 shows the RMS-value of the harmonic flux as a function of the modulation index. It should be noted that for $\cos(\phi_g) \neq 1$ at the input, all curves in Fig. 11 would be changed.

B. Input current

When the input current to the matrix converter is modulated, the instantaneous error between the input current reference vector $\underline{I}^{\star}_{gp}$ and the chosen stationary input current vector $\underline{I}_{gp}$, results in a high frequency harmonic current. This harmonic current generates high stress on the input filter capacitors and has to be considered when designing the input filter for the matrix converter. Like for the voltage quality, the harmonic current content depends on the modulation method and hence an evaluation method is needed in order to compare the input waveform quality of the different modulation schemes.

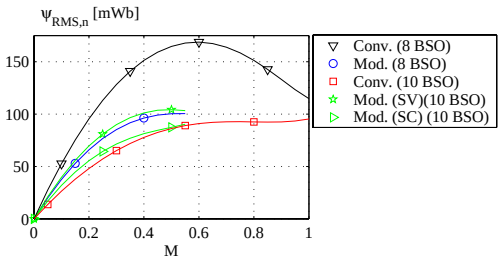

Fig. 11. The harmonic flux as a function of the modulation index, c.f. eq. (14).

In principle, the evaluation of the input current follows the same procedure as for the output voltage, however the evaluation parameter is changed from harmonic flux to harmonic charge $\tilde{Q}$. Further, the evaluation of the input current becomes a little more complex than the evaluation of the output voltage due to the fact that the amplitudes of the stationary input current vectors are affected by the output load angle ϕ_r. In the N$^{\text{th}}$ carrier cycle the harmonic charge $\tilde{Q}$ is calculated by:

$$\tilde{Q} = \int_{NT_{sw}}^{(N+1)T_{sw}} (\underline{I}_{gp} - \underline{I}^{\star}_{gp})dt \qquad (44)$$

where $\underline{I}_{gp}$ is a stationary input current vector. The amplitude of the per carrier harmonic charge is a function of the input current angle, the output voltage angle, the modulation depth and the output load angle ϕ_r. To obtain a comparison, independent of the switching frequency and power level, the harmonic charge in (44) is normalized by:

$$\tilde{Q}_n = \frac{4\tilde{Q}}{\sqrt{3}\cdot T_{sw}\cdot \hat{i}_{rp}} \qquad (45)$$

where $\hat{i}_{rp}$ is the amplitude of the output current. The normalized per-carrier cycle RMS value of the harmonic charge $\tilde{Q}_{RMS,n}$ can be calculated by:

$$\langle\tilde{Q}_{RMS,n}\rangle_{T_{sw}} = \sqrt{\int_0^1 \left(\tilde{Q}_n \cdot \tilde{Q}^*_n\right) dt} \qquad (46)$$

where $\tilde{Q}^*_n$ is the complex conjugate of $\tilde{Q}_n$. Evaluating for a general case, where the input frequency and the output frequency has no common time period, the RMS value of the harmonic charge is obtained by integrating over the entire surface. The RMS value of the harmonic charge is calculated by:

$$\tilde{Q}_{RMS,n} = \sqrt{\frac{1}{4\pi^2}\int_0^{2\pi}\int_0^{2\pi}\left(\langle\tilde{Q}_{RMS,n}\rangle_{T_{sw}}\right)^2 d\Delta_g\, d\Delta_r} \qquad (47)$$

Fig. 12 shows the normalized harmonic charge $\tilde{Q}_{RMS}$ vs. the modulation index for different load angles.

VIII. Simulation ad test results

A. Test setup

To validate the functionality of the proposed modified space vector approach and to compare the different modulation schemes in the time domain, a flexible laboratory test setup was built. Table III and Table IV show the characteristics of the test setup and specifying different test conditions.

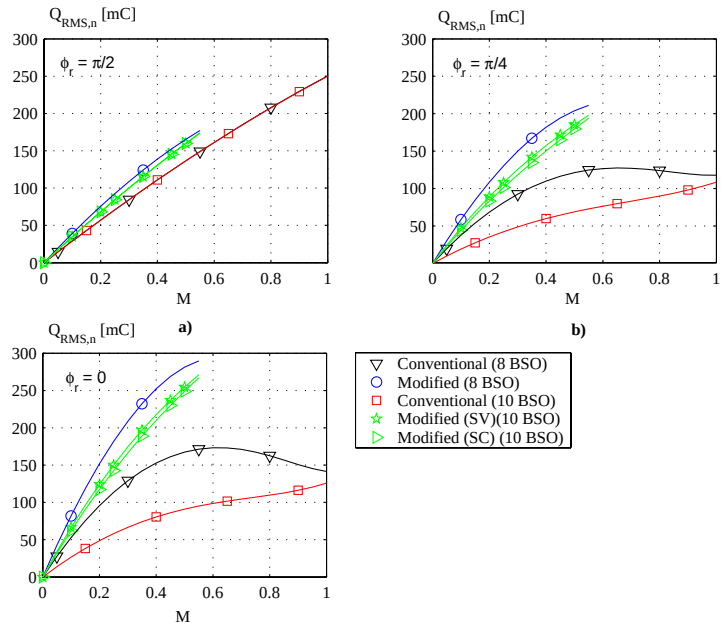

Fig. 12. The normalized harmonic charge distortion as a function of the modulation index, c.f. (14) for different load angles. **a)** load angle equals $\pi/2$. **b)** load angle equals $\pi/4$. **c)** load angle equals 0.

TABLE III
SIMULATION CONDITIONS (MATRIX CONVERTER)

Switching frequency	f_{sw}	3550	[Hz]
Power factor	$\cos(\phi_g)$	1	
Input inductance	L_f	300	[μH]
Input capacitor	C_f	61.0	[μF]
Input voltage (l-l)	V_g	400	[V]
Modulation index	M	0.58	
Input frequency	f_g	50	[Hz]
Output frequency	f_r	25	[Hz]

TABLE IV
SIMULATION CONDITIONS (INDUCTION MOTOR)

Nominal power	P_{im}	15	[kW]
Power factor	$\cos(\phi_r)$	0.84	
Pole pair	N	2	
Stator resistance	R_s	0.36	[Ω]
Rotor resistance	R_r	0.26	[Ω]
Leakage inductance	L_s	2.2	[mH]
Leakage inductance	L_r	2.2	[mH]
Mag. inductance	L_m	46.6	[mH]

TABLE V
TOTAL HARMONIC CURRENT DISTORTION (THD_i) [%]

f_r	M	**Conv. (8 BSO)**		**Mod. (8 BSO)**		**Conv. (10 BSO)**		**Mod. (SV)(10 BSO)**	
		Input	Output	Input	Output	Input	Output	Input	Output
15.0	0.35	7.30	5.57	13.01	3.69	2.86	2.87	12.20	3.85
20.0	0.46	8.87	5.87	15.84	3.72	3.42	3.11	14.33	3.87
25.0	0.58	9.14	5.57	16.68	3.43	4.03	3.07	15.93	3.49
30.0	0.69	8.30	5.10	-	-	4.37	2.99	-	-
35.0	0.81	7.15	3.95	-	-	4.66	2.60	-	-
40.0	0.92	6.10	3.06	-	-	4.89	2.39	-	-
42.5	0.98	5.87	2.73	-	-	5.00	2.34	-	-

B. Simulated results

Fig. 13 shows the simulated waveforms of the conventional (8 BSO) modulation scheme and the modified (8 BSO) modulation scheme. Fig. 14 shows the simulated waveforms for the conventional (10 BSO) modulation scheme and the modified (10 BSO) modulation scheme (SV). For each of the simulated currents, the corresponding total harmonic current distortion (THD_i) is calculated (upper right corner of the trace). Besides the conditions simulated in Fig. 13 and Fig. 14, Table V shows the total harmonic current distortion in the entire speed range. From the results in Fig. 13, Fig. 14 and Table V it appears that both with regards to the output voltage quality and the input current quality, the conventional (10 BSO) modulation scheme shows the best results. Regarding the 8 BSO modulation schemes, the proposed solution shows better output performance than the conventional method while regarding the input performance the conventional scheme is superior.

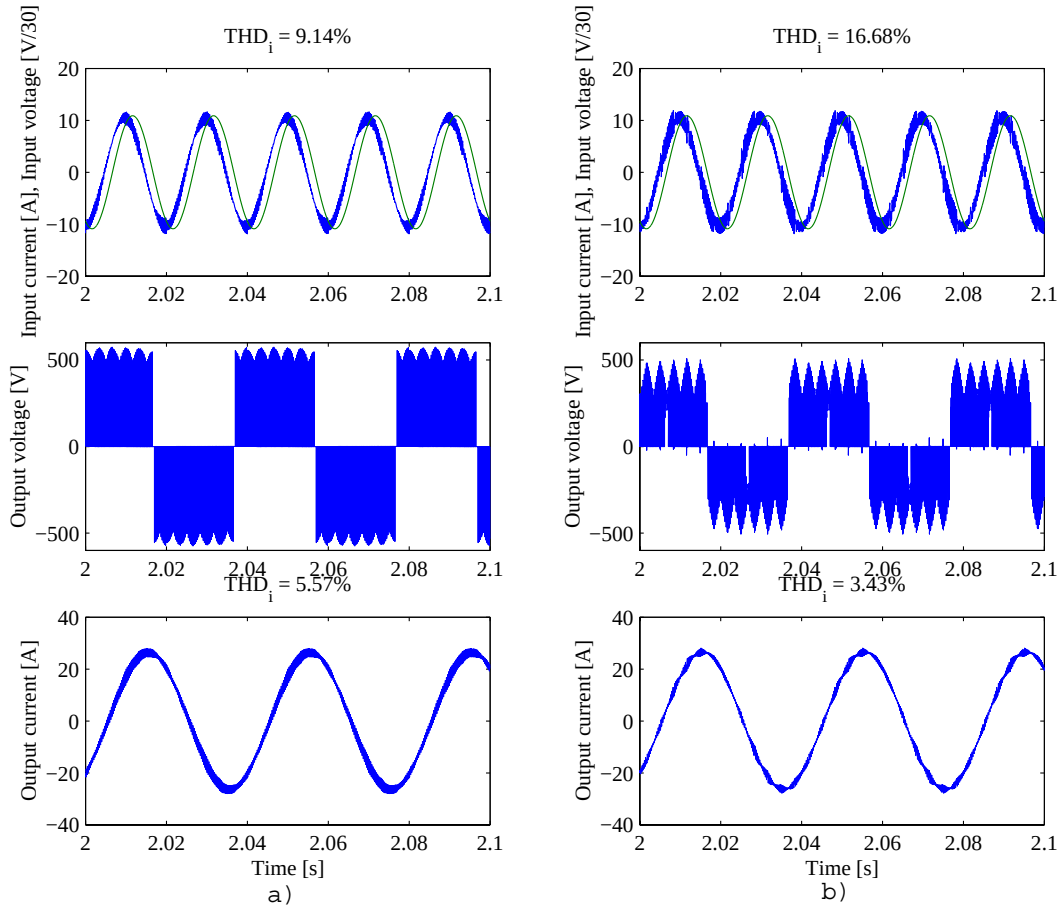

Fig. 13. Simulation results. **a)** The conventional modulation method (8 BSO). **b)** The modified modulation method (8 BSO). The upper curves show the input currents and the input voltage, the curves in the middle show the output voltages and the lower plots show the output currents. Simulation conditions are given in Table III and Table IV.

C. Experimental results

Figs. 15-17 show the experimentally obtained waveforms. Fig. 15 shows the measured waveforms for the conventional 8 BSO modulation scheme, Fig. 16 shows it for the conventional 10 BSO scheme and Fig. 17 represents the modified 8 BSO scheme.

IX. Conclusion

This paper has presented a new loss reduced modulation scheme for three-phase to three-phase matrix converters. The new modulation scheme is applicable whenever the output voltage reference is below half the input voltage. The proposed scheme reduces the switching losses by 15-35% dependent on the load angle at the output of the converter. To evaluate the proposed modulation method and matrix converter modulation schemes in general, an evaluation method is proposed, regarding the three crucial modulation properties - the switching losses, the output voltage quality and the input current quality. Four different modulation schemes are evaluated. To demonstrate the functionality of the loss reduced modulation method and to some extent validate the proposed evaluation method, a matrix converter motor drive was simulated, using the four considered modulation schemes. It turned out (both from the analytical method and from the simulations) that regarding the input and output waveform quality, the conventional (10 BSO) modulation strategy was superior while regarding the switching losses, the new modified (8 BSO) modulation was the most efficient. Finally, the functionality of some of the discussed modulation schemes were demonstrated by experimental results.

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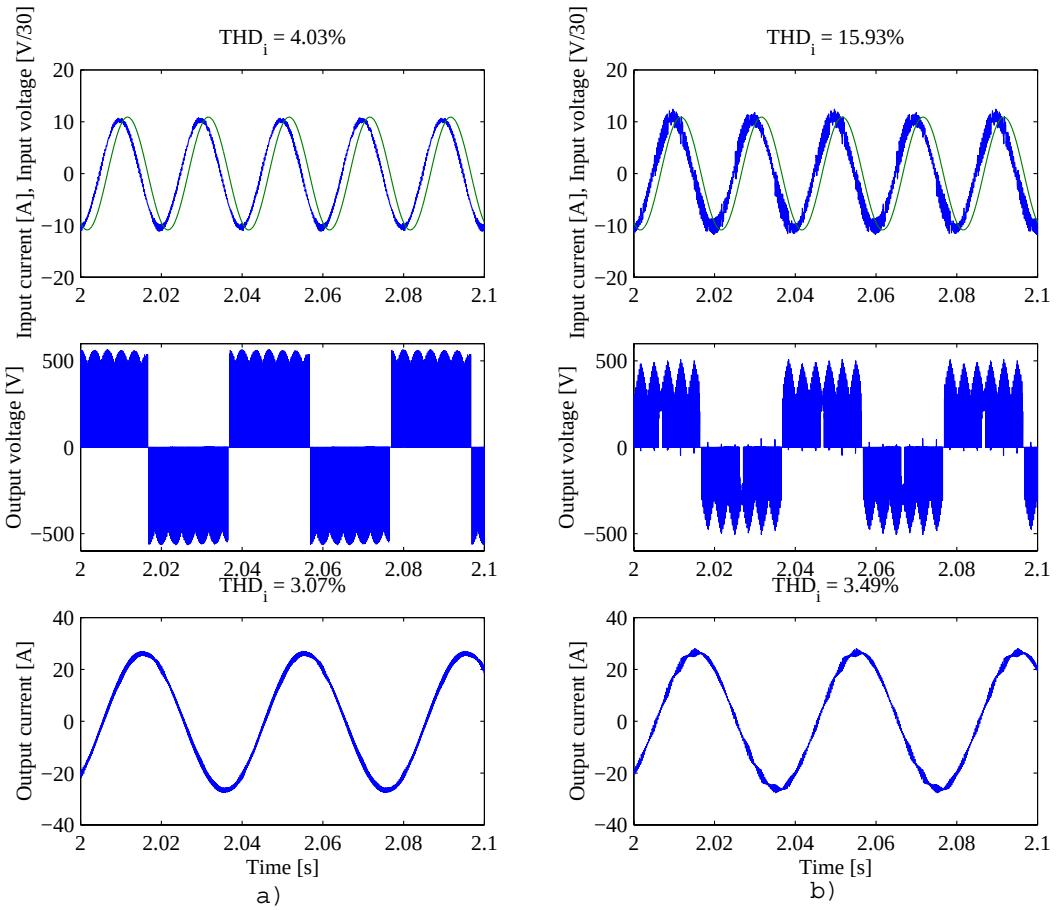

Fig. 14. Simulation results. **a)** The conventional modulation method (10 BSO). **b)** The modified modulation method (10 BSO SV). The upper curves show the input currents and the input voltage, the curves in the middle show the output voltages and the lower plots show the output currents. Simulation conditions are given in Table III and Table IV.

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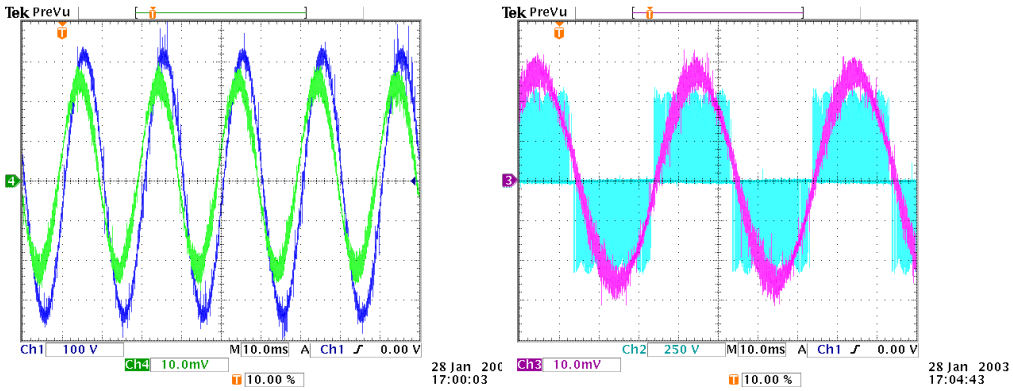

Fig. 15. Measured waveforms for the conventional 8 BSO scheme. Left: Input current and input voltage. Right: Output current and output voltage.

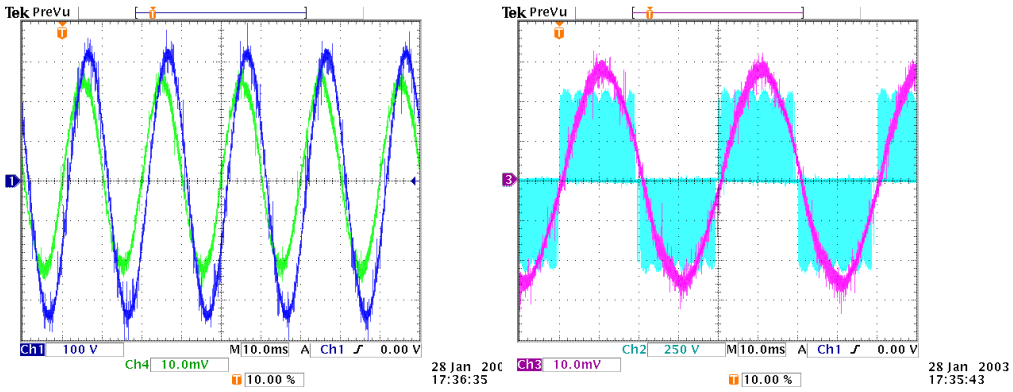

Fig. 16. Measured waveforms for the conventional 8 BSO scheme. Left: Input current and input voltage. Right: Output current and output voltage.

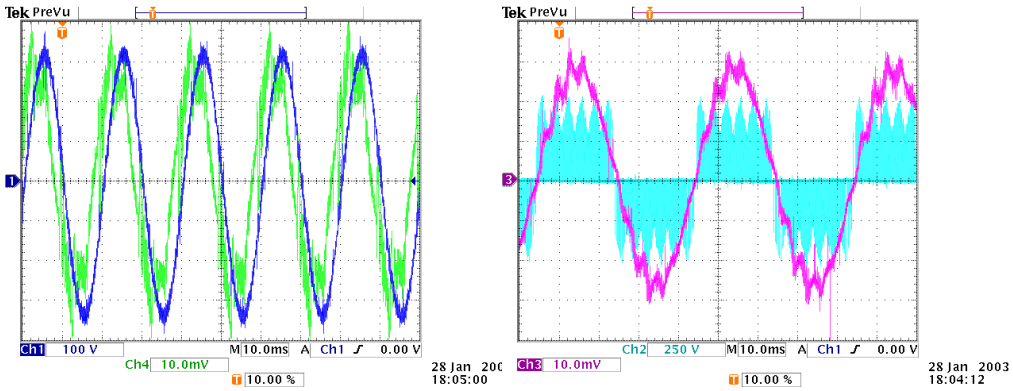

Fig. 17. Measured waveforms for the modified 8 BSO scheme. Left: Input current and input voltage. Right: Output current and output voltage.

Appendix F

Generalized Discontinuous DC-link Balancing Modulation Strategy for Three-level Inverters, PCC 2002

Generalized Discontinuous DC-link Balancing Modulation Strategy for Three-level Inverters

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Abstract— **This paper presents a new generalized discontinuous space-vector modulation approach applicable to Neutral Point Clamped (NPC) inverters. By the proposed modulation scheme the DC-link voltage can be actively controlled to maintain a stable neutral point even if unbalanced loading of the DC-link capacitors occur due to e.g. nonlinear loads containing even harmonics. The maximum unbalance for which the modulation scheme are able to compensate is theoretically investigated and found to be a function of both load angle, modulation index and output power level. The proposed modulation method is compared to conventional modulation schemes with regard to both switching losses and wave form quality. For the same number of switchings, the proposed modulation scheme offers up to 25% lower switching losses than conventional modulation schemes while maintaining the same output wave form quality. The functionality of the modulation scheme is validated by simulation results.**

I. Introduction

Since the introduction of the Neutral Point Clamped (NPC) inverter [1], c.f. Fig. 1a, this inverter has mainly been applied for high voltage- and low switching frequency power conversion applications. However, progressing advance in computational power processors and in solid state switching devices, such as the IGBT, makes the NPC inverter applicable also in high switching frequency application [2, 3]. Considering low switching frequency applications ($f_{sw} < 1$ kHz), a lot of research have been concerned about calculating optimal switching patterns to eliminate low order harmonics in the output voltage [4, 5, 6]. As the switching frequency increases, research on harmonic voltage elimination recedes while problems like reduction of switching losses becomes more urgent [7]. A simple method to reduce the switching losses of a three-level converter is to employ the discontinuous modulation schemes known from conventional two-level voltage source inverters (VSI) [8]. However, a non-modified adoption of these discontinuous two-level VSI modulation schemes is only functional when the voltage-levels in the three-level converter is built from separate DC-sources [9]. When series capacitors are used to divide the DC-link voltage, three-level inverters (and multi-level inverters in general) have a DC-link voltage unbalance problem due to the following reasons:

- Unequal capacitor values due to manufacture tolerances.
- Unequal loading of the capacitors due to unintended switching delays.
- Unequal loading of the capacitors due to e.g. non-linear loads containing even order harmonics [10].

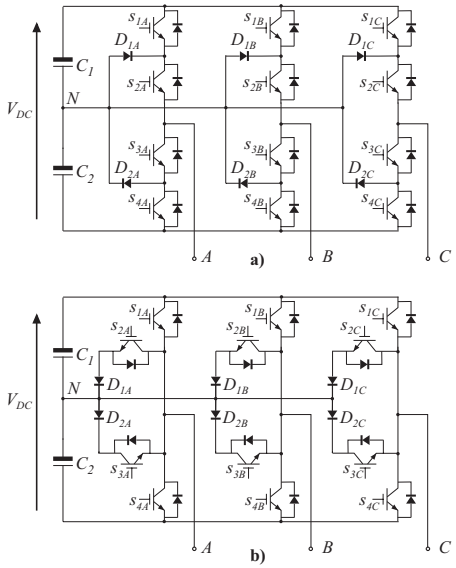

Fig. 1. Three-level NPC inverter topologies. **a)** Conventional NPC inverter [1]. **b)** Modified NPC-inverter [16].

Several methods have been proposed to solve the voltage unbalance problem, among these, the use of separate DC voltage sources [11] and active voltage regulators [12]. Unfortunately, these solutions clearly add to the complexity of the system and is not suitable in many applications [13]. In [14] and [15], two different voltage balancing techniques were proposed, where the redundancy of the switch state vectors were attributed to stabilize the DC-link voltage within each switching period. However, these methods are incapable of adopting the features of the discontinuous modulation schemes. This paper presents a new generalized discontinuous DC-link balancing modulation strategy for NPC-inverters. The proposed modulation scheme is based on the space-vector approach and provides the following features:

- Discontinuous modulation with the clamping period centered at the peak of the phase current.
- DC-link voltage balancing, even with unequal loading of the DC-link capacitors or different capacitor values.
- No need for additional hardware to perform the DC-link balancing.

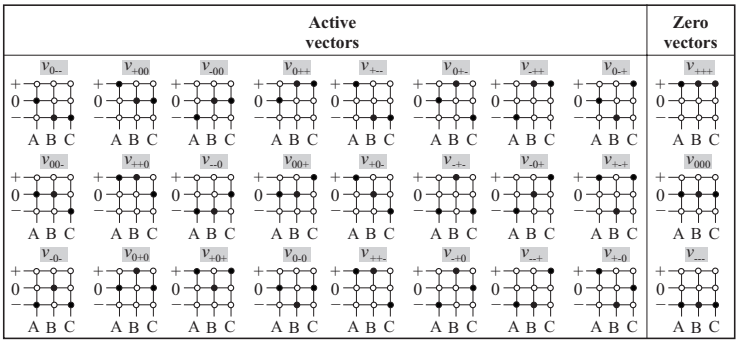

Fig. 2. Switch combinations for the three-level inverter.

The paper first reviews the topologies of NPC-type inverters and then summarizes the space-vector analysis applied for three-level inverters. Then the proposed modulation scheme is presented and compared to conventional schemes, both with regards to switching losses and wave form quality. The proposed modulation scheme is validated, by simulation results.

II. Neutral point clamped VSI

A. Configurations of the NPC inverter

Fig. 1a shows the conventional three-level NPC inverter proposed by [1]. In the conventional NPC inverter topology, each of the switches $s_{1A}..s_{4C}$ and the diodes $D_{1A}..D_{2C}$ only have to block half the DC-link voltage. Hence, the conventional NPC is well suited for high voltage applications. A topology derived from the conventional NPC inverter is shown in Fig 1b and was proposed by [16]. Compared to the conventional NPC inverter, the salient features of this topology are: Lower conducting losses in the high modulation range, due to the fact that only one semiconductor device provides the path to the upper and lower DC-bus bar. Secondly, intelligent half bridge modules like the Skiip-pack modules from SEMIKRON are directly applicable to this configuration. Although the modified NPC inverter only switches half the DC-link voltage (if modulated properly), the upper and lower switches still need to have the ability to block the total DC-link voltage. Hence this topology is not suited in high voltage applications. The modulation scheme proposed in this paper is directly applicable for both types of inverters in Fig. 1.

B. Variation of the neutral point potential

According to Fig. 1a an excessive high voltage may be applied to the switching devices if the neutral point N varies from the center potential of the DC-link. Further, both NPC type inverters in Fig. 1 may be unable to synthesize the reference voltage if too large neutral point voltage variations occur. By inspection of Fig. 1 it appears that the NPC inverter has 27 legal switching states. These switching states are summarized in Fig. 2 and it appears that with regards to output voltage, several of these switch states are redundant (in pairs). For instance, the switch combinations v_{0--} and v_{+00} produce exactly

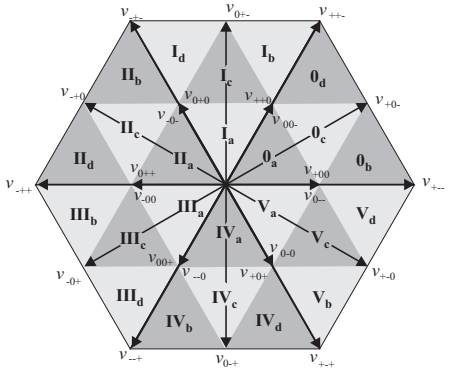

Fig. 3. The space vector hexagon for the three-level VSI.

the same output voltage (provided that the neutral point voltage is balanced) but with regards to the current flowing to/from the neutral point these two switch states behaves in the opposite manner. Hence, the selection among the redundant switch states has a vital influence on the neutral point potential and can actively be used to control/reestablish the neutral point voltage.

III. Vector analysis of the switching combinations

For the purpose of space vector modulation, the output voltage references $v_A^\star$, $v_B^\star$ and $v_C^\star$ and the output currents i_A, i_B and i_C are transformed into the complex space vector plane by the following transformation:

$$\underline{V}_s^\star = \frac{2}{3}\left(v_A^\star + v_B^\star \cdot e^{j\cdot\frac{2\pi}{3}} + v_C^\star \cdot e^{j\cdot\frac{4\pi}{3}}\right) \quad (1)$$

$$\underline{I}_s = \frac{2}{3}\left(i_A + i_B \cdot e^{j\cdot\frac{2\pi}{3}} + i_C \cdot e^{j\cdot\frac{4\pi}{3}}\right) \quad (2)$$

Applying (1) on the switch combinations in Fig. 2, the well known space vector hexagon in Fig. 3 is obtained.

A. Sector location

As indicated in Fig. 3 the space vector hexagon is divided in six main sectors (**0..V**) and 24 sub sectors (**0a..V d**). The first step in the space vector approach is to determine the sector location. Due to the symmetry

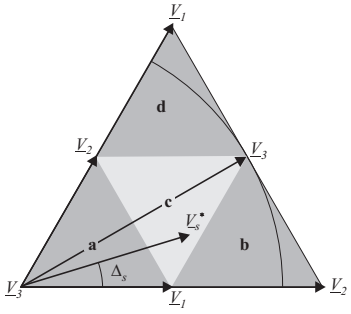

Fig. 4. The space vector hexagon for the three-level VSI.

of the six main sectors, it is convenient to define the angle Δ_s of the rotating voltage reference vector as:

$$\Delta_s = \mod\left(\omega_s t + \frac{\pi}{6}, \frac{\pi}{3}\right) \tag{3}$$

where $\omega_s t = 0$ is defined as the positive zero crossing of the phase A reference voltage ($v_A^\star = \hat{v}_A \cdot \sin(\omega_s t)$). By this, the angle Δ_s is in the interval: $\Delta_s \in [0..\frac{\pi}{3}]$. This is illustrated in Fig. 4. Due to the angle definition in (3) it is only necessary to monitor the six main sectors **0-V** and then identify whether the sector location is **a**, **b**, **c** or **d**. Defining the modulation index M as:

$$M = \frac{\sqrt{3}|\underline{V}_s^\star|}{V_{DC}} \tag{4}$$

the sector location can be determined, simply by applying the law of sines. By this, the following constrains are obtained:

$$Sector = \begin{cases} \mathbf{a} \text{ if } \left(M \le \frac{1}{2\sin(2\pi/3-\Delta_s)}\right) \\ \mathbf{b} \text{ if } \left(M > \frac{1}{2\sin(\pi/3-\Delta_s)}\right) \\ \mathbf{c} \text{ if } \begin{pmatrix} \left(M > \frac{1}{2\sin(2\pi/3-\Delta_s)}\right) \ \& \\ \left(M \le \frac{1}{2\sin(\pi/3-\Delta_s)}\right) \ \& \\ \left(M \le \frac{1}{2\sin(\Delta_s)}\right) \end{pmatrix} \\ \mathbf{d} \text{ if } \left(M > \frac{1}{2\sin(\Delta_s)}\right) \end{cases} \tag{5}$$

B. Vector time intervals

With reference to Fig. 4, the reference voltage vector $\underline{V}_s^\star$ can be obtained by applying the three adjacent stationary vectors for an angle dependent time duration. In general the following matrix equation has to be solved:

$$\begin{bmatrix} \Im m(\underline{V}_s^\star) \\ \Re e(\underline{V}_s^\star) \\ 1 \end{bmatrix} = \begin{bmatrix} \Im m(\underline{V}_1) & \Im m(\underline{V}_2) & \Im m(\underline{V}_3) \\ \Re e(\underline{V}_1) & \Re e(\underline{V}_2) & \Re e(\underline{V}_3) \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \delta_1 \\ \delta_2 \\ \delta_3 \end{bmatrix} \tag{6}$$

where $\underline{V}_1$, $\underline{V}_2$ and $\underline{V}_3$ are the three adjacent stationary vectors, c.f. Fig 4. Based on the sector identification, the on-time ratios $\delta_{1..3}$ can be calculated. Solving (6) for the voltage reference vector located in sector X_a gives:

$$\begin{aligned} \delta_{1a} &= 2 \cdot M \cdot \sin\left(\frac{\pi}{3} - \Delta_s\right) \\ \delta_{2a} &= 2 \cdot M \cdot \sin(\Delta_s) \\ \delta_{3a} &= 1 - \delta_1 - \delta_2 \end{aligned} \tag{7}$$

Solving for the voltage reference vector located in sector X_b gives:

$$\begin{aligned} \delta_{1b} &= 2 - \sqrt{3} \cdot M \cdot \cos(\Delta_s) - M \cdot \sin(\Delta_s) \\ \delta_{2b} &= \sqrt{3} \cdot M \cdot \cos(\Delta_s) - M \cdot \sin(\Delta_s) - 1 \\ \delta_{3b} &= 2 \cdot M \cdot \sin(\Delta_s) \end{aligned} \tag{8}$$

Solving for the voltage reference vector located in sector X_c gives:

$$\begin{aligned} \delta_{1c} &= 1 - 2 \cdot M \cdot \sin(\Delta_s) \\ \delta_{2c} &= 2 \cdot M \cdot \sin\left(\Delta_s - \frac{\pi}{3}\right) + 1 \\ \delta_{3c} &= 2 \cdot M \cdot \sin\left(\Delta_s + \frac{\pi}{3}\right) - 1 \end{aligned} \tag{9}$$

And finally, solving for the voltage reference vector located in sector X_d gives:

$$\begin{aligned} \delta_{1d} &= 2 \cdot M \cdot \sin(\Delta_s) - 1 \\ \delta_{2d} &= 2 - \sqrt{3} \cdot M \cdot \cos(\Delta_s) - M \cdot \sin(\Delta_s) \\ \delta_{3d} &= \sqrt{3} \cdot M \cdot \cos(\Delta_s) - M \cdot \sin(\Delta_s) \end{aligned} \tag{10}$$

The duty-cycle expressions in (7) to (10) are at any instant of time limited by the following constraint:

$$0 \le \delta_{ij} \le 1 \qquad \begin{matrix} i \in [1,2,3] \\ j \in [\text{a, b, c, d}] \end{matrix} \tag{11}$$

IV. Vector sequences

In the two-level inverter, the redundant switching states v_{000} and v_{111}, have been used to develop several discontinuous modulation schemes, providing a switching loss reduction of 50% compared to conventional modulation schemes [17]. However, these discontinuous modulation schemes can not be applied directly to the capacitor split three level inverter because they do not provide any control of the DC-link neutral potential. Hence, in order to be applied to the NPC inverter, the discontinuous modulation schemes of the two-level inverter has to be modified.

A. Discontinuous modulation scheme

In the explanation of the generalized discontinuous modulation scheme, Fig. 5 is used as an illustration. In Fig. 5 the voltage reference vector $\underline{V}_s^\star$ is located in sector $\mathbf{0_C}$ at an angle Δ_s, c.f. (3). The current vector $\underline{I}_s$ is lagging the voltage reference vector by the angle ϕ_s where ϕ_s is considered positive when lagging the voltage vector and negative when leading the voltage vector. To realize the voltage reference vector, it appears that five different switching states form the three adjacent stationary vectors, This redundancy can be used to avoid switchings of one phase leg. Actually, in the present case, $|\underline{V}_s^\star|$ can be synthesized by either (12) or (13):

$$v_{+0-} \rightarrow v_{+00} \rightarrow v_{++0} \rightarrow v_{+00} \rightarrow v_{+0-} \tag{12}$$

$$v_{+0-} \rightarrow v_{00-} \rightarrow v_{0--} \rightarrow v_{00-} \rightarrow v_{0--} \tag{13}$$

In (12), no switchings occur in phase leg A while phase leg C is clamped during the sequence in (13). Regarding switching losses, the switching sequence, clamping the leg carrying the highest current should be chosen. For this

TABLE I

SWITCHING TABLE FOR THE GENERALIZED DISCONTINUOUS MODULATION METHOD

→**Sub sector**	**a**			**b**			**c**			**d**		
↓ **if** $\Delta_s \leq \frac{\pi}{6} + \phi'_s + n \cdot \phi_c$	δ_3	δ_2	δ_1	δ_2	δ_3	δ_1	δ_3	δ_1	δ_2	δ_3	δ_1	δ_2
Sector 0	000	00−	0−−	+−−	+0−	+00	+0−	+00	++0	+0−	++−	++0
Sector I	000	0+0	++0	++−	0+−	00−	0+−	00−	−0−	0+−	−+−	−0−
Sector II	000	−00	−0−	−+−	−+0	0+0	−+0	0+0	0++	−+0	−++	0++
Sector III	000	00+	0++	−++	−0+	−00	−0+	−00	−−0	−0+	−−+	−−0
Sector IV	000	0−0	−−0	−−+	0−+	00+	0−+	00+	+0+	0−+	+−+	+0+
Sector V	000	+00	+0+	+−+	+−0	0−0	+−0	0−0	0−−	+−0	+−−	0−−
↓ **if** $\Delta_s > \frac{\pi}{6} + \phi'_s + n \cdot \phi_c$	δ_3	δ_1	δ_2	δ_3	δ_2	δ_1	δ_3	δ_2	δ_1	δ_1	δ_3	δ_2
Sector 0	000	+00	++0	+0−	+−−	0−−	+0−	00−	0−−	++−	+0−	00−
Sector I	000	00−	−0−	0+−	++−	++0	0+−	0+0	++0	−0−	0+−	0+0
Sector II	000	0+0	0++	−+0	−+−	−0−	−+0	−00	−0−	−++	−+0	−00
Sector III	000	−00	−−0	−0+	−++	0++	−0+	00+	0++	−−+	−0+	00+
Sector IV	000	00+	+0+	0−+	−−+	−−0	0−+	0−0	−−0	+−+	0−+	0−0
Sector V	000	0−0	0−−	+−0	+−+	+0+	+−0	+00	+0+	+−−	+−0	+00

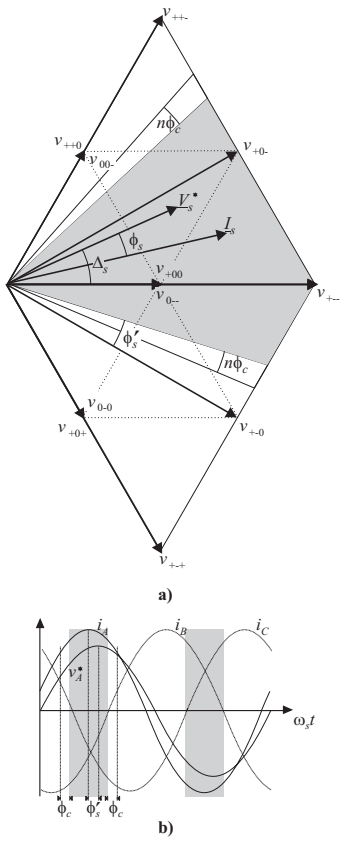

Fig. 5. Definitions of clamping interval angle ϕ'_s and DC-link balancing angle ϕ_c. **a)** in the complex space vector domain. **b)** in the time domain.

purpose, the angle ϕ'_s is introduced, c.f. Fig 5 and defined as:

$$\phi'_s = \begin{cases} \phi_s & \text{if} \quad -\frac{\pi}{6} \leq \phi_s \leq \frac{\pi}{6} \\ -\frac{\pi}{6} & \text{if} \quad \phi_s < -\frac{\pi}{6} \\ \frac{\pi}{6} & \text{if} \quad \phi_s > \frac{\pi}{6} \end{cases}$$

The angle ϕ'_s determines the angular rotation of the phase clamping interval. In Fig. 5 the shaded area illustrates the

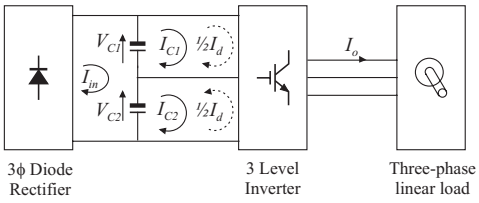

Fig. 6. Definitions of the currents and voltages used for DC-link balancing.

TABLE II

DEFINITION OF THE SIGN OPERATOR n

	a	**b**	**c**	**d**
Even Sec.	-Sign(P_o)	Sign(P_o)	Sign(P_o)	Sign(P_o)
Odd Sec.	Sign(P_o)	-Sign(P_o)	-Sign(P_o)	-Sign(P_o)

interval where phase leg A should be clamped. Generalizing the above description to an arbitrary voltage reference location, Table I is obtained.

B. DC-link balancing considerations

So far, the modulation strategy offers no ability for compensating a DC-link voltage unbalance, and since no redundant switch states are used within a switching period, DC-link balancing can not be obtained by adjusting the on-times for such redundant switch states. Using Fig. 6, DC-link voltage balance is obtained when the following condition is satisfied:

$$\begin{aligned} \langle I_{C1} \rangle_{T_0} + \frac{1}{2} \langle I_d \rangle_{T_0} &= \langle I_{C2} \rangle_{T_0} - \frac{1}{2} \langle I_d \rangle_{T_0} \\ \Downarrow & \qquad (14) \\ \langle I_d \rangle_{T_0} &= (\langle I_{C2} \rangle_{T_0} - \langle I_{C1} \rangle_{T_0}) \end{aligned}$$

where I_{C1} and I_{C2} are the DC-link currents originating from the linear balanced load of the three level converter and I_d represents the unbalanced loading of the inverter. The notation $\langle X \rangle_{T_0}$ indicates that the quantity is averaged over a fundamental having the time period T_0. From (14) it appears that an unbalance may be compensated by adjusting the ratio between $\langle I_{C1} \rangle_{T_0}$ and $\langle I_{C2} \rangle_{T_0}$. For this purpose, the angle $n \cdot \phi_c$ is introduced, c.f. Fig 5, where the sign operator n is defined in accordance with Table II and ϕ_c is defined in the interval $\phi_c \in [-\frac{\pi}{6}..\frac{\pi}{6}]$. Further

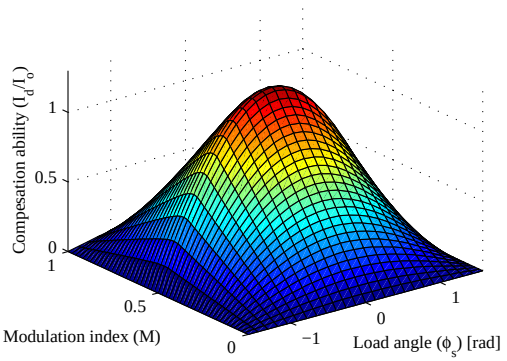

Fig. 7. DC-link load unbalance for which the modulation scheme is able to compensate.

the angle ϕ'_s defined in (14) is modified by:

$$\phi'_s = \left(1 - \frac{\phi_c}{\frac{\pi}{6}}\right)\phi'_s \tag{15}$$

From Fig. 5, Table I and Table II it appears that by increasing/decreasing the angle ϕ_c, the load on capacitor C_1 can be increased/decreased. Hence, the angle ϕ_c can be used to compensate unbalanced loading of the DC-link. To evaluate the ability of the proposed DC-link balancing technique, the current through capacitor C_1 and C_2 have to be calculated: (Eq. (16) is only formulated for sector $\mathbf{0_a}$ and in (16) it is provided that the modulation index is below 0.5.)

$$\begin{aligned}\langle I_{C1}\rangle_{T0} &= \frac{1}{2\pi}\left(\int_{\frac{\pi}{6}+\phi'_s+n\phi_c}^{\frac{\pi}{6}} (\delta_1 \cdot i_A + \delta_2 \cdot i_C)d\Delta_{vs} + ...\right. \\ \langle I_{C2}\rangle_{T0} &= \frac{1}{2\pi}\left(\int_{0}^{\frac{\pi}{6}+\phi'_s+n\phi_c} (\delta_1 \cdot i_A + \delta_2 \cdot i_C)d\Delta_{vs} + ...\right.\end{aligned} \tag{16}$$

Extending 16 to arbitrary values of the modulation index M, and calculating for $\phi_c = \pm\frac{\pi}{6}$ the maximum unbalance, for which the modulation scheme is able to compensate may be calculated. Fig. 7 shows the ability of the proposed modulation scheme to compensate DC-link unbalances. In Fig. 7 the unbalanced current I_d is normalized to the output current I_o originating from the linear loading of the inverter and plotted against the modulation index M and load angle ϕ_s. From Fig. 7 it appears that the maximum load unbalance which can be actively compensated is when the load angle is zero, e.g. a resistive load and the modulation index is about 0.52.

V. Performance evaluation

The performance evaluation of the proposed modulation scheme addresses the two important modulation scheme characteristics - switching losses and wave form quality.

A. Switching loss considerations

Assuming the switching devices of the NPC inverter to have linear current and voltage turn-on and turn-off characteristics with respect to time and accounting only

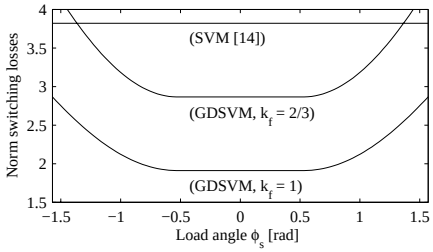

Fig. 8. Normalized switching losses versus load angle ϕ_s.

for the fundamental component of the output current, the switching losses of the NPC inverter can be analytically modeled as:

$$p_{sw} \propto \frac{V_{DC}}{2}\frac{(T_{on}+t_{off})}{2\cdot T_s}\frac{1}{2\pi}\int_0^{2\pi} i_{sw}d\theta \tag{17}$$

where i_{sw} is the current through the switching device at the switching instant and t_{on} and t_{off} are the turn-on and turn-off times of the switching device. Normalizing (17) to the peak output current, the half of the DC-link voltage the turn-on and turn-off times and the half of the switching frequency, the normalized switching losses becomes:

$$\overline{p}_{sw} = \frac{1}{2\pi}\int_0^{2\pi} \overline{i}_{sw}d\theta \tag{18}$$

Fig. 8 compares the switching losses of the generalized discontinuous modulation scheme and the conventional modulation scheme [14] when operated at the same switching frequency ($k_f = 1$). Since the discontinuous modulation scheme only involves $\frac{2}{3}$ times the number of switchings of the conventional modulation method, it might be more fair to compare the modulation schemes for the same number of switchings ($k_f = \frac{2}{3}$).

B. Wave form quality

When modulating the three-level converter in order to synthesize a desired output voltage, harmonics are introduced at integer multiples of the switching frequency and at the side bands of all these frequencies. The harmonic content depends on the chosen modulation scheme and since this undesired frequency content causes torque ripple and additional copper losses in e.g. a motor load, it is convenient to have a method to compare the harmonic behavior of different modulation schemes. In general, harmonic analysis can be done by either FFT or harmonic distortion factor (HDF). For a quantitative analysis, HDF is most suitable and hence the proposed modulation scheme is evaluated with regards to the HDF [18].

In the N^{th} carrier cycle the harmonic flux $\tilde{\psi}$ is calculated by:

$$\tilde{\psi} = \int_{NT_s}^{(N+1)T_s} (\underline{V}_s - \underline{V}_s^{\star})dt \tag{19}$$

where $\underline{V}_s$ is a stationary output voltage vector. To generalize the performance characterization, the per carrier harmonic flux error $\tilde{\psi}$ in (19), is normalized to the product of the nominal output voltage amplitude $|\underline{\hat{V}}_s|$ and half

TABLE III

TEST SETUP CONDITIONS (NPC INVERTER)

Switching frequency	f_{sw}	2.0	[kHz]
DC-link capacitors	C_1 C_2	10.0	[mF]
DC-link inductor	L_f	50	[μF]
Load resistor	R_l	20	[Ω]
Input voltage (l-l)	V_g	400	[V]
Modulation index	M	0.8	
Input frequency	f_i	50	[Hz]
Output frequency	f_o	40	[Hz]

TABLE IV

TEST SETUP CONDITIONS (INDUCTION MOTOR)

Nom. power	P_{im}	22.0	[kW]
Nom. Cos(ϕ)			
Pole pair	N	2	
Stator resistance	R_s	0.100	[Ω]
Rotor resistance	R_r	0.086	[Ω]
Leakage inductance	L_s	1.817	[mH]
Leakage inductance	L_r	1.211	[mH]
Mag. inductance	L_m	27.936	[mH]

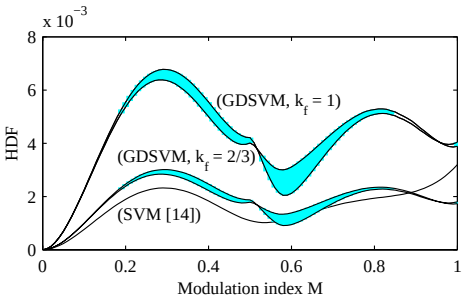

Fig. 9. Harmonic flux distortion of the conventional modulation scheme (SVM) and of the generalized discontinuous modulation scheme (GDSVM).

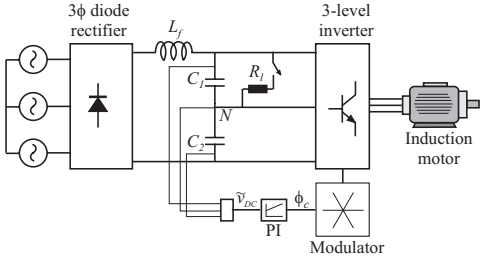

Fig. 10. The test setup used to validate the proposed modulation scheme.

the switching period. That is:

$$\tilde{\psi}_n = \frac{2}{T_s|\hat{V}_s|} \cdot \tilde{\psi} \tag{20}$$

The normalized per-carrier cycle RMS value of the harmonic flux $\tilde{\psi}_{RMS,n}$ can now be calculated by:

$$\langle \tilde{\psi}_{RMS,n} \rangle_{T_s} = \sqrt{\int_0^1 \left(\tilde{\psi}_n \cdot \tilde{\psi}_n^* \right) dt} \tag{21}$$

where $\tilde{\psi}_n^*$ is the complex conjugate of $\tilde{\psi}_n$. Due to the six fold symmetry of the space-vector modulation, the per fundamental RMS harmonic flux may be calculated by:

$$\tilde{\psi}_{RMS,n} = \sqrt{\frac{3}{\pi} \int_0^{\frac{\pi}{3}} \left(\langle \tilde{\psi}_{RMS,n} \rangle_{T_s} \right)^2 d\Delta_s} \tag{22}$$

Defining the HDF as the square of the per fundamental RMS harmonic flux, Fig. 9 is obtained. From Fig. 9 it appears that for the same number of switchings ($k_f = \frac{2}{3}$), the proposed modulation scheme produces almost the same HDF as the conventional modulation.

VI. RESULTS

A. Test setup

Fig. 10 illustrates the test setup used to validate the proposed modulation scheme and Table III and Table IV lists the characteristics of the test setup.

B. Simulation results

Fig. 11a shows the effect of an unbalanced loading of the DC-link without compensating the unbalance. At time ($t = 1.1$), the resistor R_l is connected across capacitor C_1. Due to the unbalanced load between capacitor C_1 and C_2, the voltage at the center point N starts to drift towards the voltage of the positive bus-bar. The upper plot in Fig. 11a shows the phase current, the upper middle plot shows the voltage v_{aN}, the lower middle plot shows the current through the resistor R_l and the lower plot shows the voltages across capacitor C_1 and capacitor C_2.

Applying the proposed modulation technique for DC-link balancing, the voltage in the center-point N can be reestablished. Fig 11b shows the effects of an unbalanced loading, similar to the case in Fig. 11a, where the proposed balancing technique is applied. Fig. 12 shows a zoom of figure 11b. Fig. 12a shows the phase current and the phase-neutral voltage before the unbalance is introduced and it appears that the voltage is clamped symmetrical in the vicinity of the peak phase current. Fig. 12b shows the phase current and the phase-to-neutral voltage after the DC-link neutral has been restored. From Fig. 12b it appears that in order to compensate the unbalanced load of the DC-link, the modulator adjusts the clamping interval of the upper and lower switches.

VII. CONCLUSION

This paper has presented a new generalized discontinuous modulation scheme with the capability of balancing the DC-link neutral point, even if an unbalanced loading of the two DC-link capacitors for some reason occurs. Compared to conventional modulation schemes, the proposed strategy reduces the switching losses by up to 25% while maintaining the same output voltage quality. The functionality of the proposed modulation scheme is validated by simulation results.

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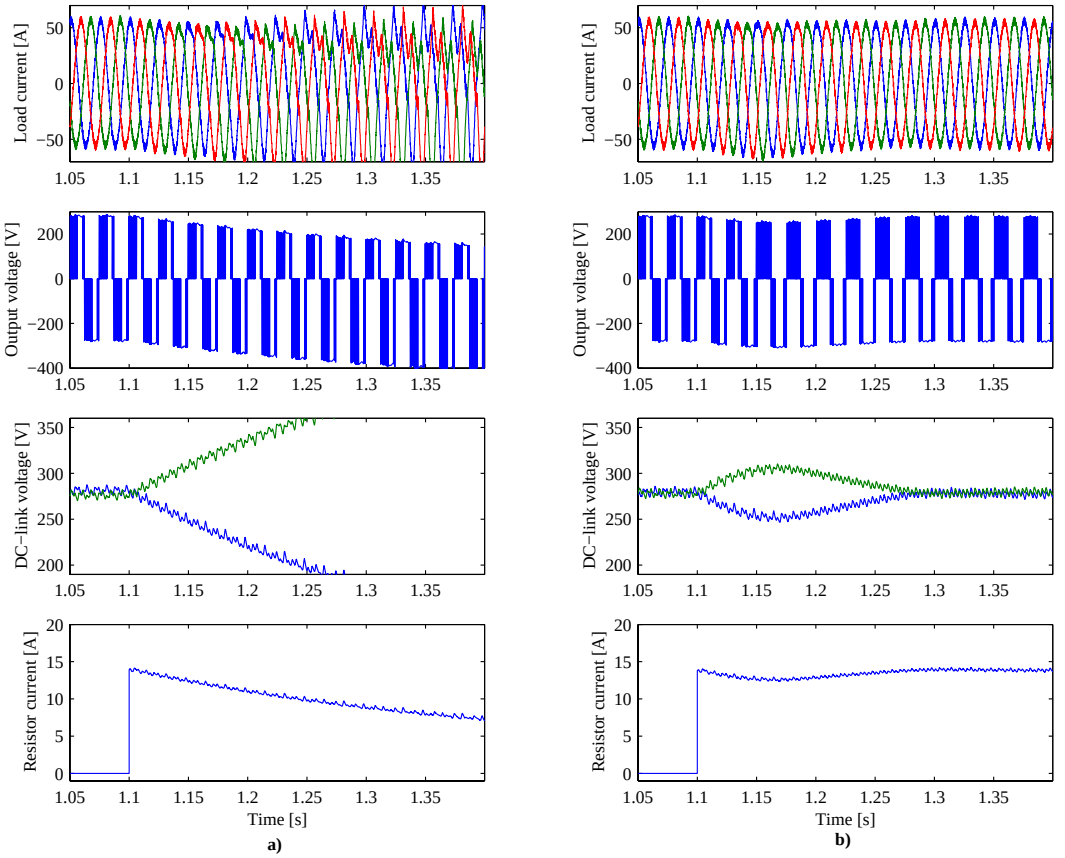

Fig. 11. Simulation results. **a)** Simulation results without DC-link compensation. **b)** Simulation results with the DC-link balancing technique applied.

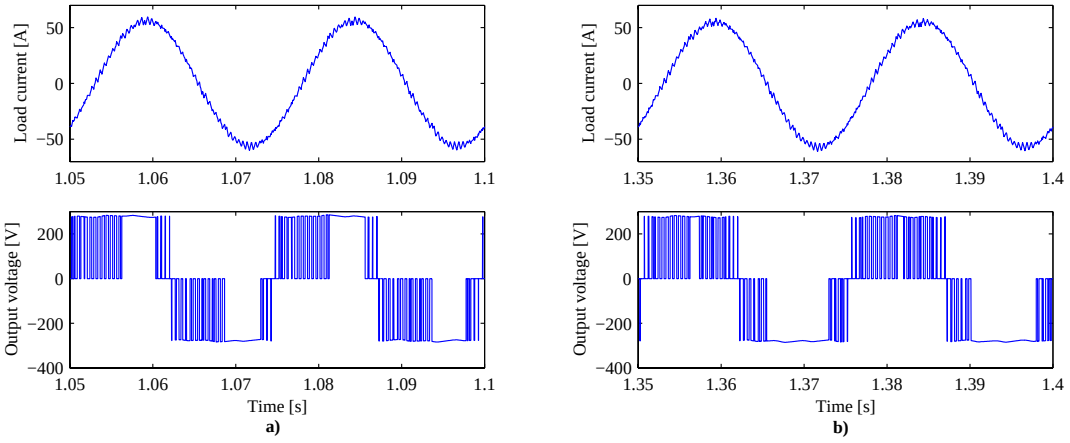

Fig. 12. Simulation results. **a)** Simulation results with DC-link compensation technique before the unbalance is introduced. **b)** Simulation results with the DC-link balancing technique after the DC-link voltage has been restored.

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Appendix G

Modulation Scheme with Common Mode-Voltage Elimination and DC-link Balancing for Three-Level Inverters, Applied for EPE 2007

Modulation Scheme with Common Mode-Voltage Elimination and DC-link Balancing for Three-Level Inverters

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Abstract— **This paper presents a novel modulation strategy for neutral point clamped inverters. The proposed strategy eliminates common-mode voltages between inverter neutral and motor neutral and at the same time, it offers full balance control of the DC-link capacitor voltages without additional hardware requirements. Compared to other modulation schemes with common-mode voltage elimination, the additional feature of DC-link voltage control requires no further reduction in the voltage transfer ratio. Although the strategy is demonstrated on a three-level neutral point clamped(NPC) inverter, the scheme can be applied to any odd-level NPC inverter. The functionality of the proposed modulation strategy is validated both by simulation results and by experimental results.**

I. Introduction

The widespread use of voltage source inverters (VSI) in electrical motor applications has introduced a number of advantages including energy savings, increased performance and the possibility to use the reliable and robust induction motor in servo drive applications. Unfortunately, along with the prevalent use of VSIs and the enhancement of semiconductor devices a couple of problems have appeared, involving electro-magnetic interference problems (EMI) and early motor failures. Besides, problems such as EMI and motor failures due to high intercoil voltages related to the fast turn-on and turn-off of the switching devices [1], the inherent generation of common-mode voltages between the inverter neutral point and the motor neutral point is a certain cause of early bearing failures. Due to electro-static couplings between motor windings and motor shaft/frame, voltage potentials may built up causing randomly appearing bearing current spikes. These bearing currents lead to bearing material erosion known as pitting and fluting and recent motor reliability studies have clarified that bearing failures account for about 40% of all motor failures [2]. Several methods have been proposed to reduce these bearing current problems [3, 4], but a common trait of these solutions are, that they increase the complexity of the hardware. For two-level inverter schemes, [5] proposed a modulation scheme where the common-mode voltage only alters six times per fundamental but this slight improvement is however obtained at the expense of a reduced voltage gain and a more distorted waveform. For three-level inverters [6, 7] proposed a similar scheme but with a complete elimination of the common-mode voltage. Unfortunately, this modulation scheme is only applicable when the DC-link voltages are build from separate DC-sources [8] or additional hardware

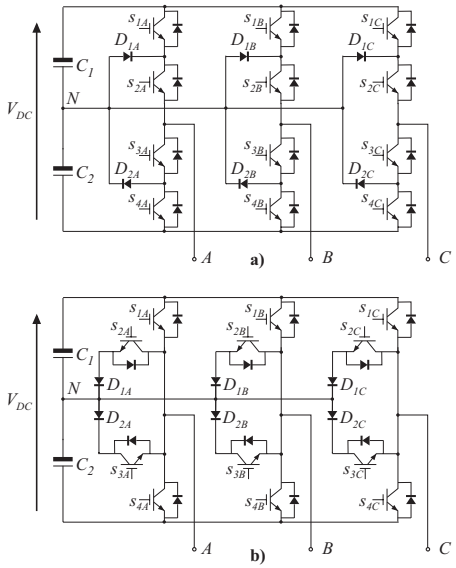

Fig. 1. Three-level NPC inverter topologies. **a)** Conventional NPC inverter. **b)** Modified NPC-inverter.

provides the DC-link balancing [9]. When series capacitors are used to divide the DC-link voltage, three-level inverters (multi-level inverters in general) have a voltage unbalance problem due to the following reasons:

- Unequal capacitor values due to manufacture tolerances.
- Unequal loading of the capacitors due to unintended switching delays.
- Unequal loading of the capacitors due to e.g. non-linear loads containing even order harmonics [10].

Several methods are proposed to solve the voltage unbalance problem, among these, [11] and [12], where the redundancy of the switch state vectors are attributed to stabilize the DC-link voltage within each switching period. Unfortunately, these methods are incapable of eliminating the common-mode voltage. This paper presents a new modulation strategy for NPC-inverters. The proposed modulation scheme is based on the space-vector approach and provides the following features:

- Common mode voltage elimination.

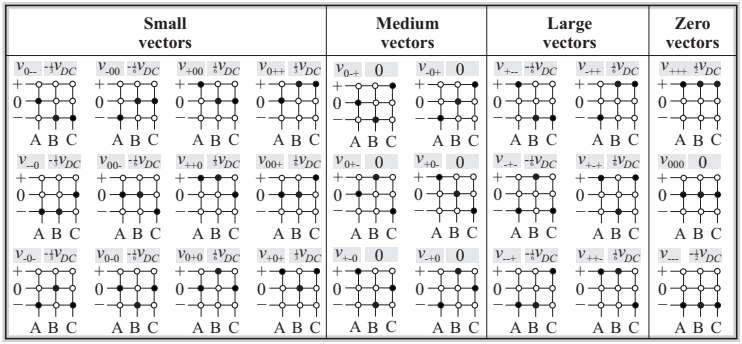

Fig. 2. Switch combinations for the three-level inverter and associated common-mode voltage generation.

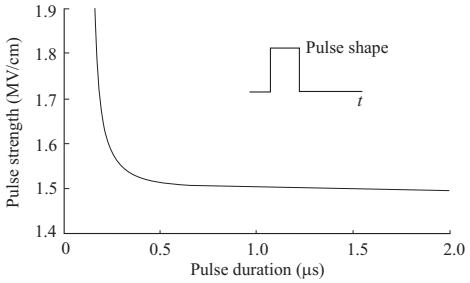

Fig. 3. The electric strength of hexane subjected to pulse voltages [19].

- DC-link voltage balancing, even with unequal loading of the DC-link capacitors or different capacitor values.
- No need for additional hardware to perform the DC-link balancing.

First the paper reviews the sources and problems related to common-mode voltages in VSI controlled motor drives and then the applicable NPC-type inverter topologies are presented. Based on the space vector analysis applied for three-level inverters, the proposed modulation scheme is derived and finally the modulation scheme is validated, by simulations and experimental results.

II. Common-mode voltage

Defining the common-mode voltage as the voltage between the motor neutral point and the converter neutral point, the common-mode voltage can be described as:

$$v_0 = \frac{1}{3}(v_{AN} + v_{BN} + v_{CN}) \tag{1}$$

In two-level inverters and multi-level converters controlled by conventional modulation schemes, this common-mode voltage never adds up to zero and hence high frequency common-mode voltages are generated within the motor windings. If there exists a common-mode path between inverter-load and ground, due to capacitive couplings, common-mode currents will be generated, resulting in e.g. bearing failures and EMI-problems.

A. Bearing failures

Motor reliability studies have indicated that motor bearing failures are the most common cause for motor failures and account for more than 30%-40% of all motor failures [4, 13]. Three electrical causes for bearing currents are reported in the literature [13, 14]:

- Primary studies on the issue indicated that bearing currents were linked to electro-magnetic induction resulting from unsymmetry in the air-gab magnetic field. Motor damages due to this phenomena occur even at sine wave operation.
- Recent studies [13, 15, 16, 17] have found that electrostatic induced shaft voltages due to common-mode voltage generation is the major source of bearing degradation.
- Improved performance in switching devices resulting in higher voltage gradients increases the current through all stray capacitances including the current through the capacitance of the bearing lubricant film. About 25% of all bearing failures are due to high voltage gradients [4].

Regarding the problems associated with common-mode voltage generated bearing currents, two different mechanisms are present, -circulating currents and non-circulating currents [18]. Circulating bearing currents are induced by oscillating circular flux around the shaft and are dominating at stand still or low low speed were the bearing lubrication does not provide an effective insulation. The non-circulating bearing currents are due to the capacitive couplings from stator winding to rotor and from rotor to ground - the latter coupling is formed by the bearing lubricant film. At each switching instant a small capacitive current through the bearings is generated, adding to the total bearing current. A more critical effect is the so-called Electro-magnetic Discharge Machining (EDM) which is a statistically occurring impulse-like current causing pitting and fluting of the bearing. The EDM occurs when the voltage across the bearing capacitance reaches the break-down voltage of the bearing lubricant film and then the lubricant capacitance is discharged. The electric strength of lubricant film depends on several factors, among these, the duration of the applied common mode voltage pulse [19]. This is shown in Fig. 3 and might be used to reduce the EDM.

B. Emission of common-mode noise

Another issue of common-mode voltage generation is the emission of common-mode noise and improper interventions of ground protection equipment. Mainly due to the parasitic capacitances between stator windings and grounded frame, the high frequency common-mode voltage will induce a common-mode current with an amplitude determined by the common-mode impedance of the stator windings and the frequency of the common-mode voltage [5]. By reducing or eliminating the generation of common-mode voltage, the electro-magnetic interference (EMI) can be reduced.

III. Neutral point clamped VSI

A. Configurations of the NPC inverter

Fig. 1a shows the conventional three-level NPC inverter proposed by [20]. In the conventional NPC inverter topology, each of the switches $s_{1A}..s_{4C}$ and the diodes $D_{1A}..D_{2C}$ only have to block half the DC-link voltage and hence, the conventional NPC is well suited for high voltage applications. A topology derived from the conventional NPC inverter is shown in Fig 1b and was proposed by [21]. Compared to the conventional NPC inverter, the salient features of this topology are: Lower conducting losses in the high modulation range, due to the fact that only one semiconductor device provides the path to the upper and lower DC-bus bar. Secondly, intelligent half bridge modules like the Skiip-pack modules from SEMIKRON are directly applicable to this configuration. Although the modified NPC inverter only switches half the DC-link voltage (if modulated properly), the upper and lower switches still need to have the ability to block the total DC-link voltage. Hence this topology is not suited in high voltage applications. The modulation scheme proposed in this paper is directly applicable for both types of inverters in Fig. 1.

B. Variation of the neutral point potential

According to Fig. 1a an excessive high voltage may be applied to the switching devices if the neutral point N varies from the center potential of the DC-link. Further, both NPC type inverters in Fig. 1 may be unable to synthesize the reference voltage if too large neutral point voltage variations occur. By inspection of Fig. 1 it appears that the NPC inverter has 27 legal switching states. These switching states are summarized in Fig. 2 and it appears that with regards to output voltage, several of these switch states are redundant (in pairs). For instance, the switch combinations v_{0--} and v_{+00} produce exactly the same output voltage (provided that the neutral point voltage is balanced) but with regards to the current flowing to/from the neutral point these two switch states behaves in the opposite manner. Hence, the selection among the redundant switch states has a vital influence on the neutral point potential and can actively be used to control/reestablish the neutral point voltage.

IV. Space vector modulation

For the purpose of space vector modulation, the output voltage references $v_A^\star$, $v_B^\star$ and $v_C^\star$ and the output currents i_A, i_B and i_C are transformed into the complex space vector plane by the following transformation:

$$\underline{V}_s^\star = \frac{2}{3}\left(v_A^\star + v_B^\star \cdot e^{j\cdot\frac{2\pi}{3}} + v_C^\star \cdot e^{j\cdot\frac{4\pi}{3}}\right) \quad (2)$$

$$\underline{I}_s = \frac{2}{3}\left(i_A + i_B \cdot e^{j\cdot\frac{2\pi}{3}} + i_C \cdot e^{j\cdot\frac{4\pi}{3}}\right) \quad (3)$$

Applying (2) on the switch combinations in Fig. 2, the well known space vector hexagon in Fig. 4 is obtained.

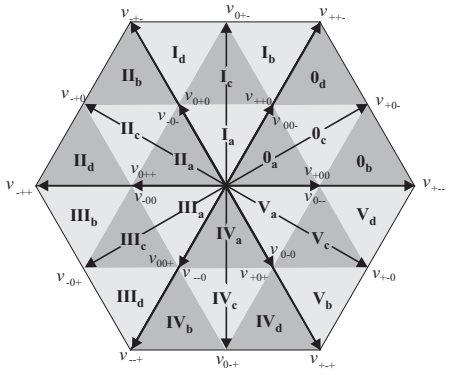

Fig. 4. The space vector hexagon for the three-level VSI.

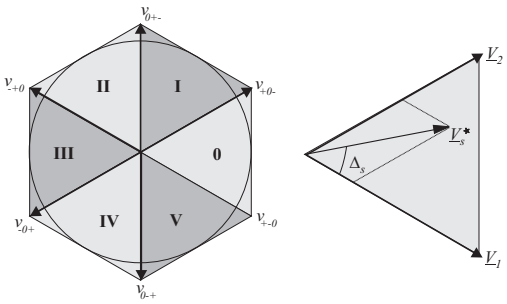

Fig. 5. **a)** Space vector hexagon for common mode voltage elimination scheme. **b)** Definition of the angle Δ_s.

A. Zero-sequence elimination

By inspection of Fig. 2 it appears that six of the active switch combinations have the property of eliminating the zero sequence voltage. In Fig. 2 these switch combinations are categorized as *medium vectors*. To eliminate the zero-sequence voltage, the modulation scheme proposed in this paper will only make use of these six active vectors and the zero vector v_{000}. Hence, the well known space-vector hexagon from Fig. 4 is reduced to the hexagon in Fig. 5a. To obtain duty cycle expressions that are independent of in which sector the voltage reference vector is located, the angle Δ_s is defined as:

$$\Delta_s = \mod(\omega_s t, \frac{\pi}{3}) \quad (4)$$

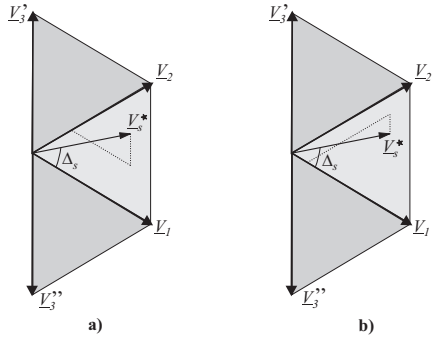

Fig. 6. Illustration of the proposed DC-balancing technique. **a)** Using voltage vector $\underline{V}_3'$. **b)** Using voltage vector $\underline{V}_3''$.

Applying conventional space vector modulation, the following duty cycle expressions can be derived:

$$\begin{aligned} \delta_1' &= \frac{2|\underline{V}_s^\star|}{V_{DC}} \cdot \sin\left(\frac{\pi}{3} - \Delta_s\right) \\ \delta_2' &= \frac{2|\underline{V}_s^\star|}{V_{DC}} \cdot \sin(\Delta_s) \\ \delta_0' &= 1 - \delta_1' - \delta_2' \end{aligned} \tag{5}$$

At all time instant the duty-cycle functions in (5) are limited by:

$$0 \leq \delta_x \leq 1 \qquad \text{where} \qquad x = [0, 1, 2] \tag{6}$$

From (5) and (6) it appears that the penalty to be paid for eliminating the zero-sequence is, that the maximum output voltage is limited to $\frac{\sqrt{3}}{2}$ the output voltage of conventional space vector modulation schemes. So far the modulation scheme is equal to the modulation scheme described by [6] and [7]. However, it is easily realized that the modulation strategy do not offer any possibility for controlling the DC-link voltage.

B. DC-link balancing considerations

If, for some reason, a DC-link voltage unbalance is introduced due to e.g. unequal capacitor sizes in the DC-link or non-linear loading containing even order harmonics, action has to be taken in order to reestablish the DC-link balance. In conventional modulation schemes for three-level inverters, DC-link balancing is achieved by adjusting the on-time ratio of redundant switch states. Since no redundant switch states are used in the present modulation scheme, this approach is not directly applicable. Instead, a kind of redundancy can be introduced by using three active vectors to form the reference vector $\underline{V}_s$. This is illustrated in Fig. 6. By use of three vectors the freedom to choose either vector $\underline{V}_3'$ or vector $\underline{V}_3''$ is obtained. By inspection of Fig. 5 it appears that the voltage vectors $\underline{V}_3'$ and $\underline{V}_3''$ for all sectors charges the DC-link capacitors in opposite manners. By this, the use of either $\underline{V}_3'$ or $\underline{V}_3''$ can be used to control the DC-link voltages.

C. Vector time intervals for proposed modulation scheme

According to Fig. 6 the reference vector $\underline{V}_s^\star$ is synthesized by:

$$\underline{V}_s^\star = \delta_1 \cdot \underline{V}_1 + \delta_2 \cdot \underline{V}_2 + \delta_3 \cdot \underline{V}_3 + \delta_0 \cdot \underline{V}_0 \tag{7}$$

where $\underline{V}_3$ can be either $\underline{V}_3'$ or $\underline{V}_3''$. Independent of the choice of vector $\underline{V}_3'$ or $\underline{V}_3''$ The on-time ratio δ_3 is calculated by :

$$\delta_3 = k \cdot (1 - \delta_1' - \delta_2') \tag{8}$$

where k is a constant proportional to the degree of unbalance. The calculations of the duty-cycles δ_1 and δ_2 depends on the choice of vector $\underline{V}_3$ If $\underline{V}_3'$ is be used to compensate DC-link unbalance, the duty-cycles δ_1 and δ_2 becomes:

$$\begin{aligned} \delta_1 &= \delta_1' + \delta_3 \\ \delta_2 &= \delta_2' - \delta_3 \end{aligned} \tag{9}$$

Complying with the restriction in (6) the limit for k becomes dependent of the modulation depth M and the angular position of the voltage reference vector. Combining (5) and (8) the limit for k when using voltage vector $\underline{V}_3'$ becomes:

$$k_{lim} = \frac{M \cdot \sin\left(\frac{\pi}{3} - \Delta_s\right)}{1 - M \cdot \left(\sin\left(\frac{\pi}{3} - \Delta_s\right) + \sin(\Delta_s)\right)} \tag{10}$$

If the unbalanced condition requires voltage vector $\underline{V}_3''$ to be used, the duty-cycles $\delta_0..\delta_2$ becomes

$$\begin{aligned} \delta_1 &= \delta_1' - \delta_3 \\ \delta_2 &= \delta_2' + \delta_3 \end{aligned} \tag{11}$$

Again, complying with the restriction in (6) the limit for k becomes:

$$k_{lim} = \frac{M \cdot \sin\left(\Delta_s\right)}{1 - M \cdot \left(\sin\left(\frac{\pi}{3} - \Delta_s\right) + \sin(\Delta_s)\right)} \tag{12}$$

The on-time ratio for the zero vector is finally calculated by:

$$\delta_0 = 1 - \delta_1 - \delta_2 - \delta_3 \tag{13}$$

By the restrictions on k formulated in (10) and (12) the voltage gain ratio of the proposed modulation scheme is not further reduced and the DC-link voltage can be balanced, even if an un-balanced loading of the DC-link capacitors occur.

V. Transient common mode voltage effects

According to Fig. 5a each change in switch state, say from v_{+0-} to v_{0+-}, involves two branch switch over (BSO). If a slight mismatch of the switchings occur due to e.g. different delays in the gate drivers, a short common-mode voltage pulse is introduced at the motor terminals. Fortunately, regarding the break down voltage of bearing lubricant oil, the fields strength increases as the pulse width decreases, c.f. Fig. 3. Alternatively, the transient common-mode voltage can be eliminated by a snubber-circuit as described in [7] or by a common-mode voltage filter as described in [3, 22], but this clearly adds to the complexity of the system.

VI. Results

A. Test setup

Fig. 7 illustrates the test setup used to validate the proposed modulation scheme. Table I and Table II lists the characteristics of the test setup.

TABLE I

TEST SETUP CONDITIONS (NPC INVERTER)

Switching frequency	f_{sw}	2.0	[kHz]
Filter inductance	L_g	400	[μH]
DC-link capacitors	C_1 C_2	10.0	[mF]
Input voltage (l-l)	V_g	400	[V]
Modulation index	M	0.8	
Input frequency	f_i	50	[Hz]
Output frequency	f_o	40	[Hz]

TABLE II

TEST SETUP CONDITIONS (INDUCTION MOTOR)

Nom. power	P_{im}	22.0	[kW]
Pole pair	N	2	
Stator resistance	R_s	0.100	[Ω]
Rotor resistance	R_r	0.086	[Ω]
Leakage inductance	L_s	1.817	[mH]
Leakage inductance	L_r	1.211	[mH]
Mag. inductance	L_m	27.936	[mH]

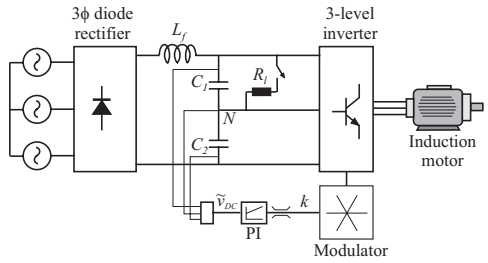

Fig. 7. The test setup used to validate the proposed modulation scheme.

B. Simulation results

Fig. 8a shows the effect of an unbalanced loading of the DC-link without compensating the unbalance. At time ($t = 1.1$), the resistor R_l is connected across capacitor C_1. Due to the unbalanced load between capacitor C_1 and C_2, the voltage at the center point N starts to drift towards the voltage of the positive bus-bar. The upper plot in Fig. 8a shows the phase current, the upper middle plot shows the voltage v_{aN}, the lower middle plot shows the current through the resistor R_l and the lower plot shows the voltages across capacitor C_1 and capacitor C_2.

Applying the proposed modulation technique for DC-link balancing, the voltage in the center-point N can be reestablished. Fig 8b shows the effects of an unbalanced loading, similar to the case in Fig. 8a, where the proposed balancing technique is applied.

C. Experimental results

VII. CONCLUSION

This paper has presented a new modulation scheme usable with three-level NPC-type inverters. The proposed modulation scheme provides elimination of the common-mode voltage between the inverter neutral point and the motor neutral point thereby reducing problems such as bearing currents and EMI. Further the proposed scheme offers the capability of balancing the DC-link neutral point, even if an unbalanced loading of the two DC-link capacitors for some reason occurs. The functionality of proposed modulation scheme is validated, both by simulation results and by experimental results.

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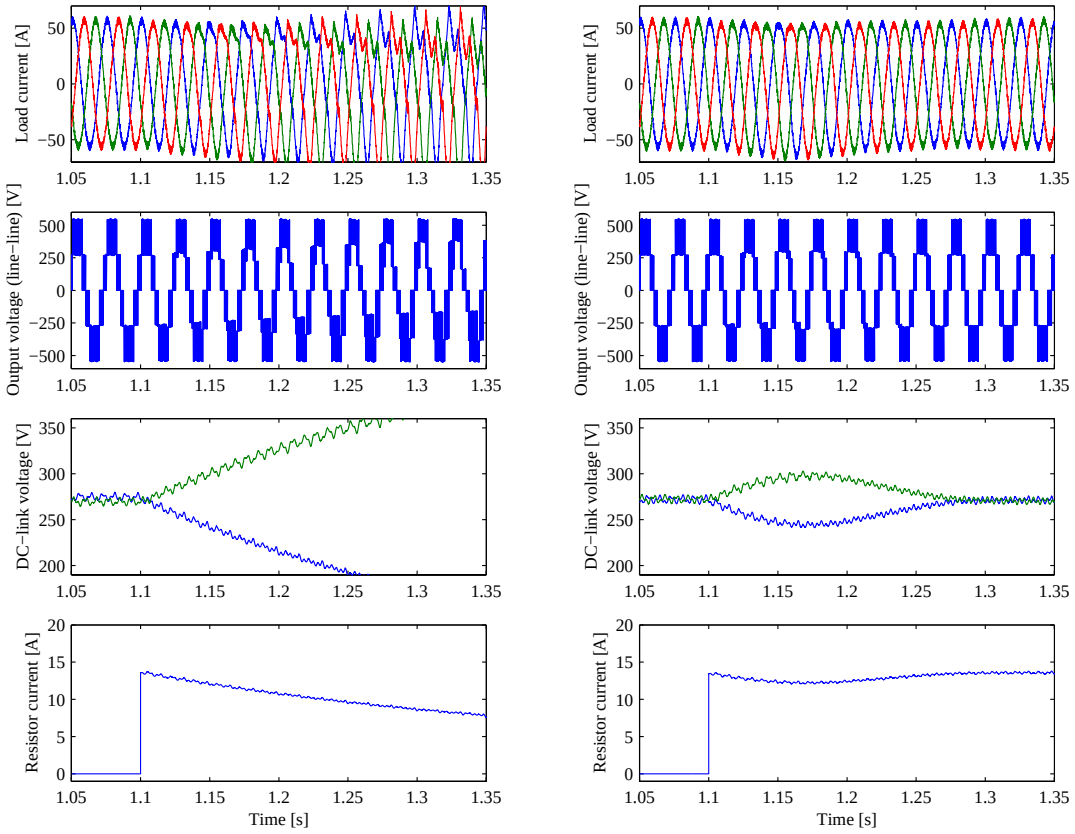

Fig. 8. Simulation results. **a)** Simulation results without DC-link compensation. **b)** Simulation results with the DC-link balancing technique applied.

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Appendix H

A Tool for Comparison of Wind Turbine Topologies, PCIM 2004

A Tool for Comparison of Wind Turbine Topologies

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Abstract— **This paper presents a tool for fast prototyping and comparison of different topologies for use in wind turbines. The models are mainly based on standard parameters but may include features such as temperature-, saturation- and skin effects in generators, temperature effects in semiconductors and the effects of applying different modulation and control strategies in the converter control. Although the tool includes several generator- and converter topologies, only the modeling of the doubly-fed induction generator and the two-level back-to-back converter are explained in detail. The effectiveness of the simulation tool is illustrated by some prototyping examples of a wind turbine including a doubly-fed induction generator and a two-level back-to-back converter. The simulated prototyping examples are to some extent validated by measurements on an existing wind turbine.**

Keywords: Wind turbine, doubly-fed induction generator, back-to-back converter, simulation.

I. Introduction

During the last decade the world wide installed wind power has increased dramatically and several forecasts expect this growth to continue [1]. Along with this growth, the average size of installed wind turbines seems to double every five years [2] and with a typical development time of a new wind turbine of about three years [3], the ever present challenges for the wind turbine engineers are quite high. Along with the developments of new components and materials, the increasing demands to the interaction between utility grid and wind turbine, formulated in different national grid codes [4-6], have a very high impact on the selection of an optimum wind turbine topology.

Because of this fast development progress and the up-coming grid requirements, the right time for introducing new topologies may very well be passed without (or with too late) notification. To be able to "hit" the market with the right topology just in time, the wind turbine engineers need to have detailed system knowledge, forecasts on upcoming requirements, acquaintance with new components and finally accurate (but also practicable) models of the involved components.

This paper presents a tool for fast comparison of wind turbine topologies. Although the tool include models of several generator topologies, and converter topologies, the presentation of the tool is limited to the doubly-fed induction generator and the two-level back-to-back converter. The effectiveness of the simulation tool is illustrated by some prototyping examples and to some extend validated by measurements.

II. System modeling

Fig. 1 shows the user interface of the comparison tool. In the left part of the user interface, the user can change the main characteristics of the considered wind turbine including change of generator- and converter topology, selection of control strategy for reactive power generation, change of parameters impacting the availability of the turbine and finally specifying models of the auxiliary power consumption.

A. Generator topologies

The tool include models of the following generator topologies:

- Doubly fed induction generator (DFIG).
- Induction generator (IG).
- Synchronous generator (SG).
- Permanent magnet synchronous generator (PMSG).
- Variable rotor resistor induction generator (VRRIG).

B. Converter topologies

The following converter topologies are modeled:

- Back-to-back two-level converter.
- Back-to-back three-level converter.
- Matrix converter.
- 2-level (passive rec on gen. side).
- 2-level (passive rec on grid side).
- None.

However, it should be noted that not all combinations of converter- and generator topologies are valid.

Depending on the overall turbine configuration, the center part of the user interface is used to specify the models and parameters of the individual components, i.e rotor, gear box, generator, converter and transformer. These models are explained in more details in the following sections.

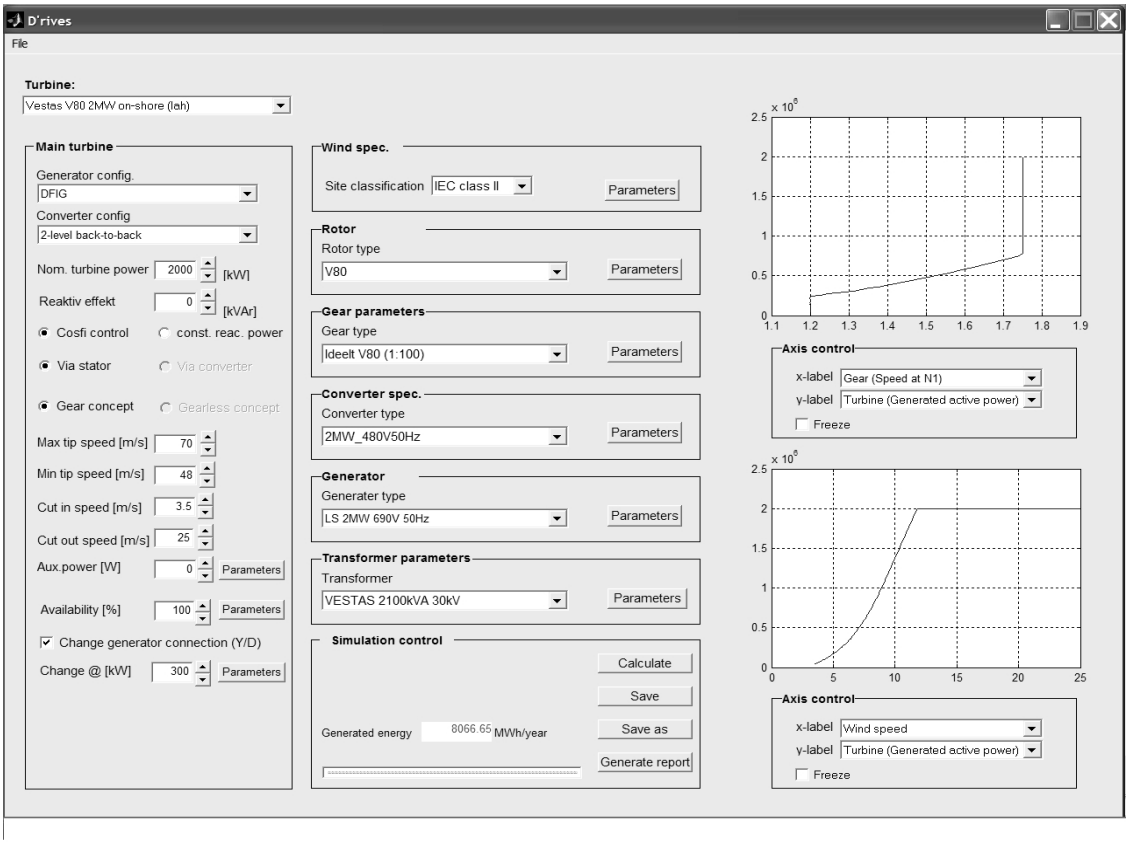

Fig. 1. User interface of the wind turbine comparison tool.

The right part of the user interface is dedicated to presentation and analysis of the simulated results. In fact, all variables can be view against each other.

III. Rotor model

The power P_{tur} transmitted to the hub shaft of a wind turbine is expressed as [7]:

$$P_{tur} = \frac{1}{2} \cdot C_p(\lambda, \theta_{pitch}) \cdot \rho_{air} \cdot A_v \cdot v_{wind}^3 \qquad (1)$$

where ρ_{air} is the air density, A_v is the area swept by the turbine rotor and v_{wind} is the wind speed (which is assumed to be constant over the swept area). C_p is the power performance coefficient describing the efficiency of the rotor blades, depending on the blade pitch angle θ_{pitch} and the ratio λ between tip speed and wind speed. Fig. 2 shows a typical C_p profile of a mega-watt wind turbine. The power performance profile is shown for different pitch angles. In partial load and while the tip speed is below the maximum allowed tip speed, the turbine runs at maximum C_p value. When the turbine reach max allowed tip speed the tip-speed ratio changes and hence the blades are pitched in order to keep the maximum available power performance coefficient. When the turbine reaches nominal load, the blades are pitched out of the wind to keep the power (measured at the grid) at the nominal value. Output from the rotor model is rotational speed ω_{g1} and and shaft torque T_{g1}. An example of generated power (i.e. T_{g1}/ω_{g1}) versus rotational speed (rad/s) is shown in the upper plot of Fig. 1.

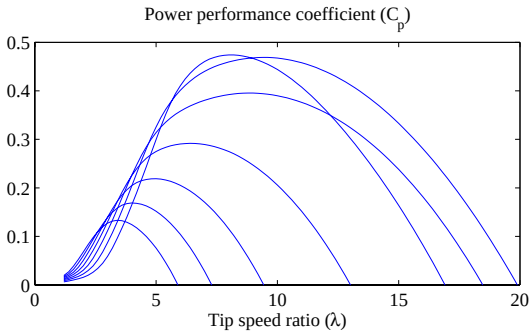

Fig. 2. Typical power performance profile of a mega-watt wind turbine.

IV. Gear model

Based on the rotational speed ω_{g1} and the shaft torque T_{g1}, the power losses $P_{loss,g}$ in the gear box is either modeled by the expression in eq. (2) or estimated through look-up tables based on measurements.

$$P_{loss,g} = k_1 \cdot \omega_{g1} + k_2 \cdot \omega_{g1}^2 + k_3 \cdot T_{g1} + k_4 \cdot T_{g1}^2 \quad (2)$$

In eq. (2), $k_1 ... k_4$ are proportional coefficients although with the possibility to implement these coefficients as linear functions of the gear oil temperature.

The torque T_{g2} applied to the generator i.e. the torque on the secondary side of the gear box is calculated by:

$$T_{g2} = \frac{T_{g1} \cdot \omega_{g1} - P_{loss,g}}{N_g \omega_{g1}} \quad (3)$$

where N_g is the gear ratio. The speed on the secondary side of the gear box is given by: $\omega_{g2} = N_g \cdot \omega_{g1}$.

A. Thermal modeling

The gear oil temperature T_{oil} is calculated by:

$$T_{oil} = \alpha_{gear} \cdot P_{loss,g} + T_{amb} \quad (4)$$

where α_{gear} is the thermal heat transfer resistance calculated from the power loss and temperature rice at nominal operation.

V. Generator model (DFIG)

A. Electrical modeling

The steady state equation for the doubly fed induction generator is given by:

$$\begin{bmatrix} \underline{V}_s \\ \underline{V}_r \end{bmatrix} = \begin{bmatrix} -R_s - j\omega_s L_s & -j\omega_s L_m \\ js\omega_s L_m & -R_r + js\omega_s L_r \end{bmatrix} \begin{bmatrix} \underline{I}_s \\ \underline{I}_r \end{bmatrix} \quad (5)$$

where s is the slip defined by: $(\omega_r - \omega_s)/\omega_s$, L_r and L_s are the rotor- and stator inductance, i.e. the sum of the main inductance and the leakage inductance.

Based on the torque T_{g2}, the speed ω_{g2}, the mechanical losses of the generator and the desired reactive power production (through the stator), eq. (5) is solved for rotor voltage $\underline{V}_r$, rotor current $\underline{I}_r$ and stator current $\underline{I}_s$.

The electrical related generator losses are modeled by:

$$P_{loss,gen} = P_{cu,s} + P_{cu,r} + P_{fe} \quad (6)$$

where $P_{cu,s}$ is the copper losses of the stator, $P_{cu,r}$ is the copper losses of the rotor and P_{fe} is the iron losses of the generator. The copper losses of the stator is given by:

$$P_{cu,s} = 3 \cdot R_s \cdot |\underline{I}_s|^2 \quad (7)$$

and the copper losses of the rotor:

$$P_{cu,r} = 3 \cdot R_r \cdot |\underline{I}_r|^2 \quad (8)$$

The core losses, i.e the sum of iron losses and hysteresis losses of the generator, is a quite complex phenomena to model. Often, the core losses are modeled by use of the Steinmetz expressions from which an equivalent variable core loss resistance R_{fe} can be derived [8]:

$$P_{fe} = 3 \cdot \frac{|\underline{V}_s + (R_s + j\omega_s L_{\sigma s}) \cdot \underline{I}_s|^2}{R_{fe}(\psi_m, \omega_s, s)} \quad (9)$$

Due to the almost constant magnetization ψ_m of the DFIG, the constant stator frequency ω_s and the limited slip s (i.e limited rotor frequency) the core loss resistance for the DFIG is assumed constant and derived from the no-load test of the generator.

A.1 Modeling of skin effects

In large machines, skin effects in the rotor windings are quite pronounced and hence the rotor resistance increases when the slip frequency increases (regarding skin effects, the slip is evaluated as an absolute value). The rotor resistance has been modeled as a linear function of the slip frequency given by:

$$R_r = R_{r|s=0} + |s| \cdot (R_{r|s=1} - R_{r|s=0}) \quad (10)$$

where $R_{r|s=0}$ is the rotor resistance at synchronous speed and $R_{r|s=1}$ is the rotor resistance measured at a blocked rotor test.

A.2 Modeling of saturation effects

In case saturation effects in the generator (i.e saturation of the main inductance) are to be included, the model in eq. (5) has to be rewritten in order to incorporate the partial differentiation of $\partial(L_m \cdot (\underline{i}_s + \underline{i}_r))/\partial t$ arising from the dynamic model description of the DFIG. The steady state description of the DFIG (including saturation effects) then becomes:

$$\begin{bmatrix} \underline{V}_s \\ \underline{V}_r \end{bmatrix} = \begin{bmatrix} -R_s - j\omega_s L_{is} & -j\omega_s L_{im} \\ j\omega_r L_m - j\omega_s L_{im} & -R_r - j\omega_s L_{ir} + j\omega_r L_r \end{bmatrix} \begin{bmatrix} \underline{I}_s \\ \underline{I}_r \end{bmatrix} \quad (11)$$

where L_{im} is the so-called dynamic inductance given by [9]:

$$L_{im} = L_m + (\underline{i}_s + \underline{i}_r) \frac{dL_m}{d(\underline{i}_s + \underline{i}_r)} \quad (12)$$

and L_{is} and L_{ir} are the stator- and rotor dynamic inductances, i.e. the sum of the dynamic inductance and the leakage inductance. Fig. 3 shows the modeling of the main inductance L_m and the dynamic inductance L_{im}. In case saturation effects are neglected, i.e. $L_{im} = L_m$ it appears that eq. (11) reduces to the expression in eq. (5).

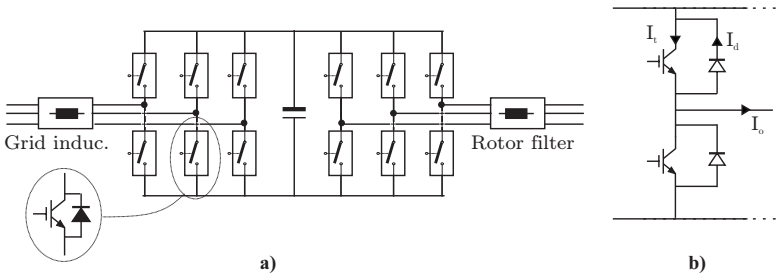

Fig. 4. Converter illustration. **a)** Two-level back-to-back converter. **b)** Single branch in the two-level back-to-back converter.

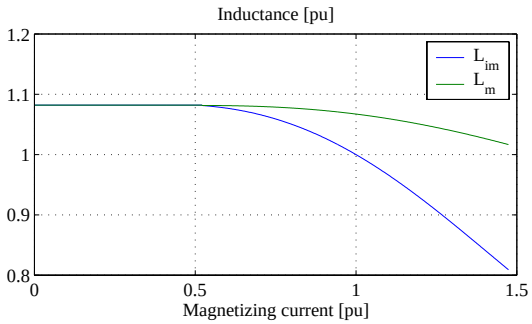

Fig. 3. Illustration of the magnetizing inductance L_m and the dynamic inductance L_{im}.

A.3 Modeling of thermal effects

The steady state temperature T_s of the stator and T_r of the rotor is calculated as:

$$T_s = \alpha_s \cdot P_{s,loss} + T_{amb} \quad (13)$$

$$T_r = \alpha_r \cdot P_{r,loss} + T_{amb} \quad (14)$$

where the thermal resistance α_s and α_r of the stator and rotor respectively are calculated from the temperature rice at nominal load. Based on the calculated temperatures, the resistances of the stator- and rotor winding in the present working point is calculated as:

$$R_s = R_{s0} + \alpha_{cu} \cdot (T_s - T_0) \quad (15)$$

$$R_r = R_{r0} + \alpha_{cu} \cdot (T_r - T_0) \quad (16)$$

The resistances R_{s0} and R_{r0} are the stator- and rotor resistance measured at temperature T_0. The coefficient α_{cu} is the temperature coefficient of resistivity of the considered material.

B. Mechanical modeling

The mechanical losses of the DFIG can either be modeled by eq. (17) or by use of look up tables obtained from measurements.

$$P_{rotloss,gen} = T_c \cdot \omega_{g2} + k_\omega \omega_{g2}^2 + k_{\omega\omega} \cdot \omega_{g2}^3 \quad (17)$$

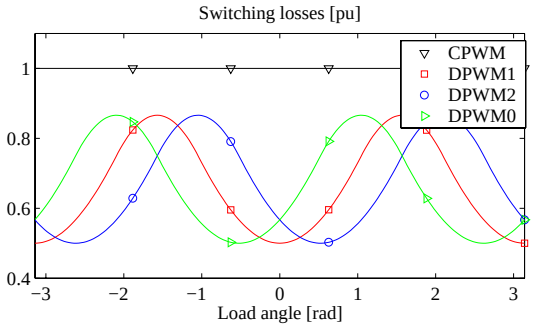

Fig. 5. Normalized switching losses for different modulation methods.

where T_c is the coloumb friction of the generator, k_ω is the viscous friction coefficient and $k_{\omega\omega}$ is the ventilation friction coefficient. The thermal effects on the mechanical parts of the generator are calculated similar to the temperature effects in the gear box, cf. eq. (4).

VI. Converter model (B2B)

Fig. 4a shows the two-level back-to-back converter.

A. Electrical modeling

Based on the rotor voltage $\underline{V}_r$, the rotor current $\underline{I}_r$, the grid voltage $\underline{V}_{g3}$ and the converter losses, the converter grid current $\underline{I}_{g3}$ can be calculated:

$$\underline{I}_{g3} = \frac{\Re e(\underline{V}_r \cdot \underline{I}_r) - P_{loss,con}}{\underline{V}_{g3}} - j\frac{Q_{con}}{\underline{V}_{g3}} \quad (18)$$

where Q_{con} is the reactive power reference for the grid inverter and $P_{loss,con}$ is the converter losses, including losses in the rotor filter and grid filter, c.f. Fig. 4. Although the converter losses are made of several loss components, only the modeling of the semiconductor losses are described in detail.

A.1 Conducting losses

The conducting losses P_{cond} of an electronic switch (Diode or IGBT) is modeled by [10]:

$$P_{cond} = U_{on} \cdot I_{avg} + R_{on} \cdot I_{RMS}^2 \quad (19)$$

where I_{avg} is the average current in the considered component and I_{RMS} is the RMS current in the considered component. Unfortunately there is no simple analytical relationship between the output current I_o and the current in the diode I_d and IGBT I_t, c.f. Fig. 4b. In fact, the current distributon between diode and IGBT is a function of both power factor ($\cos(\phi)$) and modulation index M. In [11] the average current through the diode and IGBT is approximated by:

$$I_{t,avg} \approx (0.2251 + 0.1768 \cdot K) \cdot I_o \quad (20)$$

$$I_{d,avg} \approx (0.2251 - 0.1768 \cdot K) \cdot I_o \quad (21)$$

and the RMS current by:

$$I_{t,RMS} \approx (0.5 + 0.1824 \cdot K) \cdot I_o \quad (22)$$

$$I_{d,RMS} \approx \sqrt{0.25 - 0.1824 \cdot K - 0.0333K^2} \cdot I_o \quad (23)$$

where the factor K is defined by:

$$K \triangleq M \cdot |\cos(\phi)| \quad (24)$$

The expressions in eq. (20)-(23) are valid when the power flow is out of the considered inverter. In case the power flows into the considered inverter the equations for the diode current quantities and IGBT current quantities are to be interchanged.

A.2 Switching losses

The switching losses of a PWM VSI depend on the chosen modulation strategy [12]. Assuming the inverter switching devices to have linear current turn-on and turn-off characteristics with respect to time and accounting only for the fundamental component of the load current, the switching losses can be analytically modeled for any given modulation strategy. The device switching losses per fundamental can be calculated as follows:

$$P_{sw} = \frac{1}{2\pi} \frac{V_{DC}(t_{on} + t_{off})}{2 \cdot T_s} \int_0^{2\pi} f(\theta) d\theta \quad (25)$$

where t_{on} and t_{off} represents the turn-on and turn-off times of the switching devices, V_{DC} is the DC-link voltage and $f(\theta)$ is the switching current function. The switching current function equals zero in the intervals where modulation ceases (in case of discontinuous modulation) and the absolute value of the corresponding phase current value elsewhere. Fig. 5 shows the normalized switching losses of different modulation methods implemented for the B2B converter.

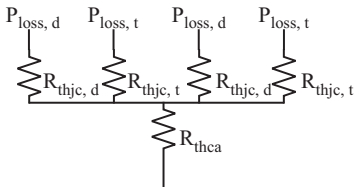

Fig. 6. Illustration of the simple thermal model used to estimate switch temperatures.

B. Thermal modeling

The thermal modeling of the switches is (so far) modeled as a steady state model, only representing the average switch temperature, i.e. the average temperature of a fundamental period. The modeling approach is illustrated on Fig. 6.

VII. Transformer model

The steady state equation for the transformer is given by:

$$\begin{bmatrix} \underline{V}_{g1} \\ \underline{V}_s \\ \underline{V}_{g3} \end{bmatrix} = \begin{bmatrix} -R_{g1} - jX_{g1} & jX_h & jX_h \\ -jX_h & R_{g2} + X_{g2} & jX_h \\ -jX_h & jX_h & R_{g3} + X_{g3} \end{bmatrix} \begin{bmatrix} \underline{I}_{g1} \\ \underline{I}_s \\ \underline{I}_{g3} \end{bmatrix} \quad (26)$$

where X_h is the main mutual reactance, $X_{g1..3}$ is the self reactance of the considered winding and $R_{1..3}$ is the resistance of the considered winding. The parameters used for the transformer modeling are all derived from standard measurements, i.e. short circuit and no load tests.

VIII. Simulation algorithm

From the modeling approach described in the previous sections a simulation algorithm has been established. Fig. 7 illustrates the simulation algorithm. From Fig. 7 it appears that as long as the variables, i.e. voltages , currents temperatures etc. have not reached a steady-state value (for all wind speeds), defined by a specified simulation tolerance, the algorithm is repeated. As the simulation tool is intended for use in design and prototyping of wind turbines, the simulation algorithm returns a warning list if one ore more component(s) are loaded beyond its rated value.

IX. Results (Examples)

One application for the developed simulation tool could be the initial design of a converter in a new wind turbine. A parameter of interest could be the converter losses. Fig. 8 shows the simulated converter losses along with measured losses (shown by ◇ □). The measurements were performed on a full size converter test bench [13].

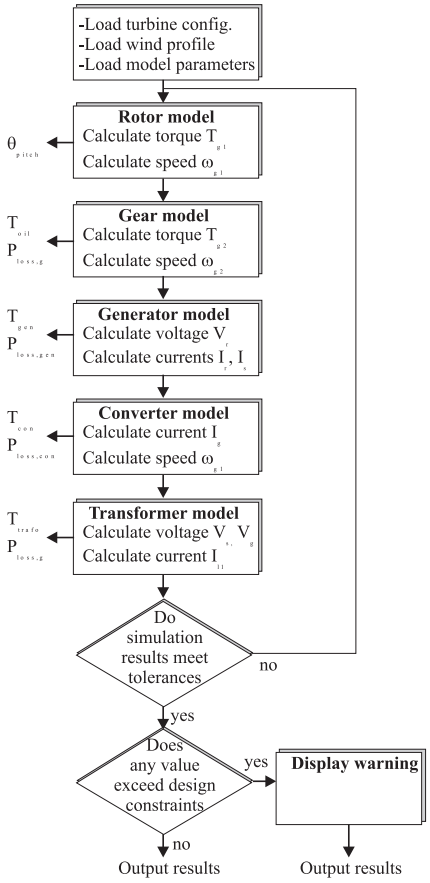

Fig. 7. Illustration of the algorithm for the simulation tool.

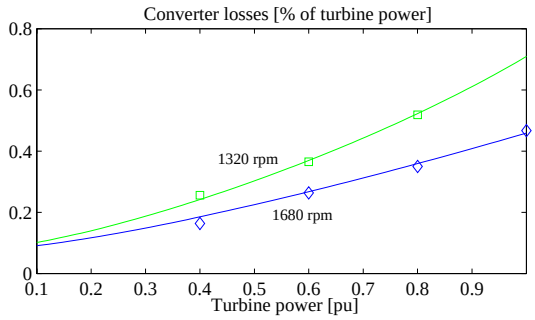

Fig. 8. Switch temperature in the back-to-back converter.

Based on the quite accurate estimated converter losses (which of course can be viewed for the individual inverters and components), the temperatures of the switching components can be calculated. Fig. 9 shows the temperature of the switching components of a back-to-back converter as a function of the normalized turbine power (The turbine follows the power-speed characteristics in the upper plot og Fig. 1). The temperatures indicated by (◇ □ ○) are calculated by a program provided by

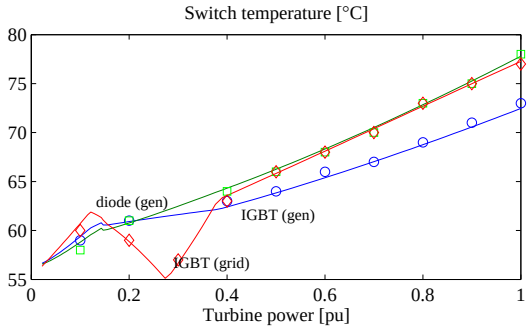

Fig. 9. Switch temperature in the back-to-back converter.

the the semiconductor manufacturer and are used as validation of the developed simulation tool.

X. Conclusion

This paper has presented a tool for fast prototyping and comparison of wind turbine topologies. The models are primarily based on standard parameters but may also include more advanced modeling approaches such as saturation , skin and temperature effects. Further, the consequences on energy production and loss distribution in the turbine by applying different modulation and control strategies are easily investigated.

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Appendix I

Analysis of Symmetrical Pulse Width Modulation Strategies for Matrix Converters, PESC 2002

Analysis of Symmetrical Pulse Width Modulation Strategies for Matrix Converters

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***Abstract* — This paper presents a new and easy way to understand the derivation of the modulation functions for matrix converters. It is shown how the duty cycles can be calculated using techniques known from the back-to-back (B2B) voltage source inverter (VSI), thus making the subject accessible to people with prior knowledge in standard drives. A new modulation strategy is presented minimizing harmonic distortion compared to the standard double-sided space vector modulation for matrix converters. An improvement to an existing modulator is also presented where the proposed modification improves the harmonic performance. The strategies are compared both analytically and by the use of both simulations and measurements on a 12 kW matrix converter prototype.**

It is found that the proposed modulator has superior performance compared to modulators with equal switching frequencies and an equal number of switchings.

***Keywords* — Matrix converter, indirect space vector modulation, PWM, harmonic distortion.**

I. Introduction

The matrix converter is known to only a limited group of electrical engineers. The high level of complexity in the matrix converter prevents a wider audience in working with the promising technology of matrix converters. However, the standard VSI is to many people a well-known technology and likewise is the space vector modulator for the VSI converter. By the use of indirect modulation which was first presented by [1] in 1989 the function of the matrix converter can be described as a rectifier and an inverter working together. This relation can be illustrated graphically by inspecting the matrix converter, which is shown in the following section.

The matrix converter is built of 9 bi-directional switches connected in a matrix as seen on Fig. 1. The switches can connect one input phase to one output phase thus impressing input phase voltages on the load. An input filter is mounted between the converter and the voltage grid to filter high frequency currents and decouple the grid impedance.

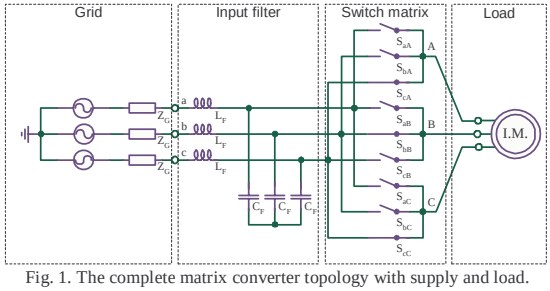

Fig. 1. The complete matrix converter topology with supply and load.

Hardware issues and practical implementation has been described and since its introduction in 1980 different strategies to minimize the number of components have been proposed, among others a way to reduce the number of components for protecting the converter [2] and a method to limit the number of floating supplies [3].

Double-sided modulation provides a good performance and the controller is known from the classical VSI, thus double-sided modulation is analysed in the paper. The derivation starts by considering the matrix converter as two separate converters.

II. Matrix Converter Modulation using B2B-VSI Theory

The controller presented by [1] as well as the most common modulator for the VSI is the space vector modulator. On Fig. 2 it is seen how the matrix converter can be redrawn as a rectifier and an inverter; the modulation function can then be derived for both the rectifier and the inverter.

The input and output voltages and currents are expressed as space vectors using the transforms shown in (1) to (4).

$$\vec{V}_{in} = \frac{2}{3}\left(v_a + v_b \cdot e^{j\frac{2\pi}{3}} + v_c \cdot e^{j\frac{4\pi}{3}} \right) \tag{1}$$

$$\vec{I}_{in} = \frac{2}{3}\left(i_a + i_b \cdot e^{j\frac{2\pi}{3}} + i_c \cdot e^{j\frac{4\pi}{3}} \right) \tag{2}$$

$$\vec{I}_{out} = \frac{2}{3}\left(i_A + i_B \cdot e^{j\frac{2\pi}{3}} + i_C \cdot e^{j\frac{4\pi}{3}} \right) \tag{3}$$

$$\vec{V}_{out} = \frac{2}{3}\left(v_{AB} + v_{BC} \cdot e^{j\frac{2\pi}{3}} + v_{CA} \cdot e^{j\frac{4\pi}{3}} \right) \tag{4}$$

The task of the modulator is to synthesise the output voltages from the input voltages, and the input currents from the output currents.

A. Space Vector Modulator for the Rectifier Side

From Fig. 2 it is seen that a virtual DC-link is established. In the indirect space vector modulator all quantities are referred to this virtual DC-link. The input currents and DC-link voltage can be found from the switch states as seen in (5) and (6).

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} S_1 & S_2 \\ S_3 & S_4 \\ S_5 & S_6 \end{bmatrix} \cdot \begin{bmatrix} i_{DC+} \\ i_{DC-} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} v_{DC+} \\ v_{DC-} \end{bmatrix} = \begin{bmatrix} S_1 & S_3 & S_5 \\ S_2 & S_4 & S_6 \end{bmatrix} \cdot \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{6}$$

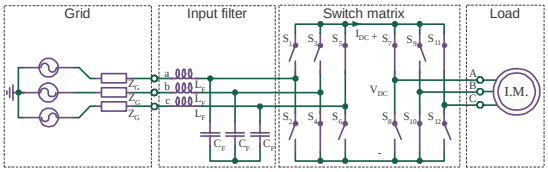

Fig. 2. The matrix converter illustrated using the indirect space vector method.

The possible switch combinations of the rectifier are seen in Table I and the space vector hexagon is seen on Fig. 3. For one such set of vectors the span is shown on Fig. 4 where also the vector lengths are shown. The duty cycles for the adjacent vectors on Fig. 4 can be calculated using (7).

$$\begin{aligned} d_\alpha &= m_{rec} \cdot \sin\left(\frac{\pi}{3} - \Delta_{rec}\right) \\ d_\beta &= m_{rec} \cdot \sin\left(\Delta_{rec}\right) \\ d_0 &= 1 - d_\alpha - d_\beta \\ m_{rec} &= \frac{\hat{i}_{in}}{i_{DC}} \end{aligned} \tag{7}$$

The modulation index m_{rec} is often chosen to be 1, as no amplitude control of the current is desired. The calculated duty cycles can then be multiplied with the switch matrix to calculate the mean value of the input currents and the DC-link voltage as shown in (8) and (9). The switch states S_x are replaced by the vectors shown on Fig. 4 for an angle between –30° and +30°.

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \left(d_\alpha \cdot \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \end{bmatrix} + d_\beta \cdot \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix} \right) \cdot \begin{bmatrix} I_{DC+} \\ I_{DC-} \end{bmatrix} \tag{8}$$

$$\begin{bmatrix} V_{DC+} \\ V_{DC-} \end{bmatrix} = \left(d_\alpha \cdot \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} + d_\beta \cdot \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \right) \cdot \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{9}$$

From the DC-link voltage the output voltages can be calculated and the modulation function for the inverter can be derived.

TABLE I. Switch states and generated vectors for the rectifier.

Type	$\begin{bmatrix} S_1 & S_3 & S_5 \\ S_2 & S_4 & S_6 \end{bmatrix}^T$	i_a	i_b	i_c	$\lvert\vec{I}_{in}\rvert$	$\angle\vec{I}_{in}$	v_{DC}
Active	$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}^T$	0	i_{DC+}	i_{DC-}	$\frac{2}{\sqrt{3}} i_{DC}$	$\frac{\pi}{2}$	v_{bc}
	$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}^T$	0	i_{DC-}	i_{DC+}	$\frac{2}{\sqrt{3}} i_{DC}$	$-\frac{\pi}{2}$	$-v_{bc}$
	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}^T$	i_{DC-}	i_{DC+}	0	$\frac{2}{\sqrt{3}} i_{DC}$	$\frac{5\pi}{6}$	$-v_{ab}$
	$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}^T$	i_{DC-}	0	i_{DC+}	$\frac{2}{\sqrt{3}} i_{DC}$	$-\frac{5\pi}{6}$	v_{ca}
	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}^T$	i_{DC+}	0	i_{DC-}	$\frac{2}{\sqrt{3}} i_{DC}$	$\frac{\pi}{6}$	$-v_{ca}$
	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}^T$	i_{DC+}	i_{DC-}	0	$\frac{2}{\sqrt{3}} i_{DC}$	$-\frac{\pi}{6}$	v_{ab}
Zero	$\begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}^T \begin{bmatrix} 0 & 1 & 0 \\ 0 & 1 & 0 \end{bmatrix}^T \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix}^T$				0		0

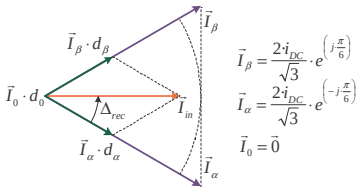

Fig. 4. Vector span for the rectifier current.

B. Space Vector Modulation for the Inverter Side

The output voltages can be found as the virtual DC-link voltage multiplied by the switch state of the inverter, and at the same time the DC-link current can be found by using the transposed matrix as seen in (10) and (11).

$$\begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} = \begin{bmatrix} S_7 & S_8 \\ S_9 & S_{10} \\ S_{11} & S_{12} \end{bmatrix} \cdot \begin{bmatrix} v_{DC+} \\ v_{DC-} \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} i_{DC+} \\ i_{DC-} \end{bmatrix} = \begin{bmatrix} S_7 & S_9 & S_{11} \\ S_8 & S_{10} & S_{12} \end{bmatrix} \cdot \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{11}$$

Fig. 5 shows the vectors that the output inverter can form by applying the DC-link voltage to the output terminals. Table II shows the possible switch states and the resulting length and direction of the vectors. Looking at one sector, the span of the vector and the output voltage relationship shown on Fig. 6 can be found.

By geometric considerations the duty cycles can be calculated as shown in (12). By projecting the V_{out} vector onto the V_λ and V_γ vectors.

$$\begin{aligned} d_\gamma &= \frac{\hat{V}_{out}}{v_{DC}} \cdot \sin\left(\frac{\pi}{3} - \Delta_{inv}\right) \\ d_\lambda &= \frac{\hat{V}_{out}}{v_{DC}} \cdot \sin\left(\Delta_{inv}\right) \\ d_0 &= 1 - d_\gamma - d_\lambda \end{aligned} \tag{12}$$

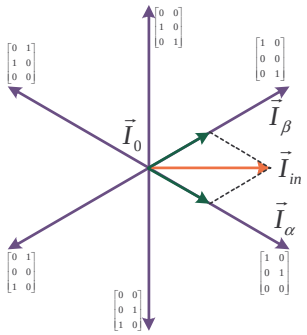

Fig. 3. Input current hexagon.

TABLE II. Switch states and generated vectors for the inverter.

Type	$\begin{bmatrix} S_7 & S_9 & S_{11} \\ S_8 & S_{10} & S_{12} \end{bmatrix}^T$	v_A v_{AB}	v_B v_{BC}	v_C v_{CA}	$\lvert\vec{V}_{out}\rvert$	$\angle\vec{V}_{out}$	i_{DC+}
Active	$\begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}^T$	$1/3v_{DC}$ 0	$1/3v_{DC}$ v_{DC}	$-2/3v_{DC}$ $-v_{DC}$	$\frac{2}{\sqrt{3}}v_{DC}$	$\frac{\pi}{2}$	$-i_C$
	$\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}^T$	$1/3v_{DC}$ v_{DC}	$-2/3v_{DC}$ $-V_{DC}$	$1/3v_{DC}$ 0	$\frac{2}{\sqrt{3}}v_{DC}$	$-\frac{\pi}{6}$	$-i_B$
	$\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \end{bmatrix}^T$	$-2/3v_{DC}$ $-v_{DC}$	$1/3v_{DC}$ 0	$1/3v_{DC}$ v_{DC}	$\frac{2}{\sqrt{3}}v_{DC}$	$-\frac{5\pi}{6}$	$-i_A$
	$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 1 \end{bmatrix}^T$	$2/3v_{DC}$ v_{DC}	$-1/3v_{DC}$ 0	$-1/3v_{DC}$ $-v_{DC}$	$\frac{2}{\sqrt{3}}v_{DC}$	$\frac{\pi}{6}$	i_A
	$\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix}^T$	$-1/3v_{DC}$ $-v_{DC}$	$2/3v_{DC}$ v_{DC}	$-1/3v_{DC}$ 0	$\frac{2}{\sqrt{3}}v_{DC}$	$\frac{5\pi}{6}$	i_B
	$\begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}^T$	$-1/3v_{DC}$ 0	$-1/3v_{DC}$ $-v_{DC}$	$2/3v_{DC}$ v_{DC}	$\frac{2}{\sqrt{3}}v_{DC}$	$-\frac{\pi}{2}$	i_C
Zero	$\begin{bmatrix} 0 & 0 & 0 \\ 1 & 1 & 1 \end{bmatrix}^T \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 0 \end{bmatrix}^T$				0		0

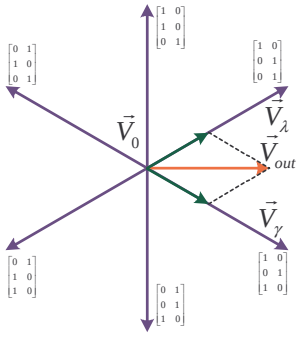

Fig. 5. Output voltage hexagon.

From the duty cycles the mean value of the output voltages and the DC-link current can be written as shown in (13) and (14).

$$\begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} = \left(d_\gamma \cdot \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} + d_\lambda \cdot \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{bmatrix} \right) \cdot \begin{bmatrix} V_{DC+} \\ V_{DC-} \end{bmatrix} \tag{13}$$

$$\begin{bmatrix} I_{DC+} \\ I_{DC-} \end{bmatrix} = \left(d_\gamma \cdot \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} + d_\lambda \cdot \begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \right) \cdot \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \tag{14}$$

Now when the modulation functions for both the rectifier and the inverter have been expressed, the combined modulation function can be formed.

C. Relationship Between the MC and B2B-VSI

The matrix converter is not, however, built as a rectifier and an inverter and therefore the modulation functions should be transformed into one modulation function for 9 bi-directional switches. If the converter is seen from an output phase; two phase-switches of the output leg and six rectifier switches are seen, such equivalent can be made for each phase. Fig. 7 shows how the VSI topology can be considered and transformed into one phase in the matrix converter. From Fig. 7 it can be seen that the switches in the matrix converter branch must be controlled with a function that is a multiple of the rectifier and inverter functions.

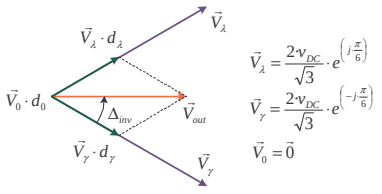

Fig. 6. Vector span for the inverter voltage.

Equations (15) and (16) show the multiplication between the rectifier and inverter switch functions.

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} S_7 & S_8 \\ S_9 & S_{10} \\ S_{11} & S_{12} \end{bmatrix} \cdot \begin{bmatrix} S_1 & S_3 & S_5 \\ S_2 & S_4 & S_6 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{15}$$

$$\begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} S_7 \cdot S_1 + S_8 \cdot S_2 & S_7 \cdot S_3 + S_8 \cdot S_4 & S_7 \cdot S_5 + S_8 \cdot S_6 \\ S_9 \cdot S_1 + S_{10} \cdot S_2 & S_9 \cdot S_3 + S_{10} \cdot S_4 & S_9 \cdot S_5 + S_{10} \cdot S_6 \\ S_{11} \cdot S_1 + S_{12} \cdot S_2 & S_{11} \cdot S_3 + S_{12} \cdot S_4 & S_{11} \cdot S_5 + S_{12} \cdot S_6 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{16}$$

By multiplying the mean value functions it can be seen how the output voltages can be formed by the input voltages and a combination of the switch matrix.

D. Indirect Space Vector Modulation for the MC

Now that the mean values have been expressed the combined indirect modulation function can be written. Equations (17) and (18) show an example of how the function for the inverter and rectifier is multiplied to give the switch states for the 9 bi-directional switches.

$$\begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} = \left(d_\gamma \cdot \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} + d_\lambda \cdot \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 1 \end{bmatrix} \right) \cdot \left(d_\alpha \cdot \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} + d_\beta \cdot \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \right) \cdot \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{17}$$

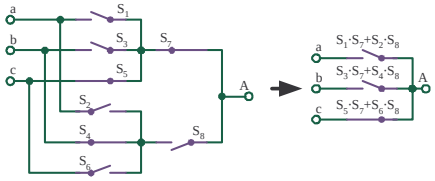

Fig. 7. One-phase VSI to one-phase matrix converter.

$$\begin{bmatrix} V_{An} \\ V_{Bn} \\ V_{Cn} \end{bmatrix} = \left(\begin{matrix} d_\gamma \cdot d_\alpha \cdot \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} + d_\lambda \cdot d_\alpha \cdot \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} + \\ d_\gamma \cdot d_\beta \cdot \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} + d_\lambda \cdot d_\beta \cdot \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \end{matrix} \right) \cdot \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad (18)$$

For the remaining time of a switch period a zero vector is applied, circulating output currents and disconnecting input voltages.

The equation for the duty cycles can now be written as shown in (19).

$$\begin{aligned} d_\gamma \cdot d_\alpha &= \frac{|\vec{V}_{out}|}{v_{DC}} \cdot \sin\left(\frac{\pi}{3} - \Delta_{inv}\right) \cdot \sin\left(\frac{\pi}{3} - \Delta_{rec}\right) \\ d_\lambda \cdot d_\alpha &= \frac{|\vec{V}_{out}|}{v_{DC}} \cdot \sin(\Delta_{inv}) \cdot \sin\left(\frac{\pi}{3} - \Delta_{rec}\right) \\ d_\gamma \cdot d_\beta &= \frac{|\vec{V}_{out}|}{v_{DC}} \cdot \sin\left(\frac{\pi}{3} - \Delta_{inv}\right) \cdot \sin(\Delta_{rec}) \\ d_\lambda \cdot d_\beta &= \frac{|\vec{V}_{out}|}{v_{DC}} \cdot \sin(\Delta_{inv}) \cdot \sin(\Delta_{rec}) \\ d_0 &= 1 - d_\gamma \cdot d_\alpha - d_\lambda \cdot d_\alpha - d_\gamma \cdot d_\beta - d_\lambda \cdot d_\beta \end{aligned} \quad (19)$$

III. Pulse Width Modulation Methods Based on Double-Sided Space Vector Modulation

The modulation functions in (19) state that four active and one zero vector is needed for the space vector modulator in each switching period. The distribution of the vectors is however free and this degree of freedom can be used to improve the harmonic distortion or limit the number of switchings. Four different methods of realizing the modulation function will now be presented.

A. 8-switch method

In 1996 [5] proposed a double-sided modulation strategy, which uses the four active vectors placed around one zero vector. The strategy gives 8 Branch Switch Overs (BSO) per switching period, and was thus an improvement of the 9-switch modulator presented in 1992 by [6]. Fig. 8 shows the strategy, where each colour represents an active vector and the white area is the zero vector.

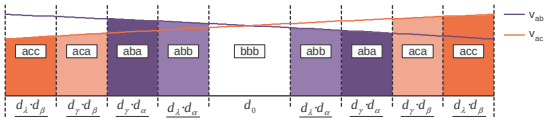

Fig. 8. The 8-switch double-sided modulator.

B. 10-switch method

The 10-switch method was presented in 2000 by [7]. The method seeks to minimize the distortion by introducing another zero-vector in the end of the sequence, resulting in 2 extra BSO. The advantage is that the apparent switching frequency is doubled as it is seen on Fig. 20. The switch frequency is reduced by 4/5 to give equal number of switchings pr. second.

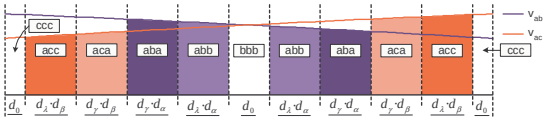

Fig. 9. The 10-switch double-sided modulator.

C. Low-distortion method

The low distortion method is a new method of reducing the harmonic distortion by having two zero vectors per period, but implementing it in a way to have 8 BSO per period. The procedure of splitting the zero vector is illustrated on Fig. 10.

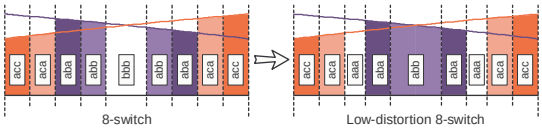

Fig. 10. Splitting the zero vector to minimize distortion.

The result of the splitting is shown on Fig 11. It can be seen that the dark red and the light blue vector are not split by the zero vector and they will thus produce harmonics around the switching frequency while the light red and dark blue will produce harmonics around the double of the switching frequency.

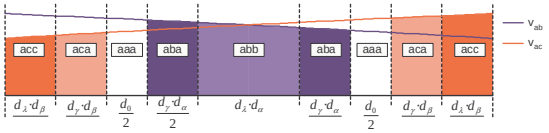

Fig. 11. Low distortion modulator.

D. Low-loss method

In 2001 [8] presented a modulator to reduce switching losses by using vectors with lower amplitude. The previous strategies all used vectors spaced by 60°, while this strategy uses vectors spaced by 120°.

The effect is shown on Fig. 12, which is a lower amplitude of the vectors and thus the output voltages are limited to half of the input voltage. The vectors are placed with the split zero vector as seen on Fig. 13.

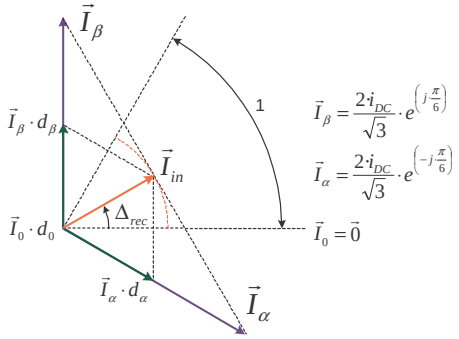

Fig. 12. Vector span by the low loss modulator.

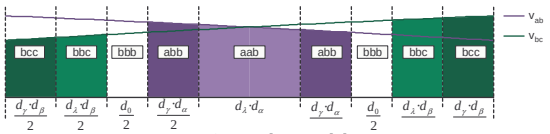

Fig. 13. Low-loss modulator.

E. Modified low loss method

The low loss modulator, however, produces low harmonics when the vector moves from one sector to the next. The low harmonics can be seen on Fig. 22. The vector suddenly jumps from the side of the period to the center resulting in low order harmonics. The occurrence is shown on Fig. 14, which shows two switch periods where the vector enters a new sector.

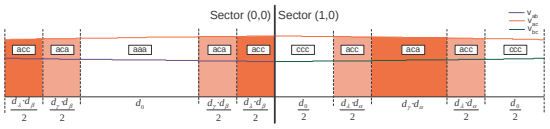

Fig. 14. Vector jump during sector change.

The low order harmonics are proposed to be avoided by choosing the vectors in reverse order. This cleans the spectrum as displayed on Fig. 22 to Fig. 23, and an improved modulator is obtained.

IV. Harmonic Analysis

The strategies are evaluated concerning the distortion on the input and output. This analysis was presented by [9] and the idea is to calculate the harmonic flux produced by the changing of the switch vectors.

During a switch period the flux in the motor will follow the black lines seen on Fig. 15. A distortion index can then be made by calculating the RMS value of the flux error. The error can be found from (20) as:

$$\psi_{RMS} = \sqrt{\sum_{n=1}^{10}\left(\begin{array}{l}\mathrm{Re}(\psi_{n-1})\cdot\mathrm{Re}(\psi_n)+\dfrac{(\mathrm{Re}(\psi_n)-\mathrm{Re}(\psi_{n-1}))^2}{3}\\ +\mathrm{Im}(\psi_{n-1})\cdot\mathrm{Im}(\psi_n)+\dfrac{(\mathrm{Im}(\psi_n)-\mathrm{Im}(\psi_{n-1}))^2}{3}\end{array}\right)\cdot(d_n-d_{n-1})} \tag{20}$$

The same evaluation can be done for the harmonic charge on the input capacitor, giving an index showing the load on the capacitors. The curves shown on Fig. 16 and Fig. 17 are normalized by the factors shown in (21).

$$\psi_{norm} = \frac{T_{sw}\left|\vec{V}_{in}\right|}{2}, \quad Q_{norm} = \frac{T_{sw}\left|\vec{V}_{in}\right|\cdot m_{mc}}{2\left|Z_{phase}\right|\cdot\cos(\varphi_{out})} \tag{21}$$

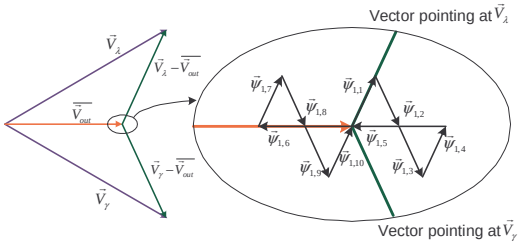

Fig. 15. Harmonic flux in a matrix converter.

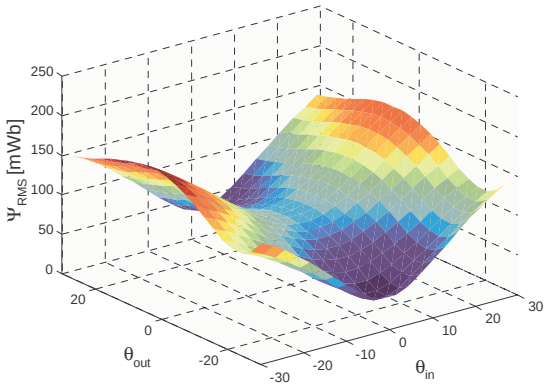

Fig. 16. Harmonic flux for the low distortion modulator.

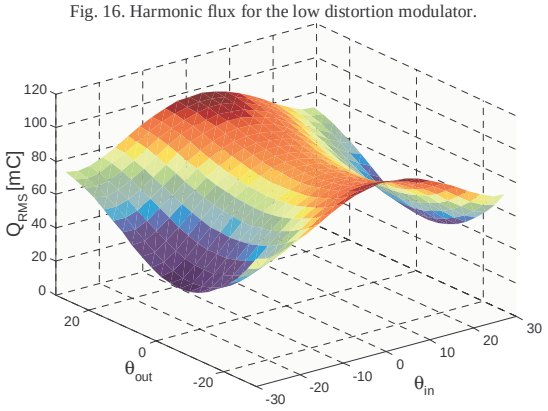

Fig. 17. Harmonic charge for the low distortion modulator.

The contour plots shown on Fig. 16 and Fig 17 are plotted for an input and output space vector angle spanning from –30° to +30° and a modulation index of 1. The power factor on the input and output are both one. From the curves the average shown on Fig. 24 and 25 are found.

V. Results

The simulated results are compared to the measured results from the prototype. The simulation model proves its usefulness in determining the location and origin of the harmonic distortion.

A. Simulated and Measured Results (FFT)

In Fig. 18 the output phase-to-phase voltage is seen (right) and the input current is seen on the left. The curve with the highest amplitude is the input phase current and the lower one is the input phase voltage plotted to show that the current and voltage are in phase. Similar measurements are used to calculate the FFT shown on Fig. 19 to Fig. 23.

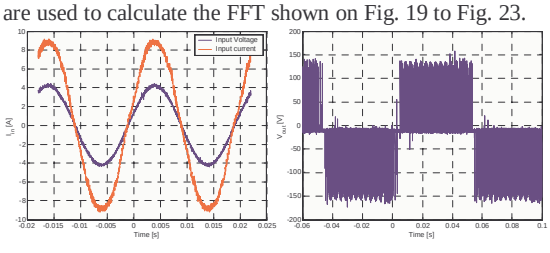

Fig. 18. Measured output voltage and input current (low-distortion).

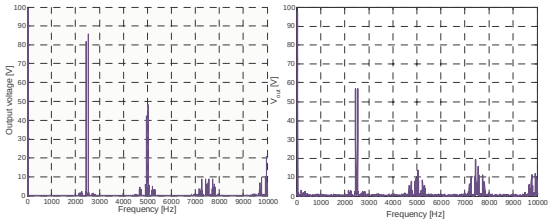

Fig. 19. Simulated and measured output voltages for the 8-switch.

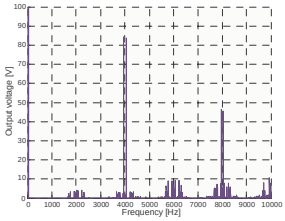

Fig. 20. Simulated output voltages for the 10-switch.

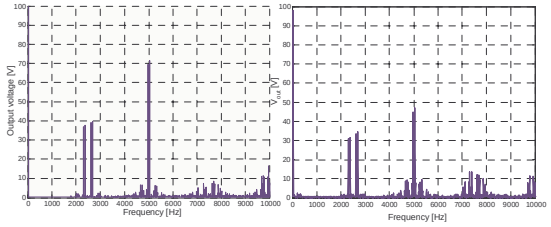

Fig. 21. Simulated and measured voltages for the low distortion.

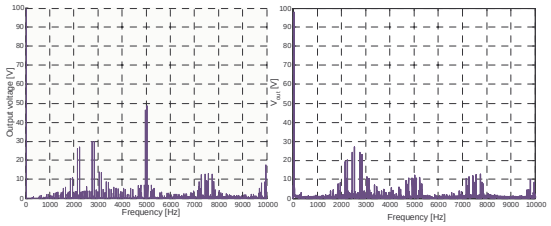

Fig. 22. Simulated and measured voltages for the low loss.

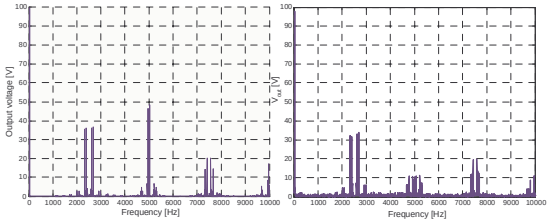

Fig. 23. Simulated and measured voltages for the modified low loss.

B. Comparison of harmonic flux and charge

The distortion for the harmonic flux and charge are calculated as a mean over 360° span for both the input and output angle. The distortion is plotted for a modulation index ranging from 0 to 1, and the mean harmonic charge are plotted for power factor 1 and 0.5 on the output. The power factor of the input is unity for all calculations, simulations and measurements.

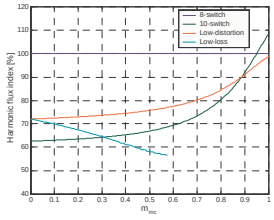

Fig. 24. Mean distortion of the output flux for the modulation functions.

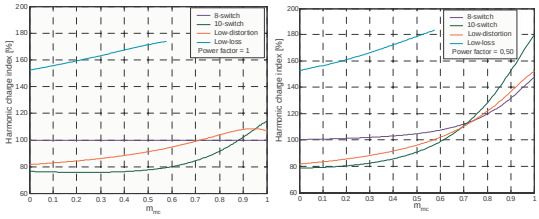

Fig. 25. Mean distortion of the input capacitor charge at PF=1 and PF=0.5.

From Fig. 24 and Fig. 25 it can be seen that the distortion is depending on the modulation index, giving that the most advantageous strategy should be chosen for the desired operating area.

VI. Conclusion

The matrix converter technology is by many considered to be a complicated technology. In this paper it is shown that prior knowledge of standard B2B drives can be used to understand the matrix converter. A new low distortion modulation strategy that performs well compared to existing modulators is presented, and the strategy is compared to three existing modulators. The comparison is done on the basis of analytical and simulation tools, which have been experimentally verified using a matrix converter prototype. In the paper it is also shown how rapid changes in the space vectors position can generate harmonic distortion, and a solution is presented to improve the performance of the low-loss modulator.

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