High Mobility Amorphous Polymer-based 3D Stacked Pseudo Logic Circuits through Precision Printing

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Abstract

Conjugated polymers have great potential for deformable electronic applications due to their excellent mechanical properties with sufficiently high charge carrier mobilities. Direct printing of conjugated polymer thin-film transistors enables the fabrication of deformable devices with low cost, high throughput, and large area. However, a relatively poor device performance of printed devices remains a major obstacle to their application in high-end display backplanes and integrated circuits. In this study, we developed high-performance and highly stackable printed organic transistors, arrays, and circuits using a near-amorphous polymer, indacenodithiophene-*co*-benzothiadiazole (IDT-BT). Our printed devices exhibited high saturation mobility (>1 $cm^2 \cdot V^{-1} \cdot s^{-1}$), high on/off ratio (>$10^7$) and low subthreshold slope (245 $mV \cdot dec^{-1}$). In addition, 16×16 printed IDT-BT arrays achieved 100% fabrication yield, with excellent device-to-device uniformity and low variations of mobility (9.55%) and threshold voltage (4.51%), and good operational and environmental stability (>365 days). Furthermore, we demonstrated five stacked 3D transistors with an excellent 3D uniformity without compromising device performance due to a low required thermal budget for processing amorphous IDT-BT. Finally, we propose and fabricate a new concept of 3D universal logic gate with high voltage gain (33.91 V/V) and record density (100 printed transistors per cm^2), which is relevant for commercialization of low-cost printed display backplanes and high-density integrated circuits based on highly processable polymeric semiconductors.

1. Introduction

Conjugated polymer organic semiconductors (OSCs) are highly promising for deformable electronic applications due to their solution processability, low temperature, and printability.[1] Over the past 25 years, various molecular structures and doping methods have been explored to significantly improve the device performance.[2–4] Despite these advancements, the transport properties within conjugated polymer films encounter constraints arising from pervasive conformational and energetic disorder.[5] These limitations impede not only the design of high-performance materials, but also the study of physical phenomena related to the extended π-electron delocalization along the polymer backbone. In order to mitigate these effects of disorder, the field has conventionally focused on improving the crystallinity of conjugated polymers via introducing higher molecular weights,[5] new molecular designs,[6,7] and processing techniques[8] for increasing the proportion of crystalline to amorphous regions in the film.

A breakthrough in new molecular designs for high-mobility semiconducting polymer emerged where indacenodithiophene-*co*-benzothiadiazole (IDT-BT), a donor-acceptor polymer with an amorphous morphology showed a field-effect mobility of up to 1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ via an enhanced intrachain ring planarity of the conjugated backbone.[9–11] The amorphous morphology of IDT-BT can increase the degree of freedom in processing the polymer-based active layer, and therefore the TFTs, without strict requirements for annealing at relatively high temperature or solvent engineering, both of which are common methods for inducing a highly crystalline morphology of small-molecule and polymer films for improving the TFT mobility.[12–14] Direct printing of organic TFTs enables the fabrication of deformable devices in low-cost, high-throughput, large-area, and eco-friendly manner. Many studies have successfully realized an array of deformable devices, integrated circuits, memory cells, etc.[15–17] However, printed TFTs have faced a major challenge due to their poor device performance relative to spin-coated devices, often due to ill-controlled morphology of active organic thin film channels. IDT-BT offers advantages that effectively address chronic problems in printed organic electronics with unique disorder-free charge transport properties, resulting in exceptional electrical properties.[10,18,19]

Especially, considering the current roadmap for vertically stacking integrated circuits (ICs) in three-dimensional fashion for realizing ultrahigh-density IC devices, minimizing the required thermal budget is a critical requirement, especially for meeting the back end of line (BEOL)-compatibility that allows the fabrication of top-layer devices without deterioration in the functionality and performance of the bottom-layer devices.[5,20–22] In this regard, we have

recently succeeded in a three-dimensional (3D) monolithic integration of complementary organic TFTs via direct printing methods to explicitly demonstrate the potential for realizing high-density organic ICs.[23] However, modest electrical characteristics of printed devices and significantly large device performance discrepancy between p- and n-type OSCs continue to pose a significant obstacle for their deployment in practical applications. Furthermore, continuous thermal stress during fabrication can significantly damage OSCs and drastically degrade the IC performance.[24] Using p-type IDT-BT TFTs with high performance and low required thermal budget for processing is facile way to design and fabricate high performance and high density printed ICs for applying real applications.

Here, we present high-performance and vertically stackable printed organic TFTs, arrays, and logic circuits using an amorphous polymer indacenodithiophene-*co*-benzothiadiazole (IDT-BT) with exceptional electrical performance and high thermal stability to overcome chronic problems in printed organic transistors. Our fabrication approach involves using nozzle printing to create a uniform OSC film morphology and inkjet printing to pattern all the electrodes without the need for a mask. The printed IDT-BT TFTs exhibited superior device performance (comparable to that of spin-coated IDT-BT devices) relative to previously reported polymer-based printed devices, including high electrical properties with mobility, on/off ratio and subthreshold swing, an outstanding manufacturing yield and uniformity, and high operational and environmental stability. After device-level investigation, we accomplished 3D integration of five TFTs on a highly flexible substrate, demonstrating remarkable device uniformity in 3D. Finally, we propose a concept of universal pseudo logic gate in a 3D configuration. The 3D integrated circuits showed a high voltage gain and a record-setting transistor density, providing a unique and unprecedented approach for designing and producing high density digital circuitry crucial for emerging applications.

2. Results and Discussion

2.1. Device characteristics of high-mobility IDT-BT-based printed TFTs

High-performance printed organic TFTs using C_{16}IDT-BT with low energetic disorder were configured in a top-gate bottom-contact geometry with seven functional material layers; ultrathin substrate, source/drain, hydrophobic bank, OSC, dielectrics, and gate (**Fig. 1**a). This structure was selected because of the superior injection characteristics of typical staggered configuration of the gate and the source/drain contacts. All gate and source/drain electrodes were inkjet-printed with Ag-nanoparticle ink. To improve charge injection, the source/drain electrodes were treated with a pentafluorobenzenethiol (PFBT) self-assembled monolayer

(SAM). A p-type C_{16}IDT-BT ink was nozzle-printed within a rectangular hydrophobic bank-guided area. An inter-dielectric layer was formed by spin-coating with CYTOP to prevent penetration of parylene monomer and minimize water-related traps at the semiconductor-dielectric interface. A main dielectric layer was formed by chemical vapor deposition with a parylene to improve the environmental stability. A microscopic image of the fabricated device is shown in **Fig. 1**b. Due to the continuous printing and drying of the OSC ink, an atomic force microscopy (AFM) topology of the printed OSC film showed a smooth surface (**Fig. 1**c).

Achieving high carrier mobility in printed TFT devices has been difficult due to the lack of high performance printable OSC channel materials and optimal fabricating methods for providing uniform films in large-area. We investigated the effect of varying the IDT-BT concentration of a printed OSC ink on the electrical properties of devices (**Fig. 1**d and Fig. S1). Reducing the thickness of the printed film can improve device performance because the vertical access resistance is reduced. In addition, the bank was removed to coat a CYTOP layer, which can reduce the surface roughness of the printed film. When comparing the transfer curves of devices with and without the CYTOP layer, it was found that there was a significant boost in performance (18.5 times greater mobility and 21 times greater the on current) (Fig. S2). The saturated hole mobility μ_{sat} was found to fluctuate with the polymer concentration, whereas the on/off ratio (I_{on}/I_{off}) remained relatively unchanged at around 10^7 across the range of concentrations. The TFT performance was optimized at C_{16}IDT-BT concentration of 2.4 $mg{\cdot}ml^{-1}$ with an average μ_{sat} of 1.11 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$ and I_{on}/I_{off} of 1.52×10^7. The device performance is decreased when the average channel thickness was below 10 nm, which may be due to a weaker connectivity of polymer chains networks for enhancing charge transport (Fig. S3). Drain current (I_D) *vs.* drain-source voltage (V_{DS}), *i.e.*, output characteristics, of the optimized device showed linear characteristics having a low contact resistance and good saturation behavior acting as constant-current sources (**Fig. 1**e). Transfer characteristics (I_D *vs.* V_{GS}) of the printed device were obtained in the saturation regime ($V_{DS} = -10$ V) (**Fig. 1**f). The representative printed TFTs showed the μ_{sat} of 1.18 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$, threshold voltage ($V_{TH}$) of −3.07 V, and subthreshold swing (SS) of 251 $mV{\cdot}dec^{-1}$. Notably, our printed TFTs showed a significantly superior performance compared to printed polymer-based devices[25–32] and comparable performance compared to spin-coated IDT-BT devices (**Table 1**).[9–11,33–35]

High mobility values of these printed TFTs indicate a high-quality dielectric/semiconductor interface that has been formed with our printing method. To investigate this further, we performed several device analyses. The upper limit for the interfacial trap density (N_{trap}^{max}) values can be estimated from the obtained SS values from the transfer

curves. $N_{\mathrm{trap}}^{\mathrm{max}}$ of our device was estimated to be 2.2×10^{11} $\mathrm{cm}^{2}\cdot\mathrm{eV}^{-2}$, which is comparable to that of spin-coated IDT-BT transistors (Table S1). In addition, the printed devices showed an ideal linearity of the square root of the saturation current and nearly gate-voltage independent mobility, leading to an unambiguous extraction of the carrier mobility (**Fig. 1**g). The temperature dependence of I_D on V_G in the saturation and linear regimes was fitted to $I_D \propto (V_G - V_{TH})^{\gamma}$ between 100 K and 340 K (**Fig. 1**h). Our devices exhibited the ideal exponent γ with temperature-independent values of 2 and 1 in the saturation and linear regimes, respectively. The saturation and linear mobilities at different temperatures were shown in an Arrhenius plot (**Fig. 1**h, inset). From the Arrhenius plot, the extracted E_a values in the linear and saturation regime were 51 meV and 49.7 meV, respectively (Fig. S4), which are comparable to the previously reported values (Table S2). Our results confirm a similar high-quality dielectric/semiconductor interface that enables a nearly disorder-free transport, as that of spin-coated IDT-BT devices, which provide direct experimental evidence for promoting these class of near-amorphous conjugated polymer materials as a printable active channel for TFTs.

High mobility values also enable high-speed operation of the printed devices. To confirm the benefit of high mobility, we observed the dynamic characteristics of the printed top-gate IDT-BT TFT. Transient response of the device showed stable operation for 100 cycles under a frequency of 100 Hz (**Fig. 1**i). When applying a single V_{GS} pulse to the printed device, the I_{DS} showed that the current becomes larger in the on state and smaller in the off state as the V_{GS} is turned on and off (**Fig. 1**j). In addition, we measured the transient response of the device according to various V_{GS} pulses with a frequency of 0.01, 0.1, 1, 10, 25, and 50 kHz (**Fig. 1**k). The cutoff frequency at which the normalized I_D is decreased by a factor of -3 dB is extracted to be 37 kHz, which corresponds to the estimated value from the current-gain cutoff frequency equation with the expected overlap capacitance.

2.2. Array characteristics of IDT-BT-based printed TFTs with large-area uniformity

IDT-BT offers several advantages that help address the chronic problems of organic semiconductors. First, it provides uniform electrical properties due to its near-amorphous microstructure with low energetic disorder. We demonstrated high uniformity of IDT-BT by fabricating 16 × 16 printed TFT arrays on 3 μm-thick ultrathin parylene film (**Fig. 2**a). The 256 C_{16}IDT-BT-based printed TFTs displayed remarkably uniform saturation transfer curves ($V_{DS} = -10$ V) with 100% fabrication yield (**Fig. 2**b). The properties of these devices, including channel geometry (L and W), μ_{sat}, V_{TH}, and SS, were thoroughly evaluated by statistical analysis. Histograms of the variations reveal an extraordinary level of device-to-device uniformity with

narrow distributions of L, W, μ_{sat}, V_{TH}, and SS (**Fig. 2**c). The relative standard deviation (RSD) of L, W, μ_{sat}, V_{TH}, and SS for 256 TFTs was 9.35%, 1.72%, 9.55%, 4.51%, and 9.35%, respectively. Our inkjet printing process achieves highly consistent L and W with the device variation of less than 10% for 256 channel geometries. In addition, our nozzle printing process allows the ink to be deposited and patterned evenly over a large area, resulting in a highly uniform μ_{sat} for 256 printed devices. It is noteworthy that the μ_{sat} variation is reduced by considering the channel geometry. The average and RSD values of the recalculated mobility decreased from 0.984 to 0.980 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and from 9.56% to 9.48%, respectively. In addition, the 32 and 128 devices with similar channel geometry showed remarkably uniform mobility RSD values of 1.65% and 4.35%, respectively. These values are much lower than those of previously reported solution-processed emerging material (organic, perovskite, carbon nanotube (CNT), and 2D)-based TFT arrays with various fabrication methods (**Fig. 2**d).[36–59] Furthermore, small variations in V_{TH} and SS values clearly confirm that the semiconductor/dielectric interface formed is not only of high-quality but with a high uniformity. The uniformity in the V_{TH} values of the 256 printed TFTs outperforms those of the other OSCs, polycrystalline silicon, indium gallium zinc oxide, CNT, 2D materials (Fig. S5).

We then assessed the reliability of the printed TFT arrays under given electrical and environmental stresses. Our devices showed stable electrical operation when biased at V_{GS} & $V_{DS} = -10$ V for 10^4 s (about 2.78 hours) (**Fig. 2**e). The initial increase in current can be attributed to the slow polarization of parylene and the decrease after the I_D peak is negligible. To quantify an excellent bias stability of the printed devices, we tracked the normalized I_D values of five printed devices. The normalized I_D values were calculated by normalizing I_D values at 10^4 s of bias with I_0 at 0 s or I_D peak, from which we observed that the change in the normalized I_D values under-bias stress were +6.28 ± 1.14% and −1.72 ± 0.38%, respectively. Remarkably, our devices maintained their electrical characteristics for 365 days with a negligible degradation when stored in a dry ambient environment (**Fig. 2**f). After 365 days, μ_{sat} still remains above 1 $cm^2 \cdot V^{-1} \cdot s^{-1}$, V_{TH} slightly decreased, and SS continues to increase. The change in μ_{sat}, V_{TH}, and SS values for 365 days with respect to the day 1 was -2.03%, -16.01%, +94.06%, respectively. Further reliability tests were performed under thermal stress conditions. The printed TFTs were heated from 30 °C to 150 °C in five successive thermal stresses for the duration of one hour and the device showed stable operation until 120 °C (Fig. S6). Overall, our printed IDT-BT TFTs showed sufficient robustness for many real-world applications, ranging from light-emitting diode arrays to sensor arrays and integrated circuits, owing to their high uniformity, excellent electrical properties and environmental stability.

2.3. 3D TFTs based on highly stackable IDT-BT and precision printing

The near-amorphous microstructure of IDT-BT thin films facilitates 3D integration of TFTs without degradation of device performances due to their low thermal budget requirements. We achieved this by designing and fabricating a vertical stack of five TFTs (5-T). The 5-T 3D TFTs comprise 40 functional layers in total; a parylene-coated plastic foil, ten conductor layers, five charge injection SAM layers, five bank layers, five C_{16}IDT-BT layers, five CYTOP layers, and nine parylene layers (**Fig. 3**a). A scanning electron microscopy (SEM) image of the fabricated 5-T 3D TFTs confirmed a conformal deposition of all functional layers as designed without a significant physical damage, which ensured a high yield and uniform device performance (**Fig. 3**b). A top view image of the 5-T devices is shown in **Fig. 3**c, demonstrating a remarkable accuracy with which the five designed TFTs are stacked within a region comparable to that of a single TFT through our precision-printing process. In the center of the 3D TFTs, five patterned C_{16}IDT-BT films were vertically stacked in the same horizontal position. All metal layers inkjet-printed on each dielectric layer can be interconnected on the top floor through laser-drilled via-holes. To control the 5-T devices independently without interfering neighboring devices, we designed the routing at different locations and layers to ensure that only the desired devices are selectively operated. In overall, we developed an array of 15×10 printed 3D TFT and confirmed the 3D uniformity of the IDT-BT devices (**Fig. 3**d).

The transfer characteristics (I_D *vs.* V_{GS}) of the printed TFTs on each floor were measured in the saturation regime ($V_{DS} = -10$ V) to test their uniformity (**Fig. 3**e). All 80 3D TFTs (16 devices fabricated on each floor) exhibited highly uniform transfer characteristics, with no discernible performance degradation with each additional stacking. Notably, the characteristics of the printed devices on the first floor were similar to those on the additional floors, even though they were exposed to over 7 hours of thermal stress below 120 °C during the fabrication processes of the entire vertical device stacks. The uniformity of 5-T stacked 3D TFTs was investigated by extracting the on-current (I_{ON}), μ_{sat}, and V_{TH} values (**Fig. 3**f). The 2D uniformity of the printed devices (i.e. within the same floor) was assessed by the variation of $|I_{ON,avg}|$, $\mu_{sat,avg}$, and $V_{TH,avg}$ values which were below 7.27%, 9.02%, and 2.13% respectively. For the 3D uniformity (i.e. across the entire floors), the RSDs of the average $|I_{ON}|$, μ_{sat}, and V_{TH} values were determined to be 9.86%, 7.07%, and 4.53%, respectively. These results highlight the effective and reliable fabrication processes and materials selection, that have been employed to ensure both an excellent 2D and 3D uniformity.

2.4. 3D NAND logic circuits based on 3D printed IDT-BT TFTs

Leveraging the 3D integration of printed TFTs, we propose a new concept of a universal logic gate NAND in a 3D configuration (**Fig. 4**a). Unlike a conventional pseudo-NAND that consist of six p-type transistors, this 3D pseudo-NAND has been achieved using only four vertically stacked TFTs – two top-gate transistors and two dual-gate transistors (**Fig. 4**b). The independent gates of two p-type transistors connected in parallel (T_1 & T_2 or T_3 & T_4) can effectively act as one p-type dual-gate transistor. This design not only reduces the transistor area by 1/6 compared to the conventional pseudo-NAND gate, but it also dramatically shortens the interconnection lines on the 2D plane, resulting in a 3D interconnection of only a few micrometers or less through the via-hole process. Photograph of microscopy image showed the 3D pseudo-NAND gate of all metal layers on floors input A, input B, output Q, V_{DD}, V_{SS}, and GND (**Fig. 4**c, inset). The AFM topology of the printed 3D NAND showed smooth surface roughness (Fig. S8).

The voltage transfer characteristics (V_{OUT} vs. V_{IN}) of the printed 3D pseudo-NAND gates were measured with supply voltages (V_{DD} = 10 V and V_{SS} = −15 V) (**Fig. 4**c). The output characteristics for two inputs in the printed 3D NAND gate were found to be almost identical. The uniformity and performance of the 3D pseudo-NAND gates was investigated by measuring the voltage gain (G_V) and switching voltage (V_{SW}) with input A and B. These are represented as histograms of the statistical variation in G_V and V_{SW} for input A and B (**Fig. 4**d). The G_V and V_{SW} of 36 devices showed an RSD of 8.39% and 1.36% for input A and 9.56% and 1.69%, for input B, respectively (**Fig. 4**d). The maximum voltage gains ($G_{V,MAX}$) of input A and B of are 33.91 and 30.53 V/V, respectively, which are significantly higher than previously reported NAND gates fabricated by solution-processed OSCs (**Fig. 4**e).[56,60–66] These results emphasize and rely on an excellent uniformity and voltage gain characteristics of our printed NAND gates.

Finally, to prove the scalability of our 3D NAND gates based on the printed IDT-BT devices, we demonstrated various logic gates (NOT, buffer, and AND) by interconnecting 3D NANDs (**Fig. 4**f). Logic gates with opposite characteristics, such as NOT and Buffer, or NAND and AND, showed similar DC characteristics, which can be attributed to the superior uniformity of 3D NAND gates based on our printed IDT-BT devices. This work has achieved a record transistor density for printed organic circuits, based on the 3D pseudo-NAND design being counted as six transistors (**Fig. 4**g).[23,60,64,67–82] The 3D stacking of TFTs provides a significant reduction in the cell area; a simple scaling argument demonstrates that for a transistor density of 25 printed transistors per cm^2 achievable for 2D pseudo-NAND by inkjet printing, the transistor density of printed 3D NAND (with six transistors) can be 4 times larger (i.e. 100

transistors per cm^2). This achieved transistor density suggests that around 4,500 transistors could be fabricated on the back of an adult's hand with an area of ~ 45 cm^2. This is comparable with the number of transistors in a commercial 8-bit microprocessor early in the computer revolution, which demonstrates a technological advance featured in our work that could herald the beginning of low-cost printable wearable computing devices.

3. Conclusion

This work presents significant advancements in the fabrication of high-performance and highly stackable printed organic TFT circuits using a near-amorphous semiconducting polymer, C_{16}IDT-BT. Our printed IDT-BT-based TFTs exhibited remarkable electrical characteristics, including high μ_{sat} of >1 $cm^2\cdot V^{-1}\cdot s^{-1}$, high I_{on}/I_{off} of >10^7, and low SS of 251 $mV\cdot dec^{-1}$. More importantly, the array of 16×16 printed TFTs demonstrated a 100% manufacturing yield and exceptional device-to-device uniformity with a low V_{TH} variation of 4.51% and low μ_{sat} variation of 9.55%. These results are among the best in comparison with devices based on other solution-processed emerging semiconductor materials (carbon nanotube, perovskite, 2D) and even commercial LTPS and oxide-based devices. Our printed TFTs showed robust operational and environmental stability over 365 days. Furthermore, the implementation of 5-T stacked 3D TFTs highlighted excellent 3D uniformity and performance. Finally, we introduced a novel concept of 3D pseudo-NAND gate with a high voltage gain of 33.91 V/V and a record density of 100 printed transistors per square centimeter. These results will provide commercially viable material and processing solutions for low-cost and high-throughput fabrication of high-performance organic electronic devices, which are compatible for designing printed active-matrix backplanes for display, large scale integration and application-specific integrated circuits for functional applications.

4. Experimental Section/Methods

C_{16}IDT-BT Synthesis: C_{16}IDT-BT was prepared according to a literature procedure,[9] using 2,7-dibromo-4,4,9,9-tetrahexadecyl-4,9-dihydro-s-indaceno[*1,2-b:5,6-b'*]dithiophene (560 mg, 0.424 mmol) and 4,7-bis(4,4,5,5-tetramethyl-1,3,2-dioxaborolan-2-yl)benzo[*c*][*1,2,5*]thia-diazole (164 mg, 0.424 mmol), $Pd_2(dba)_3$ (2 mol%), $P(o\text{-}tol)_3$ (4 mol%) and a drop of Aliquat 336. The monomers, catalyst and ligand were dissolved in degassed toluene and further degassed with nitrogen for 30 min. Degassed Na_2CO_3 solution (1.0 M, 1 mL) was added to the mixture. The reaction mixture was degassed for 10 min then stirred and heated at 120 °C for 48 h. After end-capping with tributylstannylthiophene (6 h) and 2-bromothiophene (6 h), the

reaction mixture was cooled to room temperature and precipitated into methanol. The solid was collected by filtration and further purified in a Soxhlet setup with methanol, acetone, and hexane for 24 h each. The residual solid was redissolved in chloroform and precipitated into methanol. The polymer was collected by filtration and dried under vacuum overnight. Yield: 460 mg (84 %). ^{1}H NMR ($CDCl_3$, 400 MHz, δ (ppm)): 8.11 (s, 2H), 7.95 (s, 2H), 7.41 (s, 2H), 2.41-1.77 (m, 8H), 1.38-1.94 (m, 112H), 0.86 (t, 12H). GPC in CB at 80 °C (against polystyrene standards); M_n: 58 KDa, PDI: 1.2

Material Preparation: An Ag-nanoparticle ink in hydrocarbon-based solution (NPS-JL, Harima Chemicals, Inc.) was used as a conductive metal ink. A pentafluorobenzenethiol (PFBT) were prepared in 30 mM solutions using isopropanol (IPA) to modify the work function of the printed Ag contact electrodes by self-assembled monolayer (SAM) treatment. To precisely define the semiconductor area, a hydrophobic fluoropolymer Poly[4,5-difluoro-2,2-bis(trifluoromethyl)-1,3-dioxole-*co*-tetrafluoroethylene] (Teflon AF1600, Sigma-Aldrich) was prepared in a 1 wt% solution using perfluorotributylamine (Fluorinert FC-43, 3M). For p-type semiconductor ink, the lowest degree of energetic disorder polymer IDT-BT with various concentrations (3, 2.4, 2.1, 1.5, 1.2 $mg{\cdot}ml^{-1}$) is dissolved in 1,2-dichlorobenzene (oDCB) (99%, Sigma-Aldrich). An amorphous fluorinated polymer CYTOP (CTL-809M, Asahi Glass) is dissolved with a special fluorinated solvent (CT-Solv. 180, Asahi Glass) with a volume ratio of 1:4 to form an inter-dielectric layer that blocks the penetration of parylene monomer. For main dielectric layer, a poly(p-xylylene) derivative parylene diX-SR (KISCO Ltd.) is deposited by chemical vapor deposition (CVD) (OBT-PC300, OBANG Technology).

Device Fabrication: A 3-μm-thick Parylene film was deposited by CVD on a glass substrate (Eagle XG, Corning) to form the ultrathin plastic film and control the wettability of the Ag-nanoparticle ink. On the parylene-coated surface, the source and drain electrodes were inkjet-printed using the Ag ink and a drop-on-demand inkjet printer (DMP2850, FUJIFILM Dimatix), which were then sintered at 120 °C for 30 min in air. To pattern the OSC layer, the hydrophobic fluoropolymer was printed in a rectangular shape using an air pulse nozzle printer (Image Master 350PC, MUSASHI Engineering) at a patterning speed of 50 $mm{\cdot}s^{-1}$ and a discharge pressure of 7 kPa. During the nozzle printing process, the platen temperature was set at 60 °C. Then, the hydrophobic bank was heated at 100 °C for 10 min to increase the adhesion between Teflon and lower layers. To improve the charge injection from S/D electrodes to OSC, samples were dipped into PFBT SAM solution for 5 min and then rinsed with pure IPA. The IDT-BT

inks were printed into the Teflon bank area by the air pulse nozzle printer at the discharge pressure of 1 kPa, the discharge time of 120 ms, and the stage temperature of 40 °C, followed by annealing at 100 °C for 30 min. The samples were then immerged in perfluorotributylamine for 5 min to remove the Teflon bank layer. CYTOP with ST-Solv. 180 (1:4) was spin-coated at 2000 rpm for 30 s and annealed at 100 °C for 10 min, having a thickness of 53.7 nm. For main dielectric layer, parylene film was conformally deposited to a thickness of 185.4 nm by the CVD process. The 2D device fabrication for printed organic transistors and arrays was finished by inkjet-printing the top-gate electrodes. To fabricate the 5-stacked TFTs, top-gate TFTs were formed sequentially using the same 2D fabrication process. For 3D pseudo-NAND circuits, two top-gate TFTs and two dual-gate TFTs with shared gate electrode were monolithically stacked. Via holes for all devices were formed by laser-drilling in-between dielectric layers, and then filled by inkjet-printing the Ag ink.

Device Characterization: The DC and AC *I-V* characteristics of printed devices were measured with source and pulse measure units (SMU and PMU) of a semiconductor parameter analyzer (4200-SCS, Keithley) under ambient conditions. The temperature dependent electrical properties of the TFTs were measured using a semiconductor parameter analyzer (4156B, Agilent) in vacuum chamber probe station (M5VC, MSTECH). Temperature was varied from 100K to 340K with liquid Nitrogen and hot chuck controller. The thickness of the dielectric layers was measured with a stylus profiler (Dektak XT, Bruker).

Parameter Extraction: The threshold-voltage of this work was extracted by fitting $I_D^{1/2}$-V_{GS} saturation curves in the region between −8 and −9 V. The saturation and linear charge-carrier mobility values were determined from the slopes of $I_D^{1/2}$-V_{GS} and I_D-V_{GS} in the region between −8 and −9 V, following the equations:

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2 \ and \ \mu_{lin} = \frac{L}{WC_iV_{DS}}\frac{\partial I_D}{\partial V_{GS}}$$

Where W and L are the width and length of the device, and C_i is the total capacitance per unit area (1.11×10^{-8} F·cm^{-2}) of the 239.1 nm-thick CYTOP/parylene bi-layered dielectric (ε_r=2.985). The total capacitance is calculated in a capacitor in which the CYTOP and parylene layers are connected in series. The equation for calculating total capacitance is as follows:

$$C_i = \frac{\varepsilon_r}{d} = \frac{C_1C_2}{C_1 + C_2} = \frac{\frac{\varepsilon_1}{d_1}\frac{\varepsilon_2}{d_2}}{\frac{\varepsilon_1}{d_1} + \frac{\varepsilon_2}{d_2}} = \frac{\varepsilon_1\varepsilon_2}{\varepsilon_1 d_2 + \varepsilon_2 d_1}$$

Where C_1 and C_2 are capacitances of CYTOP and parylene, ε_1 and ε_2 are dielectric constants of CYTOP (ε_1=2.1) and parylene (ε_2=3.4), and d_1 and d_2 are dielectric thicknesses of CYTOP (d_1=53.7 nm) and parylene (d_2=185.4 nm).

The subthreshold swing (SS) was determined by fitting the following equation between the threshold and the onset voltages.

$$SS = \frac{\partial V_{GS}}{\partial \log(I_D)}$$

Under the assumption that the deep bulk states and interface states are independent of energy, the upper limit for the interfacial trap density can be estimated by following the equation:

$$N_{\mathrm{trap}}^{\mathrm{max}} = \frac{C_i}{q}\left[\frac{qSS}{k_B T \ln(10)} - 1\right]$$

Where k_B is the Boltzmann's constant, T is the absolute temperature, C_i is the capacitance per unit area of the gate dielectric and q is the electronic charge.

The current-gain cutoff frequency (f_T) can be expressed by following the equation:

$$f_T = \frac{g_m}{2\pi C_i} = \frac{\mu_{sat}(V_g - V_{TH})}{2\pi L(L + L_{OV,GS} + L_{OV,GD})}$$

Where g_m is the device transconductance, C_i is the total capacitance per unit area, μ_{sat} is the saturation carrier mobility, V_{TH} is the threshold voltage, L (40 μm for single device), $L_{OV,GS}$ (36.3 μm), and $L_{OV,GD}$ (90.9 μm) are the channel, parasitic gate-to-source overlap, parasitic gate-to-drain overlap lengths, respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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Figures

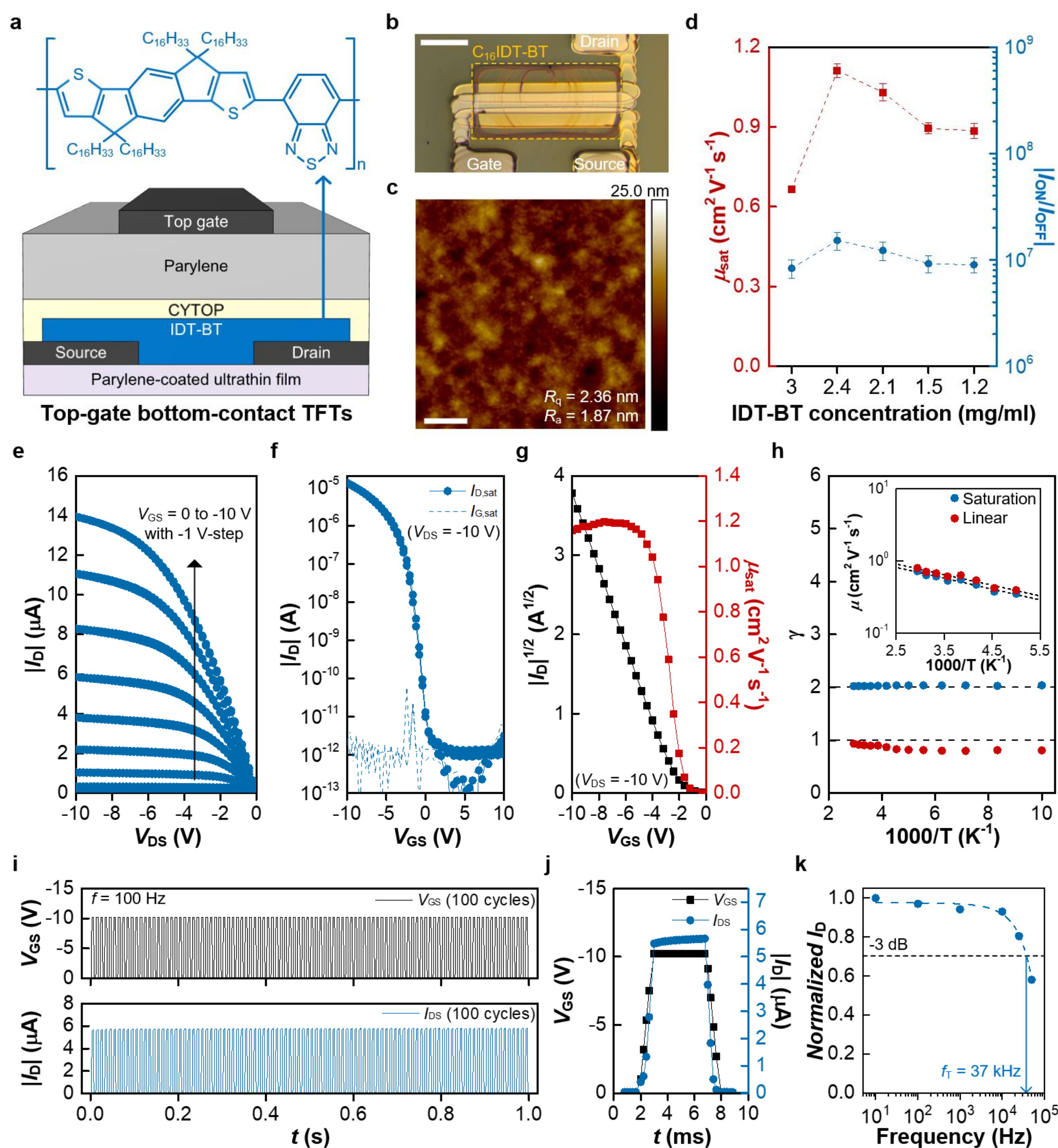

Figure 1. Device characteristics of C_{16}IDT-BT-based printed TFTs. (a) Molecular structure of IDT-BT and schematic cross-section of printed transistor with top-gate bottom-contact configuration. (b) Microscopic image of the fabricated device (scale bar, 500 μm). The dimensions of the device are L = 40 μm and W = 1500 μm. (c) AFM topology image of the printed transistors (scan size, 2 × 2 μm; scale bar, 400 nm). (d) Extracted carrier mobilities and on/off ratio in the printed TFTs with different IDT-BT concentrations (3, 2.4, 2.1, 1.5, and 1.2 mg/ml). Error bars were calculated from 7 individual devices. (e) Output curve ($|I_D|$ vs. V_{DS}) and (f) transfer curves ($|I_D|$ vs. V_{GS}) of the optimized TFTs (2.4 mg/ml). (g) Square root of the drain current and gate-voltage dependence of saturation mobility of the printed device. (h) γ vs. 1000/T in saturation and linear regimes. (inset) Arrhenius plot low-field and field-effect mobility extracted from the saturation and linear regimes. Dynamic characteristics of the printed TFTs. (i) 100 cycles of V_{GS} and I_{DS} with a period of 0.01. (j) Single cycle of V_{GS} and I_{DS} with a period of 0.01. (k) Frequency dependence of the normalized I_D as a function of frequency. Cut-off frequency is extracted from the frequency at which the normalized I_D decreases by -3 dB.

Table 1. Comparison with the previous polymer-based TFTs.

OSC [M_w (kDa)]	Processing Method of OSC	Dielectric [d (nm)]	V_{GS}, V_{DS} (V)	Mobility ($cm^2 V^{-1} s^{-1}$)	V_{TH} (V)	I_{ON}/I_{off} (log_{10})	*SS* ($V dec^{-1}$)	Ref.
IDT-BT [69]	Nozzle printing	CYTOP/Parylene (239)	-10	1.18	-3.07	>7	0.251	This work
IDT-BT	Inkjet printing	SiO_2 (90)	-3.5, -1	0.0035	>1	-	-	[25]
IDT-BT	Inkjet printing	PS/Parylene (260)	-25	0.47	-3.7	~5	-	[26]
P(NDI12-T2)	Inkjet printing	PS/Parylene (260)	30	0.13	11.4	~4	-	[26]
P(NDI12-T2) [280]	Gravure printing	D2200 (1,000)	80, 60	0.1–0.65	30–35	5–7	4–6	[27]
P3HT	Inkjet printing	PMMA (500)	-60	0.07–0.09	-20	~5	7.6	[28]
PC12TV12T	Inkjet printing	P(VDFTrFE)/PMMA (250)	-20	0.43	-3.1	~4	1.4	[29]
PHTBTz-C8 [14.2]	Inkjet printing	SiO_2 (300)	-40	0.25	-	6–7	1.05	[30]
DPPT-TT [50–100]	Inkjet printing	PMMA/Parylene (180)	-10	0.11	10.3	~6	0.44	[31]
DPP-DTT [111]	Nozzle printing	Parylene (200)	-10	0.1	-1.07	~5	-	[32]
IDT-BT [36]	Spin coating	CYTOP (900)	-60	1	-25	3~4	-	[9]
IDT-BT	Spin coating	CYTOP (500)	-60	1.5	-3	~4	-	[10]
IDT-BT [316.8]	Spin coating	CYTOP (500)	-60	1–2	7.7		4.3	[11]
IDT-BT [80]	Spin coating	CYTOP (800)	-60	2	-15	~6	-	[33]
IDT-BT [58.3]	Spin coating	CYTOP (480)	-50	1.5	-	~6	-	[34]
IDT-BT [112]	Spin coating	SiO_2 (300)	-60	1.15	-20.9	~6	-	[35]

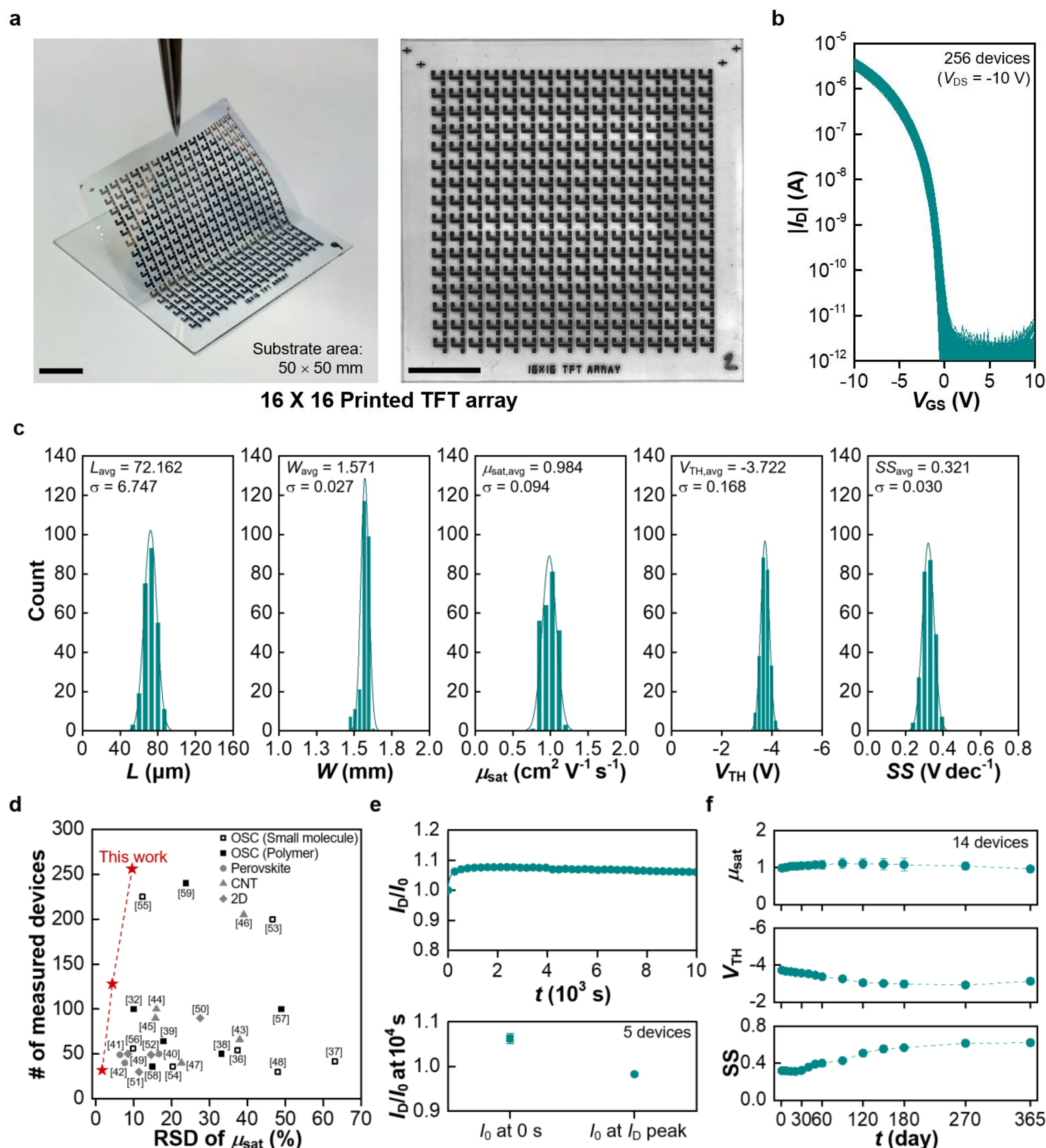

Figure 2. Array characteristics of C_{16}IDT-BT-based printed TFTs. (a) Photographs of flexible printed 16 × 16 TFT array (scale bar, 10 mm). (b) Transfer characteristics of the fabricated 256 TFTs. (c) Histograms of the 256 devices on channel length (*L*), channel width (*W*), saturation carrier mobility (μ_{sat}), threshold voltage (V_{TH}), and subthreshold swing (*SS*). (d) Number of measured devices vs. mobility's RSD compared to over 30 measured emerging material-based transistors (OSC, perovskite, CNT, and 2D). (e) Electrical stability of the devices after bias stress for 10,000 s (V_{GS} = V_{DS} = −10 V). (top) Representative data and (bottom) changing rate. (f) Long-term stability of the 14 measured devices on μ_{sat}, V_{TH}, and *SS*.

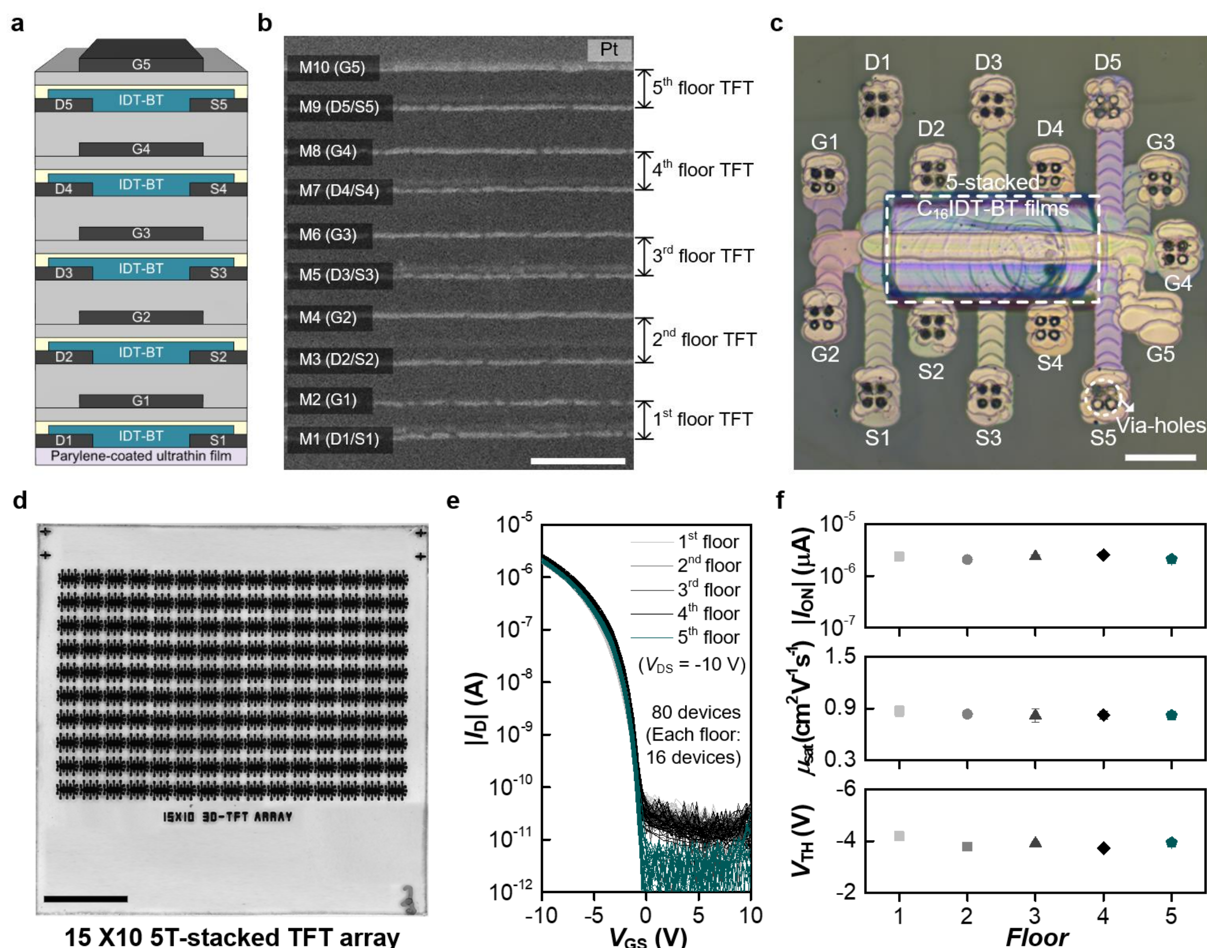

Figure 3. 3D characteristics of IDT-BT-based printed TFTs. (a) Cross-sectional schematic and (b) cross-sectional SEM image of 5-stacked IDT-BT TFTs (M1-10: metal layers, scale bar, 500 nm, Pt was sputtered on the top prior to the SEM measurement). (c) Microscopic image of the fabricated transistor (scale bar, 500 μm). (d) Photograph of 15 × 10 3D printed TFT array (scale bar, 10 mm). (e) Transfer characteristics of the 3D TFTs with 5 floors. 80 devices (16 devices for each floor) were measured and plotted. (f) Extracted parameters of the fabricated devices on I_{ON}, μ_{sat}, and V_{TH}. Error bars were calculated from 16 devices for each floor.

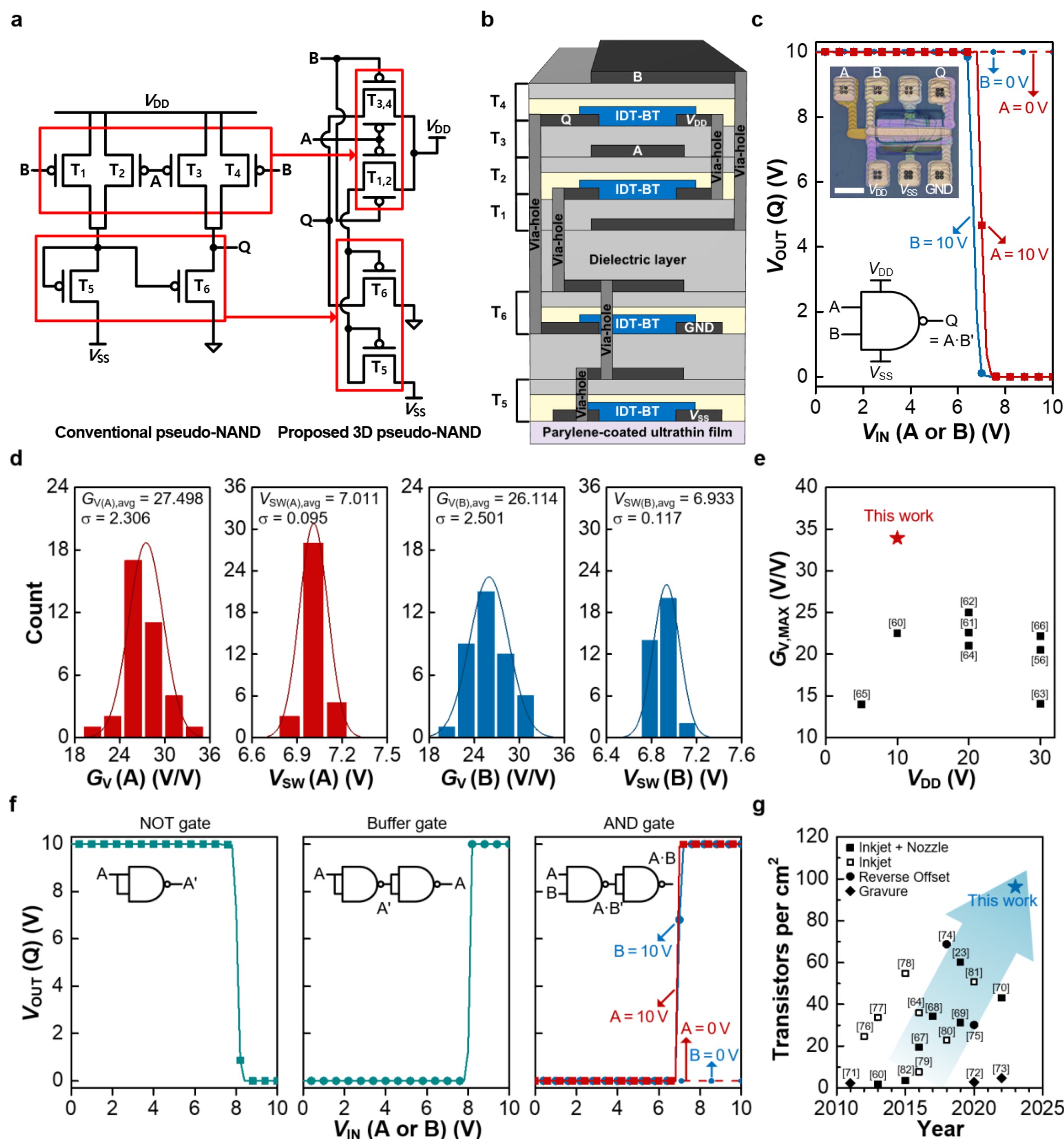

Figure 4. 3D NAND digital logic circuit based on 3D IDT-BT printed TFTs. (a) Circuit diagram of a conventional pseudo-NAND gate and a proposed 3D pseudo-NAND gate. (b) Schematic cross-section of 3D NAND gate. (c) DC V_{OUT}-V_{IN} characteristics of a 3D NAND logic gate with input A and B. (Inset) Microscopic image of the fabricated 3D pseudo-NAND gate (scale bar, 500 μm) and NAND gate symbol. (d) Histograms of the 36 devices on voltage gain (G_V) and switching voltage (V_{SW}) when sweeping inputs, A and B. (e) $G_{V,MAX}$ vs. V_{DD} of NAND gates by solution-processed OSCs. (f) V_{OUT}-V_{IN} characteristics of logic gates (NOT, buffer, and AND) by interconnecting 3D NANDs. (g) Transistor density trend of printed organic circuits fabricated by various printing techniques.