EJTAS
ISSN 2786-7447
EUROPEAN JOURNAL OF THEORETICAL AND APPLIED SCIENCES
OPEN ACCESS
PEER REVIEWED

Design and Implementation of C-Band Frequency Synthesizer Using LMX2592 IC

Ashok Kumar Khadolia, Amith S. Bhat ✉, Ramesh Babu Reddy, Md. Tosicul Wara
Spacecraft RF & Payload Checkout Divisions, Spacecraft Checkout Group,
U R Rao Satellite Center, Bengaluru-560017, India

Suggested Citation
Khadolia, A.K., Bhat, A.S., Reddy, T.R.B. & Wara, M.T. (2024). Design and Implementation of C-Band Frequency Synthesizer Using LMX2592 IC. *European Journal of Theoretical and Applied Sciences, 2*(1), 863-879.
DOI: 10.59324/ejtas.2024.2(1).76

Abstract:

The paper presents the design scheme and implementation of a PLL-based-frequency synthesizer using LMX2592 IC. The frequency synthesizer have vital role in the development of up-converter and down-converter equipments. Therefore, on the RT-Duroid RO4350 substrate, a low phase noise and stable carrier generator is designed and implemented. Graphical User Interface (GUI) & LAN based programming is developed to easily change the synthesizer frequency. The control system analysis using root locus and bode plot is presented for system stability. The experimental results representing the performance parameters, like frequency range, frequency step size, output power, phase noise, carrier stability, harmonics, and spurious, etc., are also presented in the paper. The analysis of spurious and phase noise performance at near integer boundary conditions are done by changing loop bandwidth and phase margin.

Keywords: *Charge Pump (CP), Graphical User Interface (GUI), Phase Frequency Detector (PFD), Phase Locked Loop (PLL).*

Introduction

The microwave has been broadly employed in numerous domains. The significant applications of microwaves include millimeter wave communications, radar, tracking, guidance, electronic warfare, and other areas (Skolnik, 2002; Crosson, Limaye, & Laymon, 2010; Ma, Wang, & Li, 2012; Yu, Xu, & Shen, 2012). The frequency synthesizer is a vital entity of any communication equipment. The frequency synthesizer behavior can instantly impact the wave-sending and receiving system quality. The phase-locked loop-based frequency synthesizer performs well with higher resolution frequency and broader bandwidth than different frequency synthesizing systems (Gao, & Gao, 2010; Zhu, & Wang, 2015; Tsai, Hsu, & Chao, 2015). The frequency band, phase noise, power output, spurious and harmonics are critical performance parameters of the frequency synthesizer.

Phase locked loop is an integrated-signal electronic circuit. It is mainly implemented with radio frequency (RF) and digital & analog co-design building blocks. The PLL is a non-linear negative feedback closed-loop control system. A PLL consists of a phase detector, loop filter, and voltage-controlled oscillator that locks the VCO phase to a reference signal. PLLs are used in many applications, including generating a clean, tunable, and stable reference frequency. It is also used in other applications, including a clock recovery circuit for high-speed communication, frequency modulation (FM) and demodulation,

generation of phase synchronous clock signals in microprocessors, etc.

The frequency synthesizers are used in many test and measurement equipment, defence and RADAR, cell phones, walkie-talkies, satellite receivers, etc. Frequency synthesizer stability and accuracy depend on the reference source; therefore, a temperature-compensated crystal oscillator is used as stable reference source input to the PLL. A frequency synthesizer generates a range of frequencies from a single reference frequency. In the frequency synthesis process, a new frequency is derived from a reference frequency by combining various additions, subtractions, multiplications, and divisions (Pandit, Deepak, & Basu, 2014).

The frequency synthesizer is widely classified into direct and indirect synthesizers. The direct forms of frequency synthesizer are implemented by creating a waveform directly without any form of frequency transforming element. The direct synthesizer is additionally sub-classified into direct analogue frequency synthesis (DAFS) and direct digital frequency synthesis (DDFS) (Kroupa, 2003). DAFS requires a lot of circuitry (integrate a mixer, filter, etc.) and is also called a mix-filter-divide architecture. The switching time performance of DAFS is excellent but consumes more power due to extensive circuitry. DDFS has a tiny resolution, excellent frequency switching time, and low phase noise. However, it has narrow output frequency range and has significant spurious components (Yang, Cai, & Lianfu, 2011). The indirect frequency synthesizer is based on PLL technology, where the output signal is generated indirectly. The VCO output is indirectly controlled by a low-frequency stable reference to obtain a highly stable output frequency. PLL frequency synthesizer has a broad output frequency range compared to the above schemes and significantly suppresses spurious signals.

The PLL-based frequency synthesizer in C-band will be used in the in-house development of up-converter and down-converter equipment.

The paper is organized into five different sections including the introductory Section 1. In Section 2, the C-band frequency synthesizer design principle is given. In Section 3, loop filter parameters & phase noise simulation results obtained from PLLatinum Sim software and control system analysis are discussed. In Section 4, detailed test & evaluation results for different performance parameters are given. Finally, we conclude Section 5.

C-Band Frequency Synthesizer: The Design Principle

This section discusses the specifications of the C-band frequency synthesizer, LMX2592 chip principles, system architecture & the device selection, schematic diagram, and software implementation.

Specifications of C-Band Frequency Synthesizer

The specifications of the C-Band frequency synthesizer are given in below Table 1.

Table 1. Specifications of C-Band Frequency Synthesizer

S. No.	Parameters	Specifications
1	Frequency Range	4000-6500 MHz
2	Frequency Step Size	0.5 kHz
3	Frequency Accuracy	±1 kHz
4	Internal Reference Stability	± 1 PPM over a day
5	Power Output	+ 10 dBm Minimum
6	Ageing	<± 4 PPM up to 15 years
7	SSB Phase Noise @ 1 kHz	-90 dBc/Hz
8	Output Impedance	50 Ω
9	Spurious	< -50 dBc
10	Harmonics	< -30 dBc
11	Memory Function	Non-Volatile
12	Programmability Function	Yes (LAN & GUI)

13	Supply Voltage	5V±10% & 500 mA DC (Nominal)
14	RF Connectors	SMA (Female)
15	External Reference Signal	Frequency: 10 MHz Amplitude: -3 to +3 dBm Phase Noise: Better than -150 dBc/Hz @ 1 kHz offset for 10 MHz Output Type: Sine Wave Impedance: 50 Ω
16	Operating Temperature	23±10 Degree C

Salient Features of C-Band Frequency Synthesizer

This in house developed C-band frequency synthesizer have multiple salient features supported by LMX2592 PLL chip as follows. Graphical user interface (GUI) & LAN based frequency programming, operation with external reference signal, automatic setting for Internal/External reference frequency source change over and continuous PLL lock monitoring on GUI as well as onboard LED. The main advantages of this development are easy to program, cost reduction, in-house serviceability (reduction in dependency on vendors & service charge), and reduction in indent turnaround time, etc. This frequency synthesizer logs all the operations like PLL lock/unlock, frequency change. This synthesizer can be controlled by remote mode over Web browser interface.

Operating principle of LMX2592

The LMX2592 device is a 40-pin, low-noise, wideband RF PLL (Radio Frequency Phase Locked Loop) with integrated VCO that supports frequencies ranging from 20 MHz to 9.8 GHz. The voltage-controlled oscillator generates radio frequency from 3.55 to 7.1 GHz, and the output channel divider covers the lower frequency range (20 to 3550 MHz).

The VCO-doubler covers the upper-frequency range from 7.1 to 9.8 GHz. The device supports both Integer-N and Fractional-N modes. The device accepts input frequencies from 5 to 1400 MHz, combined with programmable low noise multiplier and frequency dividers, allowing adjustable frequency planning. The phase frequency detector (PFD) can take frequencies from 5 to 200 MHz. It also works in two extended modes, namely down and up. The down mode is from 0.25 to 5 MHz and up from 200 to 400 MHz (Wideband PLLatinum, 2015).

The phase-lock loop (PLL) consists of a Sigma-Delta modulator (1st to 4th order) for fractional N-divider values. The fractional denominator is programmable to 32-bit long, allowing a very fine resolution of frequency step. The device requires a typical single 3.3 V supply voltage and 250 mA (for a single 6-GHz, 0 dBm output) total current consumption. LMX2592 internal block diagram is described in Figure 1, which consists of a programmable input path divider, programmable N divider, sigma-delta modulator, channel divider, phase frequency detector, charge pump, etc. (Wideband PLLatinum, 2015).

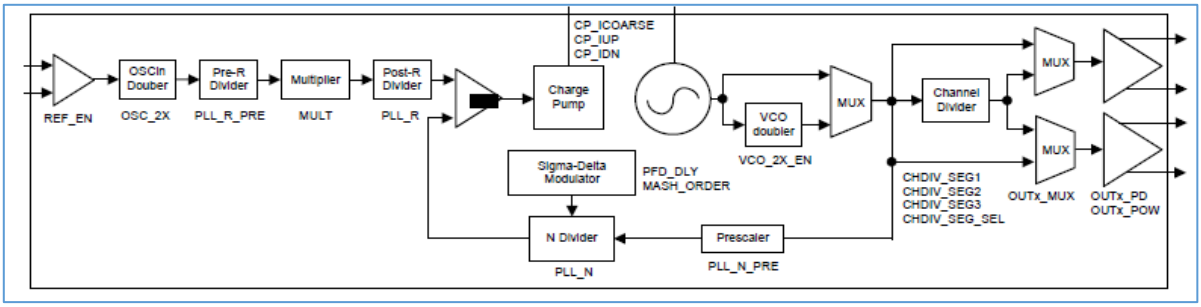


Figure 1. LMX2592 Functional Block Diagram
Source: Wideband PLLatinum, 2015

System Architecture & Device Selection

The phase noise of the VCO is degraded by a factor of $20log_{10}(N)$ compared to the reference source; N is the desired frequency ratio to the reference frequency (Chenakin, 2010). As per system architecture and specifications, the reference frequency is 100 MHz. A temperature-compensated crystal oscillator (TCXO-TX550) of 100 MHz made by VECTRON is selected as an onboard reference source. The phase noise specification is -130 dBc/Hz @ 1 kHz offset. If the onboard reference source fails, a 10 MHz symmetricom rubidium frequency standard is chosen as an external reference source. The default output of the rubidium frequency standard is a sine waveform, so LT1715-4 ns 150 MHz dual comparator circuit is used to convert the sine wave into a square waveform. The LT1715 is an ultra-fast dual comparator enhanced for low-voltage operation. It used distinct input and output power supplies to enable independent analog input ranges and output logic levels with no performance loss. The output from the rubidium source is connected to the non-inverting input of the above-discussed comparator, and the inverting input is grounded.

For the selection of internal and external reference sources, a 2:1 multiplexer circuit ADG3257 is used. The ADG3257 is a high-speed mux containing four 2:1 multiplexers. It provides low power dissipation, high impedance outputs, low on-resistance (2 Ω), and high switching speed. It allows the inputs to be connected to the outputs without adding propagation delay or generating additional ground bounce noise. A single pole double throw (SPDT) mechanical switch provides the multiplexer's select signal (Low or High).

The 3 dB bandwidth of the third order loop filter has a sharper cut-off than that of the second-order and the associated noise will be less. However, a third order loop will be only required if there is a continuous step change in frequency due to programming the N divider block, which is required only for frequency tracking applications. Here since Frequency Synthesis is the desired application, the steady state gain persisting for the duration of setting the required frequency is very less, second-order loop filter is sufficient for synthesis applications.

An RF amplifier from Analog Devices HMC392ALC4 (GaAs MMIC Low Noise Amplifier) is chosen to increase the signal strength at the output of VCO. The amplifier frequency range is from 3.5 to 8 GHz. It provides a typical gain of 17 dB, 3 dB maximum Noise Figure (NF), and minimum 16 dBm output power for 1 dB compression (P1dB). The supply voltage can range from 2 to 5.5 V (+3.3 V is used). The RF input (RFIN) and output (RFOUT) ports are DC-blocked and matched to 50 Ω for ease of use.

The Raspberry Pi 3B model is pocket sized System on Chip Computer with a 1.2 GHz Quad core ARM 64 bit processor (BCM2710A1) that runs Raspbian flavour of Linux Operating system.

Raspberry Pi 3B Board comes with 1GB RAM, Inbuilt modules for Wi-Fi, Bluetooth, Ethernet Stack, USB, HDMI , SPI,I2C, UART etc. It is also equipped with 28 General Purpose IO Pins of which 2 sets of SPI lines can be independently controlled with 2 and 3 peripherals respectively, in this case only SPI1 line is used to communicate to the SPI Slave peripheral, the Synthesizer Card.

SPI functions namely MISO (Master in Slave Out), MOSI (Master out Slave In), SClk (SPI Clock), CE (Chip Enable) is handled by GPIO pins 19,20,21,18 respectively.

The whole system architecture of the C-band frequency synthesizer with SPI interfacing from Raspberry Pi 3B to the Synthesizer is shown in Figure 2.

Principle of Operation

The frequency synthesizer working principle is that the reference signal f_{REF} passes through the input path. A frequency doubler and divider/multiplier (scaler) are the components of the input path. The reference signal of the phase frequency detector, also known as the

frequency of the phase frequency detector f_{PFD}, is the signal that is passed through the input path. After passing via the VCO doubler or direct, the VCO signal reaches the pre-scaler, N divider, and is transformed into f_N. The phase frequency detector (PFD), also known as the PLL phase detector, compares f_N and f_{PFD} and employs the charge pump to generate a correction current until the two signals are in phase (the PLL is locked).The correction current pulses from the charge pump output are converted into a DC control voltage and applied to the tuning voltage (Vtune) of the VCO by the use of external components (loop filter) (Wang, 2017).

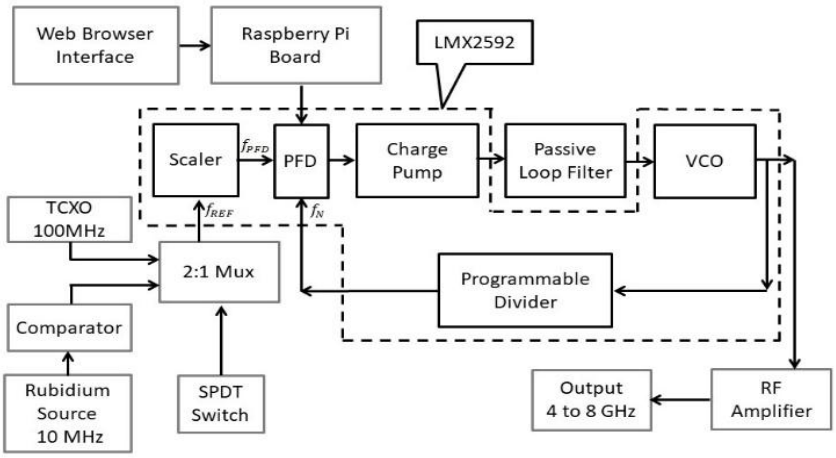


Figure 2. System Architecture of C-Band Frequency Synthesizer

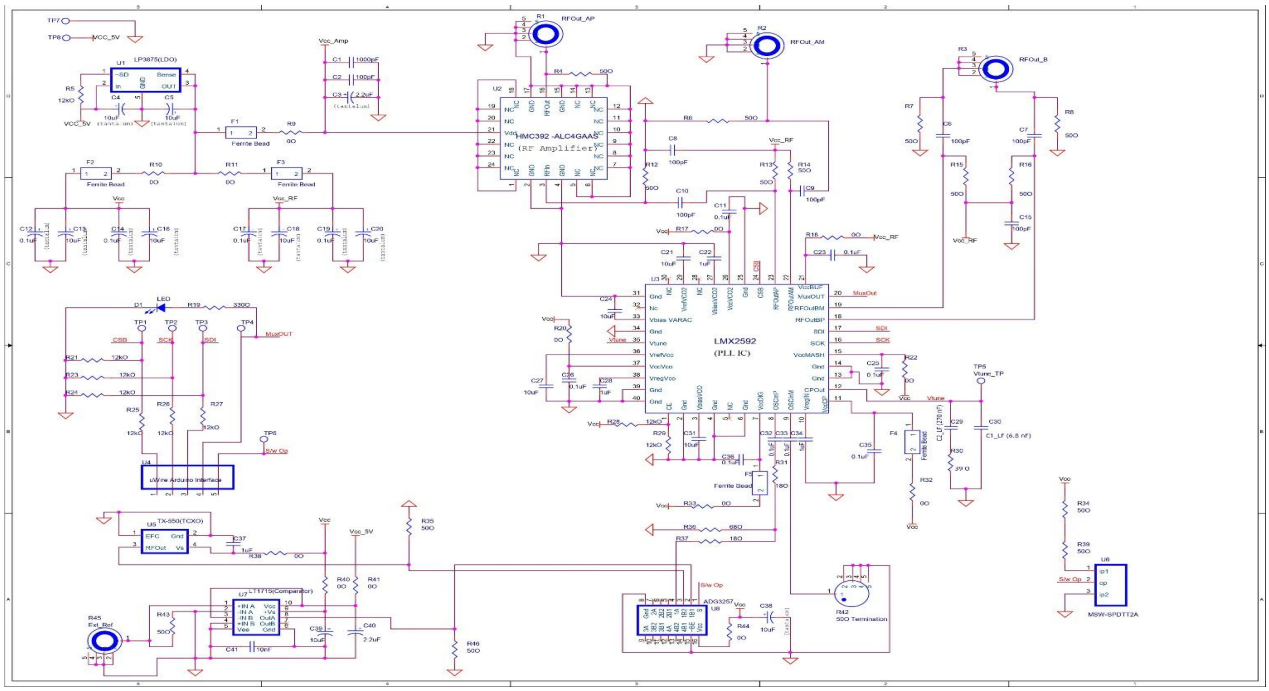


Figure 3. Circuit Diagram of C-Band Frequency Synthesizer

Layout Diagram

The circuit diagram of the C-band frequency synthesizer is given in Figure 3. The LMX2592 PLL IC, TCXO-TX550, ADG3257 multiplexer circuit, and RF amplifier HMC392ALC4 operate at 3.3 V. The Raspberry pi board and LT1715 comparator circuit operate at 5 V. To meet the frequency synthesizer's power requirement, one common power supply of 5 volts and LP3875 3.3 output voltage, a fast ultra-low-dropout linear regulator, is selected. An input and output tantalum capacitor of 10 μF is required to assure stability of the low drop-out regulator. The RFOut_AP (R1) is the main output port, and other unused ports should be terminated with 50-Ω termination.

Graphical User Interface (GUI) Development

The frequency synthesizer card based on LMX2592 is connected to the Serial Peripheral Interface (SPI) control pins of a Raspberry Pi 3B Board, which is intended to be the functional controller for the Synthesizer.

Raspberry Pi 3B acts as the SPI Master to enable the flow of control signals and data to & from the LMX2592. The register sets to be programmed onto LMX2592 for the desired synthesizer operation is calculated via a python based program after accepting relevant inputs from the user. A web-based Graphical User Interface application is developed and hosted on a web-server on the Raspberry Pi 3B itself and is designed to have low-latency, less overhead and high throughput, running on the secure http interface.

The Web Interface allows user to input the required fields such as Mode Selection, Frequency selection, Output section selection, RF enable etc. and the same is validated before getting processed for the register calculation program.

The features of such a GUI are:

Instantaneous control of synthesizer operation and changeover between modes, RF on/off feature, RF Output port control, network-wide availability of the application through simple web browser(no need of installation of additional software), continuous monitoring of lock status of the Synthesizer PLL, Error handling at user input level for all parameters etc.

Mode: Set Frequency Mode

In this mode, the user enters the frequency of his choice (within C-Band range) for synthesis and selects the output port (RF_A or RF_B or RF_AB).

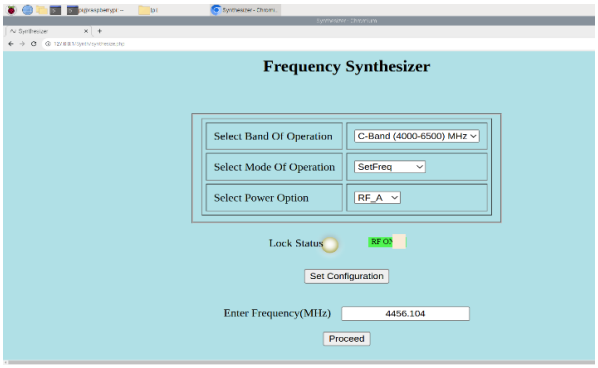


Figure 4. Set Frequency Mode

Based on user inputs and pressing the proceed button, the Raspberry Pi 3B gathers the user requirement and calculates registers accordingly, transmits the calculated register set to the LMX2592 over SPI. The PLL lock status is monitored through a readout register from LMX2592, which is displayed in real-time on the GUI.

RF On/Off button can be used to start/stop the RF power at output ports as per user requirement.

Mode: Continuous Sweep Mode

In this mode the user enters Start and Stop the frequencies of his choice (both must be within C-Band range) for continuous sweeping signal at an incremental step frequency and step delay of their choice. The provision of selecting the output port (RF_A or RF_B or RF_AB) is also provided.

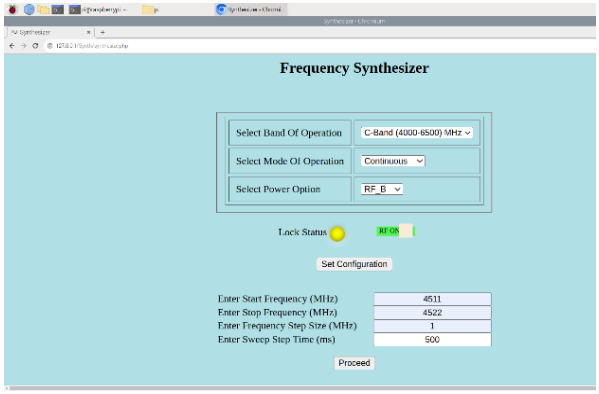


Figure 5. Continuous Sweep Mode

The Raspberry Pi 3B then continuously calculates the required frequency and corresponding register set, transmits it to the LMX2592 over SPI in a loop with incremental frequency change after the selected step delay.

The PLL lock status is also continuously monitored for each incremental frequency through a readout register from LMX2592 which is displayed in real-time on the GUI.

RF On/Off button can be used to momentarily stop the RF power at the output ports and then resume sweeping from the exact same frequency previously stopped at.

Mode: Single Sweep Mode

This mode is similar to continuous sweep mode except that the frequencies are swept over the user-defined range only once. Upon completing the full range sweep, last frequency in the range will persist at the selected output.

RF On/Off button can be used to pause the sweep momentarily and can be resumed any point of time to reach the stop frequency and persist at the same frequency.

In the realization process, the four General Purpose Input/output (GPIO) ports of Raspberry Pi 3B are connected with the four control pins of LMX2592. LMX2592 contains Chip Select Bar (CSB pin 24), Serial Clock (SCK pin 16), Serial Data in (SDI pin 17), and Serial Data Out/Lock Detect (SDO/LD pin 20) as serial interface control pins. The CSB pin is for SPI chip select bar or uWire latch enable (LE), and the SCK pin is for the serial clock input. The SDI pin is for serial data input, and the SDO/LD pin, which is for serial data output or lock detection, can output different internal signals through the configuration of internal registers.

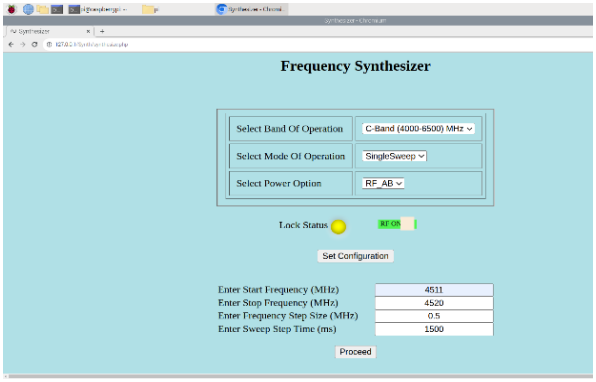


Figure 6. Single Sweep Mode

Table 2. Interface Details between Raspberry Pi 3B & LMX2592

Part	Interface from Raspberry Pi 3B to LMX2592			
Raspberry Pi 3B	GPIO Pin 18 CE0	GPIO Pin 21 SCK	GPIO Pin 20 MOSI	GPIO Pin 19 MISO
LMX2592	Pin 24 CSB	Pin 16 SCK	Pin 17 SDI	Pin 20 SDO/LD

The interface information for four control signals from the Raspberry Pi 3B to the LMX2592 IC is provided in Table 2. 24-bit shift registers are used for programming. An R/W bit (MSB), a 7-bit address field, and a 16-bit data field make up the shift register. In the R/W (bit 23), 0 indicates a write and 1 a read. The internal register address is decoded by the address field ADDRESS (bits 22–16). The data field DATA comprises the remaining 16 bits (bits15:0). Serial

data is sent into the shift register on the rising edge of the clock while CSB is low (data is programmed MSB first). Data is moved from the data field into the chosen register bank when the CSB signal is strong.

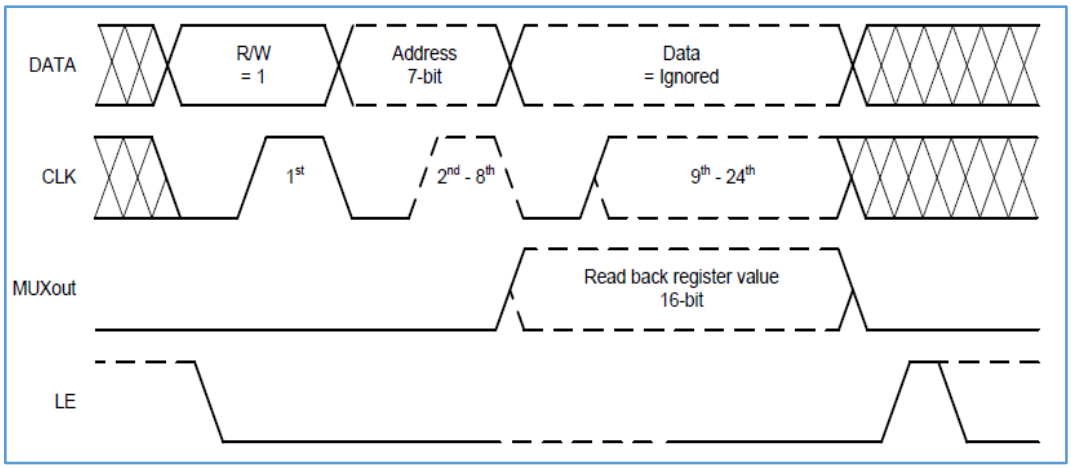


Figure 7. Register Read back Timing Diagram
Source: Wideband PLLatinum, 2015

Process Flow Chart Description

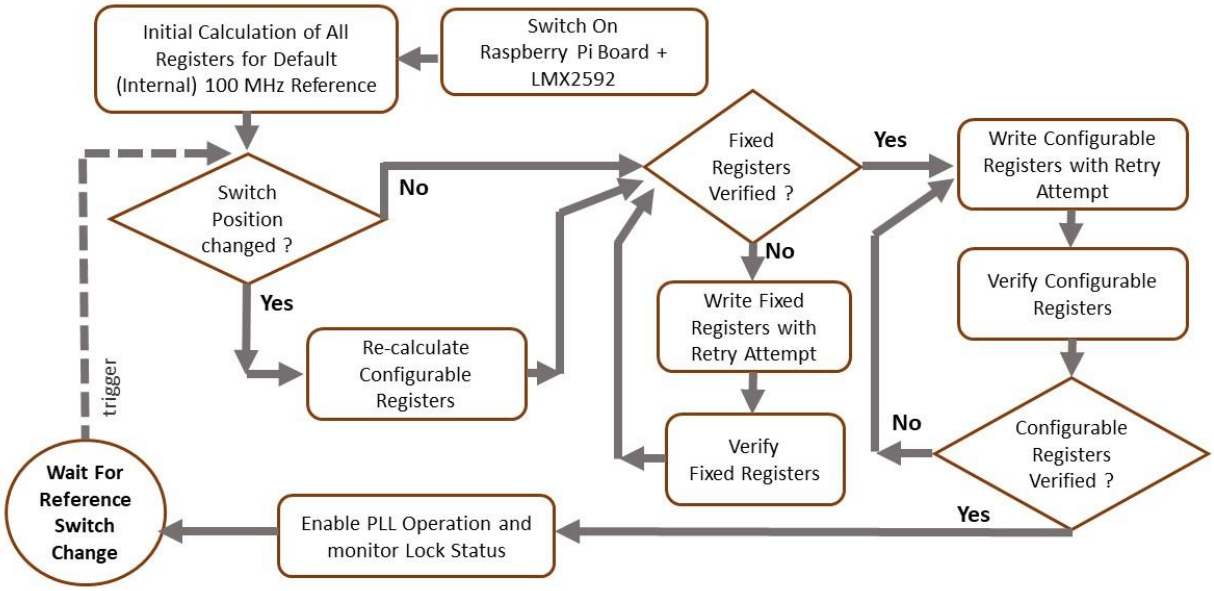


Figure 8. Process Flow Chart for Raspberry Pi 3B and LMX2592 Operation

As seen in the flow chart, the initial programming of the LMX2592 chip for a selected frequency happens immediately after the startup/power ON the board for the default 100 MHz reference source. The change in position of the SPDT switch is constantly monitored by an input pin of Raspberry Pi 3B, whose change indicates that there is a switch over to a different reference source from the current one. It triggers the recalculation of the corresponding re-configurable register settings required for LMX2592 for the updated reference

source. Raspberry Pi 3B attempts to write on the LMX2592 registers via the serial peripheral interface (SPI) after completion of registers calculation. Raspberry Pi 3B functions the role of SPI master and LMX2592 being the SPI slave. The reconfigured internal registers of LMX2592 are read back from the Muxout Pin after changing the appropriate register for the SPI read-back operation. The register read back is then verified with the calculated registers to ensure errorless transmission over SPI. The PLL operation is enabled by a register setting which is then monitored by the lock detect status. The Raspberry Pi 3B then switches to a low-power mode where it indefinitely waits for a change in the reference source through the SPDT switch position change. Hence there is no need to re-program the Raspberry Pi 3B with a requirement to change to a pre-defined reference source.

Loop Filter Parameters & Phase Noise Simulation And Control System Analysis

In this section, loop filter parameters & phase noise simulation results obtained from PLLatinum Sim software and control system analysis are discussed.

Loop Filter Parameters and Phase Noise Simulation

The spurious high-frequency signal is suppressed by a loop filter, which is a low-pass filter. Furthermore, it is crucial to the system's stability and phase noise components. Depending on their design, loop filters can be active or passive. The amplifier gain in the active filter introduces noise into the system. Hence the phase noise performance of the PLL created by the passive filter is better than that of the PLL with the active filter (Wang, 2017). This design's tuning voltage range of the LMX2592 is 0 to 2.5 V. The range of the output voltage at the loop filter output (V_{CTRL}) is sufficient for the range of the VCO tuning voltage. Therefore, the passive filter should be taken into account.

The software PLLatinum Sim PLL design can be helpful when designing the loop filter. Designing the loop filter requires a few key parameters. They are the charge pump current I_{CP}, loop bandwidth (BW), phase margin, VCO tuning sensitivity K_v, and filter design (active or passive; order). The closed-loop bandwidth of the loop is typically 1/10 or 1/20 of the reference frequency so that good phase noise performance can be achieved. It can be smaller (Wang, 2017) for better phase noise. The design of this external loop filter has a loop bandwidth of around 100 kHz. The loop phase margin must be in the system's stable zone to meet stability requirements. Here 72 degrees is selected except near the integer boundary (generally greater than 40 degrees is the best phase margin). These parameters are finalized based on software simulation results and same is verified during detailed test & evaluation. After optimization, the loop filter simulation parameters are C_1 = 6.8 nF, C_2 = 270 nF, and R_2 = 39 Ω. In real circuit design, we usually select similar capacitance and resistance values.

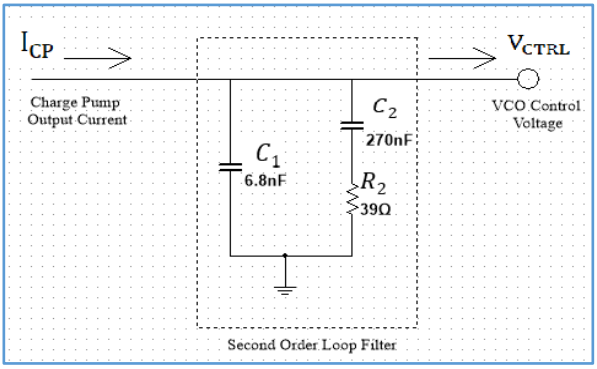


Figure 9. External Second-Order Passive Loop Filter

The impedance of the loop filter, which can be represented as follows (Banerjee, 2017), provides the transfer function for this second-order loop filter.

$$F(s) = \frac{V_{CTRL}(S)}{I_{CP}(S)} = \frac{1}{C_1 S} \,||\, \left(R_2 + \frac{1}{C_2 S}\right) \quad (1)$$

Where, V_{CTRL} is the voltage across the loop filter and I_{CP} is the current coming from the charge pump. After simplification of the above equation, we get

$$F(s) = \frac{R_2C_2S+1}{R_2C_1C_2S^2+S(C_1+C_2)} \quad (2)$$

$$F(s) = \frac{\tau_2 S+1}{S(\tau_1 S+1)(C_1+C_2)} \quad (3)$$

Where,

$$\tau_2 = R_2C_2 = 10.53 * 10^{-6}\ sec \quad (4)$$

$$\tau_1 = R_2C_2 * \frac{C_1}{(C_1+C_2)} = 0.259 * 10^{-6}\ sec \quad (5)$$

Substitute Equations (4) and (5) in equation (3), we get

$$F(s) = \frac{10.53*10^{-6}S+1}{S(0.259*10^{-6}S+1)*276.8*10^{-9}} \quad (6)$$

$$F(s) = \frac{38.04\ S+3.61*10^{6}}{S(0.259*10^{-6}S+1)} \quad (7)$$

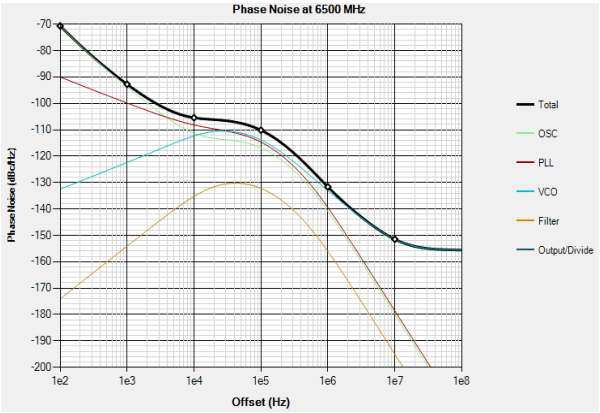


Figure 10. Simulation Result of Total Phase Noise @ 6500 MHz

The phase noise performance is simulated using the software, which can be seen in Figure 7. The total phase noise is -92.7dBc/Hz@1 kHz offset at 6500MHz.

Control System Analysis

The phase-locked loop is a closed-loop control system, and the stability of this will affect the performance of the frequency synthesizer. For this purpose, control system analysis is required, and stability can be defined based on the location of poles in the root locus plot. The other method of system stability can be obtained from Bode-Plot phase margin information.

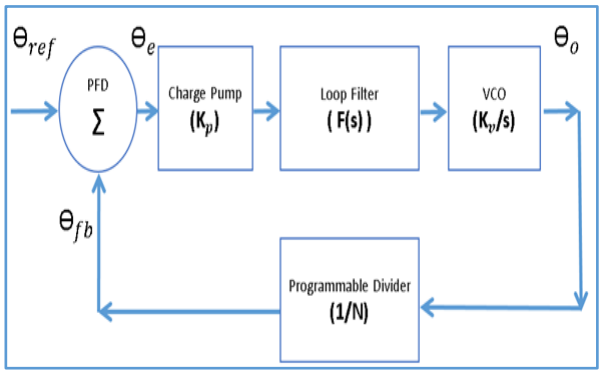


Figure 11. Simplified Control System Block

This section describes the transfer function of PLL, the Root Locus, and the Bode plot. The stability and phase margins are derived by analyzing the open and closed loop transfer functions. Root locus means closed loop poles path by varying the gain from zero to infinity. As the gain changes, the roots of the characteristic equation are indicated by root locus. A Bode plot is a graph showing the magnitude (in dB) or phase (in degrees) of the transfer function versus frequency.

Here,K_p = Charge pump gain = 19.375 mA (Fixed optimum gain for better phase noise & spur performance)

$F(s)$ = The second-order passive loop filter's transfer function

K_v= VCO gain, a function of the desired frequency

N = Programmable divider, set as per the desired frequency

The open-loop transfer function of the above control system, when derived in the proper form, yields the function:

$$G(s)H(s) = \frac{S(0.74)+(69.94*10^3)}{S^3(0.259*10^{-6})+S^2} * \frac{K_v}{N} \quad (8)$$

As shown in equation (8), the overall gain for the frequency of interest is varied with VCO gain to programmable divider ratio $\left(\frac{K_v}{N}\right)$.The PFD input frequency range of PLL IC LMX2592 is 5-200 MHz, and the VCO core frequency is 3550 to 7100 MHz. The root locus plot is obtained as a function of open-loop gain and plotted using below MATLAB command.

SYS_R= tf([0.74,69940],[0.259*10^-6,1,0,0]);

rlocus(SYS_R);

Case-1

PFD = 5 MHz & VCO Frequency =3550 MHz

For the above values of phase frequency detector (PFD) and voltage-controlled oscillator (VCO) frequency, the programmable divider (N) value is 710, and VCO gain (K_v) 24.25 MHz/V.

$$\frac{K_v}{N} = \frac{24.25}{710} = 0.03415 \frac{MHz}{V} = 3.415 * 10^4 \frac{Hz}{V} \quad (9)$$

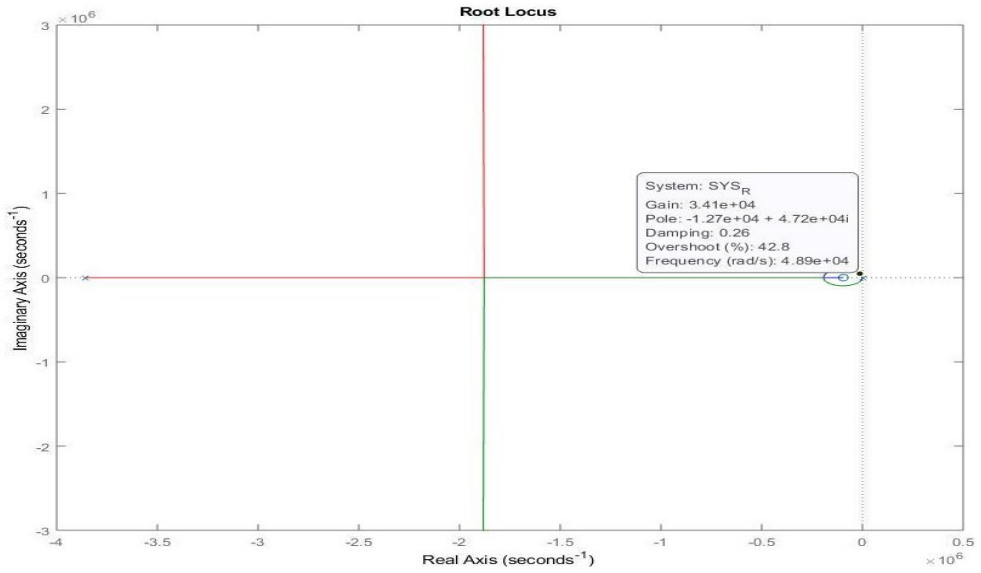


Figure 12. Root Locus for 5 MHz PFD

Case-2

PFD = 200 MHz & VCO Frequency =7100 MHz

For the above PFD and VCO frequency values, the programmable divider (N) value is 35.5, and the VCO gain is 57.05 MHz/V.

$$\frac{K_v}{N} = \frac{57.05}{35.5} = 1.6070 \frac{MHz}{V} = 1.6070 * 10^6 \frac{Hz}{V} \quad (10)$$

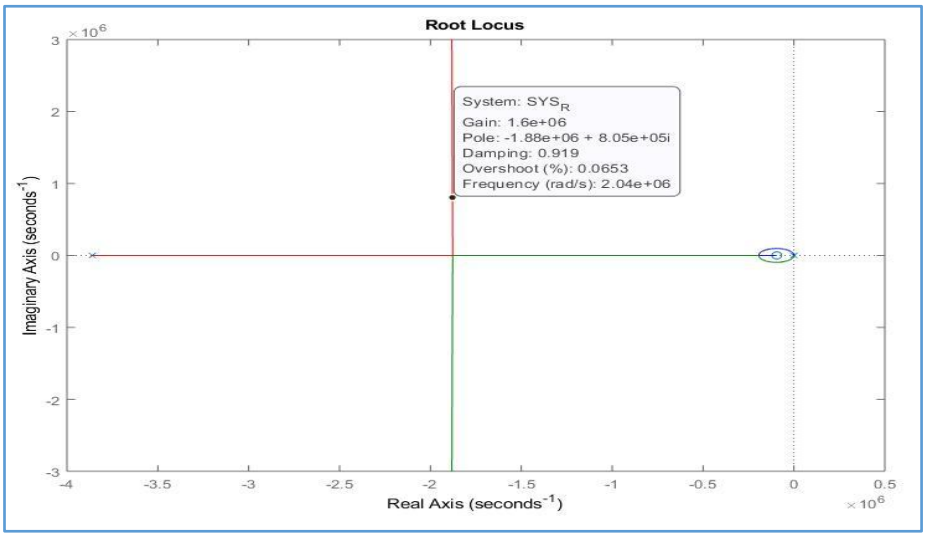


Figure 13. Root Locus for 200 MHz PFD

From the above root locus plot, it is clear that the system is stable (poles are located in the left half of the s-plane) for the given open loop gain parameters and hence the specified frequency range.

Phase Margin (PM)

From the root locus, the open-loop gain of 0.8875 MHz/V is chosen, and the transfer function now becomes

$$G(s)H(s) = \frac{S(0.74)+(69.94*10^3)}{S^3(0.259*10^{-6})+S^2} * (0.8875 * 10^6) \quad (11)$$

$$G(s)H(s) = \frac{S(0.656*10^6)+(62.07*10^9)}{S^3(0.259*10^{-6})+S^2} \quad (12)$$

The bode plot of the above transfer function is obtained using the MATLAB command below

SYS_B=tf([0.656*10^6,62.07*10^9], [0.259*10^-6,1,0,0]);bode(SYS_B);

The gain cross-over frequency can be obtained from the above plot as around 6.51 *10^5 rad/s, and the corresponding phase margin is around (-108 + 180) = 72 degrees.

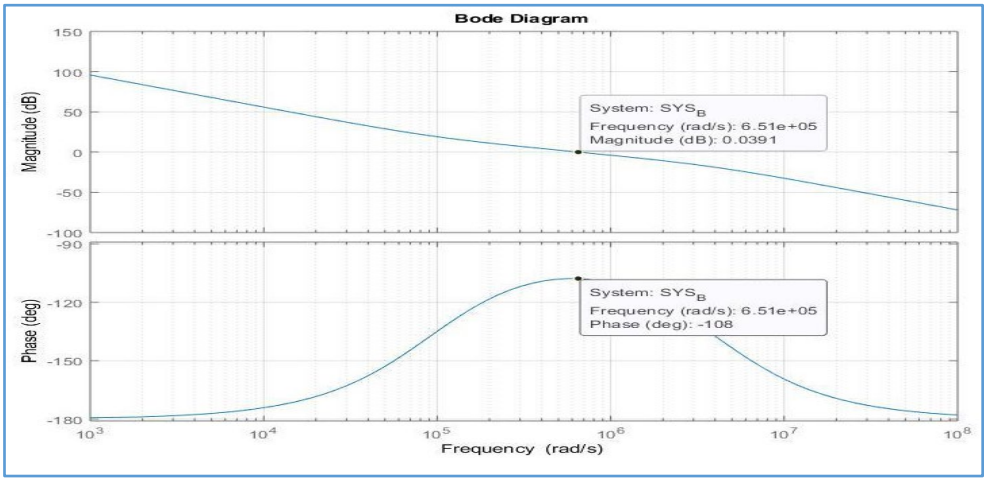


Figure 14. Bode Plot Obtained from MATLAB

Test And Evaluation (T&E) Results

The summary of the test and evaluation results of the C-band frequency synthesizer is mentioned below in Table 3. Detailed results for ten random frequencies in the frequency range of 4000-6500 MHz are given in Table 4.

Table 3. Summary of Test and Evaluation Results

S.No.	Parameters		Specifications	Results
1	Carrier Generation Verification		CW Carrier	CW Carrier
2	Carrier Generation at all available output ports		@ RF_OutAP, RF_OutAM, RF_OutB	Yes
3	Carrier Generation with Reference Source Changeover		Internal or External	Yes
4	Frequency Range (MHz)	**Test Condition** At Amplifier Output Port RF_OutAP with Internal Reference Source	4000-6500	4000-6500
5	Frequency Step Size (kHz)		0.5	0.5
6	Frequency Accuracy (kHz)		± 1	< ± 0.75
7	Power (dBm)		Minimum 10	> 10
8	Phase Noise (dBc/Hz) @ 1kHz		-90	<-90
9	Spurious (dBc)		<-50	<-50
10	Harmonics (dBc)		<-30	<-25
11	Carrier Stability (dB)		1 dB for 8 Hours	< 0.5 dB (8 hours)

Table 4. Test and Evaluation Results

S. No.	Case	Set (f_s) Frequency (Hz)	Measured (f_m) Frequency (Hz)	Delta ($f_m - f_s$) Frequency (Hz)	Power Out--put (dBm)	Phase Noise (dBc/Hz) @ 1kHz	Spurious (dBc)	Harmonics (dBc)
1	Normal	4000000000	3999999941	-59	15.10	-97.90	NIL	-30.01
2	Near Integer Boundary	4000124567	4000124704	137	15.10	-97.10	-61.43 @ -125 kHz	-29.88
3	Normal	4154213458	4154213327	-131	14.95	-95.29	NIL	-36.49
4	Near Integer Boundary	4999866768	4999866993	225	13.68	-95.73	-66.86 @ 133 kHz	-33.65
5	Near Integer Boundary	5199924156	5199924450	294	13.55	-93.68	-50.17 @ -76 kHz	-35.26
6	Normal	5289467856	5289467752	-104	13.38	-94.60	NIL	-30.50
7	Normal	5995597836	5995597606	-230	10.97	-93.61	NIL	-32.39
8	Near Integer Boundary	6100087352	6100087354	2	10.91	-93.62	-66.57 @ 87 kHz	-33.63
9	Normal	6218356871	6218356901	30	10.81	-93.28	NIL	-35.95
10	Normal	6500000000	6500000245	245	10.58	-92.71	NIL	-26.08*

T&E Results for C-Band Frequency Synthesizer being used as Local Oscillator (LO) inside Down-Converter unit corresponding to common range of C-Band Transmitter Frequencies.

Down converters, translate satellite C-Band Transmitter frequency to an Intermediate Frequency (IF) of 70 MHz. For this purpose, the above-designed C-Band frequency synthesizers are used as LO, whose frequency is given by,

$$LO\ Frequency = (Transmitter\ Frequency \pm 70)\ MHz \quad (13)$$

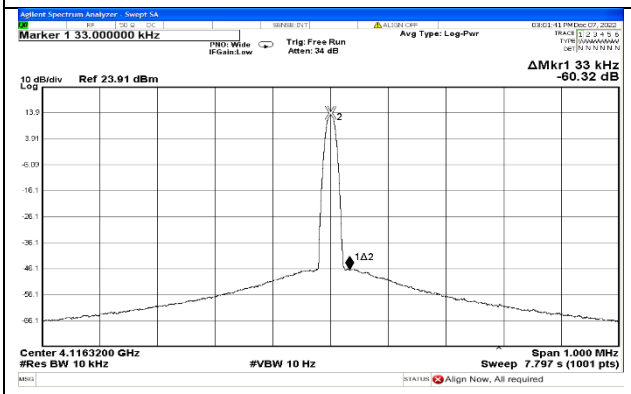
Table 5. Test & Evaluation Results @ D/C LO Frequencies for C-Band Transmitter Frequencies

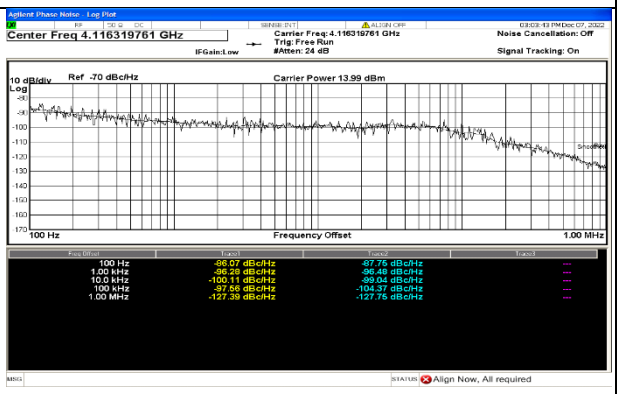
S. No.	Transmitter Frequency (Hz)	LO Frequency (Hz)	Measured Frequency (Hz)	Delta Frequency (Hz)	Power Output (dBm)	Phase Noise (dBc/Hz) @ 1kHz	Spurious (dBc)	Harmonics (dBc)
1	4186847000	4116847000	4116847102	102	15.06	-96.14	NIL	-32.53
2	4189344000	4119344000	4119344183	183	15.03	-96.11	NIL	-33.11
3	4186320000	4116320000	4116319761	-239	15.04	-96.48	NIL	-32.44
4	4191840000	4121840000	4121839798	-202	15.02	-96.42	NIL	-34.04
5	4187520000	4117520000	4117519977	-23	15.03	-97.08	NIL	-32.62
6	4197504000	4127504000	4127503852	-148	15.00	-96.56	NIL	-35.87
7	4188768000	4118768000	4118768005	5	15.02	-96.49	NIL	-32.84
8	4196928000	4126928000	4126928176	176	15.00	-96.63	NIL	-35.71
9	4195776000	4125776000	4125775840	-160	15.00	-96.37	NIL	-35.49
10	4199280000	4129280000	4129279731	-269	14.99	-95.56	NIL	-36.44

Note: Harmonics performance will be improved by adding Band Pass Filter at the output of the amplifier.

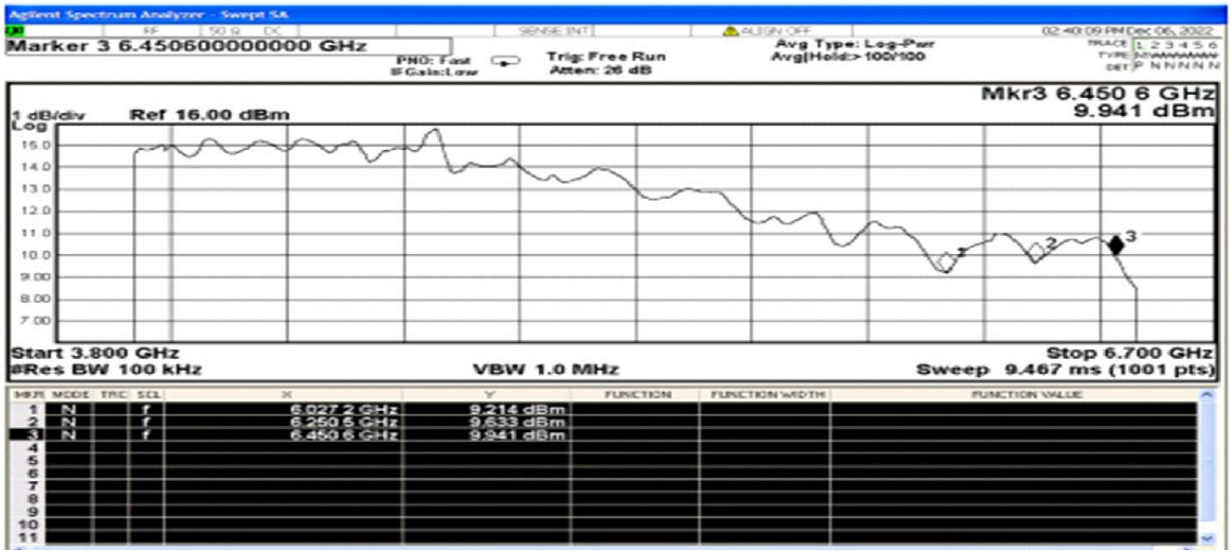
Table 6. Plots of the Basic Performance Parameters of the Synthesizer

Spurious & Phase Noise Measurement for LO Frequency @ 4116.320 MHz

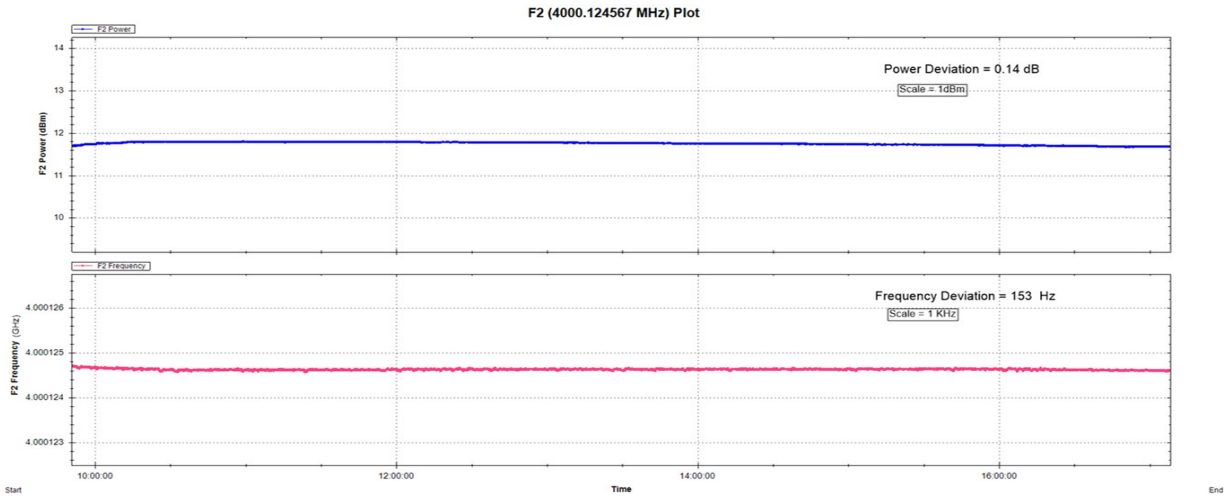




Frequency Response at Single Ended Amplifier Output Port (RFOut_AP) with cable loss 0.9 dB above 6 GHz



Power and Frequency Stability (8 Hrs) @ 4000.124567 MHz



Conclusion and Discussion

The frequency synthesizer PCB card has four layers: the **top, ground, power,** and **bottom layer** and is realized using base material RO4350 (RT Duroid) Er 3.66, High Tg FR4. PCB card design is based on a single-ended microstrip structure, and trace parameters like width, height, spacing, etc., are selected for achieving a controlled impedance of approximately 50 Ω. In below Figure 12, component marking on PCB top layer is given.

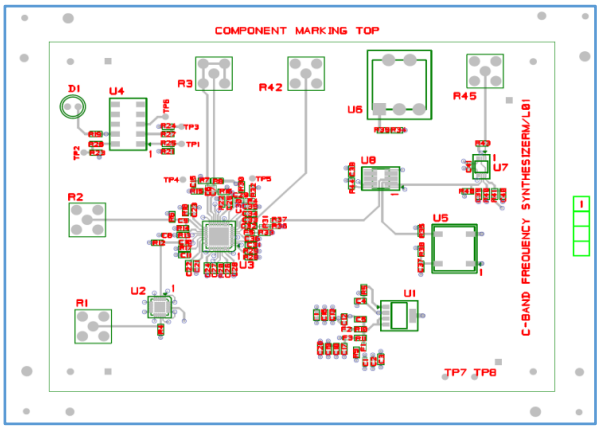


Figure 15. Components Marking on PCB Top Layer

The PLL-based fractional frequency synthesizer in C-band developed using PLL IC LMX2592 has been presented in this paper. On the RT-Duroid RO4350 substrate, a Low Phase Noise carrier generator is designed and implemented utilizing a PLL synthesizer. This implemented model shows frequency accuracy of less than ±1 kHz and the phase noise better than -90 dBc/Hz @ 1 kHz offset. The carrier stability results at different frequencies are within 0.5 dB for 8 hours. The bandpass filter will be added to the amplifier's output to improve harmonics performance.

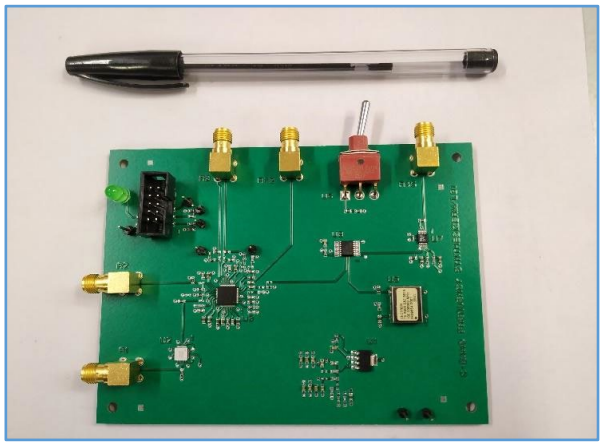


Figure 16. Frequency Synthesizer PCB Card on RO4350 substrate

Table 7: Analysis of Spurious & Phase Noise Performance

Case	Spurious Offset (kHz)	PFD (MHz)	CP Gain (mA)	Over 4000-6500 MHz		Output Frequency (MHz)	Spurious Level (dBc)	Phase Noise (dBc/Hz) @ 10 kHz Offset
				Loop BW (kHz)	Phase Margin (Degree)			
Normal	Any Offset	100	19.375	103.7 to 94.1	72.1 to 72.2	4000	NIL	-102.11
Near Integer Boundary	1000 > Offset ≥ 130	100	19.375	103.7 to 94.1	72.1 to 72.2	4000.131	-35.4	-100.34
Near Integer Boundary	1000 > Offset ≥ 130	66.66	19.375	70.5 to 64.1	71.4 to 70.8	4000.131	-44.47	-98.37
Near Integer Boundary	1000 > Offset ≥ 130	66.66	5	21.8 to 20.2	53.2 to 51.3	4000.131	-54.96	-98.79
Near Integer Boundary	130 > Offset ≥ 100	66.66	3.75	17.7 to 16.5	47.8 to 46	4000.100	-54.24	-96.32
Near Integer Boundary	100>Offset≥80	66.66	3.438	16.6 to 15.5	46.2 to 44.3	4000.080	-52.76	-96.08
Near Integer Boundary	80>Offset≥65	66.66	2.5	13.4 to 12.6	40.4 to 38.7	4000.065	-53.00	-93.02

As per Table 5, the C-Band frequency synthesizer's performance meets all required specifications given in Table 1. Hence, it can be used as a local oscillator for the in-house development of up/down converter equipment.

In Table 7, loop bandwidth and phase margin are computed using **PLLatinum Sim** software for different PFD and charge pump gain values over the frequency synthesizer operating range. As per the analysis, spurious performance can be improved for near integer boundary conditions by reducing phase frequency detector (PFD) frequency and charge pump gain resulting in lower loop bandwidth and phase margin. The trade-off between spurious and phase noise here is that as loop bandwidth & phase margin reduce, spurious performance is improved, and phase noise performance at 10 kHz offset is poorer.

Acknowledgment

The authors are thankful to the Deputy Director, ICA, Shri Ramanagouda V Nadagouda, and Group Director, SCG, Shri. Krishnan.V for their constant encouragement and motivation for writing this paper.

Disclosure Statement

The authors reported no potential conflict of interest.

References

Chenakin, A. (2010). Low Phase Noise PLL Synthesizer. US Patent No. 7,701,299.

Crosson, W., Limaye, A. & Laymon, C. (2010). Impacts of Spatial Scaling Errors on Soil Moisture Retrieval Accuracy at L-Band. *IEEE Journal of Selected Topics in Applied Earth Observations and Remote Sensing, 3*, 67-80. https://doi.org/10.1109/JSTARS.2010.2041636

Gao, W., & Gao, X. (2010). Design of PLL frequency synthesizer based on the fourth-order active filter. *2010 International Symposium on Signals, Systems and Electronics, 2*, 1-3. https://doi.org/10.1109/ISSSE.2010.5606981

Kroupa, F. (2003). *Phase Lock Loops and Frequency Synthesis*, NY, John Wiley.

Ma, M., Wang, H. & Li, Z. (2012). Phase-locked frequency source in the S-band transceiver system. In *Communication Technology (ICCT), 2012 IEEE 14th International Conference on, Chengdu*, pp. 924-928. https://doi.org/10.1109/ICCT.2012.6511330

Pandit, V.K., Deepak, V.I. & Basu, S. (2014). Design and Implementation of Pll Frequency Synthesizer using PE3336 IC for IRS Applications. *Electrical and Electronics Engineering: An International Journal, 3,* 31-41. https://doi.org/10.14810/ELELIJ.2014.3303

Skolnik, M.I. (2002). Role of radar in microwaves. *IEEE Transactions on Microwave Theory and Techniques, 50*, 625-632. https://doi.org/10.1109/22.989947

Tsai, J.-H., Hsu, C.-Y. & Chao, C.-H. (2015). An X-band 9.75/10.6 GHz low-power phase-locked loop using 0.18-µm CMOS technology. In *2015 10th European Microwave Integrated Circuits Conference (EuMIC),* pp. 238-241. https://doi.org/10.1109/EuMIC.2015.7345113

Wang, H. (2017). Design and Implementation of Ku-band Frequency Synthesizer. In *IEEE International Conference on Integrated Circuits and Microsystems.*

Wideband PLLatinum. (2015). LMX2592 High Performance, Wideband PLLatinum™ RF Synthesizer With Integrated VCOSNAS646F.

Yang, Y., Cai, J., & Lianfu, L. (2011). A Frequency Synthesis Structure in Radar Target Simulation System with High Agility and Resolution Performance. *Microwave Conference Proceedings (CJMW)*, pp. 1-4.

Yu, S., Xu, J., & Shen, Z. (2012). X-band frequency synthesizer with high frequency resolution. *2012 4th International High Speed Intelligent Communication Forum*, pp. 1-3. https://doi.org/10.1109/HSIC.2012.6212962

Zhu, Y., & Wang, L. (2015). Design and Implementation of Nanosecond Pulse Generator based on Reconfiguration PLL in FPGA. In *2015 International Conference on, Electronic Science and Automation Control Atlantis Press.* https://doi.org/10.2991/ESAC-15.2015.78