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A Computer Controlled Phase and Magnitude Self-Calibration Methodology for Phased Array Antennas

Zain Shafiq[1] [2], Dimitris E. Anagnostou [2] (Senior Member, IEEE), Symon K. Podilchak [1] [2] (Senior Member, IEEE)

[1]The Institute for Imaging, Data, and Communications (IDCOM), The University of Edinburgh, Edinburgh, EH9 3JW UK
[2]Institute of Sensors Signals and Systems (ISSS), School of Engineering and Physical Sciences, Edinburgh, EH14 4AS UK

CORRESPONDING AUTHOR: Symon K. Podilchak (e-mail: mailto:s.podilchak@ed.ac.uk).

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ABSTRACT A circuit-based calibration system is presented for active phased arrays. In particular, to achieve the desired (and corrected) consecutive phase differences and relative magnitudes between RF channels, a computer controlled circuit system was developed for dynamic adjustment. The proof-of-concept demonstrator uses a phase sensor, phase shifters (PSs), and variable gain amplifiers, along with other active hardware, to realize a self-calibrating circuit system which achieves the required magnitude and phase for each array element. In addition, measured magnitude and phase imbalances are less than 0.10 dB and 3°, respectively. The computer-controlled feed network is then used to demonstrate that the system can automatically calibrate an active antenna array for various beam steering examples. Also, the S-band feed system can self-calibrate due to any monitored magnitude and phase drifts due to temperature changes and practical component ageing, or, other general channel offsets. This can be considered advantageous and simpler when compared to more established approaches which characterize the coupling between elements or the response of the entire array in the near- or far-field for example.

INDEX TERMS Active feed circuit, calibration, beam-steering, phased array.

I. Introduction

PHASED array antennas are used to electronically steer the far-field beam pattern to a desired direction. This is typically achieved using phase shifters (PSs) at each element. Moreover, an active electronically scanned array (AESA) is a type of phased antenna array commonly employed for radar, usually controlled by a computer or some digital hardware to govern the angular steering direction.

The accuracy and steering capability of the array is linked to the quality of the PSs which are needed to generate the required consecutive phase differences for each RF channel. Often if a lower resolution PS is used (e.g. a 5-bit phase shifter, see Table 1) to save on system costs, the steering ability will be limited and gaps or holes will develop for the steered pattern [1]. More specifically, a hole is an angle which the array system cannot steer to. As further discussed in [2], a 4-bit (or higher) PS can be considered at each antenna element to mitigate such beam steering challenges. However, with improved PS quality (see Table 1), costs can increase to implement the N-element array.

Calibration of phased arrays is also needed to ensure that the beam can be positioned to the correct angle when required. Basically to steer the main beam, a consecutive phase shift is applied at each antenna element and often with a controlled amplitude level for the RF channels [2]. Unwanted offsets in magnitude and phase, or deltas (δ_1, δ_2, δ_3, ..., δ_N, see Figs. 1 to 4) can cause the overall beam pattern to diverge, offsetting the beam maximum from its desired position and causing sidelobe levels (SLLs) to increase. The depth of the pattern nulls can also be affected which is important for sum and difference patterns (i.e. monopulse setups) and clutter mitigation. For these reasons, phase and magnitude errors, reflection mismatches, and system drifts need to be corrected to enable accurate array operation [3]. These offsets can originate at the element level due to temperature variations as well as the supporting RF

circuit channels feeding these elements. Basically any active electronics; i.e. for instance, the amplifiers, analog-to-digital converters, and PSs.

As outlined in [4] and [5], the importance of addressing these phase imbalances that can develop for arrays by the appropriate calibrations was discussed. These unwanted δ phase errors can be introduced from both passive or active components (see Fig. 1). For example, a power divider can add a set magnitude and phase offset between RF channels which may need to be calibrated. Errors can also be introduced from element mutual coupling as well as other non-idealities introduced by the PSs and amplifiers. For instance, a practical PS can introduce the required consecutive phase difference for the array when steering the far-field beam, however, the accuracy of the PS can also be problematic in practice (see Table 1) requiring some type of calibration or correction.

To overcome these practical challenges, several different approaches exist for array calibrations and these can generally be categorised into on-board calibration and on-ground calibration [6]. On-board calibration is more desirable as lab equipment such as an anechoic chamber is not required. The full calibration can be done on the system when it is in the intended environment. The calibration can also be completed outside the lab for example, if the array system is contained within vehicles such as cars, boats, or aircraft. In addition, a number of built-in-self-test CMOS circuits have developed as in [7], [8], however, phase errors of 3° or more are typical for these types of integrated circuit transceiver chipsets.

When considering the total active phased array antenna system; i.e. the RF chains and the individual antenna elements, the most basic form of calibration is the scanning probes method as presented in [9]. This specific method uses a probe which mechanically moves in-front of each radiating element, where the probe measures the amplitude and phase of each element individually. This method can achieve a high accuracy calibration but should be performed in an anechoic chamber, and also requires high precision equipment such as a near-field scanner and vector network analyser (VNA). The probe must also be calibrated to ensure it moves to the centre of the element under test. As described in [6], this method is generally thought to be time consuming and complex.

In [5] and [10], the mutual coupling method was used to perform array calibrations. This method takes advantage of the mutual coupling between elements and uses said coupling to measure the phase and amplitude differences among elements by transmitting from an element and then receiving from another. This method is very practical, and requires no prior in factory calibration. However for the method to be applicable, the array must meet several requirements which are as follows: (1) antenna elements must simultaneously transit and receive, (2) there needs to be control of the power at each element, (3) the array should be symmetric, and (4), coupling levels should be between -15 and -25 dB. These requirements can often make the array difficult to implement in practice as the array needs to be designed around this calibration technique.

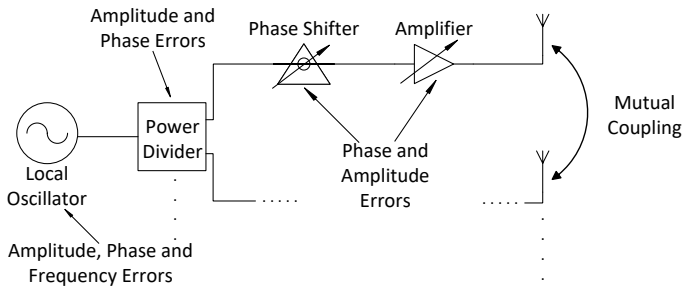

FIGURE 1. Diagram of an N-element phased array antenna system indicating points where phase drift errors or RF channel deltas (δ) can be introduced.

Another approach for array calibrations is the rotating element electric field vector (REV) method [11]. It uses power measurements to determine the magnitude of the electric field, and does not require any direct phase measurements. However, the insertion phase of the PS at each element is varied from 0° to 360°, and from this, the complex electric field can be determined. Due to its simplicity this method is common, however, it can result in large data sets making calibration time consuming and laborious [11]. This method also assumes that the PSs are ideal which isn't the case in practice.

These aforementioned calibration techniques all have merits and limitations. However, the proposed calibration strategy newly developed in this paper, can be said to be an advancement of the calibration lines method [15] (which uses external transmission lines directly connected to each antenna element within the array, for amplitude and phase sampling and post-processing corrections [15]). More specifically, our proposed antenna feed system can be considered an integrated version of the calibration lines method, in that, the required transmission lines and calibration electronics are build directly into the antenna system itself. This is made possible by implementing a computer controlled feed system with an RF comparator and other supporting hardware.

To our best knowledge this is a new calibration approach, and as further reported in the paper, is able to perform high accuracy on-board phase corrections in an automated way whilst outperforming other commercially available digital PSs in terms of cost and possible phase errors (see Table 1). The proposed active antenna feed system also offers

TABLE 1. Commercial Phase Shifters Compared to the Proposed System

Commercial Component	Phase Resolution	Phase Error	Auto Calibration	Normalized Cost
5-bit PS [12]	11.25°	±8°	No	2 units
6-bit PS [13]	5.625°	±3°	No	1.5 units
8-bit PS [14]	1.4°	±1°	No	21 units
Proposed System	**1.5°**	**±1.4°**	**Yes**	**1 unit**

improved performance when compared to more conventional techniques such as the scanning probes and the mutual coupling methods as no pilot signals for calibration (or specific calibration signals) are required. These features can simplify the overall element corrections as the calibration functionality is built directly into the RF channels feeding the array elements themselves. This new approach is computer controlled and will be fully described in the paper. In addition, the architecture is made completely automatic by the designed circuit system.

The main difference with our proposed methodology is that a conventional vector network analyzer (VNA) and near-field or far-field (FF) range, are not mandatory for full array characterization and continued performance assessments of the calibration, like in more traditional in-factory or initial antenna system validation. These traditional testing and calibration approaches (as described above) can be costly and time consuming, and when performing standard array drift assessments on the beam pattern, gain, and SLL, for example. However, these conventional approaches can always be used for validation of the proposed antenna system (once self-calibrated), and this will be further studied in the paper for the demonstrator prototype.

As will be shown also, the proposed self-calibration method is proven to be highly accurate (see Table 1), when considering the calibration and correction of the RF channels. Basically, after full assessment of the employed RF components, the adopted system parts can be easily integrated into a phased array system for real-time characterization as well as continued correction of the relative magnitude and phase differences between the RF channels and thus removing any unwanted offsets at the antenna element-levels. The proposed methodology is also low-cost and is easily adaptable to varied temperature conditions which can cause system drift, and, can be up-scaled to larger arrays. An additional novel feature of the proposed system is the added feedback loop which can actively monitor the magnitude and phase of the RF system and adjust the channels for corrections as needed.

Given these design capabilities and to show proof-of-concept, a self- or auto-calibration circuit system is proposed and experimentally verified in this paper. In addition, the proof-of-concept system demonstrator uses off-the-shelf RF hardware which is automatically controlled and computer programmed, and this can provide self-calibration of antenna systems. Simple look-up tables (LUTs) are populated and reported for component characterization which can be implemented in the factory, in the lab, or on-board (i.e. on-ground, or in the field) as desired. In addition, the developed LUTs can be used to apply the needed corrections ensuring minimal system drift, and, can be easily re-generated should the element feeding or the RF channel electronics change or need updating. Basically the computer controlled system can continuously check for any system drifts and has the capability to automatically re-calibrate or generate LUTs, and then, correct the magnitude and phase for each channel within the array.

This paper is organized as follows. Section II describes some more background theory on the calibration of AESAs and illustrates how phase and magnitude errors can spoil the beam pattern. Section III introduces the proposed self-calibrating circuit system which uses a phase comparator providing readings to the computer controlled system in real-time. As further described in the paper, interpolation and the aforementioned LUTs overcome the practical challenges of the low-cost comparator and other active hardware, mainly by, embedded data processing in MATLAB. Then bench top measurements are taken from the simple 2×1 demonstrator and applied to phased array examples to initially show how the unwanted δ_N phase errors introduced, and controlled for each RF channel, can be corrected. Feeding circuit results are then used to model array calibrations. As it will be further shown in the paper, the developed methodology is successful at correcting the consecutive phase difference at each element. In effect, the δ_N introduced within each RF channel is removed by the self-calibrating active feed circuit system for AESAs.

Section IV reports on the extended development of a 4 channel system which corrects both magnitude and phase errors. Basically, the S-band circuit system is able to self-calibrate for insertion losses introduced by the PS using a variable gain amplifier (VGA), as well as, compensate for any additional and unwanted phase shifts introduced by the VGAs. Further bench-top results, which are automatically corrected, are documented and show how the required magnitude and relative channel phases can be made user selective. Section V reports on a 4×1 system testing in the FF using a patch array for further proof-of-concept and verification. As further reported in the paper, the developed circuit system is able to accurately steer the beam as well as apply amplitude tapering at the element level. The paper concludes with a summary and important appendices are included which discuss the developed LUTs and full characterization of the employed VGAs and PSs. These details are important to ensure accuracy for the proposed self-calibrating active antenna system.

II. Phased Arrays and Calibration Considerations

For a phased array antenna system, it is imperative to ensure that the applied phase is correct. The progressive differences can be calculated using $2\pi d\sin(\theta_0)/\lambda$ [2], where d is the element spacing, λ is the wavelength and θ_0 is the steering direction. However, achieving this phase shift in practice is difficult and expensive based on the number of elements. At microwave frequencies, PSs can be designed using: ferromagnetic materials, semiconductors or MEMS Devices [16]. Each method will have its own advantages and disadvantages. The most important factors for PSs is the root mean-square (RMS) phase error. This is basically linked to the percentage errors introduced for the studied arrays

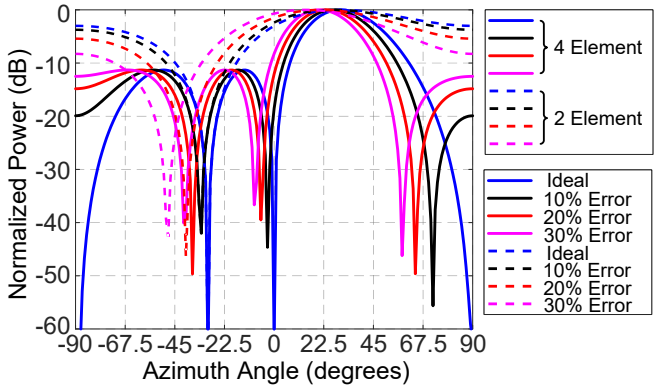

FIGURE 2. Normalized array factor (AF) plots for a 2×1 and 4×1 array showing how a percentage error in phase can alter the far-field (FF) pattern, mainly by perturbing the phase from ideal (by θ_0 variation or δ for each element).

(see Fig. 2), but expanded when considering the statistical relationship for many devices. Generally speaking, the lower the RMS phase error, the higher the cost, therefore making it important to understand the effect of these errors [17] which can cause increased sidelobes and unwanted steering offsets for example.

A. Phase Error Affects on the Array Factor

The array factor (AF) for a linear phased array is as follows [2]:

$$AF = \sum_{n=1}^{N} A_n e^{j(n-1)\psi}, \tag{1}$$

where A_n is the amplitude assigned to each of the n elements, N is the number of elements, and ψ is the progressive phase difference which controls the angular direction of the main beam. To illustrate the need for array calibrations, numerical calculations were completed in MATLAB considering a two- and four-element linear array with uniform excitation; i.e. a uniform linear array (ULA) defining a common magnitude (with $A_n = 1$). Calculations of the array factor with random phase errors were also carried out using

$$AF = \sum_{n=1}^{N} e^{j((n-1)\psi)(1-\delta_n)}. \tag{2}$$

Here the phase error δ_n is introduced for each element and represented by a random number with an upper bound, and this is defined as a percentage from the ideal. As shown in Fig. 2, the array is steered to 30° and results are further detailed in Table 2.

These findings show that when uniform phase errors are applied to each $\lambda/2$-spaced element, which are representative of the δ_n introduced within the individual RF channels (as outlined in Fig. 1), challenges can be observed in the far-field (FF) array pattern. It can also be observed from Table 2 that as the level of error increases, the position of the beam maximum moves as well as the position of the nulls. For most applications this level of error and drift is undesirable and can degrade system performance. It should be mentioned that the 0% error case, can be considered an ideal scenario where ideal phase shift values were applied and where δ_N = 0. Errors can be common if active equipment is not properly calibrated, for example, therefore the resulting phases at each element can drift by a certain percentage as illustrated here.

TABLE 2. Results for a 4×1 Array Showing how Different δ Phase Errors can Affect the Pattern. The Array was Steered to 30°

δ Error Weight	Beam Max Position	First Null Position	Second Null Position
0%	30°	0°	-30°
10%	27°	-3°	-33°
20%	24°	-6°	-37°
30%	21°	-9°	-41°

From Fig. 2 and Table 2 it is evident that phase offsets can significantly affect the FF beam pattern. If we consider the 20% error case (i.e. the red curve), it can be observed that the beam position is offset by 6° from the desired maximum of 30°. The depths of the first and second nulls are also raised and offset. The main beam offset in practice will cause uncertainty in any antenna related system. For example, for radar target detection, accuracy can decrease for this case and when considering larger arrays. It is also important for nulls to stay in the desired position for radar antenna arrays. This is because nulls are typically adjusted and at the required depths to support the mitigation of ground clutter [18]. This reduces the illumination of foreign objects which ultimately reduces return interference. For all these reasons it is important to maintain deep nulls [19] and mitigate any unwanted effects by the necessary calibrations.

B. Magnitude and Phase Error Challenges

To further investigate the effects of both random phase and magnitude errors for larger scale antenna systems, the case of a 128×1 array was also studied. Results are shown in Figs. 3 and 4, where the same approach to introduce a random error (and maximized by a certain percentage from the ideal) was considered as in Fig. 2 for the 2×1 and 4×1 arrays, except, with a magnitude error also introduced for the array elements:

$$AF = \sum_{n=1}^{N} (1-\delta_m) e^{j((n-1)\psi)(1-\delta_n)} \tag{3}$$

where δ_m and δ_n are introduced to model random errors altering the magnitude and phase from the ideal, respectively.

Figure 3 shows the array steered to -30°. It can be seen that the side lobes increase significantly as the error increases. For example, for the 30% error case, the SLL increases to about -15 dB when compared to the main beam maximum. In addition, the beam is slightly offset but this is difficult to observe in Fig. 3 as the half-power beamwidth (HPBW) of the 128×1 array is about 1.5°. Basically, the peak of the pattern offset is minor simply due to the HPBW of the large array. Regardless, this offset can still have a significant impact on the array performance, as typically larger scale AESAs have stricter steering accuracy requirements. Figure 4 shows the same array, however, this time it is steered to -60°. Again it can be seen that the SLLs increase with

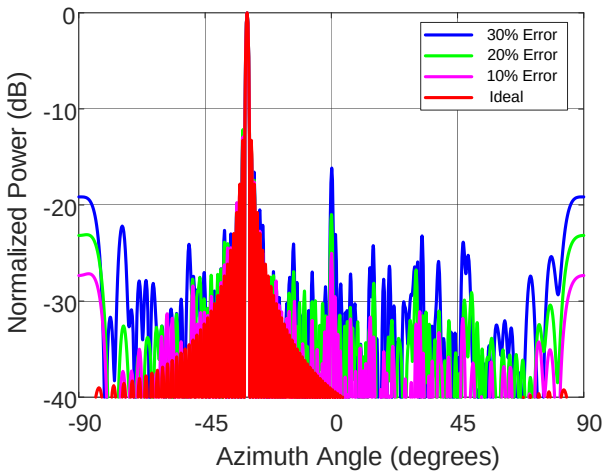

FIGURE 3. Normalized AF for a 128×1 array showing how percentage errors can alter the FF pattern, mainly by perturbing the magnitude and phase of each element from the ideal. With increasing error the the SLLs increase, but the beam position is also slightly offset, this is difficult to observe since the HPBW is about 1.5°. In this case the AF is steered to -30°.

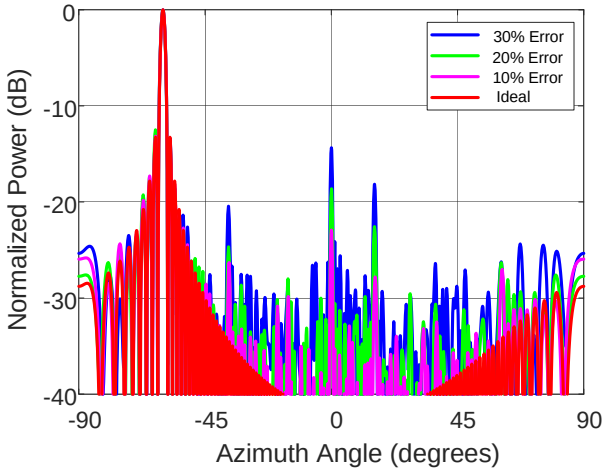

FIGURE 4. Normalized AF for a 128×1 array showing how magnitude and phase errors can alter the FF pattern. In this case the AF is steered to -60°.

added error. These results show that for smaller scale arrays that magnitude errors can alter the beam position, and that both magnitude and phase errors can be problematic for the required beam position and maintaining best possible SLLs for larger arrays.

It should also be mentioned that high or increased sidelobes are problematic. This is because power is wasted in the creation of these sidelobes in the far-field. Also, in a radar antenna system, sidelobes may mask the detection of a weak target, introduce unwanted system noise, and diminish accurate target detection [20]. Phased array systems, specifically AESAs are intended to steer the beam to a desired direction [21], and there will always be aforementioned errors and offsets due to the reasons mentioned above requiring calibrations.

III. Circuit System Design for Phase Correction

Initially and for simplicity, the developed feeding system considers phase corrections only in this section. Basically, the proposed circuit-based calibration system is designed to work at 2 GHz and can act within an individual RF chain for phase control. This helps to ensure that desired and accurate phases are applied to each array element. Table 3 shows a list of components used in this system. The main circuit component is the AD8302 phase detector [22], and this detector is capable of measuring phase differences between its two inputs. The inputs of the AD8302 are referred to as channels ”(a)” and ”(b)” in this paper. Also, Fig. 5 shows a flowchart of the developed calibration process for the entire phase-correction circuit system. It details each step in the calibration procedure. For example, showing where users will be prompted to enter the desired and consecutive phased difference between the channels.

To further explain, a user will be prompted as to if a calibration is required in the computer-controlled system. If no calibration is required, then a previous calibration can be loaded to correct for any imbalances. If the user chooses to calibrate the system, the process will begin where the phase balance is measured between channels as illustrated in Fig. 5. Basically phase versus the PS bias is checked, and an LUT is then created. After some data analysis and interpolation (as further described next), the calibration is complete, however, a feedback loop is used to continuously check that the LUT is accurate. This simply checks a previous LUT value against real-time measurements.

A. Phase Comparator Characterization

Initially to assess the operation and accuracy of the AD8302 some test measurements were made using delay lines. The aim was to measure the phase offset between (a) and (b) which is caused by the delay lines (see Fig. 6). In the setup, the VCO output was split and one side was fed directly into the AD8302 and the other was fed into the AD8302 via a controlled delay line. In this characterization, three distinct PCB-based delay lines were manufactured: 30°, 45° and 60°. Each was measured independently. If there was a difference in phase, the AD8302 would output a voltage to identify this phase difference. Also, the AD8302 has no RF pass through, therefore the device terminates any input signals.

Shown in Fig. 7 is the basic look-up-table (LUT) which converts the AD8302 input phase difference (horizontal axis) to output voltage (vertical axis). The figure also shows some of the initial measurements collected: 30° (red), 45° (blue), and 60° (green). The results of these initial measurements were accurate and follow the data sheet specifications. It should be made clear that the LUT in Fig. 7 is documented in this paper to highlight the challenges when employing practical RF comparitors. More specifically, these limitations are related to the phase ambiguity, where the device cannot distinguish between a positive or negative phase shift as well as the possible error regions when detecting phase. Given these limitations, the AD8302 comparitor is unable

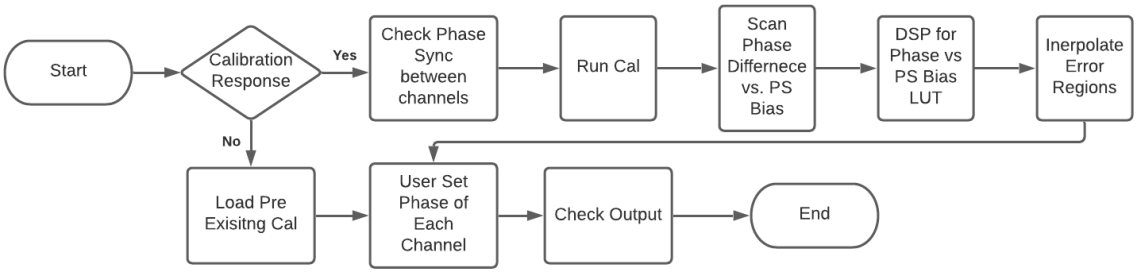

FIGURE 5. System-level outline for the developed algorithm for the channel phase calibration process. An Arduino-MATLAB connectivity platform was adopted.

TABLE 3. Phase Correction Circuitry Required Per RF Channel to Support Pattern Corrections and Array Calibrations

Component	Manufacturer	Model
Micro-controller	Arduino	Mega
Comparator	Analog Devices	AD8302
Phase Shifter (PS)	Mini-Circuits	JSPHS-2484
Local Oscillator (VCO)	Mini-Circuits	ZX95-2400-S

to provide totally accurate phase readings. In addition, the AD8302 does not support an RF pass-through, and as such the incoming channels to be phase interrogated need to be terminated (see Figs. 6 to 8). These issues are described in more detail next and the approaches to overcome these challenges.

Regardless of any apparent limitations for the AD8302, it is important to describe and analyse our adopted characterization and phase error mitigation procedure. As observed in Fig. 7, it can seen that each phase difference measurement is approximately 15° apart which is consistent with the employed PCB delay lines. Other testing measurements using PSs were completed but are not reported due to brevity. Regardless, all these findings and circuit studies (see Fig. 6) are important and were needed to fully assess the complete LUT as defined by the continuous line (see Fig. 7). These results are needed for development of the more advanced phase calibration circuit system as described next.

It should now be highlighted that the AD8302 board itself has inaccuracies of at least 10° within the following regions: -180° to -160°, -20° to 20°, and +160° to +180° [22]. Also, the AD8302 is only designed to provide conversion data from -180° to +180° with positive output voltage values [20]. This is a problem which can generate phase ambiguity, for example, with reference to the basic LUT in Fig. 5, in that the AD8302 alone cannot differentiate between ±50°. Similar limitations exist for all phases, due to the symmetry in the voltage curve of Fig. 7 about 0°, in that, the AD8302 comparator cannot be used alone for array calibrations.

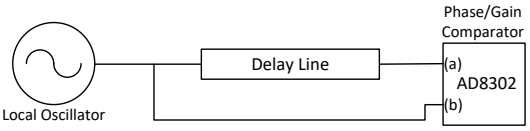

FIGURE 6. Testing circuit diagram using a PCB-based transmission line delay to initially test the accuracy and operation of the AD8302 phase detector.

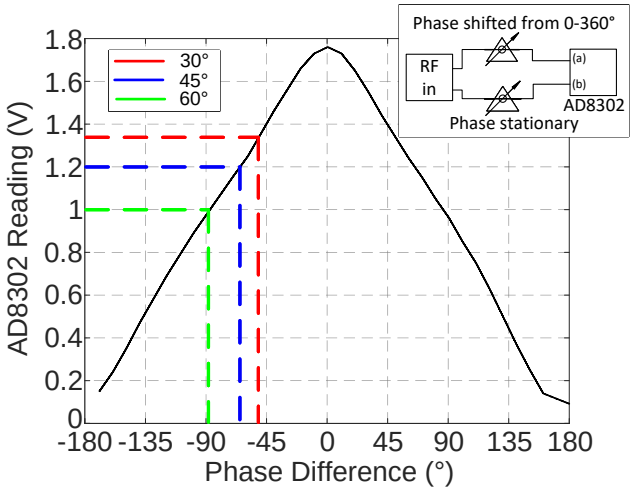

FIGURE 7. Initial LUT for phase characterization. The measurements show the phase differences for the delay lines with respect to the AD8302 output voltage (see the green, blue, and red dashed lines) using the circuit in Fig. 6. For the black continuous curve, the testing circuit in the inset was employed.

B. Look-up-table and Interpolation

To overcome these limitations, a more advanced LUT was desired and developed using the proposed active feeding circuit (see Figs. 8 and 9), which also employed voltage-based PSs and interpolation. The resulting and more advanced LUT, see Fig. 10, reports the phase difference versus the input voltage of the PS. Basically the input bias voltage of the PS controls the phase difference between the RF channels using a controlled loop (see Fig. 8) for correction and system calibration. Our developed circuit and advanced LUT is also able to provide reference data from 0° to 360°. Figure 8 also shows a black dotted line, which is where an antenna can be connected to the system.

This is an important advancement from Figs. 6 and 7 as well as the basic functionality of the PS itself, mainly due to the limited ±180° phase range and the phase ambiguity of the AD8302. However, it should be noted that in the 0° to 360° phase range, errors still exist between 0° to 20°, 160° to 200° and finally 340° to 360°. This phase error can be simply translated by taking the previous errors and unwrapping the phase. For example, the previous error region of -20° to 20° becomes 340° to 20°. Regardless, as described in the following, interpolation will be used to mitigate these error regions (see Fig. 10).

To populate this advanced LUT in Fig. 10, and record the phase differences with respect to the applied PS input bias voltage, an Arduino-MATLAB connectivity platform was developed. This further helps full characterization of the AD8302 comparator, and for this an exterior PS was needed. According to the data sheet of the employed PS [23], 15 V is required for the full phase spectrum (i.e.; 0° to 360°), however, the Arduino can only output a 5 V pulse-width modulated (PWM) signal. Therefore a digital-to-analog converter (DAC) was introduced to convert the PWM to an analogue output and an op-amp was also used to amplify the output to 15 V. This allowed for the programmable phase difference between the channels to be between 0° and 360°. The PS employed in the circuit system is the Mini-Circuits JSPHS-2484+ [23], and an analogous PS was also added to the other RF branch to observe equivalent losses for the RF circuit.

The circuit diagram in Fig. 8 also shows where antenna elements could be added to the two-channel system while the measured circuit for non-radiating bench-top studies is shown in Fig. 9. It should be noted that this bench-top circuit system was implemented to initially assess the phase shifting accuracy between channels 1 and 2 using a VNA. Antennas were not connected to the circuit system as this was a non-radiating test. Also, during the development of the advanced LUT, the phase of PS-1 (Fig. 8), was shifted by varying the voltage bias. This was changed in steps of 0.03V. For every set bias a respective reading was taken from the AD8302 and during this process PS-2 was kept constant. Alternatively, PS-2 can be varied and PS-1 kept constant to characterize the other branch. This process was fully automated and programmed and is needed for full characterization of the AD8302 comparator. Also, to record these data sets, the duration for the characterization was about 15 seconds (or less) for each RF channel.

After some post-processing a graph of the phase difference versus the input bias was prepared for the proposed circuit system. This is shown in Fig. 10 (blue curve), where the error regions are shown in red. The new error regions (due to the AD8302 as described previously) are roughly from 0° to 40°, 165° to 200°, and 330° to 360°. This offers some improvement when considering the AD8302 phase detector alone. It was then thought to use interpolation to better characterize these error regions and improve the accuracy for the entire circuit system. In particular, using MATLAB, a 9th-order polynomial was created and then programmed into the algorithm (see Fig. 5). The result is shown in Fig. 10 (red part). This interpolation can better support the required (full and complete) phase differences from 0° to 360° enabling any required consecutive phase difference, while the basic LUT (see Fig. 7); i.e. mainly the AD3802 RF comparator alone has errors regions and can only register absolute value phases from 0° to 180°, due to the noted phase ambiguity. This unwanted feature severely limits array

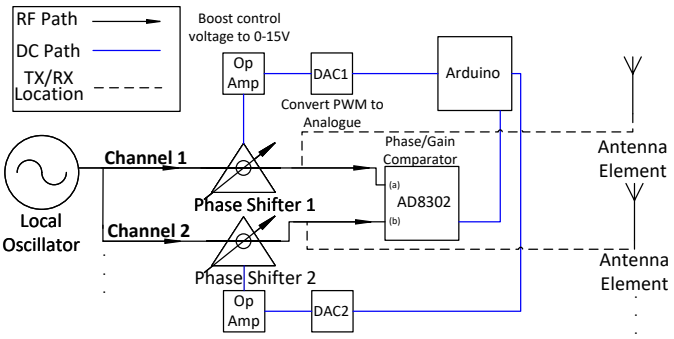

FIGURE 8. Circuit block diagram for phase channel correction at each antenna element, to support element-level self-calibration. The circuit system configuration is used to generate an advanced LUT (see Fig. 10, which overcomes the phase ambiguity problem shown in Fig. 7) and can also be used to characterize larger arrays as further reported in the paper (not just 2 channels as shown). Also, the black dotted lines shows where antennas could be connected using an RF switch or a power divider.

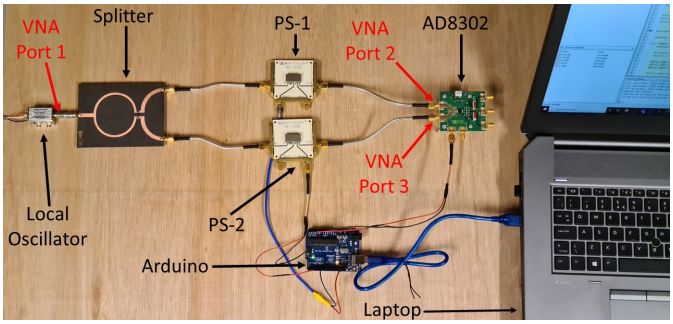

FIGURE 9. Non-radiating experiment to test the phase shifting accuracy. This initial two-channel circuit system (showing only the test source, VNA ports, splitter, PSs, and the AD8302) was connected a control laptop. It should be noted that antennas were not connected to the system.

correction functionality and further justifies the need of the developed computer-controlled system with interpolation.

At this stage, the antenna feeding circuit system for element-level calibrations was further programmed such that a desired phase difference could be set by sending a MATLAB command. Basically, the circuit could measure and correct any phase offsets and achieve the required phase difference between the RF chains, calibrating the system. For example, if a 100° consecutive phase difference was required at the array element terminals, MATLAB would check the required phase shifter bias from the advanced LUT (Fig. 10) which in this case would be 2V. Measurements to test the accuracy of the interpolation and the resulting circuit are described next.

C. Channel Measurements

The circuit system was tested using a 3-port VNA and the PSs were set to multiple different phases. Basically the VNA was used to confirm the set phase differences between ports (a) and (b) of the AD8302, or the antenna ports. The feeding circuit also operated well with low $S_{(1,1)}$ reflections (which were always below -30 dB), for the induced phase shifts and all results not reported for brevity. Similarly, for $S_{(2,2)}$ and

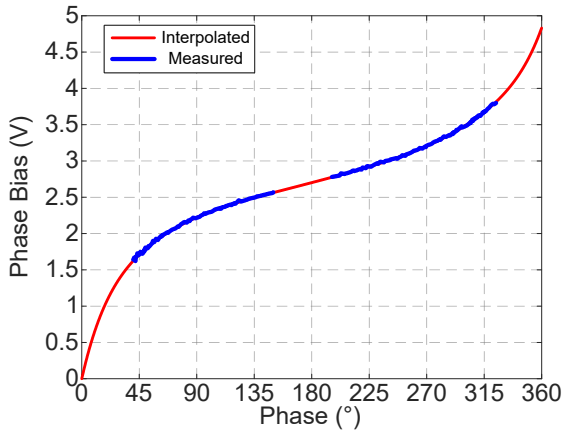

FIGURE 10. Generated LUT by measuring the circuit in Fig. 9 where the PS bias controls the relative phase difference between RF channels. The gaps from about 0° to 40°, 165° to 200°, and 330° to 360° illustrate where the AD8302 cannot accurately measure due to device limitations [22]. MATLAB interpolation shown in red to complete the advanced LUT.

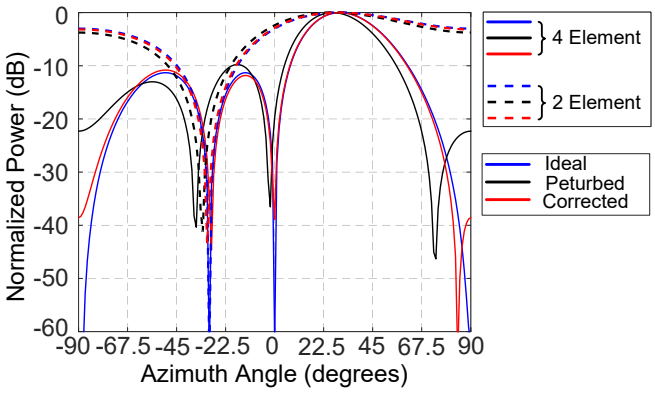

FIGURE 11. Steered beam to +30°. The 2×1 AF was calculated using measured results from the circuit system while the 4×1 array was also emulated from two-channel measurements. For these corrected patterns, the perturbed (20%) and ideal responses are compared to findings from Fig. 2.

$S_{(3,3)}$. Overall the system worked well and was extremely accurate at correcting and setting the desired consecutive phase differences between the RF channels achieving calibration.

Measurements are reported in Table 4 with errors of 3° or less. The average error can be said to be 1.4°. This is highly accurate as a 1.5° phase resolution can be achieved for each channel. This means that the system offers phase offsets (with embedded correction and interpolation) from 0° to 360° in control steps of 1.5°. This would essentially be equivalent to using an 8-bit digital PS which has a control resolution of 1.4° and costs significantly more. Table 1 compares the accuracy of the system demonstrator to that of a digital PS, and this gives an indication of the accuracy of the developed feeding and automatic calibration system when compared to other commercially available PSs. As mentioned previously, the AD8302 was also programmed in the aforementioned control loop (see Fig. 5), to actively monitor the phase in real time. For example, if there was

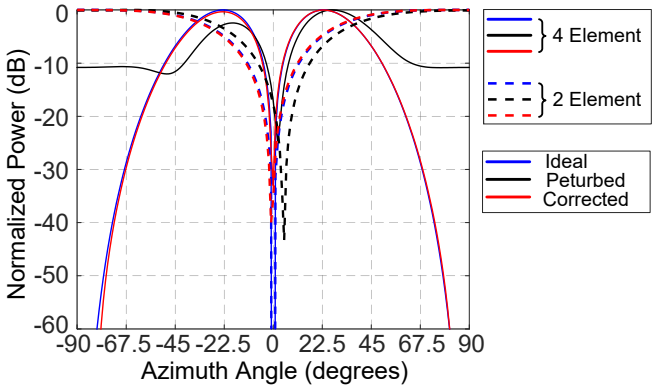

FIGURE 12. Similar to Fig. 11, but for monopulse difference patterns.

a substantial drift in phase above 5°, the system would recalibrate as required.

The findings reported at this stage have considered the designed circuit system prototype, and the comparator was attached to the channels in place of the antenna elements. However, in practice, the comparator could also be positioned alongside the antenna using a splitter with an unequal power split ratio [24]. Regardless, the final system would aim to utilise RF comparators which support RF pass through so the components can be added into the circuit system with no requirement for additional power dividers. However, as this is a simple prototype version and the employed AD8302 comparator does not support an RF pass through, antenna elements can replace the RF comparators after calibration. This is studied next given these results and the findings in Table 4.

D. Array Studies & Emulations

Using these channel measurement results of the circuit prototype, phase values were employed to emulate self-calibrations of a 2×1 and 4×1 antenna array and results are in Figs. 11 and 12. These emulations are basically mathematical calculations of the beam patterns considering the ideal responses compared to the corrected pattern. This builds upon the theory and findings outlined in Sec. II and Fig. 2, respectively.

TABLE 4. VNA Phase Measurements (Imbalances) $\angle S_{(3,2)}$ Between the RF Channels

Required Phase	Measured Phase	Error
0°	0°	0°
5°	5°	0°
30°	33°	3°
50°	53°	3°
100°	100°	0°
150°	151°	1°
180°	181°	1°
240°	238°	2°
270°	267°	3°
315°	312°	2°
350°	350°	0°

The blue lines in Figs. 11 and 12 show ideal patterns for the numerically examined or simulated array in MATLAB, the ideal case adds no errors. The black continuous lines show how the array pattern can be perturbed by introducing phase errors. In particular, the phase errors have been set to random by introducing a 20% variation from the ideal phases. The corrected patterns (red lines) are achieved by taking phase measurements of the developed circuit (Fig. 8) considering the required beam steering angles. This defined the consecutive phase differences between elements for the simulated array.

Figure 11 considers an array steered to 30°. It can be seen that the pattern with an error (black curve) steers to around 20° and the null depths are reduced. The corrected pattern steers correctly to 30°, consistent with the ideal array whilst retaining deep nulls. Shown in Fig. 12 is a monopulse difference pattern example where it can be seen that the ideal curve produces a well defined null centered at 0°. The error pattern can be seen to be offset by around 10° and the pattern is skewed. When inspecting the corrected pattern it can be observed that a deep null is recovered at 0° and the pattern is otherwise consistent with the ideal curve. For monopulse radar systems such nulls are important for accurate target detection and tracking [25].

IV. Four Channel System Development with Magnitude and Phase Correction

The previous section outlined the circuit calibration system considering only phase (see Fig. 8) and measurements were used to emulate beam corrections for a 2×1 and 4×1 phased array. The next step for the circuit system development is to include an active calibration system to correct both phase and magnitude. This system will have a PS and a variable gain amplifier (VGA) within each channel. Also, the two channel self-calibration feeding network developed in the previous section is extended to a four channel system herein.

A diagram of the 4×1 system is shown in Fig. 13. It can be seen that PSs and VGAs are added to each channel. It can also be seen that another AD8302 is employed for the four-channel system, when compared to the 2×1 system. This new system will be able to compensate for PS insertion loss and amplifier phase shift (see Appendix A). Each RF circuit element will require a dedicated control voltage and this is provided by the MATLAB controlled Arduino. The employed DAC is the MCP4728; i.e. it is a 4-channel DAC, meaning it connects to the Arduino via I2C and can output up to 4 individual DC voltages.

In total, 2 DACs are needed as 8 DC control channels are required (4 for the VGAs, 4 for the PSs). The DAC2 unit, which is connected to the PSs, will be connected via an op-amp to achieve the required 0 to 15V control range. The selected op-amp is an LM348 for the 4×1 system. The LM348 is a quad op-amp meaning it has 4 op-amps within a single chip. Therefore each channel for DAC2 could be connected to the LM348 op-amp and then connected from

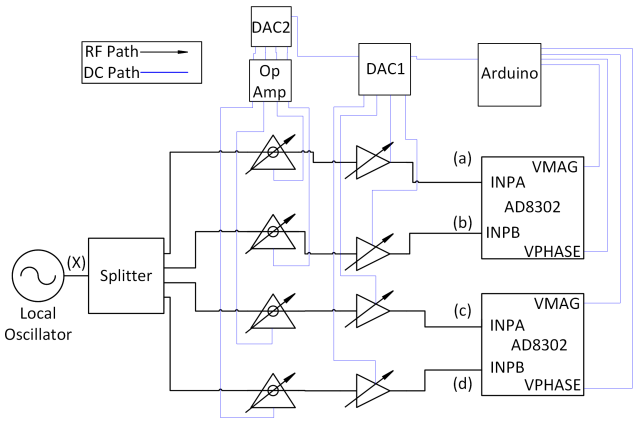

FIGURE 13. Diagram showing the 4-channel system with the DACs and Arduino. The RF path is shown in black and the DC/control path shown in blue.

the op-amps output to the PSs. DAC1 is used to control the VGAs, as each amplifier is voltage-controlled. Each DAC1 channel can be directly connected to the VGAs as shown in Fig. 13.

It should be mentioned that all channels cannot be compared directly. For example, in Fig. 13 channels (a) and (c) are not directly compared given the comparator positioning. However, the Arduino microcontroller monitors these two comparators programmatically and this allows the relative magnitude and phases between the four channels to be determined. In addition, the architecture allows for the calibration (and continuous monitoring) of the individual PSs and VGAs for each channel independently. This is because two independent DACs are used in the system. Knowledge of the signal channels is also well characterized given that the 1-to-4 splitter was fully assessed for imbalances, and these were calibrated into the system prior to integration. Therefore, unless there is a fault with the hardware, the signal coming out of the splitter for each channel should be relatively similar. If multiple splitters were used when up-scaling the circuit system for a larger array, then these would also need to calibrated prior to use in the system as done here for all passive and active components.

A. Step 1: Phase Characterisation for the 4×1 System

The first step is to calibrate the phase for all four channels and studying the response of the AD8302 comparators. This is achieved by the same principles as for the two channel system. Basically, this element-level calibration follows the approach and results in Figs. 6 and 7.

Measurements were completed to relate the output voltage of the AD8302 comparators to input phase, this is needed for best operation. As the AD8302 has two channels, each channel had to be characterised individually as it cannot be assumed both channels have the same behaviour. To further explain, the phase of input (a) was changed whilst keeping input (b) constant in phase, and its connecting channel was used as a reference of comparison (shown in Fig. 7). However, if the opposite is studied where input (b) is phase

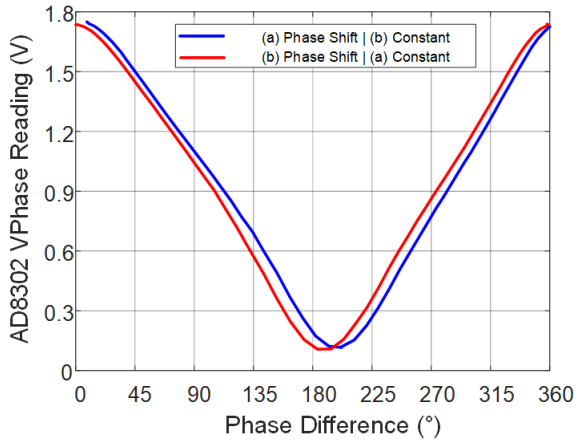

FIGURE 14. **Comparison between the phase LUT for each port of the AD8302. It can be observed that the phase response is slightly different for each port.**

TABLE 5. **Results of Phase Shifts Relative to the Channel Input**

Channel 1		Channel 2		Channel 3		Channel 4	
Set	Meas.	Set	Meas.	Set	Meas.	Set	Meas.
0°	0°	0°	0°	0°	0°	0°	0°
0°	0°	30°	30°	60°	61°	90°	89°
10°	10°	20°	20°	30°	28°	40°	40°
90°	88°	180°	178°	270°	273°	360°	360°
60°	61°	120°	118°	180°	179°	240°	241°

shifted and input (a) is kept at a constant phase, it is likely that both channels will not have an identical response.

This is reported in Fig. 14 where a comparison between the LUT for each channel is shown. It can be seen as expected that the response between input (a) and input (b) are different. This means that for calibration of the different channels, the relevant LUT should be used (as in Fig. 14). For simplicity input (a) can be referred to as the left side and input (b) as right side. As shown in Fig. 13, two AD8302s are used for a four-element system therefore the left and right sides of each device require a phase LUT. For calibration each input into the AD8302 was completed separately. This element level calibration is completed sequentially: left side calibration and then right side. This technique is also scalable and multiple AD8302s can all be calibrated for the left side and then the right side together. For example, referring to Fig. 13, channels (a) and (c) were calibrated simultaneously and then channels (b) and (d). Basically, the odd channels were calibrated together and then the even channel numbers. Also, during this step the VGAs were kept at a constant gain level.

Bench top measurements from the four-channel phase calibration are shown in Table 5. Basically, the desired phase was set or programmed, and then measured with an external VNA. It can be observed that the system is working with high accuracy. Any channel can be set to the desired phase allowing for the ability to create a phased array antenna with the desired consecutive phase difference, which is, self-calibrated accurately. This means that the system is able to correct for any δ within each channel (relative to the other channels) and introduced by the active components as illustrated in Fig. 1. The average phase error for the 4×1 system was observed to be about 1°, with the maximum phase error being 3°. This is an accurate result using low-cost hardware (see Table 1) and defines the first step in the characterization of the built-in self-calibration system for active phased arrays.

B. Step 2: Amplitude & Phase Correction for the 4×1 System

The next step is also to accommodate for unwanted magnitude offsets and the employed comparator; i.e. the AD8302 is also capable of measuring gain/magnitude differences between channels. This follows the approach for the phase difference calibration; i.e. Step 1. However, this second step is crucial as PSs can generate some unwanted insertion losses for each channel. Similarly, amplifiers can introduce some unwanted phase accrual. This is further described in Appendix A. For further details on this amplitude calibration procedure for the 4×1 system; i.e. Step 2, see Appendix B.

C. Magnitude and Phase Procedure for Self-Calibration

This section outlines our developed and MATLAB programmed self-calibration procedure such that there is a corrected (and user defined) relative magnitude and phase between channels. This allows for a broadside array in the simplest case, or more advanced beam-steering and tapering scenarios. Basically it encompasses all the element level calibration and LUTs as described in this paper whilst embedding Steps #1 and #2 for the circuit system as previously outlined in Sections A and B, respectively. The process is represented using a flowchart as in Fig. 15 and can be briefly described mathematically for each channel within the active phased array system.

1) Set magnitude and phase differences (ψ), to get $Ae^{j\psi}$ for each channel.
2) Phase shifters creates an insertion loss, denoted as α_L which should be looked up from the predefined LUT leading to $(A-\alpha_L)e^{j\psi}$.
3) Set VGAs to compensate for the insertion (IS) loss. This gain is donated as α_G leading to $(A-\alpha_L+\alpha_G)e^{j\psi}$.
4) This gain increase by the VGAs will create a phase shift which can be donated as Δ. This leads to $(A-\alpha_L+\alpha_G)e^{j(\psi+\Delta)}$.
5) The phase shift (Δ) caused by these VGAs when set to α_G can be determined using a LUT. The initial phase difference ψ can then be set to $\psi-\Delta$. This leads to $(A-\alpha_L+\alpha_G)e^{j((\psi-\Delta)+\Delta)}$.
6) These corrections finally cancel to $Ae^{j\psi}$ for each channel. A feedback loop is also shown to check the final phase is equal to the phase which is set by the user.

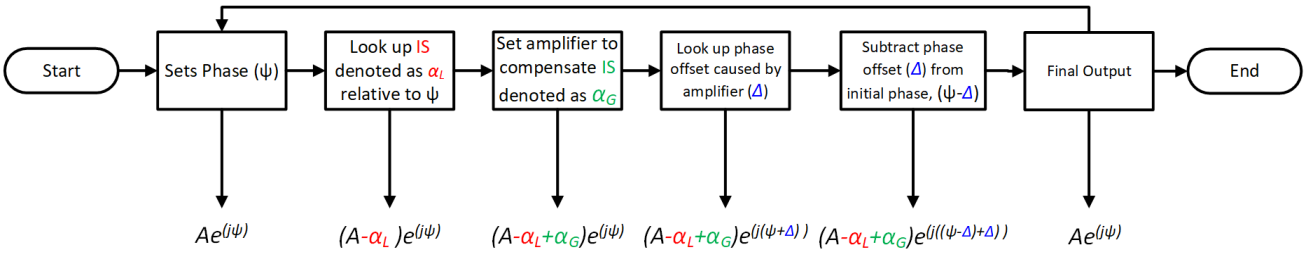

FIGURE 15. Self-calibration procedure to achieve the desired phase and amplitude offsets (and corrected) due to insertion loss (IS) and other imbalances for the active phased array system within a feedback loop. Once complete, the desired consecutive phase differences between each channel can be selected by adjusting the relevant PS. Array tapering is also possible by similar amplifier control and the system can accommodate LUT updating as needed. In addition, since this computer controlled system can run continuously to offer self-calibration, operation can be in-field and not require traditional VNAs (for example).

This process allows for the phase to be set with no insertion loss and compensates for the errors caused by the amplifiers. It should also be noted that in step 5) above the phase is set to $\psi - \Delta$. This will technically alter the insertion loss, but in practice, the effects have observed to be negligible for the system. However, if this minor gain deviation was problematic for each channel, phase setting steps 1) to 5) could be iteratively repeated or made recursive to minimize insertion loss. Also, once zero phase difference and zero magnitude balance has been achieved between channels (defining self-calibration), the system can also be further programmed to set the magnitude or gain as required. This is useful for a binomial array or other array tapering cases [2] as well as conventional phased array beam steering.

The procedure has been tested for the four channel system and the results yielded high accuracy calibrations for the magnitude and phase for each channel. The system was able to set a consecutive phase difference between channels and also hold the magnitude at the required level. Table 6 shows the measurement results for each channel after setting a 90° consecutive phase shift. The average phase error is calculated to be 1°, and the average amplitude error between channels is about 0.05 dB. This can be considered an accurate self-correction result, especially since each channel will have a different insertion loss due to the different phase shifts applied. Other cases were also studied (not reported for brevity) and similar findings were observed. This sub-section concludes the circuit system bench top self-calibrations and measurement verification, with the next sub-section providing a testing summary and then moving on to far-field measurements with a 4×1 patch array in Sec. V.

D. Testing Summary and Further System Integration

The adopted experimental testing procedure for the proof-of-concept system can be summarized as follows. (1): Initiate the computer-controlled self-calibration routine for magnitude and phase using the AD8302s which are directly connected to the circuit system. This ensures that any imbalances can be removed and consecutive channel phasing set. (2): Then, to further test the system prototype for radiation studies, the AD8302 comparators can be removed, and (3): the relevant channels re-connected to the antenna array element ports. (4): This allows for additional studies in an anechoic chamber defining the testing and array calibration methodology.

TABLE 6. Calibrated Output per Channel for a 90° Consecutive Phase Difference with Reference to Channel (a)

Channel	Set Phase	Meas. Phase	Meas. Imbalance
(a)	0°	0°	0.00 dB
(b)	90°	88°	-0.10 dB
(c)	180°	181°	-0.10 dB
(d)	270°	267°	0.00 dB

If considering further experimentation and full array and self-calibrating system integration and testing, an RF switch or splitter could also be employed for each channel. Or, as previously discussed in Sec. C, a custom comparator can be developed supporting RF pass through, and this defines future work. This means that the system can simultaneously operate in a self-calibration and operational radiating routine, and without re-connecting any antenna channels. This is because the self-calibrating circuit system would be fully built-in and integrated into the array.

V. System Far-Field Measurements

The developed and programmable active feeding circuit system has been tested using non-radiating measurements, mainly, to demonstrate its self-calibration capability. This has been reported in the previous sections as well as the supporting appendices. Also, given that it employs PSs and VGAs for each channel, the system can provide beam-steering functionality and array tapering once calibrated. To assess this, the circuit system was tested in the anechoic chamber at The University of Edinburgh, whilst being connected to a simple phased array antenna. In particular, a conventional 4×1 patch array was designed and optimised using CST Microwave Studio Suite for operation at 2 GHz whilst being printed on FR-4. Reflection coefficient simulations and measurements demonstrated -15 dB matching or better (50-Ω impedance) for each element. Results not reported for brevity. A photo of the fabricated array is shown in Fig. 16.

The active phased array was measured in transmit mode, and when connected to the active feeding system as shown

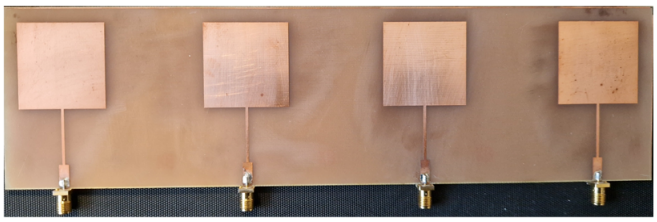

FIGURE 16. **Fabricated array for far-field testing of the self-calibrating system. The patch array was designed to operate at 2 GHz and with $\lambda/2$ spacing.**

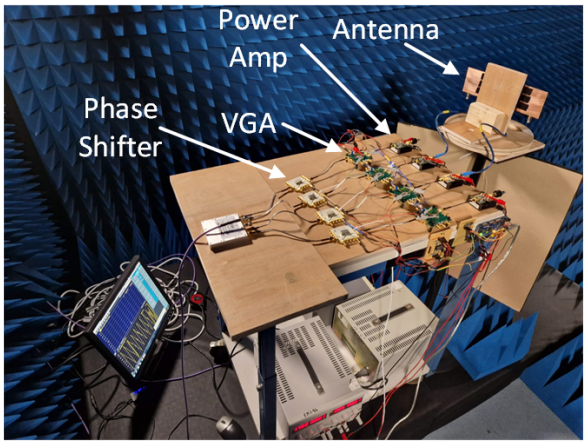

FIGURE 17. **Measurement setup where the main system components are shown.**

in Fig. 13. A receiving horn was placed in the FF to measure the received power. In addition, power amplifiers (Qorvo TQP111) were also added to each channel to increase the transmit power. This achieved a higher dynamic range above the noise floor and when no power amplifiers were employed. An image of the measurement setup is shown in Fig. 17. This image shows the system in TX mode, with a horn placed in the FF (not shown) sampling the received signal.

As mentioned, Fig. 17 shows the measurement setup. The system was first self-calibrated (as discussed in the last few sections), and then the two AD8302s were removed and replaced with array element connections (see Fig. 13). This was done so FF measurements could be completed defining the *System On* trials. The array was connected in this way as the developed system is a prototype demonstrator. However, in future work, additional RF components such as non-equal power dividers, couplers, or circulators could be included in the circuit system architecture and depending on the specific requirements. In addition, our calibration approach does not take into account any antenna mismatches as the system design considered a 50-Ω system impedance for every port connection, including the comparators. It is expected that any small mismatches would cause a minor shift from the calibration, assuming low reflection coefficient values.

A standard broadside pattern measurement was initially realized by the self-calibrating system by programming a uniform array; i.e. by setting all elements to have a common phase difference and equal gain. This will result in a beam maximum at 0° in the FF. Results are also compared with simulations in Fig. 18. It can be observed that the simulated and measured patterns are in good agreement. The system was then set to steer the beam to -20° and the measured result is shown in Fig. 19. It again be observed that the results show agreement with the simulations indicating the self-correcting feeding system is working as programmed. Figure 20 reports difference patterns (simulations compared to measurements) where two of the four elements have been set to a 180° phase difference, and the system amplitudes are all equal. In addition, the measured difference pattern is in good agreement with the simulated, in that a deep null can be found at 0° as expected.

It should be mentioned that there is a small but noticeable difference from the simulations and measurements. For example, the position and depth of the measured nulls are not fully consistent with the simulations. This could be related to a number of factors relating to fabrication of the array itself. For example, there might have been some minor manufacturing tolerances when compared to the more ideal simulation model. In addition, for low-cost implementation and testing of the experimental prototype, the array was fabricated using an FR-4 substrate and designed assuming a constant relative dielectric of 4.3. However, there could have be some variations with this material from this ideal in terms of a change in the relative dielectric constant.

Calibrations of the circuit system also included up to the antenna array ports only, however, no corrections were completed for the phaseless cables which observed some bending and twisting during the angular pattern measurements. This practicality can add some minor phase imbalances between the channels. Future work can include self-calibrations of any attached cabling connected to the array elements themselves. In addition, as shown in Fig. 17, the self-calibrating circuit system was placed on a platform inside the anechoic chamber with power supplies and cabling attached, and this was required for experimental testing. This arrangement could have also caused some unwanted scattering and can further explain the minor discrepancies between the CST simulations and experiments. Regardless, measurement findings are in general agreement with the simulations and the observed deviations are typical to what one can expect when measuring proof-of-concept demonstrators.

As previously outlined, the circuit feeding system can also set each channel to specific gain amounts. This capability allows for array tapering, in general, and a binomial pattern [2] was programmed and measured. It should be mentioned that a binomial pattern typically has theoretically no side lobes at the cost of an increase in the half-power beam width (HPBW). This can be observed when compared to a uniform broadside pattern as in Fig. 21. As expected, reduced side lobe levels (SLLs) can be seen with an increase in the HPBW. Other pattern synthesis scenarios are also possible, such as triangular, cosine, or Chebyshev [2], and

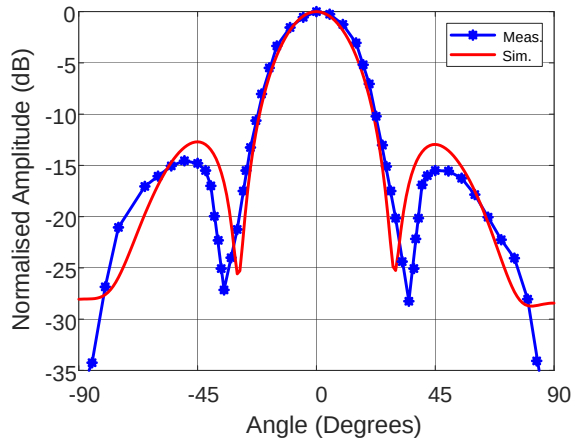

FIGURE 18. Full-wave pattern simulation and measurement comparison for a broadside beam at 2 GHz with the self-calibration *System On*.

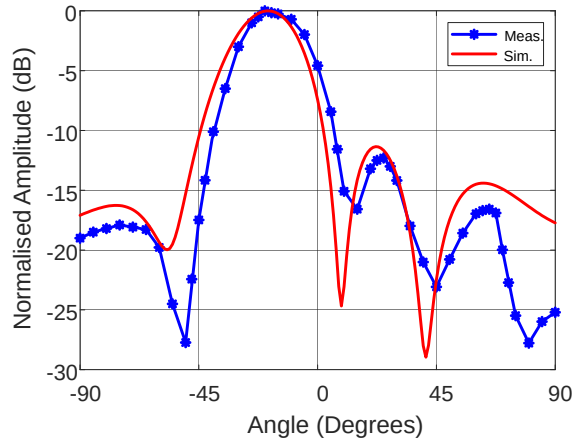

FIGURE 19. Full-wave pattern simulation and measurement of the beam steered to -20° at 2 GHz with the self-calibration *System On*.

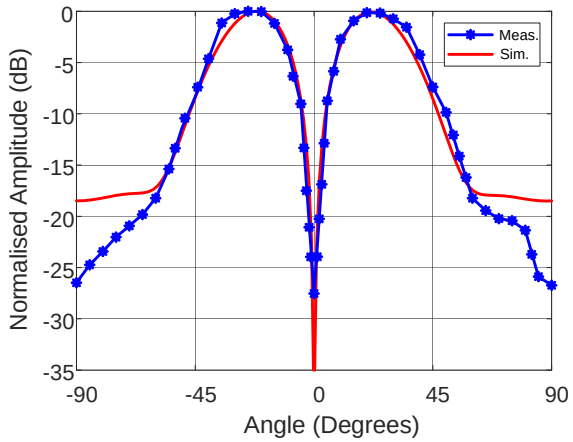

FIGURE 20. Full-wave difference pattern simulation and measurement (both centered at 0°) at 2 GHz with the self-calibration *System On*.

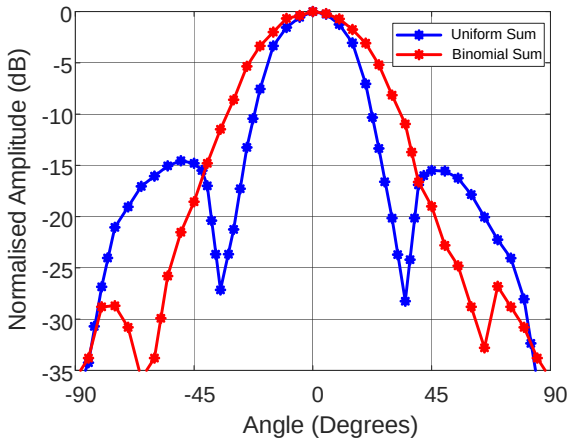

FIGURE 21. Measurement comparison of a uniform and a binomial broadside beam which considers active array tapering. Reduced SLLs and an increase in the HPBW can be observed for the array formed with binomial tapering. Measurement completed at 2 GHz with the self-calibration *System On*.

are considered future work. Regardless, measurements and simulations are in agreement for the steered beam cases while the amplitude tapering approach was also validated and these findings demonstrate proof-of-concept for the self-calibrating circuit feeding system.

As mentioned in the last section, the active system automatically corrects the magnitude and phase of each channel to ensure a negligible error; i.e. defining the self-correcting phased array. Figure 22 shows a comparison with the *System On* (defining a calibrated scenario), and with the *System Off*. This *Off* case implies that there will be unwanted magnitude and phase imbalances between channels (defining a non-calibrated system). Also, with the *System Off* case, the phase and magnitude is not properly characterised for each component in the channels and the datasheet was crudely used to set the magnitude of the PGA, as well as the phase of the PS.

Given these definitions and if we consider Fig. 22, it can be observed that the *On* case has low and symmetric side lobes, whereas the *Off* case has high SLLs which approach -5 dB. The beam for the *Off* case is also narrower, likely due to power being directed into those side lobes. Basically, this is related to more power being lost in the side-lobes and opposite to the binomial tapered array (which has no sidelobes). In summary, these observed beam pattern features (i.e. high SLLs) are generally unwanted and linked to the aforementioned magnitude and phase imbalances between the RF circuit channels.

The system was then set to steer the beam to -30°, this is shown in Fig. 23 (red). For other measurement trials, some artificial magnitude and phase errors were also programmed into the system to show the importance of accurate calibration. Figure 23 (blue) has errors up to 10% and the black curve shows errors up to 15%. Also, the peak

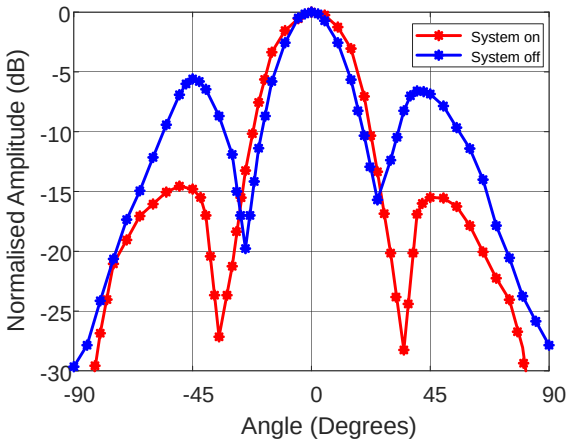

FIGURE 22. Measured comparison for a broadside beam when the system is on (self-calibrated, red) and when the system is off (blue); i.e. defining no automatic correction. Measurement completed at 2 GHz.

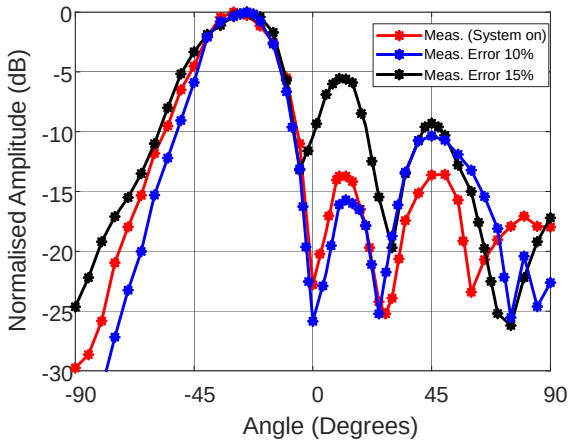

FIGURE 23. Measured beam at 2 GHz, steered to -30° whilst employing the calibration circuit system (red). The result is also compared to different cases for various phase and magnitude errors. These artificially induced errors are programmed by the active feeding system and defined in the legend (black and blue curves). It also should be mentioned that the red curve maximum is at -30° (as expected), whereas the black and blue maximums were measured at -25°. This deviation is due to the noted errors introduced into the RF channels.

of the main beam also becomes offset by 5° when errors were introduced; for more details see the caption of Fig. 23.

It can also be observed that with the added and controlled errors, the SLLs increase again to about -5 dB in the worst case. In addition, higher power is observed at +45° for the second side lobe when compared to the calibrated case (i.e. programmed with no errors). These results are expected as outlined in Sections II and III, in that magnitude and phase errors will perturb the beam position and increase the SLLs. This is because for the 10% and 15% error cases, the beam is offset by 5°, and these results are consistent with the calculations in Table 2. For example, for similar percentage errors, Table 2 outlines that the main beam can be easily offset from its desired location by about 5°. Also, that the first and second null positions can be altered by more than 6° from the ideal null position (for like error cases) and this too is observed in Fig. 23.

A. General Discussion

As observed, the self-calibrating phased array system performs well in the FF when compared to the programmatically added errors. The theory supporting this testing approach was discussed earlier in Sections II and III and shown in Figs. 2, 3 and 4. Generally that with increase in both magnitude and phase errors the SLLs can increase as well as the beam position for smaller arrays. The results also show that after the self-calibration, or for the *System On* cases that, there is generally a good agreement with the simulated beam pattern showing proof-of-concept for the circuit system demonstrator. Moreover, these findings show the benefits of the proposed active beamforming system, mainly, in terms of its well controlled beam steering, close to ideal HPBWs, well predicted beam pointing maximums, and SLLs, as well as array tapering by self-calibrated channel amplitude and phase control.

B. System Scalability and Other Considerations

It is important to identify that the experimentally verified four channel system can be upscaled to larger arrays as required. Figure 24 illustrates a possible array (or sub-array) implementation which uses a custom-made N-port comparator, and with an RF pass through to the antenna element ports. This larger-scale comparator allows for each channel to be calibrated (using a feedback loop to control the PSs and VGAs), and where the first (or middle) channel of the array could offer system magnitude and phase references, for example. Also, the comparator, PSs, and VGAs can be specially designed and integrated on one common PCB for more commercial implementations. Other active circuit system architectures are also possible for such an analogue design, but Fig. 24 is probably the most basic configuration when considering a larger sized, self-calibrating system.

VI. Conclusion

An active feeding circuit for automatic calibration of magnitude and phase for array antennas has been reported. Using commercial circuit components and Arduino-MATLAB programming, an automated and accurate phase steering and tapering system was designed and experimentally verified as well as practically demonstrated for proof-of-concept. As mentioned in the paper, the developed array calibration feed system can be considered a more integrated version of the calibration lines method [15]. This is because the typical transmission lines and calibration electronics, which are usually external to the array (as in the calibration lines method [15]), are now built directly into the array itself. To the best knowledge of the authors, no similar feeding circuit

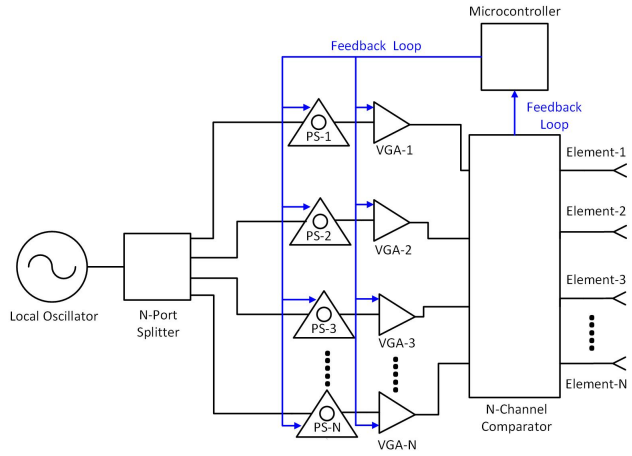

FIGURE 24. Possible system architecture for larger scale arrays (or sub-arrays) using an N-port comparator which has an RF pass through for the channels and connectivity to the individual antenna elements. This will allow the system to be scaled with ease; different and other practical circuit system architectures are also possible.

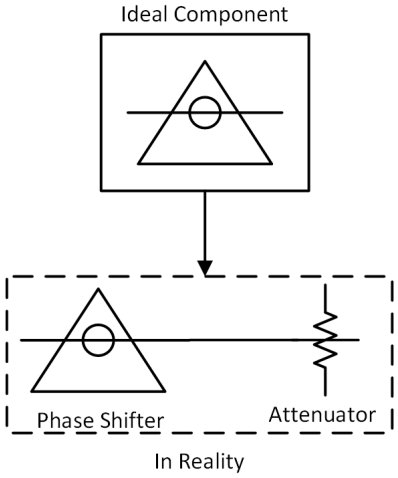

FIGURE 25. Illustration of an ideal PS and the PS in reality, with an added attenuator. The practical PS will have a phase-dependant insertion loss.

system has been reported previously enabling automatic calibration of phased array antennas.

Basically, at the element-level, the phase differences between RF channels was controlled using PSs and simultaneously monitored in real-time using a phase comparator. The comparator was also able to monitor the magnitude difference between channels and a VGA was placed within each channel to control the magnitude at the element level as well. This was all governed by a computer-controlled Arduino-MATLAB script with user input. This enabled self-calibration of the channels as well as accurate control of the desired magnitude and consecutive phase difference between elements. Furthermore, the developed 4×1 system was tested in the far-field with a patch array and results showed good agreement with simulations for various broadside cases, steered beam scenarios, and array tapering.

VII. Acknowledgement

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Appendix A
Phase Shifter and Variable Gain Amplifier Characterization

Both PSs and amplifiers can be considered to be the most important components in a phase array system and these circuit elements have non-idealities which need full characterization and correction (and prior to full system integration). Phase shifters themselves, for example, will have an insertion loss dependant on the amount of phase shift or voltage applied. This is illustrated in Fig. 25.

For the particular PS employed in the circuit system (i.e. the JSPHS-2484), the insertion loss is reported in the data sheet to be typically around 2 dB [23]. However the

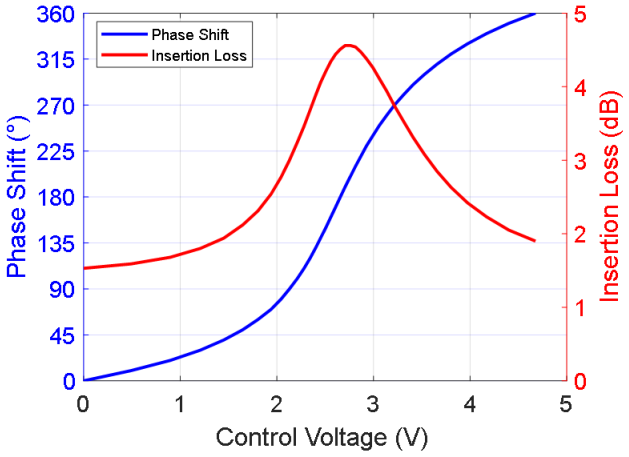

FIGURE 26. Phase shifter (JSPHS-2484) characterisation to observe the phase shift and insertion loss with respect to the phase control voltage.

maximum insertion loss is significantly higher. For example, the measured characteristics for the JSPHS-2484 PS are reported in Fig. 26. It can be observed that the insertion loss is 1.5 dB for 0 V (red line). The curve also shows how the loss changes with control voltage and the blue curve shows how the phase changes with control voltage. It can be seen that the maximum loss is around 4.5 dB. It should also be noted that each PS will perform slightly different in practice due to manufacturing tolerances, etc. however, with a number of device test trials, results were consistent to those reported in Fig. 26.

An amplifier on the other hand will increase the gain of a signal, however, it will also add a phase shift. The size of phase shift depends on the specific amplifier, and the amount of amplification. This will cause phase errors for the circuit system, therefore, it is important to characterize the behaviour of the amplifiers used within the proposed phased

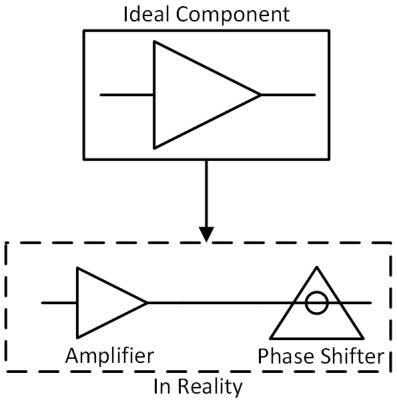

FIGURE 27. Illustration of an ideal amplifier and then showing a practical amplifier in reality. The PS is included as the amplification in practice causes a phase shift.

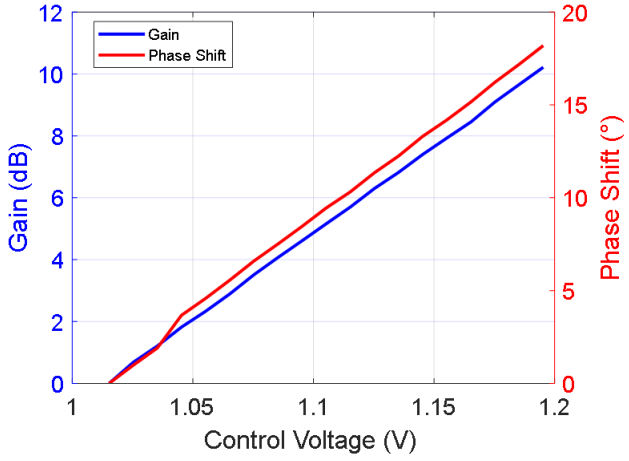

FIGURE 28. Variable gain amplifier (ADL5330) characterisation using an external VNA to observe the gain and phase shift with respect to the control voltage.

array system. Figure 27 shows a comparison between an ideal amplifier and an amplifier in practice. In the proposed circuit system (see Fig. 13) the chosen amplifier is the ADL5330 [26], produced by Analog Devices. It is a voltage controlled amplifier (VGA) operating between 10 MHz and 3 GHz. The device is capable of amplifying up to 20 dB. However, for our active feeding system we simply need to amplify by a maximum of 4.5 dB to counter the effects of the PS insertion loss. The data sheet also reports no relationship between amplification and phase shift. However, we can measure the amplifier using a VNA and a DC power supply to understand the characteristics of the VGA. Results are reported in Fig. 28 and these findings are required when including gain correction (and subsequent phase correction) as further described in Section IV.

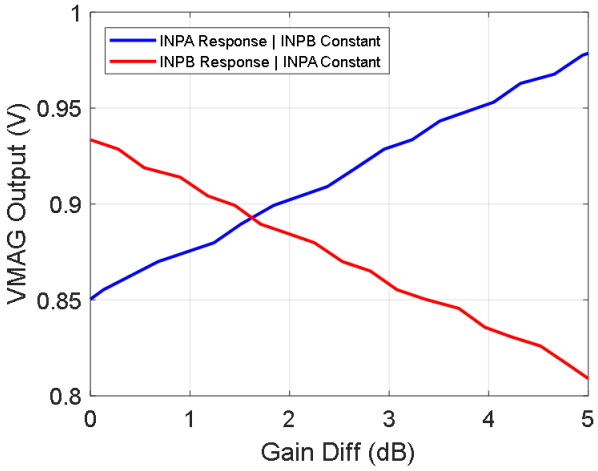

FIGURE 29. Measured LUT using a VNA converting the output of the AD8302 (i.e. VMAG) to a gain difference, and this is specific for the VGA. Both channels of the AD8302 are shown and the gradient difference can be observed.

Appendix B
Details on the System Calibration

As the magnitude of the input RF signals connected between channels, (a) and (b), of the AD8302 comparitor vary, the output voltage of the VMAG port (see Fig. 29) will also change. The data sheet [22] (TPC 1-6) shows that as port (a) is changed in magnitude and port (b) held stationary the gradient of the VMAG versus the magnitude difference is positive. If the ports are reserved the gradient will become negative. This result indicates that an element-level calibration and LUT for the response of each scenario is required. It can also be noted that the response is linear. Moreover, unlike with phase characterization between the channels (see Figs. 7 and 10), there is no ambiguity between a positive and negative magnitude differences for the employed comparator.

It also needs to be highlighted that the AD8302 was unable to accurately measure the insertion loss of the individual PSs (JSPHS-2484) in the channels. After further examination and bench top measurements, it was determined that this challenge was related to the significant insertion losses of the individual PSs (see Fig. 26). Basically, as the phase is changed significantly due to an insertion loss of more than 4 dB, the AD8302 is unable to measure insertion loss accurately. However, as the insertion losses are required to be characterized for the circuit system and to achieve the noted calibrations, this loss was measured for each channel PS. This was done in a separate experiment using a calibrated VNA, and results were stored as reference data in MATLAB, more specifically, insertion loss data was recorded and related to each phase measurement value. For example, if the phase of channel 1 was set to 15°, the MATLAB program stored data of the insertion loss associated with this phase shift. In this case, the insertion loss for a 15° offset is 0.25 dB.

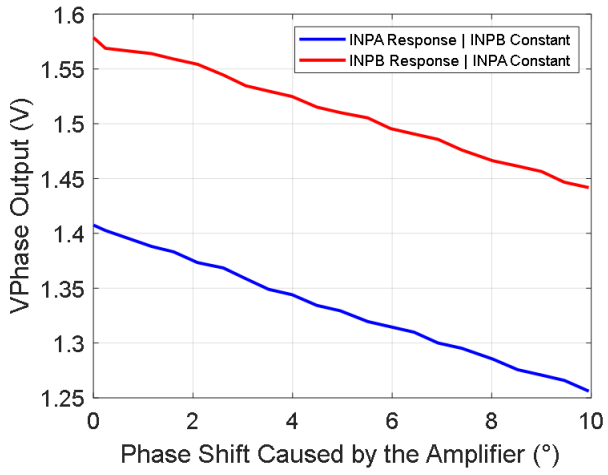

FIGURE 30. Measured LUT using a VNA, converting the VPhase output in volts to a phase in degrees. This is specific to the phase shift brought about by the VGA only. The difference in the blue and red curves is for the same reasons as in Fig. 14, in that there are slightly different voltage outputs for each port of the AD8392 comparitor.

It can also be observed that the phase shift caused by the VGA (see Fig. 28) is around 7° for an amplification of 5 dB. Also, as previously mentioned, the AD8302 comparitor has an error region when measuring phase differences between 0 and 30° (see Fig. 10). Only the 0 to 30° region is an issue here as the amplifier does not change the phase more than approxiametely 20°. To overcome this challenge, an artificial phase shift of 30° was added programically. This phase offset moves the phase difference out of the erroneous range. The PSs will also add an insertion loss, however, this can be neglected as the motivation is to characterise the VGAs at this stage. The result of the VMAG output when the phase shifter is set to 30° is also taken as a 0 dB reference and the response of the VPHASE port is taken to be 0°, which basically ignores the phase shift caused by the JSPHS-2484 PHs.

A. Look-up Tables for Amplitude Characterization

Figure 29 shows the response of the AD8302s VMAG output, when varying the gain difference between ports. Both scenarios have been reported; i.e. by varying channel (a) whilst holding channel (b) constant, as well as, varying channel (b) and holding channel (a) constant. The difference in gradient can be seen for the different scenarios. The plot goes from 0 to 5 dB as this is enough to cover the insertion loss of the PS. This plot can be used as an LUT for converting the AD8302s VMAG output to a gain difference, specifically for the ADL5330 VGA.

As mentioned previously, this VGA will also cause a varying phase shift as the amplification increases. This can be observed in Fig. 28, and as the gain increases so does the phase. The AD8302 is capable of measuring phase differences and gain differences simultaneously, therefore, the phase shift of the VGAs can be measured relative to its gain. Figure 30 reports the LUT for phase differences specific for this VGA. This LUT will convert the VPhase output of the AD8302 comparitor to a phase difference in degrees. This LUT is specific to the VGAs as the aforementioned phase shift is added to move away from the noted error region.

It can also be observed in Figs. 29 and 30 that all the LUTs are linear. This means the LUT can be represented in a linear equation form (within MATLAB) as the raw measured data demonstrated some small variations as function of control bias, see Fig. 31. As there is an LUT for magnitude and phase per circuit element (within each channel) there will be a total of 8 equations for the developed four-channel system. In this appendix, we will explain the analysis for a single VGA element for brevity. The corresponding AD8302 output for gain can be represented as $VMAG = m \cdot [Gain\ Diff] + c$, where m and c are the gradient and y-intercept, which are calculated to be 0.025 and 0.851, respectively. The phase LUT shown in Fig. 30 can also be represented as $VPhase = m \cdot [Phase\ Diff] + c$, where m and c are calculated to be -0.01506 and 1.405, respectively. These two linear equations can be used to link the AD8302 output voltages to the respective magnitude and phase differences.

B. Amplifier and Phase Shifter Simultaneous Calibration

The next step is to take measurements from the VGA. It can be observed in Fig. 13 that a second DAC is connected to each amplifier. We will look at the calibration procedure of a single amplifier at this stage. Moreover, by using the AD8302 we can measure the amplifiers gain and the phase shift associated for each desired gain. It can be the seen from Fig. 28 that the amplifier has a very sensitive control voltage. Next, whilst maintaining the PS of channel (a) at 30°, the control voltage of the VGA (within this channel) was then controlled by the DAC. In MATLAB, a loop was created to run from 1.0 to 1.1 V in increments of 0.001 V. For every control voltage, the amplifier is set to a respective reading taken from VMAG and VPhase of the AD8302.

Using this approach we will first look at the VMAG output, which is based on the VGA control bias as shown in Fig. 31. It can be seen that as the amplifier control bias increases, the AD8302 VMAG output increases. The data can also be seen to have small variations and this is likely due to added noise by the VGA and also the accuracy of the AD8302 and the DAC. The VMAG output can then be converted to a dB value (using the aforementioned linear equation), and this leads to the LUT shown in Fig. 32. It can be seen that the data is still noisy (blue curve) therefore a line of best fit was added (red curve). The red line can be used to determine the control bias required for a specific amount of channel gain.

The same process was repeated for the VPhase output, shown in Fig. 33, which is the raw data output of the AD8302s VPhase port. Again, for the same reasons mentioned, some noise can be observed in the phase output. Using the above equation for $VPhase$, the output (y-axis)

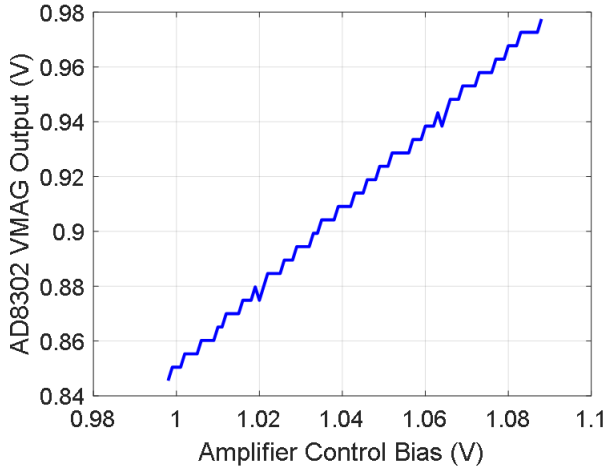

FIGURE 31. Measured voltage for the VMAG output port of the AD8302 comparitor when changing the VGA control bias.

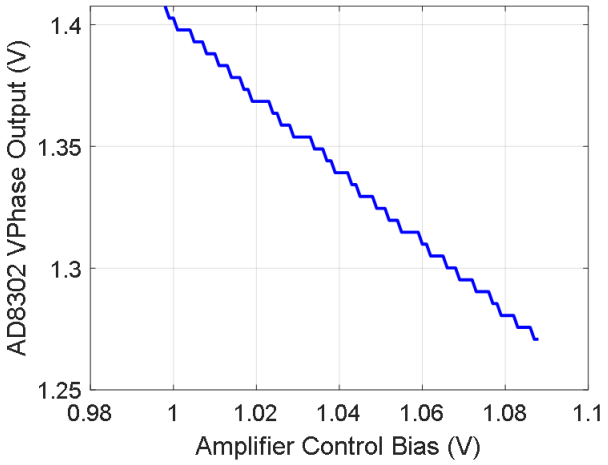

FIGURE 33. Measured voltage for the VPhase output port of the AD8302 comparitor when changing the VGA control bias.

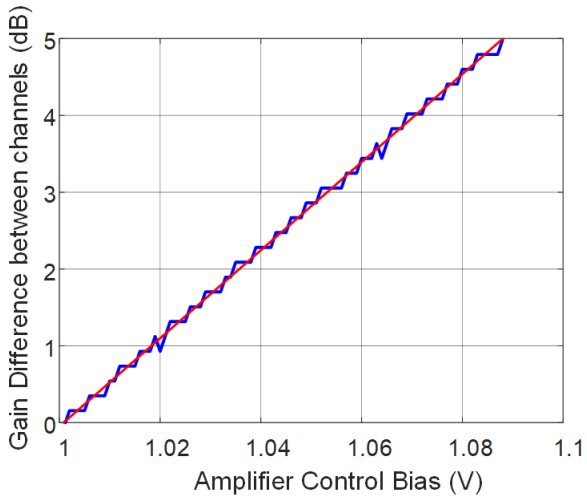

FIGURE 32. Measured plot (blue) for the VGA bias versus the amplitude difference between the channels connected to the AD8302. The linear curve of best fit (red) defines a LUT for the VGA bias versus channel magnitude difference.

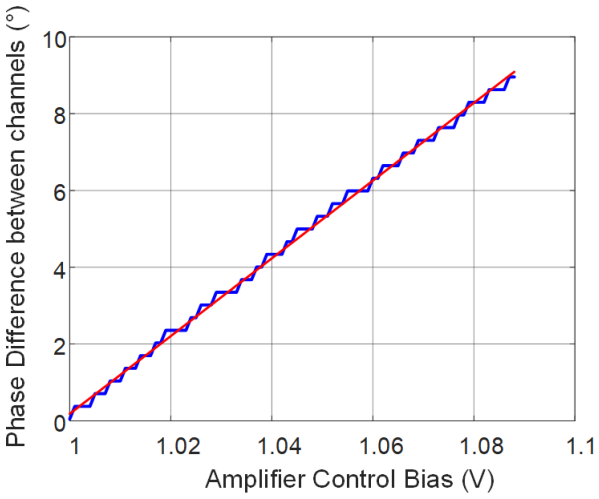

FIGURE 34. Measured plot (blue) for the VGA bias versus the phase difference between the channels connected to the AD8302. The linear curve of best fit (red) defines a LUT for the VGA bias versus the added phase increase.

can be converted to degrees. This is shown in Fig. 34. A line of best fit was also added which can be observed in red. This LUT allows us to determine the phase shift caused by the amplifier at a given control voltage.

C. Overview of the all the Look-up Tables

If we consider Figs. 32 and 34, we have two LUTs which relate the control voltage to gain, and, VGA control voltage to phase shift. Given this detailed characterization, if there was a 2 dB insertion loss created by PS-1, as an example, we can refer to Fig. 32 to find the control voltage needed for a 2 dB amplification by the VGA, which is around 1.035 V. We can then refer to Fig. 34 to determine the phase shift added due to the amplification. In this case, a 3.8° phase shift is added by the VGA.

The system was tested by setting the amplifier to specific gain amounts using the gain LUT (Fig. 32) and the expected phase shift is also recorded from the phase LUT (Fig. 34). The results can then be measured using a VNA connected from (x) to (1) (see Fig. 13). The results are shown in Table 7. For a single channel a total of 4 LUTs are needed, therefore for a four channel system, 16 LUTs are created. However, this does not consider the LUTs for the AD8302 voltage to phase/mag conversion which can be common for all channels, but should be done individually for each comparator for best accuracy.

At this stage we have now described the 4-element system and for each channel we have: an LUT for phase control with an accuracy of 1°, an LUT for the insertion loss relative

TABLE 7. Amplifier Gain Control Accuracy and Channel Phase Shift Relative to the Desired Gain Setting

Desired Gain	Expected Phase	Meas. Gain	Meas. Phase
0.5 dB	1.2°	0.5 dB	1°
2.0 dB	3.8°	2.1 dB	4°
3.0 dB	5.5°	2.9 dB	6°
3.5 dB	6.5°	3.5 dB	7°

to the phase setting of the PS. There is an LUT for the amplifiers gain control as well as an LUT for the phase shift incurred by the amplification. This knowledge allows us to create a calibrated system which can compensate for the PS insertion loss and the VGAs inherent phase shift. This can support a highly accurate self-calibrated phased array with minimal errors present, and these errors can be brought about by the employed active component within the channels which are susceptible to drift.

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Zain Shafiqwas born in Edinburgh, Scotland in 1996. He received his B.Eng. degree from Heriot-Watt University, Edinburgh in 2018 and completed his Ph.D. in 2023 while studying at this same university as well as The University of Edinburgh, while also, completing multiple industrial internships. His PhD research was co-funded by the EPSRC Doctoral Training Programme in Embedded Intelligence. His research interests focuses on using RF circuits and electronic hardware to characterize and self-calibrate for any magnitude and phase errors in phase array antennas and thus mitigating unwanted channel imbalances.

DIMITRIS E. ANAGNOSTOU (Senior member, IEEE) received the B.S.E.E. degree from the Democritus University of Thrace, Greece, in 2000, and the M.S.E.E. and Ph.D. degrees from the University of New Mexico, Albuquerque, NM, USA, in 2002 and 2005, respectively.

From 2005 to 2006, he was a Postdoctoral Fellow with the Georgia Institute of Technology, Atlanta, GA, USA. In 2007, he joined as an Assistant Professor with the South Dakota School of Mines and Technology, Rapid City, SD, USA, where he was promoted to an Associate Professor with tenure. In 2016, he joined the Institute of Signals, Sensors, and Systems, Heriot-Watt University, Edinburgh, U.K., where he is currently an Associate Professor. He has also worked with Kirtland AFB, NM, USA, in 2011 as an AFRL Summer Faculty Fellow, and with the Democritus University of Thrace as an Assistant Professor. He has authored or coauthored more than 150 peer-reviewed journal and conference publications, and holds two U.S. patents on MEMS antennas and on optically scannable antennas. His research interests include reconfigurable antennas and arrays, miniaturized and electrically small antennas, antennas for wearable, and space/satellite applications, radars and wireless sensing for assisted living, microwave circuits and packaging, functional phase-change materials such as VO_2 for reconfigurable electronics, direct-write electronics on organics, RF-MEMS, and applications of artificial neural networks, deep learning and signal processing in electromagnetics and healthcare.

Dr. Anagnostou has received the 2010 IEEE John D. Kraus Antenna Award, the 2011 DARPA Young Faculty Award by the U.S. Department of Defense, the 2014 Campus Star Award by the American Society for Engineering Education (ASEE), the 2017 Young Alumni Award by the University of New Mexico, and four Honored Faculty Awards by SDSMT. Most recently, he received the prestigious H2020 Marie Skłodowska-Curie Individual Reintegration Fellowship (MSCA-IF-RI) for research on wireless vital sign monitoring. His students have also been recognized with IEEE and university awards (Engineering Prize, HWU, Best Ph.D. Thesis, SDSMT, and other). He serves or has served as an Associate Editor for the IEEE Transactions on Antennas and Propagation from 2010 to 2016 and the IET Microwaves, Antennas, and Propagation since 2015. He was a Guest Editor of IEEE Antennas and Wireless Propagation Letters (Special Cluster on Antennas Using Advanced Materials). He is a member of the IEEE AP-S Educational Committee, and of the Technical Program Committee of the IEEE AP-S International Symposia. He is a member of the HKN Honor Society, ASEE, and of the Technical Chamber of Greece (registered Professional Engineer).

SYMON K. PODILCHAK (Member, IEEE) received the B.A.Sc. degree in engineering science from the University of Toronto, Toronto, ON, Canada, in 2005, and the M.A.Sc. and Ph.D. degrees in electrical engineering from Queen's University, Kingston, ON, Canada, in 2008 and 2013, respectively.

He was an Assistant Professor with Queen's University from 2013 to 2015. In 2015, he joined Heriot-Watt University, Edinburgh, U.K., as an Assistant Professor, and became an Associate Professor in 2017. He is currently a Senior Lecturer with the School of Engineering, The University of Edinburgh, Edinburgh. He was a Lecturer with the European School of Antennas. He has had industrial experience as a computer programmer, and has designed 24 and 77 GHz automotive radar systems with Samsung and Magna Electronics. His recent industry experiences also include the design of high frequency surface-wave radar systems, professional software design and implementation for measurements in anechoic chambers for the Canadian Department of National Defense and the SLOWPOKE Nuclear Reactor Facility. He has also designed compact antennas for wideband military communications, highly compact circularly polarized antennas for CubeSats with COM DEV International (now Honeywell) and The European Space Agency, and new wireless power transmission systems for Samsung. His research interests include surface waves, leaky-wave antennas, metasurfaces, UWB antennas, phased array antenna systems, and RF integrated circuits. These activities have resulted in several patents and more than 200 peer-reviewed journal and conference publications.

Dr. Podilchak has been the recipient of many best paper awards and scholarships, most notably Research Fellowships from the IEEE Antennas and Propagation Society, IEEE Microwave Theory and Techniques Society (MTT-S), and five Young Scientist Awards from the International Union of Radio Science. He was also the recipient of a Fellowship from the Natural Sciences and Engineering Research Council of Canada. In 2012, he received the Best Paper Prize for Antenna Design at the European Conference on Antennas and Propagation for his work on CubeSat antennas, and in 2016, The European Microwave Prize for his research on surface waves and leaky-wave antennas. In 2017 and 2019, he was bestowed a Visiting Professorship at Sapienza University, Rome, Italy, and from 2016 to 2019, his research was supported by a H2020 Marie Sklodowska-Curie European Research Fellowship. In 2021, he was also the recipient of the COVID-19 Above and Beyond Medal for leading research on remote microwave sterilization of the coronavirus. Also, in 2011, 2013, 2020, and 2021, he and his students were the recipient of Student Paper Awards at the IEEE International Symposium on Antennas and Propagation. He was also the Founder and First Chairman of the IEEE AP-S and IEEE MTTS Joint Chapters in Canada and Scotland, in 2014 and 2019, respectively. In recognition of these services, he was presented with an Outstanding Volunteer Award from IEEE, and in 2020 and 2021 respectively, IEEE MTTS and AP-S recognized this Scotland Chapter for its activities and it was awarded the winner of the Outstanding Chapter Award hosted by these two IEEE Societies. He was also the recipient of the Outstanding Dissertation Award for his Ph.D. and a Registered Professional Engineer (P.Eng.). He was an Associate Editor for the IET Electronics Letters and a Guest Associate Editor for the IEEE Open Journal of Antennas and Propagation and IEEE Antennas and Wireless Propagation Letters. He is currently an Associate Editor for IEEE Transactions on Antennas and Propgation. He was also recognized as an Outstanding Reviewer for this same journal in 2014 and 2020.