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Hybrid Power Filter with Reduced Inverter Power Rating

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Abstract—This paper presents a novel hybrid filter configuration for mitigation of current harmonics. Proposed topology provides significant inverter power rating reduction. This topology is compared with a pure active solution and another hybrid topology used for the same type of non-linear loads. Both simulation and implementation results are presented. Currents and voltages measured in proper points are collected in tables to provide with useful knowledge and easily comparable data about analyzed topologies. The investigation shows that proposed circuit configuration together with the developed control algorithm provide significant reduction of the power rating and the cost of a hybrid power filter. The results obtained in simulations are proven by a laboratory analysis on a real system.

Index Terms—active filters; harmonic distortion; passive filters; power quality; power system harmonics.

I. INTRODUCTION

Many loads installed in power systems are classified as non-linear devices. This term includes: converters, electrical machines, arc furnaces, light sources. The operation of these appliances usually causes harmonic distortion of the electrical currents and voltages. In recent years, increasing number of non-linear loads installed in power systems results in the rise of harmonic distortion, which causes problems within the plants and the electrical power system [1], [2].

To mitigate these undesirable phenomena harmonic filters were designed, implemented and installed. Initially, shunt passive filters consisting of tuned LC branches were used. However, their limited efficiency, components aging, dependence on grid impedance and the rapid progress in high-speed power semiconductor switching devices resulted in increased interest in active filtering applications [3]. Active power filters offer better compensation features and are not so much dependent of the power system modifications [4]. Their main disadvantage is that the cost of power electronic inverters is high, especially for high power ratings [5]. Therefore, another harmonic mitigation solution - hybrid topologies were investigated and introduced. These devices combine the advantages of passive and active filtering. Moreover, they are free from drawbacks related with the earlier mentioned filtering approaches. They offer independence of the grid parameters and good efficiency for significantly lower cost than active filters [6].

To examine different features of hybrid filters various topologies were investigated. The detailed results of this study are discussed in [7]. The way active and passive filters are

connected has an influence on the application cost and compensation accuracy. Some hybrid devices are not optimized in terms of investment cost. The potential solution to these problems is a hybrid topology with a proper connection between the filters. By applying specific circuit configuration and developing filter control algorithm, inverter power rating can be minimized. This solution will potentially result in good current harmonics mitigation effectiveness and significant device cost reduction.

In this research a novel hybrid power filter topology was developed and examined. The active filter is inserted between the capacitors and inductors of the shunt passive filter tuned for the 4.6 harmonic order (as shown in Fig. 1). This configuration offers good harmonic mitigation performance for a lower cost than other solutions. The main goal of the study is to prove that this connection provides a considerable reduction of inverter power rating by decreasing both its line current and line-to-line voltage.

This paper is aimed to present the hybrid filter topology from the point of view of inverter power rating reduction and harmonic mitigation effectiveness. The paper is organized as follows: first the theoretical considerations related with electrical circuit theory are given, then the novel control algorithm is presented, simulation and implementation results and conclusions are provided at the end. Comparison with two other topologies: a shunt active filter and hybrid topology consisting of active filter and shunt passive filter connected in series (see Fig. 3) compensating for 10 kVA (for simulations) and 3 kVA (for laboratory tests) load is carried out.

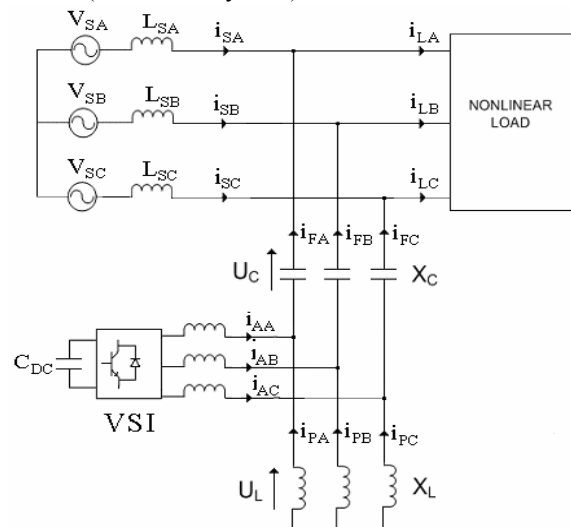


Fig. 1. Analyzed hybrid power filter topology. The active part is a voltage source inverter (VSI) connected between the passive components.

II. THEORETICAL CONSIDERATIONS

In considerations regarding a hybrid power filter for a current source load (in this case a 6-pulse diode rectifier) the most common choice is a connection of a shunt passive power filter and a shunt active power filter [8]. However, the circuit configuration of the filter can be chosen in different ways, providing different topologies.

In a case of improving the harmonic mitigation performance of a classical passive power filter or pure active solution, a separate connection to the grid of both filters (as shown in Fig. 2) is beneficial. As both filters are connected to the grid independently, such topology does not require any changes in the devices or the system. The passive filter sinks the most of the harmonic current, providing good conditions for the active filter to improve the compensation accuracy but with reduced power rating in comparison with pure active solution working alone. However, this topology is not the best in terms of cost. The main reason is that the inverter has to work against the full line voltage, like in the case of a pure active filter, what results in higher voltage rating of the semiconductor switches.

A possible solution to this problem is a series connection of the passive and active power filters, as shown in Fig. 3. In this topology the fundamental frequency component voltage drops on the capacitor of the passive filter, since it presents high reactance for low frequencies. At higher frequencies the voltage drop on the capacitor is low. As fundamental component voltage drops on the capacitor, the inverter has to work against a lower line voltage (dominant fundamental frequency component). It means that the required voltage rating of the inverter is significantly reduced. However, as both filters are connected in series, the full passive filter current flows into the power electronic inverter, what makes it necessary to use high current-rated semiconductor switches. As the inverter voltage is reduced but the current is increased, this solution is not optimal for the power rating of the inverter.

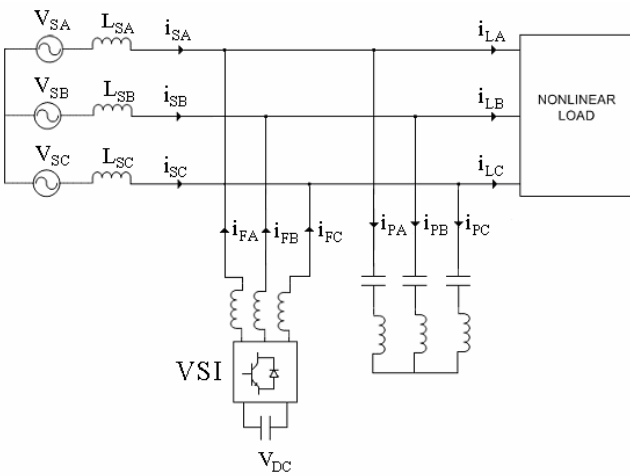


Fig. 2. Hybrid topology consisting of shunt passive and shunt active filter connected separately to the grid.

To eliminate the mentioned disadvantage of a shunt connection of filters – high inverter current, another solution was proposed [9]. This solution was based on connecting the active power filter between the inductors and capacitors of the passive filter using a matching transformer. However the transformer is the most bulky part of the power filter and increases the cost. Therefore, in this research a novel topology is analyzed. This paper presents a hybrid power filter with inverter connected in shunt with passive power filter inductors without a matching transformer as shown in Fig. 1. In this topology low frequency harmonic currents do not flow into the inverter, as a low-impedance path for these currents is provided by the tuned passive branch. This circuit configuration eliminates disadvantages of other proposed topologies. The fundamental frequency voltage drop on passive filter capacitors lowers significantly the rated voltage of the power electronic converter. The additional path provided by the passive tuned branch sinks the harmonic current, what results in the lower current rating of the inverter. With the reduction of both voltage and current rating of the inverter, the overall cost of the harmonic filter is significantly lower.

III. CONTROL ALGORITHM

The control part of the filter has been initially designed and simulated in Matlab Simulink and then implemented using Real Time Workshop libraries for TMS320 DSP. The control block of the proposed topology is shown in Fig. 4. Regarding which harmonic current detection method to apply, frequency-domain methods were not taken into account as they require large computation power of the DSP, memory storage for samples and give unsatisfactory results under transient conditions [11].

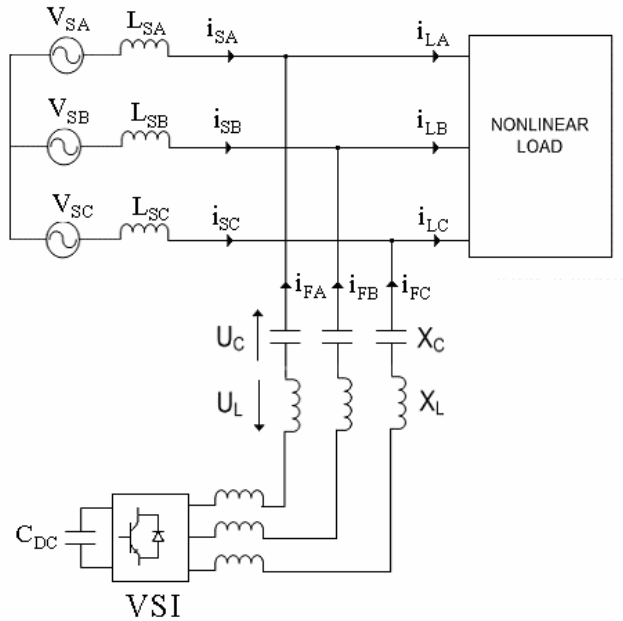


Fig. 3. Hybrid topology consisting of shunt active power filter and shunt passive power filter connected in series.

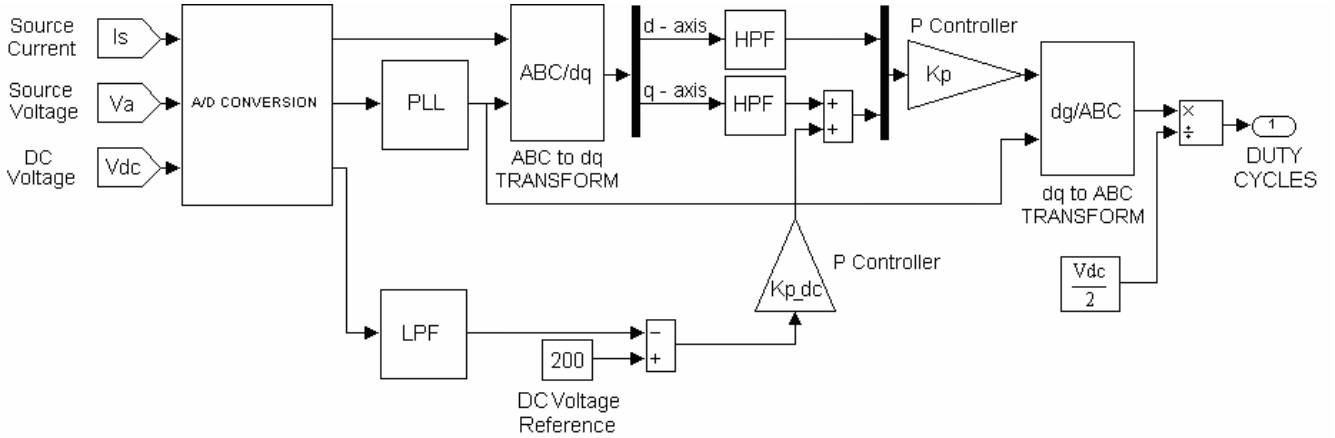


Fig. 4. Control block diagram.

Therefore, only time-domain methods were considered, namely synchronous dq-frame and instantaneous power theory [12]. The fact that instantaneous power theory requires sinusoidal input voltages makes the control more complicated and more difficult to implement than the dq-frame. The distortion of the current and the voltage comes together in an inseparable way, thus because of the current harmonics, voltages will also be distorted. Because the pq-theory requires pure sinusoidal voltage, the implementation would have to include voltage harmonics filtering. This would require additional numerical filters, what would result in more complicated control diagram and require a larger number of calculations made by DSP.

Therefore, synchronous reference frame has been used here as the harmonic detection method. It uses Park transformation of the input signals, which are collected in abc coordinates from the sensors (see Fig. 5). These signals are transformed into fundamental dq frame. Because d and q axes rotate anticlockwise with the fundamental frequency, in that reference system the fundamental frequency component is a DC signal and other frequencies are AC signals. To detect the harmonics it is necessary to remove the DC signal with high pass filter (HPF). However, the quality of detection is dependent on the characteristic of used HPF, as the filter causes a phase shift between the input and output signal. To solve the problem of phase error '1-LPF' filter has been applied. This resulted in proper harmonic current phase detection, what was necessary for effective harmonic disturbance mitigation.

The input signals are the source currents and voltages the DC-voltage. The output current signal representing the harmonic distortion is delivered to the proportional controller, hence it is amplified by the K_p coefficient. Additionally, source voltage needed by the PLL and dc voltage required for capacitor charging control loop are measured.

Proportional controller (K_p in Fig. 5), used in current control loop provides fast response. This value has been set to 80. The DC-voltage control loop was designed using similar method to the one proposed in [10].

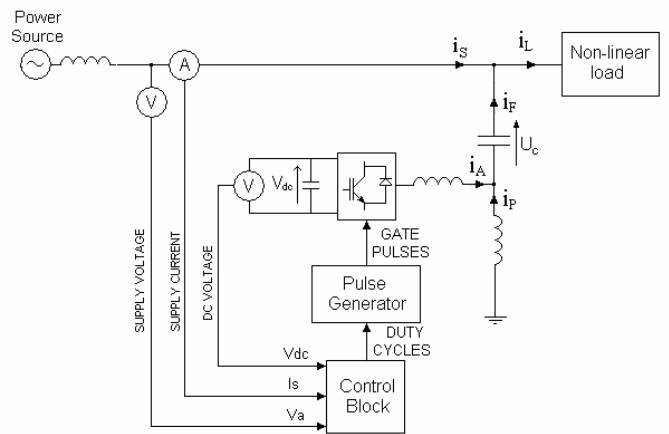


Fig. 5. Hybrid filter sensors layout.

In order to charge the DC capacitor to the desired value of the voltage, some active power must be provided to the inverter. This active power is formed by the leading fundamental frequency current and the fundamental component of the line voltage. In the presented topology, the line current is phase shifted by 90° to the voltage. In dq stationary frame, the current that is phase-shifted with the grid voltage by 90 degrees, is represented in q-axis and for that reason the dc control loop should be connected to this axis. What is important is that the gain of dc voltage controller (K_{p_dc}) should be considerably lower than the gain used in the main control circuit (K_p). That is because capacitor voltage value is changing much slower than the load current, which is controlled in the main circuit. By setting different gains for the current and voltage loops their decoupling is obtained, thus the design of both loops can be done independently. Finally, proportional gain (K_{p_dc} in Fig. 4) was set to the value of 0.1 resulting in the DC-voltage as shown in Fig. 6 for a step of 200 V. Regarding DC-voltage, this value depends mainly on the voltage drop on the capacitor (C in Fig. 1). The best simulation results were obtained for 200V and such a constant value is used as a reference for the proportional controller. The steady state ripple is low (see Fig.

7), hence it is easier for the hybrid filter to mitigate the harmonic distortion of the load current. Desired voltage value is achieved after reasonable time and the first voltage overshoot is low, what prevents the inverter from over-voltage stress during switching on the hybrid power filter.

The output signal is divided by the half of the dc voltage value, in order to maintain the duty cycles below 1.

IV. SIMULATION RESULTS

Simulations were performed for three different current harmonic compensation devices: shunt active filter (APF) shown in Fig. 8, hybrid topology consisting of shunt active and passive filters connected in series (series HPF) shown in Fig. 3 and proposed topology (proposed HPF) shown in Fig. 1. The results are gathered in Table 1 - Table 4.

For both simulation and implementation passive filter in series HPF and proposed HPF was tuned to 4.6 harmonic order (230 Hz). It has not been tuned to the exact 5th harmonic order because of the capacitor aging (capacitance decrease), what increases resonance frequency.

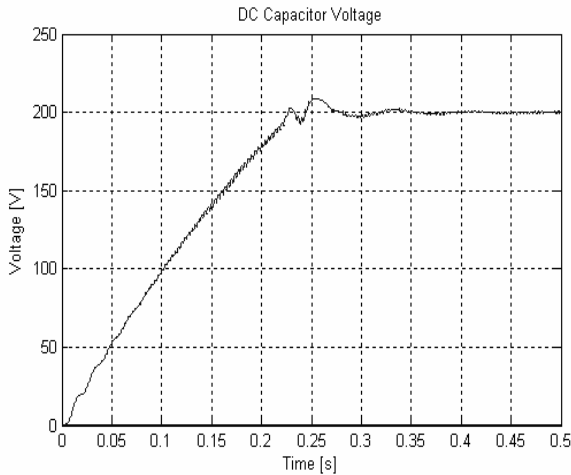


Fig. 6. DC-voltage after switching on the filter.

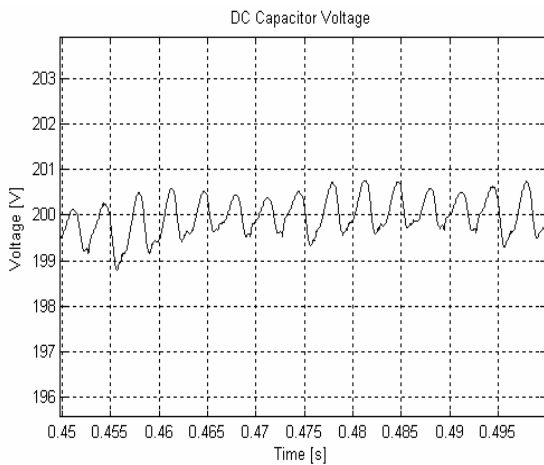


Fig. 7. Dc voltage ripple in steady-state conditions. The ripple value is maximum 2 V, what is 1% compared to the DC reference.

Additionally, tuning to 4.6 harmonic order minimizes the possibility of unwanted harmonic resonance, which may take place if system parameters change. These three filter topologies were simulated for the same load – 10 kVA 3-phase diode rectifier. The rectifier drains current $i_L=16A$ RMS current with 24.8% THD from the system. The RMS value for 5th harmonic is $i_{L5}=3.2$ A and $i_{L7}=1.8$ A for the 7th (see Table 1). These values are the same for all the filters as they are load-dependent only.

After the compensation, the system current is around $i_S=15A$ in all 3 cases with THD 4.6% for the APF, 0.1% for series HPF and 3.4% for proposed HPF (see Table 2). The 5th and 7th harmonic source currents - i_{S5} , i_{S7} are less than 0.5 A in all cases.

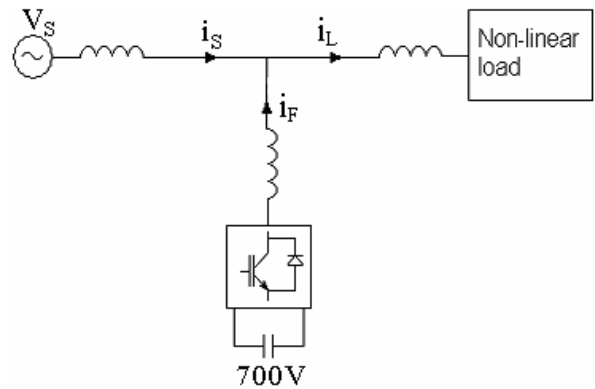


Fig. 8 One phase diagram of the active filter.

Table 1. Load current and voltage RMS values and THD value obtained in simulation.

| | APF (Fig. 8) | series HPF (Fig. 3) | proposed HPF (Fig. 1) |
|---------------|-----------------|------------------------|--------------------------|
| i_L [A] | 16.5 | 16.0 | 15.9 |
| i_{L1} [A] | 15.6 | 15.5 | 15.5 |
| i_{L5} [A] | 3.2 | 3.2 | 3.2 |
| i_{L7} [A] | 1.8 | 1.8 | 1.8 |
| i_L THD [%] | 24.8 | 24.8 | 24.8 |
| V_L [V] | 231.0 | 229.3 | 229.3 |

Table 2. Supply current and voltage RMS values and THD value obtained in simulation.

| | APF (Fig. 8) | series HPF (Fig. 3) | proposed HPF (Fig. 1) |
|---------------|-----------------|------------------------|--------------------------|
| i_S [A] | 15.5 | 14.8 | 15.3 |
| i_{S1} [A] | 15.9 | 15.2 | 15.3 |
| i_{S5} [A] | 0.1 | 0.1 | 0.4 |
| i_{S7} [A] | 0.3 | 0.1 | 0.2 |
| i_S THD [%] | 4.6 | 0.1 | 3.4 |
| V_S [V] | 231.0 | 229.3 | 229.3 |

Table 3. Filter current and voltage RMS values obtained in simulations.

| | APF (Fig. 8) | series HPF (Fig. 3) | proposed HPF (Fig. 1) |
|--------------|-----------------|------------------------|--------------------------|
| i_F [A] | 4.0 | 6.0 | 5.9 |
| i_{F1} [A] | 0.4 | 4.6 | 4.4 |
| i_{F5} [A] | 3.1 | 3.2 | 3.2 |
| i_{F7} [A] | 1.8 | 1.8 | 1.8 |
| V_F [V] | 231.0 | 52.5 | 37.0 |

However, the filter i_F current RMS value differs depending on applied topology. For the APF it is $i_F=4A$ and for hybrid devices its value is $i_F=6A$ (see Table 3). The difference in values comes from the fact that APF current contains less fundamental frequency component. That is because of the fundamental frequency voltage drop on the passive filter capacitor in hybrid topologies. To provide the dc-capacitor with the power, the current must be increased while the voltage is reduced. This current (i_F) for the APF and series HPF, current i_A for the proposed HPF are the inverter currents that flow through the semiconductor switches (see Table 3 and Table 4). Thus, the requirement for the current rating of the inverter's switches is dependent on that current. According to the simulations, the values are $i_F=4A$ for the APF, $i_F=6A$ for the series HPF and $i_A=3A$ for the proposed HPF.

The conclusion is that the current value is bigger in series HPF than in active power filter as APF drains less fundamental frequency, while the 5th harmonic currents are almost the same. It is the lowest in proposed HPF because almost the whole 5th harmonic current is flows into the path provided by inductors ($i_p=2.8A$). The proposed HPF inverter current contains bigger amount of fundamental frequency component than in APF ($i_{A1}=2.5$) but very low amount of 5th harmonic current ($i_{A5}=0.2$). In addition, the 7th harmonic current value is also reduced (APF $i_{F7}=1.8$, series HPF $i_{F7}=1.8$ and proposed HPF $i_{A7}=0.9$). The conclusion is that the path for the 5th harmonic current provided by connecting the inverter between capacitors and inductors of the passive filter benefits with large inverter current reduction – it is halved in comparison with series connection of the filters and it is 25% less than in APF. It proves the theoretical considerations from the chapter I.

The data from the table proves that the presence of the capacitor decreases the value of the voltage applied to the inverter from $V_S=230V$ in APF to $V_F=52V$ in series HPF and $V_A=37V$ in proposed HPF (see Table 3). Moreover, in accordance to the series HPF this voltage contains only 15V fundamental frequency component, 33,6V 5th, 13.1V 7th, 5V 11th and 3V 13th harmonic.

This proves that the series connection provides significant inverter back voltage reduction because of the large fundamental voltage drop on the capacitor.

Table 4. Proposed HPF inverter currents and passive filter inductors currents RMS values.

| i_A [A] | i_{A1} [A] | i_{A5} [A] | i_{A7} [A] | i_p [A] | i_{p1} [A] | i_{p5} [A] | i_{p7} [A] |
|-----------|--------------|--------------|--------------|-----------|--------------|--------------|--------------|
| 2.9 | 2.5 | 0.2 | 0.9 | 3.8 | 2.2 | 2.8 | 0.8 |

Table 5. Inverter currents, voltages and ratings, supply current THD.

| | APF (Fig. 8) | series HPF (Fig. 3) | proposed HPF (Fig. 1) |
|--|-----------------|------------------------|--------------------------|
| Inverter RMS voltage [V] | 400 | 88 | 54 |
| Inverter RMS current [A] | 4 | 6 | 3 |
| Inverter power rating [VA] | 1600 | 528 | 162 |
| Inverter power rating / Load power rating [%] | 16 | 5.3 | 1.6 |
| Supply current THD [%] | 4.6 | 0.1 | 3.4 |

Table 6. Measured supply current THD.

| | Active | Series HPF | Proposed HPF |
|------------------------|--------|------------|--------------|
| Supply current THD [%] | 6.37 | 0.1* | 0.75 |

For the proposed HPF the values are $V_{A1}= 5V$ and 33,2V 5th, 13.1V 7th, 5V 11th and 3V 13th harmonic. The difference in RMS value between the two topologies comes from the presence of inter-harmonics in series topology.

The most important data is gathered in Table 5. It presents inverters currents, voltages and power ratings calculated according to (1).

$$S = V_{pp} \cdot I_A \quad (1)$$

where: V_{pp} - inverter phase-to-phase voltage, I_A - inverter phase current.

As it can be seen in Table 5 the power rating of the inverter has the lowest value in proposed topology. It is 10 times lower than in active filter and more than 3 times lower than in series hybrid topology. It has been achieved by reducing both current and voltage of the inverter. The voltage in proposed topology is almost 8 times lower than in active filter while the current is reduced by 25%. The series hybrid topology has a voltage 4 times lower than in active filter but it suffers from 50% bigger current as the passive filter current flows into the inverter. The power rating of the inverter is 16% of the load rating in the case of active filter, 5.3% for series hybrid topology and 1.6% for the proposed topology.

The theoretical considerations from chapter I were verified and simulations have proved that both current and voltage rating of the inverter can be reduced by applying proposed hybrid filter topology.

V. IMPLEMENTATION

Laboratory tests were performed for APF and proposed HPF compensating for 3-phase 3kVA diode rectifier. The active power filter DC-voltage is 700 V, current RMS is 1 A. For the proposed HPF the DC-voltage is 100 V and the current RMS value is 2 A. The laboratory setup diagram for the proposed HPF is shown in Fig. 9. The implementation has been made using Real Time Workshop and dSpace. Control Desk software was used for controllers parameters design, optimization and filter function analysis.

Compensation effectiveness – supply current THD is presented in Table 6 (* - simulation result for series HPF).

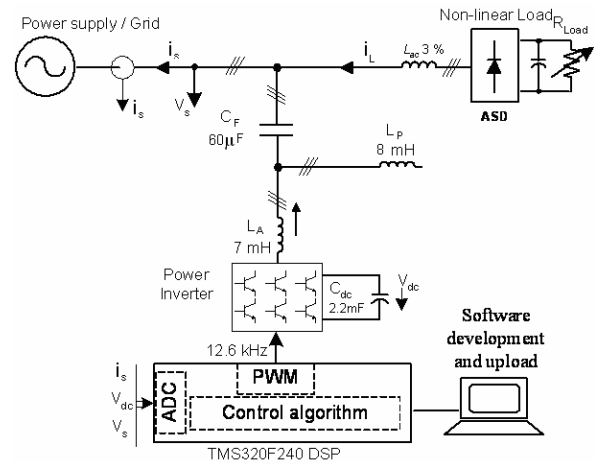


Fig. 9. Laboratory test setup for proposed HPF.

0.75%. Inverter power rating has been significantly reduced.

VI. CONCLUSION

In this paper a novel hybrid power filter was described. The paper presents simulation and implementation results, which prove that the proposed HPF topology provides significant inverter power rating reduction and high harmonic mitigation effectiveness. Inverter power rating reduction was achieved by applying hybrid filter topology which reduces both voltage and current ratings of semiconductor switches. Moreover, the reduction has been obtained by applying improved control algorithm. This resulted in significant cost reduction, as the power rating of the inverter is the most important factor, which influences the cost of the filter. The paper shows that the investigated novel topology provides an efficient and cost-effective solution for current harmonics mitigation.

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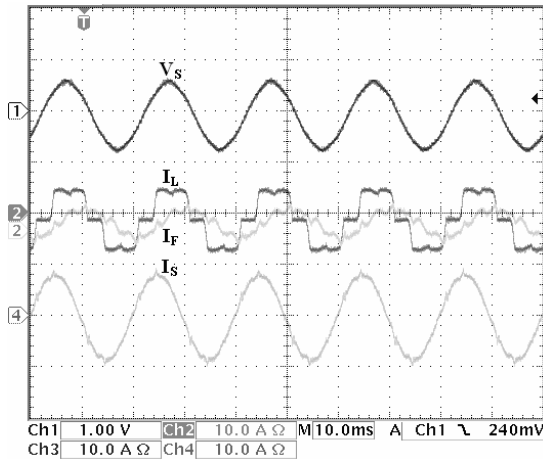


Fig. 10. Measured waveforms for the proposed HPF in steady state: supply voltage – '1', filter current – '2', load current – '3' and source current – '4' waveforms in steady state operation.

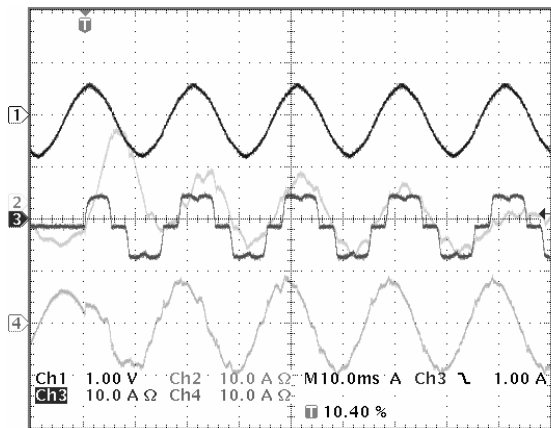


Fig. 11. Measured waveforms for the proposed HPF in transient conditions: supply voltage – '1', filter current – '2', load current – '3' and source current – '4' waveforms in steady state operation.

Obtained waveforms for the steady state are presented in Fig. 10. It can be seen that source voltage V_s lags behind the filter current I_f . That is because of capacitive character of the current I_f – it compensates inductive reactive power of the load. Fundamental component of this current is 5.8A RMS. For the active filter it is lower – 4.4 A RMS. It confirms simulation results, higher value of the fundamental current component is needed to charge the DC-bus capacitor in proposed HPF than in APF. Since the fundamental voltage component is reduced by the voltage drop on the passive filter capacitor, to provide active power for the DC side, higher fundamental current is required.

Fig. 11 presents proposed HPF operation under transient conditions. It can be noticed, that the steady state is achieved after 5 fundamental frequency cycles, the value of the filter current is higher in the first cycle after switching on the load.

The simulation results have been proven. DC-bus voltage was 7 times lower than in an APF, while the compensation effectiveness was higher – supply current THD was only