2nd order Incremental Data Weighted Averaging (IDWA) Technique to Reduce In-band Tones of an 8-bit Digital-to-Analog Convertor (DAC)

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ABSTRACT

A second order of IDWA (Incremental data weighted averaging) technique is proposed to improve 8-bit digital-to-analog convertor (DAC). In addition, this paper discusses the impact of mismatch between DAC unit elements. The Proposed IDWA/8-DAC circuits, which results in a completely second order mismatch noise shaping while solving in band tone problem. The simulation results show the effectiveness of the IDWA technique in reduction of inband tones, also IDWA technique proves its ability to solve DAC unit elements mismatch. The inband tones are converted into a broadband. It was found that IDWA algorithm proves its ability to solve this problem. The inband tone reduction is improved 8 dB if, element mismatch, σ=0.01 and 7 dB if σ=0.08 with proposed IDWA, thus improving the DAC performance if compared with DAC performance without using IDWA circuit. MATLAB (V.7.12) program is used for simulation.

Keywords: Digital-to-Analog converter (DAC), DAC mismatch, Dynamic Element Matching (DEM), Incremental Data Weighted Averaging (IDWA) technique.

أستخدام خوارزمية البيانات المتوسط المرجح التزايدي من الدرجة الثانية لتقليل مستوى نغمات داخل الحزمه لمحول الاشارة الرقمية الى التماثلية

الخلاصة

يتضمن هذه البحث مقتراح لأستخدام خوارزمية(البيانات المتوسط المرجح التزايدي) من الدرجة الثانية لتحسين أداء محول الاشارة الرقمية الى التماثلية(8-Bit DAC). اضافة الى ذلك تم مناقشة مشكلة عدم التوليف بين عناصر محول الاشارة الرقمية الى التماثلية (DAC). نتائج المحاكاة بينت فعالية تقنية (البيانات المتوسط المرجح التزايدي) في تقليل مستوى نغمة داخل الحزمة وكذلك التغلب على مشكلة عدم التوليف بين عناصر (DAC). تم تخفيض قيمة نغمة داخل

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الحزمة بمقدار (8 dB)عندما يكون قيمة عدم التوليف (σ =0.01) ومقدار (7 dB) عندما يكون قيمة عدم التوليف (σ =0.08). تم أستخدام برنامج MATLAB (V.7.12) في عملية المحاكاة.

INTRODUCTION

New Consumer formats such as digital video disc are pushing the performance of audio digital-to-analog (DAC) converters to higher and higher levels. Digital-to-analog converters with very high dynamic range and very low cost are now in demand [1]. The main requirement of DACs for these applications is good linearity, which implies high spectral purity and small output errors. To maintain good linearity, trimming and calibration have been used to directly decrease element mismatches that result in high spurious-free dynamic range (SFDR) and small maximum output errors. Another technique called dynamic element matching (DEM) has been successfully applied to reduce the correlation of DAC noise to the input signal for achieving high SFDRs. Randomization, which is one of the DEM techniques, is mostly used for Nyquist-rate DACs to spread the harmonics as white noise over the output spectrum. However, the possible maximum output errors of randomization are still large because the elements are selected randomly [1].

The DEM schemes are implemented with unitary elements steering DACs. The way the elements are selected gives the name to the algorithm, and this result in a given characteristic of dynamic matching. Some of the most important are: Individual Level Averaging (ILA), Clocked Averaging (CLA), Random Averaging, and Data Weighted Averaging (DWA). One of the simplest DEM scheme is the DWA which selects the unitary elements cyclically. The main characteristic of the DWA is the capability to shape the spectrum of the mismatch error as a first order high-pass filter [2], the components of the quantization noise and the DAC noise outside of the signal band in Figure (1a) will be removed by the filter but much of the DAC noise will be in band. Using noise-shaping DEM techniques results in DAC noise that pushes DAC noise outside the signal band as illustrated in Figure (1b). However, the DWA can cause significant baseband tones, resulting in reduction of SDM performance. Although the tone problem can be circumvented by rotated DWA and bi-directional DWA, these techniques contribute additional noise to the baseband and result in the degradation of first-order DAC noise shaping. To increase DAC noise shaping ability, several second-order mismatch-shaping techniques have been proposed, but very complex implementation is needed and circuit speed is limited. A very efficient technique, referred to as incremental data weighted averaging (IDWA) algorithm, for moving DAC tones away from the baseband without increasing baseband noise. IDWA can achieve ideal first-order mismatch shaping [3]. In this paper, a second order noise shaping is proposed for the implementation of the IDWA/8-bit DAC.

PRINCIPLE OF IDWA ALGORITHM

To illustrate the principle of IDWA, a 4-bit DAC example is shown in Figure (2) where 17 unit elements are used, instead of 16 for a conventional DWA/DAC.

IDWA algorithm operates like a conventional DWA, in which DAC elements are selected in a circular way. Moreover, in IDWA, one extra element is added to shift the notable tones away from the baseband. The baseband tones are closely correlated to the number of unit elements used in the DAC. For N+K elements used in the IDWA, where N is the original DAC element number and K is the number of added extra element(s), the tones are shifted to, as equation (1) [3,4]:

$$f_{tone} = \frac{r}{2(N+K)} \times f_s \times m \text{, m=1,2,3……if N is odd} \quad \text{….(1)}$$

Where: r is the greatest common divisor (gcd) value of the number of N and the number of N+K.

Because tones can be moved to out-of-band, total in-band DAC noise power due to element mismatches can be lowered. Therefore, a careful choice of N and K can result in a DAC noise floor lower than the first-order shaping curve, $(1-Z^{-1})$, in the baseband.

DAC Elements (u_0,u_1,u_2,u_3... u_{15}) must be selected circularly based its consecutive input value (v). From one period to another, the status of selected elements is simply memorized by a pointer called Ptr.

As shown in Figure (3), input codes of DAC (8,8,10,9) are used as an example. In the beginning, the value of Ptr is 0, and the input of DAC is 9. The elements of DAC { $u_0,u_1,u_2,u_3,u_4,u_5,u_6,u_7$,} are selected according to the value of input. At the end of first cycle, the value of Ptr indicates the DAC elements (u_8). For the second input of DAC, the elements {$u_8,u_9,u_{10},u_{11},u_{12}, u_{13},u_{14},u_{15}$}are selected, and the value of Ptr indicates the DAC elements (u_0), and so on.

PROPOSED OF IDWA CIRCUIT

The proposed IDWA for an 8-bit DAC is illustrated in Figure (4). The code is converted to thermometer code (Binary-to-Thermometer code = (2^B + 1)). The algorithm cycles through the DAC elements by sequentially selecting the elements based are upon the input data. The DAC inputs produces an M+1 level signal v(n), which is fed into the mismatch-shaping logic block. The sv(n) output of the block contains M bits, each of which enables a particular unit element in the subsequent unit-element DAC. The number of elements enabled at each instant is equal to v(n).The element select logic (ESL) of Figure (4) selects elements in such a way that the mismatch error existing between those elements is noise shaped. The system shows that the output of the DAC is [5]:

$$DAC_{error} = (1 - z^{-1})^2 \text{ IM (Ptr (Z))} \quad \text{….(2)}$$

Where:

IM (Ptr (Z)) = Integral mismatch,

$(1-z^{-1})^2$ = Second order noise-shaping

$$IM(Ptr) = \sum_{i=0}^{Ptr-1} (U_i - U_{mean}) / U_{mean} \quad \text{....(3)}$$

$$= \frac{1}{N} \sum_{i=0}^{Ptr-1} De_i \quad \text{..... (4)}$$

Where: U_{mean} is the average value of the DAC unit elements, $U_{mean} = \frac{1}{N} \sum_{i=0}^{ptr-1} U_i$, U_i is the ith DAC unit element value, De_i is the DAC mismatch error ith DAC unit element, and $N=2^B+1$ = is the number of total DAC units.
The general form of DAC is:

$$Dv(z) = k.v(z) + (1-Z^{-1})^2 De(z) \quad \text{.....(5)}$$

Where k is the average element value, v(z) is the output of the DAC, De(z) is an error signal introduced by element mismatch, and $(1-Z^{-1})^2$ is a second order mismatch transfer function. The key point is that the error due to element mismatch is shaped by the $H(z) = (1-Z^{-1})^2$.

The flow chart of the program is shown in Figure (5).

SIMULATION RESULTS

The proposed 2nd order IDWA Circuit is used in 8-bit DAC circuit. The DAC is composed of (1 to 2^B+1) unit elements, where B is the number of bits in the DAC. In order to match the unit elements, the IDWA algorithm is used. Without IDWA enabled, the unit element mismatch leads to a large amount of tones feed-through. Figure (6) present the result of simulation for 8-bit DAC with 0.01 unit element mismatch (σ) without using proposed IDWA. Simulation show high tones at the output of the DAC. Figure (7) shows the result of simulation of proposed 8-bit DAC/2nd order noise shaping IDWA with (σ=0.01). In order to evaluate the impact of increase of DAC unit elements current sources mismatch on DAC performance, a suite of simulations was run with the DAC mismatch error set to 0.08, as shown in figure (8). Simulation results show that the high tone appears at the output of DAC.

To matching between the unit elements and suppressing tones of DAC, the proposed IDWA is used. Figure (9) shows the effectiveness of the proposed IDWA/DAC in reducing of tones. The IDWA technique proves its ability to solve DAC unit elements mismatch. The element mismatch error is converted into a broadband, shaped noise that appears to have the same profile as the quantization noise spectrum. Figures (10) and (11) show the maximum in-band tone reduction with a 0.01 and 0.08 mismatch DAC, is 8 dB and 7 dB respectively.

CONCLUSIONS

Mismatch between DAC elements is studied and shows that the tones level increase with increasing the mismatch between DAC elements. It was found that

IDWA algorithm proves its ability to solve this problem. The net improvement in inband tone reduction is founded 8 dB if σ=0.01 and 7 dB if σ=0.08 with proposed IDWA, thus improving the DAC performance if compared with DAC performance without using IDWA circuit.

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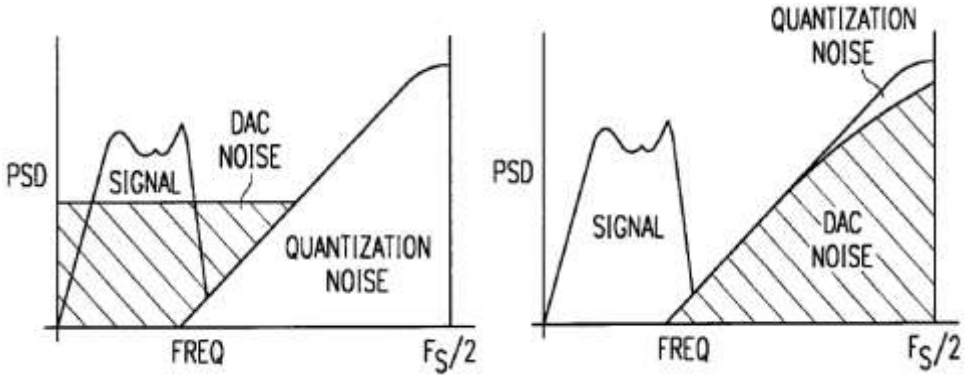

(a) **(b)**

Figure (1) typical power spectral densities at the output of the DAC (a) Without DEM, (b) with DEM algorithm.

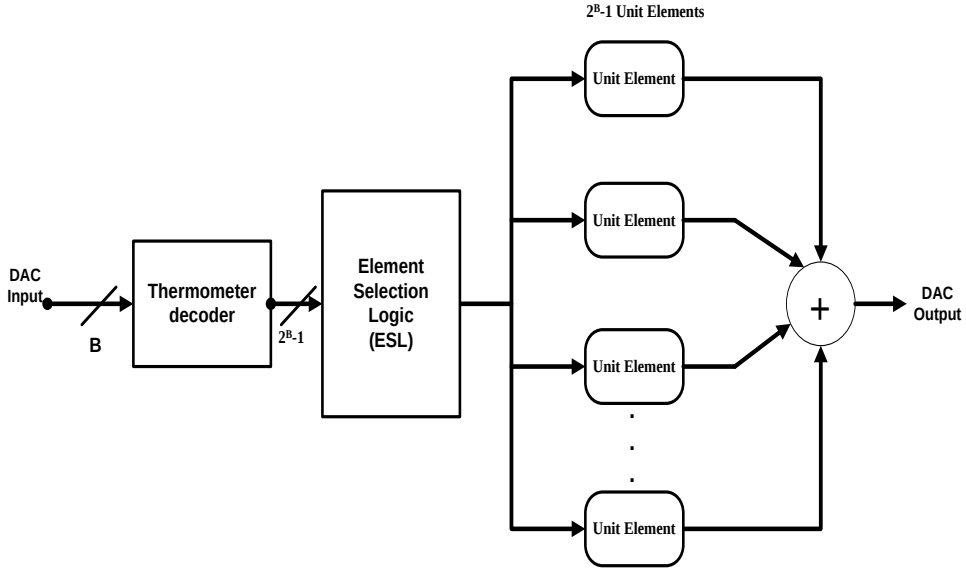

Figure (2) Traditional DWA circuit.

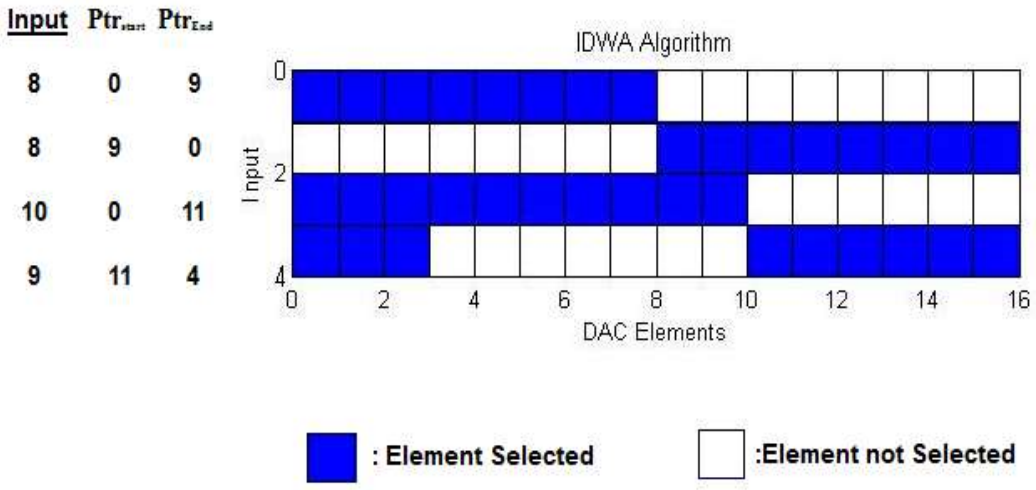

Figure (3) Simulation showing the IDWA operation for a 4-bit DAC.

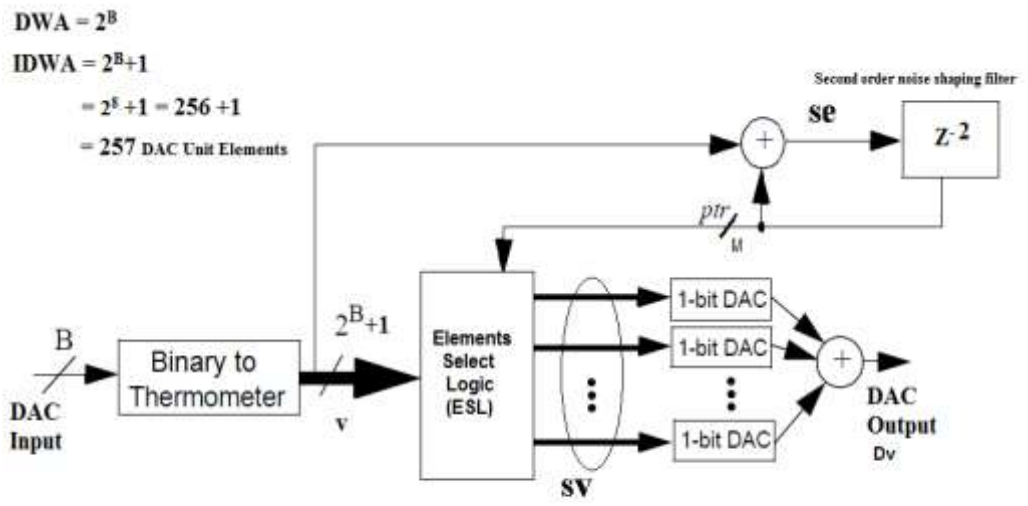

Figure (4) Proposed 2nd order IDWA algorithm for an 8-bit DAC.

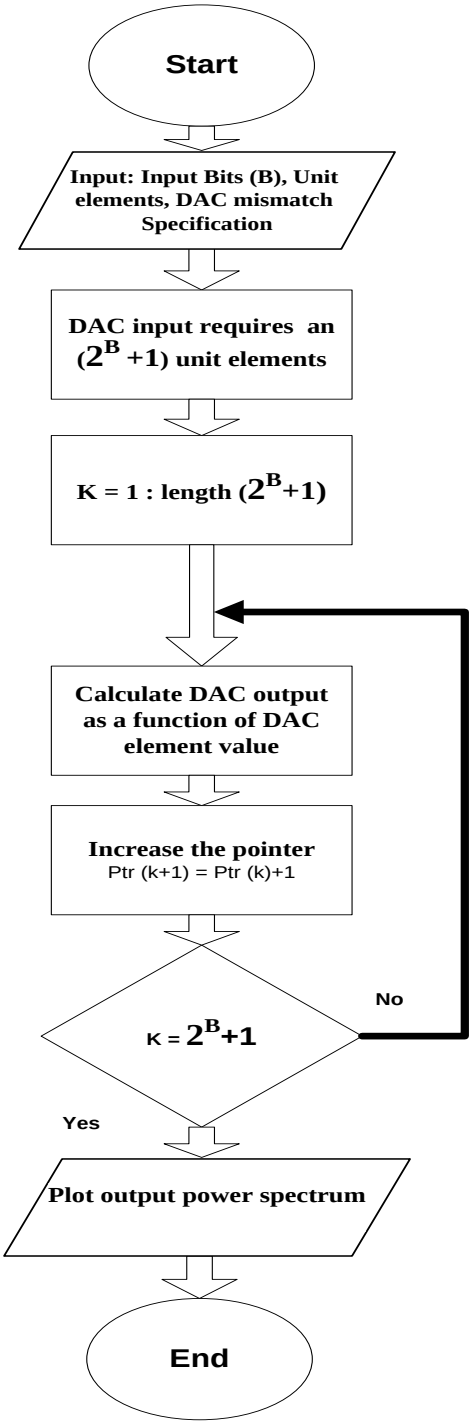

Figure (5) Flow chart of the IDWA algorithm.

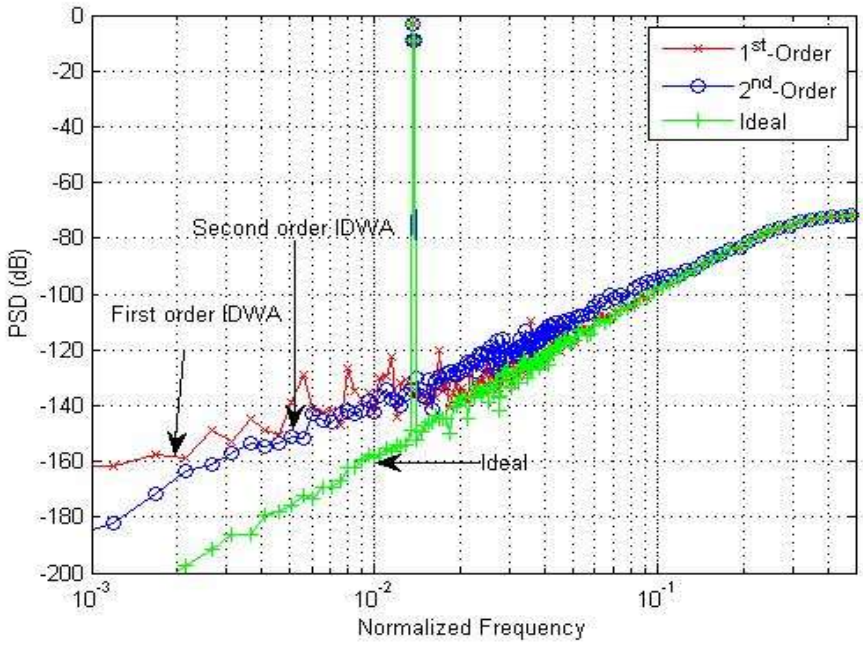

Figure (6) Simulation results showing the impact of 1st, 2nd, and ideal IDWA on the quantization noise spectrum for an 8-bit DAC (σ = 0.01).

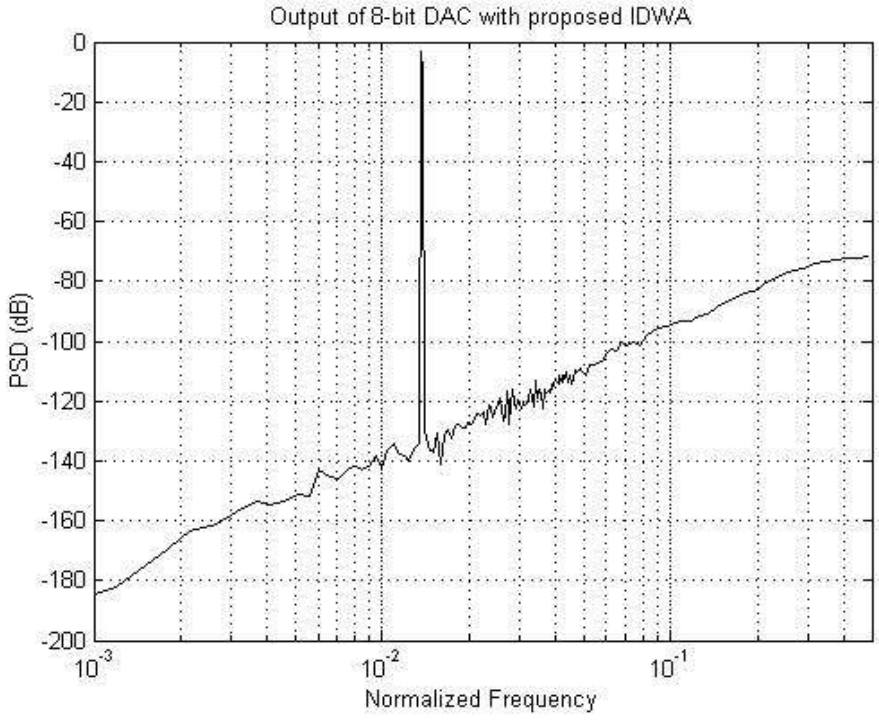

Figure (7) Simulation results showing the output of an 8-bit DAC with 2nd order IDWA (Elements mismatch error (σ) = 0.01).

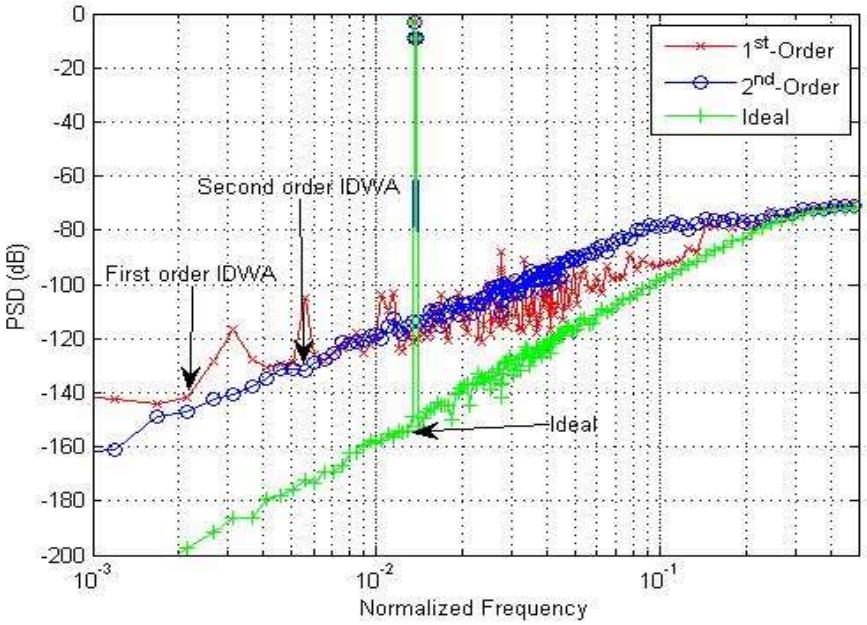

Figure (8) Simulation results showing the impact of 1st, 2nd, and ideal IDWA on the quantization noise spectrum for an 8-bit DAC (σ = 0.08).

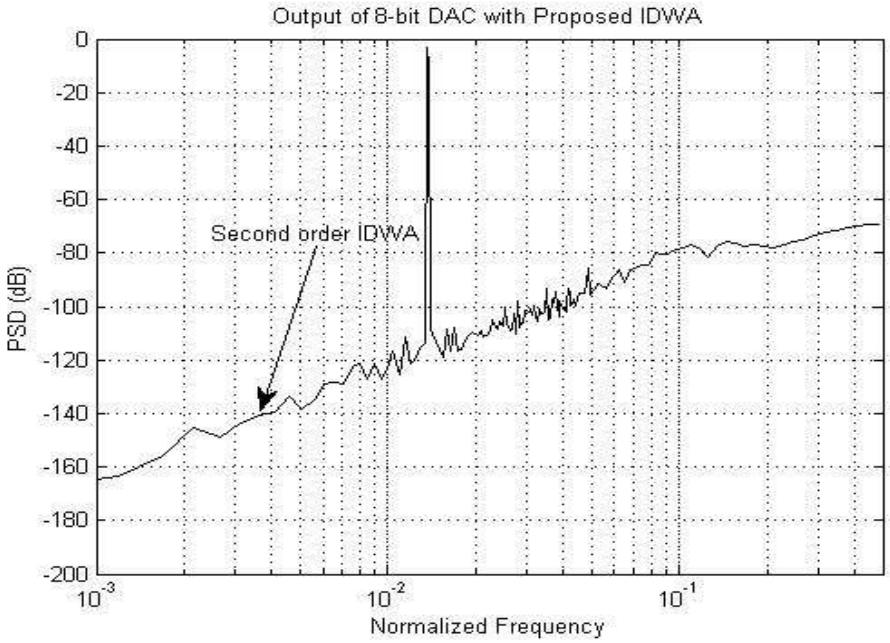

Figure (9) Simulation results showing the output of an 8-bit DAC with 2nd order IDWA ((Elements mismatch error (σ) = 0.08).

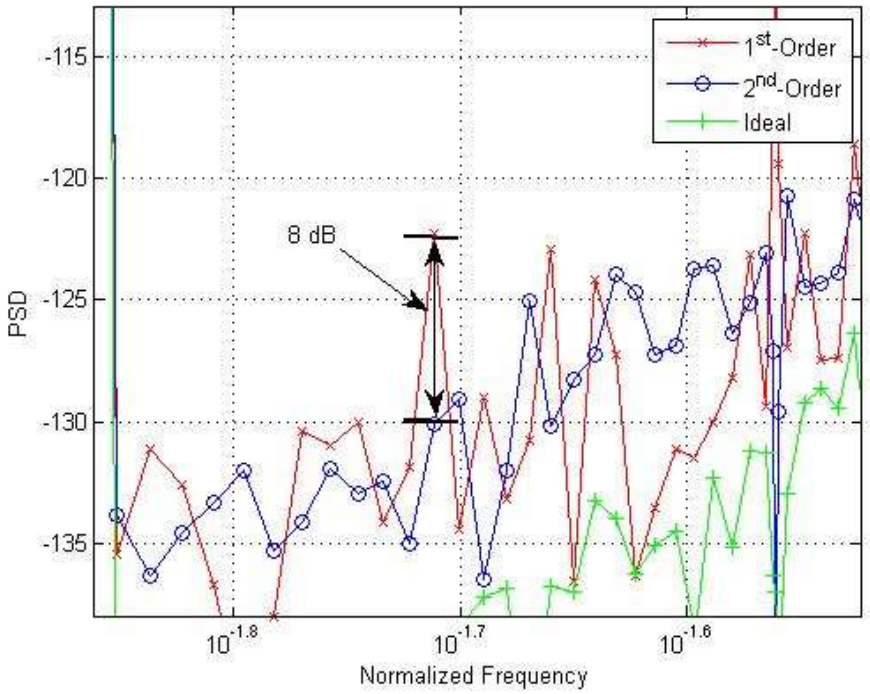

Figure (10) Simulation results showing the maximum in-band tone reduction with DAC mismatch (σ = 0.01).

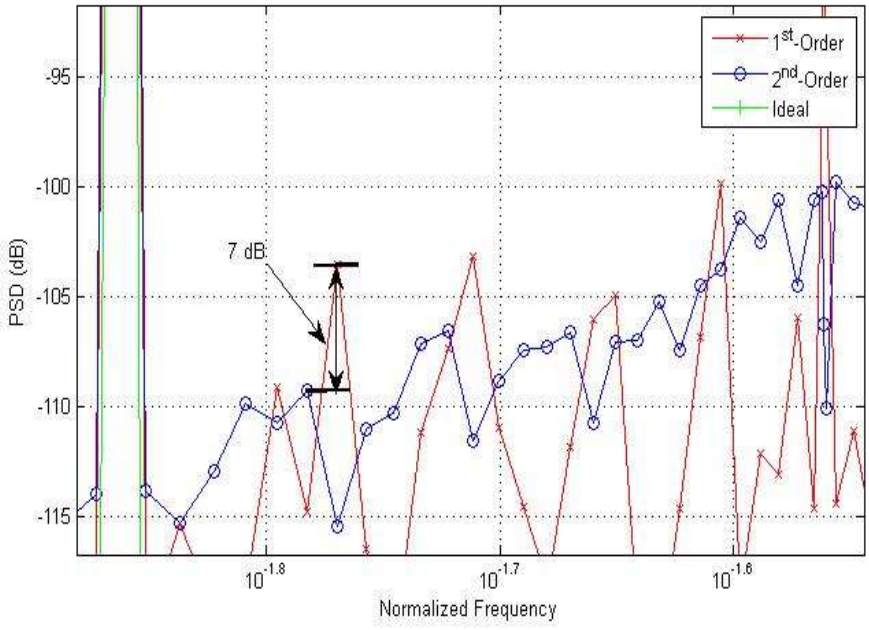

Figure (11) Simulation results showing the maximum in-band tone reduction with DAC mismatch (σ = 0.08).