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Design and Simulation of a Second-Order Universal Switched-Capacitor Filter as a 10-Pin Dual-In-Line Package Integrated Circuit

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ABSTRACT

This paper explains the design of a Universal (Low, High, Band and Notch) Second-Order Filter using switched capacitor (SC) technique. The design depends on the crystal oscillator circuit that generates two non-overlapping clocks by making full use of the two independent comparators of the LM741. The oscillator circuit is used to drive a switched-capacitor integrator which is used in the design of the universal second order filter. The circuit is performed as a single IC (Integrated circuit) which can be used for different standard applications. The proposed IC design differs than other IC's such as MF10 by adding the notch filter to this design for used in wide band of applications. The design is simulated using MultiSim 9 program.

Keywords: Filter, Switched-Capacitor, Crystal Oscillator

تصميم ومحاكاة مرشح عام من الدرجة الثانية كدائرة متكاملة مكونة من 10 أطراف باستعمال تقنية المتسعة المفتاحية

الخلاصة

يهدف هذا البحث الى تصميم مرشح عام (واطئ، عالي، حزمي، قاطع) من الدرجة الثانية باستعمال تقنية المتسعة المفتاحية. ويعتمد التصميم على استعمال دائرة مذبذب كريستال تقوم بتوليد اشارتين رقميتين غير متداخلة للسيطرة على تشغيل مقارنات من نوع LM741 بتقنية المتسعة

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المفتاحية والتي تدخل في تصميم المرشح. تم تمثيل الدائرة الالكترونية على شكل دائرة متكاملة تستعمل لتطبيقات مختلفة. إن الدائرة المتكاملة تختلف عن الدوائر المتكاملة الاخرى مثل MF10 باضافة المرشح القاطع اليها لاستعمالها في مدى اوسع من التطبيقات. تم استعمال الحقيبة البرمجية MultiSim 9 في اجراء المحاكاة.

INTRODUCTION

The essence of the switched-capacitor is the use of capacitors and analog switches to perform the same function as a resistor. This replacement resistor, along with operational amplifier based integrators, forms an active filter [1]. A capacitor can be implemented on a chip more easily than a resistor. Capacitors also offer other advantages such as no power dissipation [2]. The resistors and capacitors required for filter design may be fabricated on monolithic integrated circuits along with the op- amps but they usually require a large amount of area and are subject to temperature drift and annoying effects such as parasitic capacitance. The problem of component variation may be overcome with switched capacitor filters [3].These use small integrated circuit capacitors whose terminals are switched by a high frequency clock signal using MOSFET switches to simulate large values of resistance. The MOSFETs are fabricated on the same integrated circuit while the clock may be external or also resident on the integrated circuit. A MOS Transistor is a good switch with a small resistance when it conducts and as an open-circuit when it does not conduct [4]. Although switched-capacitor were developed in order to meet the need to incorporate analog active filters on silicon along with digital functions, they have since found many other uses. These include, besides filters, instrumentation amplifiers, voltage-to-frequency converters, data converters, programmable capacitor arrays, balanced modulators, peak detectors, and oscillator.

Erik Lauwers et al [5] is show how behavioral models are used to support system design. Models of two basic analog functions(operational amplifier and switch) are developed in Verilog-A and are used in the design of a first order switched capacitor low-pass filter, J. L. Ausin et al[6] described the design and implementation of a second-order switched-capacitor (SC) band pass filter with very wide quality factor(Q) programmability range. The filter selectivity is digitally programmed by varying the effective sampling frequency of an SC branch without modifying any capacitor value. Mingliang Liu [7] provided a design of low pass switched capacitor filter. Computer simulations are carried out to investigate how the circuitry non-idealities influence the performance of a switched-capacitor filter design. Optimum capacitance assignment techniques are also discussed that optimize the capacitor sizes and in turn to tight up the silicon chip area as well as the power budget. David Base-Lopez and Tomas Escalante [8] show a software package based in Matlab that simplifies the process of designing analog filters. The main menu and all the other required windows are programmed directly in Matlab.

Also, all the mathematical operations involved are done using Matlab. Bashir AL-Hashim [9] shows how commercially available SC devices are used to design sharp, frequency variable low pass filters. Norbert et al [10] are present a new second-order voltage and current mode universal biquadratic frequency filters using only single current convey or transconductance amplifier and four passive elements

SWITCHED CAPACITOR THEORY

Integrator

Figure (1) shows the switched capacitor incorporated into the op-amp integrator circuit [11]. The response of the integrator now depends on the ratio of two capacitor values, C_1 and C_F. It is relatively easy to fabricate two capacitors which have an accurately matched ratio and so the integrator is suitable for use in integrated circuit.

The clock signal $c(t)$ with frequency f_c and period $T_C = 1/f_c$ is applied to both the gate input of MOSFET M_1 and the digital inverter. When the clock is high MOSFET M_1 is ON and M_2 is OFF. Capacitor C_1 has the signal applied to the gate of MOSFET M_2 which is the complement of the clock. Hence, excepts for the switching transient, one MOSFET is ON while the other is OFF.

The duty cycle should be 50% so that the switch in each position is half of the period [2]. Two non-overlapping 100kHz, 50% duty cycle voltages that are 180^0 out-of-phase with each other are applied to the transistor switches as shown in igure(1).

When the clock is High, MOSFET M_1 is ON and M_2 is OFF. Capacitor C_1 has a charge $\Delta q = C_1 v_i$ placed on it by the input to the filter. If the clock frequency is large compared to the bandwidth of v_i the input may be considered to be constant during the sampling interval $T_C/2$. During the next clock half cycle, M_1 is OFF and M_2 is ON which places the top node of the capacitor C_1 at the virtual ground of the op-amp which causes the charge on it to be transferred to C_F. The average current flowing into capacitor C_1 is:

$$i(t) = \frac{\Delta q}{T_c} = \frac{C_1}{T_c} v_i = C_1 f_c v_i \qquad \ldots(1)$$

Which means that it is equivalent to a resistor $R_{eq} = 1/C_1 f_c$. The output of the op-amp is then given by[12]:

$$v_o = -\frac{1}{C_F}\int_{-\infty}^{t} i(u)du = -\frac{C_1 f_c}{C_F}\int_{-\infty}^{t} v_i(u)du = -\frac{1}{C_F R_{eq}}\int_{-\infty}^{t} v_i(u)du \qquad \text{--- (2)}$$

Which makes this circuit an integrator. Integrators are the heart of the state variable filter which means that any of the classical filters may be realized with this switched capacitor arrangement. The circuit in figure(1) illustrates the basic principle. The equivalent resistance being set as $R_{eq} = 1/C_1 f_c$, this makes controlling the critical frequencies of the filter elementary. The system clock sets the critical frequencies. Therefore, such filters may be easily electronically tuned.

Second Order Filter Categories

Because switched capacitor filters are digital circuits, the appropriate mathematical artifice to analyze them is the z- transform. However, classical frequency domain analysis is sufficiently accurate and more amendable to a mathematical tractable analysis.

a- Low-Pass Filter

The complex transfer function for a second-order low-pass filter is[13]:

$$T_L(s) = K \frac{1}{(\frac{s}{w_o})^2 + \frac{1}{Q}(\frac{s}{w_o}) + 1} \qquad \text{---(3)}$$

and $w_o = 2p.f_o$

where K is the gain of the filter, Q is the quality factor, and f_o is the resonant frequency of the filter. The magnitude of the complex transfer function is plotted in figure(2). The -3dB or half-power cutoff frequency f_c is the frequency at which the gain is reduced to $K/\sqrt{2}$ and is given by

$$f_c = f_o \sqrt{(1 - \frac{1}{2Q^2}) + \sqrt{(1 - \frac{1}{2Q^2})^2 + 1}} \qquad \text{---(4)}$$

b- High-Pass Filter

The complex transfer function for a second-order high-pass filter is[13]

$$T_H(s) = K\frac{(\frac{s}{w_o})^2}{(\frac{s}{w_o})^2 + \frac{1}{Q}(\frac{s}{w_o}) + 1} \qquad \text{----(5)}$$

The magnitude of the complex transfer function is plotted in figure(3). The -3dB, half-power, critical, or cutoff frequency f_c is the frequency at which the gain is reduced to $K/\sqrt{2}$ and is given by

$$f_c = \frac{f_o}{\sqrt{(1-\frac{1}{2Q^2}) + \sqrt{(1-\frac{1}{2Q^2})^2 + 1}}} \qquad \text{----(6)}$$

c- Band-Pass Filter

The complex transfer function for the second-order band-pass filter is [13]

$$T_B(s) = K\frac{\frac{I}{Q}(\frac{s}{w_o})}{(\frac{s}{w_o})^2 + \frac{1}{Q}(\frac{s}{w_o}) + 1} \qquad \text{----(7)}$$

The plot of the magnitude of the complex transfer function as a function of frequency is shown in figure(4). This circuit has both an upper, f_U, and lower, f_L, half-power frequencies given by

$$f_U = f_o(\frac{1}{2Q} + \sqrt{(\frac{1}{2Q})^2 + 1}) \qquad \text{----(8)}$$

and

$$f_L = f_o(-\frac{1}{2Q} + \sqrt{(\frac{1}{2Q})^2 + 1}) \qquad \text{----(9)}$$

The differences between these two half-power frequencies is known as the half-power band-width, BW, given by[14]

$$BW = f_U - f_L = \frac{f_o}{Q} \qquad \text{----(10)}$$

which reveals that:

$$Q = \frac{f_o}{BW} \qquad \text{----(11)}$$

The center frequency is also the geometric mean of the half-power frequency, i.e.

$$f_o = \sqrt{f_U f_L} \qquad \text{---(12)}$$

d- Notch Filter

The complex transfer function of the second order notch filter is given by[13]

$$T_N(s) = K\frac{(\frac{s}{w_o})^2 + 1}{(\frac{s}{w_o})^2 + \frac{1}{Q}(\frac{s}{w_o}) + 1} \qquad \text{----(13)}$$

A plot of the magnitude of the complex transfer function for notch filter is shown in figure(5).

CIRCUIT DESIGN

An integrator with a switched-capacitor circuit that emulates the resistor is shown in figure(6). The values are determined as follows; assume that the switched-capacitor value is $1\,nF$. In a switched capacitor, the emulating of emulate a $10\,k\Omega$ resistor is by effectively providing the same average current as the actual resistor. Using the formula;

$$T = RC = (10k\Omega)(1nF) = 10ms$$

this means that each switch must be operated at a frequency of

$$f = 1/T = 1/10ms = 100kHz$$

The duty cycle should be 50% so that the switch in each position half of the period of two non-overlapping $100kHz$. The 50% duty cycle voltages that are 180 out-of-phase with each other are applied to the transistor switches.

The circuit in figure(6) shows a crystal oscillator circuit that generates two nonoverlapping clocks by making full use of the two independent comparators of the $LM741$. $C1$ oscillates as before, but with a lower reference level, $C2's$ output will toggle at different times[15]. The resistors set the degree of separation between the outputs high pulses. With the values shown, each output has a 44% high and 56% low duty cycle, sufficient to allow $2ns$ between the high pulses where both are at logic low. The optional $A1$ feedback network shown can be used to force identical output duty. Since the reference level set for $C2$ is lower than that for $C1$, the steady state duty cycles will be 44% rather than 50%. Note, though, that the addition of this network only adjusts the percentage of time each output is high to be the same, which can be important in switching circuits requiring identical settling times. It cannot adjusts the relative phases between the two outputs to be exactly 180 apart because the signal at the input node driven by the crystal is not an exact sinusoid.

Figure(8) shows a circuit diagram of a second-order universal switched-capacitor filter including external resisters connected to provide High-Pass, Band-Pass, Low-Pass and Notch outputs. The center frequency of this filter is proportional to the clock frequency f_{CLK}. The resonant frequency f_o is given by[3]:

$$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \qquad \text{----(14)}$$

depending on whether the clock is being divided by 100 or 50; this is the center frequency

of both the band-pass and the notch filter. The quality factor is given by

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2} \qquad \text{----(15)}$$

The DC gain of the low-pass filter is

$$K_{LP} = -\frac{R4}{R1} \qquad \text{---- (16)}$$

The high-frequency gain of the high-pass filter is

$$K_{HP} = -\frac{R2}{R1} \qquad \text{----(17)}$$

The gain at the center frequency of the band-pass filter is

$$K_{BP} = -\frac{R3}{R1} \qquad \text{----(18)}$$

The gain of the notch filter at the notch frequency f_o is given by

$$A_n = \left| Q(\frac{R5}{R6} K_{LP} - \frac{R5}{R7} K_{HP}) \right| \qquad \text{----(19)}$$

which would normally be picked to be zero. The gain of the notch filter at DC is

$$K_N = \frac{R5}{R6} \times K_{LP} \qquad \text{----(20)}$$

while the gain at the frequency, which is half of the clock frequency, is

$$K_{\frac{CLK}{2}} = -\frac{R5}{R7} \times K_{HP} \qquad \text{---(21)}$$

THE RESULTS

Figure(6) shows the circuit gives two non-overlapping clocks. The waveforms is shown in figure(7), the frequency of the clocks are the same but the phase difference between them is 180^0. The clocks control the operating of two switching transistor of type 2N700. Figure (8) represents the electronic circuit diagram of the proposed universal switched capacitor filter which contains the High, Low, Band and Notch filters. The frequency response of all types filters are shown in figures (10,11and12). The specifications of the Universal Filter designed is shown in table (1). Figure(13) shows the filter and function generator circuits which represent the proposed IC, and the numbers in the circle represents the Pins Out of IC. Figure(14) represent 10-pin dual-in-line package IC connected to bode plot and power supply devices. Table(2) indicates the function of each pin in IC.

CONCLUSIONS

Universal Filter design of an operational amplifier and switch have been developed and simulated in MultiSim Package Version 9. The switched-capacitor techniques enable the design of various filters that can be realized in monolithic integrated circuits using state-of-art MOS technology. By replacing the noisy physical resistors with the switched-capacitor pairs, one is likely to draw the conclusion that many of the conventional methods developed for active-RC filters can be directly adapted to SC filters. However, 10-pin dual-in-line package which contains 6 op-amps for multi application are cheap, and so this circuit does not necessarily have to occupy a great deal more board space or be any more expensive than the single op-amp implementations.

By compare between figure(13) and figure(15), the proposed IC design differ than IC MF10 by adding the notch filter and clock generator in the proposed design, then no external requirements are used to establish the desired filter parameters. Also in this design, the outputs of each section of each filter are brought out to keep he device as universal as possible.

Filter center frequency accuracy and stability are only as good as the clock provided standard crystal oscillator combined with digital counters can provide very stable clocks for specific filter frequencies.

Switched-capacitor filters (SCFs) are renowned for ease of use. They are accurate, require no external components, and maintain a predictable response over all specified operating conditions. For integrated-circuit SCFs, their tightly matched and trimmed internal capacitors produce a fixed frequency and phase response that is proportional solely to the external clock frequency.

The differences between the theoretical (th) and practical (p) results is small that is enable the circuit operates correctly under required specifications.

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Table (1) : Specifications of the designed Universal Filter.

Types of filters	**Frequency**		**Quality Factor**		**Gain**	
	f_L	f_U	Q_{th}	Q_p	$G_{th}(dB)$	G_p (dB)
HPF	------	1.63KHz	------	------	19.171	19.044
BPF	140.549Hz	1.136KHz	0.305	0.401	0.0	-1.871
LPF	475.807Hz	-------	------	------	1.444	1.443
NPF	179.952Hz	1.605KHz	0.305	0.377	21.444	20.578

Table (2): Pins Assignment.

Pin number	**function**
1	Common
2	i/p signal 50mV, 200KHz
3	Ground
4	Vc= 2V
5	Notch filter o/p
6	LPF o/p
7	BPF o/p
8	HPF o/p
9	Vdd= -15V
10	Vcc= +15V

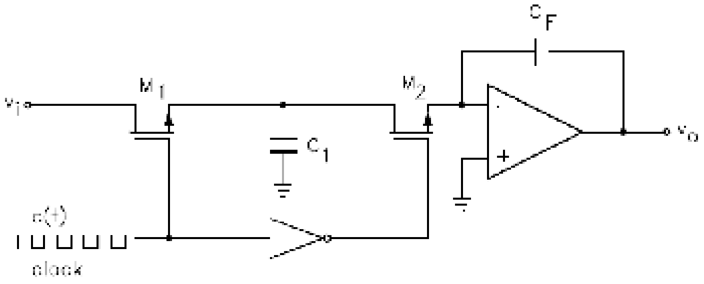


Figure (1): Switched Capacitor Integrator.

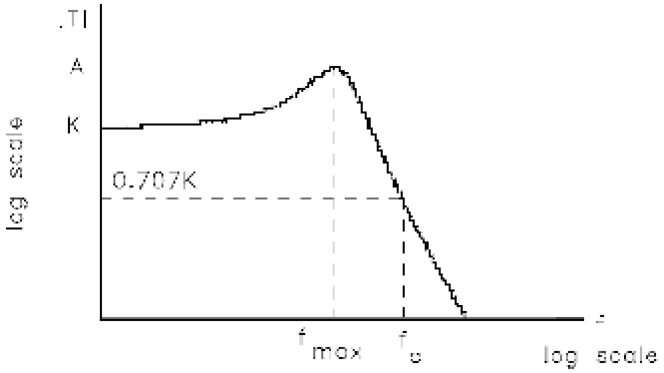


Figure (2): Frequency response of Low Pass Filter(theoretical).

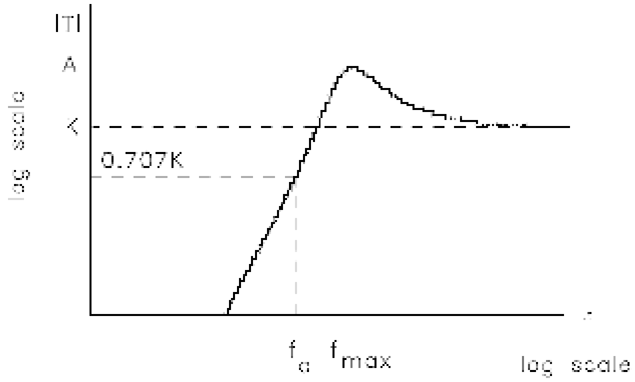


Figure (3): Frequency response of High Pass Filter(theoretical).

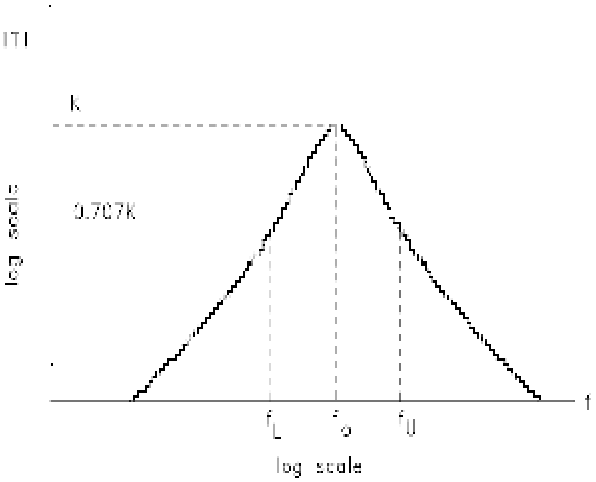


Figure (4): Frequency response of Band Pass Filter(theoretical).

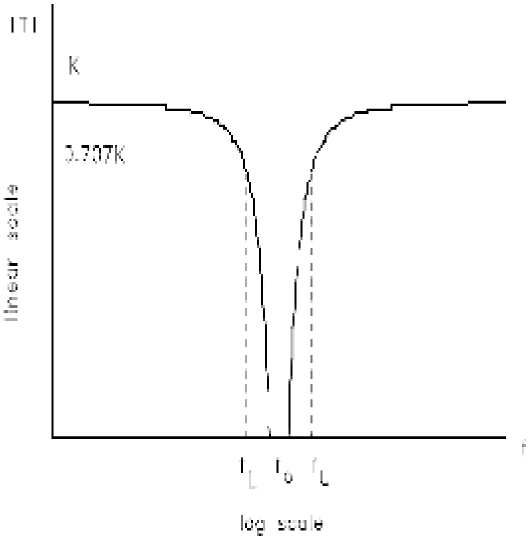


Figure (5): Frequency response of Notch Pass Filter(theoretical).

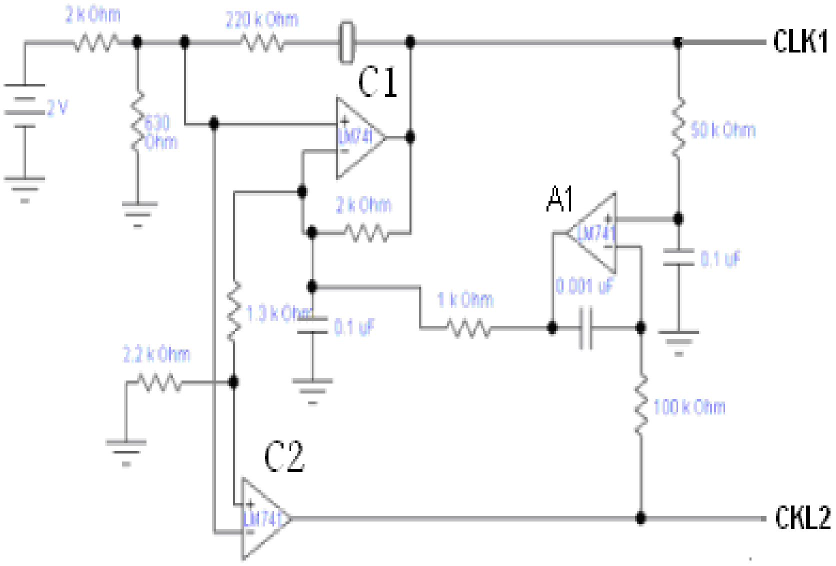
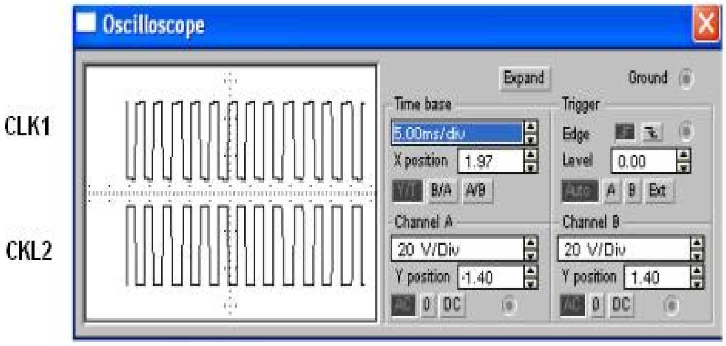


Figure (6): Clock Function Generator.



Time base
5.00ms/div
X position 1.97

Trigger
Level 0.00

Channel A
20 V/Div
Y position -1.40

Channel B
20 V/Div
Y position 1.40

Figure (7): Waveforms from Clock Function Generator.

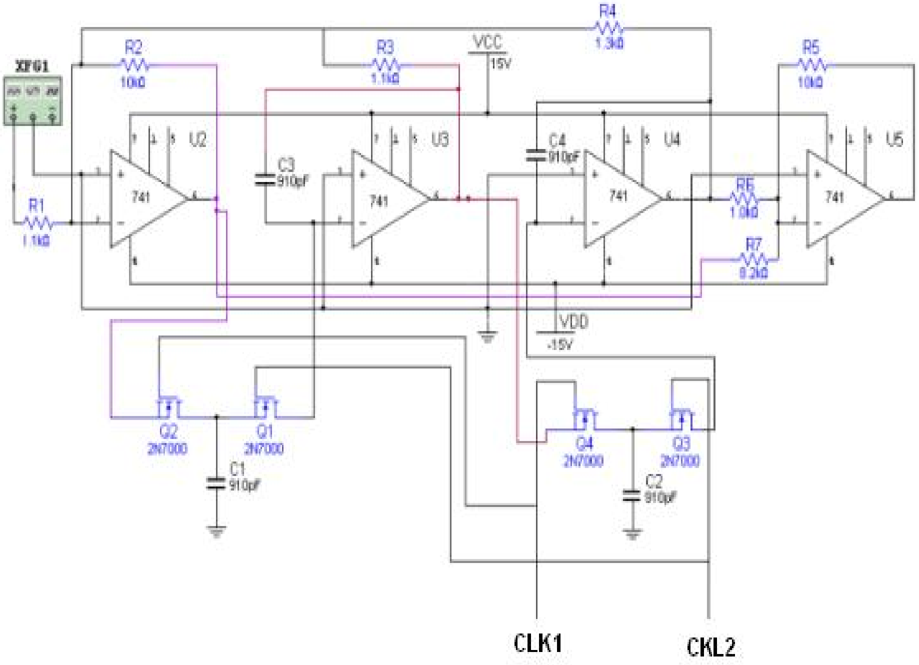
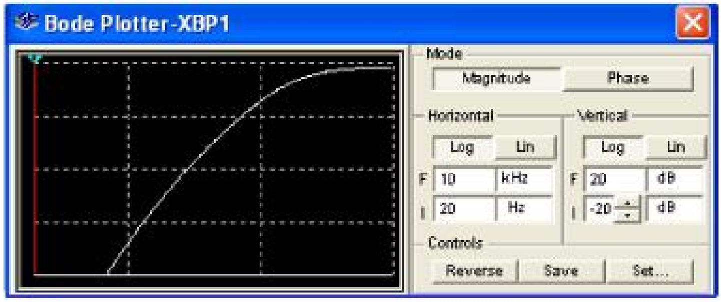


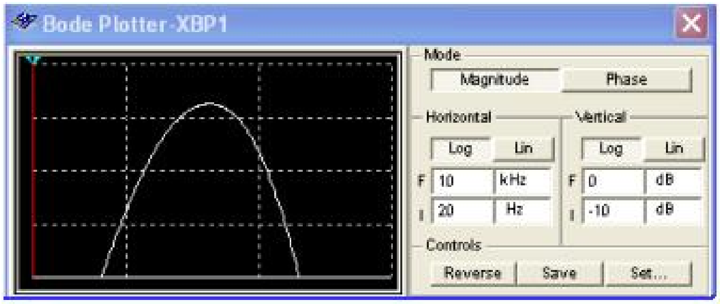
Figure (8): Circuit Diagram of Universal Switched Capacitor Filter.



Horizontal: F 10 kHz, I 20 Hz

Vertical: F 20 dB, I -20 dB

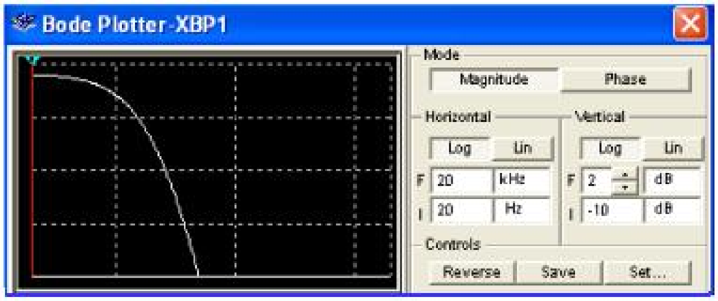
Figure (9): Frequency response of Low Pass Filter(practical).



Horizontal: F 10 kHz; I 20 Hz

Vertical: F 0 dB; I -10 dB

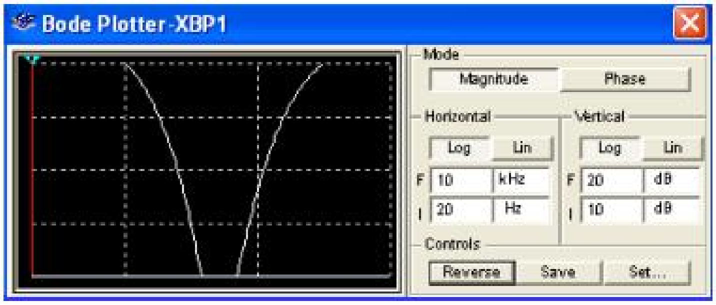
Figure (10): Frequency response of Band Pass Filter(practical).



Horizontal: F 20 kHz; I 20 Hz

Vertical: F 2 dB; I -10 dB

Figure (11): Frequency response of High Pass Filter(practical).



Horizontal: F 10 kHz; I 20 Hz

Vertical: F 20 dB; I 10 dB

Figure (12): Frequency response of Notch Pass Filter(practical).

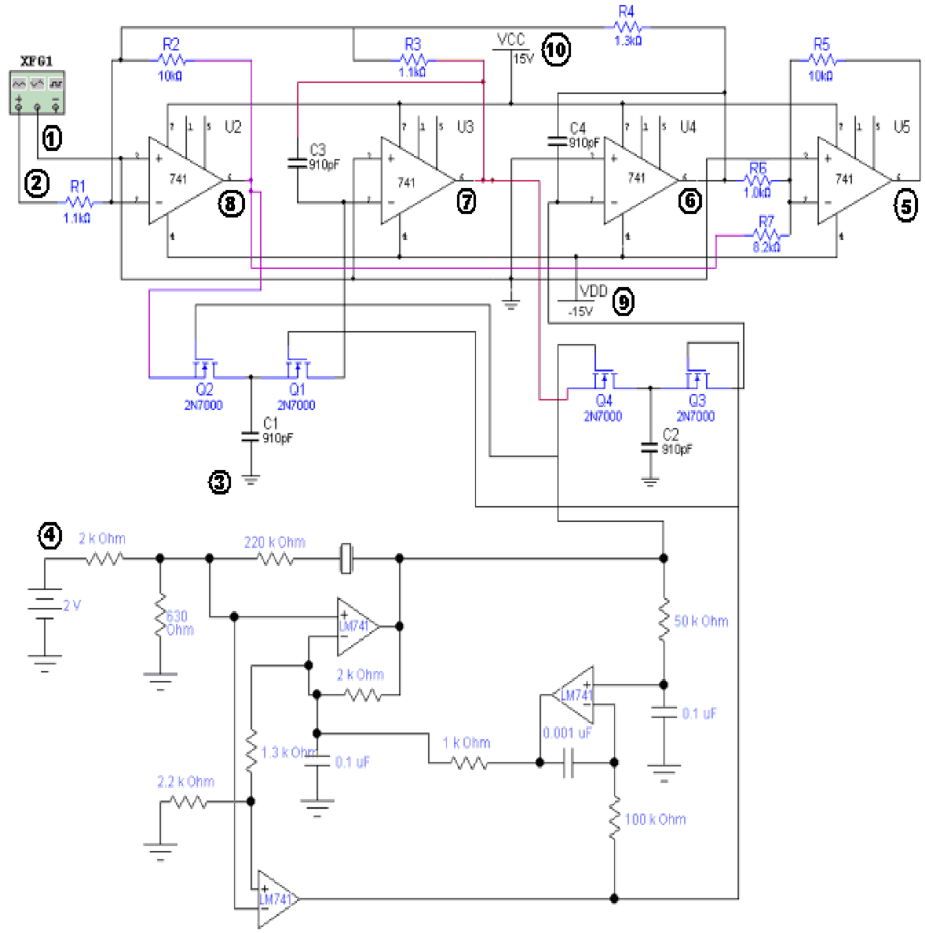
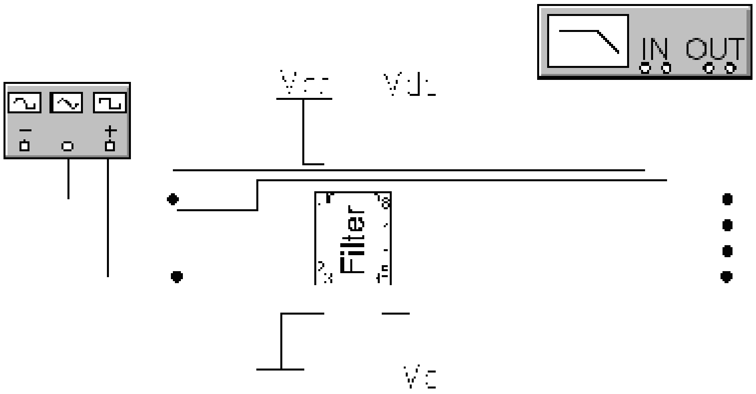


Figure (13): Filter and Function Generator Circuits.



Figure(14): 10-pin dual-in-line package IC connected to bode plot and power supply.

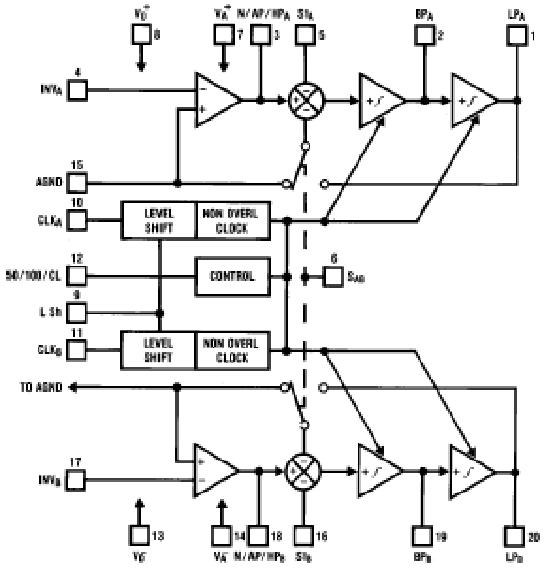


Figure (15): Block diagram of the MF10