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An Optimal Switching Sequence Model Predictive Control Scheme for the 3L-NPC Converter with Output LC Filter

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Abstract: In some applications of microgrids and distributed generation, it is necessary to feed islanded or stand-alone loads with high-quality voltage to provide low total harmonic distortion (THD). To fulfil these demands, an *LC* filter is usuallyconnected to the output terminals of power electronics converters. A cascaded voltage and current control loop with pulse-width modulation schemes are used to regulate the voltages and currents in these systems. However, these strategies have some drawbacks, particularly when multiple-input–multiple-output plants (MIMO) are controlled using single-input–single-output (SISO) design methods. This methodology usually produces a sluggish transient response and cross–coupling between different control loops and state variables. In this paper, a model predictive control (MPC) strategy based on the concept of optimal switching sequences (OSS) is designed to control voltage and current in an *LC* filter connected to a three-level neutral-point clamped converter. The strategy solves an optimisation problem to achieve control of the *LC* filter variables, i.e., currents and output voltages. Hardware-in-the-loop (HIL) results are obtained to validate the feasibility of the proposed strategy, using a PLECS–RT HIL platform and a dSPACE Microlab Box controller. In addition to the good dynamic performance of the proposed OSS–MPC, it is demonstrated using HIL results that the control algorithm is capable of obtaining low total harmonic distortion (THD) in the output voltage for different operating conditions.

Keywords: model predictive control (MPC); optimal switching sequence (OSS); multilevel inverters; optimal control

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1. Introduction

When power converters are utilised to supply electrical energy to islanded loads, in microgrids or distributed generation applications, typically an *LC* filter is connected at the converter outputs [1]. For instance, converters augmented by *LC* filters are used in applications such as uninterruptible power supplies (UPS) [2], energy storage systems [3], motor drives [4,5], microgrids [6–8], wind energy systems [9], etc.

When SISO control tools are utilised to design the control systems of power converters equipped with *LC* filters, typically two cascaded PI or PR control loops are required: an outer voltage control loop and an inner current control loop [1,10]. The voltage loop computes the reference for the inner current loop, and the current loop computes the desired converter voltage to be synthesized by a pulse-width modulation (PWM) scheme. However,

as discussed in [6], the cascaded interconnection of the voltage and current control loops has some drawbacks. Firstly, because SISO design tools are used, the inner and outer loops are separately designed with different bandwidths to avoid cross–couplings between the dynamics of the voltage and current control loops (usually, the outer loop is one order of magnitude slower than the inner loop). This produces a relatively slower transient response. Secondly, the controllers must be carefully tuned because their parameters affect the system's dynamic response. To overcome the drawbacks of cascaded linear controllers, model predictive control schemes, which are MIMO systems, have recently been proposed.

Model predictive control (MPC) has been garnering growing interest in the realm of power electronics converter applications. Most common applications include grid-connected converters, inverters with *RL* loads, inverters with output *LC* filters, and high-performance drives [11]. MPC has several advantages, such as simplicity for the inclusion of nonlinearities, simple treatment of constraints, the multivariable case and stochastic case can be easily considered [12], dead times can be compensated [13,14], etc. On the other hand, the disadvantage of some MPC algorithms, for instance, finite set MPC (or FS–MPC), is their relatively high computational load, particularly in power converter topologies where a large number of vectors are available. However, the exponential development in the processing power of microprocessors (such as digital signal processors and field-programmable gate arrays) has allowed the implementation of MPC algorithms in real-time platforms [14,15].

A wide variety of MPC algorithms for power electronics converters exist. An MPC algorithm can be considered, in general terms, as any algorithm that uses a model of the system to predict its future behaviour and select the most appropriate control action based on the solution to an optimal criterion [16]. The optimal criterion is evaluated in a cost function and can be, for example, tracking of the system state variables, minimising common-mode voltage, or reducing the converter switching frequency [16,17]. After the optimal criterion has been reached, and consequently the best possible solution to the optimisation problem has been obtained, the algorithm sends it to the converter to be synthesised.

MPC algorithms are classified according to the nature of the optimisation variable in the control problem. In broad terms, these algorithms for power electronics are classified as direct MPC or indirect MPC methods [17]. In direct MPC methods, the optimisation variable is an integer-valued vector representing the state of the converter switching device. Conversely, in indirect MPC the optimisation variable is a real-valued vector representing the fundamental component of the converter output voltage or duty cycles.

Direct MPC methods are subdivided into three categories: optimal switching vector MPC (OSV–MPC), MPC with hysteresis bounds, and MPC with an implicit modulator. OSV-MPC, commonly named finite control set MPC (FCS–MPC) in the literature, was first proposed to control the output current of a two-level inverter connected to an RL load [18]. Since then, it has been applied to many converter topologies [16]. In this strategy, the converter switches are directly computed and sent to the converter, thus allowing direct manipulation of the controlled variables. The advantages of OSV-MPC are an intuitive design procedure, straightforward implementation, and fast transient response [17]. However, they come at the cost of high computational complexity, particularly for multilevel power converters, and variable switching frequency due to the absence of a modulator [19].

Direct MPC methods with implicit modulators have been proposed to overcome the issue of variable switching frequency introduced by OSV-MPC while maintaining its advantages [20,21]. These strategies attempt to emulate the behaviour of pulse-width modulation techniques. In particular, optimal switching sequence MPC (OSS–MPC) and modulated MPC (M^2PC) introduce the concept of variable switching time instants [17]. According to the concept of variable switching time instants, the position of the converter switches can change at any moment during a sampling interval. Then, the strategies compute a sequence of switch positions and their corresponding duty cycles to be applied during the next sampling interval. Thus, a fixed switching frequency is achieved, resulting

in a reduction of harmonic distortion [17]. However, M^{2}PC is prone to suboptimality because the optimisation problem is solved in two stages: the first stage is to find the optimal switch positions and the second stage is to compute the duty cycles [22].

OSS–MPC avoids suboptimal solutions by computing the optimal sequence of switch positions and their corresponding duty cycles in one stage. The strategy was first introduced for power control of a grid-connected two-level inverter [21]. Then, the strategy was modified to be used in other converter topologies, such as a three-level neutral-point-clamped (3L-NPC) inverter and Vienna rectifier [23–26]. In [27], OSS–MPC was used for voltage control of an *LC*-filtered two-level inverter, achieving low output voltage ripple and reduced harmonic content compared to other MPC methods (such as OSV–MPC).

In this paper, the OSS–MPC presented in [26] is extended to three-level neutral-point-clamped (3L-NPC) inverters with output *LC* filters in stand-alone operation (such as UPS). The strategy uses a prediction model based on the improved-Euler method to compute the future value of the load output voltage and inductor filter current. The predicted values are compared against the desired reference values in the cost function of an optimisation problem. The cost function penalises the deviation between the measured values and the reference values, and also the control effort of the converter. The optimisation problem is solved offline to compute an optimal switching sequence to be applied by the converter. The optimal switching sequence is then transformed into a three-phase reference signal, which is used in an optimisation problem, to compute an optimal common-mode voltage to balance the DC-link capacitors of the converter. The common-mode voltage is then added to the three-phase reference signal, using the methodology already discussed in [26], and the resulting optimal three-phase reference is sent to an in-phase disposition PWM scheme to generate the pulses of the switching devices.

The contributions of this work are as follows:

- A new OSS–MPC algorithm is proposed for the control of a 3L-NPC converter feeding an *LC*-filtered stand-alone load. It is shown that the system is more complex to regulate than the grid-connected applications discussed in [24,26], where typically only two state variables, the $\alpha - \beta$ current components, are regulated. Conversely, for an *LC*-filtered stand-alone load, there are two more state variables, the $\alpha - \beta$ components of the inductance currents and load voltages, and the system is not reachable using a one-step horizon OSS–MPC (for a discussion of reachability, see [28]). Moreover, as discussed in Section 3.2.1, the forward-Euler discretisation algorithm may produce some performance issues when implementing current and voltage control for an *LC*-filtered stand-alone load.
- It is shown in this work that the proposed OSS–MPC, based on the improved-Euler discretisation method, can simultaneously control the 3L-NPC converter output current and load voltage with good tracking of the references (see the final paragraphs of Section 3.2.1). This is not considered in previously reported OSS–MPCs [27], where good output-current regulation is neglected, focusing mainly on load-voltage control. Moreover, in [27] the solution to the optimal problem is obtained using an extensive search of all the space vectors available in the 3L-NPC converter. Conversely, in this work a simpler methodology with a much lesser computational burden is applied to obtain the optimal solution (see Section 5.2).
- It is shown in this work that the proposed methodology can achieve good performance for linear and nonlinear loads. This is extensively demonstrated using HIL results. Moreover, in Section 8 it is shown that the OSS–MPC proposed in this work outperforms the OSS–MPC strategy reported in [27] for several tests, including applications involving nonlinear loads.

The rest of this paper is organised as follows. Section 2 presents the 3L-NPC converter topology, including modelling and modulation issues. Section 3 discusses the OSS–MPC algorithms used in this work, including state variable modelling of the system and the forward-Euler and improved-Euler discretisation methods. The advantages of improved-Euler, when compared to forward-Euler, are further addressed in Section 3.2.1. Section 4

discusses further details of the OSS–MPC proposed in this work, including the cost function; meanwhile, solving the optimal problem and reaching the optimal solution are discussed in Section 5 and Section 5.2, respectively.

Section 6 discusses an optimisation algorithm to calculate the common-mode voltage. This has already been discussed in [26] but, for completeness, is briefly discussed in this section. Section 7 presents the hardware-in-the-loop (HIL) system utilized to validate the proposed control strategy as well as the results obtained with the HIL platform. In Section 8, the performance of the proposed OSS–MPC algorithm is compared with that obtained with the state-of-the-art OSS–MPC reported in [27]. Finally, an appraisal of the work is discussed in the conclusions.

2. The 3L-NPC Inverter

The 3L-NPC inverter was the first multilevel converter topology, proposed by the group of Akagi in [29]. It was introduced around 1980 to reduce the pulsating torque and harmonic losses on AC drives, thus improving the efficiency and reducing the cost of the system. Nowadays, this converter topology is the standard for medium- and high-voltage applications [30,31]. In the mining industry, for example, 3L-NPC converters are used in variable frequency drives (VFD) for long belt-conveyor systems carrying ore [32].

As shown in the circuit diagram in Figure 1a, the 3L-NPC converter is composed of four switches and two clamped diodes per leg, producing a total of 27 three-phase switching states, $\boldsymbol{u}_{\text{abc}}$, for the whole converter, where $\boldsymbol{u}_{\text{abc}} \in \mathbb{U} \triangleq \{-1, 0, 1\}^3$. As depicted in Figure 1b, these switching states produce 19 non-redundant and 8 redundant switching vectors (SVs), $\boldsymbol{u}_{\text{s}}$, in the $\alpha\beta$ frame, where $\boldsymbol{u}_{\text{s}} = \mathbf{T}_{\alpha\beta}\boldsymbol{u}_{\text{abc}}$ and $\mathbf{T}_{\alpha\beta}$ is the amplitude invariant *abc*-to-$\alpha\beta$ transformation [33].

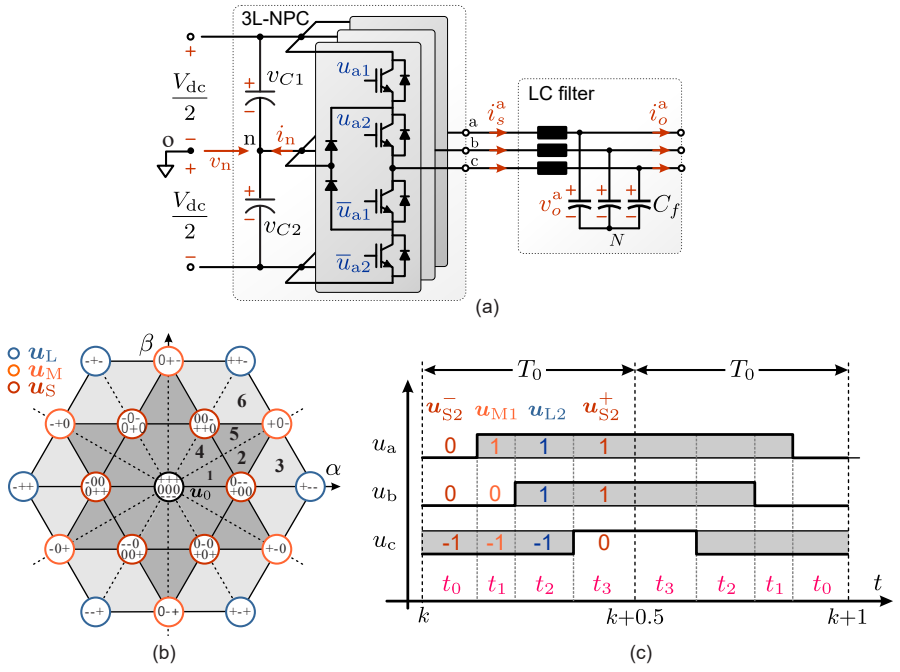

Figure 1. 3L-NPC converter: (**a**) topology; (**b**) space of switching vectors; (**c**) 7S-SS for the region $\mathcal{R}_6$.

According to the circuit diagram depicted in Figure 1a, the inverter voltages, $\boldsymbol{v}_{\text{abc}} = \begin{bmatrix} v_{\text{ao}} & v_{\text{bo}} & v_{\text{co}} \end{bmatrix}^{\mathsf{T}}$, are provided by

$$\boldsymbol{v}_{\text{abc}} = \frac{1}{2} V_{\text{dc}} \boldsymbol{u}_{\text{abc}} + (1 - |\boldsymbol{u}_{\text{abc}}|) v_{\text{n}} \tag{1}$$

where $|\boldsymbol{u}_{\mathrm{abc}}|=\left[|u_{\mathrm{a}}|\ |u_{\mathrm{b}}|\ |u_{\mathrm{c}}|\right]^{\intercal}$ and $v_{\mathrm{n}}=\frac{1}{2}(v_{C2}-v_{C1})$ is the NP-voltage. Using the transformation, $\mathbf{T}_{\alpha\beta}$, the inverter voltages (1) in the stationary $\alpha\beta$ frame can be expressed as

$$\boldsymbol{v}_{\mathrm{s}}=\frac{1}{2}V_{\mathrm{dc}}\boldsymbol{u}_{\mathrm{s}}-\mathbf{T}_{\alpha\beta}|\boldsymbol{u}_{\mathrm{abc}}|v_{\mathrm{n}}. \tag{2}$$

On the other hand, for a three-phase load with a floating neutral, the NP-voltage evolves as a function of the NP-current, i_{n}, according to

$$(C_1{+}C_2)\frac{\mathrm{d}v_{\mathrm{n}}}{\mathrm{d}t}=i_{\mathrm{n}},\quad i_{\mathrm{n}}=|\boldsymbol{u}_{\mathrm{abc}}|^{\intercal}\boldsymbol{i}_{\mathrm{abc}} \tag{3}$$

Therefore, for a given output current, $\boldsymbol{i}_{\mathrm{abc}}=\left[i_{\mathrm{s}}^{\mathrm{a}}\ i_{\mathrm{s}}^{\mathrm{b}}\ i_{\mathrm{s}}^{\mathrm{c}}\right]^{\intercal}$, as shown in (3), only small- and medium-size SVs, $\boldsymbol{u}_{\mathrm{S}}$ and $\boldsymbol{u}_{\mathrm{M}}$ (see Figure 1b) respectively, can affect the NP-voltage [34]. However, to balance the NP voltage, small SVs play a significant role because the redundancy of each SV drives an NP-current of the same amplitude but in the opposite direction. This tendency impacts v_{n} but not $\boldsymbol{v}_{\mathrm{s}}$ when the capacitors are balanced with a negligible voltage ripple, i.e., $v_{\mathrm{n}}\approx 0$.

To synthesize a desired inverter output voltage, the three nearest SVs are typically employed in carrier-based and space-vector PWM techniques [34,35]. Due to the presence of redundancies, several switching sequences (or switching patterns) can synthesize the desired output voltage. Therefore, the generation of switching sequences can be used for several purposes, such as to reduce the switching frequency and to minimize the NP-voltage ripple [34].

Based on the above analysis, the seven-segment switching sequence (7S-SS) [34] will be adopted in this work to implement the OSS–MPC strategy for voltage and current control. This switching pattern consists of four SVs, which are arranged in such a way that the transition between two adjacent switching states demands only one switching action. Additionally, each switching period is split into two sub-cycles of duration $T_0 = T_{\mathrm{s}}/2$, in which the disposition of the second sub-cycle is a reversal of the arrangement of the first [34], as shown in the example in Figure 1c. Furthermore, the first sub-cycle starts with an N-type small-size SV ($\boldsymbol{u}_{\mathrm{S}}^{-}$) and ends with the P-type redundancy ($\boldsymbol{u}_{\mathrm{S}}^{+}$). Therefore, each 7S-SS candidate can be defined accordingly as

$$\boldsymbol{S}\triangleq\left\{\boldsymbol{u}_{\mathrm{S}}^{-}[t_0],\boldsymbol{u}_1[t_1],\boldsymbol{u}_2[t_2],\boldsymbol{u}_{\mathrm{S}}^{+}[2t_3],\boldsymbol{u}_2[t_2],\boldsymbol{u}_1[t_1],\boldsymbol{u}_{\mathrm{S}}^{-}[t_0]\right\} \tag{4}$$

where t_i is the time in which the ith switching vector is synthesized by the converter, as depicted in Figure 1c.

Since the twelve internal regions (highlighted in grey in Figure 1b) have two N-type small-size SVs, each of them is further partitioned into two sub-regions to reduce the NP-voltage ripple [34]. Thus, to determine which dominant N-type small-size SV should be utilised to assemble the desired switching sequence, the space of SVs is divided into 36 regions, as shown in Figure 1b. Then, according to the OSS–MPC principles, a 7S-SS candidate is denoted as $\boldsymbol{S}_j$, where $j\in\mathcal{R}\triangleq\{1,\ldots,36\}$.

3. OSS-MPC Strategy for Voltage and Current Control

In this work, an OSS–MPC scheme will be employed to simultaneously control the voltage and current at an *LC* filter, while maintaining balanced voltages at the capacitors of the DC-link in a 3L-NPC converter. The overall controller is a predictive control scheme based on the solution to two optimisation problems.

The proposed control scheme is shown in Figure 2. The first optimisation problem—hereinafter called the outer optimisation loop—computes the optimal switching vectors sequence and duty cycles that minimize a cost function. The cost function is designed to track the desired values of the state vector and minimize the control effort of the converter. The second optimisation problem—hereinafter called the NP-voltage optimisation loop—computes an optimal common-mode injection signal (see bottom left-hand side

of Figure 2). The common-mode injection signal is designed to balance the neutral-point voltage between the DC-link capacitors. Notice that the NP-voltage optimisation loop presented in this work has already been discussed in [26]. However, for completeness, it is briefly summarised in Section 6.

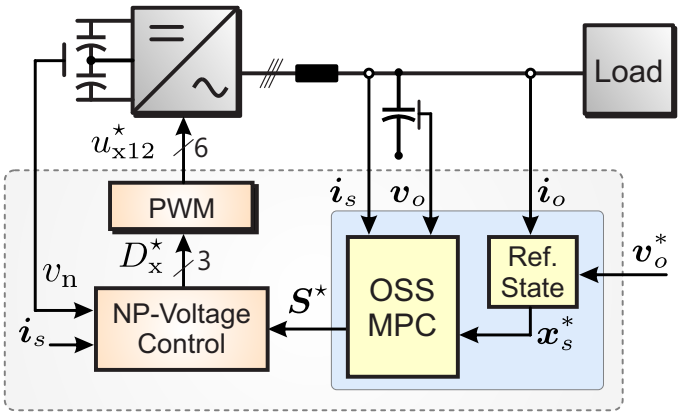

Figure 2. Proposed control system, composed of an MPC where the load voltage and the converter's output current are controlled in a single-stage MPC. The common-mode voltage is obtained using a second MPC algorithm, as already discussed in [26].

3.1. Continuous-Time Model

Let us consider a three-phase 3L-NPC converter connected to an *LC* filter, as shown in Figure 1a. The system of differential equations describing the dynamics of the *LC* filter can be written as

$$L_f \frac{d\boldsymbol{i}_s^{\alpha\beta}}{dt} + R_f \boldsymbol{i}_s^{\alpha\beta} = \boldsymbol{v}_s - \boldsymbol{v}_o^{\alpha\beta} \tag{5a}$$

$$C_f \frac{d\boldsymbol{v}_o^{\alpha\beta}}{dt} = \boldsymbol{i}_s^{\alpha\beta} - \boldsymbol{i}_o^{\alpha\beta} \tag{5b}$$

Assuming that the DC-link NP-voltage is balanced (i.e., $v_n = 0$), the converter output voltage in (2) is equal to $\boldsymbol{v}_s = \frac{V_{\mathrm{dc}}}{2}\boldsymbol{u}_s$. Moreover, by rearranging the equations and defining the state, input, and disturbance vectors as $\boldsymbol{x}_s = [i_s^{\alpha}\ i_s^{\beta}\ v_o^{\alpha}\ v_o^{\beta}]^{\intercal}$, $\boldsymbol{u}_s = [u_s^{\alpha}\ u_s^{\beta}]^{\intercal}$, and $\boldsymbol{i}_o = [i_o^{\alpha}\ i_o^{\beta}]^{\intercal}$ (The superscripts $\alpha\beta$ in the vectors will be avoided to simplify the notation), the state-space model of the AC side dynamics is then calculated as

$$\dot{\boldsymbol{x}}_s = \mathbf{A}\boldsymbol{x}_s + \mathbf{B}\boldsymbol{u}_s + \mathbf{E}\boldsymbol{i}_o \tag{6a}$$

$$\boldsymbol{y} = \mathbf{C}\boldsymbol{x}_s \tag{6b}$$

Matrices **A**, **B**, and **E** contain the parameters of the filter and matrix **C** is the identity matrix.

$$\mathbf{A} = \begin{bmatrix} -\mathbf{L}^{-1}\mathbf{R} & -\mathbf{L}^{-1} \\ \mathbf{C}_f^{-1} & \mathbf{0} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} \frac{V_{dc}}{2}\mathbf{L}^{-1} \\ \mathbf{0} \end{bmatrix} \quad \mathbf{E} = \begin{bmatrix} \mathbf{0} \\ -\mathbf{C}_f^{-1} \end{bmatrix} \tag{7}$$

The resistance, inductance, and capacitance matrices are defined as follows:

$$\mathbf{R} = R_f\mathbf{I}_2 \quad \mathbf{L} = L_f\mathbf{I}_2 \quad \mathbf{C}_f = C_f\mathbf{I}_2 \tag{8}$$

The dimensions of the system matrices are $\mathbf{A} \in \mathbb{R}^{4\times4}$, $\mathbf{B} \in \mathbb{R}^{4\times2}$, $\mathbf{E} \in \mathbb{R}^{4\times2}$, $\boldsymbol{x}_s(t) \in \mathbb{R}^{4\times1}$, $\boldsymbol{u}_s(t) \in \mathbb{R}^{2\times1}$, and $\boldsymbol{i}_o(t) \in \mathbb{R}^{2\times1}$.

3.2. Discrete-Time Model

MPC algorithms use the discrete-time mathematical model of the system to make predictions of the state-vector trajectory, then utilise the predicted values in an optimisation problem and compute the best control action that fulfils the control objectives.

Typically, for the discrete implementation of the continuous-time model, the forward-Euler method is applied, and this is briefly reviewed below. However, the forward-Euler methodology has some disadvantages for the control of *LC*-filtered stand-alone loads, and this is further discussed at the end of Section 3.2.1.

3.2.1. Forward-Euler-Based Discrete Time Model

It is assumed in this work that a 7S-SS is applied to the converter during every switching cycle. Considering the forward-Euler method, the instantaneous trajectory of the state vector when a switching vector is applied can be computed as

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + T_0 f(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}) d_\ell \tag{9}$$

where $\ell \in \{0, 1, 2, 3\}$ is the index for the switching vectors of the sequence. The instantaneous evolution of the state-vector prediction at the end of the sub-cycle corresponds to its average trajectory when the seven-segment SS defined by (4) (see [24]) is applied to the system:

$$\overline{\boldsymbol{x}}_s[k+1] = \boldsymbol{x}_s[k] + T_0 \sum_{\ell=0}^{3} \left. \frac{d\boldsymbol{x}_s}{dt} \right|_{t=\ell} d_\ell \tag{10}$$

To simplify the analysis, every subinterval slope, $m_\ell = f(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell})$, is approximated using the values of the state and disturbance vector at the sampling instant, k, as $m_\ell \approx f(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k])$. Therefore, the prediction of the average trajectory can be expressed as

$$\overline{\boldsymbol{x}}_s[k+1] = \mathbf{A}_d \boldsymbol{x}_s[k] + \mathbf{E}_d \boldsymbol{i}_o[k] + \mathbf{B}_d \sum_{\ell=0}^{3} \boldsymbol{u}_{s\ell} d_\ell \tag{11}$$

where $\mathbf{A}_d = \mathbf{I}_4 + T_0 \mathbf{A}$, $\mathbf{E}_d = T_0 \mathbf{E}$ and $\mathbf{B}_d = T_0 \mathbf{B}$. Because for any N-type seven-segment SS, $\boldsymbol{u}_{s0} = \boldsymbol{u}_S^-$, and $\boldsymbol{u}_{s3} = \boldsymbol{u}_S^+$, the duty cycles d_0 and d_3 can be combined as $d_s = d_0 + d_3$, which is the duty cycle for the small vectors of the sequence [24]. Then, the following linear representation of the average trajectory can be stated as

$$\overline{\boldsymbol{x}}_s[k+1] = \mathbf{A}_d \boldsymbol{x}_s[k] + \mathbf{E}_d \boldsymbol{i}_o[k] + \mathbf{B}_d \boldsymbol{U} \boldsymbol{d} \tag{12}$$

where the dwell-time vector, $\boldsymbol{d}$, and switching matrix, $\boldsymbol{U}$, are defined as

$$\boldsymbol{d} = \begin{bmatrix} d_s & d_1 & d_2 \end{bmatrix} \in \mathbb{D} \triangleq [0, 1]^3 \tag{13a}$$

$$\boldsymbol{U} = \begin{bmatrix} \boldsymbol{u}_s & \boldsymbol{u}_1 & \boldsymbol{u}_2 \end{bmatrix} \tag{13b}$$

Even when the forward-Euler discretisation algorithm is widely used for the implementation of MPC algorithms, there are some issues which are produced when this methodology is applied to *LC*-filtered stand-alone loads. Some of these issues are as follows:

- For these sort of applications, usually two cascaded MPC algorithm are implemented [36] to regulate the voltages and currents. An outer MPC regulates the voltages and an inner MPC regulates the converter's output currents; in this case, the standard forward-Euler algorithm performs well. Nevertheless, when nested cascaded MPC loops are implemented, two cost functions are required and a global optimum is not necessarily reached. This is further discussed in [37].
- To obtain a global optimum, a single cost function is recommended, which has to consider the tracking errors of the currents and load voltages. However, an *LC*-filtered load is a plant which is not reachable in a single-step horizon, i.e., the output currents

and load voltages cannot reach their reference values in one step because the **B** matrix of (11) is not squared (see [28]). To solve this issue when the forward-Euler discretisation method is used, an MPC algorithm with a two-step horizon has been proposed in [37]; nevertheless, this larger prediction horizon may produce a relatively large computer burden, which can be justifiable for a large and costly modular multilevel converter but is hardly convenient for a smaller stand-alone application.

- Moreover, one of the main disadvantages of forward-Euler-based MPC algorithms for single-stage implementation (i.e., the application presented in this work) is the unconstrained solution obtained from the cost solution of (30). The matrices $\mathbf{A_d}$ and $\mathbf{B_d}$ obtained using the forward-Euler discretisation method (see (12)) are prone to producing an unconstrained solution for $\mathbf{U_d}$ which is very weakly related to the load-voltage tracking error. Therefore, when forward-Euler is applied to the system of Figure 1b, poor performance or even a complete lack of control could be obtained for the regulation of the load voltage. Conversely, when the improved-Euler method is used to discretise (6a) and (6b), more exact matrices are obtained for $\mathbf{A_d}$ and $\mathbf{B_d}$ (see (17)) and the unconstrained solution for $\mathbf{U_d}$ can be tuned (by adjusting the cost weights) to be dependent on both the tracking error of the load voltage as well as on the tracking error of the 3L-NPC converter output current.

Based on the comparison presented above, in this work the discretisation of the continuous-time model is performed using the improved-Euler method [38]. This is further discussed in the next section.

3.2.2. Improved-Euler-Based Discrete Time Model

The improved-Euler method is a second-order Runge–Kutta method to compute the solutions of ordinary differential equations [38]. In this method, the weighted average of the approximations to the derivative at intermediate points on the solution curve is computed. Specifically, the improved-Euler method uses the extreme points of the solution interval (i.e., kth and $(k+1)$th points). Higher-order Runge–Kutta methods use more intermediate points to increase the accuracy of the solution.

Once again, it is assumed that a 7S-SS is applied by the converter during the complete switching cycle. Considering the improved-Euler method, the instantaneous evolution of the state vector is given by the following equation:

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + \frac{T_s}{2}\left[f(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}) + f(\boldsymbol{x}_{s\ell}[k+1], \boldsymbol{u}_{s\ell}[k+1], \boldsymbol{i}_{o\ell}[k+1])\right] d_\ell \tag{14}$$

The average slope is multiplied by T_s because it is the time length between predictions in the interval $[k, k+1]$ and predictions in the interval $[k+1, k+2]$. To simplify (14), some assumptions about the states and inputs used for computational purposes are required. Firstly, the slope of the system at the kth time instant is computed with the values measured at the time instant k (i.e., $f(\boldsymbol{x}_{s\ell}, \boldsymbol{u}_{s\ell}, \boldsymbol{i}_{o\ell}) \approx f(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k])$). Secondly, the slope at the $(k+1)$th time is computed with the predicted state vector, $\overline{\boldsymbol{x}}_s[k+1]$, using the forward-Euler approximation defined by (12). The switching sequence applied is the same as that of time instant k (i.e., $f(\boldsymbol{x}_{s\ell}[k+1], \boldsymbol{u}_{s\ell}[k+1], \boldsymbol{i}_{o\ell}[k+1]) \approx f(\overline{\boldsymbol{x}}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1])$). The disturbance vector is assumed to be constant during the switching cycle but different between switching cycles (i.e., $\boldsymbol{i}_o[k] \neq \boldsymbol{i}_o[k+1]$). Considering these assumptions, the state-vector trajectory is described by

$$\boldsymbol{x}_{s(\ell+1)} = \boldsymbol{x}_{s\ell} + \frac{T_s}{2}\left[f(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k]) + f(\boldsymbol{x}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1])\right] d_\ell \tag{15}$$

The slopes $\boldsymbol{m}_\ell[k] = f(\boldsymbol{x}_s[k], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k])$ and $\boldsymbol{m}_\ell[k+1] = f(\overline{\boldsymbol{x}}_s[k+1], \boldsymbol{u}_{s\ell}, \boldsymbol{i}_o[k+1])$ are described by the following equations:

$$\boldsymbol{m}_\ell[k] = \mathbf{A}\boldsymbol{x}_s[k] + \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k] \tag{16a}$$

$$\boldsymbol{m}_\ell[k+1] = \mathbf{A}\overline{\boldsymbol{x}}_s[k+1] + \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k+1] \tag{16b}$$

Replacing $\overline{\boldsymbol{x}}_s[k+1]$ in (16b), the expression for the slope $\boldsymbol{m}_\ell[k+1]$ is obtained as follows:

$$\begin{aligned}\boldsymbol{m}_\ell[k+1] = &\left(\mathbf{A} + \frac{1}{2}T_s\mathbf{A}^2\right)\boldsymbol{x}_s[k] + \frac{1}{2}T_s\mathbf{A}\mathbf{B}\boldsymbol{U}\boldsymbol{d} + \frac{1}{2}T_s\mathbf{A}\mathbf{E}\boldsymbol{i}_o[k] \\ &+ \mathbf{B}\boldsymbol{u}_{s\ell} + \mathbf{E}\boldsymbol{i}_o[k+1]\end{aligned} \tag{17}$$

Then, the average trajectory of the state vector, using the improved-Euler method, is computed as

$$\overline{\boldsymbol{x}}_s[k+1] = \boldsymbol{x}_s[k] + \frac{T_s}{2}\sum_{\ell=0}^{3}\left[\boldsymbol{m}_\ell[k] + \boldsymbol{m}_\ell[k+1]\right]d_\ell \tag{18}$$

Replacing (16a) and (17) into (18), and after some algebraic manipulations, the following expression is obtained:

$$\begin{aligned}\overline{\boldsymbol{x}}_s[k+1] = &\left(\mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2\right)\boldsymbol{x}_s + \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}\boldsymbol{U}\boldsymbol{d} \\ &+ \frac{1}{2}\left(\mathbf{I} + \frac{1}{2}T_s\mathbf{A}\right)T_s\mathbf{E}\boldsymbol{i}_o[k] + \frac{1}{2}T_s\mathbf{E}\boldsymbol{i}_o[k+1]\end{aligned} \tag{19}$$

Equation (19) is useful when an observer-predictor computes $\boldsymbol{i}_o[k+1]$, and the difference between $\boldsymbol{i}_o[k]$ and $\boldsymbol{i}_o[k+1]$ is sufficiently large. However, if it is assumed that $\boldsymbol{i}_o[k] \approx \boldsymbol{i}_o[k+1]$ then the average prediction model is simplified to

$$\begin{aligned}\overline{\boldsymbol{x}}_s[k+1] = &\left(\mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2\right)\boldsymbol{x}_s + \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}\boldsymbol{U}\boldsymbol{d} \\ &+ \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{E}\boldsymbol{i}_o[k]\end{aligned} \tag{20}$$

The discrete-time model in (20) can be written as the linear representation (12) with $\mathbf{A}_d = \mathbf{I} + T_s\mathbf{A} + \frac{1}{4}T_s^2\mathbf{A}^2$, $\mathbf{B}_d = \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{B}$, and $\mathbf{E}_d = \left(\mathbf{I} + \frac{1}{4}T_s\mathbf{A}\right)T_s\mathbf{E}$. This discrete-time model will be used in this work.

4. OSS-MPC Formulation for Voltage and Current Control

The main objective of the controllers is to keep the voltage of the *LC* filter capacitors as sinusoidal non-distorted waveforms. Meanwhile, the converter currents are controlled as a secondary objective. In this regard, the reference voltage vector is

$$\boldsymbol{v}_o^*[k+1] = V^* e^{j\omega[k+1]T_s} \tag{21}$$

where V^* is the magnitude of the reference voltage vector and ω is the fundamental frequency of the output voltage ($\omega = 2\pi f_0$).

The reference current is obtained as a function of the reference voltage. Replacing the reference voltage vector into the dynamic equation of the output voltages yields [39]

$$\frac{d\boldsymbol{v}_o^*}{dt} = \frac{1}{C_f}(\boldsymbol{i}_s^* - \boldsymbol{i}_o) \tag{22}$$

Solving the equation for $\boldsymbol{i}_s^*$, the converter reference current vector is obtained:

$$\boldsymbol{i}_s^* = \omega C_f \mathbf{J}\boldsymbol{v}_o^* + \boldsymbol{i}_o \tag{23}$$

where the matrix $\mathbf{J}$ is defined as

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \tag{24}$$

It is desirable to constrain the reference current to a maximum value, I_{max}. When the amplitude of the reference current is less than the specified limit, the reference current vector is described by Equation (23). In the other case, the reference current vector is saturated at I_{max}. Therefore, the constrained reference current is represented by the following piecewise function:

$$\boldsymbol{i}_s^* = \begin{cases} \omega C_f \mathbf{J} \boldsymbol{v}_o^* + \boldsymbol{i}_o & \|\boldsymbol{i}_s^*\|_2 < I_{max} \\ \frac{I_{max}}{\|\boldsymbol{i}_s^*\|_2} \boldsymbol{i}_s^* & \|\boldsymbol{i}_s^*\|_2 \geq I_{max} \end{cases} \tag{25}$$

Thus, the reference state vector is

$$\boldsymbol{x}_s^*[k+1] = \begin{bmatrix} \boldsymbol{i}_s^* \\ \boldsymbol{v}_o^* \end{bmatrix} \tag{26}$$

4.1. Cost Function

At the heart of the MPC strategy lies the cost function. In the cost function, the variables related to the control objectives are weighted to choose the best possible action. In FCS-MPC schemes, the cost function is most commonly designed to minimize the tracking error [5,16]; however, it has been shown that FCS-MPC strategies without penalization of the control effort are equivalent to quantised deadbeat controllers [19]. Deadbeat controllers feature fast dynamic response [28], but they have poor robustness against model mismatches, parameter uncertainties, and noise on measured variables [40]. To alleviate the unwanted effects of deadbeat controllers, the control effort is usually penalised in the cost function [28]. In the control proposed in this work, the OSS–MPC control has two objectives: minimise the tracking error between the state vector and its reference and penalize the control effort. Therefore, the following cost function is defined:

$$J(\boldsymbol{U}_j, \boldsymbol{d}_j) = \|\boldsymbol{x}_s[k+1] - \boldsymbol{x}_s^*[k+1]\|_{\mathbf{Q}}^2 + \lambda_u \|\boldsymbol{u}[k] - \boldsymbol{u}_{ss}[k]\|_2^2 \tag{27}$$

The positive-definite matrix $\mathbf{Q}$ = diag(λ_i,λ_i,λ_v,λ_v) is used to trade-off the control objectives of the state-vector tracking. Similarly, the weighting factor, λ_u, is used to penalize the control effort. The optimisation variable of the problem is the average switching vector, $\boldsymbol{u}(k)$. The average switching vector is the product between the switching matrix and the duty cycle vector, $\boldsymbol{u}(k) = \boldsymbol{U}\boldsymbol{d}$.

Firstly, the term of the cost function used to penalize the reference tracking error will be reformulated as a function of the average switching vector, $\boldsymbol{u}(k)$. Replacing (12) in (27) yields

$$\|\mathbf{B}_d \boldsymbol{u} - \underbrace{(\boldsymbol{x}_s^*[k+1] - \mathbf{A}_d \boldsymbol{x}_s[k] - \mathbf{E}_d \boldsymbol{i}_o[k])}_{:=\boldsymbol{\kappa}[k]}\|_{\mathbf{Q}}^2 \tag{28}$$

where the value of $\boldsymbol{\kappa}$ can be obtained using (12). If $\boldsymbol{x}_s^*[k+1] = \mathbf{A}_d \boldsymbol{x}_s[k] + \mathbf{E}_d \boldsymbol{i}_o[k] + \mathbf{B}_d \boldsymbol{U}\boldsymbol{d}$, then the required $\mathbf{B}_d \boldsymbol{U}\boldsymbol{d}$ to produce $\boldsymbol{x}_s^*[k+1]$ is equal to $\boldsymbol{x}_s^*[k+1] - \mathbf{A}_d \boldsymbol{x}_s[k] - \mathbf{E}_d \boldsymbol{i}_o[k]$. This is defined as $\boldsymbol{\kappa}$ in (28).

The second term of the cost function in Equation (27) has the vector $\boldsymbol{u}_{ss}$. Vector $\boldsymbol{u}_{ss}$ is the steady-state control action. The steady-state control action is the input vector needed to drive the system towards the steady-state solution. The expression for this vector is obtained by solving the circuit of Figure 3 for $\boldsymbol{u}_{ss}$. The steady-state control input, $\boldsymbol{u}_{ss}$, is defined as

$$\boldsymbol{u}_{ss} = \frac{2}{V_{dc}} \left\{ \left[\left(1 - \omega^2 L_f C_f\right) \mathbf{I}_2 + \left(\omega R_f C_f\right) \mathbf{J} \right] \boldsymbol{v}_o^* + \left[R_f \mathbf{I}_2 + \omega L_f \mathbf{J} \right] \boldsymbol{i}_o \right\} \tag{29}$$

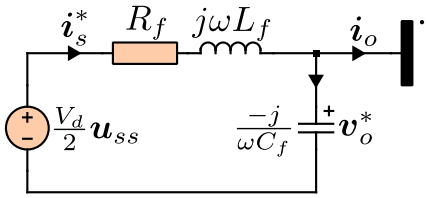

Figure 3. Circuit diagram to obtain the steady–state control action.

Finally, the cost function for the optimisation problem can be written as

$$J_j(\boldsymbol{U}_j, \boldsymbol{d}_j) = \|\mathbf{B}_d \boldsymbol{u}[k] - \boldsymbol{\kappa}\|_{\mathbf{Q}}^2 + \lambda_u \|\boldsymbol{u}[k] - \boldsymbol{u}_{ss}[k]\|_2^2 \tag{30}$$

4.2. Optimisation Problem

In OSS–MPC, the optimal switching sequence (OSS) is obtained by solving an optimisation problem. The solution must comply with constraints such that the sum of leg duty cycles is equal to one, and each duty cycle must be equal to or greater than zero. Therefore, the optimisation problem to be solved is as follows:

$$\{\boldsymbol{U}^\star, \boldsymbol{d}^\star\} = \arg\min_{\boldsymbol{U}_j} \Big\{ \min_{\boldsymbol{d}_j} J_j(\boldsymbol{U}_j, \boldsymbol{d}_j) \Big\} \tag{31a}$$

$$\text{s.t.} \quad \mathbf{1}^\intercal \boldsymbol{d} = 1 \tag{31b}$$

$$\boldsymbol{d}_j \geq \mathbf{0} \tag{31c}$$

The optimisation problem has the same form as the one solved in [26]. Therefore, the same optimiser will be used. Thus, the usual strategy to solve MPC problems with 3L-NPC converters of evaluating each region, $\mathcal{R}_j \in \{\mathcal{R}_1, \ldots, \mathcal{R}_{24}\}$, of the space of vectors is avoided.

5. Optimal Solution

In this section, the optimisation problem presented in (31a), (31b) and (31c) will be solved to obtain the optimal switching vector sequence and its corresponding duty cycles to be applied during the next sampling instant. Two cases of the problem are distinguished: first, the linear modulation stage where the duty cycles are positive, and second, the overmodulation stage where the duty cycle of the small switching vectors becomes negative.

5.1. Non-Negative Duty Cycles: The Linear Modulation Stage

To relax the optimisation problem, the inequality constraints are removed from the problem formulation. Thus, the solution is assumed to be in the linear modulation stage, where the duty cycles are always non-negative. The relaxed optimisation problem is then stated as

$$\min_{\boldsymbol{d}} \; J_j(\boldsymbol{U}_j, \boldsymbol{d}_j) \tag{32a}$$

$$\text{s.t.} \quad \mathbf{1}^\intercal \boldsymbol{d}_j = 1 \tag{32b}$$

Expanding the cost function (30) yields

$$J_j = (\mathbf{B}_d \boldsymbol{u} - \boldsymbol{\kappa})^\intercal \boldsymbol{Q} (\mathbf{B}_d \boldsymbol{u} - \boldsymbol{\kappa}) + \lambda_u (\boldsymbol{u} - \boldsymbol{u}_{ss})^\intercal (\boldsymbol{u} - \boldsymbol{u}_{ss}) \tag{33}$$

The following expression is obtained:

$$J_j = \boldsymbol{u}^\intercal \big(\boldsymbol{Q}' + \lambda_u \mathbf{I}_2\big)\boldsymbol{u} - 2\boldsymbol{u}^\intercal \big(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\big) + \big(\lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss} + \boldsymbol{\kappa}^\intercal \boldsymbol{Q}\boldsymbol{\kappa}\big) \tag{34}$$

where Q' is the modified weight matrix, $\mathbf{Q}' = \mathbf{B}_d^\intercal \mathbf{Q} \mathbf{B}_d$. The elements of the switching matrix, $\boldsymbol{U}_j \in \mathbb{R}^{2\times 3}$, are the vectors of the switching sequence:

$$\boldsymbol{U}_j = \begin{bmatrix} u_{s\alpha} & u_{1\alpha} & u_{2\alpha} \\ u_{s\beta} & u_{1\beta} & u_{2\beta} \end{bmatrix} \tag{35}$$

Considering the equality constraint of the relaxed optimisation problem, the duty cycles for the small switching vectors, as a function of the remaining duty cycles, can be written as

$$d_{Sj} = 1 - d_{1j} - d_{2j} \tag{36}$$

An auxiliary variable, $\boldsymbol{d}_{\eta j}$, is defined to eliminate the dependent variable d_S from the optimisation vector $\boldsymbol{d}_j$:

$$\boldsymbol{d}_{\eta j} = \begin{bmatrix} d_{1j} & d_{2j} \end{bmatrix}^\intercal \tag{37}$$

The relationship between $\boldsymbol{d}_j$ and $\boldsymbol{d}_{\eta j}$ is as follows:

$$\boldsymbol{d}_j = \underbrace{\begin{bmatrix} -1 & -1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}}_{\boldsymbol{M}} \boldsymbol{d}_{\eta j} + \underbrace{\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{N}} \tag{38}$$

Then, $\boldsymbol{u} = \boldsymbol{U}\boldsymbol{d} = \boldsymbol{U}(\boldsymbol{M}\boldsymbol{d}_{\eta j} + \boldsymbol{N}) = \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} + \boldsymbol{U}\boldsymbol{N}$ and $\boldsymbol{u}^\intercal = \boldsymbol{d}^\intercal \boldsymbol{U}^\intercal = (\boldsymbol{M}\boldsymbol{d}_{\eta j} + \boldsymbol{N})^\intercal \boldsymbol{U}^\intercal = \left(\boldsymbol{d}_{\eta j}^\intercal \boldsymbol{M}^\intercal + \boldsymbol{N}^\intercal\right)\boldsymbol{U}^\intercal$. The cost function in terms of $\boldsymbol{d}_{\eta j}$ is

$$\begin{aligned} J = {} & \boldsymbol{d}_{\eta j}^\intercal \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} \\ & + 2\boldsymbol{d}_{\eta j} \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{N} \\ & - 2\boldsymbol{d}_{\eta j} \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}) + \boldsymbol{N}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{N} \\ & - 2\boldsymbol{N}^\intercal \boldsymbol{U}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}) + (\boldsymbol{\kappa}^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss}) \end{aligned} \tag{39}$$

Computing the gradient of J with respect to $\boldsymbol{d}_{\eta j}$ and making it equal to zero yields

$$\begin{aligned} \nabla J(\boldsymbol{d}_{\eta j}) = {} & 2\boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} \\ & + 2\boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{N} \\ & - 2\boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}) = \mathbf{0} \end{aligned} \tag{40}$$

Reorganizing (40) to leave the terms related to the duty cycles on the left, (41) is obtained:

$$\begin{aligned} & \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{M}\boldsymbol{d}_{\eta j} = \\ & \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}) - \boldsymbol{M}^\intercal \boldsymbol{U}^\intercal (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2) \boldsymbol{U}\boldsymbol{N} \end{aligned} \tag{41}$$

Solving the equation for $\boldsymbol{d}_{\eta j}$ yields

$$\boldsymbol{d}_{\eta j} = [\boldsymbol{U}\boldsymbol{M}]^{-1} \boldsymbol{u}_{unc} - [\boldsymbol{U}\boldsymbol{M}]^{-1} \boldsymbol{U}\boldsymbol{N} \tag{42}$$

Therefore, the unconstrained control action ($\boldsymbol{u}_{uc}$) is defined as

$$\boldsymbol{u}_{uc} = (\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2)^{-1} \left(\boldsymbol{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right) \tag{43}$$

Now, it is necessary to map the solution back to its original variables. Replacing (42) in (38) yields

$$\boldsymbol{d}_{rj} = \begin{bmatrix} \boldsymbol{M}(\boldsymbol{U}\boldsymbol{M})^{-1} & \boldsymbol{N} - \boldsymbol{M}(\boldsymbol{U}\boldsymbol{M})^{-1}\boldsymbol{U}\boldsymbol{N} \end{bmatrix} \begin{bmatrix} \boldsymbol{u}_{uc} \\ 1 \end{bmatrix} \tag{44}$$

The optimal duty cycles for the linear modulation stage are computed using the (3×3) matrix:

$$\boldsymbol{d}_{rj} = \frac{1}{\Delta}\begin{bmatrix} u_{1\beta} - u_{2\beta} & u_{2\alpha} - u_{1\alpha} & \boldsymbol{u}_1 \times \boldsymbol{u}_2 \\ u_{2\beta} - u_{s\beta} & u_{s\alpha} - u_{2\alpha} & \boldsymbol{u}_2 \times \boldsymbol{u}_s \\ u_{s\beta} - u_{1\beta} & u_{1\alpha} - u_{s\alpha} & \boldsymbol{u}_s \times \boldsymbol{u}_1 \end{bmatrix}\begin{bmatrix} u_{uc,\alpha} \\ u_{uc,\beta} \\ 1 \end{bmatrix} \tag{45}$$

where Δ is the determinant of matrix product $(\boldsymbol{UM})^{-1}$:

$$\Delta = \boldsymbol{u}_S \times \boldsymbol{u}_1 + \boldsymbol{u}_2 \times \boldsymbol{u}_S + \boldsymbol{u}_1 \times \boldsymbol{u}_2 \tag{46}$$

with $\boldsymbol{u}_x \times \boldsymbol{u}_y = u_{x\alpha}u_{y\beta} - u_{x\beta}u_{y\alpha}$ denoting the cross product.

5.2. Handling the Negative Duty Cycles: The Overmodulation Stage

In the previous section, the relaxed solution to the optimisation problem was calculated. The relaxed duty cycles vector, $\boldsymbol{d}_{rj}$, is the local solution for each region, $\mathcal{R}_j \in \mathcal{R}$, of the control hexagon, $\mathbb{V}$. The relaxed solution computed with (32a) and (32b) fulfills the equality constraint $\mathbf{1}^\intercal \boldsymbol{d} = 1$. Thus, all regions can be mapped onto $\boldsymbol{u}_{uc}$ in the $\alpha\beta$-plane. However, only one region fulfils the non-negativity constraint [24]. The non-negativity constraint can then be considered in the solution with a simple methodology (as reported in [24,26]). The methodology introduced therein also reduces the computational burden, avoiding the search over all 24 regions of the control region $\mathbb{V}$ to only four. The methodology will be explained in this section.

Firstly, considering the $\alpha\beta$-plane shown in Figure 4a with the space of vectors of the 3L-NPC converter is divided into 12 regions. The algorithm seeks the region where $\boldsymbol{u}_{uc}$ is located, and then the three sectors in that region are evaluated in the control algorithm. Given that $\boldsymbol{u}_{uc}$ is the desired solution of the optimisation problem, its angle is used to find the optimal region in the plane. The optimal sector, $\mathcal{S}^\star$, is obtained from the following equation:

$$S^\star = \text{floor}\left\{\frac{6}{\pi}\tan^{-1}\left(\frac{u_{uc,\beta}}{u_{uc,\alpha}}\right)\right\} + 1 \tag{47}$$

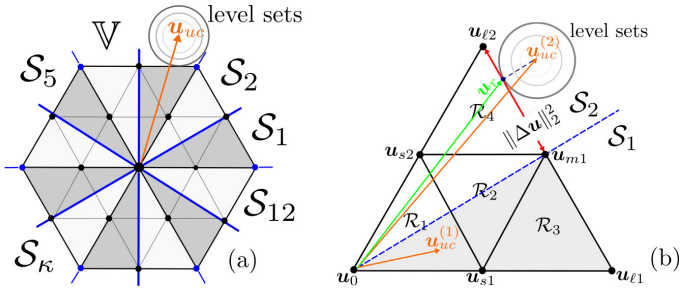

Figure 4. Control region of the 3L-NPC converter. (**a**) Hexagon divided into 12 sectors to reduce the computational burden of the OSS–MPC algorithm, and (**b**) close-up look into sectors $\mathcal{S}_1$–$\mathcal{S}_2$.

When the optimal sector is calculated, the duty cycles of the switching sequences contained in it are evaluated. The sector whose duty cycles complies with the non-negativity constraint is the optimal sector, and thus the optimal switching sequence is found.

The conventional enumeration algorithm can be reduced to only three regions after the sector has been identified. Each sector has three candidate switching sequences, but only one of them fulfils the non-negativity constraint. Thus, the optimal pair $\{\boldsymbol{U}^\star, \boldsymbol{d}^\star\}$ is found by evaluating the non-negativity condition over the duty cycles vector of each candidate region. However, if $\boldsymbol{u}_{uc}$ falls outside control region $\mathbb{V}$ (e.g., see $\boldsymbol{u}_{uc}^{(2)}$ in Figure 4b) then none of the candidate switching sequences fulfil the non-negativity constraint.

The aforementioned case occurs during a transient operation. The candidate switching sequence is then reduced to one and is built by the medium and large switching vectors belonging to the only outer region that intersects the optimal sector. The case is further analyzed in the next subsection.

5.2.1. Relaxed Optimisation Problem

The unconstrained average switching vector goes outside the hexagon, thus the duty cycle for the small switching vector becomes negative. Defining $d_{Sj} = 0$, the optimisation variable becomes

$$\boldsymbol{d}_j = \begin{bmatrix} 0 \\ d_{1j} \\ d_{2j} \end{bmatrix} \tag{48}$$

Consider the equality constraint

$$\mathbf{1}^\intercal \begin{bmatrix} 0 & d_{1j} & d_{2j} \end{bmatrix} = 1 \tag{49}$$

Notice that one of the two optimisation variables is dependent. Thus, if we set d_{2j} to be dependent of d_{1j}, we can find an auxiliary vector to reduce the equality-constrained optimisation problem into an unconstrained optimisation problem:

$$\boldsymbol{d}_j = \underbrace{\begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix}}_{\boldsymbol{M}'} d_{1j} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}}_{\boldsymbol{N}'} \tag{50}$$

Then, $\boldsymbol{u} = \boldsymbol{U}\boldsymbol{d} = \boldsymbol{U}\left(\boldsymbol{M}'\boldsymbol{d}_j + \boldsymbol{N}'\right) = (\boldsymbol{u}_1 - \boldsymbol{u}_2)d_1 + \boldsymbol{u}_2$ and $\boldsymbol{u}^\intercal = \boldsymbol{d}_j^\intercal \boldsymbol{U}^\intercal = \left(\boldsymbol{M}'\boldsymbol{d}_j + \boldsymbol{N}'\right)^\intercal \boldsymbol{U}^\intercal$ $(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal d_1 + \boldsymbol{u}_2^\intercal$. The cost function is

$$\begin{aligned} J = {} & (\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)d_1^2 \\ & + 2(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2 d_1 \\ & - 2(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{u}'_{db} + \lambda_u \boldsymbol{u}_{ss}\right)d_1 \\ & + \boldsymbol{u}_2^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2 - 2\boldsymbol{u}_2^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right) \\ & + \left(\boldsymbol{\kappa}^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}^\intercal \boldsymbol{u}_{ss}\right) \end{aligned} \tag{51}$$

5.2.2. Solution of the Relaxed Optimisation Problem

The unconstrained optimisation problem is solved by setting to zero the derivative of the cost function with respect to the optimisation variable:

$$\begin{aligned} \frac{d}{d(d_{1j})} J = {} & 2(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)d_1 \\ & + 2(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2 \\ & - 2(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right) = 0 \end{aligned} \tag{52}$$

Solving this for d_1 yields

$$d_1 = \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right)}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)} - \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)\boldsymbol{u}_2}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)(\boldsymbol{u}_1 - \boldsymbol{u}_2)} \tag{53}$$

The matrix $\left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)$ corresponds to a scalar multiplied by the identity matrix. Bearing on mind that $\boldsymbol{u}_{uc} = \left(\boldsymbol{Q}' + \lambda_u \boldsymbol{I}_2\right)^{-1}\left(\mathbf{B}_d^\intercal \boldsymbol{Q}\boldsymbol{\kappa} + \lambda_u \boldsymbol{u}_{ss}\right)$, the optimal duty cycle, $d_1^\star$, is

$$d_{1j}^\star = \frac{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_{uc} - \boldsymbol{u}_2)}{(\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_1 - \boldsymbol{u}_2)} \tag{54}$$

Notice that the denominator of $d_{1j}^\star$ is the length between a large and the medium vector in the hexagon frontier (see Figure 4b), thus,

$$\|\Delta \boldsymbol{u}\|_2^2 = (\boldsymbol{u}_1 - \boldsymbol{u}_2)^\intercal (\boldsymbol{u}_1 - \boldsymbol{u}_2) = \frac{4}{9} \tag{55}$$

Then, the optimal solution for the overmodulation stage is:

$$d_{1j}^{\star} = \text{mid}\left\{0, \frac{9}{4}(\boldsymbol{u}_1 - \boldsymbol{u}_2)^{\intercal}(\boldsymbol{u}_{unc} - \boldsymbol{u}_2), 1\right\} \tag{56a}$$

$$d_{2j}^{\star} = 1 - d_{1j} \tag{56b}$$

6. NP-Voltage Control and PWM Modulator

The objective of the NP-voltage control loop is to compute an optimal common-mode signal, $u_0^{\star}$, to balance the DC-link capacitors of the 3L-NPC converter.

The strategy assumes that a PWM stage is used to synthesize the solution obtained from the outer optimisation loop. To this end, the OSS $\boldsymbol{S}^{\star}$ is mapped into a three-phase reference signal, $\boldsymbol{D}_{abc} = [D_a\ D_b\ D_c]^{\intercal} \in [-1, 1]^3$, obtained as [26]

$$\boldsymbol{D}_{abc} = d_1^{\star}\boldsymbol{u}_{abc,1}^{\star} + d_2^{\star}\boldsymbol{u}_{abc,2}^{\star} + \frac{1}{2}d_S^{\star}\left(\boldsymbol{u}_{abc,0}^{\star} + \boldsymbol{u}_{abc,3}^{\star}\right) \tag{57}$$

in which $\boldsymbol{u}_{abc,\ell}^{\star} = \mathbf{T}_{\alpha\beta}^{-1}\boldsymbol{u}_{s\ell}^{\star}$ are the three-phase switching states that produce the OSS.

Finally, the three-phase reference signals sent to the PWM modulator are

$$\boldsymbol{D}_{abc}^{\star} = \boldsymbol{D}_{abc} + u_0^{\star} \tag{58}$$

where $u_0^{\star}$ is the optimal common-mode signal to be injected to reduce the NP-voltage tracking error. For further analysis and discussion of the methodology proposed to obtain the common-mode signal, the reader is referred to [26].

7. Hardware-in-the-Loop (HIL) Results

In this section, hardware-in-the-loop (HIL) results are shown to validate the proposed controller. The 3L-NPC converter, *LC* filter, and loads are emulated using PLECS-RT box 1 HIL platforms with a time-step of 5 µs. The control system is separately implemented using a dSPACE MicroLabBox platform. This dSpace controller is equipped with a Freescale QorIQ P5020 dual-core 2 GHz processor (DSpace Gmbh, Paderborn, Germany), for number crunching, and a Kintex-7 XC7K325-T FPGA. The FPGA handles the AD conversion, performs an in-phase disposition PWM strategy, and implements a dead time of 1 µs for each switching device; the HIL system is shown in Figure 5a. The processor computes the Clark transform of the measured three-phase variables, executes the optimisation algorithm, and computes the appropriate three-phase reference signals for the modulator. The loads considered for the study are a three-phase resistive load bank and a nonlinear load implemented using a three-phase diode rectifier with a capacitor and resistor connected in parallel at the DC side, as shown in Figure 5b. The parameters of the system are shown in Table 1 and are similar to those used in a previous work (see [27]).

Table 1. System Parameters.

Parameter	Value
Switching and sampling frequency	f_s = 20 kHz
DC-link voltage	V_{dc} = 700 V
LC filter	R_f = 1 mΩ L_f = 2.4 mH C_f = 15 µF
Load resistance	R_L = 30 Ω
Nonlinear load	L_n = 1.8 mH C_n = 2.2 mF R_n = 60 Ω
Filter current weight factor	λ_i = 0.25
Load-voltage weight factor	λ_v = 0.02

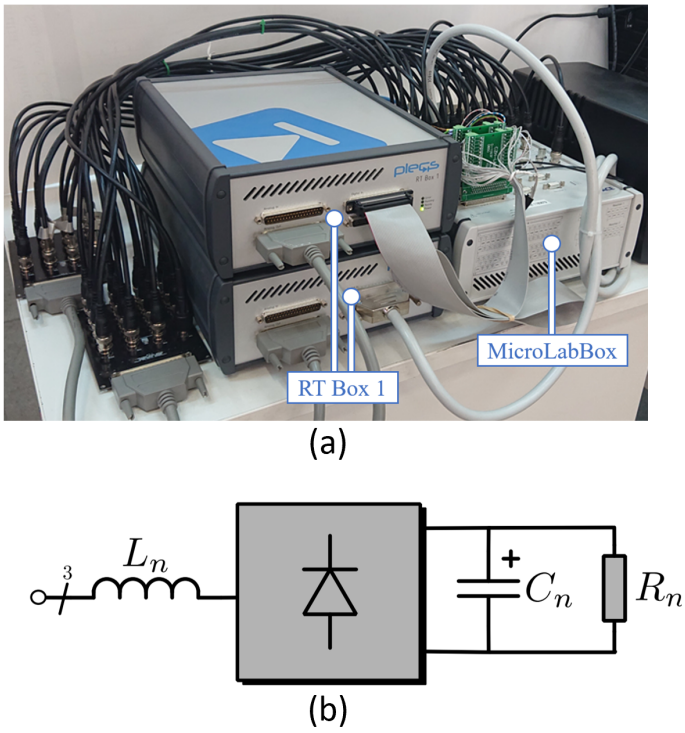

Figure 5. (**a**) HIL platform used to perform the experiments, (**b**) topology of the nonlinear load.

For the HIL results discussed in this section, the current of the nonlinear load used in some tests, corresponds to that shown in Figure 6; notice that the non-linear current is estimated in the processor using the auto-regressive model provided by the Lagrange polynomial shown in Equation (61). For the results shown in Figures 7–10, the weight related to the control effort is set to $\lambda_u = 0$. The effects of using different values of λ_u in the performance of the proposed control system are discussed using Figures 11 and 12.

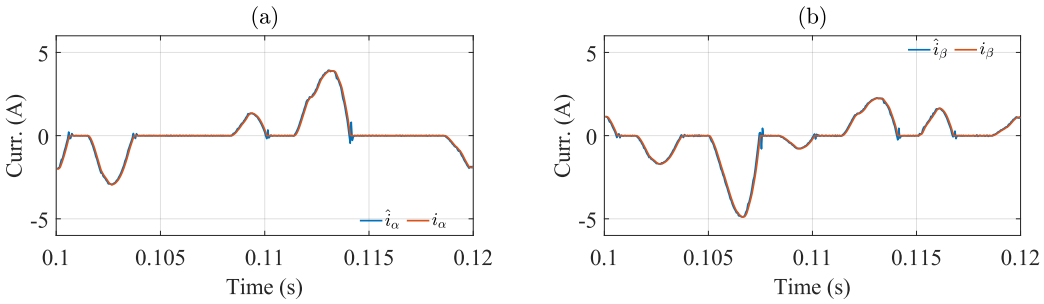

Figure 6. Estimated and measured current when a nonlinear load is connected: (**a**) $\alpha-$component of the load current, (**b**) $\beta-$component of the load current.

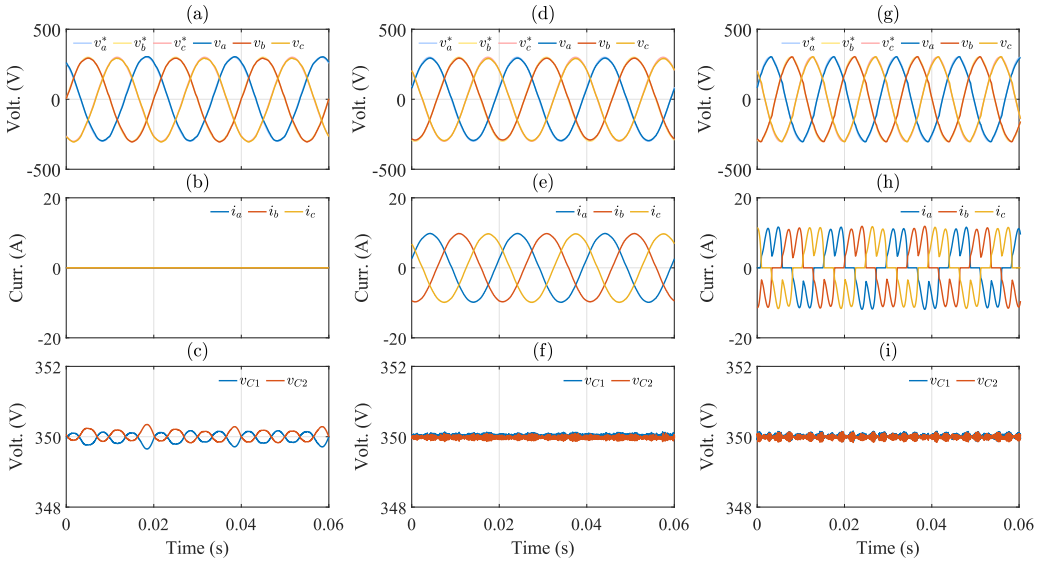

Figure 7. Steady–state results for different load conditions: (**a**,**d**,**g**) load output voltage without load, with resistive load and with nonlinear load, (**b**,**e**,**h**) load output current without load, with resistive load and with nonlinear load, (**c**,**f**,**i**) DC–link capacitor voltages without load, with a resistive linear load and nonlinear load.

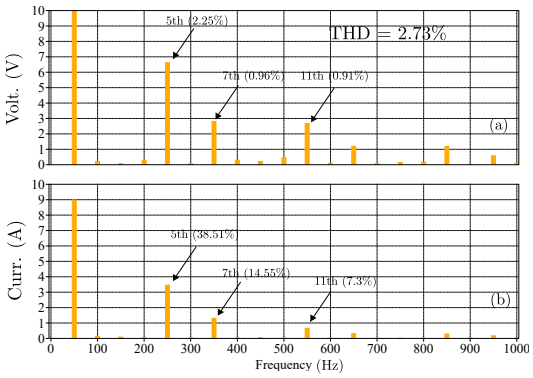

Figure 8. Harmonic spectrum of (**a**) load output voltage and (**b**) load output current when a nonlinear load is connected.

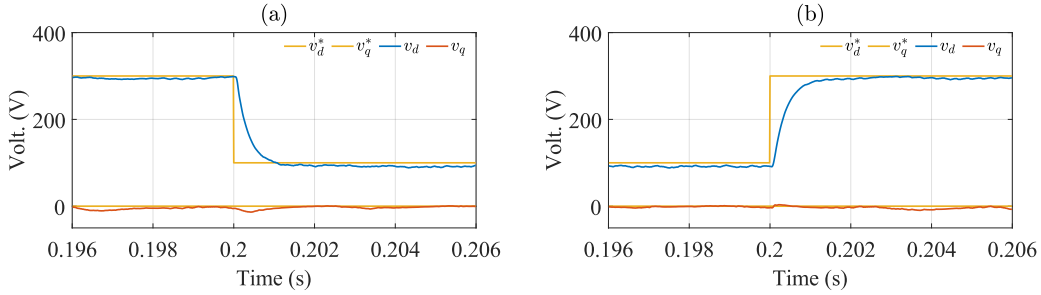

Figure 9. Transient operation of the system for reference voltage step: (**a**) voltage step from 300 (V) to 100 (V), (**b**) voltage step from 100 (V) to 300 (V).

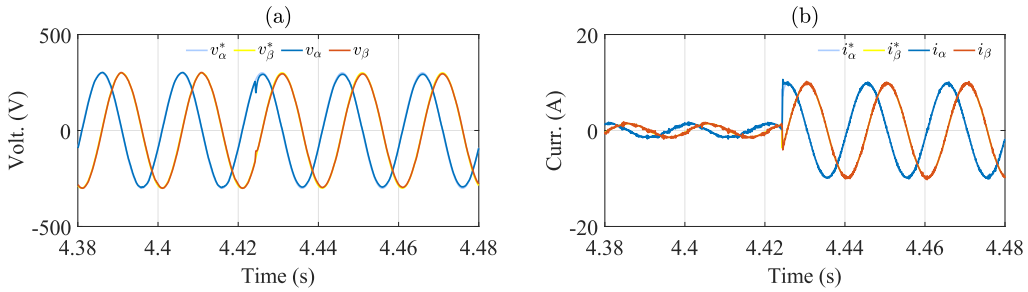

Figure 10. Transient operation of the system for a load step: (**a**) load output voltage, (**b**) filter inductor current.

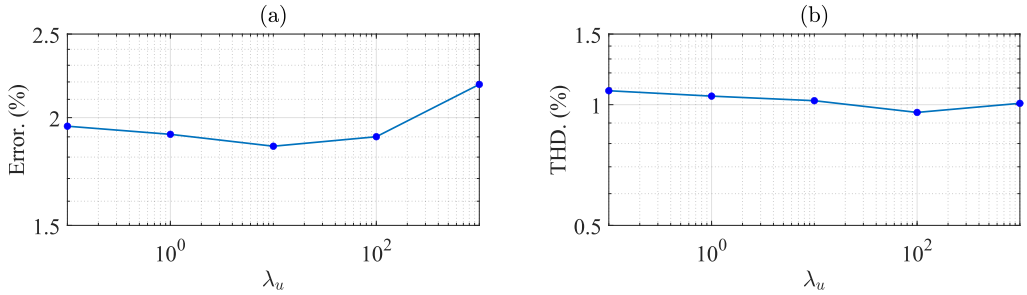

Figure 11. System performance over variation of λ_u: (**a**) Percentage of the effective (RMS) load voltage tracking error respect to the λ_u variation, (**b**) Total harmonic distortion of the load voltage, considering a wide λ_u variation.

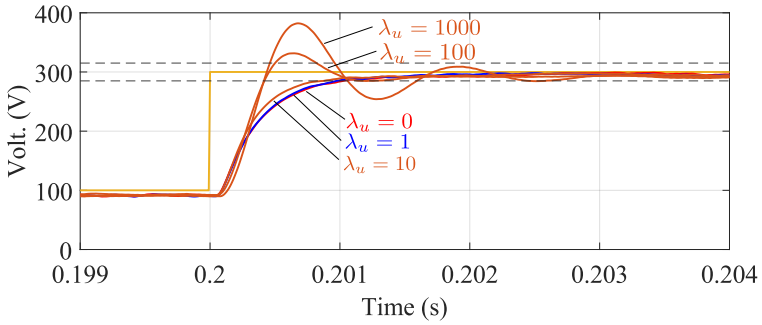

Figure 12. Transient operation of the system for different values of λ_u.

The performance of the controllers is evaluated using the following goodness factors: RMS error (RMSE), percentage of voltage error (E_v), and total harmonic distortion (THD). The percentage of error is defined as follows:

$$E_v[\%] = \frac{100}{\|\boldsymbol{v}^*\|}\sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{P}}\|\boldsymbol{v}(k)-\boldsymbol{v}^*(k)\|_2^2} \tag{59}$$

where $\mathcal{P} = \{1, 2, \ldots, N_p\}$ is the set of indices of the measurements vector and $N_p = T_1/T_s$ is the total number of elements in the vector. T_1 is the period of the fundamental frequency and T_s is the period of the sampling frequency. Whenever the desired reference amplitude is unknown, the root-mean-square error (RMSE) will be used. The RMS error is defined as follows:

$$\text{RMSE}(\boldsymbol{x}-\boldsymbol{x}^*) = \sqrt{\frac{1}{N_p}\sum_{k\in\mathcal{P}}\|\boldsymbol{x}(k)-\boldsymbol{x}^*(k)\|_2^2} \tag{60}$$

A one-step delay compensation is carried out to compensate for the computational delay introduced by the digital platform. The state vector, $\boldsymbol{x}_s[k+1]$, is computed using (20) with the values measured at the kth instant and the switching sequence applied during the

previous switching interval. The voltage reference, $\boldsymbol{v}_o[k+1]$, is computed by shifting the phase of the reference signal one step ahead. The load output current, $\boldsymbol{i}_o[k+1]$, is estimated using the Lagrange extrapolation technique. The Lagrange extrapolation technique uses the actual and past measurements of the signal to estimate its future value. The load output current, $\boldsymbol{i}_o[k+1]$, is computed as follows [41]:

$$\boldsymbol{i}_o[k+1] = 4\boldsymbol{i}_o[k] - 6\boldsymbol{i}_o[k-1] + 4\boldsymbol{i}_o[k-2] - \boldsymbol{i}_o[k-3] \tag{61}$$

The estimated load output current has an RMS error of 0.0603 (A) in the α-component, and 0.0640 (A) in the β-component for the worst-case scenario (nonlinear load). The estimated and measured load output current are shown in Figure 6. As shown in this figure, the estimated current tracks the measured current relatively well.

In Figure 7a, the output voltages when the system operates without load are shown. The reference voltage has an amplitude of 300 V with a frequency of 50 Hz. For this condition, the load output voltages have a voltage error of 2.04% and a THD of 1.74%. Then, a three-phase resistive load is connected as in Figure 7d. In this condition, the voltage error is 2.05% and the THD is 1.03%. When a nonlinear load is connected, as in Figure 7g, the voltage error is 2.83%. The harmonic spectrum for the load output voltage and load output current are shown in Figure 8a,b. The voltage THD in this case is 2.73% with the presence of 5th and 7th harmonics, which are produced by the bridge rectifier. In Figure 7b–h, the load output current is shown for the three aforementioned cases. Finally, in Figure 7c–i the DC-link capacitor voltages are shown. The control strategy is capable of keeping the DC-link voltages balanced and well regulated for all operating conditions, with very small oscillations.

The transient operation of the controlled system is studied in Figure 9, considering changes in the reference voltage amplitude with $\lambda_u = 0$. The variables are presented in the synchronous reference frame to verify the settling time of the load output voltage.

The settling time is computed as the time required by the output voltage to reach and stay within 5% of the desired voltage. In Figure 9a, the reference voltage receives a step variation from 300 V to 100 V at t = 0.2 s. The voltage error amounts to 5.98% under steady-state conditions. The rise in voltage error results from the reduction in the amplitude of the reference voltage. In Figure 9b, the reference voltage varies from 100 V to 300 V at t = 0.2 s. In this case, the load output voltage manages to stay within the band of 5% around the desired voltage. Thus, the settling time is approximately 1.03 ms .

Notice that a relatively low steady-state error is presented in the HIL results shown in Figure 9a,b. This small steady-state error is produced because there is not an integrator in the MPC algorithm [42,43]. If the steady-state error is a must, then the state-space matrix, $\boldsymbol{A}$ (see (7)), must be augmented with additional states to represent the integrator [42]; however, this topic is considered to be outside the scope of this work.

Figure 10 shows the operation of the system for a load step. A dip occurs in the load output voltage, as shown in Figure 10a, and takes approximately 1 ms to recover. Notice that there is a sudden increase in the inductor reference current to approximately 10 A, and the current features a fast dynamic response to the step change.

The cost function of (30) has two terms: the first term penalizes the deviation of the system states from a reference vector and the second term penalizes the control effort of the converter. The control effort is penalized in the cost function by the deviation between the optimisation variable, $\boldsymbol{u}(k)$, and the steady-state control effort, $\boldsymbol{u}_{ss}$. The weight of this deviation on the optimisation problem is set by the parameter λ_u. Increasing λ_u will lead the converter's response to move closer to open-loop operation since $\boldsymbol{u}_s s$ depends only on the load reference voltage and load output current. The system's performance with a logarithmic variation of parameter λ_u is shown in Figure 11. The results are obtained considering a three-phase resistive load at the LC filter terminals. The best trade-off in terms of voltage error between open-loop and closed-loop operation of the converter is achieved when $\lambda_u = 10$, as shown in Figure 11a. When λ_u is increased, the response of the

system tends toward $\boldsymbol{u}_{ss}$, which does not penalize the voltage error. Thus, the voltage error increases.

As shown in Figure 11b, the voltage THD presents slight variations around 1%, as shown in Figure 11b. The system's transient response is also dependent on the value of λ_u. A trade-off between settling time and overshoot must be reached, as shown in Figure 12. Increasing λ_u up to 100 will reduce the settling time of the system but increase the voltage overshoot. However, for $\lambda_u >> 100$, the system response will present a damped sinusoidal oscillation which increases the settling time.

8. Comparison with a Previously Reported OSS-MPC Algorithm

In this section, the proposed scheme is compared with the prior OSS–MPC method discussed in [27]. In that publication, it is proposed to regulate the voltage in the *LC*-filtered load without considering a term weighting the control effort. This is similar to using $\lambda_u = 0$ in (30). In addition to ignoring the control effort, regulation of the converter's output current is not considered in [27]. For the comparison, simulation work using PLECS 4.7 software has been performed.

Figure 13 shows simulation results considering a step change from 0 to 300 V in the load voltage for both control strategies, i.e., the one published in [27] and that proposed in this work. In this case, the value λ_u in (30) has been set to 0. As shown in Figure 13a, the proposed method presents neither overshoot nor noticeable oscillation in the load voltages, as opposed to the results obtained with the OSS–MPC of [27] (see Figure 13a,c). The smooth transition in the load voltage is obtained by the utilisation of the cost function of (30), which considers the inductor current and output voltage tracking errors. Moreover, the utilisation of a term in the cost function weighting the output-current tracking error produces a considerably smaller current peak (16.35 A, see Figure 13b) when compared to the 32.1 A obtained for the method of [27] (see Figure 13d). The proposed method also has a slightly faster response, taking 0.81 ms to reach steady-state in Figure 13. Meanwhile, the prior OSS–MPC method takes 0.83 ms to reach steady-state.

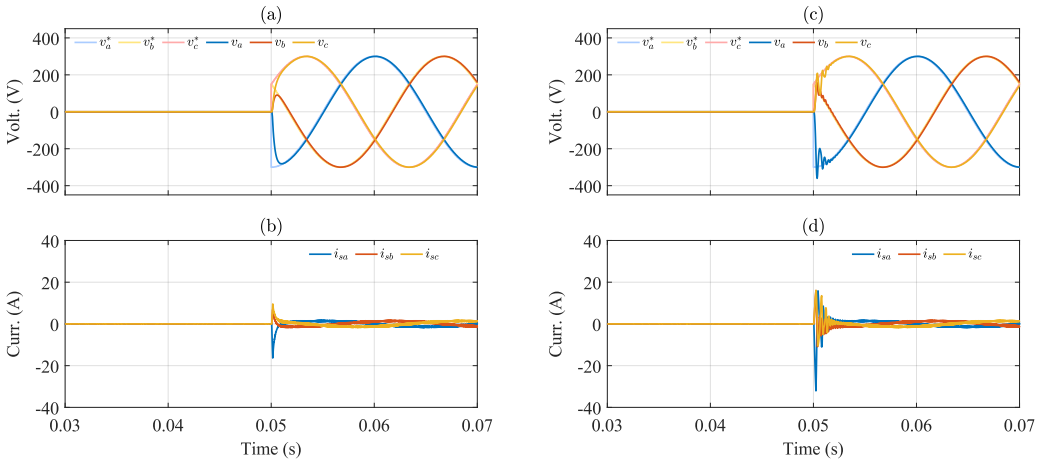

Figure 13. Simulation of the system performance when the reference voltage is changed from 0 V to 300 V: (**a**) output capacitor voltages with the proposed method, (**b**) inductor currents with the proposed method, (**c**) output capacitor voltages with prior OSS–MPC [27], (**d**) inductor currents with prior OSS–MPC [27].

An amplified view of Figure 13 is shown in Figure 14. The effects produced by neglecting an output current-related term, in the cost function of [27], are clearly shown in Figure 14c,d. A large peak current, as well as relatively large undamped current oscillations, are produced for ≈1.2 ms after the step change. These large current oscillations affect the quality of the load-output voltage. Notice the smooth variation in the output voltages produced when the control method proposed in this work is applied. This is shown in Figure 14a,b.

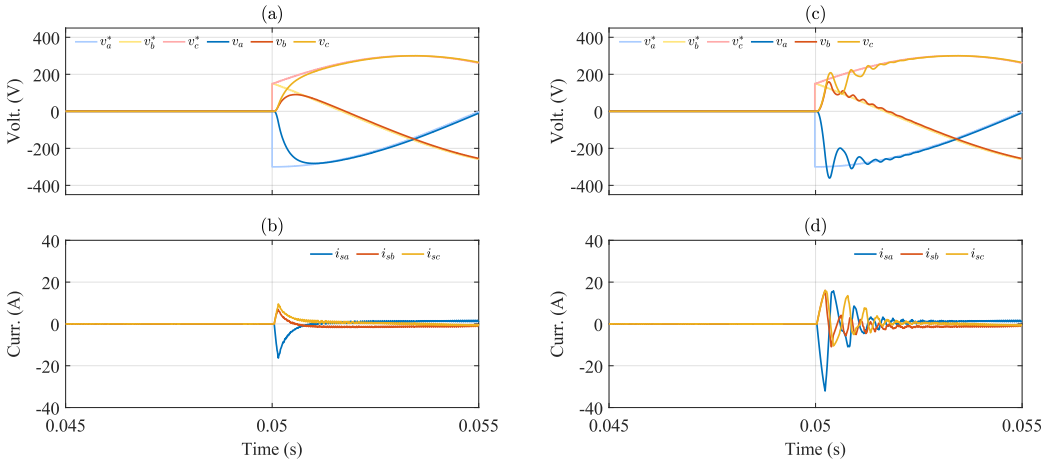

Figure 14. Amplification of Figure 13: (**a**) output capacitor voltages with the proposed method, (**b**) inductor currents with the proposed method, (**c**) output capacitor voltages with prior OSS–MPC [27], (**d**) inductor currents with prior OSS–MPC [27].

The performance of the control systems has also been tested considering a balanced load step of 30 Ω in t = 0.1 s. Before the step, the system is operating without a load parallel connected with the capacitor of the *LC*-filter. Figure 15a,b shows the performance obtained with the OSS–MPC strategy proposed in this work; meanwhile, Figure 15c,d shows the results obtained with the work reported in [27]. Again, the peak current overshot shown in Figure 15b is smaller than that of Figure 15d, with peak values of approximately 14.5 A and 21.5 A, respectively. The control strategy of [27] has a smaller dip in the load voltage for the step in t = 0.1 s; however, this better performance is obtained because neither the control effort nor the peak currents are considered in the cost function reported in that work. Moreover, as discussed previously for the results presented in Figure 14d, lightly damped current oscillations are produced after the load step, as depicted in Figure 15d. These current oscillations also affect the load voltage, as shown in Figure 15c, for the time immediately after t = 0.1 s. It is concluded that, for the load step change, the performance of the proposed control system is better than that of [27], which is shown in Figure 15c,d. The peak current is lower and the lightly damped oscillations in the currents and voltages are completely avoided, as depicted in Figure 15a,b.

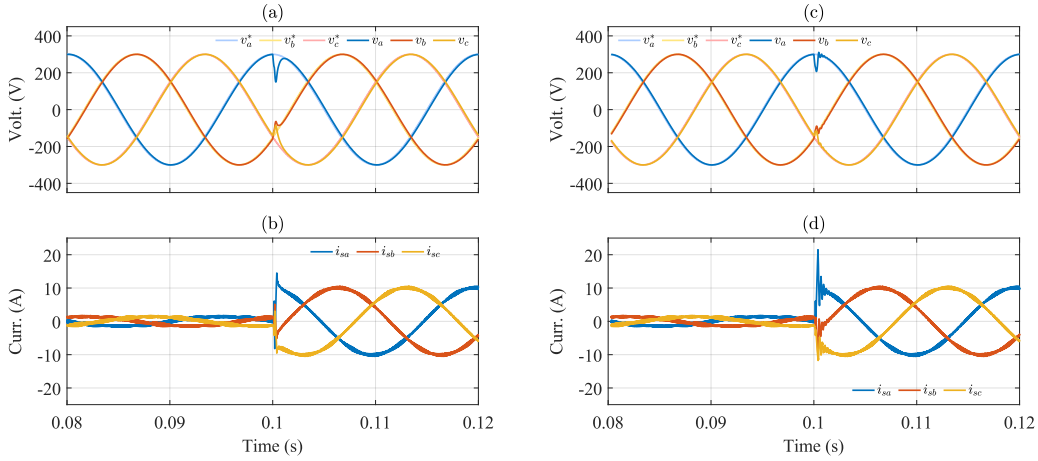

Figure 15. Simulation of the system performance when a linear load is connected: (**a**) output capacitor voltages with the proposed method, (**b**) inductor currents with the proposed method, (**c**) output capacitor voltages with prior OSS–MPC [27], (**d**) inductor currents with prior OSS–MPC [27].

The performance of the proposed control system is also clearly superior to that reported in [27], when the nonlinear load of Figure 5b is connected at the output of the

LC-filter. The simulation results are shown in Figure 16a,b; before $t \approx 0.05$, the capacitor at the nonlinear load is completely discharged and it is equivalent to a short circuit immediately after the nonlinear load is connected at $t \approx 0.05$ s. Therefore, the control system reported in [27] has a bad performance because neither current control nor current limitation is considered in the cost function reported in that paper. Hence, the current shown in Figure 16b reaches a peak value of 297.2 A; meanwhile, the peak current achieved by the OSS–MPC algorithm reported in this work is 33 A. Of course, with this large current the control strategy of [27] manages to regulate the load voltage in approximately 20 ms vs. 80 ms for the proposal, but it is unlikely that the power converter and *LC* filter could withstand this large output current surge. Therefore, the lack of current regulation is certainly a very strong drawback of the control strategy being compared with the MPC scheme reported in this work.

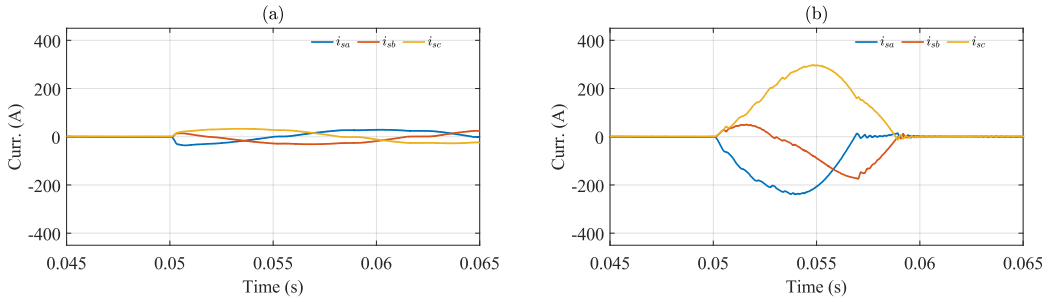

Figure 16. Simulation of the system performance when a nonlinear load is connected at the output of the *LC* filter: (**a**) inductor currents with the proposed method, (**b**) inductor currents with prior OSS–MPC [27].

9. Conclusions

In this paper, an optimal switching sequence MPC algorithm was proposed for a three-level neutral-point-clamped inverter with an output *LC* filter. The strategy is an extension of the cascaded optimal switching sequence MPC proposed in the literature for current and direct power control of active front-end 3L-NPC inverters. The control objectives of the algorithm were twofold: (1) achieve good tracking performance for the *LC* filter variables (current and voltages) and (2) maintain a balanced neutral-point voltage between the DC-link capacitors of the converter using the algorithm already reported in [26]. To achieve the objectives, the strategy solves two cascaded optimisation problems. The first optimisation problem—called the outer optimisation loop—computes the optimal sequence of switching vectors and their corresponding duty cycles to achieve the objectives related to tracking the AC side variables. Then, the optimal solution of the outer optimisation loop reported previously in [26] is used to compute an optimal common-mode signal designed to balance the neutral-point voltage between the DC-link capacitors.

As discussed in the final paragraphs of Section 3.2.1 of this work, the standard forward-Euler implementation typically used for predictive control has some problems implementing a single-stage OSS–MPC algorithm regulating the current and voltage of a load connected to an *LC*-filtered 3L-NPC converter, because the unconstrained solution is weakly dependant on the load-voltage tracking error. Therefore, a two-step horizon has to be considered, or another discretisation methodology, as the improved forward-Euler has to be selected. Therefore, a discrete-time model based on the improved-Euler discretisation method was used to predict the future values of the state-vector trajectory. Notice that this methodology allows the implementation of a single-stage MPC algorithm to regulate the load voltage and the converter output current.

Experimental results are provided to validate the performance of the proposed strategy using the PLEXIM hardware-in-the-loop (HIL) platform RT Box 1 to emulate the power electronics stage, and the control algorithm was executed by the dSPACE MicroLabBox control platform. Three cases were considered in steady-state operation: (1) system performance without load, (2) system performance with linear load, and (3) system performance

with nonlinear load. In all cases, the MPC algorithm is capable of achieving good tracking of the load-voltage reference with a small error and low THD. In addition, the strategy is capable of maintaining well-balanced voltages at the DC-link capacitors. Moreover, the performance of the proposed control system has been compared with that obtained from the work reported in [27] using simulations. For all the tests performed, i.e., step changes in the output voltage, step changes in the load voltage, and operation with a nonlinear load at the output, the proposed control system has consistently outperformed the results obtained with the control strategy of [27].

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Abbreviations

The following abbreviations are used in this manuscript:

7S-SS	Seven Segments Switching Sequence
DC	Direct Current
AC	Alternate Current
FPGA	Field Programmable Gate Array
FCS-MPC	Finite Control Set Model Predictive Control
M^2PC	Modulated Model Predictive Control
HIL	Hardware-in-the-Loop
LC-filter	Inductance Capacitor Filter
MIMO	Multiple-Input–Multiple-Output
MPC	Model Predictive Control
NPC	Neutral Point Clamped
OSS	Optimal Switching Sequence
OSV	Optimal Switching Vector
PWM	Pulse Width Modulation
RT	Real Time
SISO	Single-Input–Single-Output
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
VFD	Variable Frequency Drives

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