Journal of Instrumentation

Measurement of UKRI-MPW0 after irradiation: an HV-CMOS prototype for high radiation tolerance

Published by IOP Publishing for Sissa Medialab

Received: *November 3, 2023*
Accepted: *February 12, 2024*
Published: *March 27, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

Measurement of UKRI-MPW0 after irradiation: an HV-CMOS prototype for high radiation tolerance

C. Zhang,* **J. Hammerich**, **S. Powell**, **E. Vilella** and **B. Wade**

Department of Physics, University of Liverpool,
Oliver Lodge Building, Oxford Street, Liverpool L69 7ZE, U.K.

E-mail: chenfan@liverpool.ac.uk

Abstract: UKRI-MPW0 was developed to further improve the radiation tolerance of HV-CMOS pixel sensors. It implements a novel sensor cross-section that uses backside-only biasing to allow high substrate bias voltages > 600 V. In this contribution, the measured results of irradiated UKRI-MPW0 samples are presented, including their current-to-voltage (I-V) characteristics, depletion depth and pixel performance. The chip is proved to have survived high radiation fluence of 3×10^{15} n_{eq}/cm^2.

Keywords: Particle tracking detectors (Solid-state detectors); Radiation-hard detectors

*Corresponding author.

https://doi.org/10.1088/1748-0221/19/03/C03061

2024 JINST 19 C03061

Contents

1 Introduction

High-Voltage CMOS (HV-CMOS) is a promising sensor technology for future tracking and vertexing applications, due to its advantages in material budget, fabrication cost, pixel granularity, time resolution and radiation tolerance [1]. Its monolithic structure, which integrates the sensor together with the readout electronics into the same substrate, eliminates the need for bump-bonding and makes the pixel granularity not restricted by the bump bond size. Its single silicon layer (can be thinned to $< 100\,\mu m$) reduces the material budget. By biasing the silicon substrate to a high voltage, the depletion region increases hence improving the sensor radiation tolerance. Due to the energy and luminosity increase (to $\sim$ TeV and $\sim 10^{34}\,cm^{-2}\,s^{-1}$) in future experiments, pixel detectors will be exposed to unprecedented radiation environments [2]. To meet the requirements of future experiments, the radiation tolerance of HV-CMOS sensors needs to be further improved. An HV-CMOS prototype, UKRI-MPW0 as shown in figure 1, is developed with the aim of achieving this goal. It increases the bias voltage that can be applied to the substrate to unprecedented values ($> 600\,V$), given examples of 250 V (AstroPix [3]) and 460 V (LF-Monopix2 [4]). This was achieved with a novel sensor cross-section that uses backside biasing only.

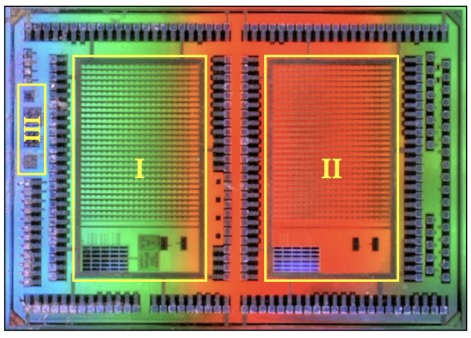


Figure 1. UKRI-MPW0, composed of two pixel matrices (I and II) and test structures (III).

This paper presents the design of UKRI-MPW0 in section 2 with an explanation of the cross-section and a brief introduction of its pixel matrix. In order to characterise the radiation tolerance, UKRI-MPW0 samples have been irradiated to various neutron fluence (up to $1 \times 10^{16}\,n_{eq}/cm^2$). The

2024 JINST 19 C03061

measurements of irradiated samples are presented in section 3 including their current-to-voltage (I-V) characteristics and edge-TCT results. Section 4 shows the pixel performance after irradiation.

2 Design of UKRI-MPW0

UKRI-MPW0 uses the 150 nm HV-CMOS process from LFoundry S.r.l. Figure 2 shows the sensor cross-section of the chip. The sensing diode for particle detection is formed by a Deep N-type WELL (DNWELL) in a p-type substrate which is biased to a negative high voltage. The DNWELL not only collects charges generated by particle hits, but also isolates the enclosed readout electronics from the substrate. There is no p-type contact to the substrate on the topside of sensor and the high voltage can only be applied from the contact implanted on the backside. With this novel cross-section, the distance between the high voltage p-type contacts and low-voltage DNWELL becomes the thickness of the sensor, hence leading to a higher breakdown voltage [5]. Since the depletion region width W_d is related to bias voltage V_{bias} and substrate resistivity ρ_{sub} as $W_d \propto \sqrt{\rho_{sub} \cdot V_{bias}}$, higher biasing voltages allow for a substantial depletion in the sensor even after high radiation fluence. Therefore, UKRI-MPW0 is expected to achieve improved radiation tolerance.

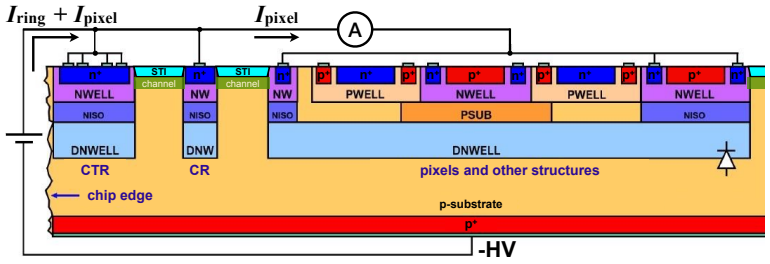


Figure 2. Sensor cross-section of UKRI-MPW0 near the chip edge, and the configuration for I-V measurement. Two n-type rings are implemented around the chip edge: a Current Terminating Ring (CTR) which collects most of the leakage current caused by edge defects and serves as a seal ring; a Clean-up Ring (CR) which collects the remaining stray charge from the edge. This double-ring structure prevents the edge leakage current from affecting the charge collection of pixels [6].

UKRI-MPW0 samples are fabricated on two high-resistivity wafers (1.9 kΩ · cm). The two wafers were firstly thinned to 280 µm, then backside processed using two different methods:

1. A p^+ layer as substrate contact was implanted on the backside using Beam-Line Ion Implantation (BLII) and activated by Rapid Thermal Annealing (RTA);
2. The backside p^+ contact was added using Plasma-Immersion Ion Implantation (PIII) and activated by UV laser annealing.

UKRI-MPW0 is mainly composed of the following parts and more detailed description of the chip design can be found in [5].

I. A 20×29 pixel matrix including 3 pixel flavours with a pixel size of 60 µm × 60 µm;

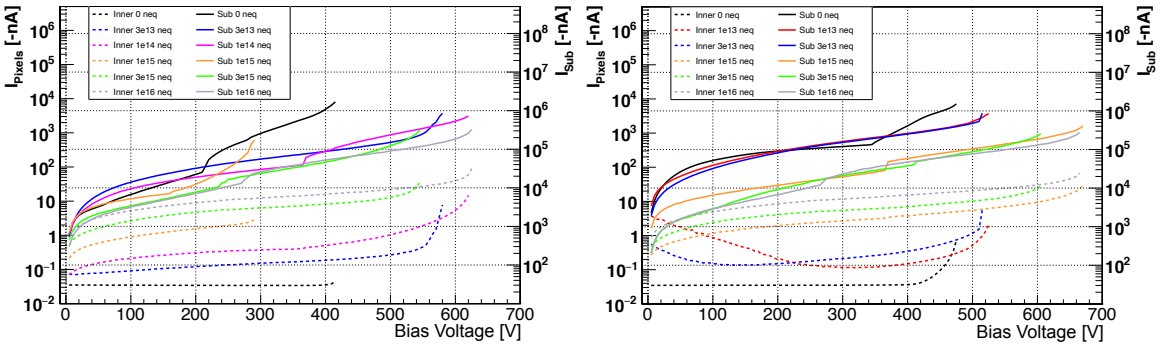
II. A copy of matrix I, which uses two Enclosed Layout Transistors (ELTs) instead of linear transistors inside each pixel for higher radiation tolerance;

III. Test structures for I-V and edge-Transient Current Technique (edge-TCT) measurements.

2024 JINST 19 C03061

3 I-V and edge-TCT results of irradiated samples

The performance of the UKRI-MPW0 sensing diode was evaluated by characterising its leakage current, breakdown voltage and depletion depth. The I-V curves were measured on PCBs with a cooling setup, and the depletion depth with an edge-TCT setup [7]. Figure 3 shows the I-V curves of samples before and after neutron irradiation up to $1 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$ fluence. As shown in figure 2, the I-V measurement configuration records both the leakage currents of a single pixel and the chip rings. A current compliance of 1 mA was used in the measurements, which was reached by the ring currents due to the large leakage current caused by edge defects. With higher radiation fluence, the pixel leakage current increases, which was due to the lattice damage in the silicon substrate. On the contrary, the ring current decreases with the fluence as the chip edge is passivated by irradiation and becomes less conductive. The decrease in the ring leakage currents makes them reach the compliance at larger voltages, thus allowing the chips to be biased to higher voltages ($> 600\,\mathrm{V}$). The high leakage currents add a non-negligible power consumption with high bias voltages. In the case of the highest fluence at 400 V, the ring dissipates $0.1\,\mathrm{mA} \times 400\,\mathrm{V} = 40\,\mathrm{mW}$, and the leakage of a pixel dissipates $10\,\mathrm{nA} \times 400\,\mathrm{V} = 4\,\mu\mathrm{W}$ when the in-pixel readout electronics consumes $20\,\mu\mathrm{W}$.



(a) BLII + RTA.

(b) PIII + UV laser.

Figure 3. I-V curves of samples before and after irradiation, including the leakage currents of single pixels (dashed lines) and the chip rings (solid lines). Results for samples treated with the two backside processing methods are included. Data were taken when samples were cooled to −25 °C.

The depletion depths at different bias voltages for samples before and after irradiation are shown in figure 4. At fluence $\leqslant 1 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$, the samples are fully depleted with bias voltage $> 300\,\mathrm{V}$. With higher fluence, the depletion depth is reduced, however a 50 µm depletion depth is still achieved with the high fluence of $1 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$.

4 Pixel performance after irradiation

The three pixel flavours in the pixel matrix are continuous-reset pixel, switched-reset pixel and modulated-reset pixel. The first two pixel flavours have been implemented and tested in a previous prototype [9, 10]. The modulated-reset pixel is dedicated to improving the timing resolution, and will be published elsewhere. Each pixel includes a charge sensitive amplifier and a discriminator. The discriminator determines a particle hit by comparing the amplifier output signal with a threshold voltage. The continuous-reset pixel has its comparator output signal proportional to the input charge and

2024 JINST 19 C03061

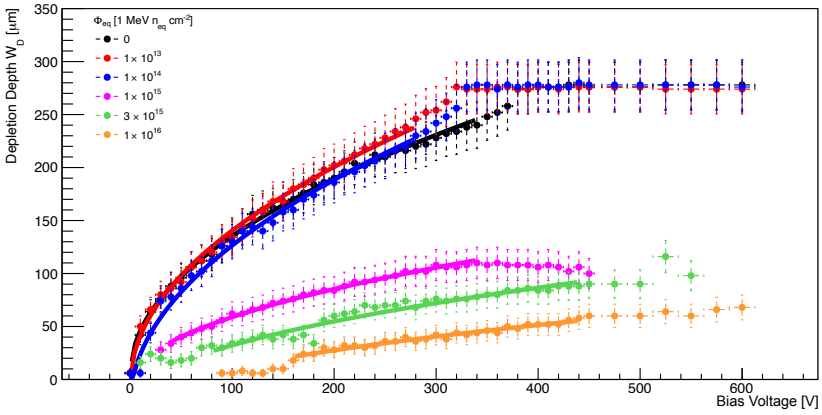
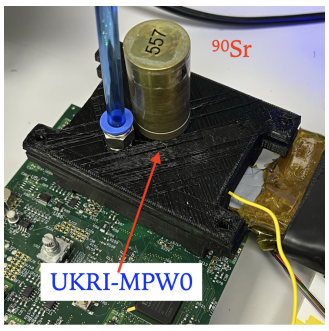


Figure 4. Depletion depth as a function of the bias voltage for unirradiated and irradiated UKRI-MPW0 samples (BLII + RTA) [8].

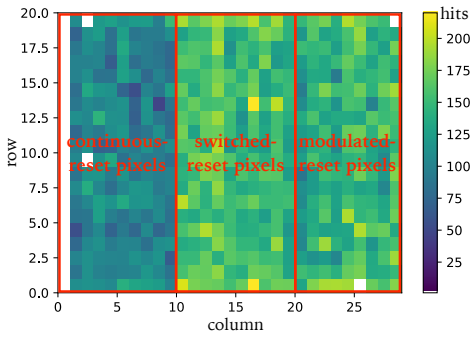
therefore can use the Time over Threshold (ToT) to measure the collected charge. The switched-reset pixel has much shorter event processing time (< 25 ns), and therefore is interesting for applications where excellent occupancy is required.

The Data AcQuisition (DAQ) for the pixel matrix is based on the Caribou system [11]. UKRI-MPW0 has no address-based readout, instead it provides one comparator output per column. In order to address the output signals from the 29 columns, and to measure the ToT and count the number of hits, these signals are routed to an FPGA which implements the digital readout at the PCB level. The FPGA on the chipboard uses a custom firmware to decode and measure the ToT of each comparator signal simultaneously and count the number of hits. All the measured results presented next are obtained with the samples backside processed with the BLII + RTA method.

A ^{90}Sr source was used to test the pixel matrix as shown in figure 5(a). The number of hits detected by pixels within 20 s was recorded. The hit map in figure 5(b) shows the switched-reset pixels (columns 11–20) detected more hits than the other pixel flavours, this is because of their larger gain as evaluated in [10].



(a) Setup for hit map measurement.



(b) Hit map of an unirradiated sample.

Figure 5. Record the number of hits detected by pixels over a window of 20 s and plot the hit map, when the chip was exposed to a ^{90}Sr source. A 400 V bias voltage and 200 mV threshold were used.

Figure 6 plots the curves of hit number as a function of the bias voltage for samples that are unirradiated and irradiated to different fluence. The hit number increases with the bias voltage due

2024 JINST 19 C03061

to larger depletion depth and is influenced by the irradiation as it weakens the depletion which is in accordance with figure 4.

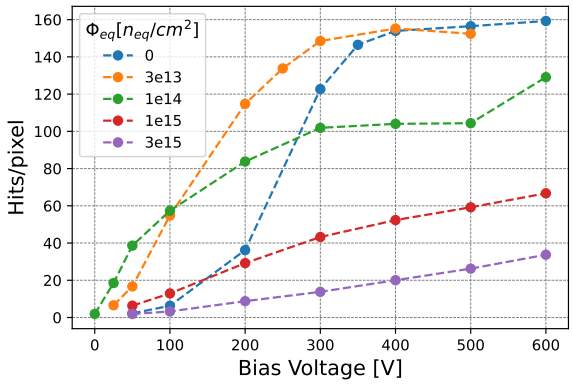


Figure 6. Average hits detected by the switched-reset pixels as a function of the bias voltage for samples before and after irradiation.

The performance of in-pixel readout electronics is tested by analysing the S-curve response of each pixel to injection pulses when the chip is biased to 400 V. Table 1 lists the mean values of Equivalent Noise Charge (ENC) and gain extracted from S-curves for the samples measured in figure 6. Since the neutron irradiation has little impact on CMOS circuitry, the change in the performance with radiation fluence is related with the parasitic capacitance between DNWELL and substrate. The radiation reduces the depletion depth, thus increasing the parasitic capacitance, which results in higher noise and lower gain.

Table 1. Mean values of ENC and gain of the continuous-reset pixels for samples before and after irradiation.

Φ_{eq} [n_{eq}/cm^2]	0	3e13	1e14	1e15	3e15
ENC [e^-]	140	145	151	170	175
gain [mV/ke^-]	96	94	89	87	84

5 Conclusion

UKRI-MPW0 is a prototype with a novel sensor cross-section to further improve the performance of HV-CMOS sensors. With its backside-only biasing scheme, the chip can be biased to an unprecedented high voltage of > 600 V. Measurements on irradiated samples show UKRI-MPW0 is able to achieve a 50 µm depletion depth after high radiation fluence of 1×10^{16} n_{eq}/cm^2, and its pixels are fully functioning after fluence of 3×10^{15} n_{eq}/cm^2.

Acknowledgments

This work has received funding from UK Research and Innovation (UKRI) under the grant reference MR/S016449/1.

2024 JINST 19 C03061

References

[1] I. Perić et al., *High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments*, *Nucl. Instrum. Meth. A* **731** (2013) 131.

[2] E. Sicking, *Detector requirements for future high-energy collider experiments*, in the proceedings of the 15^{th} *Trento Workshop on Advanced Silicon Detectord*, Vienna, Austria, 17–19 February 2020, https://indi.to/yBwWf.

[3] I. Perić, *HVCMOS Sensors*, in the proceedings of the 14^{th} *Terascale Detector Workshop*, 21–25 February 2022, https://indico.desy.de/event/32537/contributions/114360/.

[4] M. Barbero et al., *Radiation hard DMAPS pixel sensors in 150 nm CMOS technology for operation at LHC*, 2020 *JINST* **15** 05 [arXiv:1911.01119].

[5] C. Zhang et al., *Design and evaluation of UKRI-MPW0: An HV-CMOS prototype for high radiation tolerance*, *Nucl. Instrum. Meth. A* **1040** (2022) 167214.

[6] E. Noschis, V. Eremin and G. Ruggiero, *Simulations of planar edgeless silicon detectors with a current terminating structure*, *Nucl. Instrum. Meth. A* **574** (2007) 420.

[7] G. Kramberger et al., *Investigation of Irradiated Silicon Detectors by Edge-TCT*, *IEEE Trans. Nucl. Sci.* **57** (2010) 2294.

[8] B. Wade et al., *Edge-TCT evaluation of high voltage-CMOS test structures with unprecedented breakdown voltage for high radiation tolerance*, 2022 *JINST* **17** C12017.

[9] C. Zhang et al., *Development of RD50-MPW2: a high-speed monolithic HV-CMOS prototype chip within the CERN-RD50 collaboration*, *PoS* **TWEPP2019** (2020) 045.

[10] R. Marco Hernández, *Latest Depleted CMOS Sensor Developments in the CERN RD50 Collaboration*, *JPS Conf. Proc.* **34** (2021) 010008.

[11] T. Vanat, *Caribou — A versatile data acquisition system*, *PoS* **TWEPP2019** (2020) 100.

2024 JINST 19 C03061