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Original article

New analysis of VSC-based modular multilevel DC-DC converter with low interfacing inductor for hybrid LCC/VSC HVDC network interconnections

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ABSTRACT

The integration of multiterminal hybrid HVDC grids connecting LCC- and VSC-based networks faces several technical challenges such as DC fault isolation, ensuring multi-vendor interoperability, managing high DC voltage levels, and facilitating high-speed power reversal without interruptions. The two-stage DC-DC converter emerges as a key solution to address these challenges. By implementing the modular multilevel converter (MMC) structure, the converter's basic topology includes half-bridge sub-modules on the VSC side and full-bridge sub-modules on the LCC side. However, while this topology has been discussed in the literature, its connection to an LCC-based network with controlled current magnitude lacks detailed analysis regarding operational challenges, control strategies under various scenarios, and design considerations. This paper fills this gap by providing comprehensive mathematical analysis, design insights, and control strategies for the modular DC-DC converter to regulate DC voltage on the LCC-HVDC side. Additionally, the proposed control scheme minimizes the interfacing inductor between the two bridges, ensuring uninterrupted power flow during reversal and effective handling of DC faults. Validation through Control-Hardware-in-the-Loop testing across diverse operational and fault scenarios, along with a comparative analysis of different converters, further strengthens the findings.

1. Introduction

The rapid expansion of renewable energy resources has spurred significant investment in transmission infrastructure, primarily due to the remote locations of these renewable sources, often far from urban load centres [1]. In this context, direct current (DC) transmission has emerged as a preferable alternative to alternating current (AC) transmission due to its elimination of skin effect, high controllability, and lack of requirement for reactive power compensation, which traditionally limits the length of AC transmission lines. Voltage source converters (VSCs) have gained prominence as a mature technology for long-distance, high-power HVDC (High Voltage Direct Current) transmission, particularly with the advent of modular multilevel converters (MMCs) in recent years [2]. In VSC-based converters, power flow is managed by adjusting the direction and magnitude of transmitted current, while maintaining a constant DC voltage [2]. On the other hand, line-commutated converter (LCC) HVDC has a much longer and established commercial track record, with several projects worldwide continuing to run using this highly mature technology benefiting from using thyristor valves with their lower losses and higher ratings. DC current is regulated in LCC-based converters, while the DC voltage is varied in magnitude and polarity to control power flow.

The emergence of VSC HVDC technology has paved the way for the inevitable integration of hybrid grids, where both LCC and VSC technologies coexist. However, this integration presents numerous challenges, which can be effectively addressed through the use of DC-DC converters offering several benefits:

- Facilitating multi-vendor interoperability.

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- Providing zone and galvanic isolation between HVDC networks to prevent blackout propagation and enabling the connection between systems with differing grounding schemes.
- Enabling rapid power reversal without interruptions.
- Supporting high DC voltage stepping/matching ratios.
- Facilitating DC fault isolation.

DC-DC converter topologies are broadly categorized into isolated and non-isolated configurations [3,4], as summarized in Fig. 1. The isolated category encompasses three sub-categories. The first involves single-stage DC-DC converters, depicted in Fig. 2, characterized by the absence of an AC link and therefore lacking galvanic isolation. DC choppers are a prime example of such converters [5–7] where the concept of submodules (SMs) serves as the smallest building unit where inductive/capacitive energy storage elements are employed. However, due to hard switching, they exhibit an AC circulating component leading to increased conduction losses, rendering them unsuitable for HVDC applications due to their inability to block DC faults. The second sub-category comprises non-modular non-isolated converters, illustrated in Fig. 3. Resonant converters as in [8,9] are an excellent example of DC-DC converters without galvanic isolation. One of the resonant converters introduced in [10] is based on resonant balancing modules for multichannel LED drives. However, the resonant inductor is inversely proportional to the operating frequency of the converter. Therefore, it is not suitable for HVDC applications due to low operating frequency. Resonant DC-DC converters are further classified into two groups. The first one is the single tank [8], which utilizes different resonant tanks such as LC and LCL [11,12]. However, it suffers from low efficiency due to reactive power circulation and high stresses on the resonant tank as in [13–15]. On the other hand, the second group is based on multi-resonant tanks [16], which uses parallel connection of capacitors at the low voltage side and series connection at the high voltage side. However, multi-resonant tanks suffer from the same voltage and current stresses as in [17]. Additionally, the DC-DC auto-transformer, proposed in [18,19] consists of three VSCs mainly made of hybrid MMC interconnect VSC and LCC-based HVDC networks. Although this topology lacks interface inductance, it incurs large conduction losses due to the high number of submodules.

A two-stage modular multilevel DC-DC converter was proposed in [20], which consists of a half-bridge MMC followed by an H-bridge MMC. Despite the absence of interfacing AC inductance, this topology finds applicability in medium-voltage applications due to the contribution of the DC link capacitor to short-circuit current. Another alternative topology [21] substitutes the second stage MMC with a two-level converter to reduce the number of utilized semiconductors. However, the power capability of the converter is restricted to medium-power applications due to the presence of DC link capacitors and the lack of galvanic isolation. Additionally, a transformer-less DC MMC, was proposed in [22]. This converter primarily comprises arms and branches of FB-SMs. However, it requires bulky filters to eliminate the circulating AC component due to an imbalance between FB-SMs in the primary and secondary sides.

Regarding the second category, isolated converters are divided into two sub-categories, either modular or non-modular, as described in Fig. 4. The main advantage of the isolated converters is the presence of

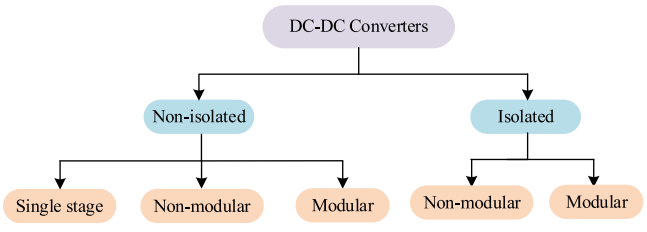

Fig. 1. DC-DC converters family tree.

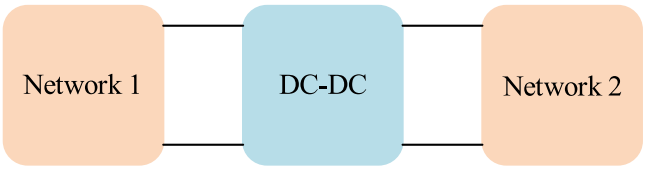

Fig. 2. Single-stage DC-DC converters block diagram.

an isolating transformer that allows for voltage stepping, galvanic isolation and DC fault isolation. The traditional two-level-DAB converter [23,24] is composed of two H-bridges with a series number of insulated gate bipolar transistors (IGBTs) in each arm. However, a large inductance is required at low frequency operation. Another modification for DAB has been presented in [25,26] to provide interconnection between VSC and LCC networks, where one H-bridge semiconductors are replaced by insulated gate commutated thyristors (IGCTs). The series connection is used to withstand high voltage but leads to high stresses on the isolating transformer. Moreover, the complexity of the snubber circuits to provide dynamic voltage sharing among the involved semiconductors is a major drawback. Additionally, these topologies suffer from large interfacing inductance due to operation at low frequency which is typical for HVDC. Also, there is the cascaded multilevel DAB, presented in [27,28], which is built using low power/voltage cascaded DAB converters. Each unit withstands a partial part of the applied DC voltage. These converters can be operated with soft switching, but they require high insulation, which limits their applications to medium voltage. The modular form of the DAB (named MMC-DAB) was presented in [29–31]. Each H-bridge is replaced by an MMC, where the stresses on the transformer are significantly reduced and the need for dynamic voltage-sharing snubber circuits is eliminated. Nevertheless, there is a tradeoff between the transformer size and losses in the converter depending on the operating frequency. Similarly, to conventional DAB, it suffers from large AC inductance. The DAB-MMC can be operated in two modes depending on the waveform at the AC link. The sinusoidal mode offers a low power density and uses higher capacitors in the sub-modules (SMs). On the other hand, the quasi-two-level (Q2L) mode yields a small loading time on the capacitors compared with the sinusoidal mode, therefore, the cell sizing is reduced [3,32]. Additionally, for the MMC-DAB to provide a connection between VSC and LCC networks while permitting power flow reversal without power interruption, one solution is to replace the voltage source-based MMC (VS-MMC) also known as the half-bridge MMC (HB-MMC), which is connected to the LCC network side by a current source-based MMC (CS-MMC) as proposed in [33]. However, the CS-MMC requires a very large SM inductor as the power increases. Another technique proposed in [34,35] known as the Active Forced-commutation (AFC) bridge, which utilizes thyristors for power transfer and the transitions are maintained by the FB chain link (FB-CL). However, it lacks the ability to use higher frequencies and the DC link capacitors lead to high transient DC fault current.

Another solution is to use a VSC-based converter with the capability to reverse DC link voltage polarity as in full-bridge SM-based MMC (FB-MMC) instead of the CS-MMC, as mentioned in [30,31]. However, in this case, all the analysis that has been done only assumes a DC voltage control-based LCC network. Therefore, there is no detailed analysis, design, or control have been provided in the literature for this converter in case of a connection to an LCC-based network with controlled DC current despite its simple basic topology and importance for the application of interfacing LCC and VSC HVDC networks. In this case, the DC-DC converter should build the DC voltage at the LCC side using the FB-MMC and hence control the power flow.

Therefore, this paper serves to provide this purpose for researchers and industry. Moreover, the performance of the system is studied under normal operation and different fault scenarios. Also, a comparison between different types of converters is presented. The main contributions

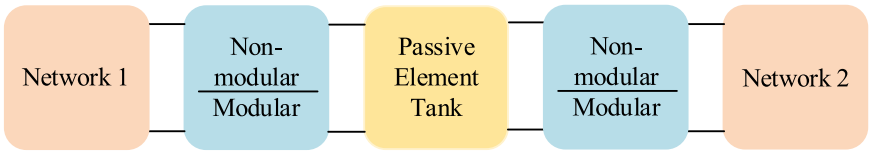

Fig. 3. Non-isolated non-modular/modular DC-DC converters block diagram.

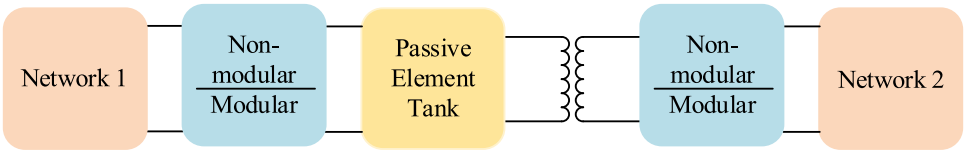

Fig. 4. Isolated non-modular/modular DC-DC converters block diagram.

of this paper can be summarized as follows:

- A new comprehensive mathematical analysis for capacitor sizing is provided for the full-bridge MMC-based DC-DC converter for ease of direct implementation in case connecting LCC-based HVDC network (with controlled DC link current) at the DC side of FB-MMC.
- Sizing of AC inductance independent of the amount of power flow.
- A new active power flow controller is proposed for the VSC-based DC-DC converter independent of the intermediate stage AC inductance value. This has the advantage of requiring only a small value of inductance which minimizes internal circulating/reactive power.
- Comparison between different converters that can be used in DC-DC converters in a front-to-front connection in HVDC applications.

This paper is organized as follows. Section 2 addresses the DC-DC converter structure with the main analysis required for both MMCs. Section 3 presents a detailed mathematical analysis of parameter design of the modular DC-DC converter. Section 4 provides equivalent power circuit analysis and active power control. Section 5 shows the results of the Control-Hardware-in-the-Loop (CHiL) test validation under healthy and fault scenarios. Section 6 discusses the comparison between different types of converters that can be used in DC-DC converters.

2. DC-DC converter topology analysis

The overall system of the DC-DC converter under study is shown in Fig. 5. It is mainly composed of two VSC converters for interconnection between LCC and VSC-based HVDC networks. However, the first one must be capable of reversing the DC-link voltage in order to reverse the power flow at the LCC side. The DC-DC converter employed for analysis is based on two H-bridge MMCs as shown in Fig. 6, where a FB-MMC is connected to an LCC-HVDC network and a HB-MMC connected to a VSC-HVDC network. The two MMCs are connected at their AC terminals via an isolating transformer, which provides voltage matching and galvanic isolation.

This paper considers a case with a DC current-controlled LCC network, where the DC-DC converter aims to build up the LCC network

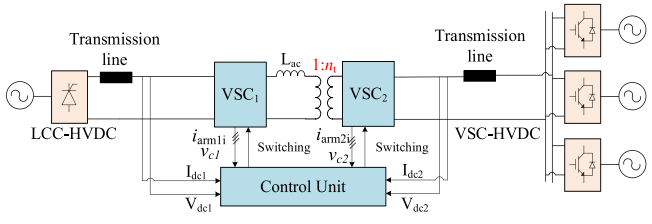

Fig. 5. Overall system diagram. including the DC-DC converter connected to the HVDC networks through transmission lines.

DC voltage magnitude and hence the power flow value. A single-phase configuration is employed in this paper for simplicity where the system can be expanded to a typical three-phase system. The AC inductance (leakage inductance of the transformer plus an auxiliary inductance) is used in this converter to limit the current stresses between both MMCs rather than controlling the power flow value. Because the control method used does not depend on the phase shift between both AC voltages. However, the control scheme aims to control the DC voltage at the LCC-based network. This is achieved by controlling the HB-MMC to determine the AC voltage at the AC link while the FB-MMC is used to control the DC voltage and hence controlling the power flow. Therefore, it can be deduced that the AC inductance has a negligible effect on the power flow, Further explanation on the power flow equations will be discussed in Section 4.1. In order to analyze the behaviour of both MMCs, a simplified model of equivalent arm variable capacitance is adopted as shown in [36], where all SMs per arm are replaced by an equivalent variable capacitor as shown in Fig. 7. The arm capacitance value depends on the number of connected SMs as in (1).

$$C_{ji} = \frac{C_{SM_j}}{n_{ji}} \tag{1}$$

where, C_{ji}, n_{ji} are the equivalent arm capacitance and the number of inserted SMs of the i^{th} arm in the j^{th} MMC, respectively, and C_{SMj} is the capacitance of each SM of the j^{th} MMC (j=1 for FB-MMC and j=2 for HB-MMC). The nominal voltage value across each capacitor in the SMs ($V_{C_{jnom}}$) is determined by (2).

$$V_{C_{j\,nom}} = \frac{V_{dc_{jrated}}}{N_j} \tag{2}$$

where, $V_{dcj_{rated}}$ is the rated DC voltage of the j^{th} MMC and N_j is the total number of SMs in each arm for the j^{th} MMC. To get the control equations of the j^{th} MMC, the arm inductances and resistances are neglected, then by applying KVL at loop 1 in Fig. 7, the DC voltage is defined as:

$$V_{dc_j} = v_{arm_{j2}} + v_{arm_{j1}} \tag{3}$$

where, v_{armj1} and v_{armj2} represent the instantaneous 1stand 2nd arm voltage in the j^{th} MMC. Then by applying KVL at loop 2, the instantaneous AC voltage of j^{th} MMC can be defined as:

$$v_{ac_j} = v_{arm_{j3}} - v_{arm_{j1}} \tag{4}$$

By solving (3) and (4), while taking into consideration that $v_{armj1} = v_{armj4}$ and$v_{armj2} = v_{armj3}$, the following is deduced:

$$v_{armj1} = \frac{V_{dc_j} - v_{ac_j}}{2} \tag{5}$$

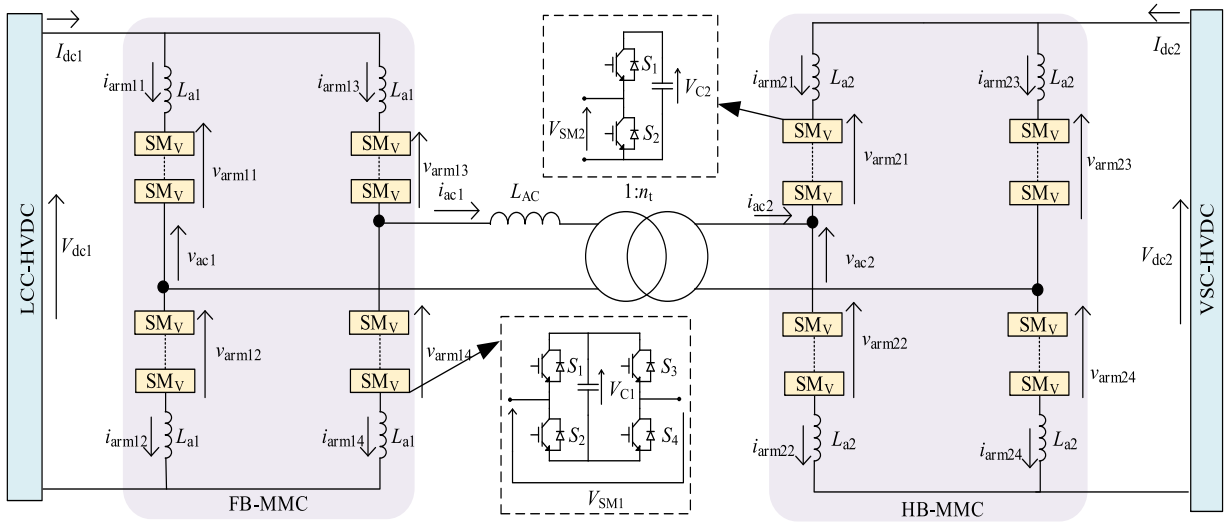

Fig. 6. The modular DC-DC converter for hybrid HVDC network connection.

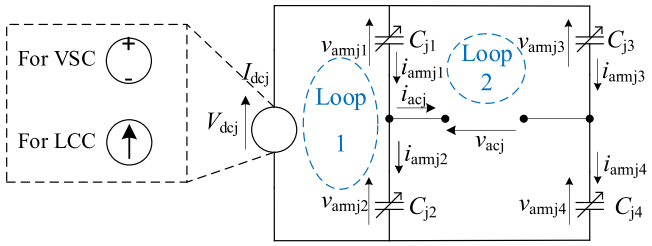

Fig. 7. MMC simplified circuit of equivalent arm capacitances.

$$v_{arm_{j2}} = \frac{V_{dc_j} + v_{ac_j}}{2} \tag{6}$$

Since the nominal SM capacitor voltage is calculated in (2), therefore, the nominal arm voltages can be represented as follows:

$$v_{arm_{ji_{nom}}} = n_{ji} \quad V_{C_{j_{nom}}} = n_{ji}\frac{V_{dc_{j_{rated}}}}{N_j} \tag{7}$$

By substituting (7) in (5) and (6), the number of SMs inserted in each arm can be calculated as in (8) and (9), assuming that the capacitor voltages are at kept at their nominal values.

$$n_{j1} = n_{j4} = \frac{N_j(V_{dc_j} - v_{ac_j})}{2V_{dc_{j_{rated}}}} = \frac{N_j(v^*_{dc_j} - v^*_{ac_j})}{2} \tag{8}$$

$$n_{j2} = n_{j3} = \frac{N_j(v^*_{dc_j} + v^*_{ac_j})}{2} \tag{9}$$

where, $v^*_{dc}j$ and $v^*_{ac}j$ are the per-unit reference values of the DC and AC voltages of j^{th} MMC respectively. A trapezoidal waveform is adopted [37] for the AC voltage of the MMCs, where both $v^*_{ac}j$ and $v^*_{dc}j$ are shown in Fig. 8 and can be represented by (10) and (11), respectively.

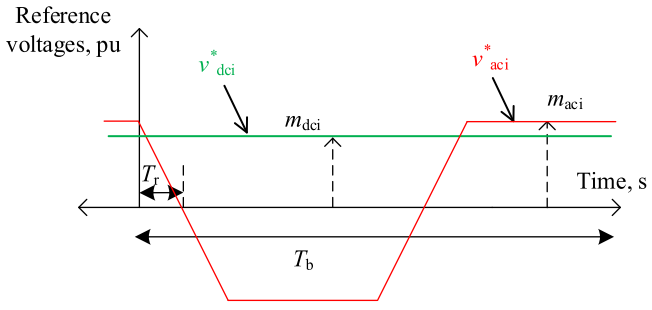

Fig. 8. The reference DC and AC normalized voltages of the MMC.

$$v^*_{ac}j = m_{ac_j}G$$

$$G = \begin{cases} 1 - \frac{t}{T_r}, \&0 < t < 2T_r \\ -1, \&2T_r < t < 0.5T_b \\ \frac{(t - 0.5T_b)}{T_r} - 1, \&0.5T_b < t < 0.5T_b + 2T_r \\ 1, \&0.5T_b + 2T_r < t < T_b \end{cases} \tag{10}$$

$$v^*_{dc_j} = m_{dc_j} \tag{11}$$

where, m_{dcj} is the ratio between the required DC voltage at DC side of j^{th} MMC and the rated DC voltage, while m_{acj} is the ratio between the peak of the AC voltage and rated DC voltage. T_b is the periodic time of the AC waveform and T_r is the rise time of the trapezoidal waveform as shown in Fig. 8.

It is worth noting that in case of VSC-based HVDC network, m_{dc2} is kept unity due to the fixed DC voltage. However, $m_{dc1} \in \{-1,1\}$ with respect to the power flow in LCC-based HVDC network. According to (8) and (9), it can be observed that the number of inserted SMs in each arm (n_{ji}) is a function of the reference waveform variables $v^*_{dc_j}$ and $v^*_{ac_j}$. Regarding the FB-MMC, n_{1i} can be positive or negative value, where positive value means that the inserted SM voltage is $+V_{C_{1i}}$ while the negative value means that the inserted SM voltage is $-V_{C_{1i}}$. Since the FB-MMC is connected to an LCC-based HVDC network, then both waveforms $v^*_{dc_1}$ and $v^*_{ac_1}$ range from −1–1 pu. By substituting in (8) and (9), n_{1i} ranges from $-N_1$ to N_1. On the other hand, regarding the HB-MMC, the value of $v^*_{dc}2$ is maintained at unity value and n_{2i} ranges from 0 to N_2 due to the unipolar nature of HB-SM.

3. Circuit parameters design

This section is divided into three subsections which provide detailed analysis and design of the AC link inductance and SM capacitor of the FB/HB-MMCs, respectively.

3.1. Calculation of the AC link inductance

To simplify the analysis, it is assumed that the HB-MMC can be replaced by an AC voltage source as depicted in Fig. 9. The AC

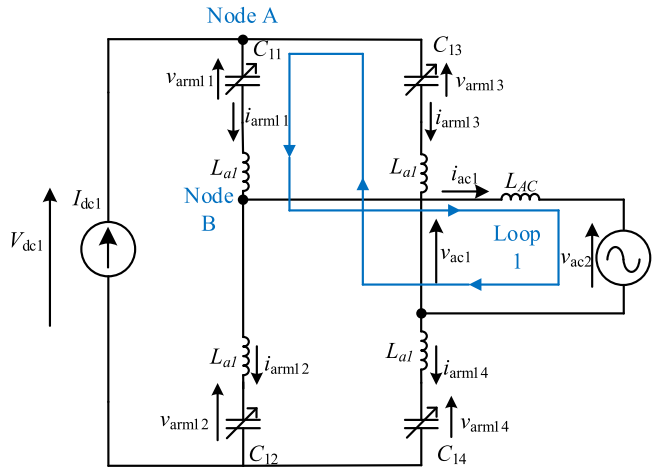

Fig. 9. Simplified model of the DC-DC converter assuming that the HB-MMC is a voltage source of AC trapezoidal waveform.

inductance is determined such that it achieves resonance with the SM capacitors on FB-MMC side at double the fundamental frequency in order to limit the current stresses at the AC link between both MMCs without absorbing much reactive power. The equivalent circuit of the FB-MMC side with the AC inductance is shown in Fig. 10, which is used in calculation of the equivalent impedance as in (12).

$$Z_{eq} = jX_{L_{AC}} + \frac{Z_u Z_l}{Z_u + Z_l} \tag{12}$$

where, Z_u and Z_l are upper and lower equivalent impedances and are given by (13) and (14), respectively.

$$Z_u = j2X_{L_{a1}} - jX_{C11} - jX_{C13} \tag{13}$$

$$Z_l = j2X_{L_{a1}} - jX_{C12} - jX_{C14} \tag{14}$$

Due to the symmetrical operation between arm 1 and arm 4, also between arm 2 and arm 3, then the following can be deduced,

$$X_{C11} = X_{C14} \& X_{C12} = X_{C13} \tag{15}$$

$$X_{C11} + X_{C13} = X_{C12} + X_{C14} = X_{Ceq} \tag{16}$$

Substituting by (1), then the equivalent capacitive reactance (X_{ceq}) can be calculated as (17).

$$X_{ceq} = \frac{1}{\omega C_{11}} + \frac{1}{\omega C_{13}} = \frac{n_{11}}{\omega C_{SM_1}} + \frac{n_{13}}{\omega C_{SM_1}} \tag{17}$$

Substituting by (8) and (9) in (17) and considering (11),

$$X_{ceq} = \frac{N_1 m_{dc1}}{\omega C_{SM_1}} \tag{18}$$

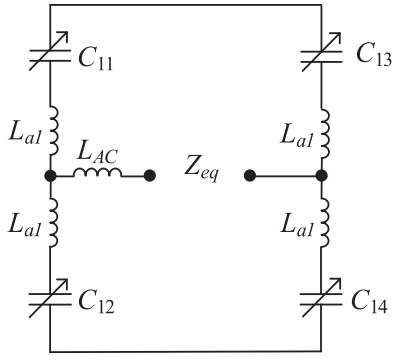

Fig. 10. The equivalent circuit of the FB-MMC side with the AC inductance.

Substituting by (18) in (13) and (14)

$$Z_u = Z_l = 2j\omega L_{a1} - j\frac{N_1 m_{dc1}}{\omega C_{SM_1}} \tag{19}$$

Then the equivalent impedance is given by;

$$Z_{eq} = j\omega L_{AC} + j\omega L_{a1} - j\frac{N_1 m_{dc1}}{2\omega C_{SM_1}} \tag{20}$$

It can be assumed that the arm inductance of the FB-MMC is neglected compared to the AC link inductance as the MMC arm inductance is very small due to the trapezoidal modulation as in [37]. At resonance, the equivalent impedance should be equal to zero, then the resonance frequency is obtained as in (21).

$$f_r = \frac{1}{2\pi}\sqrt{\frac{N_1 m_{dc1}}{2L_{AC}C_{SM_1}}} \tag{21}$$

The AC link inductance (L_{AC}) is designed to achieve a resonant frequency equal to double the fundamental frequency at $m_{dc1} = 1$ and is therefore calculated by the formula given in (22).

$$L_{AC} = \frac{N_1 T_b^2}{16 C_{SM\,1}\pi^2} \tag{22}$$

Additionally, Eq. (22) shows that the AC link inductance design is not based on power flow as the conventional DAB. Hence, the value is small in comparison with other DABs in literature. Additionally, it will only affect the voltage magnitude due to the proposed control.

3.2. SM capacitor design of the FB-MMC

In this subsection, it is required to design the suitable SM capacitance in the FB-MMC for a given voltage ripple. The FB-MMC in the DC-DC converter acts as a voltage rectifier, where the voltage on the DC side (V_{dc1}) depends on the voltage of the AC side (v_{ac1}). By applying KVL on loop 1 in Fig. 9 while neglecting the arm inductance,

$$v_{ac2} = v_{arm13} - v_{arm11} - L_{AC}\frac{di_{ac1}}{dt} \tag{23}$$

where, i_{ac1} is the instantaneous AC current of the FB-MMC. By applying KCL at node B in Fig. 9:

$$i_{ac1} = i_{arm11} - i_{arm12} \tag{24}$$

where, i_{arm1i} is instantaneous arm current of FB-MMC. Since, $v_{arm11} = v_{arm14}$ and $v_{arm12} = v_{arm13}$, thus $i_{arm11} = i_{arm14}$ and $i_{arm12} = i_{arm13}$. Substituting by (24) in (23) therefore;

$$v_{ac2} = v_{arm12} - v_{arm11} + L_{AC}\frac{d(i_{arm12} - i_{arm_{11}})}{dt} \tag{25}$$

To determine the suitable capacitance value of the SMs, the transients of the arm voltages must be taken into consideration. Therefore, v_{arm1i} can be divided into two terms: the nominal arm voltage ($v_{arm1i_{nom}}$) and the change in the arm voltage (Δv_{arm1i}) and according to (7), the AC voltage of the HB-MMC can be given as follows:

$$v_{ac2} = \Delta v_{arm12} + n_{12}\left(\frac{V_{dc\,rated_1}}{N_1}\right) - \Delta v_{arm11} - n_{11}\left(\frac{V_{dc\,rated_1}}{N_1}\right) + \frac{L_{AC}d}{dt}(i_{arm12} - i_{arm_{11}}) \tag{26}$$

To keep all the capacitor voltages of the FB-MMC at their nominal value and to decrease the current stresses between both MMCs, the AC modulation indices in both MMCs should be kept equal ($m_{ac1} = m_{ac2}$). Therefore, it can be assumed that the AC voltage of the HB-MMC is equal to the nominal AC voltage of the FB-MMC as in (27) assuming that the transients of the HB-MMC AC voltage are neglected for simplicity.

$$v_{ac_2} = v_{ac2_{nom}} = v_{ac\,1_{nom}} = (n_{12} - n_{11})\frac{V_{dc\,rated_1}}{N_1} \tag{27}$$

Therefore, by substituting with (27) in (26), the following equation is realized:

$$0 = \Delta v_{arm12} - \Delta v_{arm11} + L_{AC}\frac{d(i_{arm12} - i_{arm_{11}})}{dt} \tag{28}$$

Using the equivalent arm capacitance model, the change in the arm voltage of the FB-MMC (Δv_{arm1i}) can be calculated as a function of the arm current as follows:

$$\Delta v_{arm1i} = \frac{1}{C_{1i}}\int_{t_0}^{t} i_{arm_{1i}} \quad dt \tag{29}$$

Substituting (29) in (28), then

$$\frac{1}{C_{12}}\int_{t_0}^{t} i_{arm_{12}} \quad dt - \frac{1}{C_{11}}\int_{t_0}^{t} i_{arm_{11}} \quad dt + \frac{L_{AC}d}{dt}(i_{arm_{12}} - i_{arm_{11}}) = 0 \tag{30}$$

Applying KCL at node A

$$I_{dc1} = i_{arm_{11}} + i_{arm13} \tag{31}$$

Substituting (1) and (31) in (30), then the following is obtained:

$$\frac{n_{12}}{n_{11}+n_{12}}I_{dc1}\mathrm{t} - \int_{t_0}^{t} i_{arm_{11}} \quad dt = \left(\frac{2L_{AC}C_{SM_1}}{n_{11}+n_{12}}\right)\frac{d}{dt}(i_{arm_{11}}) \tag{32}$$

Substituting by (8) and (9) in (32);

$$\int_{t_0}^{t} i_{arm_{11}}dt + \left(\frac{2L_{AC}C_{SM_1}}{N_1 v_{dc1}}\right)\frac{d}{dt}(i_{arm_{11}}) = \frac{v^*_{dc}1 + v^*_{ac}1}{2v^*_{dc}1}I_{dc1}t \tag{33}$$

Applying derivative to (33) and substituting by the AC inductance in (22),

$$i_{arm_{11}} + \left(\frac{T_b^2}{16\pi^2}\right)\frac{d^2}{dt^2}(i_{arm_{11}}) = \frac{I_{dc1}}{2v^*_{dc}1}\left(v^*_{dc}1 + \frac{d}{dt}\left(v^*_{ac}1t\right)\right) \tag{34}$$

It is found that by assuming $m_{dc1} = m_{ac1} = m$ in (8) and (9), the number of inserted SMs in each arm is zero in both the flat (2nd or 4th) periods of the trapezoidal waveform, thus minimizing the loading on the capacitors, which results in minimizing the required capacitance in the FB-MMC. Also, for simplicity T_r is assumed to be fixed at $0.1T_b$. Substituting by (10) and (11) in the 2nd order differential Eq. (34), the resultant 2nd order differential equations of the arm currents are solved for each of the four periods, and the arm currents are given by (35).The SM capacitor voltage in the first arm can be deduced for each of the four periods as mentioned in (36).

$i_{arm11} =$

$$\begin{cases} I_{dc_1}\left(1 - 0.64\cos\left(\frac{12.57t}{T_b}\right) + 0.37\sin\left(\frac{12.57t}{T_b}\right) - \frac{10t}{T_b}\right), \&0 < \mathrm{t} < 2T_r \\ I_{dc_1}\left(-0.27\cos\left(\frac{12.57(t-2T_r)}{T_b}\right) - 0.72\sin\left(\frac{12.57(t-2T_r)}{T_b}\right)\right), \&2T_r < \mathrm{t} < 0.5T_b \\ I_{dc_1}\left(0.64\cos\left(\frac{12.57(t-0.5T_b)}{T_b}\right) - 0.37\sin\left(\frac{12.57(t-0.5T_b)}{T_b}\right) + \frac{10(t-0.5T_b)}{T_b}\right), \&0.5T_b < t < 0.5T_b + 2T_r \\ I_{dc_1}\left(1 + 0.27\cos\left(\frac{12.57(t-0.5T_b-2T_r)}{T_b}\right) + 0.72\sin\left(\frac{12.57(t-0.5T_b-2T_r)}{T_b}\right)\right), \&0.5T_b + 2T_r < \mathrm{t} < T_b \end{cases} \tag{35}$$

The instantaneous capacitor voltage can be determined by substituting (35) into (36) and is illustrated in Fig. 11, where the peak-to-peak ripple voltage is approximately determined by calculating the change in the capacitor voltage from the beginning of the 2nd period until the minimum voltage point of 2nd period. This condition is correct as long as the AC inductance achieves resonant frequency at double the fundamental frequency as mentioned earlier. Therefore, the ripple voltage can be calculated approximately as in (37).

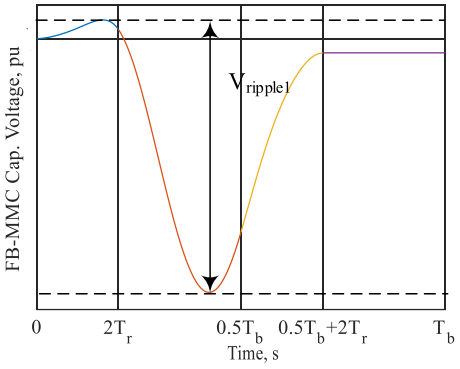

Fig. 11. The FB-MMC SM capacitor voltage ripple waveform.

Table 1
Design equations constants.

T_r	k_1	k_2	k_3
0.025 T_b	0.085	0.1258	0.1253
0.05 T_b	0.096	0.1309	0.1272
0.075 T_b	0.11	0.1424	0.1308
0.1 T_b	0.1225	0.1589	0.1343

$$v_{C_1} = \frac{1}{C_{SM1}}\int_0^t i_{arm_{11}}\left(\frac{n_{11}}{N_1}\right) \quad dt + H \tag{36}$$

where, v_{C1} is the individual capacitor voltage in FB-MMC and H is the integration's constant.

$$V_{ripple_1} = \frac{k_1 T_b I_{dc1} m}{C_{SM1}} \tag{37}$$

where, k_1 is a constant dependent on the rise time value.

Table 1 shows different values for k_1 numerically evaluated based on different rise time values. It can be observed from (37) that the voltage ripples decrease with decreasing the modulation index below unity. Since the voltage ripple percentage is calculated as follows:

$$\%V_{ripple_1} = \frac{V_{ripple}}{V_{dc\,rated\,1}/N_1} \tag{38}$$

then, the capacitor design formula can be calculated by (39)

$$C_{SM1} = \frac{k_1 T_b I_{dc1} m N_1}{\%V_{ripple_1} V_{dc\,rated\,1}} \tag{39}$$

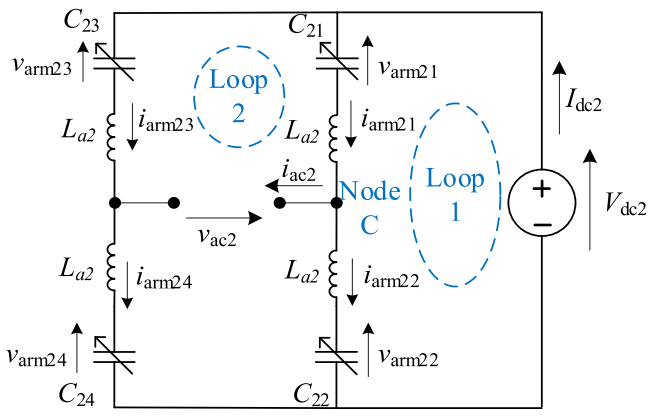

Fig. 12. The HB-MMC simplified model with equivalent arm capacitance.

3.3. SM capacitor design of the HB-MMC

The change in the SM capacitor voltages of the HB-MMC is calculated as in (40)

$$\Delta v_{C2} = \frac{1}{C_{SM_2}} \int_{t_0}^{t} i_{arm_{21}} \left(\frac{n_{21}}{N_2}\right) \quad dt \tag{40}$$

where Δv_{c2} is the voltage ripple across capacitor in HB-SM.

$$i_{ac_2} = i_{arm21} - i_{arm22} \tag{41}$$

By applying KCL on node C in Fig. 12, the AC current of the HB-MMC is deduced.

Using (4) and (41) while neglecting the arm inductance, the arm currents are defined as a function of the arm voltages and can be calculated as $\left(i_{arm2i} = C_{2i}\frac{dV_{arm2i}}{dt}\right)$. The AC current i_{ac_2} is split among the HB-MMC arms depending on the equivalent capacitance of each arm as in (42) and (43).

$$i_{arm_{21}} = i_{arm24} = i_{ac2}\frac{C_{21}}{C_{21}+C_{22}} = i_{ac_2}\frac{1+v_{ac}^{*}2}{2} \tag{42}$$

$$i_{arm_{22}} = i_{arm23} = -i_{ac_2}\frac{C_{22}}{C_{21}+C_{22}} = -i_{ac_2}\frac{1-v_{ac}^{*}2}{2} \tag{43}$$

By substituting (42) in (40), then the capacitor voltage waveform is calculated and can be shown as in Fig. 13, where the peak-to-peak capacitor voltage ripple can be calculated based on (44).

By further simplifications, the voltage ripple of the HB-MMC SM capacitors (V_{ripple_2}) is calculated as follows:

$$V_{ripple_2} = \frac{T_b I_{dc_1}(\quad k_2 - k_3 m^2)}{C_{SM_2} n_t} \tag{45}$$

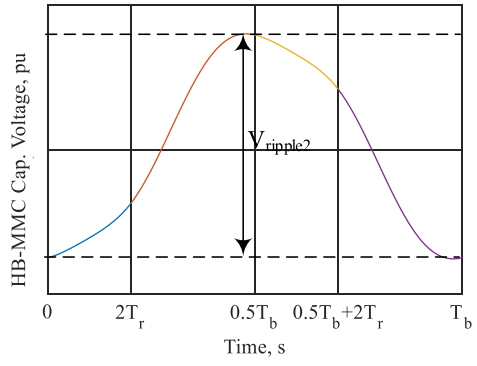

Fig. 13. The HB-MMC SM capacitor voltage ripple waveform.

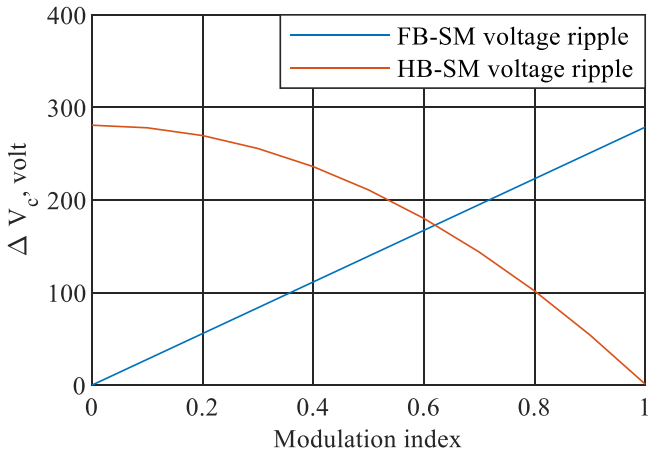

Fig. 14. Relation between voltage ripple of each sub-module and modulation index.

Table 2
Numeric example parameters.

Symbol	*Quantity*	Value
f	Fundamental frequency	200 Hz
I_{dc1}	DC link current	$4kA$
N_1	Number of FB-SMs	16
C_{sm1}	FB-SM capacitance	$0.56mF$
N_2	Number of HB-SMs	16
C_{sm2}	HB-SM capacitance	$0.56mF$

where, k_2 and k_3 are constants dependent on the rise time (T_r) and listed in Table. It is obvious from (45) that the voltage ripple of the HB-MMC SMs increases with decreasing the modulation index m.

Finally, the HB-MMC SM capacitor design formula is designed based on the worst case, where m equals to zero as given by (46) and $\%V_{ripple_2}$ is the percentage voltage ripple of the HB-MMC SM capacitors,

$$C_{SM2} = \frac{N_2 T_b I_{dc_1} k_2}{\%V_{ripple_2} V_{dc2} n_t} \tag{46}$$

$$\%V_{ripple_2} = \frac{V_{ripple_2}}{V_{dc2}/N_2} \tag{47}$$

By observing (37) and (45), it can be observed that the voltage ripple of the capacitor in FB-SM is directly proportional with modulation index. Therefore, the voltage ripple increases as the power flow achieves the rated value.

On other hand, it can be noted that the voltage ripple of the capacitor in HB-SM is inversely proportional with square of modulation index. Hence, the voltage ripple decreases as the power flow achieves rated value. A numerical example is shown in Fig. 14 based on the following parameters listed in Table 2.

4. Converter power analysis and control

In this section, the converter power equations and control structure for normal operation are discussed.

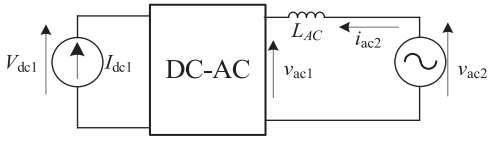

Fig. 15. Power flow equivalent circuit diagram.

4.1. Power equations

To extract the power equation, the LCC-based HVDC network is assumed as a constant DC current source while the HB-MMC at the VSC-based HVDC network is replaced by a controlled AC voltage source interfaced through a DC-AC conversion stage as depicted in Fig. 15. All arm inductances as well as AC link inductance have little or no effect on the active power flow (as explained in Section 2) and can be neglected in deducing the power equation. The active power at DC side of the equivalent circuit can be computed from the following, assuming a lossless converter:

$$P_1 = V_{dc1} I_{dc1_{rated}} = -P_2 \tag{48}$$

Hence, the value of the V_{dc1} determines the power transferred between the two DC networks. By substituting (7) in (4) at $j = 2$, the nominal AC voltage of HB-MMC as a function of VSC-based HVDC network DC link voltage can be given by (49),

$$v_{ac_2 nom} = \frac{n_{22} - n_{21}}{N_2} V_{dc_{2_{rated}}} \tag{49}$$

Also, by substituting (7) in (4) at $j = 1$ and taking into consideration that $V_{dc1} = m_{dc_1} V_{dc_{1_{rated}}}$, then the LCC-based HVDC network's DC link voltage as a function of nominal AC voltage of FB-MMC is given by;

$$v_{ac1 nom} = (n_{12} - n_{11}) \frac{V_{dc1}}{m_{dc1} N_1} \tag{50}$$

Since the AC modulation indices in both MMCs are kept equal ($m_{ac1} = m_{ac2}$) to minimize the current stresses between both MMCs, as mentioned in Section 3, and due to the design condition of the AC inductance which cancels ripples and transients of capacitors voltages in FB-SM.

It is safe to assume that $v_{ac_1 nom} = v_{ac_2 nom}$, therefore, the rated value of DC link voltage at LCC-based HVDC network side can be depicted by equating (50) and (49):

$$V_{dc_1} = m_{dc1} \frac{N_1}{N_2} \frac{n_{22} - n_{21}}{n_{12} - n_{11}} V_{dc_{2_{rated}}} \tag{51}$$

Hence, by substituting (51) in (48) and using (8) and (9) for $j = 1$ and $j = 2$, respectively, the general active power formula is given by:

$$P_1 = \frac{m_{dc1} m_{ac2}}{m_{ac1}} V_{dc_{2_{rated}}} I_{dc1_{rated}} \tag{52}$$

Since $m_{ac1} = m_{ac2}$ the final power flow equation can be summarized as follows:

$$P_1 = m_{dc1} V_{dc_{2_{rated}}} I_{dc1_{rated}} \tag{53}$$

Also, it can be deduced from Section 3 that $m_{dc1} = m_{ac1} = m_{ac2} = m$, then, the power equation can be generalized as follows:

$$P_1 = -P_2 = m V_{dc_{2_{rated}}} I_{dc1_{rated}} \tag{54}$$

4.2. Power flow control

According to (53), the power flow to/from the LCC-based HVDC network depends entirely on the DC modulation index of the FB-MMC (m_{dc1}) which is designated as a generic control variable m. The control block diagram of the DC-DC converter is shown in Fig. 16. The active power error is fed to PI controller, which generates the modulation index (m). Then the modulation index (m) is routed to waveform generator to adjust the DC reference ($v^*_{dc}1$) and AC references ($v^*_{ac}1$and $v^*_{ac}2$) of both MMCs. The AC reference ($v^*_{ac}2$) of HB-MMC is used to generate the required number of SMs to be inserted (n_{2i}), which is fed to a balancing algorithm to generate the required switching sequence. On the other hand, the AC and DC references ($v^*_{ac}1$and $v^*_{dc}1$) of FB-MMC are used to generate the required number of SMs to be inserted (n_{1i}), which is fed to a balancing algorithm to generate the necessary switching sequence. A conventional balancing algorithm is used for the HB-MMC as described in [38], while a balancing algorithm is applied to the FB-SMs capacitors as mentioned in [39].

5. Experimental validation using CHiL testing platform

This section is divided into three subsections to validate the DC-DC converter in three different cases. Each subsection validates the capability of the DC-DC converter under study to overcome the aforementioned challenges during operation. The different cases employed in experimental validation are listed below:

- Power flow under normal operation (rated, partial and reversal).
- DC pole-to-pole fault at VSC-based network DC side.
- DC pole-to-pole fault at LCC-based network DC side.

Mainly, the DC-DC converter is built and validated based on the CHiL setup shown in Fig. 17. The CHiL system is composed of two parts. The first part is the DC-DC converter established on the OPAL-RT real-time

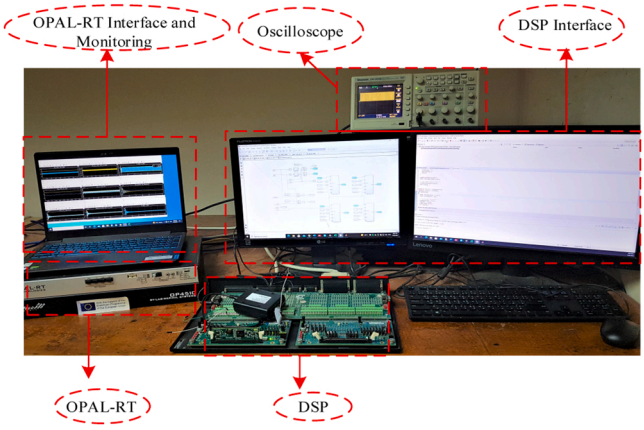

Fig. 17. Control-Hardware-in-the-Loop platform.

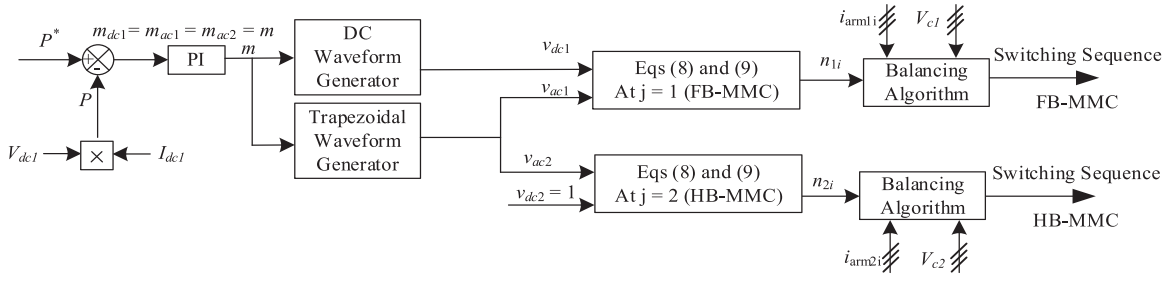

Fig. 16. Control block diagram of the DC-DC converter.

Table 3
CHiL system parameters.

Symbol	Quantity	Value
OPAL-RT	Number of cores	4
	RAM	2×8 GB
	Processor	Intel core Xeon
DSP	TMS320F28335ZJZA	150 MHz
P_r	Rated power	500 MW
I_{dc1}	LCC-based HVDC DC link current	4000 A
V_{dc2}	VSC-based HVDC DC link voltage	500 kV
f	Fundamental Frequency	100 Hz
$1/n_t$	Transformer turns ratio	¼
L_{AC}	The transformer leakage inductance	840 μH
T_r	Trapezoidal waveform rise time	1 ms
N_1	Number of SMs per arm in FB-MMC	16
N_2	Number of SMs per arm in HB-MMC	16
C_{SM1}	Capacitance of FB-SM	6.1 mF
C_{SM2}	Capacitance of HB-SM	510 μF
L_{a1}	Arm inductance of FB-MMC	10 μH
L_{a2}	Arm inductance of HB-MMC	10 μH
L_1	DC limiting inductor at FB-MMC	80 mH
L_2	DC limiting inductor at HB-MMC	50 mH
C_1	DC filter capacitor at FB-MMC	65 μF
C_2	DC filter capacitor at HB-MMC	0.1 μF
$l_{transmission}$	line inductance per meter	1.2mH/km
$r_{transmission}$	line resistance per meter	33mΩ/km
Line	Transmission line length	600 km

platform. The second part is the hardware DSP (Digital Signal Processor) control board, where the controller unit is established to perform the required actions to reach the desired outcome/reference. The OPAL-RT platform has 4 cores based on Intel Core Xeon processor at 3 GHz and RAM 2 ×8 GB. The communication port is based on Gigabit Ethernet LAN. Additionally, the controller is a 150 MHz DSP labelled as TMS320F28335ZJZA.

The overall system is depicted in Fig. 5, where the LCC-HVDC network is connected to the FB-MMC through a transmission line of 600 km while the VSC-HVDC network is connected to the HB-MMC through a transmission line of 600 km as well. The system parameters are given in Table 3. The FB-MMC SM capacitor selection is based on (39), where the capacitor is chosen to achieve 10% ripple voltage at the unity modulation index, which represents the highest ripple condition. On the other hand, the HB-MMC SM capacitor selection is based on the formula presented in (46) at a ripple voltage percentage equal to 10% at the lowest modulation index that corresponds to the highest ripple case. Additionally, the AC inductance is calculated based on (22).

5.1. Power flow control under normal operation

This subsection validates the capability of the DC-DC converter to provide uninterruptible power flow during reversal and partial power flow cases. The power flow is assumed to be from port 1 to port 2. Whereas the control of the DC-DC converter is based on the reference AC and DC voltages assuming $m_{ac1} = m_{dc1} = m_{ac2} = m$ as mentioned earlier. The utilized control block diagram is depicted in Fig. 16, where the main control variable for active power control is the modulation index (m) as in (54). The control range of modulation index (m) is from −1–1, where positive values indicate power flow from LCC to VSC HVDC network and negative values indicate power flow in the opposite direction. Fig. 18(a) and Fig. 18(b) show the active and reactive power at the FB-MMC and HB-MMC sides, respectively, where the active power is reversed successfully without power interruption. On top of that, the reactive power is at low value due to the design criteria of the AC inductance. It can be observed that as the active power flow decreases, the reactive power decreases corresponding to the reduction of current flow. Moreover, Fig. 18(c) and Fig. 18(d) show the DC link voltage and current of FB/HB-MMCs, respectively, where the DC voltage at FB-MMC terminals and DC current at HB-MMC terminals are changing polarity according to the power flow magnitude and direction. It can be observed that the DC current at FB-MMC is fixed due to the nature of LCC HVDC and by duality the same applied for the DC voltage at HB-MMC. Fig. 18 (e) and Fig. 18(f) depict the AC voltage of both MMCs and AC current during rated and partial power flow, respectively. It is worth noting that both AC voltages are in phase due to the control used but with a small difference in magnitude. Additionally, Fig. 19(a) and Fig. 19(b) show the FB-SM capacitor voltages in per-unit during rated and partial power flow, respectively. It can be observed that the capacitor voltage ripple decreases as the active power deviates from the rated value (unity modulation index) as explained in Section 3. On the other hand, Fig. 19 (c) and Fig. 19(d) show the HB-SM capacitor voltages in per-unit at rated and partial power flow, respectively, where the capacitor voltage ripple increases as the active power flow deviates from the rated power (unity modulation index) which has also been addressed in Section 3. It can be noted that the waveform of voltage ripple in FB-SMs is completely different from the voltage ripple in HB-SM due to the different types of

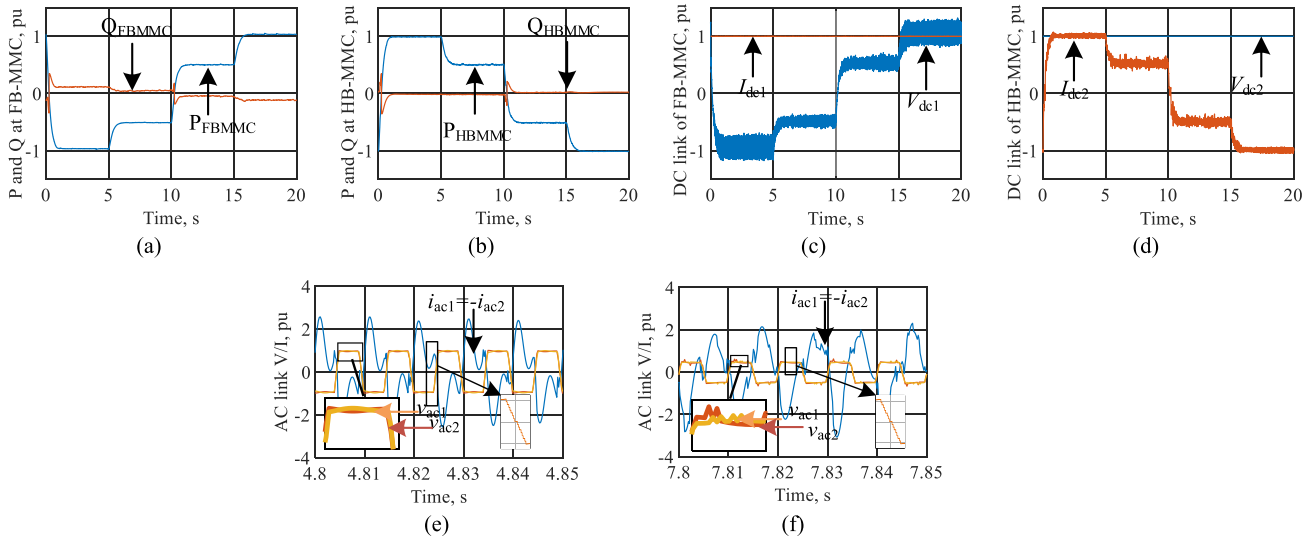

Fig. 18. Performance of the DC-DC converter: (a) active and reactive power at FB-MMC side, (b) active and reactive power flow at HB-MMC side, (c) DC link voltage and current at FB-MMC, (d) DC link voltage and current at HB-MMC, (e) FB-MMC AC voltage and current at P_{rated}, and (f) FB-MMC AC voltage and current at 0.5 P_{rated}.

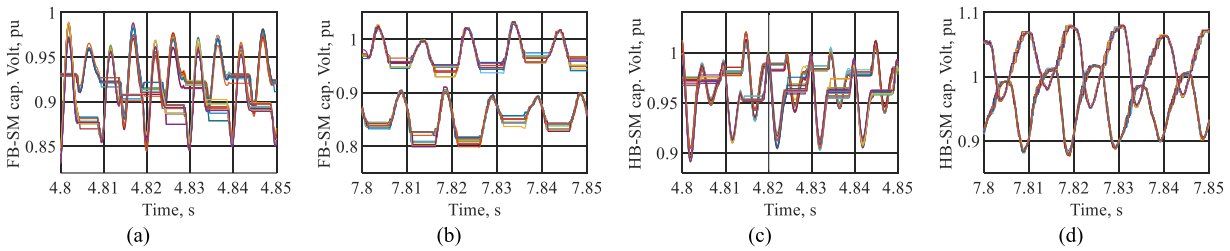

Fig. 19. (a) FB-SMs capacitors voltages at P_{rated}, (b) FB-SMs capacitors voltages at 0.5 P_{rated}, (c) HB-SMs capacitors voltages at P_{rated} and (d) HB-SMs capacitors voltages at 0.5 P_{rated}.

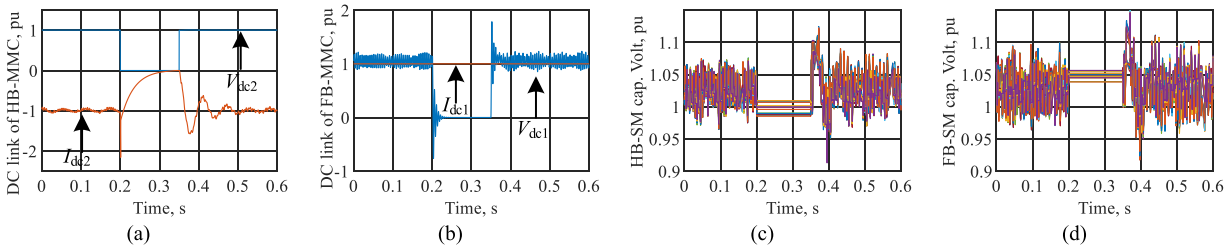

Fig. 20. Performance of the studied DC-DC converter under DC pole-to-pole fault at HB-MMC, (a) DC link voltage and current at HB-MMC, (b) DC link voltage and current at FB-MMC, (c) HB-SMs capacitor voltages and (d) FB-SMs capacitor voltages.

the connected HVDC ports, where port 1 is connected to the LCC HVDC network while port 2 is connected to the VSC HVDC network.

5.2. DC pole-to-pole fault at HB-MMC

This subsection illustrates the performance of the DC-DC converter during the DC pole-to-pole fault at the midpoint of the transmission line at the HB-MMC DC side. The power flow is assumed to be from port 1 to port 2. The criteria at which the fault is detected is based on an increase in DC link current above 1.2 pu and the reduction of DC link voltage below 0.7 pu. At the instant of fault detection, the controller action is to block the HB-MMC, where all the switches' gating signals are inhibited, while the FB-MMC SMs are bypassed. The fault is assumed to start at t = 0.2 s and is cleared at t = 0.35 s, where it is assumed to be temporary persisting for t = 150 ms. The fault detection is assumed to act after 1 ms of fault occurrence. Fig. 20(a) and Fig. 20(b) show the DC link voltage and current of the HB and FB-MMCs, respectively. At the instant of the fault, the DC voltage of HB-MMC collapses to zero and the DC current increases due to HB-SM capacitors discharging in fault. On the other hand, the DC current at FB-MMC side is maintained constant due to the nature of LCC HVDC but the voltage collapses to zero. Furthermore, after the fault detection, both HB and FB-MMCs are blocked and the fault current decreases to zero, thus achieving fault blocking. Moreover, Fig. 20(c) and Fig. 20(d) show HB and FB-SM capacitor voltages, respectively, where at the instant of the fault before fault detection, the HB-SMs capacitors discharge marginally until fault detection, the capacitor voltages are maintained constant due to blocking of both MMCs. Normal operation is restored after fault clearance.

5.3. DC pole-to-pole Fault at FB-MMC

This subsection illustrates the performance of the DC-DC converter during a DC pole-to-pole fault in the transmission line midpoint at the FB-MMC DC side. The power flow is assumed to be from the VSC to the LCC HVDC. A temporary fault is assumed, which starts at t = 0.2 s and ends at t = 0.35 s, where it persists for 150 ms. The fault detection is based on an increase of DC link current above 1.2 pu and a reduction of DC link voltage under 0.7 pu. At the instant of fault detection, the control unit nullifies the DC modulation index of the FB-MMC (m_{dc1} = 0) without blocking both sides' SMs. The DC link voltage and current at HB and FB-MMCs are shown in Fig. 21(a) and Fig. 21(b), respectively. It can be observed that the DC current at the HB-MMC side collapses to zero at the instant of fault occurrence and voltage is maintained constant due to the nature of VSC HVDC. On the other hand, the DC current of the FB-MMC increases slightly due to the discharge of FB-SMs in the fault before fault detection. After the fault detection, the fault current is decreased to zero, while after fault clearance, normal operation is restored. Moreover, the HB and FB-SMs capacitor voltages are depicted in Fig. 21(c) and Fig. 21(d), respectively, where both SM capacitors exhibit transient ripple at fault occurrence as well as fault clearance.

6. Discussion

This section presents a comparison between different DC-DC

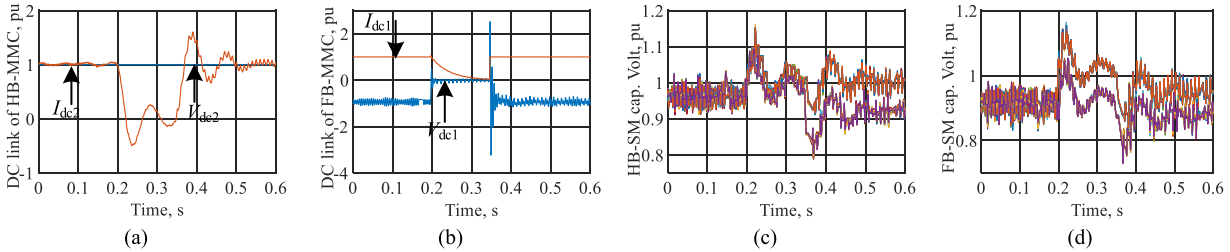

Fig. 21. Performance of the studied DC-DC converter under DC pole-to-pole fault at the DC side of FB-MMC with applying the first fault handling technique, (a), and (b) DC link voltage and current at HB/FB-MMC, respectively, (c), and (d) HB/FB-SMs capacitor voltages, respectively.

Table 4
Key feature comparison of different converters.

Converter Type	Line Commutated DC-DC converter [26]	Modified Universal DC-DC converter [25]	Hybrid-based MMC DC-DC converter [33]	AFC-based DC-DC converter [34,35]	FB-MMC-based DC-DC converter under study
Energy-storing element	None	None	L and C	C	C
DC voltage polarity reversal	Positive	Bipolar	Bipolar	Bipolar	Bipolar
Control scheme in connecting VSC/LCC networks	AC phase shift control	AC phase shift control	AC phase shift control	AC phase shift control	DC voltage control
AC filter complexity in DC-DC converter VSC/LCC networks	LC	CLC	LC	L	L
Reactive power	$Q\alpha\sin(\delta)$	$Q\alpha\cos(\delta)$	$Q\alpha\sin(\delta)$	$Q\alpha\cos(\delta)$	$Q\alpha m^2$
Power flow dependency on AC inductance	Yes	Yes	Yes	Yes	No
Dependency of controller on bridge topology	Yes	Yes	Yes	Yes	No
Control range	$\{-\delta,\delta\}$	$\{-\delta,\delta\}$	$\{-\delta,\delta\}$	$\{-90^\circ,90^\circ\}$	$\{-1,1\}$
AC filter inductance in connecting VSC/LCC networks $I_{dc1}=4kA, V_{dc2}=500kV, P=400MW$ *and* $f=100Hz$	$26.5L_{FB-MMC}$	$17.4L_{FB-MMC}$	$26.5L_{FB-MMC}$	$152.3L_{FB-MMC}$	$L_{FB-MMC}=1.3mH$
No of SWs per arm	N	2 N	4 N	2 N	4 N
Frequency range operation	Wide	Wide	Wide	Narrow (near 50/60 Hz)	Wide
Chain-link SWs	None	None	None	12 N	None
Type of SWs used	IGBT and IGCT	IGBT	IGBT and IGCT	IGBT and Thyristors	IGBT
No of limb inductors	None	None	4	1	4
No of limb capacitors	None	None	4	None	None
DC link capacitor	None	None	None	Yes	None
DC-fault tolerance capability	No	No	Yes	Yes	Yes
Dynamic voltage sharing snubber circuit	Yes	Yes	Yes	No	No
Voltage/current stress at the AC link	Yes	Yes	No	No	No

converters that can be used in the interconnection of LCC and VSC-based HVDC applications including hybrid based 2-level DC-DC converter mentioned in [26], hybrid-based MMC DC-DC converter mentioned in [33], AFC-based DC-DC converter mentioned in [34] and the FB-MMC under study in this manuscript. The comparison in Table 4 shows the type of energy-storing element in SMs, the ability to provide hybrid connection, the number of switches used per arm, DC fault tolerance, and the need for dynamic voltage-sharing snubber circuits. The FB-MMC, AFC and CS-MMC can provide bipolar DC voltage. However, only the AFC and FB-MMC can be connected to HVDC grid types (VSC/LCC). Since the AFC utilizes thyristors, it is limited to very low frequency operation, unlike the FB-MMC which can operate under a relatively wider frequency range. The control scheme of the CS-MMC and AFC DC-DC converters is based on the phase shift between the AC waveforms. However, the control scheme in the studied DC-DC converter is based on controlling the DC voltage at the LCC port side. Therefore, the needed AC link inductance is very low compared to that of the CS-MMC and AFC topologies.

Therefore, it is observed that the FB-MMC prevails in HVDC applications despite the large number of semiconductors used as it provides a hybrid connection, fault-tolerant due to the negative polarity of FB-SMs. Additionally, it does not suffer from the problem of dynamic voltage sharing. Also, it achieves low voltage stresses across the transformer.

7. Conclusion

This paper has provided a new parameter design and control technique in hybrid interconnection between a DC current-controlled LCC-based network and a VSC-based network. A DC-DC converter has been utilized comprising an HB-MMC at the VSC network side and an FB-MMC at the LCC side. The analysis and equivalent power circuit model have succeeded in reducing the interfacing AC inductance as the power flow is independent of AC filter inductance. As indicated in the comparison, the AC inductance of the other converters is greater than the AC inductance of FB-MMC based DC-DC converter, where the AC inductance is reduced by a factor ($6x10^{-3}$). Furthermore, the CHiL validation of the proposed control of the DC-DC converter shows that any VSC converter with the capability to reverse DC link voltage can be used in interconnection with LCC-based HVDC. Additionally, it depicts a limited reactive power due to the low interfacing AC inductance. Also, the DC-DC converter under study has shown superior performance under different cases of healthy and unhealthy power flow.

Also, a comparison between different converters has been discussed, which concludes that the FB-MMC is superior in the interconnection between VSC and LCC HVDC networks. The usage of FB-MMC solves the high insulation inductor SM in CS-MMC. Also, it evades the utilization of thyristors, which limits the frequency operation near 50/60 Hz, as in AFC. In addition to that, the absence of DC link capacitors limits the DC fault transient current in comparison with AFC.

CRediT authorship contribution statement

Yousef N. Abdelaziz: Investigation, Methodology, Software, Validation, Writing – original draft, Writing – review & editing, Formal analysis. **Y. Al-Turki:** Funding acquisition, Project administration. **Ayman Abdel-Khalik:** Supervision, Writing – review & editing. **Khaled H. Ahmed:** Conceptualization, Supervision, Writing – review & editing. **Fahd Alsokhiry:** Funding acquisition, Project administration. **Ahmed A. Aboushady:** Supervision, Writing – review & editing. **Mohamed Mansour:** Formal analysis, Investigation, Methodology, Software, Validation, Writing – original draft, Writing – review & editing.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper

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