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Review

A Comparative Review of Three Different Power Inverters for DC–AC Applications

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Abstract: This paper presents a comparative review of three different widely used power inverters, namely the conventional six-switch inverter; the reduced switch count four-switch inverter; and the eight-switch inverter. The later inverter can be reconfigured as a neutral-point diode-clamped inverter at the failure of one inverter leg. The three power inverters are compared and discussed with respect to cost, complexity, losses, common mode voltage, and control techniques. The paper is intended to serve as a guide regarding selecting the appropriate inverter for each specific application. Simulation results are presented to demonstrate the performance of the three power inverters, followed by a comprehensive comparison between the three power inverters.

Keywords: common mode voltage; DC–AC power inverters; neutral-point diode-clamped inverter; reduced-switch-count inverter; space vector modulation

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1. Introduction

A DC–AC power inverter is a key component in the electrical power system. Adjustable speed drives [1], uninterruptible power supplies [2], active power filtering [3], electric vehicles [4], and the integration of renewable energy generation in power systems [5] are some areas where DC–AC inverters are deployed.

Conventionally, the six-switch (B6) inverter is utilized [6–12]. However, interest has increased in utilizing inverters with higher efficiency, better performance, and lower costs. In so doing, a four-switch (B4) inverter was proposed by Broeck and Wyk in 1984 [13], where one inverter leg is replaced by two DC link series tapped capacitors, hence reducing the power switches from six to four.

B4 inverters have been deployed in a wide range of applications, including three-phase [14,15] and two-phase [16] induction motor drives, brushless DC [17] and AC [18] motor drives, permanent magnet synchronous motor drives [19,20], synchronous reluctance motor drives [21], doubly fed induction generators [22], shunt active power filters [23], and grid-connected applications [24].

Reducing the number of power switches results in a more robust and reliable inverter with a low computational burden on the controller side. In addition, the number of gate drives along with interfacing circuitry is reduced [25]. It is claimed that reducing the number of switching devices from six to four reduces the cost of the converter along with decreasing the switching and conduction losses, thereby increasing inverter efficiency [26].

Since one inverter leg is removed, one phase must be connected to the center point of the two DC side series capacitors. This connection results in capacitor voltage imbalance, requiring high DC capacitance—leading to increased inverter costs and the utilization of undesirable (low-reliability) electrolytic capacitors [27].

However, DC link voltage utilization is reduced to 50% even when space vector modulation (SVM) is utilized [28]. Additionally, the available switch (states) combinations are reduced from eight (in B6 inverter) to four (in B4 inverter) without a zero-voltage vector [29].

To maintain the same output voltage, the DC link voltage must be doubled. Increasing the DC link side voltage dictates the use of switching devices with higher ratings [30]. Moreover, for adjustable speed drives, an increase in stress on motor winding is expected as a result of raising the DC link voltage [31]. Additionally, switching losses depend on the voltage, hence an increase in switching losses may be expected despite using fewer switches.

Higher-voltage-rated power semiconductor devices not only implies slower responses with lower overall efficiency but also higher costs and greater size [32]. Thus, multilevel inverters, particularly neutral-point diode-clamped inverters (NPC), become a viable solution [33]. Typically, multilevel inverters are used in medium-voltage high-power applications [34]. They offer lower voltage harmonics along with less electromagnetic interference. In addition, lower-voltage-rated switches are used hence reducing *dv/dt* [35].

The eight-switch (B8) inverter, which emerged as the post-fault reconfiguration of the conventional NPC inverter, is considered a potentially cost-effective inverter [36,37]. Compared with the B6 inverter, the B8 inverter has the merit of offering three-level operation, only with two extra switches [38,39], and hence better performance with an expected slightly higher cost.

On the other hand, the B8 inverter utilizes eight switches, which is double the number of power semiconductors in the B4 inverter; however, lower-voltage-rated switches are deployed [40,41]. Hence, the B8 inverter allows a series connection of fast, low-voltage, and efficient switches, but with the penalty of an increased number of gate drives and clamping diodes [42,43]. Increasing the number of switches in the B8 inverter results in nine different voltage vectors as opposed to four voltage vectors in the B4 inverter. Importantly, a zero-voltage vector is available in the B8 inverter (being particularly useful for common mode voltage control) which is absent in the B4 inverter [44–47].

There has not been any assessments comparing the performance of the B8 with the B6 inverter or with the B4 inverter. Furthermore, there is no thorough comparison between the B4 and B6 inverters. This paper presents a comprehensive comparative review to assess the performance and cost of three power inverters, namely the B6, B4, and B8 inverters, for applications below ≈3.3 kV ac.

This paper is organized as follows: Section 2 sheds light on the operation of the conventional six-switch (B6) inverter. Section 3 studies the reduced-cost four-switch (B4) inverter, highlighting the available voltage vectors, SVM operation, and the generation of zero voltage vector. Section 4 considers the NPC eight switch (B8) inverter illustrating its configuration, operation, and control. A comprehensive comparison between the three inverters is presented in Section 5, along with guidelines to properly select a suitable power inverter based on the application. Finally, conclusions and suggestions for future research are given in Sections 6 and 7, respectively.

2. Six Switch (B6) Inverter

Figure 1 shows the circuit diagram of a conventional six-switch, or the B6, inverter.

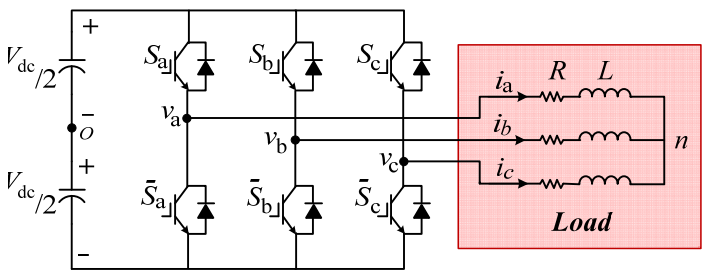

Figure 1. Six switch (B6) inverter.

The two series switches in each leg are normally complementary, at least so that no two series switches are on simultaneously, to avoid a DC supply short circuit.

The balanced three-phase voltages $(v_{an},\ v_{bn},\ v_{cn})$ are described via (1):

$$v_{xn} = v_{xo} - v_{on} \tag{1}$$

where x represents the phase (a, b, and c).

The inverter voltage with respect to the reference, o, is as follows:

$$v_{xo} = (2S_x - 1)\frac{V_{dc}}{2} \tag{2}$$

with S_x representing the state of the switch; 1 is for the ON state and 0 is for the OFF state.

Therefore, from (1) and (2), v_{on} (which represents the common mode voltage, CMV) is defined via the following:

$$v_{on} = {}^1\!/_3(v_{ao} + v_{bo} + v_{co}) \tag{3}$$

Combining (1)–(3), the balanced three-phase load voltages in matrix form are given via (4):

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} V_{dc} \tag{4}$$

Generally, SVM is utilized to control the switches, thus generating the required balanced three-phase load voltages. SVM maximizes DC link voltage utilization, and also has lower switching losses and total harmonic distortion than those in conventional sinusoidal pulse width modulation.

To implement the SVM control approach, the three-phase voltages in *abc* co-ordinates are transformed into a two-phase $\alpha\beta$ co-ordinate system using Clarke's transformation, which is described via (5):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = {}^2\!/_3 \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & 1/2\sqrt{3} & 1/2\sqrt{3} \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{5}$$

where the factor $2/3$ is used to maintain constant output voltage magnitude.

The magnitude of the reference voltage along with its angle are defined via (6) and (7), respectively:

$$v_{ref} = \sqrt{v_\alpha^2 + v_\beta^2} \tag{6}$$

$$\theta = \tan^{-1}\frac{v_\beta}{v_\alpha} \tag{7}$$

The B6 inverter has eight switch states (six active states and two zero states) which are utilized to generate the required balanced three-phase load voltages. Figure 2 shows the active switch states along with the voltage sectors, while Table 1 summarizes the output of the eight possible switch combinations along with the corresponding CMV.

Table 1. B6 inverter switch states.

Vector	S_a	S_b	S_c	$v_{ref}\angle\theta$	CMV
0	0	0	0	$0\angle 0^\circ$	$-1/2V_{dc}$
1	1	0	0	$2/3V_{dc}\angle 0^\circ$	$-1/6V_{dc}$
2	1	1	0	$2/3V_{dc}\angle 60^\circ$	$1/6V_{dc}$
3	0	1	0	$2/3V_{dc}\angle 120^\circ$	$-1/6V_{dc}$
4	0	1	1	$2/3V_{dc}\angle 180^\circ$	$1/6V_{dc}$
5	0	0	1	$vV_{dc}\angle 240^\circ$	$-1/6V_{dc}$
6	1	0	1	$2/3V_{dc}\angle 300^\circ$	$1/6V_{dc}$
7	1	1	1	$0\angle 0^\circ$	$1/2V_{dc}$

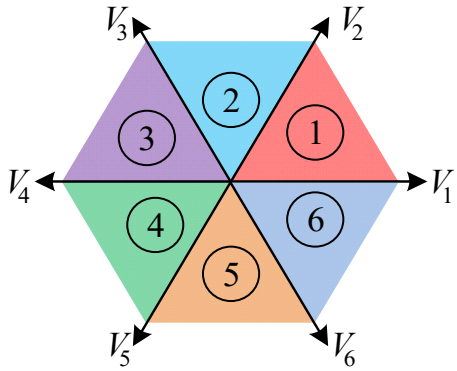

Figure 2. B6 switch states.

The three-phase balanced voltages are represented by a rotating vector when transformed to the space vector domain. Hence, the required balanced three-phase load voltages are transformed from *abc* co-ordinates into $\alpha\beta$ co-ordinates via (5) and then represented by a rotating vector using (6) and (7). Depending on the location of the reference voltage, the sector is determined and hence the proper switch states are deployed. The reference voltage is synthesized using two adjacent active voltage vectors and the two zero vectors.

To determine the time of each switch state, the volt second equation, defined by (8), must be satisfied.

$$v_{ref}T_s = v_xT_x + v_yT_y + v_0T_0 \tag{8}$$

where T_s is the sampling time, v_x and v_y represent the two adjacent active vectors, with times T_x and T_y respectively, while v_0 represents the zero vector with time T_0. The switch times T_x, T_y, and T_0 are defined via (9)–(11), respectively:

$$T_x = \frac{\sqrt{3}T_sv_{ref}}{V_{dc}}\sin(60^\circ m - \theta) \tag{9}$$

$$T_y = \frac{\sqrt{3}T_sv_{ref}}{V_{dc}}\sin(\theta - 60^\circ\{m-1\}) \tag{10}$$

$$T_0 = T_s - T_x - T_y \tag{11}$$

where m is the sector

Table 2 summarizes the switch times for switches S_a, S_b, and S_c, where these times are compared with a carrier signal of amplitude, T_s, to generate the required gating pulses.

Table 2. B6 inverter switch times.

Sector	S_a	S_b	S_c
1	$T_x + T_y + {}^1/_2T_0$	$T_y + {}^1/_2T_0$	${}^1/_2T_0$
2	$T_x + {}^1/_2T_0$	$T_x + T_y + {}^1/_2T_0$	${}^1/_2T_0$
3	${}^1/_2T_0$	$T_x + T_y + {}^1/_2T_0$	$T_y + {}^1/_2T_0$
4	${}^1/_2T_0$	$T_x + {}^1/_2T_0$	$T_x + T_y + {}^1/_2T_0$
5	$T_y + {}^1/_2T_0$	${}^1/_2T_0$	$T_x + T_y + {}^1/_2T_0$
6	$T_x + T_y + {}^1/_2T_0$	${}^1/_2T_0$	$T_x + {}^1/_2T_0$

From Figure 2 (according to the radius of the largest circle inscribed in the hexagon), the maximum output phase voltage (in the linear modulation region) which can be synthesized using SVM for the B6 inverter is $V_{dc}/\sqrt{3}$.

3. Four Switch (B4) Inverter

The four-switch (B4) inverter only has two semiconductor legs (each containing two complementary switches), while the conventional third leg is replaced with a split DC capacitor as illustrated in Figure 3.

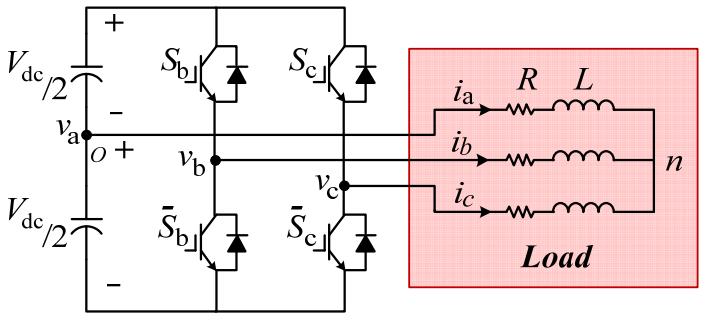

Figure 3. Four-switch (B4) inverter.

Since one of the phases (phase 'a' for example) is connected to the mid-point of the split DC capacitor, its voltage is fixed to zero, as defined via (12):

$$v_{ao} = 0 \tag{12}$$

While phases b and c voltages with respect to the reference, o, are given via (13):

$$v_{xo} = (2S_x - 1)\frac{V_{dc}}{2} \tag{13}$$

The balanced three-phase load voltages in matrix form are given via (14):

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} 1/2 \\ S_b \\ S_c \end{bmatrix} V_{dc} \tag{14}$$

The B4 inverter only has two sectors with four active switch states without any zero states. Figure 4 shows the four available switch states along with the voltage sectors.

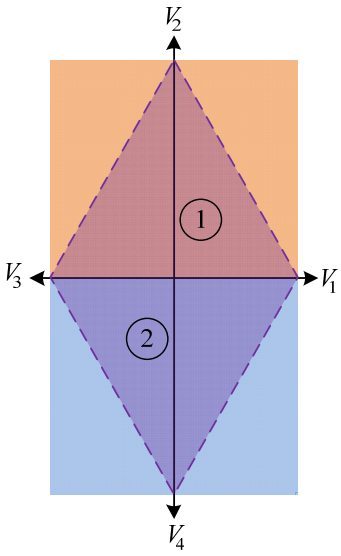

Figure 4. B4 switch states.

Table 3 summarizes the output of the four possible switch combinations and the different CMVs.

Table 3. B4 inverter switch states.

Vector	S_b	S_c	$v_{ref}\angle\theta$	CMV
1	0	0	$1/3V_{dc}\angle 0^{\circ}$	$-1/3V_{dc}$
2	1	0	$1/\sqrt{3}V_{dc}\angle 90^{\circ}$	0
3	1	1	$1/3V_{dc}\angle 180^{\circ}$	$1/3V_{dc}$
4	0	1	$1/\sqrt{3}V_{dc}\angle 270^{\circ}$	0

Depending on the location of the reference voltage, the sector is determined and hence the proper switch states are deployed. The reference voltage is synthesized using three active vectors (where two opposite vectors are used to generate the missing zero state).

For operation in sector one, the three vectors V_2, V_1, and V_3 are utilized with the switch times T_2, T_1, and T_3 defined via (15)–(17), respectively:

$$T_2 = \frac{\sqrt{3}v_{ref}}{V_{dc}} T_s \sin\theta \tag{15}$$

$$T_1 = \frac{T_s}{2}\left\{1 - \frac{T_2}{T_s} + \frac{3v_{ref}}{V_{dc}}\cos\theta\right\} \tag{16}$$

$$T_3 = T_s - T_1 - T_2 \tag{17}$$

On the other hand, when the reference voltage vector is in sector two, the switch times T_4, T_1, and T_3 for the vectors V_4, V_1, and V_3 are given by (18)–(20), respectively:

$$T_4 = -\frac{\sqrt{3}v_{ref}}{V_{dc}} T_s \sin\theta \tag{18}$$

$$T_1 = \frac{T_s}{2}\left\{1 - \frac{T_4}{T_s} + \frac{3v_{ref}}{V_{dc}}\cos\theta\right\} \tag{19}$$

$$T_3 = T_s - T_1 - T_4 \tag{20}$$

Table 4 summarizes the switch times for S_b and S_c.

Table 4. B4 inverter switch times.

Sector	S_b	S_c
1	$T_2 + T_3$	T_3
2	T_3	$T_3 + T_4$

From Figure 4, the maximum output phase voltage (in the linear modulation region) which can be synthesized using SVM for the B4 inverter is $V_{dc}/2\sqrt{3}$.

4. Eight Switch (B8) Inverter

The eight-switch (B8) inverter (which is the post-fault reconfiguration of the three-level NPC inverter) is shown in Figure 5.

The B8 inverter has two legs with four switches in each leg. Switches S_{x1} and S_{x3}, and S_{x2} and S_{x4} are complementary. Phase a is connected to the mid-point of the split DC capacitor; hence, its voltage is fixed as given via (21):

$$v_{ao} = 0 \tag{21}$$

Phases b and c voltages with respect to the reference, o, are given via (22):

$$v_{xo} = (S_{x1} + S_{x2} - 1)\frac{V_{dc}}{2} \tag{22}$$

The balanced three-phase load voltages are given via (23):

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \begin{bmatrix} 1 \\ S_{b1} + S_{b2} \\ S_{c1} + S_{c2} \end{bmatrix} \frac{V_{dc}}{2} \tag{23}$$

The B8 inverter has nine different switch states (eight active states and one zero state) which are utilized to generate the required balanced three-phase load voltages. Table 5 summarizes the output of the eight possible switch combinations along with the generated CMV.

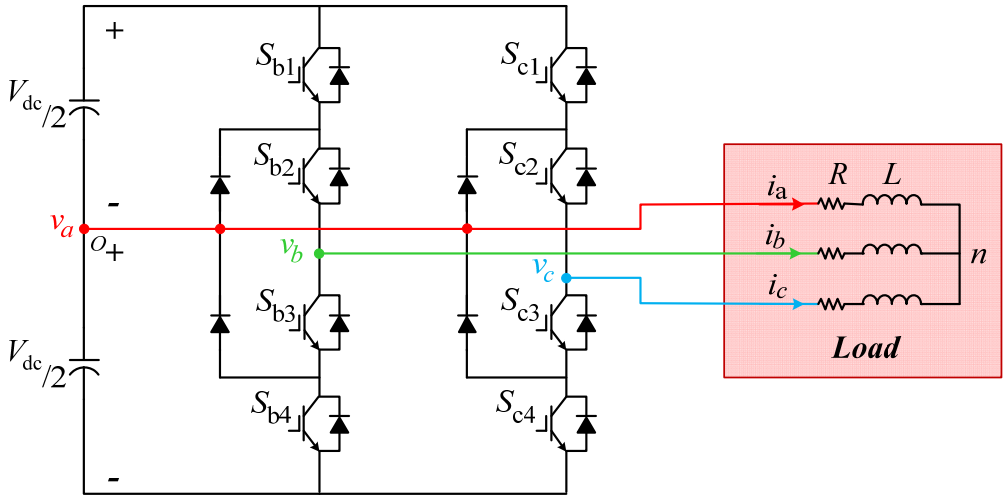

Figure 5. Eight-switch (B8) inverter.

Table 5. B8 inverter switch states.

Vector	S_{b1}	S_{b2}	S_{c1}	S_{c2}	$v_{ref}\angle\theta$	CMV
0	0	1	0	1	$0\angle 0^\circ$	0
1	0	0	0	0	$1/3V_{dc}\angle 0^\circ$	$-1/3V_{dc}$
2	0	1	0	0	$1/3V_{dc}\angle 60^\circ$	$-1/6V_{dc}$
3	1	1	0	0	$1/\sqrt{3}V_{dc}\angle 90^\circ$	0
4	1	1	0	1	$1/3V_{dc}\angle 120^\circ$	$1/6V_{dc}$
5	1	1	1	1	$1/3V_{dc}\angle 180^\circ$	$1/3V_{dc}$
6	0	1	1	1	$1/3V_{dc}\angle 240^\circ$	$1/6V_{dc}$
7	0	0	1	1	$1/\sqrt{3}V_{dc}\angle 270^\circ$	0
8	0	0	0	1	$1/3V_{dc}\angle 300^\circ$	$-1/6V_{dc}$

The eight active switch states are divided into six short vectors and two medium vectors, hence two possible SVM approaches are available. However, utilizing the six active short vectors and avoiding the two active medium vectors gives better performance than does utilizing the eight active vectors [47].

Figure 6 shows the eight active switch states along with the six voltage sectors.

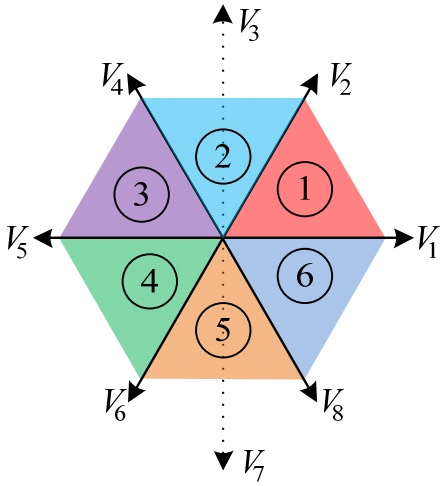

Figure 6. B8 switch states.

Depending on the location of the reference voltage, the sector is determined and hence the proper switch states are deployed. The reference voltage is synthesized using two adjacent active short voltage vectors and the zero vector.

The switch times T_x, T_y, and T_0, representing the times of the two adjacent active short vectors and the zero vector respectively, are defined via (24)–(26):

$$T_x = \frac{2\sqrt{3}T_s v_{ref}}{V_{dc}} \sin(60^\circ m - \theta) \tag{24}$$

$$T_y = \frac{2\sqrt{3}T_s v_{ref}}{V_{dc}} \sin(\theta - 60^\circ \{m - 1\}) \tag{25}$$

$$T_0 = T_s - T_x - T_y \tag{26}$$

The times calculated in (24)–(26) are similar to those of the B6 inverter except for the multiplication by a factor of two (this is due to the reduction in DC link utilization as will be illustrated later). Furthermore, the switch time of the zero vector is achieved using the only available zero state for the B8 inverter. But two zero vectors are available for the B6 inverter which are both utilized to generate the zero-voltage state.

Table 6 summarizes the switch times for switches S_{b1}, S_{b2}, S_{c1}, and S_{c2}.

Table 6. B8 inverter switch times.

Sector	S_{b1}	S_{b2}	S_{c1}	S_{c2}
1	–	$T_y + T_0$	–	T_0
2	T_y	$T_x + T_y + T_0$	–	$T_y + T_0$
3	$T_x + T_y$	$T_x + T_y + T_0$	T_y	$T_x + T_y + T_0$
4	T_x	$T_x + T_y + T_0$	$T_x + T_y$	$T_x + T_y + T_0$
5	–	$T_x + T_0$	T_x	$T_x + T_y + T_0$
6	–	T_0	–	$T_x + T_0$

The maximum output phase voltage (in the linear modulation region) which can be synthesized using SVM for the B6 inverter is $V_{dc}/2\sqrt{3}$.

5. Comparison between the B6, B4, and B8 Inverters

This section presents a comprehensive comparison between the three inverters, viz the conventional six-switch (B6) inverter, the reduced switch count four-switch (B4) inverter, and the eight-switch (B8) NPC inverter. The comparison covers aspects including DC link

voltage utilization, switch ratings, losses, cost, and performance. Table 7 illustrates the parameters of the simulation model. The Simulink model for the B4 inverter, as an example, is illustrated in Appendix A. Results are demonstrated in Figure 7.

Table 7. Simulation parameters.

Parameter	Value
Output voltage (rms L-L)	380 V
Output frequency	50 Hz
Load resistance	10 Ω
Load inductance	10 mH
DC link capacitor	5 mF
Switching frequency	2.75 kHz

The DC link voltage of the B6 inverter is 600 V since the DC link voltage utilization of the B4 and the B8 inverters is half that for the B6 inverter. Therefore, a 1200 V DC link is utilized for the B4 and the B8 inverters to attain the same output voltage. Figure 7a shows the three-phase load currents for the three inverters, where B6 has the best current quality with 2.38% total harmonic distortion (THD). However, using a 1200 V DC link voltage for the B4 inverter increases the THD to 5.95%. Introducing a three-level operation for the B8 inverter reduces the THD to 3.41% (which is still higher than that of the B6 inverter as a result of the need to double the DC link voltage). Figure 7b shows the harmonic content for the three inverters, while Figure 7c shows the pole voltage for the three inverters. The voltage harmonic spectrum is demonstrated in Figure 7d. Investigating the voltage harmonic spectrum is crucial to identify which harmonic order has the highest magnitude. This guides the designer in selecting the appropriate passive filter in grid-connected applications [48].

Since CMV is an important factor [49,50] for three-phase inverters (particular when feeding electrical machines), it is highlighted in Figure 7e. The B6 inverter has a CMV of $\pm 1/2 V_{dc}$. Since the DC link voltage is 600 V for the B6 inverter, the CMV is ±300 V. The CMV for the B4 and the B8 inverters is $\pm 1/3 V_{dc}$, specifically ±400 V, since the DC link voltage is doubled.

The performance of the three inverters is investigated at half the load given in Table 7 with the results in Figure 8. Balanced three-phase currents are achieved with the three inverters as shown in Figure 8a. The current harmonic content is demonstrated in Figure 8b. As expected, reducing the load (while maintaining the same switching frequency) increases the THD. However, still, the B6 inverter has the lowest THD, at 4.57%, followed by the B8 inverter, at 6.54% and finally, the B4 inverter with the highest THD, at 11.48%. Phase voltage is shown in Figure 8c with the voltage harmonics illustrated in Figure 8d. Finally, CMV is highlighted in Figure 8e.

For a comprehensive comparison, the switching losses and conduction losses of the three inverters must be assessed [51,52]. Table 8 illustrates the main specifications of the utilized power switches. All switches are IXYZ—the same technology.

Table 8. Specifications of the power switches.

Point	B4 Inverter	B6/B8 Inverter
Switch	IXFB30N120P	IXFR48N60P
Voltage rating (V)	1200	600
Current Rating (A)	30	32
Turn on resistance (Ω)	0.35	0.15
Turn on rise time (ns)	60	25
Turn off fall time (ns)	56	22

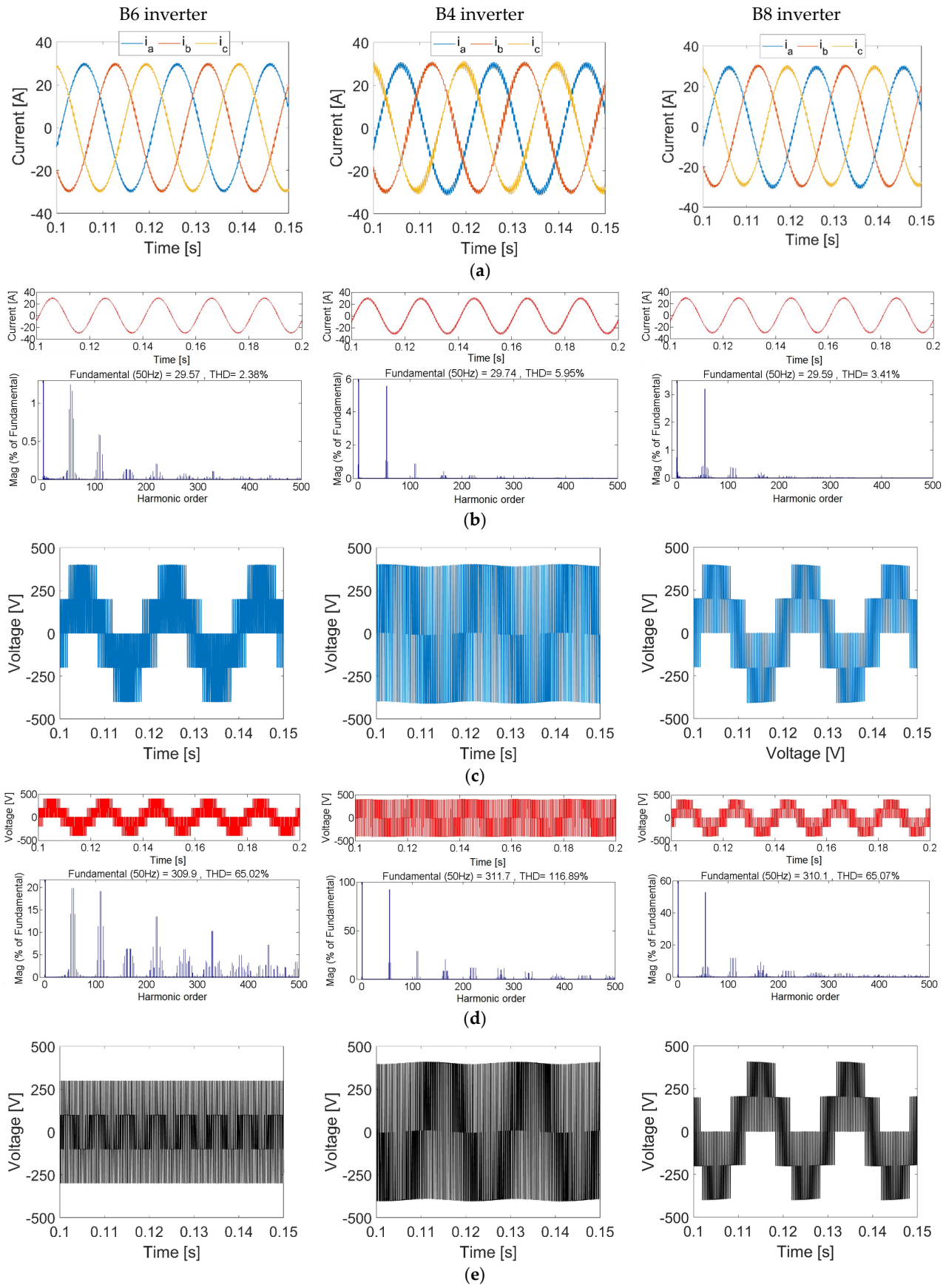

Figure 7. Comparison between B6, B4, and B8 inverters at full load. (**a**) Load currents, (**b**) current FFT analysis, (**c**) pole voltage, (**d**) voltage FFT analysis, and (**e**) CMV.

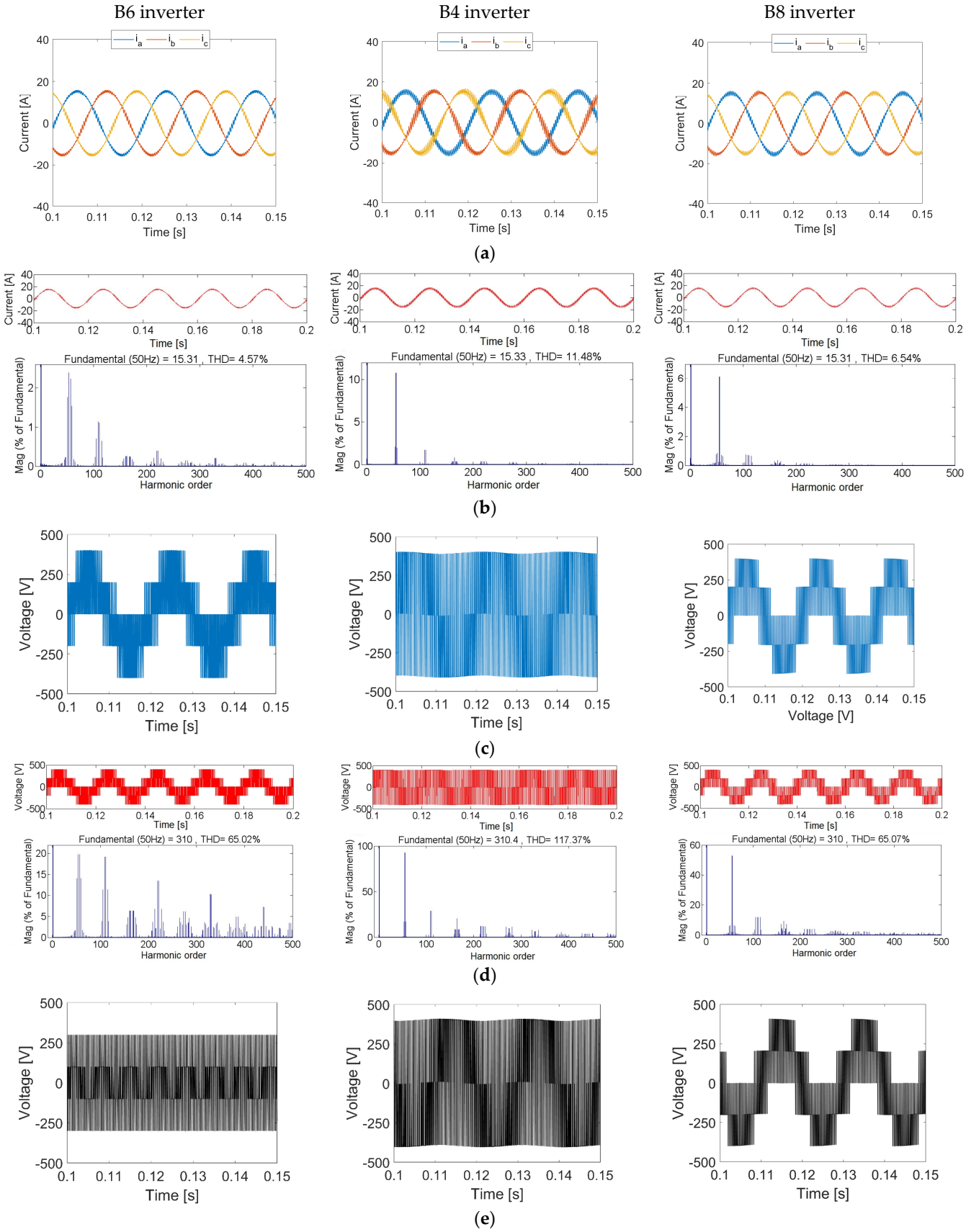

Figure 8. Comparison between B6, B4, and B8 inverters at half load. (**a**) Load currents, (**b**) current FFT analysis, (**c**) pole voltage, (**d**) voltage FFT analysis, and (**e**) CMV.

The power MOSFET conduction loss is as follows:

$$P_{cond} = I_{D,rms}^2 R_{DSon} \tag{27}$$

where R_{DSon} is the drain-source on-state resistance and $I_{D,rms}$ is the load rms current.

The conduction loss can be calculated using the drain-source on-state resistance which is obtained from the datasheet, as in Table 8 with the B4 inverter utilizing four 1200 V switches. The B6 and B8 inverters utilize six and eight 600 V switches, respectively. Using (27), and for the same rms current, the conduction losses of the B4 and B8 inverters with respect to the B6 inverter are 1.56 and 1.33, respectively.

Switching losses arise during switch turn on/off, where the losses depend on the drain-source voltage (V_{DS}), load current (I_D), switching frequency (f_s), and the turn-on/off times (t_{on}, t_{off}, respectively) (losses in clamping diodes are neglected as fast Schottky devices are deployed).

Equation (28) defines the switching losses assuming a linear voltage/current switching behavior.

$$P_{sw} = \frac{V_{DS}\ I_D \left(t_{on} + t_{off}\right)}{6} f_s \tag{28}$$

For the same switching frequency and load current, the switching losses of the B4 and B8 inverters with respect to the B6 inverter are in the ratio of 3.3:1 and 1.33:1, respectively. Since the B8 inverter uses the same switch ratings as the B6 inverter, a 33% increase in the switching and conduction losses is expected as a result of requiring two extra switches (neglecting losses in clamping diodes as fast Schottky devices can be deployed), while the B4 inverter requires fewer switches. However, the increase in the switch voltage rating results in an increase in switching and conduction losses.

Converter efficiency is calculated as follows:

$$\eta = \frac{output\ power}{output\ power + losses} \times 100\% \tag{29}$$

The three inverters feed a 13.5 kW load. Based on (27)–(29), the efficiencies of the B6, B8, and B4 inverters are 97.0%, 96.1%, and 95.5%, respectively. This reveals that the B6 inverter has the best efficiency, followed by the B8 inverter, with the B4 inverter coming last. This is expected as the B4 inverter has the highest switching and conduction losses as a result of deploying slow, higher-voltage power semiconductor devices. Subsequently, the B4 inverter requires a larger heat sink followed by B8 and finally the B6 inverter.

To extend the inverter performance study, Figure 9 investigates the efficiency and THD at different power levels.

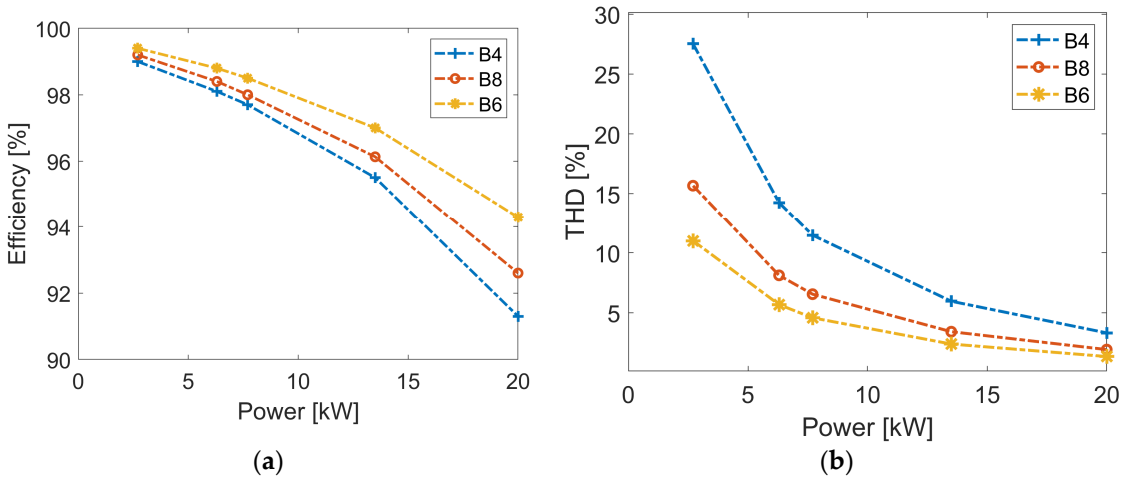

Figure 9. B6, B4, and B8 inverters' performances at different power levels. (**a**) Efficiency and (**b**) THD.

Figure 9a shows the efficiency at different converter output powers. At low output power levels, the switching and conduction losses are minimal as the load current is reduced, hence the efficiency is high. Increasing the load power results in an increase in current and thereby switching and conduction losses result in efficiency degradation. Furthermore, Figure 9a reveals that at all power levels the B6 inverter has the highest efficiency, while the B4 has the lowest.

Since THD is an important performance aspect, Figure 9b studies the variation in THD for the three inverters at different output power levels with the same switching frequency. As expected, the B6 inverter has the best performance with the lowest THD, followed by the B8 inverter, and then the B4 inverter. All the results are at the same switching frequency, for a valid comparison. At light loads with low currents, the THD increases as expected.

The previous results presented the performance of the three inverters when feeding a static RL load, so to further investigate inverter performance, a dynamic load is required. An induction motor (IM), with the parameters in Table 9, is used as the dynamic load. The switching frequency is the same as that for previous results (2.75 kHz).

Table 9. IM parameters.

Parameter	Value
Voltage (rms L-L)	380 V
Frequency	50 Hz
Torque	50 Nm
Speed	1440 rpm
Stator resistance	0.6 Ω
Rotor resistance	0.63 Ω
Stator leakage inductance	3.5 mH
Rotor leakage inductance	5.47 mH
Mutual inductance	35.4 mH

The performance of the three inverters is demonstrated in Figure 10. The three-phase stator currents are shown in Figure 10a from the instant of IM starting until the steady state. Direct on-line starting is applied, which justifies the high starting current. The current harmonic spectrum is illustrated in Figure 10b. As expected, the B6 inverter has the lowest THD, at 2.57%, while the B4 inverter recorded the lowest THD, at 6.22%. The three-level operation of the B8 inverter improves the THD to 3.66%, compared to the B4 inverter; however, its performance is not better than that of the B6 inverter due to the higher DC link voltage.

All the previous results are obtained at the same low switching frequency (2.75 kHz). In order to illustrate the switching frequency effect on inverter performance, the IM load, with the parameters in Table 9, is fed from the three inverters operating at a 5 kHz switching frequency. Results are seen in Figure 11.

Balanced three-phase stator currents are achieved in the steady state by the three inverters, as shown in Figure 11a. Increasing the switching frequency improves the current quality as highlighted in Figure 11b, where a reduction in THD is recorded for all the three inverters, when a 5 kHz switching frequency is deployed as opposed to that of 2.75 kHz. The results are given in Figure 10. Additionally, as expected, the B6 inverter still offers the best performance with the lowest THD among the three inverters at 1.41%, followed by the B8 inverter, at 2.01%, and finally the B4 inverter, at 3.42%.

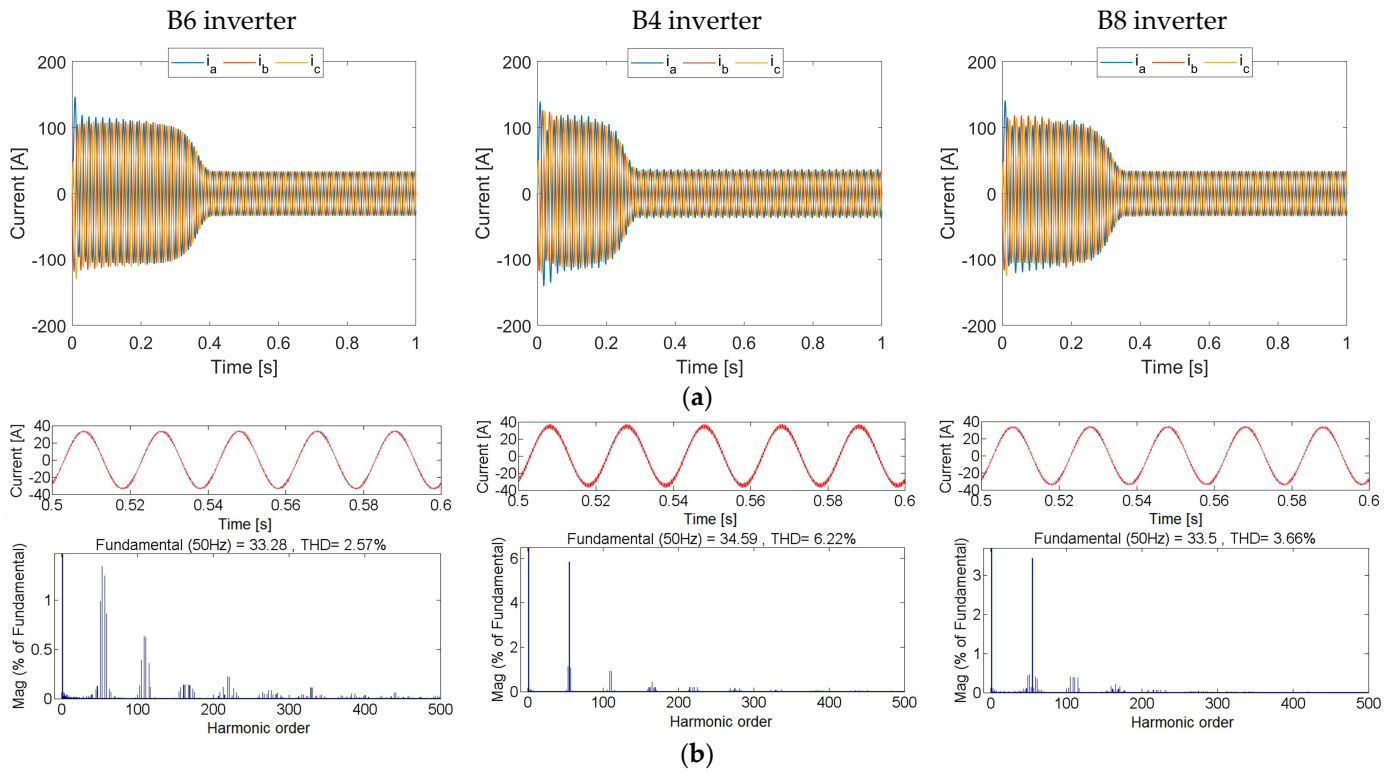

Figure 10. Comparison between B6, B4, and B8 inverters feeding an IM load. (**a**) Load currents and (**b**) current FFT analysis.

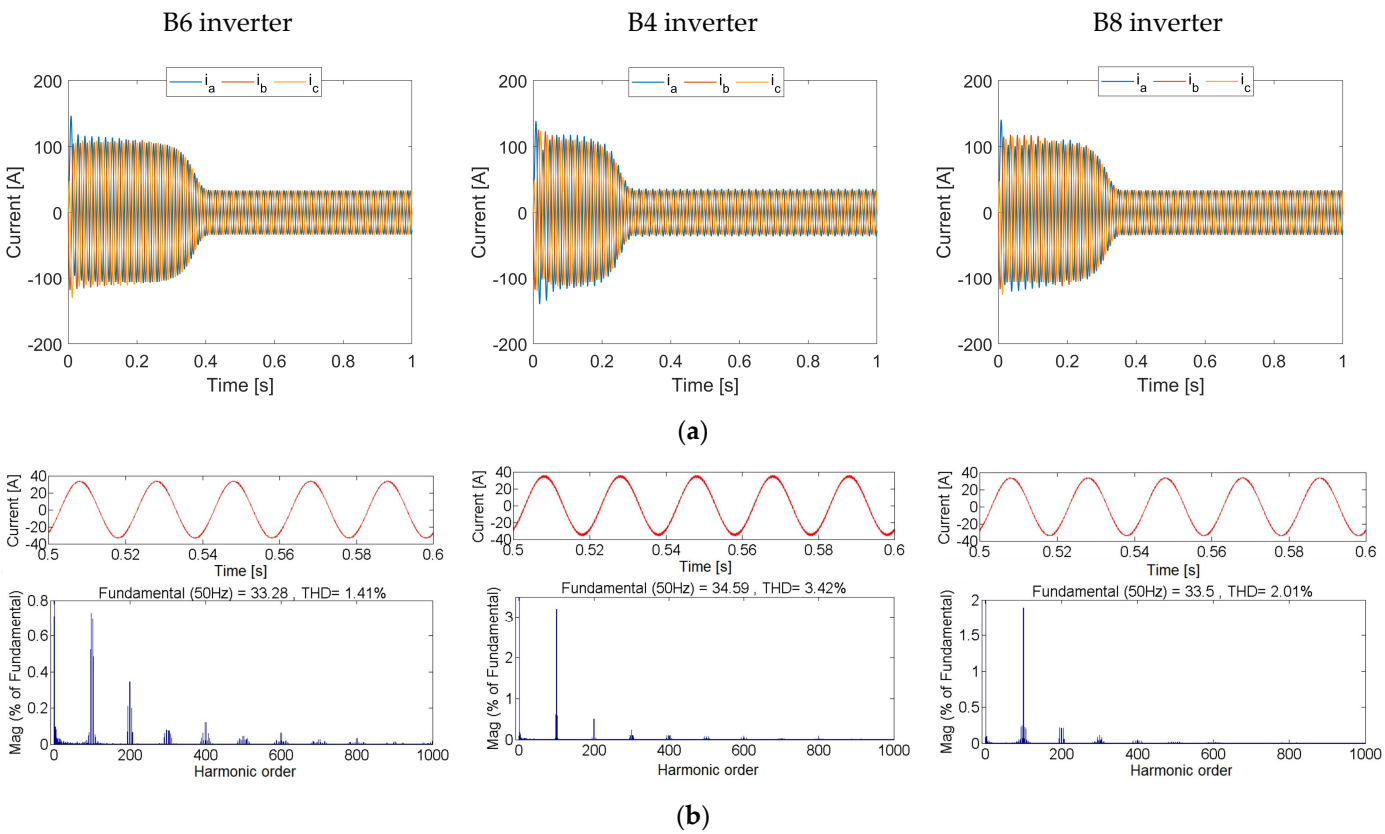

Figure 11. Comparison between B6, B4, and B8 inverters with higher switching frequency feeding IM load: (**a**) load currents, and (**b**) current FFT analysis.

For critical applications, reliability is of prime importance [53]. Reliability could be defined as the ability of a component to function properly for a period of time without failure. In power inverters, semiconductor devices and particularly DC link electrolytic capacitors are items prone to failure. Electrolytic-type capacitors tend to be avoided, at the expense of increased costs. Due to the switching and conduction losses in power semiconductor devices, where energy is dissipated in the form of heat, a rise in junction temperature is expected. The variation in junction temperature leads to thermomechanical stress which can result in device failure. Furthermore, gate drive circuit failure will result in converter malfunction. With the B8 inverter being composed of eight power switches, four clamping diodes and eight gate drivers, the probability of converter failure is higher. On the other hand, the B4 inverter has only four power switches and gate drivers; hence, it has the highest reliability among the three inverters from the power semiconductor device's point of view.

Since the B4 inverter operates with a DC link voltage that is twice that of a corresponding B6/B8 inverter, the voltage rating of B4 power semiconductor devices is higher, resulting in higher switching and conduction losses. If the generated heat energy is not efficiently dissipated via the proper selection of switches, and heat sink design, the B4 inverter will be more prone to failure.

On the other hand, both the B4 and B8 inverters connect one of the phases to the center point of the DC link capacitor, resulting in capacitor voltage ripple. This capacitor voltage ripple (hence current ripple) suggests that B4 and B8 DC link capacitors are more prone to failure than is the B6 inverter capacitor.

Generally, four approaches could be implemented to improve power inverter reliability, specifically utilizing robust components in a better-cooled environment, continuous monitoring and control, utilizing advanced power semiconductor devices, specifically wide-bandgap GaN and SiC devices, and finally increasing inverter redundancy by utilizing extras switches to reconfigure the inverter in case of switch failure.

Table 10 gives a comprehensive comparison between B6, B4, and B8 inverters.

Table 10. Comparison between B6, B4, and B8 inverters.

Feature	B6	B4	B8
DC link voltage (for same output voltage)	V_{dc}	$2V_{dc}$	$2V_{dc}$
Number of DC link capacitors	2	2	2
DC link capacitor voltage	$1/2V_{dc}$	V_{dc}	V_{dc}
Number of gate drivers	6	4	8
Number of switches (and freewheel diodes)	6	4	8
Switch voltage rating	V_{dc}	$2V_{dc}$	V_{dc}
Total switches, VA	$6\ V_{dc}I$	$8\ V_{dc}I$	$8\ V_{dc}I$
Number of clamping diodes	–	–	4
Clamping diode rating	–	–	V_{dc}
Total clamping diodes, VA	–	–	$4\ V_{dc}$
Circuit complexity	Moderate	Low	High
Converter size	Moderate	Compact	Large
Converter reliability	Moderate	High	Low
Computational burden	Moderate	Low	Moderate
Switch states	8	4	9
Switching/Conduction losses	Low	High	Moderate
Heat sink size	Small	Large	Medium
THD	Low	High	Moderate
CMV	Low	Moderate	Moderate

Figure 12 summarizes the comparison between the B6, B4, and B8 inverters in terms of seven aspects, namely cost effectiveness, compactness, converter simplicity, computational speed, efficiency, THD, and CMV. Each aspect is scaled from 1 to 10.

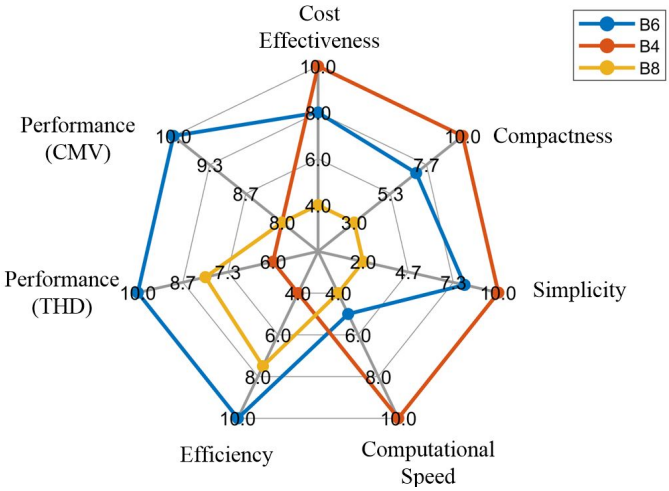

Figure 12. Converter comparison.

6. Conclusions

This paper presented a comprehensive comparison between three types of widely deployed power inverters used in lower-voltage applications (<3.3 kV ac); namely, the six-switch (B6) inverter, the reduced-switch-count (B4) inverter, and the eight-switch NPC (B8) inverter. The comparison covered aspects including circuit diagram, operation, SVM techniques, semiconductor device rating, switching and conduction losses, output current THD, and the complexity of the inverters. It is concluded that the B6 inverter is superior in performance, which justifies its wide deployment in applications including high-power variable speed drives, renewable energy systems, electric vehicles, and active power filters. The B4 inverter is suitable for low-power applications where a compact and simple inverter is required. Typical applications for the B4 inverter include domestic home appliances, heating, ventilation and air-conditioning systems (HVAC), uninterruptable power supplies (UPS), micro-grid interfaces, photo-voltaic (PV) cells, motion control systems, and electric bikes.

Finally, the B8 inverter is seen to not be a suitable option in any application as it is complex, expensive, and has low performance (even with the presence of three-level operation due to the increase in DC link voltage) when compared with that of the B4 (compact inverter) and B6 (high-performance) inverter. Therefore, the B8 inverter is only suitable as a post-fault reconfiguration of the NPC inverter or possibly at voltage levels just beyond those suitable for the other two inverters (where other multi-series switch configurations become applicable).

7. Future Research

In order to extend the inverter operating range and improve the voltage utilization factor, overmodulation techniques are proposed and studied in detail in the literature for the conventional six-switch B6 inverter. However, overmodulation techniques have not been extensively investigated for the four-switch (B4) and eight-switch (B8) inverters. Enhancing the output voltage of the B4 inverter, which is suitable for applications requiring compact-size inverters, is beneficial to extending the operating range of the inverter. From another perspective, the B4 inverter switch voltage rating could be reduced (while maintaining the same output voltage by operating in the overmodulation region), resulting in a reduction in losses, hence an increase in inverter efficiency.

Furthermore, in the past decades there has been increased interest in the use of renewable energy resources. The use of inverters is inevitable for grid connection, resulting in harmonics being injected into the grid. The passive filter design has been investigated for the conventional B6 inverter. However, there has not been any research reported on the design of passive filters for the B4 and B8 inverters.

Finally, this paper presented a comprehensive comparison and evaluation of B6, B4, and B8 converters when deployed for DC–AC inverter applications. The research could be extended and generalized to compare the three converters when used for other applications, like AC–DC rectification (active front end rectifiers) and harmonic elimination, as shunt active power filters.

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Data Availability Statement: The data presented in this study are available in Appendices A and B.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The MATLAB/Simulink model for the B4 inverter is illustrated in Figure A1.

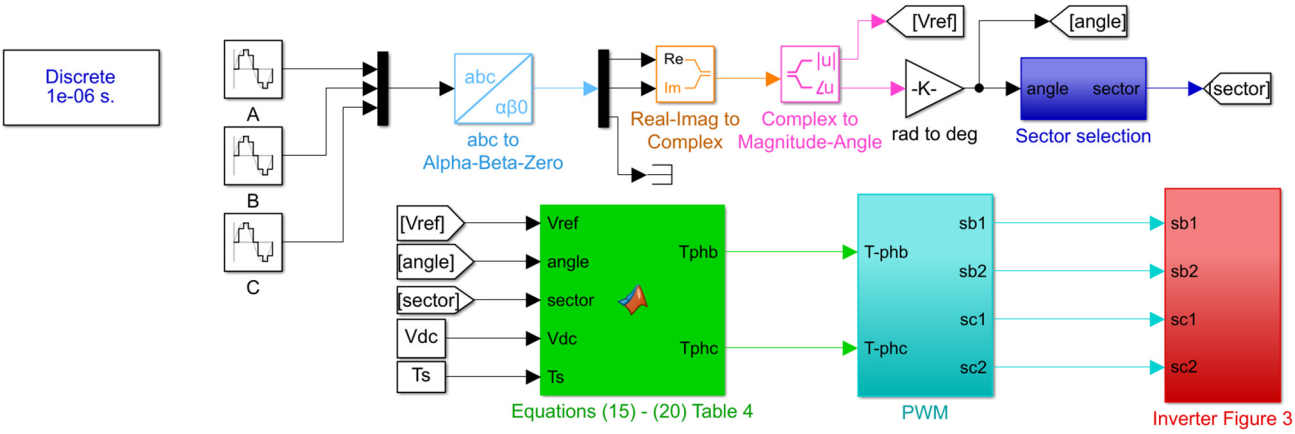

Figure A1. B4 MATLAB/Simulink model.

The required three-phase reference voltage is generated using sinusoidal sources.

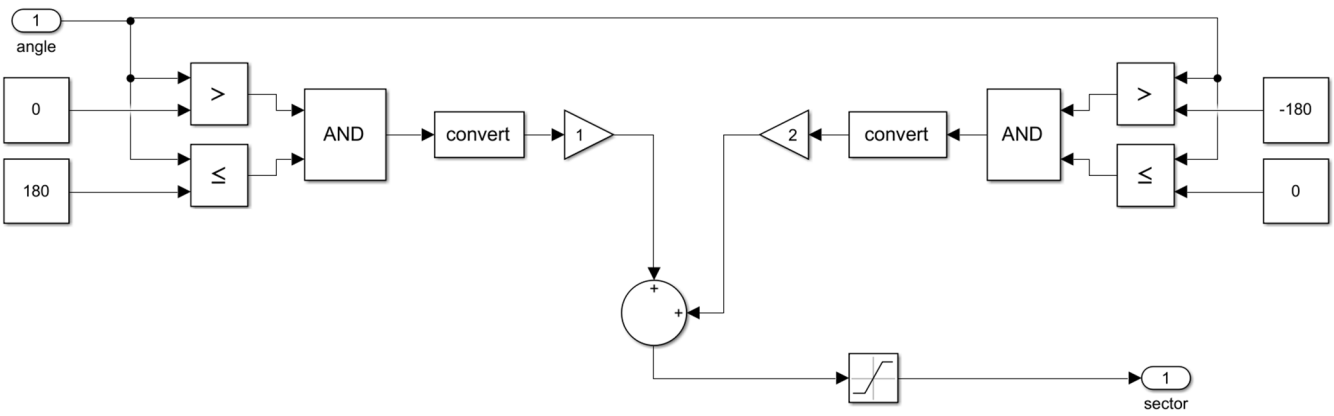

Figure A2. Sector determination.

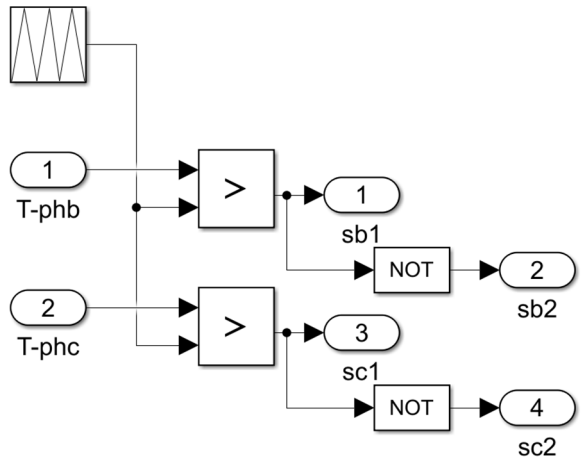

Figure A3. B4 PWM.

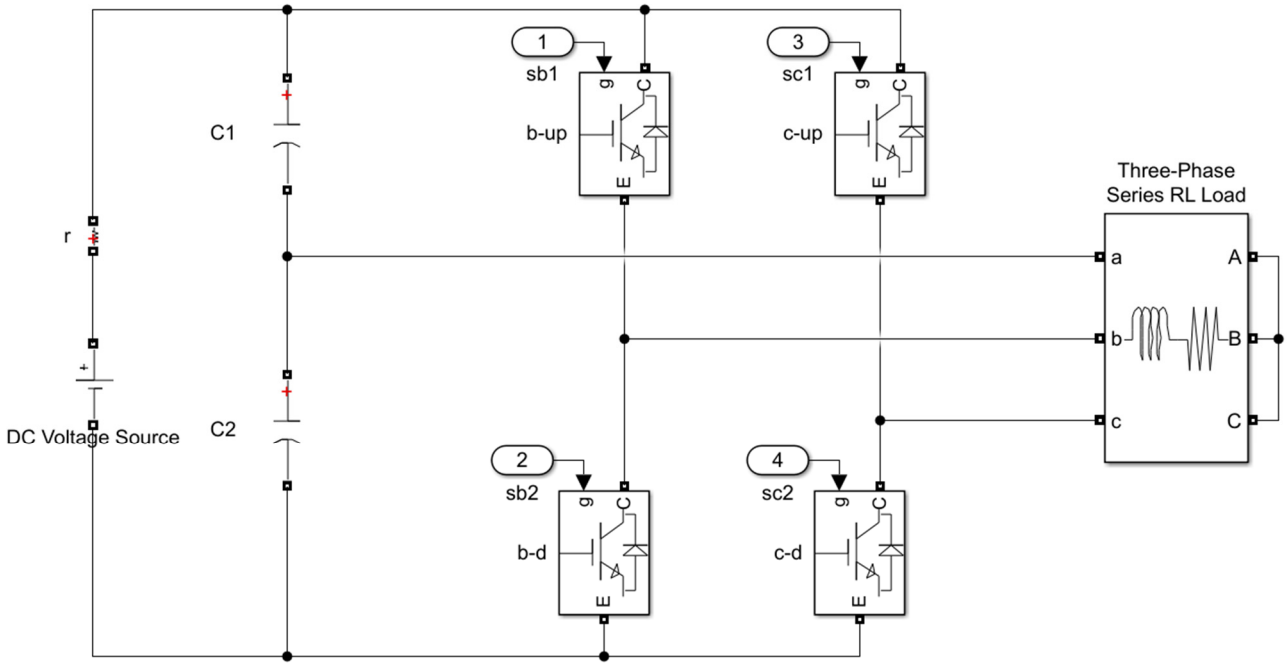

Figure A4. B4 inverter.

The balanced three-phase voltage is transformed using a Clarke transformation block (abc to αβ) as given via (5). The magnitude and phase are then extracted as defined via (6) and (7). Figure A2 shows the process of sector determination, where the phase is checked to determine if the reference vector is in sector 1 or 2. Based on the sector, an m-file MATLAB function block is used to determine the vector times as given via (15)–(20). Additionally, the switching times are then calculated as illustrated in Table 4. A copy of the m-file code is presented in Appendix B. A PWM block, as demonstrated in Figure A3, is deployed to generate the required gating signals. Considering a VSC, two switches in a leg are complementary; hence, the inversion of the upper switches' gate signal is evident. The switching times calculated via the function block are compared against a sawtooth signal. The generated gating signals control the B4 inverter switches shown in Figure A4. The B4 inverter is built using built-in Simulink IGBT/diode blocks.

The B6 and B8 inverters are simulated using the above detailed approach, but with the corresponding equations and circuit configuration.

Appendix B

MATLAB code:

```
function [Tphb, Tphc]= fcn(Vref,angle,sector,Vdc,Ts)


if sector==1
    T2=sqrt(3)*Vref/Vdc*Ts*sind(angle);
    T1=Ts/2*(1-T2/Ts+3*Vref/Vdc*cosd(angle));
    T3=Ts-T1-T2;
    T4=0;
      Tphb=T2+T3;
      Tphc=T3;
else
    T4=-sqrt(3)*Vref/Vdc*Ts*sind(angle);
    T1=Ts/2*(1-T4/Ts+3*Vref/Vdc*cosd(angle));
    T3=Ts-T1-T4;
    T2=0;
      Tphb=T3;
      Tphc=T4+T3;
end
```

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