A Two-Stage Interpolation Time-to-Digital Converter Implemented in 20 nm and 28 nm FGPAs

Yu Wang, Wujun Xie, Haochang Chen, Chengquan Pei, and David Day-Uei Li

***Abstract*—This article presents a two-stage interpolation time-to-digital converter (TDC), combining a Vernier gray code oscillator TDC (VGCO-TDC) and a tapped-delay line TDC (TDL-TDC). The proposed TDC uses the Nutt method to achieve a broad, high-resolution measurement range. It utilizes look-up tables (LUTs)-based gray code oscillators (GCOs) to build a VGCO-TDC as the first-stage interpolation for fine-time measurements. Then the overtaking residual from the VGCO-TDC is measured by a TDL-TDC to achieve the second-stage interpolation. Due to the two-stage interpolation architecture, the carry-chain-based delay line only needs to cover the resolution of the VGCO-TDC. Hence, we can reduce the delay-line length and related hardware resource utilization. We implemented and evaluated a 16-channel TDC system in Xilinx 20-nm Kintex-UltraScale and 28-nm Virtex-7 field-programmable gate arrays (FPGAs). The Kintex-UltraScale version achieves an average resolution (least significant bit, LSB) of 4.57 picoseconds (ps) with 4.36 LSB average peak-to-peak differential nonlinearity ($DNL_{pk\text{-}pk}$). The Virtex-7 version achieves an average resolution of 10.05 ps with 2.85 LSB average $DNL_{pk\text{-}pk}$.**

***Index Terms*—Two-stage interpolation, hybrid time-to-digital converter (TDC), field-programmable gate array (FPGA), low hardware utilization.**

I. INTRODUCTION

HIGH-resolution time-interval (TI) measurements play a crucial role in time-resolved scientific applications, including particle physics [1]–[5], time-of-flight positron emission tomography (ToF-PET) [6]–[9], Raman spectroscopy [10], [11] and fluorescence lifetime imaging microscopy (FLIM) [12]–[14]. Besides, industrial applications (such as hardware trojan detection [15], [16], light detection and ranging (LiDAR) [17]–[20], and analog-to-digital conversion [21]–[24]) also benefit from high-quality TI measurements. Hence, time-to-digital converters (TDCs) are highly focused due to picosecond (ps)-level resolutions.

The Nutt-TDC architecture (including both coarse counters and fine-time measurements) [25] is the mainstream for modern TDCs since it can simultaneously achieve a wide measurement range and a high resolution [26]–[28]. The coarse counter can be easily implemented through a clock-driven counter. So, most research focuses on fine-time measurements [29]. The main parameters to evaluate fine-time measurements are resolution, linearity, and precision. The resolution, also referred to as the least significant bit (LSB), is the quantization step for a TDC and defined as $Q = \frac{T}{n}$, where T is the period of the coarse-counting clock and n is the number of quantization steps in a period. However, quantization steps are not uniform, and this difference is characterized by differential nonlinearity (DNL) and integral nonlinearity (INL). They are respectively defined as $DNL[k] = \frac{W[k]-Q}{Q}$ and $INL[k] = \sum_{j=0}^{k} DNL[j]$, where $W[k]$ is the time interval of the *k-th* quantization step. Due to jitters and quantization errors, measurement results fluctuate for repetitive fixed-TI measurements. This measurement uncertainty is characterized by precision (called the RMS resolution) and calculated as the repetitive measurements' standard deviation (σ). It is defined as $\sigma^2 = \sum_{i=1}^{N} \frac{(x_i-\mu)^2}{N-1}$, where x_i is the *i-th* measurement and μ is the average value for N measurements when the TI is constant.

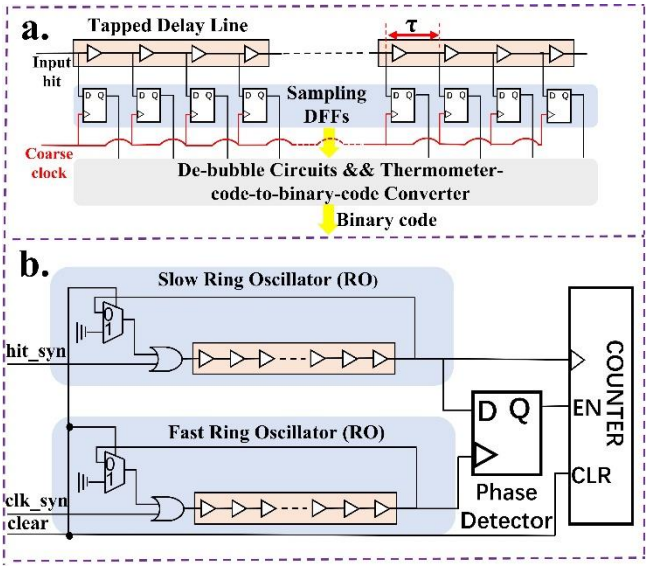

Fig.1. The block diagram of (a) a TDL-TDC and (b) a VRO-TDC.

With rapid advances in complementary metal-oxide-semiconductor (CMOS) transistor technologies, TDCs can be implemented by application-specific integrated circuits (ASICs) and field-programmable gate arrays (FPGAs). Compared with FPGA-TDCs, ASIC-TDCs can perform better due to customized placing and routing strategies [30], [31]. However, FPGA-TDCs are more prevalent in scientific experiments and prototype designs, benefiting from low development costs and short developing cycles. Tapped delay line (TDL), Vernier, and multi-phase-clock-driven counter (MPCDC) architectures are the most used architectures for fine-time measurements among FPGA-TDCs [32]. However, most MPCDC-TDCs have resolutions from 100 ps to 1000 ps [32]. Hence, high-resolution TDCs (LSB < 30 ps) are usually TDL-TDCs and Vernier ring oscillator (VRO)-TDCs. For example, Kwiatkowski *et al.* proposed a TDL-based multi-sampling wave union type B (WU-B) architecture achieving a 0.4 ps resolution with a 5.95 LSB maximum bin [33]. Wang *et al.* used a TDL-based bin-decimation architecture achieving a 6 ps resolution with a 2.5

This is a peer-reviewed, version of record of the following paper: Xie, W., Chen, H., Pei, C., Li, D., & Wang, Y. (in press). A two-stage interpolation time-to-digital converter implemented in 20 nm and 28 nm FGPAs. IEEE Transactions on Industrial Electronics.

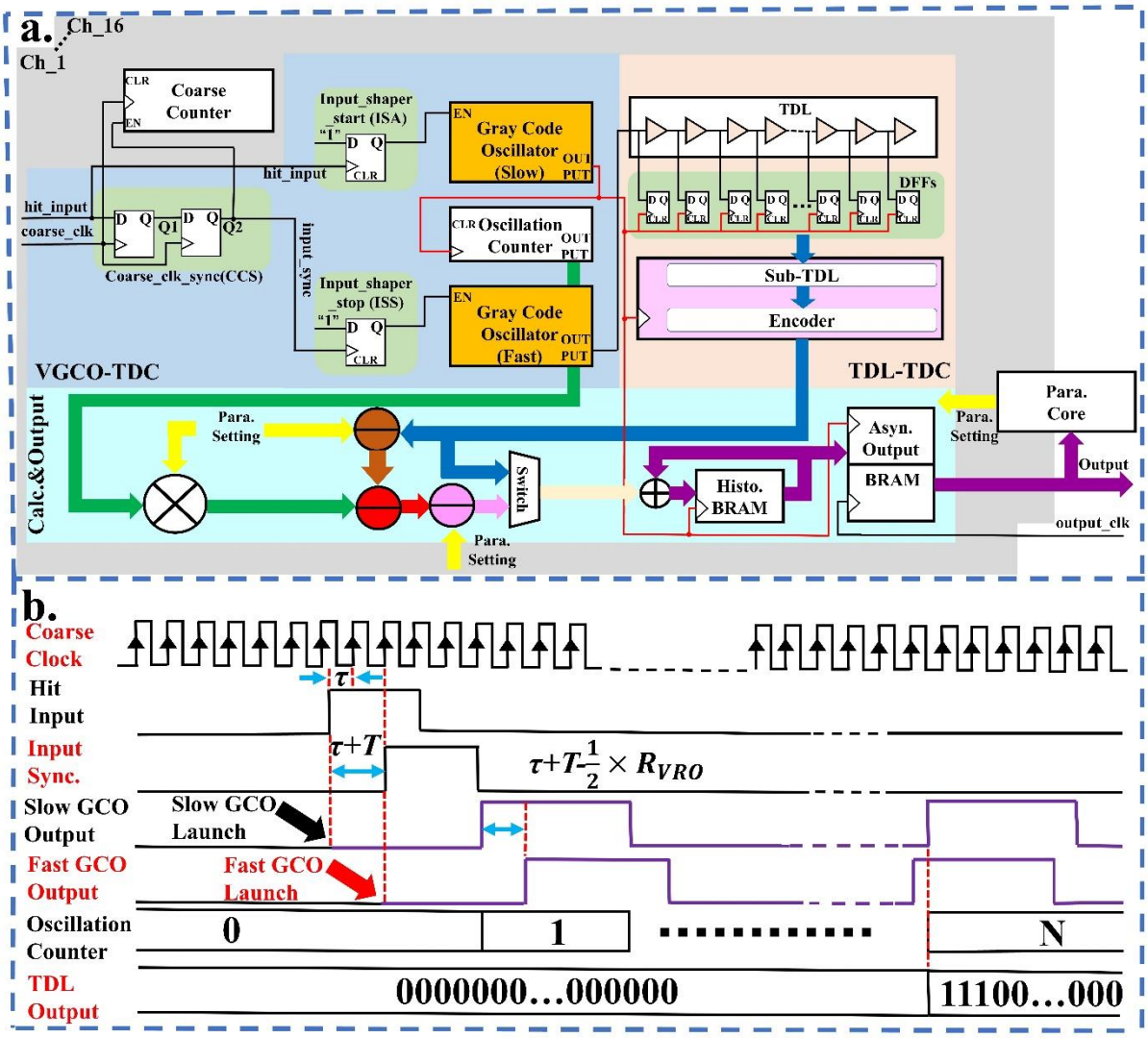

Fig.2. (a) The diagram of the proposed TDC system. (b) The timing diagram of the proposed TDC.

LSB maximum bin, and Cui *et al.* proposed a VRO-based multistep fine time measurement architecture achieving a less than 10 ps resolution with a 1.3 LSB maximum bin [34]. A TDL-TDC's resolution depends on the propagation delay of delay elements (τ in Fig. 1a). In contrast, a VRO-TDC's resolution depends on the oscillation-speed difference between fast and slow oscillators, as shown in Fig. 1b. So, there are different features between TDL-TDCs and VRO-TDCs. For TDL-TDCs, they can achieve a high throughput benefiting from pipeline sampling and encoding. However, they have higher hardware utilization due to complex de-bubble circuits and thermometer-code-to-binary-code converters. For example, the TDC in Ref. [35] achieves a 350M samples/second throughput. But 646 LUTs and 1112 D-type flip flops (DFFs) were used per channel. VRO-TDCs are more hardware-efficient compared with TDL-TDCs. However, VRO-TDCs suffer from a long dead time. For example, the TDC in Ref. [36] only consumes 104 LUTs and 319 DFFs per channel. But its dead time is around 400 ns, corresponding to 2.5M samples/second. Besides, the propagation delay of CARRY4/CARRY8 has been improved to less than 10 ps, benefiting from advances in manufacturing processes [37], [38]. This allows TDL-TDCs to deliver better resolutions. But lower propagation delay also requires a TDL having more CARRY4s/CARRY8s to cover a whole period of the coarse counting clock. So, more taps are sampled and encoded. Similarly, for VRO-TDCs, more oscillation cycles are required for a fixed TI when the resolution is improved, resulting in an increasing dead time and degraded measurement precision.

Nowadays, the multi-channel design is an increasing trend for photon-electric detectors. For example, Ref. [39] introduces a 128 × 128 single-photon avalanche diode (SPAD) array with 16×2 TDCs, and Ref. [40] presents a 16-channel SiPM with 16 TDCs. Benefiting from high hardware-utilization efficiency, VRO-TDCs are appropriate for multi-channel designs. However, suffering from a long dead time, VRO-TDCs are only suitable for applications accepting low conversion rates, such as FLIM [41]. Besides, an improved TDC's resolution is also demanded for accurate fluorescence-lifetime evaluation.

Therefore, we propose a new architecture, aiming at a shorter

delay line and less hardware resource utilization than conventional TDL-TDCs, with a better resolution and a lower dead time than conventional VRO-TDCs. The contributions of this work are:

1) We propose a new TDC architecture combing a TDL-TDC and a VRO-TDC and introduce the measurement principle of this architecture in detail.
2) Unlike the carry-chain-based ring oscillator (RO), we use LUTs to construct a Vernier gray code oscillator TDC (VGCO-TDC) to reduce carry-element utilization.
3) The TDL-TDC only needs to cover the resolution of the VGCO-TDC in our proposed architecture, reducing the length of the delay line and related hardware utilization.
4) We developed and evaluated 16-channel TDCs in 20 nm Kintex-UltraScale XCKU040 and 28 nm Virtex-7 XC7V690T FPGAs to show our methods.

This article is structured as follows: Section II describes the principle and design of the proposed TDC. Section III presents the experimental results and implementation details, Section IV compares with other designs, and Section V summarizes our TDC.

II. Principle and Design

As shown in Fig. 2a, the proposed TDC works with a coarse counter, and each fine-time interpolator consists of a VGCO-TDC, a TDL-TDC, and a calculation and output module (Calc.&Output in Fig. 2a). The VGCO-TDC is responsible for the first-stage fine-time measurement with a resolution of several hundred picoseconds. Then the overtaking residual (δ) from the VGCO-TDC is measured by the TDL-TDC with a ~10 ps resolution for the second-stage measurement. After finishing both measurements, the VGCO-TDC and TDL-TDC output measurement results from the oscillation counter and encoder, respectively. Then these two results are calculated in the Calc.&Output module for the final result. Like the conventional Nutt-method-based TDL-TDC [26], the combination of outputs from the oscillation counter (VGCO-TDC) and encoder (TDL-TDC) shown in Fig. 2a ensures that the second-stage fine-time measurement is immune to synchronization problems caused by the TDL-TDC's input and sampling clock. Similarly, the proposed two-stage interpolation TDC is also immune to these synchronization problems because it works with a coarse counter, as Fig. 2a shows. Besides, we also use block random access memories (BRAMs) for the on-chip histogram and asynchronous output (Histo. BRAM and Asyn. Output BRAM in Fig. 2a), respectively. For parameters (highlighted in yellow in Fig. 2a) input to the multiplier and subtracters, we use a state-machine-based parameter core (Para. Core in Fig. 2a) to configure channel-by-channel according to histograms stored in BRAMs.

A. Measurement Principle

When a hit comes, the input hit respectively launches the slow and fast GCOs (highlighted in orange) as shown in Fig. 2a. For launching the slow GCO, the input hit first arrives at the Input_shaper_start (ISA) and changes this module's output to "1" (high-logic level) when the input hit's rising edge occurs. Then, the ISA output keeps "1" to launch the slow GCO until the global asynchronous clear (CLR in Fig. 2a) is asserted. Simultaneously, the input hit is also transferred to the fast GCO. Differently, the input hit first reaches the Coarse_clk_sync (CCS) module and is synchronized with the coarse-counting clock (coarse_clk in Fig. 2a) after two rising edges of the coarse-counting clock. Then, the synchronized input (input_sync in Fig. 2a) launches the fast GCO, similar to the input hit launching the slow GCO. The timing diagram of the proposed TDC is shown in Fig. 2b. The resolution of the VGCO-TDC (R_{VRO} in Fig. 2b) is determined by the oscillation speed difference between two GCOs. And the output of the oscillation counter is stored when the fast GCO first overtakes the slow GCO. However, the TI between slow and fast GCOs' launch is (τ+T) rather than τ, where τ is the measured TI between the rising edges of the input hit and the subsequent coarse-counting clock, and T is the period of the coarse-counting clock. Hence, T should be subtracted from the VGCO-TDC measurement result. But an extra T between GCOs' launches is necessary. Without this, when an input hit appears close to the rising edge of the coarse clock, the launching sequence of slow and fast GCOs can disorder due to uneven timing delays of internal connections, causing VGCO-TDCs to work incorrectly.

Unlike previous VRO-TDCs using a DFF as the phase detector to detect overtaking [36], [42], we use a TDL-TDC to detect it in the proposed two-stage interpolation TDC. Besides, we also use the TDL-TDC to measure the δ at a ~10 ps resolution. For the TDL-TDC in our design, the fast GCO's output is fed into the delay line. And the slow GCO's output is used as the clock for the sampling DFFs, encoder, and so on, as shown in Fig. 2a. The sampled outputs from the TDL are "0"s (low-logic level) when the fast GCO runs behind the slow GCO. But a thermometer code ("11100…000") is output when the fast GCO first overtakes the slow GCO (shown in Fig. 2b). Simultaneously, the thermometer code is also encoded to a binary code as a measurement of δ. Hence, the measured TI is calculated as follows:

$$\tau = (N_{Osci} + \frac{1}{2}) \times R_{VRO} - T - \delta, \quad (1)$$

where N_{Osci} is the oscillation number of the slow GCO when the fast GCO first overtakes the slow GCO.

B. VGCO-TDC and TDL-TDC

Vernier-TDCs utilize the oscillation speed difference between the two oscillators to achieve fine-time measurements. Theoretically, two asynchronous clocks with different frequencies are appropriate for Vernier-TDCs. However, the oscillators in the Vernier-TDC launch independently, meaning every Vernier-TDC consumes at least two PLLs/MMCMs [43], [44], which is unaffordable. Therefore, we use GCOs here to construct VGCO-TDCs. Unlike using a GCO to directly measure a TI in Ref. [45], [46], we use two GCOs in the Vernier way (as slow and fast oscillators). The diagram of the VGCO-TDC is shown in Fig. 2a, and the working principle has also been introduced in Sec. II A. Here, we detailly present the GCO.

For a GCO, the output changes following the gray-code sequence. Hence, only one bit experiences a transition between two continuous states. Benefiting from this feature, the GCO is immune to the "race and competition" phenomenon, a common problem in traditional counters that more than one bit toggle simultaneously [47]. So GCO can be implemented by combinational logics. And we can use free-run (not driven by a

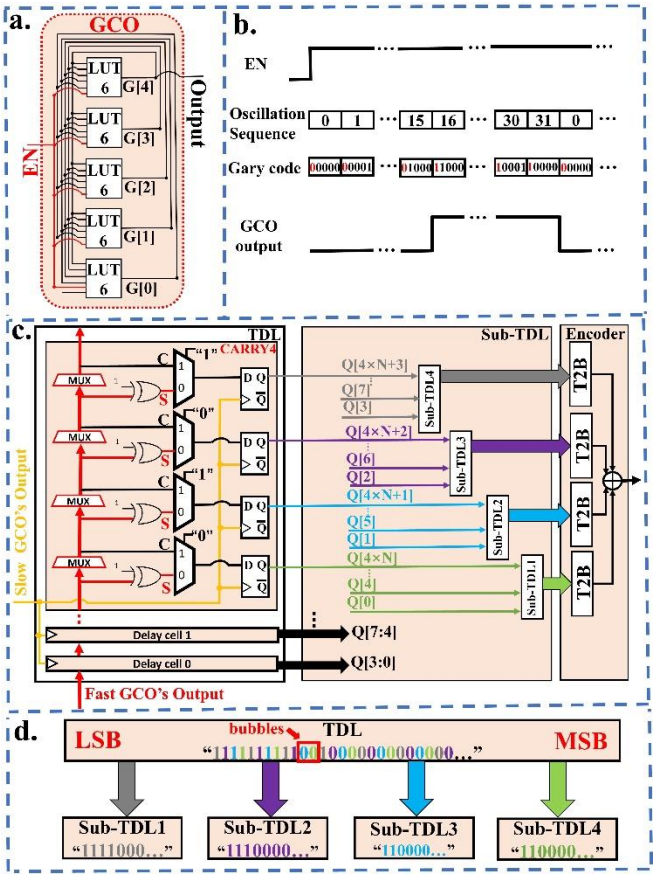

Fig.3. (a) Block diagram of the GCO. (b) Timing diagram of the GCO. (c) Block diagram of the TDL-TDC in the Virtex-7 FPGA. (d) Principle of Sub-TDL.

clock) GCOs as slow and fast oscillators in the Vernier architecture. The GCO is shown in Fig. 3a. In 7-series and more advanced Xilinx FPGAs, each LUT has up to six inputs [43], [44]. Hence, we use five 6-input LUTs to achieve a 32-state GCO. In each LUT, one of its inputs is connected to "EN" (highlighted in red in Fig. 3a) to launch and reset the GCO. The other inputs are used to get feedback from outputs (G[4:0] in Fig. 3a). We instantiate LUTs with Vivado primitives and use G[4] in Fig. 3a as the slow and fast oscillators' outputs fed into the TDL-TDC. The timing diagram of the GCO is shown in Fig. 3b.

As shown in Fig. 3c, we use CARRY4s in the Virtex-7 FPGA (CARRY8s in the Kintex-UltraScale FPGA) as delay elements to achieve the second-stage interpolation at a ~10 ps resolution. In previous TDL-TDCs [37], [38], the input hit is fed into the delay line directly. Outputs from delay elements are sampled by coarse-clock-driven DFFs, as shown in Fig. 1a. However, in the proposed TDC shown in Fig. 2a, we use the fast GCO's output as the delay line's input and use the slow GCO's output as the sampling clock, to measure the δ. Hence, the TDL in the proposed TDC only needs to cover the resolution of the VGCO-TDC, benefitting from the two-stage interpolation method. But bubbles (unexcepted "0"s between "1"s) still appear in TDL's outputs due to clock skews and uneven propagation delays. So, as shown in Fig. 3c, we use Sub-TDLs [38], [48], [49] to split TDL's outputs into 4/8 groups (4 groups in the Virtex-7 FPGA and 8 groups in the Kintex-UltraScale FPGA) in a constant interval to minimize the bubbles' impact. The principle of the

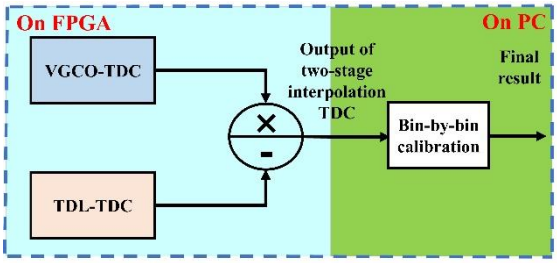

Fig.4 Data flow of the proposed TDC.

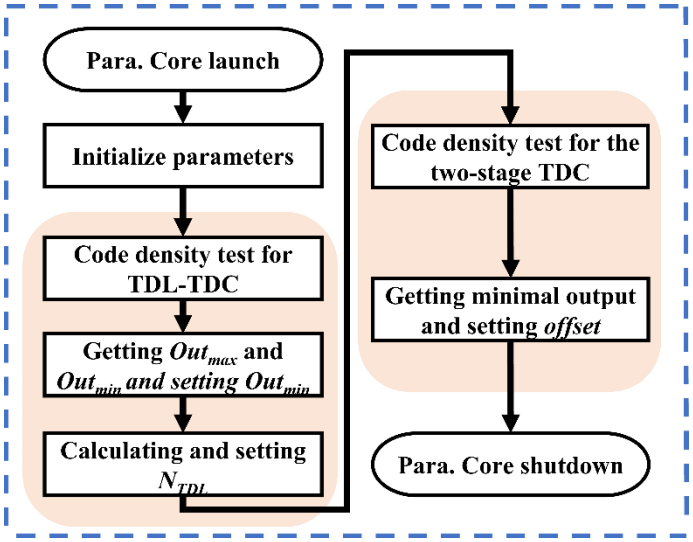

Fig.5. Workflow of the Para. Core.

Sub-TDL is shown in Fig. 3d. Then, outputs from all Sub-TDLs are encoded to binary codes, which are summed together as the result of the TDL-TDC.

C. Result Calculation and Parameter Configuration

The TI is measured, and then corresponding results are output from the VGCO-TDC and TDL-TDC. However, these two outputs still require post-processing for the final result. Hence, we design a Calc.&Output module shown in Fig. 2a for this task. The calculation is conducted according to Eq. (1). However, the TDL-TDC's output is a raw binary code rather than a calibrated timestamp. Therefore, it cannot be directly used as δ in Eq. (1). So, we use a raw binary code instead of a calibrated timestamp as the final output of the proposed TDC, considering the complexity of hardware-implemented bin-by-bin calibration [50]. And we conduct the bin-by-bin calibration in our PC as shown in Fig.4. Referring to Eq. (1), the two-stage interpolation TDC's output is also calculated as:

$$Out_{TDC} = N_{Osci.} \times N_{TDL} - Out_{TDL} - Offset, \quad (2)$$

where N_{TDL} is the number of TDL-TDC's time bins covering the VGCO-TDC's resolution, Out_{TDL} is the raw output from the TDL-TDC, and *Offset* is the offset caused by the CCS module, uneven routing delays and so on. Besides, in the designed Sub-TDL TDC, the TDC's output is valid only when all Sub-TDLs have non-zero outputs, causing the minimal valid output of TDL-TDC is more than 1. To cancel this offset, we calculate N_{TDL} and Out_{TDL} as:

$$N_{TDL} = Out_{max} - Out_{min} + 1, \quad (3)$$

and

$$Out_{TDL} = Out_{bin} - Out_{min} + 1, \quad (4)$$

where Out_{bin}, Out_{max} and Out_{min} are the raw binary code, the maximum and minimal output from the TDL-TDC.

The parameters mentioned in Eq. (2) can be calculated and configured manually. But it is time-consuming for all 16 channels. Hence, we design a Para. Core to calculate and configure parameters channel by channel. The Para. Core is implemented through a state-machine. The workflow of the Para. Core is shown in Fig. 5. It requires two code density tests (CDTs) [29], [51], CDT1 and CDT2. The CDT1 is only for TDL-TDC, with the switch in Fig. 2a selecting data from TDL-TDC (highlighted in blue) as output. While the CDT2 is for the two-stage interpolation TDC with the switch outputting data after calculation (highlighted in pink in Fig. 2a). According to the result from CDT1, the Para. Core can extract Out_{max} and Out_{min}, and calculate N_{TDL}. Then, the Para. Core configures N_{TDL} as the coefficient for the multiplier and configures Out_{min} as the subtrahend for the subtractor highlighted in brown in Fig. 2a. After configuration, CDT2 is conducted for the two-stage interpolation TDC. *Offset* in Eq. (2) can be extracted and is configured as the subtrahend for the subtractor highlighted in pink in Fig. 2a, ensuring the CDT's histogram of the proposed two-stage interpolation TDC begins from 1. CDTs' histograms for the TDL-TDC and the two-stage interpolation TDC after offset cancellation are shown in Fig. 6. As shown in Fig. 6b, the pattern (inverted from the histogram of the TDL-TDC and highlighted in blue in Fig. 6b) periodically appears in the histogram of the proposed two-stage interpolation TDC, matching the expectation of the proposed TDC.

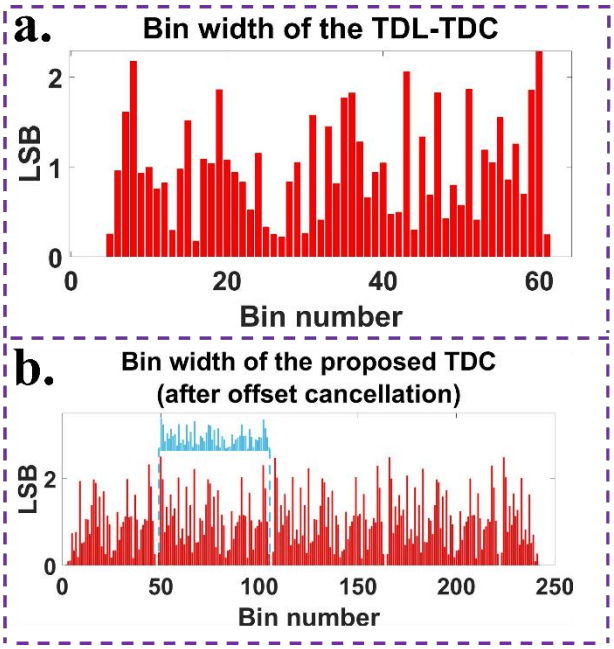

Fig.6. Histograms of time bins for (a) the TDL-TDC and (b) the proposed two-stage interpolation TDC from the Virtex-7 FPGA.

III. Experimental Results and Implementation Details

We implemented and evaluated the proposed TDC in KCU105 [52] and NetFPGA-SUME [53] evaluation boards, respectively. We used an uncorrelated 3.7777777 MHz hit from SRS-635 (Stanford Research System) as a random input for CDTs [29], [51]. While we used on-chip delay macros (IDELAY3 [43] in the Kintex-UltraScale FPGA and IDELAY2 [44] in the Virtex-7 FPGA) to generate controllable delays (relative to coarse-counting clocks) for TI tests. Coarse counting clocks are from low-jitter crystal oscillators on boards (SI-570 in KCU 105 and DSC-1103 in NetFPGA-SUME) and are configured to 400 MHz in both FPGAs. However, clocks for TDL-TDCs source from designed GCOs. Hence, we conducted timing constraints according to measured GCOs' oscillation frequencies (measured by Teledyne LeCroy 640Zi). Besides, the temperature and voltage are maintained in experiments.

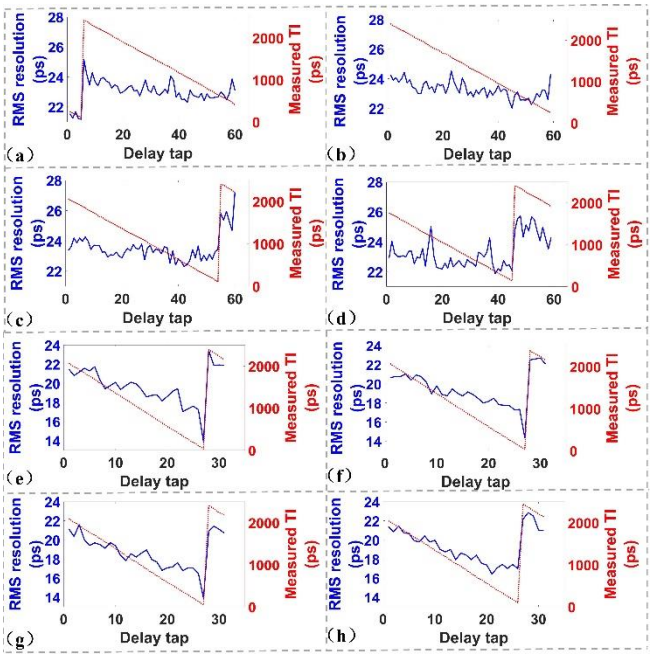

Fig.7. RMS resolutions and measured TIs of the (a) channel-1, (b) channel-5, (c) channel-9 and (d) channel-13 in the Kintex-UltraScale FPGA, and (e) channel-1, (f) channel-5, (g) channel-9 and (h) channel-13 in the Virtex-7 FPGA.

A. Resolution and Linearity

We measured oscillation periods of GCOs in both evaluation boards to calculate the resolutions of VGCO-TDCs. Besides,

TABLE I
PERIODS OF GCOS AND RESOLUTIONS OF VGCO-TDCS

	1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*
								Unit (× 10 ps)								
								UltraScale								
Peri. (slow GCO)	1092	1092	1090	1091	1101	1097	1099	1098	1107	1104	1108	1105	1100	1099	1094	1095
Peri. (fast GCO)	1010	1008	1009	1002	1030	1020	1009	1007	1032	1021	1018	1020	1024	1008	1018	1012
Reso.	82	84	81	89	81	77	90	91	75	83	90	85	76	91	76	83
								Virtex-7								
Peri. (slow GCO)	788	796	794	798	788	785	793	790	786	785	793	788	788	784	788	785
Peri. (fast GCO)	726	736	734	738	725	736	730	732	731	725	723	731	734	738	740	737
Reso.	62	60	60	60	63	49	63	58	55	60	80	57	54	46	48	48

TABLE II
PERFORMANCE OF THE PROPOSED TWO-STAGE INTERPOLATION TDC

	1	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*	*10*	*11*	*12*	*13*	*14*	*15*	*16*	*Ave.*
UltraScale																	
Reso. (ps)	4.54	4.51	4.50	4.50	4.62	4.54	4.63	4.52	4.65	4.55	4.55	4.63	4.53	4.63	4.66	4.55	4.57
$DNL_{pk\text{-}pk}$ (LSB)	4.29	5.32	4.14	4.27	3.91	3.86	4.25	5.30	4.22	5.72	3.80	4.35	4.58	4.12	3.77	3.79	4.36
$INL_{pk\text{-}pk}$ (LSB)	18.23	21.61	18.24	19.64	20.32	19.12	18.05	18.14	15.95	23.66	16.91	16.34	19.29	16.11	12.88	17.70	18.26
ω_{eq} (ps)	9.95	10.68	9.16	9.66	9.72	9.86	9.80	10.65	9.82	10.44	9.63	9.82	9.32	10.23	10.17	9.91	9.93
σ_{valid} (ps)	23.03	23.11	22.71	22.94	23.28	22.92	22.91	22.57	23.55	22.89	22.31	22.74	23.32	22.20	22.75	22.80	22.88
Virtex-7																	
Reso. (ps)	10.25	10.25	10.12	10.20	10.00	9.96	9.73	10.12	9.65	10.20	10.29	9.84	10.16	10.08	10.25	9.68	10.05
$DNL_{pk\text{-}pk}$ (LSB)	2.46	4.29	3.29	2.56	2.24	3.67	2.60	2.97	2.36	4.22	2.29	2.25	2.43	3.01	2.67	2.31	2.85
$INL_{pk\text{-}pk}$ (LSB)	12.42	15.25	14.10	12.90	16.71	14.42	14.21	16.79	19.71	11.04	9.46	14.00	12.24	13.56	11.07	9.91	13.61
ω_{eq} (ps)	15.39	19.54	16.76	15.69	14.98	17.19	15.19	16.27	14.69	19.28	14.62	14.62	15.05	16.22	15.72	14.26	15.97
σ_{valid} (ps)	19.76	20.58	20.48	20.69	19.51	21.63	19.56	20.29	18.80	19.41	18.93	19.30	19.43	19.72	19.46	19.34	19.81

the resolutions and linearities of two-stage interpolation TDCs were also evaluated. The linearity is characterized by DNL and INL introduced in Sec. I. Moreover, the overall impact of the nonlinearity on measurements is also estimated by the equivalent resolution (ω_{eq}) [54]. It is defined as $\omega_{eq} = \sqrt{\sum_{i=1}^{n} \frac{W[i]^3}{W_{total}}}$, where $W_{total} = \sum W[i]$.

The oscillation periods of GCOs and resolutions of VGCO-TDCs are summarized in TABLE I. As TABLE I shows, the oscillation periods are designed from 7 ns to 11 ns for TDL-TDCs' fast timing-closure in the implemented FPGAs. The resolutions of Kintex-UltraScale-implemented VGCO-TDCs range between 750 ps and 910 ps with an average resolution of 831 ps. Differently, the resolutions of Virtex-7-implemented VGCO-TDCs range between 460 ps and 800 ps with an average resolution of 579 ps. GCOs in the Virtex-7 FGPA have faster oscillation frequencies than GCOs in the Kintex-UltraScale FPGA. So, the VGCO-TDC in the Virtex-7 FPGA can achieve a similar dead time (for a 5-ns maximum measurement range, τ+T) even with a finer resolution. The resolutions and linearities of two-stage TDCs implemented in both evaluation boards are also summarized in TABLE II. For TDCs in the Kintex-UltraScale FPGA, resolutions fluctuate between 4.50 ps and 4.66 ps with an average resolution of 4.57 ps, showing good uniformity between channels. And the average $DNL_{pk\text{-}pk}$ and $INL_{pk\text{-}pk}$ are respectively 4.36 LSB and 18.26 LSB, with a 5.72 LSB maximum $DNL_{pk\text{-}pk}$ and a 23.66 LSB maximum $INL_{pk\text{-}pk}$. Besides, the $\boldsymbol{\omega_{eq}}$ is from 9.16 ps to 10.68 ps with an average $\boldsymbol{\omega_{eq}}$ of 9.93 ps, simultaneously determined by the resolution and linearity. For TDCs in the Virtex-7 FPGA, the resolutions are from 9.65 ps to 10.29 ps, with an average resolution of 10.05 ps. And the average $DNL_{pk\text{-}pk}$ and $INL_{pk\text{-}pk}$ are respectively 2.85 LSB and 13.61 LSB, with a 4.29 LSB maximum $DNL_{pk\text{-}pk}$ and a 19.71 LSB maximum $INL_{pk\text{-}pk}$. Moreover, the $\boldsymbol{\omega_{eq}}$ fluctuates between 14.26 ps and 19.54 ps with an average value of 15.97 ps. Compared with TDCs in the Viretex-7 FPGA, TDCs in the Kintex-UltraScale FPGA has an average resolution enhanced by more than 2-fold, from 10.05 ps to 4.57 ps. However, the $\boldsymbol{\omega_{eq}}$ only improves by 1.6-fold (from 15.97 ps to 9.93 ps), suffering from worse linearity.

B. Time Interval Test

We use the standard deviation introduced in Section I to evaluate measurement uncertainty induced by quantization errors and jitters. To avoid jitters introduced by the input signal, we use on-chip programmable delay macros (IDELAY3 [43] in the Kintex-UltraScale FPGA and IDELAY2 [44] in the Virtex-7 FPGA) to delay a 5 MHz clock (synchronized with the coarse-counting clock), and use the delayed clock as the input for TI tests. Besides, we also use bin-by-bin calibration [50] to minimize the impacts of quantization errors and INL on measurements. It is calculated as:

$$t_k = \frac{W[k]}{2} + \sum_{j=0}^{k-1} W[j], \quad (5)$$

where t_k is the calibrated timestamp corresponding to the center of the k-th time bin.

The TDCs' RMS resolutions of both FPGAs are shown in Fig. 7. We use 60 delay taps to cover a period of the coarse-counting clock (2.5 ns @ 400MHz) in the Kintex-UltraScale FPGA. However, only 32 delay taps are required to cover the same period in the Virtex-7 FPGA, due to a worse resolution of IDELAY2 compared to IDELAY3. For TDCs in both FPGAs, most measured groups containing different TIs (highlighted in red in Fig. 7) have a sharp change caused by spanning coarse-counting clocks' cycles. However, the delay-tap numbers corresponding to sharp changes are varied due to different path delays of the input signal. Different placement and routing strategies cause these various path delays. In general, RMS resolutions have a deteriorating trend with increasing measured TIs. Jitters' accumulation from VGCO-TDCs causes this phenomenon. As Fig. 2a shows, the slow GCO's output drives the oscillation counter. And more oscillation cycles of GCOs are required for longer TIs, resulting in more accumulation of GCOs' jitters. Then the accumulated jitters from VGCO-TDCs deteriorate RMS resolutions of two-stage interpolation TDCs. Besides, the accumulated jitters of the VGCO-TDC are also influenced by the period of the coarse-counting clock rather than the stability of GCOs only. Because the period of the coarse-counting clock determines the maximum measured TI of the VGCO-TDC. Simultaneously, it is worth noting that the trend of the proposed TDC's RMS resolution slightly differs from that of the measured TI, especially in the Kintex-

UltraScale FPGA. There are two reasons for this phenomenon. Firstly, measurement uncertainty is not sourced from GCOs only. Measurement uncertainty from the TDL-TDC, unrelated to the measured TI, also contributes to RMS resolutions. Secondly, for the same measured TI, the GCOs in the Virtex-7 FPGA oscillate more than GCOs in the Kintex-UltraScale FPGA, due to better VGCO-TDCs' resolutions. Therefore, the trend of accumulated jitters is more prominent in the Virtex-7 FPGA.

Figure 7 shows RMS resolutions for different intervals (less than one coarse-clock period). However, we must also characterize the RMS resolution for the whole coarse-clock period. Hence, the valid RMS resolution (σ_{valid}) [55] is used, defined as $\sigma_{valid}^2 = \sum_1^H \frac{\sigma_i^2}{H}$, where σ_i is the standard deviation of measurements for the i-th fixed TI and H is the number of different TIs. The valid RMS resolution for each channel in both FPGAs is summarized in TABLE II.

C. Hardware resource utilization and constraint for design

We implemented the proposed TDCs in both FPGAs. The hardware resource utilization of both FPGAs is summarized in TABLE III. For TDCs in the Kintex-UltraScale FPGA, each channel consumes 402 LUTs and 544 DFFs. Besides, each channel also uses 1.5 BRAMs for Histo. BRAM and 1.5 BRAMs for Asyn. Output BRAM. Moreover, 29 CARRY8s are needed to construct TDL, and 23 CARRY8s for calculation, including accumulation, multiplication and subtraction. In addition to the hardware utilization mentioned above, 614 LUTs and 419 DFFs are also used for the Para. Core which calculates and configures parameters for all 16-channel TDCs in the Kintex-UltraScale FPGA. However, the hardware utilization is less in the Virtex-7 FPGA due to VGCO-TDCs' better resolutions and worse TDL propagation delays. For TDCs in the Virtex-7 FPGA, each channel consumes 257 LUTs and 360 DFFs. Besides, each channel also uses 1 BRAM for Histo. BRAM and 1 BRAM for Asyn. Output BRAM. And 20 CARRY4s are used for TDLs, and 38 CARRY4s as arithmetic units. Unlike the Para. Core in the Kintex-UltraScale FPGA, the Para. Core in the Virtex-7 FPGA only consumes 574 LUTs and 396 DFFs, due to parameters' shorter bin-width. The hardware resource utilization indicates the proposed design is more hardware-efficient than conventional TDL-TDCs [38], and has similar hardware utilization compared with the VRO-TDC presented in Ref. [42] (a comparison is shown in TABLE IV).

The TDC's implementation layouts in the Kintex-UltraScale FPGA are shown in Fig. 8a. We placed the VGCO-TDC close to the corresponding TDL-TDC to minimize jitters and skews induced by inner connections. Besides, as shown in Fig. 8b and 8c, the GCO is manually routed (manually constrained routes are highlighted as yellow dotted lines in Fig. 8b) and placed (LUTs are highlighted in red in Fig. 8c) to ensure the uniformity between channels. We used the Tcl command "set_property BEL" and "set_property LOC" to place LUTs, and used "set_property FIXED_ROUTE" to perform routing manually. Moreover, timing constraints differ from previous TDL-TDCs since the designed TDL-TDCs' sampling and encoding clocks are from GCOs rather than MMCMs [43], [44]. Hence, we use "create clock -period" to claim the GCO's output as a clock and set the period for it. Meanwhile, we also need to use "set_clock_groups -asynchronous" to set asynchronous-clock groups to avoid unnecessary timing checks between different clock regions.

TABLE III
HARDWARE RESOURCE UTILIZATION

		LUT	*DFF*	*CARRY*[1]	*CLB/Slice*[2]
UltraScale	Available	242400	484800	30300	30300
	1-ch	402	544	52	155
	16-ch	6431	8704	832	2495
	Para. Core	614	419	1	165
Virtex-7	Available	433200	866400	108300	108300
	1-ch	257	360	58	177
	16-ch	4113	5760	928	2695
	Para. Core	574	396	5	248

[1]CARRY8s in UltraScale FPGA and CARRY4s in Virtex-7FPGA. [2]CLB in UltraScale FPGA and slice in Virtex-7 FPGA.

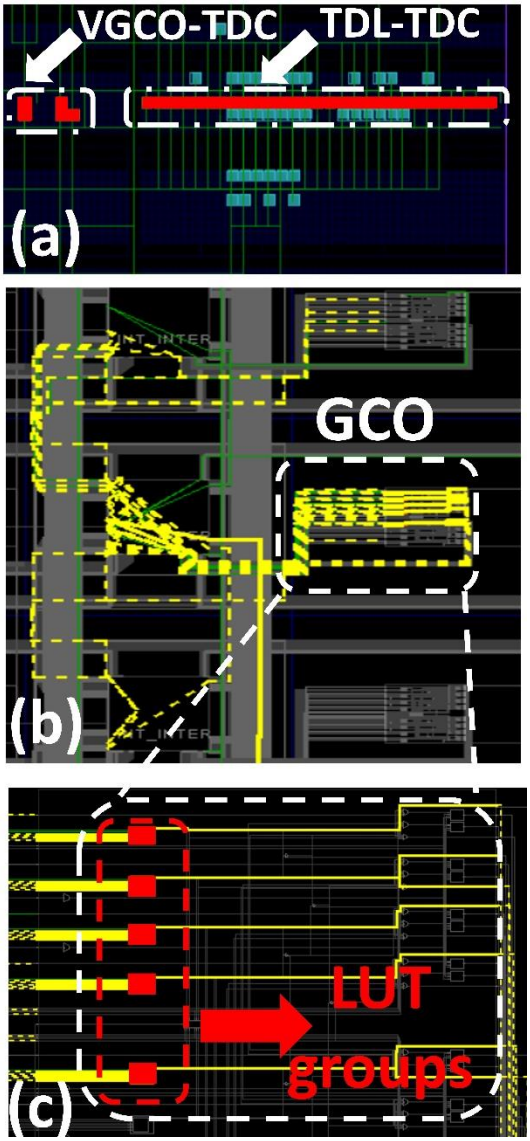

Fig.8. (a) Implementation layouts of the two-stage interpolation TDC, (b) routing details of the GCO, and (c) implementation layouts of the GCO in the UltraScale-Kintex FPGA.

IV. Comparison and Discussion

Table IV summarizes recently published TDL-TDCs and VRO-TDCs. We use the maximum oscillation number and maximum oscillation period for the proposed TDC to evaluate the dead time for all 16 channels. Hence, the dead time of the design is calculated as follows:

$$T_{Dead} = (N_{Osci.}^{max} + T_{code} + T_{calc.} + T_{his.} + T_{reset}) \times P_{max}, \quad (6)$$

where $N_{Osci.}^{Max}$ is the maximum oscillation number of the slow GCO for the 5-ns maximum measurement range, T_{code}, $T_{cacl.}$, $T_{his.}$, and T_{reset} are required clock cycles for the encoder, result calculation, histogram and resetting the TDC (they are 2, 3,1 and 1 clocks cycles, respectively), and P_{max} is the maximum oscillation period for the slow GCOs.

As shown in TABLE IV, the TDL-TDC is the mainstream design. And the VRO-TDC is also well-developed. However, in this work, we first proposed the two-stage interpolation architecture combing a VGCO-TDC and a TDL-TDC, achieving a better dead time and a finer resolution than conventional VRO-TDCs and better hardware utilization than conventional TDL-TDCs.

TDL-TDCs normally have a one-cycle or two-cycle dead time, benefiting from pipeline sampling and encoding. And the VRO-TDCs' dead time is much longer due to the measuring principle (the measurement is conducted by the fast oscillator "chasing" the slow oscillator). But, benefiting from the two-stage interpolation architecture, the oscillation number in our design is reduced dramatically even with a finer resolution, further reducing the dead time. For example, TDCs' dead time in Ref. [36] and [42] is 400 ns and 602 ns. However, the dead time of our design is 155 ns (in the Kitex-UltraScale FPGA) and 144 ns (in the Virtex-7 FPGA), respectively.

Moreover, the reduced oscillation number also benefits precision since fewer jitters are accumulated. For example, our designs have similar precision compared to those in Ref. [36] and [42], although our designs have much better resolutions. Simultaneously, the proposed TDC has a similar hardware utilization compared to the Ref. [42] design. But our method is less hardware-efficient than the design in Ref. [36] due to the on-chip calculation and histogram.

TDL-TDCs in Ref. [38] and Ref. [58] have similar resolutions compared with the proposed TDCs. However, the TDL-TDC in the proposed two-stage interpolation TDC only needs to cover the resolution of the VGRO-TDC, indicating the proposed TDC is more hardware-efficient than conventional TDL-TDCs. The designs in Ref. [56] and Ref. [59] have similar hardware utilization compared with ours. The TDL-TDC in Ref. [56] requires 228 LUTs and 678 DFFs, similar to the design in the Kintex-UltraScale FPGA. However, our design has a much finer resolution (improved from 20 ps to 5 ps). Compared with the design in Ref. [59], the design in the Virtex-7 FPGA has similar hardware utilization. But our design performs worse resolution and precision Here, the advantage of our method is fewer CARRY4s to construct the TDL and lower-frequency

TABLE IV
COMPARISON OF RECENTLY PUBLISHED TDL-TDCS AND VRO-TDCS

Ref-year	*Methods*	*Devi. Proc. (nm)*	*LSB (ps)*	*ω_{eq} (ps)*	*Prec. (ps)*	*DNL (LSB)*	*INL (LSB)*	*Dead Time (ns)*	*LUT*	*DFF*	*CARRY*	*CLB /Slice*
TDL-TDCs												
[38]-19	Sub-TDL, Bin-width compensation and calibration.	20	5.02	5.03	7.81[1]	[-0.12,0.11]	[-0.18,0.46]	NS[2]	703	1195	80[3]	NS[2]
		28	10.54	10.55	14.59[1]	[-0.05,0.08]	[-0.09,0.11]	NS[2]	1145	1916	NS[2]	712[4]
[56]-22	Dual-mode encoder.	28	22.1	NS[2]	22.35[1]	[-0.71,1.05]	[0.85,0.86]	4	228	678	48[5]	NS[2]
[57]-22	Wave union A, DSP delay line.	28	NS[2] NS[2]	NS[2] NS[2]	11.49[1] 13.60[1]	NS[2] NS[2]	NS[2] NS[2]	NS[2] NS[2]	NS[2] NS[2]	NS[2] NS[2]	NS[2] NS[2]	10%[6] 3.78%[6]
[58]-22	Wave union A, bin merging.	28	10	NS[2]	17	[-0.13,0.15]	[-2.26,3.54]	NS[2]	1136[7]	2716[7]	NS[2]	NS[2]
[26]-23	Wave union A, dual-sampling, bidirectional encoder	16	0.46	1.81	<9	[-0.99,6.42]	[-8.79,51.56]	NS[2]	11773	13547	234[3]	NS[2]
[33]-23	Multi-sampling wave union B.	28	0.4	0.55	<5.2	[-0.97,5.95]	[-8.02,219.30]	NS[2]	2840	1165	NS[2]	953[4]
[59]-23	Folding-TDC.	28	4.4 6.5	NS[2] NS[2]	4.6 6.4	NS[2] NS[2]	NS[2] NS[2]	4.4 4.4	339 231	740 352	NS[2] NS[2]	NS[2] NS[2]
VRO-TDCs												
[36]-17	Period difference recording.	65	[23,37]	NS[2]	[32,39]	[-0.4,0.4]	[-0.7,0.7]	400	104	319	NS[2]	NS[2]
[42]-20	Bidirectional-Operating.	65	24.5	NS[2]	28	[-0.20,0.25]	[0.03,0.82]	602	172	986	NS[2]	NS[2]
Other-TDCs												
[60]-23	SSP-SCFC-TDC	28	625	NS[2]	180[1]	0.05[8]	0.05[8]	NS[2]	212	333	64	84[4]
			317	NS[2]	92.3[1]	0.26[8]	0.20[8]	NS[2]	238	424	64	108[4]
			156	NS[2]	68.3[1]	0.23[8]	0.26[8]	NS[2]	295	431	64	110[4]
This work	**Two-stage interpolation.**	**20**	**4.57**	**9.93**	**22.88[1,2]**	**[-1,3.14] 4.36[9]**	**[-8.81,9.44] 18.26[10]**	**155**	**402 440[11]**	**544 570[11]**	**52[3]**	**155[12]**
		28	**10.05**	**15.97**	**19.81[1,2]**	**[-1,1.46] 2.85[9]**	**[-6.01,6.40] 13.61[10]**	**144**	**257 293[11]**	**360 385[11]**	**58[5]**	**177[4]**

[1] Sigle shot precision; [2] NS=not specified; [3] CARRY8; [4] Slice; [5] CARRY4; [6] Percentage of used DSPs in a Artix-7 200T FPGA; [7] Averaged value for 19 channels; [8] $DNL_{pk\text{-}pk}$/$INL_{pk\text{-}pk}$; [9] Average $DNL_{pk\text{-}pk}$ for 16 channels; [10] Average $INL_{pk\text{-}pk}$ for 16 channels; [11] Each channel's average hardware utilization with the Para. Core; [12] CLB.

clock required for TDL-TDC's sampling and encoding. In Ref. [59], over 200 taps (50 CARRY4s) cover the 554 MHz sampling clock. However, in our design, only 80 taps (20 CARRY4s) are used to construct the TDL to cover the resolution of the VGRO-TDC rather than the period of the coarse clock. Compared with conventional TDL-TDCs, this architecture allows TDL's length unrelated to the coarse-counting clock, further reducing the difficulty of timing closure (a high-frequency TDL-TDC sampling clock is preferred to reduce the length of the TDL in conventional TDL-TDCs). Besides, although 257 LUTs and 360 DFFs are used per channel for the TDC in the Virtex-7 FPGA (402 LUTs and 544 DFFs are used for the TDC in the Kintex-UltraScale FPGA), only 86 LUTs and 116 DFFs are used for the VGCO-TDC and TDL-TDC (only 213 LUTs and 284 DFFs are used for the VGCO-TDC and TDL-TDC in the Kintex-UltraScale FPGA), indicating our design can be more compact.

V. Conclusion

In this work, we use GCOs to replace CARRY4s/CARRY8s to build oscillators for Vernier-TDCs and propose the two-stage interpolation architecture. With the new architecture, the TDL-TDC in our design only needs to cover the resolution of the VGCO-TDC, reducing the hardware utilization of the designed TDC. Besides, the length of the TDL is not related to the frequency of the TDL-TDC's clock, reducing the difficulty of timing closure (a high-frequency TDL-TDC clock is preferred to reduce the length of the TDL). Compared with previous VRO-TDCs, the proposed TDCs improve the dead time and precision even with a finer resolution by reducing oscillation numbers.

We implemented the proposed 16-channel TDC in Kintex-UltraScale and Virtex-7 FPGAs to evaluate our design. Experimental results indicate that the proposed TDC is hardware-efficient compared with VRO-TDCs and TDL-TDCs and has competitive performances compared with VRO-TDCs. It is appropriate for multi-channel and low-conversion-rate applications such as FLIM although the precision needs to be further improved compared with TDL-TDCs. Besides, the multiphase clock method [61] for the VGCO-TDC and the WU method [50] for TDL-TDC can be implemented in future work to improve the precision.

VI. Acknowledgements

This work has been funded by the EPSRC (EP/T00097X/1): the Quantum Technology Hub in Quantum Imaging (QuantiC), Innovate UK HYDRI (10005391), and the University of Strathclyde.

Reference

[1] S. Conforti Di Lorenzo *et al.*, 'HKROC: an integrated front-end ASIC to readout photomultiplier tubes for the Hyper-Kamiokande experiment', *J. Inst.*, vol. 18, no. 01, p. C01035, Jan. 2023.

[2] C. Liu *et al.*, 'SECALROC2: A Low-Noise, High-Speed, and Full Digital Outputs Front-End ASIC for STCF Electromagnetic Calorimeter With APD Detectors', *IEEE Trans. Nucl. Sci.*, vol. 70, no. 2, pp. 139–149, Feb. 2023.

[3] J. Lu *et al.*, 'Readout Electronics Prototype of TOF Detectors in CEE of HIRFL', *IEEE Trans. Nucl. Sci.*, vol. 68, no. 8, pp. 1976–1983, Aug. 2021.

[4] R. Wang *et al.*, 'Picosecond Timing Electronics for a DIRC-Like Detector at the Super Tau-Charm Facility', *IEEE Trans. Nucl. Sci.*, vol. 69, no. 11, pp. 2262–2270, Nov. 2022.

[5] W. Zhang *et al.*, 'A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade', *IEEE Trans. Nucl. Sci.*, vol. 68, no. 8, pp. 1984–1992, Aug. 2021.

[6] S. Pourashraf *et al.*, 'Investigation of Electronic Signal Processing Chains for a Prototype TOF-PET System With 100-ps Coincidence Time Resolution', *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 6, no. 6, pp. 690–696, Jul. 2022.

[7] X. Kong, Y. Wang, L. Wang, Y. Xiao, and J. Kuang, 'An FPGA-Based Fast Linear Discharge Readout Scheme Enabling Simultaneous Time and Energy Measurements for TOF-PET Detectors', *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 4, no. 1, pp. 30–36, Jan. 2020.

[8] E. Venialgo *et al.*, 'Toward a Full-Flexible and Fast-Prototyping TOF-PET Block Detector Based on TDC-on-FPGA', *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 3, no. 5, pp. 538–548, Sep. 2019.

[9] J. Y. Won and J. S. Lee, 'Highly Integrated FPGA-Only Signal Digitization Method Using Single-Ended Memory Interface Input Receivers for Time-of-Flight PET Detectors', *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 6, pp. 1401–1409, Dec. 2018.

[10] T. Talala, E. Parkkinen, and I. Nissinen, 'CMOS SPAD Line Sensor With Fine-Tunable Parallel Connected Time-to-Digital Converters for Raman Spectroscopy', *IEEE J. Solid-State Circuits*, pp. 1–12, 2022.

[11] T. Talala *et al.*, 'Time-Resolved Raman Spectrometer With High Fluorescence Rejection Based on a CMOS SPAD Line Sensor and a 573-nm Pulsed Laser', *IEEE Trans. Instrum. Meas.*, vol. 70, pp. 1–10, 2021.

[12] R. K. Henderson *et al.*, 'A 192×128 Time Correlated SPAD Image Sensor in 40-nm CMOS Technology', *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 1907–1916, Jul. 2019.

[13] A. T. Erdogan *et al.*, 'A CMOS SPAD Line Sensor With Per-Pixel Histogramming TDC for Time-Resolved Multispectral Imaging', *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1705–1719, Jun. 2019.

[14] A. C. Ulku *et al.*, 'A 512 × 512 SPAD Image Sensor With Integrated Gating for Widefield FLIM', *IEEE J. Select. Topics Quantum Electron.*, vol. 25, no. 1, pp. 1–12, Jan. 2019.

[15] S. Moini *et al.*, 'Voltage Sensor Implementations for Remote Power Attacks on FPGAs', *ACM Trans. Reconfigurable Technol. Syst.*, vol. 16, no. 1, pp. 1–21, Mar. 2023.

[16] H. Ma *et al.*, 'On-Chip Trust Evaluation Utilizing TDC-Based Parameter-Adjustable Security Primitive', *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 40, no. 10, pp. 1985–1994, Oct. 2021.

[17] D. Li, J. Hu, R. Ma, X. Wang, Y. Liu, and Z. Zhu, 'SPAD-Based LiDAR With Real-Time Accuracy Calibration and Laser Power Regulation', *IEEE Trans. Circuits Syst. II*, vol. 70, no. 2, pp. 431–435, Feb. 2023.

[18] J. Hu, X. Wang, D. Li, Y. Liu, R. Ma, and Z. Zhu, 'A 50-ps Gated VCRO-Based TDC With Compact Phase Interpolators for Flash LiDAR', *IEEE Trans. Circuits Syst. I*, vol. 69, no. 12, pp. 5096–5107, Dec. 2022.
[19] S. Park *et al.*, 'An 80 × 60 Flash LiDAR Sensor With In-Pixel Delta-Intensity Quaternary Search Histogramming TDC', *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3200–3211, Nov. 2022.
[20] C. Zhang *et al.*, 'A 240 × 160 3D-Stacked SPAD dToF Image Sensor With Rolling Shutter and In-Pixel Histogram for Mobile Devices', *IEEE Open J. Solid-State Circuits Soc.*, vol. 2, pp. 3–11, 2022.
[21] Y. Zhang and Z. Zhu, 'Recent Advances and Trends in Voltage-Time Domain Hybrid ADCs', *IEEE Trans. Circuits Syst. II*, vol. 69, no. 6, pp. 2575–2580, Jun. 2022.
[22] Y. Lyu and F. Tavernier, 'A 4-GS/s 39.9-dB SNDR 11.7-mW Hybrid Voltage-Time Two-Step ADC With Feedforward Ring Oscillator-Based TDCs', *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1807–1818, Jul. 2020.
[23] K. Ohhata, 'A 2.3-mW, 1-GHz, 8-Bit Fully Time-Based Two-Step ADC Using a High-Linearity Dynamic VTC', *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 2038–2048, Jul. 2019.
[24] B. Xu, Y. Zhou, and Y. Chiu, 'A 23-mW 24-GS/s 6-bit Voltage-Time Hybrid Time-Interleaved ADC in 28-nm CMOS', *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1091–1100, Apr. 2017.
[25] R. Nutt, 'Digital Time Intervalometer', *Review of Scientific Instruments*, vol. 39, no. 9, pp. 1342–1345, Sep. 1968.
[26] Y. Wang, W. Xie, H. Chen, and D. Day-Uei Li, 'High-resolution time-to-digital converters (TDCs) with a bidirectional encoder', *Measurement*, vol. 206, p. 112258, Jan. 2023.
[27] Z. Wang, Y. Jin, and B. Zhou, 'A Novel 12-Bit 0.6-mW Two-Step Coarse-Fine Time-to-Digital Converter', *IEEE Trans. Circuits Syst. II*, vol. 69, no. 12, pp. 4654–4658, Dec. 2022.
[28] Y. Hua and D. Chitnis, 'A Highly Linear and Flexible FPGA-Based Time-to-Digital Converter', *IEEE Trans. Ind. Electron.*, vol. 69, no. 12, pp. 13744–13753, Dec. 2022.
[29] J. Kalisz, 'Review of methods for time interval measurements with picosecond resolution', *Metrologia*, vol. 41, no. 1, pp. 17–32, Feb. 2004.
[30] J. Liu, M. Hassanpourghadi, and M. S.-W. Chen, 'A 10-GS/s 8-bit 2850-μm ^{2} Two-Step Time-Domain ADC With Speed and Efficiency Enhanced by the Delay-Tracking Pipelined-SAR TDC', *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3757–3767, Dec. 2022.
[31] H. Wang, F. F. Dai, Z. Su, and Y. Wang, 'Sub-Sampling Direct RF-to-Digital Converter With 1024-APSK Modulation for High Throughput Polar Receiver', *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1064–1076, Apr. 2020.
[32] R. Machado, J. Cabral, and F. S. Alves, 'Recent Developments and Challenges in FPGA-Based Time-to-Digital Converters', *IEEE Trans. Instrum. Meas.*, vol. 68, no. 11, pp. 4205–4221, Nov. 2019.
[33] P. Kwiatkowski, D. Sondej, and R. Szplet, 'Subpicosecond resolution time interval counter with multisampling wave union type B TDCs in 28 nm FPGA device', *Measurement*, vol. 209, p. 112510, Mar. 2023.
[34] K. Cui, J. Yu, J. Zou, and X. Li, 'A High-Resolution TDC Design Based on Multistep Fine Time Measurement by Utilizing Delay-Adjustable Looped Carry Chains on FPGAs', *IEEE Trans. Instrum. Meas.*, vol. 72, pp. 1–10, 2023.
[35] Z. Song, Y. Wang, and J. Kuang, 'Implementation of 5.3 ps RMS precision and 350 M samples/second throughput time-to-digital converters with event sampling architecture in a Kintex-7 FPGA', *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 944, p. 162584, Nov. 2019.
[36] K. Cui, X. Li, Z. Liu, and R. Zhu, 'Toward Implementing Multichannels, Ring-Oscillator-Based, Vernier Time-to-Digital Converter in FPGAs: Key Design Points and Construction Method', *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 1, no. 5, pp. 391–399, Sep. 2017.
[37] W. Xie, H. Chen, and D. D.-U. Li, 'Efficient Time-to-Digital Converters in 20 nm FPGAs With Wave Union Methods', *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 1021–1031, Jan. 2022.
[38] H. Chen and D. D.-U. Li, 'Multichannel, Low Nonlinearity Time-to-Digital Converters Based on 20 and 28 nm FPGAs', *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 3265–3274, Apr. 2019.
[39] S. Zhuo *et al.*, 'Solid-State dToF LiDAR System Using an Eight-Channel Addressable, 20-W/Ch Transmitter, and a 128 × 128 SPAD Receiver With SNR-Based Pixel Binning and Resolution Upscaling', *IEEE J. Solid-State Circuits*, vol. 58, no. 3, pp. 757–770, Mar. 2023.
[40] M. Liu *et al.*, 'A 16-Channel Analog CMOS SiPM With On-Chip Front-End for D-ToF LiDAR', *IEEE Trans. Circuits Syst. I*, vol. 69, no. 6, pp. 2376–2386, Jun. 2022.
[41] R. Scott, W. Jiang, and M. J. Deen, 'CMOS Time-to-Digital Converters for Biomedical Imaging Applications', *IEEE Rev. Biomed. Eng.*, vol. 16, pp. 627–652, 2023.
[42] K. Cui and X. Li, 'A High-Linearity Vernier Time-to-Digital Converter on FPGAs With Improved Resolution Using Bidirectional-Operating Vernier Delay Lines', *IEEE Trans. Instrum. Meas.*, vol. 69, no. 8, pp. 5941–5949, Aug. 2020.
[43] Xilinx, 'UltraScale Architecture Libraries Guide (UG974)', 2018, Accessed: Mar. 07, 2023. [Online]. Available: https://docs.xilinx.com/r/en-US/ug974-vivado-ultrascale-libraries/Introduction
[44] Xilinx, 'Vivado Design Suite 7 Series FPGA Libraries Guide', 2012, Accessed: Mar. 07, 2023. [Online]. Available: https://docs.xilinx.com/v/u/2018.3-English/ug953-vivado-7series-libraries
[45] Y. Wang, W. Xie, H. Chen, and D. D.-U. Li, 'Low-Hardware Consumption, Resolution-Configurable Gray Code Oscillator Time-to-Digital Converters Implemented in 16 nm, 20 nm, and 28 nm FPGAs', *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 4256–4266, Apr. 2023.
[46] J. Wu and J. Xu, 'A Novel TDC Scheme: Combinatorial Gray Code Oscillator Based TDC for Low Power and Low Resource Usage Applications', in *2019 5th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP)*, Vienna, Austria: IEEE, May 2019, pp. 1–7.

[47] S. H. Unger, 'Hazards, critical races, and metastability', *IEEE Trans. Comput.*, vol. 44, no. 6, pp. 754–768, Jun. 1995.
[48] N. Lusardi, F. Garzetti, R. D. Marco, and A. Geraci, 'Implementation Issues of a High-Performance Multi-Channel Time-to-Digital Converter in Xilinx 20-nm UltraScale FPGAs', in *2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC)*, Sydney, Australia: IEEE, Nov. 2018, pp. 1–4.
[49] N. Lusardi, F. Garzetti, N. Corna, R. D. Marco, and A. Geraci, 'Very High-Performance 24-Channels Time-to-Digital Converter in Xilinx 20-nm Kintex UltraScale FPGA'.
[50] J. Wu, 'Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs', *IEEE Trans. Nucl. Sci.*, vol. 57, no. 3, pp. 1543–1548, Jun. 2010.
[51] N. Lusardi, N. Corna, F. Garzetti, S. Salgaro, and A. Geraci, 'Cross-Talk Issues in Time Measurements', *IEEE Access*, vol. 9, pp. 129303–129318, 2021.
[52] Xilinx, 'KCU105 Board User Guide', 2019, Accessed: Mar. 07, 2023. [Online]. Available: https://www.mouser.com/datasheet/2/903/ug917-kcu105-eval-bd-1596175.pdf
[53] Digilent, 'NetFPGA-SUME Reference Manual', Accessed: Mar. 07, 2023. [Online]. Available: https://digilent.com/reference/programmable-logic/netfpga-sume/reference-manual
[54] J. Wu, 'Uneven bin width digitization and a timing calibration method using cascaded PLL', in *2014 19th IEEE-NPSS Real Time Conference*, Nara, Japan: IEEE, May 2014, pp. 1–4.
[55] W. Xie, Y. Wang, H. Chen, and D. D.-U. Li, '128-Channel High-Linearity Resolution-Adjustable Time-to-Digital Converters for LiDAR Applications: Software Predictions and Hardware Implementations', *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 4264–4274, Apr. 2022.
[56] M. Parsakordasiabi, I. Vornicu, A. Rodriguez-Vazquez, and R. Carmona-Galan, 'An Efficient TDC Using a Dual-Mode Resource-Saving Method Evaluated in a 28-nm FPGA', *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–13, 2022.
[57] S. Tancock, J. Rarity, and N. Dahnoun, 'The Wave-Union Method on DSP Blocks: Improving FPGA-Based TDC Resolutions by 3x With a 1.5x Area Increase', *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–11, 2022.
[58] D. Portaluppi, K. Pasquinelli, I. Cusini, and F. Zappa, 'Multi-Channel FPGA Time-to-Digital Converter With 10 ps Bin and 40 ps FWHM', *IEEE Trans. Instrum. Meas.*, vol. 71, pp. 1–9, 2022.
[59] Y. Zhou, Y. Wang, Z. Song, and X. Kong, 'A High-Precision Folding Time-to-Digital Converter Implemented in Kintex-7 FPGA', *IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT*, vol. 72, 2023.
[60] N. Lusardi, F. Garzetti, A. Costa, E. Ronconi, and A. Geraci, 'From Multiphase to Novel Single-Phase Multichannel Shift-Clock Fast Counter Time-to-Digital Converter', *IEEE Trans. Ind. Electron.*, pp. 1–9, 2023.
[61] H. Chen, Y. Zhang, and D. D.-U. Li, 'A Low Nonlinearity, Missing-Code Free Time-to-Digital Converter Based on 28-nm FPGAs With Embedded Bin-Width Calibrations', *IEEE Trans. Instrum. Meas.*, vol. 66, no. 7, pp. 1912–1921, Jul. 2017.

Yu Wang was born in Chongqing, China in 1995. He received the B.Eng. degree in measurement and control from the Harbin University of Science and Technology, in 2017, and the M.Eng. degree in electronics and communication engineering from Harbin Engineering University, in 2020. Since 2020, he has been working toward the Ph.D. degree founded by China Scholarship Council at the University of Strathclyde, Glasgow, U.K. His current research interest is the FPGA-based mixed signal circuit.

Wujun Xie was born in Hunan, China, in 1996. He received he M.S. degree in embedded systems from the University of Southampton, Southampton, U.K., in 2018 and the Ph.D. degree from the University of Strathclyde, Glasgow, U.K, in 2023. He is currently working with Adaps Photonics Shenzhen, as senior system engineer. His current research interests are in SPAD based photon-sensing techniques.

Haochang Chen was born in Xian China, in 1990. He received the M.S. degree in embedded digital systems from the University of Sussex, Brighton, U.K., in 2013, and the PhD degree from the University of Strathclyde, Glasgow, U.K., in 2020. His current research interests include FPGA-based high-precision time metrology systems for ranging and biomedical imaging applications.

Chengquan Pei received the Ph.D. degree from Xi'an Jiaotong University, Xi'an China, in 2017. He was a post doctor in Tsinghua university from October 2018 to October 2021.He is currently a lecturer with the School of Artificial Intelligence, Xidian University, China. His research interests include computational photography, circuit and system, and computational femtosecond imaging.

David Day-Uei Li received his PhD in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2001. He then joined the Industrial Technology Research Institute, working on complementary metal-oxide-semiconductor (CMOS) optical and wireless communication chip- sets. From 2007 to 2011, he worked at the University of Edinburgh, Edinburgh, on two European projects focusing on CMOS single-photon avalanche diode sensors and systems. He then took the lectureship in biomedical engineering at the University of Sussex, Brighton, in mid-2011, and in 2014, he joined the University of Strathclyde, Glasgow, as a senior lecturer. He has published more than 100 research articles and patents. His research interests include time-resolved imaging and spectroscopy systems, mixed-signal circuits, CMOS sensors and systems, embedded systems, optical communications, and field programmable gate array/GPU computing. His research exploits advanced sensor technologies to reveal low-light but fast biological phenomena.