ANALYSIS AND DESIGN OF AN ULTRA-LOW POWER LOW-NOISE DTMOS BASED INSTRUMENTATION AMPLIFIER APPLIED TO THE PHYSIOLOGICAL SIGNAL ACQUISITION SYSTEM

By

YULING LIU

A thesis submitted in partial fulfillment of
the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

WASHINGTON STATE UNIVERSITY
School of Electrical Engineering & Computer Science

DECEMBER 2021

To the Faculty of Washington State University:

The members of the Committee appointed to examine the thesis of YULING LIU find it satisfactory and recommend that it be accepted.

_____

Subhanshu Gupta, Ph.D., Chair

_____

Daehyun Kim, Ph.D.

_____

Deukhyoun Heo, Ph.D.

ACKNOWLEDGMENT

I would like to express my special thanks of gratitude of my instructors Subhanshu Gupta to gave me the opportunity to do this wonderful project in this area as well as supportive and helpful with my thesis. Your insightful suggestion and feedback brought my work to a higher level.

Secondly, I would like to thanks our lab member Huan Hu, Qiuyan Xu, Chung-Ching Lin, Shrestha Bansal, and Leonardo Carreira for their valuable guidance throughout my studies. Their patient guidance and support brighting my research approach and study direction.

In addition, I would like to thank my parents, my girl and my cat. I could not have completed this thesis without the support from them. They are always there whenever I need.

ANALYSIS AND DESIGN OF AN ULTRA-LOW POWER LOW-NOISE DTMOS BASED INSTRUMENTATION AMPLIFIER APPLIED TO THE PHYSIOLOGICAL SIGNAL ACQUISITION SYSTEM

Abstract

by Yuling Liu, M.S.
Washington State University
December 2021

Chair: Subhanshu Gupta

With the rapid development of Internet of Things (IoT) technology and the popularity of portable devices, portable medical devices will become widely available soon. Physiological signal monitoring sensors are widely used for personal health management and long-term healthcare monitoring, especially for preventing acute illnesses and chronic disease monitoring for pediatric and elderly. Physiological signal monitoring sensors have the ability to monitor people's behavior in real-time for various daily activities, such as physiological signals that exhibit different waveforms and amplitudes when sleeping and awake. The real-time collected signals can be frequently compared to medical databases to detect abnormal health data for preventive healthcare.

Therefore, an accurate and error-free system that provides high-quality monitoring of physiological signals is very important. Typically, an instrumentation amplifier (IA) is used for high accurate acquisition and amplification within this system. An IA with excellent performance gives patients safer health conditions and allows patients to have better health protection.

This work introduces an ultra-low-power instrumentation amplifier operating at sub-0.4V voltage. Using dynamic threshold voltage MOSFET (DTMOS). The DTMOS reduces threshold voltage further and increases the driven current while the device is operating. Therefore, the DTMOS-based folded-cascode has been chosen, resulting in an increases the common-mode rejection ratio (CMRR) of the circuit while increasing the output signal swing compared over conventional topologies. The IA takes the benefit of the rail-to-rail common-mode feedback circuit and chopping to reduce flicker noise and DC offset. Reducing the chip area and power consumption leads to the output signal's high signal-to-noise ratio (SNR). The post-simulation shows that the circuit archives 45dB gain, DC to 2.07KHz operating bandwidth, and 0.8μW total power consumption. The simulated CMRR is 103dB, with 80dB power supply rejection ratio (PSRR). The simulated input reference noise is $140nV/\sqrt{Hz}$ (@100Hz) with 7.27 Noise Efficiency Factor (NEF).

Keywords: Instrumentation Amplifier, DTMOS, rail-to-rail, chopping, clock boosting switch, physiological acquisition, bio-medical application.

TABLE OF CONTENTS

Page

LIST OF TABLES

Page

LIST OF FIGURES

Page

Dedication

To my parents, wife, and lovely cat Nemo

CHAPTER ONE: INTRODUCTION

1.1 Motivation and background

According to WHO survey statistics, the global elderly population will more than double to 2.1 billion by 2050, with more people aged 60 and older than teenagers and young adults [1]. Especially in developing countries, the pace of population aging accelerates even more, but the ability of society to provide healthcare-related infrastructure is usually much lower than in developed countries. Existing medical resources are unable to meet the care needs of older people and are gradually becoming saturated. Therefore, home health care for the elderly is becoming more popular. And intelligent wearable devices, as small and efficient home medical and health devices, can provide good health management services for the elderly.

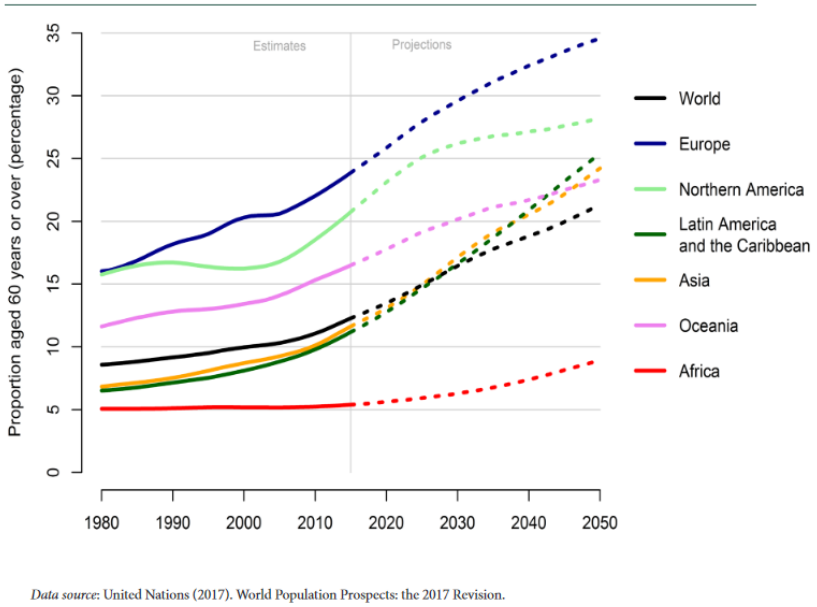

Fig. 1.1.1 World Population Prospects [1].

Wearable devices can play an essential role in monitoring health. Frequently and continuously measurements of physiology signal, such as electrocardiography (ECG), electroencephalography (EEG), electromyography (EMG) and physical activity, is significative

and actionable. According to the Stanford study, the physiological signal reveals personality differences in daily activity patterns. For example, a drop in blood oxygen levels always accompanies fatigue. However, a healthy person usually visits a hospital for a regular health checkup every year or even more than two years. These potential health hazards are generally challenging to detect if clinical symptoms appear several months before [2]. Therefore, combining information from wearable sensors with frequent medical measurements is easy and efficient to determine if there has been a significant change in someone's health condition. In conclusion, the short-term measurement is precious and meaningful to doctors or nurses.

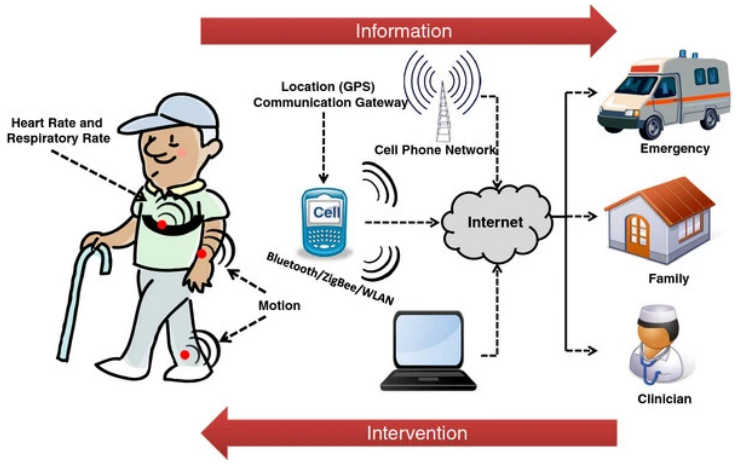

Fig. 1.1.2 Illustration of the wearable sensor-based remote health monitoring system[3].

Electrodes are commonly used to measure electrophysiological signals implement outside the body. The difference in ion concentration between the extracellular and intracellular of the cell provides potential energy. When the person is active, or when neurons are communicating, the cell contracts lead to membrane allow ions to penetrate, resulting in the flow of ions and create currents.

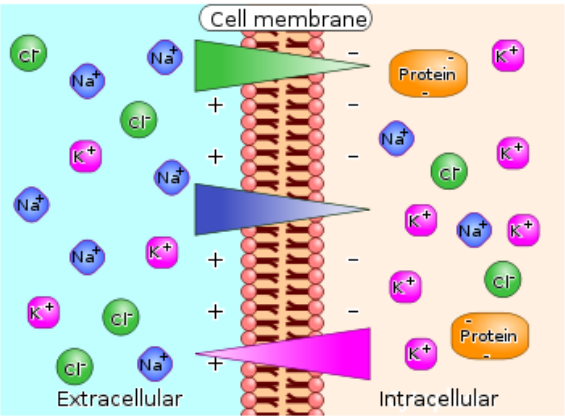

Fig. 1.1.3 Differences in ion concentrations on both sides of the cell membrane produce voltage differences[4].

The signal produced by ion flow is feeble. We cannot tolerate any attenuation before entering the AD/DA converter, which can seriously affect experimental and research results, or worse, lead to misjudgment of the patient's health condition by the doctor. Therefore, a high-performance general-purpose amplifier is significant in the long-term monitor bio-medical system. A well-performance amplifier will help the integrity of the signal and the accuracy of the AD/DA converter. In long-term monitoring sensor applications, the amplifier needs to target low power consumption characteristics, low noise, high energy-efficient, and high signal-to-noise ratio.

With the rise of the IoT, biomedical, and mobile device market, wireless sensor networks, biochips, and portable devices such as iPhones and iPad are increasing demands on system endurance and power utilization. The energy-efficient system with high speed, high energy density, and small size, low power consumption becomes the critical factor in ultra-low-power IC design. The most effective and command method for energy-thirsty application is to reduce the power supply voltage, which causes the transistor's driving capability reduction because the

threshold voltage does not decrease at the same rate as VDD reduction. Therefore, it becomes especially significant to develop a power-saving technology that can reduce the threshold voltage in ultra-low-voltage supply applications.

1.2 Thesis Organization

This thesis focuses on the instrumentation amplifier circuit module for bio-signal monitoring systems. The paper is divided into six chapters to complete the introduction of IA design. Chapter 1 describes the need of high performance instrumentation amplifier in biomonitoring systems. Chapter 2 describes the research background and main development direction.

Chapter 3 introduces the design, analysis, and performance improvement of the ultra-low voltage clock boosting switch, analyzing the non-ideal factors of the IA. Next, it presents the noise and offset mitigation techniques based on the previously mentioned clock boosting switch.

Chapter 4 determines the structure and specs of IA based on preliminary research, analysis and compares the difference between DTMOS and NMOS at ultra-low supply voltage. Then the circuit is designed, including the transconductance stage, output stage, rail-to-rail common-mode feedback circuit, and negative feedback amplifier circuit, and finally, the overall system framework and circuit arrangement are depicted.

Chapter 5 presents the layout and compares the post-layout simulation results with other state-of-art.

Chapter 6 provides a summary and describes future work.

CHAPTER TWO: SYSTEM DESIGN CONSIDERATION

2.1 History and development of IA

The first instrumentation amplifier was proposed in 1968 by Breuer[5]. This amplifier is easily implemented which built by op-amp and resistor (Fig. 2.1.1). Still, the input resistance is relatively small, and the resistor needs to be precisely matched to achieve a better common-mode rejection ratio. Because resistors cannot perfectly match, hence $\frac{R_1}{R_2} \neq \frac{R_3}{R_4}$.

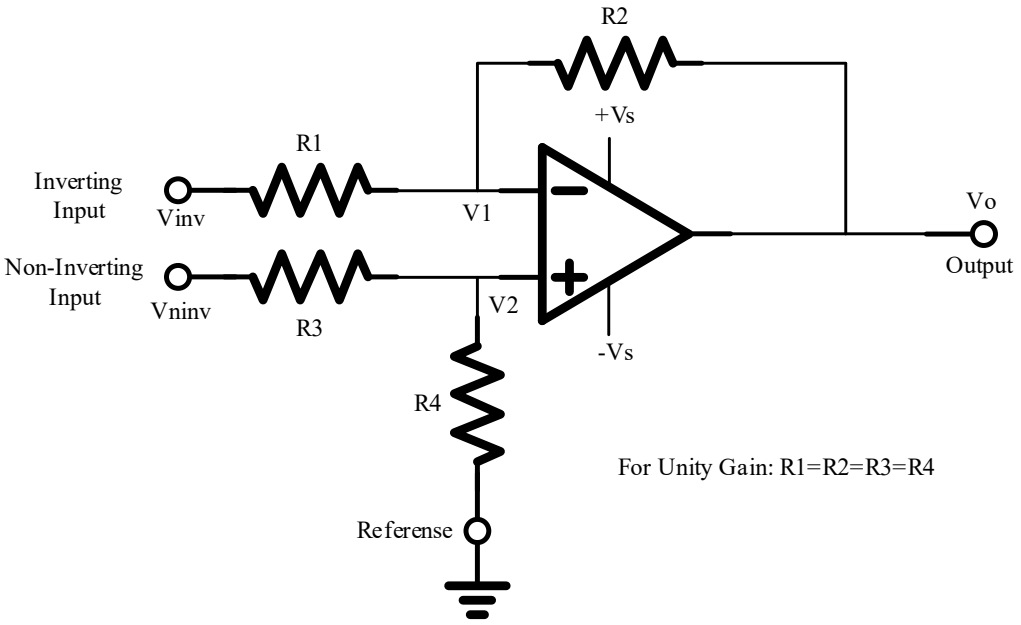

Fig. 2.1.1 The Unity-Gain Differential Instrumentation Amplifier [6].

Let us assume 0.1% resistor mismatch and ideal op-amps. $R_1 = R_4 = 9990\Omega, and\ R_2 = R_3 = 10010\Omega$. The common-mode rejection ratio can be presented by:

$$CMRR = \frac{A_{V,DM}}{A_{V,CM}} \tag{1}$$

The output voltage can be written by:

$$V_o = -\frac{R_2}{R_1} v_{inv} + \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) v_{ninv} \tag{2}$$

when $v_{inv} = \frac{v_{id}}{2}$ and $v_{ninv} = -\frac{v_{id}}{2}$

$$A_{V,DM} = -\frac{R_2}{2R_1} - \frac{R_4(R_1 + R_2)}{2R_1(R_3 + R_4)} = -\frac{1.0010V}{V} \tag{3}$$

when $v_{inv} = v_{ninv} = v_{cm}$

$$A_{v,CM} = -\frac{R_2}{R_1} + \frac{R_4(R_1 + R_2)}{R_1(R_3 + R_4)} = -\frac{0.0020V}{V} \tag{4}$$

Hence:

$$CMRR = 500 = 53dB \tag{5}$$

Due to the resistor mismatch, CMRR becomes a finite number. 53dB seems to be a terrible value for CMRR, this only considers the mismatch of four resistors, and the large resistors on the chip take up a large area and are difficult to match. What is worse is that when the source impedance is not equal at the input, and the resistance from the reference pin to ground is not zero, the common-mode rejection ratio will be seriously degraded[6].

Because the IA mentioned above in Fig. 2.1.1 does not meet the high CMRR design requirements, the three amplifiers were introduced[6]. This amplifier consists of two buffer amplifiers on the inputs and provides higher CMRR and better voltage gain (Fig. 2.1.2).

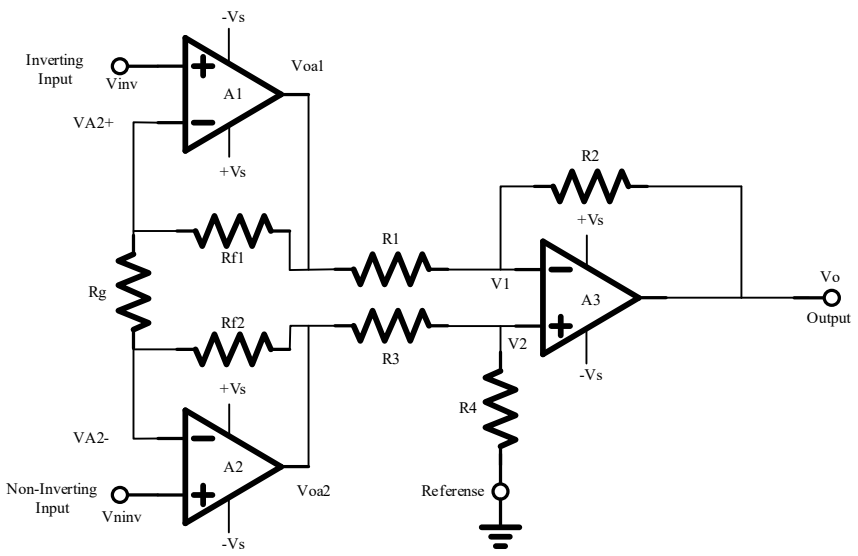

Fig. 2.1.2 The Classical three Op-Amp Instrumentation Amplifier.

Let us make some analysis here, same as signal op-amp IA. Again, assume 0.1% of resistor mismatch, and A1, A2 are two ideal op-amps. $R_{f1} = 9990\Omega, R_{f2} = 10010\Omega, R_g = 1K\Omega$

The overall gain equation for a three op-amp IA:

$$A_{v,DM} = (1 + \frac{R_{f1} + R_{f2}}{R_g}) * A_{v,cm}(second\ stage) = 21 * 1.001 = -21.021\frac{V}{V} \quad (6)$$

And common-mode gain for a three op-amp IA:

$$A_{v,CM} = 1 * A_{v,DM}(second\ stage) = -0.002 \quad (7)$$

Hence, the CMRR of a three op-amp IA can be written as:

$$CMRR = -\frac{21.021}{-0.002} = 80dB \quad (8)$$

The CMRR has been increased from 53dB to 80dB. Hence, the three op-amps IA could significantly improve CMRR by providing differential mode gain and unity common-mode gain.

Again, if we need to push CMRR further, a larger resistor must be used here, and large resistors are very difficult to match.

With the advent of SoCs, IA was often designed as a general-purpose amplifier due to market factors and cost considerations. But in fact, IA becomes a specific module to meet the application requirements. Some applications require low noise, and some applications require high output power, general purpose IA cannot meet all the application requirements simultaneously, which leads to IA as a fully customized amplifier nowadays. A highly degree of customization has led to the diversification of IA structures and functions in the last two decades, and researchers and scholars worldwide have been studying amplifier circuits more and more to design powerful performance IA.

Another problem arises here since large resistors are area-consuming and difficult to matching, and electrode offset voltage can be 100mV or worst. In other words, 100mV electrode offset my saturate the three op-amps IA. How are about using a coupling capacitor and reject DC offset at the input side? The answer is yes, coupling capacitor improvs not only high input impedance but also suppresses the DC bias of the electrodes. In 2003[7], Harrison et al. designed an IA using coupling capacitor feedback. Under a 2.5V power supply, the amplifier achieves 1.6uV input-referred noise, the CMRR and PSRR exceeded 80dB, exhibited a bandwidth of 30Hz at a power dissipation of 0.9uW using AMI ABN 1.5um CMOS process. Compared to three op-amps IA, the topology in Fig. 2.1.3 has a much simpler structure, lower power consumption, rejected electrode offset, and easy matching of on-chip capacitors. However, another problem here is how to determine the bias voltage of the input. Well, typically, the amplifier places a resistor to keep the input gate from floating. In fact, this resistance

requirement is enormous, reaching up to a few Giga Ohms and implemented usually using MOS-Bipolar pseudo-resistors to set DC bias level.

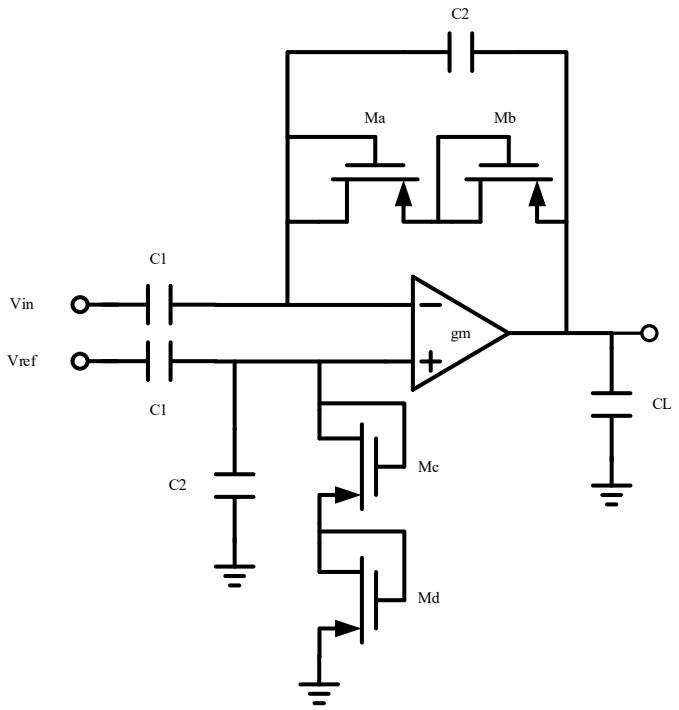

Fig. 2.1.3 Schematic of coupling capacitor feedback instrumentation amplifier [7].

In general, the first problem to overcome in physiological signal recording IA is flicker noise, and one of the current approaches to overcome this drawback is to combine an instrumentation amplifier with an offset cancellation technique. In 2012 [8], Yuhwai Tseng et al. utilized folded-cascode structure and chopper stabilization technique under the TSMC 180nm process to achieve 0.09uW power consumption, >120dB CMRR, and 0.88μV integrated in-band noise at 0.4V power supply.

In 2015 [9], A. Pipino el at. designed a rail-to-rail input chopper instrumentation amplifier in the 28nm CMOS process. This amplifier takes the benefits of NMOS and PMOS input pair, ensures a constant gm over the available common-mode range. The circuit operates

with a 0.9V power supply and exhibits a simulated 106dB DC gain and 329kHz GBW. Input referred noise is $27nV/\sqrt{Hz}$, the supply current is 60uA, and NEF is 8.

In 2017 [10], Hyun-Sik Lee el at. introduced high-performance current-feedback instrumentation amplifier (CFIA) for portable low power bio-potential sensing applications. The design takes the benefits of nested chopping frequencies, further reducing the residual offset and 1/f noise. Sharing cascode branches technology and Class-AB output stage improves power efficiency. The design achieves good noise and power consumption performance of the ripple reduction feedback loop (RRFL) simultaneously. The amplifier achieves 250dB low-frequency open-loop gain with gain boosting input stage. When operated as 60dB closed-loop gain, the amplifier's noise voltage density is $18nV/\sqrt{Hz}$, and the flicker noise corner below 3Hz. Under 3.3V voltage supply, amplifier consumes $75\mu A$ current, and both CMRR and PSRR > 110dB, with an average input offset of about $6.5\mu V$, achieves NEF of 4.2.

In 2021 [11], Sanfeng Zhang introduced a CMRR enhancement technique for ac-coupled instrumentation amplifiers (ACIAs), where improved mismatch of passive components leads to improvements of CMRR. The improved chopping topology is proposed to mitigate the mismatch effect of the pseudo-resistors. Utilizing a successive approximation-based capacitor trimming loop, the design achieves 110dB of CMRR at 50/60Hz, with in-band integrated input-referred noise as 3.2uV, implemented in 180nm process, the IA consumes 2.3uA current with 9.4 NEF.

In summary, for the IA design applied to the physiological signal acquisition, high CMRR, low noise, low power became the primary design approach. The main design ideas can be summarized as follows: High CMRR can be realized through current feedback technology[12] and coupling capacitor feedback[7]. Lower noise can be realized through offset and noise

cancellation technology such as chopping and auto-zeroing[13]. Advantages techniques such as ripple reduction loop and pseudo feedback DC servo loop, can push CMRR furthermore[14]–[16]. Technology scaling has also been shown to optimize chip area and integration through more advanced processes[9]. Higher gain can be provided with gain-boosting input stage and folded cascode topology in the main amplifier stage[10].

2.2 Physiological signal acquisition system

Wearable technology has changed over the last decade, however, with the dispersion of the functionality of wearable devices, such as portable watches and cameras, wearable glasses, intelligent belts, and shoes. The variety of smart mobile devices is increasing, and it is generally impossible to wear many devices on the human body. Hence, wearable devices are moving towards higher integration and smaller size, and the sensors need to be designed as small as possible and seamlessly into daily life. Moreover, the battery charge circle for each device needs to be short; devices need to be designed as ultra-low-power and energy-efficient systems.

A generalized physiological signals acquisition system usually consists of sensors, instrumentation amplifiers, signal processors, and signal transmitters. The sensing elements convert physical data to an electric signal, usually, consist of internal and body surface sensors. Internal sensors are generally placed electrodes inside the body through invasive procedures, such as implementing an electrodes matrix on the dura mater to measure electrocorticography (ECoG) signal. ECG, EEG recording can be done with body surface latch electrodes. The sensed signal is very tiny and cannot afford any attenuation. The signal is passed to the next stage, processed and amplified by IA, and the desired signal will be amplified in IA. Ideally, a clean and high-quality signal will be obtained at the IA output side. The signal is then fed into the AD converter, and the digitized signal is encoded and transmitted at the wireless communication RF

transmitter or decoded at the display monitor. Therefore, the IA plays a critical role in the acquisition system. Its performance directly affects the performance of the physiological signal acquisition system and concerns the health and safety of measurand.

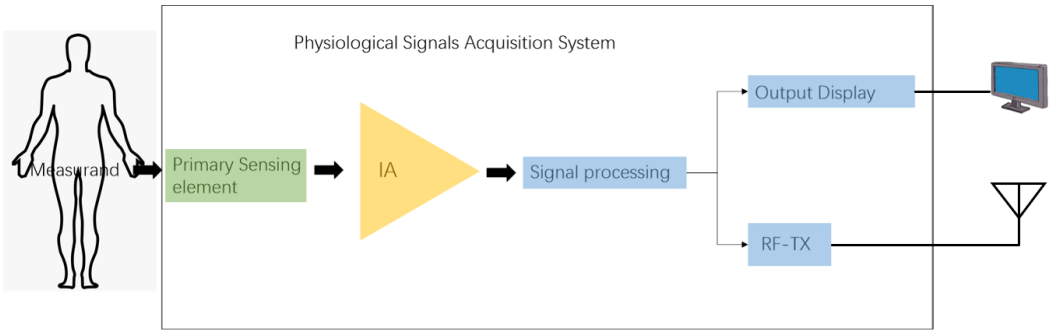

Fig. 2.2.1 A typical physiological signals acquisition system

CHAPTER THREE: ULTRA-LOW-VOLTAGE CHOPPER SWITCH DESIGN

3.1 Switching technique

The chopper switch is an essential block in the composition of the chopping, and its performance plays a decisive role in the overall performance of the chopper block and IA. Still, the leakage current during off-stage can cause a rapid degradation in the operating accuracy of IA. Especially at low supply voltages, the signal swing of the control signal is tiny. The on-state performance of the switch is seriously degraded, leading to the limitation of circuit bandwidth. In order to improve on-state capability, a common approach is to increase the ratio of W/L, which leads to the decrease of MOS threshold voltage. However, this increases the leakage current of the switch and deteriorates the linearity of the switch. Therefore, a good performance chopper switch is a prerequisite for a high quality, low noise IA.

3.1.1 Conventional switch

Fig. 3.1.1 Shows conventional NMOS switch, PMOS switch, and transmission gate. The on-resistance can be written as [17]:

$$R_{on,NMOS} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{DD} - V_{in} - V_{THN})} \tag{3.1.1}$$

$$R_{on,PMOS} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_P (V_{in} - |V_{THP}|)} \tag{3.1.2}$$

$$R_{on,tranmission\ gate} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_N (V_{in} - V_{THN}) - \left[\mu_n C_{ox} \left(\frac{W}{L}\right)_N - \mu_p C_{ox} \left(\frac{W}{L}\right)_P\right] V_{in} - \mu_n C_{ox} \left(\frac{W}{L}\right)_P |V_{THP}|} \tag{3.1.3}$$

From Eq. 3.1.1 to 3.1.3, the on-resistance of NMOS and PMOS is related to the input swing. It is interesting to note that the on-resistance of the transmission gate does not relate to input swing. In fact, μ_n and μ_p are not the same depending on doping density, $\mu_n C_{ox}\left(\frac{W}{L}\right)_N \neq \mu_p C_{ox}\left(\frac{W}{L}\right)_P$. Hence, its on-resistance is still a function of the correlation of the input signal.

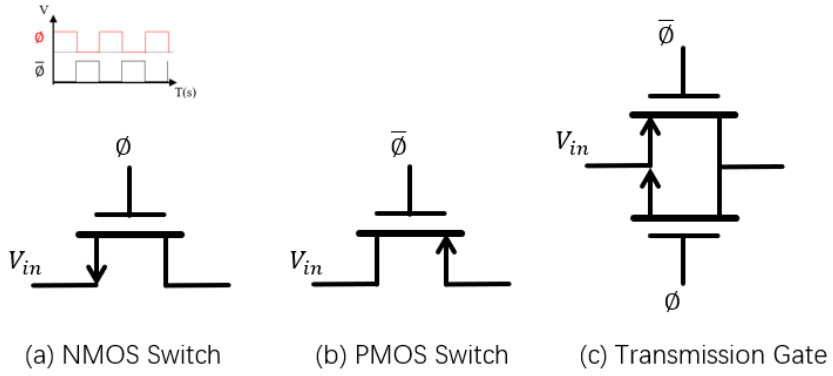

Fig. 3.1.1 Conventional (a) NMOS Switch, (b) PMOS Switch, and (c) Transmission Gate.

Fig. 3.1.2 plots the behavior of on-resistance of transmission gate in the general case, revealing much less variation than that corresponding to each switch alone [17]. On the contrary, NMOS only pass low-voltage signals; PMOS only pass high-voltage level signals.

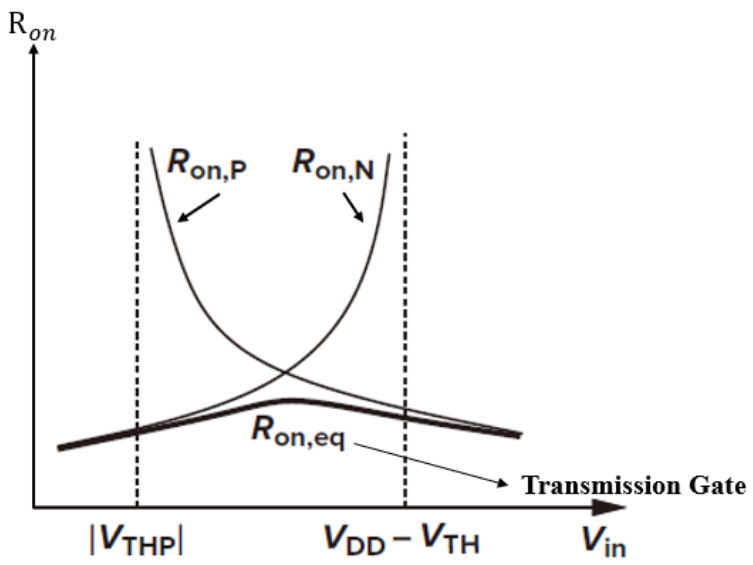

Fig. 3.1.2 On-resistance of the transmission gate[17].

3.1.2 Bootstrapped switch

The bootstrapped switch is a common method for improving switch on-state performance and switches linearity. The basic principle of the bootstrapped switch is shown in Fig. 3.1.3 When the switch is off-stage, the gate of the MOS switch shorted to the ground; When the switch is on-state, a battery capacitor connected to the gate and the source of the MOS switch, the gate voltage varies following the input signal due to the constant voltage of $V_{gs} = V_{DD}$.

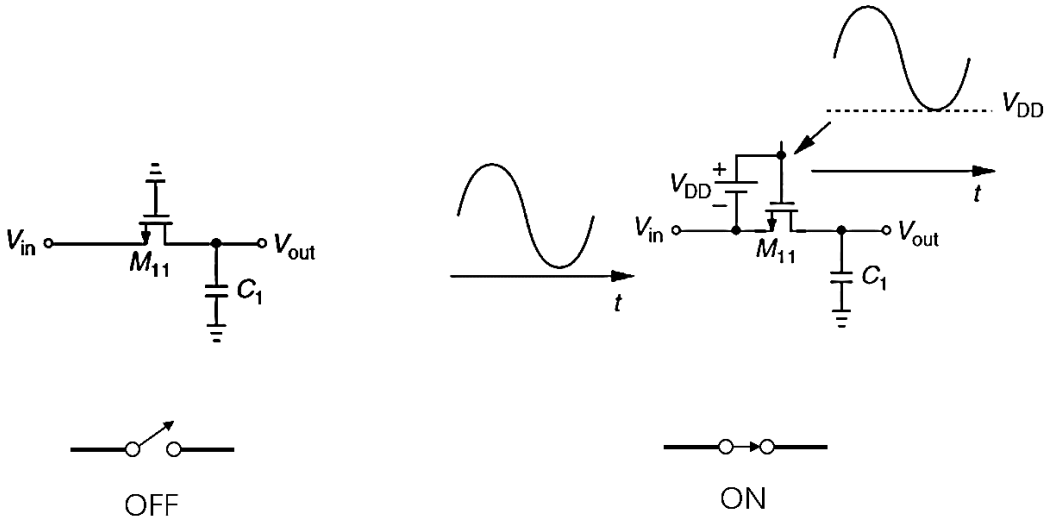

Fig. 3.1.3 The bootstrapped MOS switch.

Fig. 3.1.4 shows the actual circuit built by a charge pump and a bootstrap circuit. During the off-state, ϕ is low and $\bar{\phi}$ is high. M4 turns on, M5 turns off, charging the gate of M8 to VDD, M8 is disabled. M10 and M7 turn on discharge the gate voltage of M11 and M9 to the ground. In the meantime, M3 and M12 turn on, VDD is applied across the battery capacitor C3. Since both M8 and M9 turn off, the battery capacitor C3 isolates the gate-source of the transistor. During the on-state, ϕ goes high and $\bar{\phi}$ is low. M5 turns on, pulls down the gate voltage of M8, forces M8 and M9 to turn on, letting charge stored in battery capacitor C3 to flow charging note G[18], hence, the gate voltage of M11 is following the input signal, while Vgs constant equals to VDD. Equation 3.1.4 present the relation between gate-source voltage and battery capacitor. Hence, C3 must be sufficiently large to reduce the effect of the linearity of the switch.

$$V_g - V_{in} = \frac{C_3}{C_3 + C_p} * V_{DD} \tag{3.1.4}$$

Cp is the total parasitic capacitance connected to the top plate of C3 during the switch on-state[18].

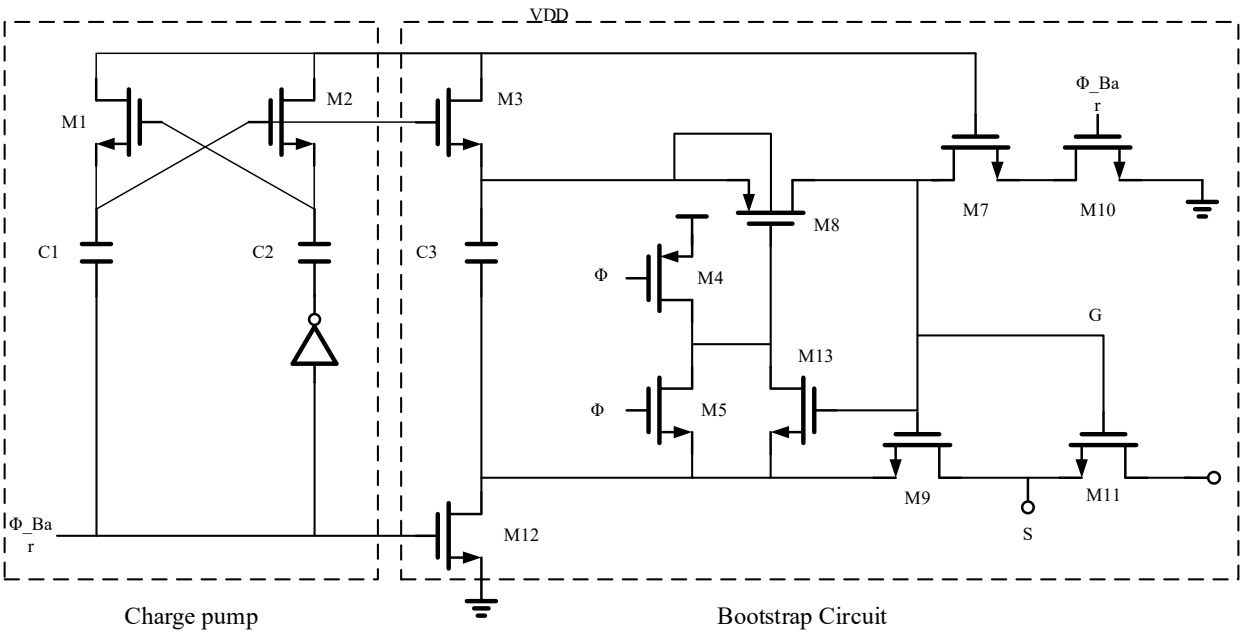

Fig. 3.1.4 The Bootstrap circuit including charge pump[18].

3.1.3 Clock boosting switch.

Another common technique to improve the linearity of the switch is the Clock Boosting Switch technique. In Fig. 3.1.4, the charge pump circuit can be used as the conventional clock boosting circuit. However, this circuit uses two capacitors while operating, occuping a larger area. An improved clock boosting switch has been introduced in this work. In Fig. 3.1.5, this circuit only requires one capacitor to be involved in the operation, so the area of the circuit can be smaller[19].

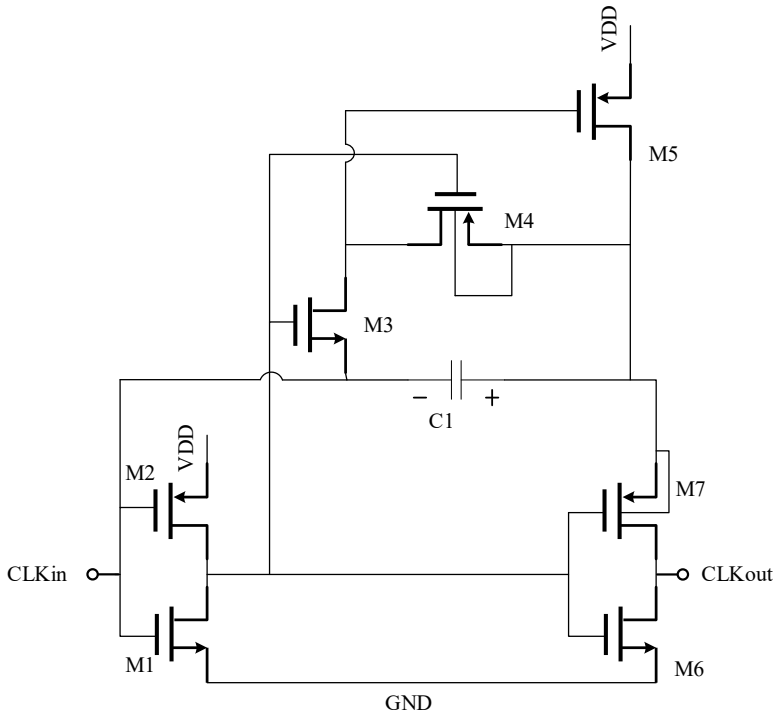

Fig. 3.1.5 Improved clock boosting switch.

When the input CLKin signal is low, the CLKout is low as well. M3 is on-state, pulls down the gate voltage of M5, enabling M5, and charging capacitor C1. When the input CLKin signal converts to high, it turns on M4 and disables M3, which leads to M5 turning off. Due to the VDD connected to the bottom-plate of C1, the voltage of the top-plate of C1 becomes 2*Vdd. And output signal CLKout becomes 2*Vdd as well.

3.1.3.1 Ultra-low-leakage current clock boosting switch.

In section 3.1.3, an improved single-cap clock boosting switch has been introduced. This circuit only improved on-state switch resistance. The modified ultra-low-leakage clock boosting switch combines dynamic threshold switching technique and with clock boosting switch technique allowing the switch to enhance the on-state and off-state performance simultaneously by decreasing on-resistance and off-state leakage current (Fig. 3.1.6) [20].

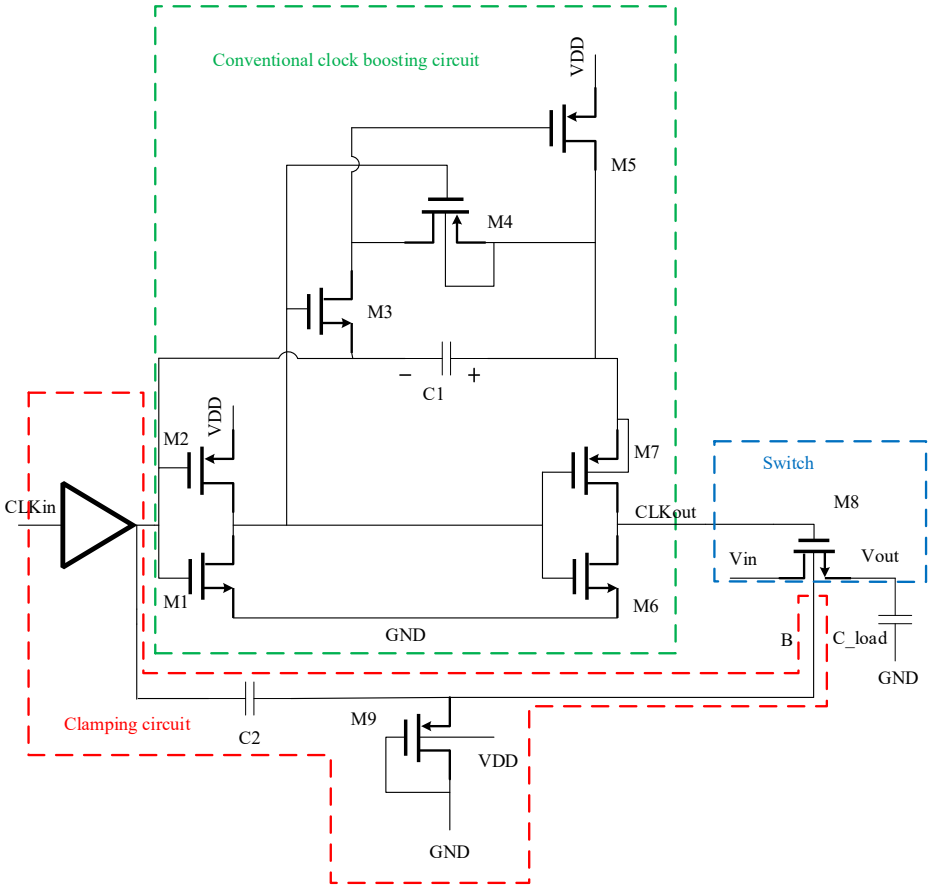

Fig. 3.1.6 Modified ultra-low-leakage clock boosting switch[20].

The proposed ultra-low-leakage clock boosting switch consists of a conventional clock boosting circuit, a clamping circuit, and a sampling switch. For the conventional clock boosting switch, when CLKin signal is low, M3 turns on, lead to M6 turn on, charging the top-plate of C1 to Vdd; When the CLkin signal goes high, the top-plate voltage of C1 pumps to 2*Vdd, and CLKout signal becomes 2*Vdd during the on-state phase. When the CLKin signal is high for the clamping circuit, M9 turns on, and a positive voltage can be seen at node B; when CLKin goes low, M9 turns off, the voltage at node B decreases to a negative voltage following the change with the CLKin signal. Therefore, when the switch is on-state, the gate voltage of the switch is pumped to 2*Vdd. Because the substrate voltage becomes positive, this leads to a decrease in the

threshold voltage, and increasing the on-state performance. During off-state, due to the voltage of substrate becomes negative, leads to the increasing of threshold voltage, and decreasing of the off-stage leakage.

The simulated results are shown in Fig. 3.1.7. During the on-state phase, the CLKout signal can be boosted to 786mV, and the voltage of node B can be clamped to a positive voltage around 55mV; During the off-state phase, the voltage at node B is pulled down to a negative value equals to -341mV. The simulated results verified that with a clamping circuit, the leakage current is limited to less than 8.027fA, but without a clamping circuit, the leakage current is as high as 9.28fA, the difference is 15%.

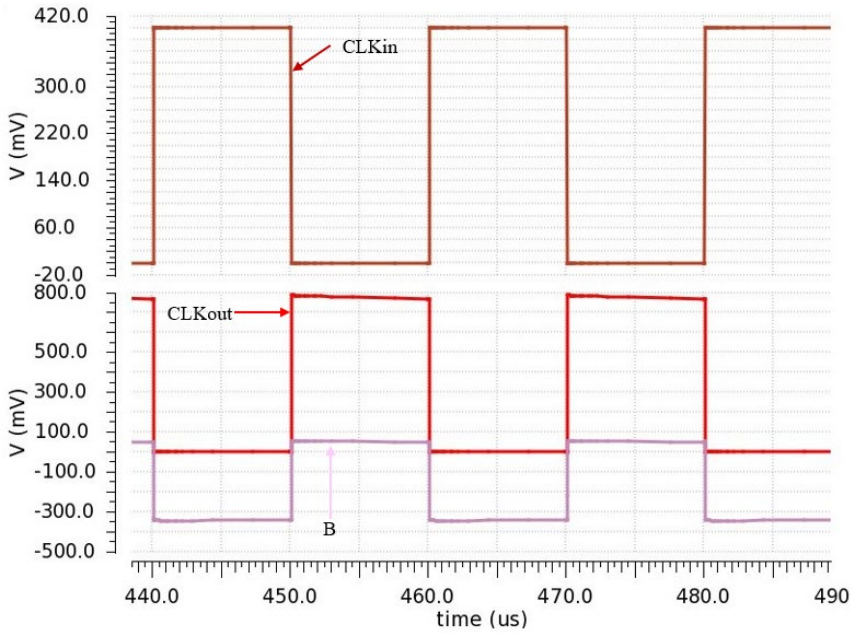

Fig. 3.1.7 Simulated results of ultra-low-leakage clock boosting circuit.

3.2 Noise, offset, and mitigation strategies.

As an operational amplifier consisting of CMOS, it also suffers from noise and offset, which severely limits the performance of IA. In practical applications, physiological signal monitoring

systems usually do not desire the noise to be amplified and hit the AD converter, so noise and offset should be eliminated at the IA. This section will analyze the components of noise in IA design, DC offset, and 50/60HZ interference. Then, two dynamic offset cancellation techniques are introduced and compared.

3.2.1 Noise, offset, and interference.

3.2.1.1 Thermal noise and flicker noise

Noise in IA design mainly comes from thermal noise, MOS thermal noise, and flicker noise. Resistor thermal noise is primarily caused by the random motion of electrons in the conductor, leads to fluctuation in the voltage across the resistor, and is independent of frequency[17]. When the temperature becomes higher, the electrons move faster, hence the thermal noise spectrum proportional to absolute temperature.

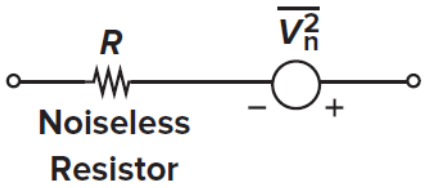

Fig. 3.2.1 Resistor thermal noise equivalent model.

As shown in Fig. 3.2.1, the thermal noise of a resistor R can be moduled by a noiseless resistor and a series noise source. Its one-side spectral density can be written as

$$\overline{V_n^2} = 4kTR, f \geq 0 \tag{3.2.1}$$

Where k is Boltzmann constant, T is Kelvin temperature, R is the resistance of the resistor.

MOS transistors' most significant noise generated in the channel, the thermal noise for a long channel MOS device operating in the saturation region can be modulated with a current

source connected between drain-source terminals. And MOS transistor thermal noise PSD is shown in Eq 3.2.2.

$$\overline{I_n^2} = 4kT\gamma g_m \tag{3.2.2}$$

Where g_m is the transconductance of MOS transistor, and γ typically equal to $\frac{2}{3}$ for long channel device, for submicron devices, the estimation value of γ become larger.

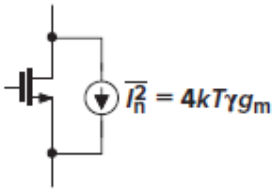

Fig. 3.2.2 MOS transistor thermal noise equivalent model.

For MOS transistors, another significant source of noise is flicker noise, 1/f noise. Unlike thermal noise, the average power of flicker noise is difficult to predict and varies with the CMOS process. The principle of flicker noise is when the carrier moves to the interface between the gate oxide and the silicon substrate, and many "dangling" bonds appear at the boundary of the silicon crystal. Hence some carriers will be randomly trapped and subsequently released by such energy states, leads to the flicker noise in the drain current[17]. Flicker noise can be roughly given by

$$\overline{V_n^2} = \frac{K}{C_{ox}WL}\frac{1}{f} \tag{3.2.3}$$

Where K is a process-dependent constant and roughly around $10^{-25}\ V^2F$. f is signal frequency, W and L are width and length of the transistor, and C_{ox} is gate capacitance per unit area.

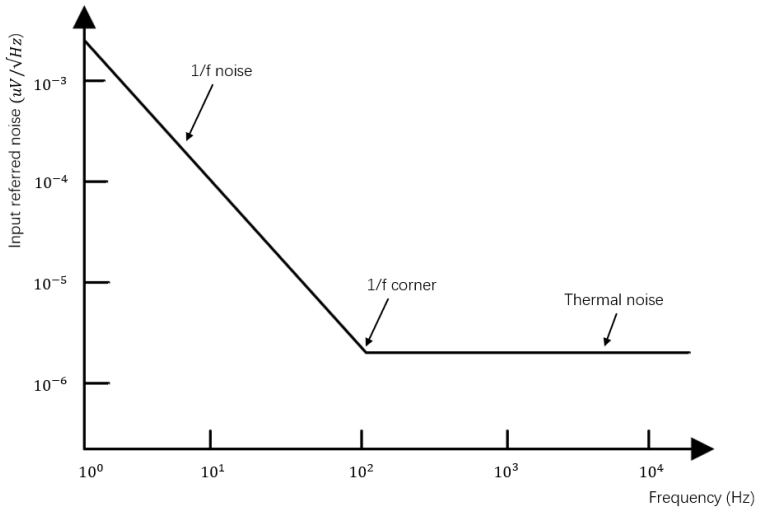

Fig. 3.2.3 Amplifier noise spectrum.

Fig. 3.2.3 shows that the noise spectrum consists of two significant noise sources: flicker and thermal noise. The 1/f noise is mainly located on the low-frequency band. As the frequency goes up, 1/f noise disappears, thermal noise becomes significant. Since physiological signal monitoring specifically targeted on low-frequency range. Hence, the major problem in IA design is to reduce the effect of flicker noise.

3.2.1.2 Offset

Offset is another factor that affects the design of high precision IA. The schematic of the ideal and non-ideal differential amplifier is shown in Fig 3.2.4. Ideally, the balanced differential amplifier is an offset-free structure, and the circuit can reject common-mode and power supply interference as well, however, due to process variation and lithographic errors. The size and the threshold voltage of the two input transistors will be different, and the load resistor will also be different, especially in the CMOS process.

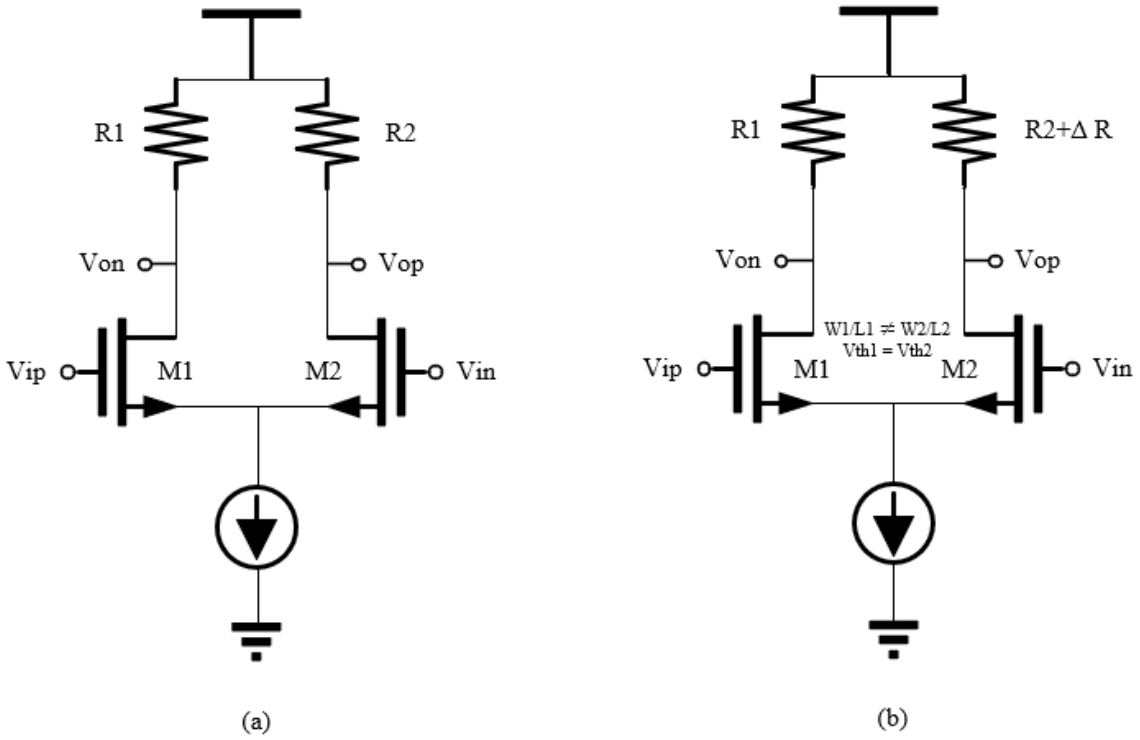

Fig 3.2.4 (a) A ideal differential amplifier (b) a non-ideal differential amplifier

The offset voltage V_{OS} can be given by

$$V_{OS} = \Delta V_{th1,2} - \frac{I}{g_{m1,2}}\left(\frac{\Delta R_{1,2}}{R_{1,2}} + \frac{\Delta \beta_{1,2}}{\beta_{1,2}}\right) \tag{3.2.4}$$

Where $\Delta V_{th1,2}$ is threshold voltage mismatch of two transistors. $\Delta R_{1,2}$ is load resistor mismatch. And $\beta = \mu_n C_{ox}\left(\frac{W}{L}\right)$, $\Delta \beta_{1,2}$ is the mismatch of the size of two transistors. With Eq. 3.2.4, to suppress the offset voltage, decreasing the gm/id ratio is a good approach, which usually depends on the DC bias point.

3.2.1.3 50/60Hz interference

The human body is an excellent coupler of external electromagnetic activity, especially at the low frequency of 50/60Hz. When electronic products are operating or powered lines, these devices are usually driven by 50/60 Hz AC power and 50/60 Hz interference riding on the common mode of the human body. Moreover, the output signal can be interfered with by power supply noise which is not desired. Therefore, the IA needs to reject the noise from the human body and power supply. The common-mode rejection ratio and power supply rejection ratio are important technical indicators to measure the noise suppression capability of IA [21].

3.2.2 Mitigation technique

According to the analysis in chapter 3.2.1, DC offset and low-frequency noise can significantly impact the performance of the overall physiological signal acquisition system. In fact, flicker noise can research several microvolts to hundreds of microvolts at DC and ultra-low frequency, resulting in extremely low signal-to-noise ratios. This falls far short of the design parameters presented at the beginning of the article, so special techniques are introduced to eliminate the performance impact of noise and offset in the actual IA design. Among the IA designs, the two most commonly used techniques are Auto-zeroing and chopping techniques. This chapter will briefly discuss these two techniques.

3.2.2.1 Auto-zeroing

The auto-zeroing technique is performed by discrete-time sampling, by estimating the offset and then substrate it from the desired signal. The basic principle can be elaborated in two phases: In the first phase or sampling phase, the circuit first samples the DC offset, measuring and storing the sampled charge for further use; In the second phase or auto-zero

phase, the signal is amplified, and the sampled offset, noise is automatically subtracted [22]. The schematic of the fully differential auto-zeroing amplifier is shown in Fig. 3.2.5.

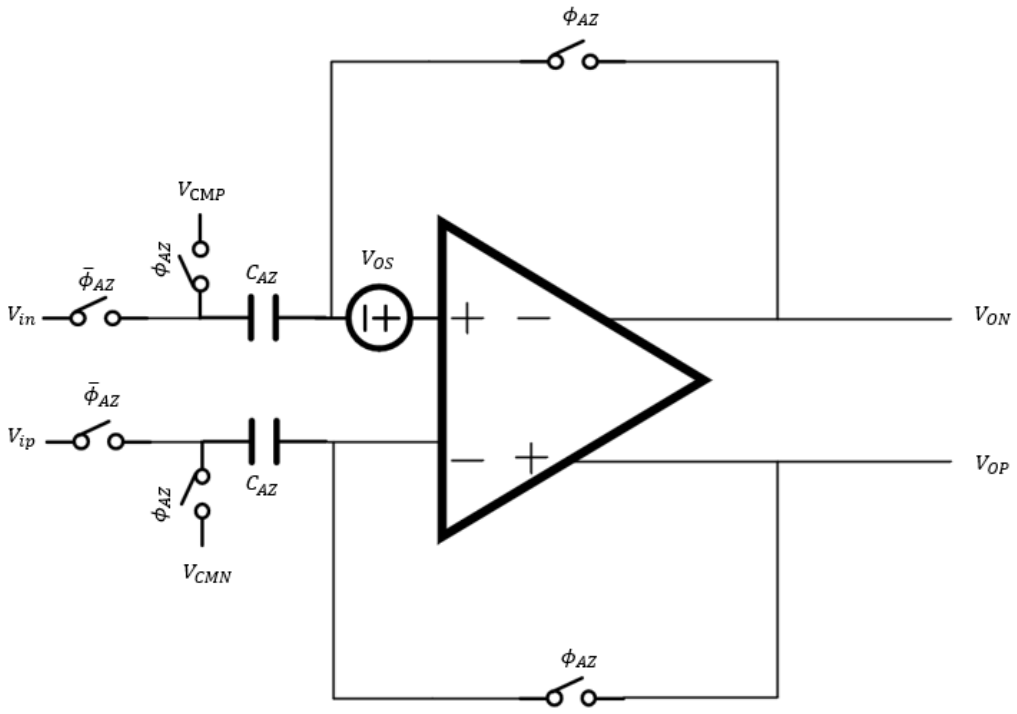

Fig. 3.2.5 Schematic of the fully differential auto-zeroing amplifier.

An auto-zeroing differential amplifier consists of six switches, two sampling capacitors, and the main amplifier. ϕ_{AZ} and $\bar{\phi}_{AZ}$ are two non-overlapping clock signals, and Vcm provides DC bias during the sampling phase. The clock phase can be analyzed as follows:

The sampling phase equivalent schematic is shown in Fig. 3.2.6, ϕ_{AZ} goes high, input signals are open circuit. The amplifier forms a unity gain loop structure, the offset in the amplifier is stored in the capacitor C_{AZ}.

The relationship between the offset voltage and the output voltage can be written as equation 3.2.5.

$$[(V_{ON} - V_{OS}) - V_{OP}]A = V_{OP} - V_{ON} \tag{3.2.5}$$

Where A is the open-loop gain of the amplifier, and after simplifying Eq. 3.2.5, Eq. 3.2.6 can be obtained:

$$V_{OP} - V_{ON} = \frac{-V_{OS} * A}{A + 1} \tag{3.2.6}$$

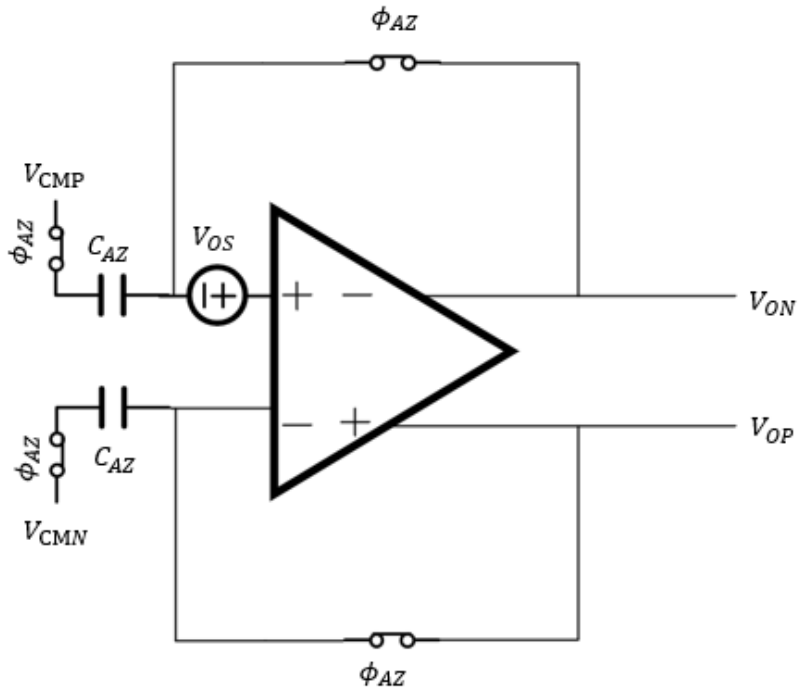

Fig. 3.2.6 Sampling phase schematic of the fully differential auto-zeroing amplifier.

During the auto-zero phase, ϕ_{AZ} goes low, and $\bar{\phi}_{AZ}$ is high voltage. The auto-zero phase schematic of the fully differential amplifier is shown in Fig. 3.2.7. In this phase, the input switches turn on, and the relationship between the input voltage and output voltage can be written as Eq. 3.2.7. The residual offset is only $\frac{V_{OS}}{A+1}$ at the amplifier output side.

$$V_{OP} - V_{ON} = (V_{IN} - V_{IP}) - (V_{CMP} - V_{CMN}) - \frac{V_{OS}}{A + 1} \tag{3.2.7}$$

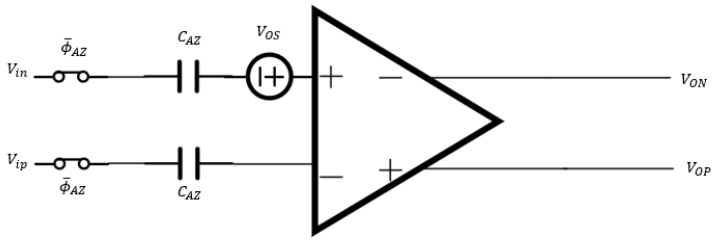

Fig. 3.2.7 Auto-zero phase schematic of the fully differential auto-zeroing amplifier.

In fact, the sampled offset is almost perfect due to charge injection and clock feed-through[23]. Therefore, choice of reasonable size of C_{AZ} becomes critical. If a large capacitor is used, the charge injection is smaller, but more chip area. If a small capacitor is used, the circuit setting time becomes faster, and auto-zero can happen at a faster rate but affects the equivalent input capacitance.

Another interesting point is that the auto-zeroing technique is partially effective in canceling the 1/f noise but increases the white noise due to noise foldover[24]

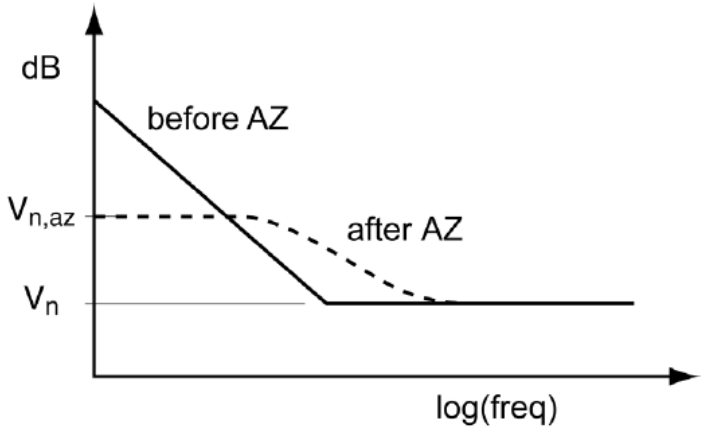

Fig. 3.2.8 Noise difference before and after auto-zeroing.

Auto-zeroing is a discrete-time sampled technique, noise removed by sampling the noise and then subtracting the amount of offset from the signal. Because of signal discontinuities and increased white noise, the chopping technique was introduced to overcome these problems.

3.2.2.2 Chopping

Chopping is a continuous-time noise cancellation technique, using modulation and demodulation technology, the desired signal and noise are separated through the frequency band, and noise can be filtered out by the low-pass filter. In practice, the chopper is usually composed of four identical transistors. Fig. 3.2.9 shows the schematic of the chopper.

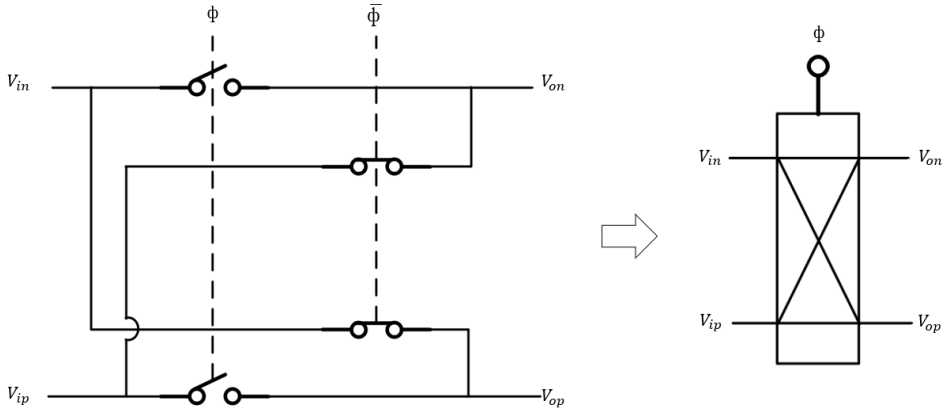

Fig. 3.2.9 Schematic of chopper switch.

The chopper switch is a polarity reversing circuit which can multiply the input signal by exactly +1 or -1 [22]. Using CMOS switch, the chopper can be used as a near-perfect square wave modulator ϕ and $\bar{\phi}$ are non-overlapping square wave signals used for the control of the switch clock signal.

A conventional chopper amplifier with the time-domain signal diagrams is shown in Fig. 3.2.10.

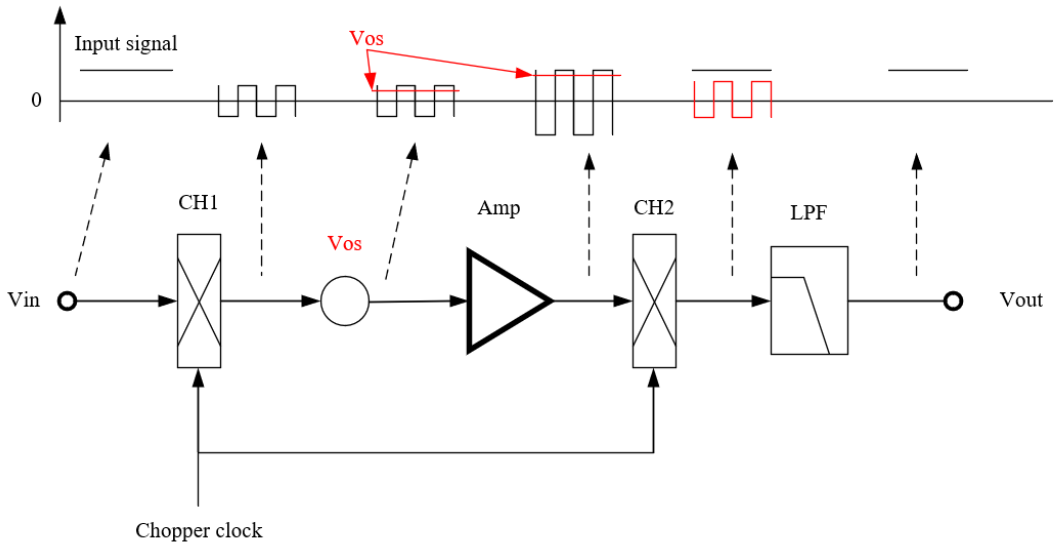

Fig. 3.2.10 Principal signals of the chopper in time domain.

For the input signal, Vin is passed through the first chopper switch CH1 and is modulated to a square wave signal. Then the modulated signal gets amplified, demodulated by the second chopper switch CH2, back to the DC, and pass to the low-pass filter (LPF). The noise and offset pass through the amplifier and square wave modulator once. Hence, they are amplified and modulated to a higher frequency. When this noise signal passes through the LPF, the noise is filtered out.

In the frequency domain, the noise cancellation process of the chopper amplifier is more easily observed. Same as the time domain, the input signal is modulated to a high frequency from the baseband at the odd harmonic of the chopping frequency after the chopper CH1. The modulated signal is then mixed with the amplifier's noise and offset and amplified simultaneously. Next, the amplified signal is modulated back to the baseband by chopper switch CH2 at the odd harmonic of the chopper frequency. Finally, the noise is filtered out by the LPF.

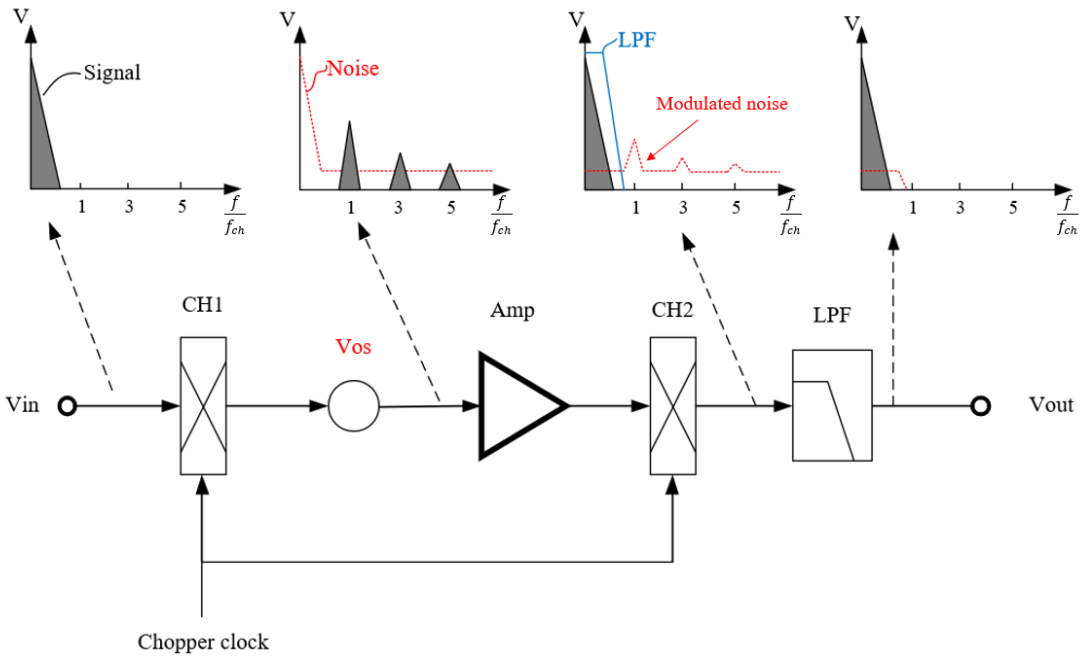

Fig. 3.2.11Principal signals of chopper in the frequency domain.

So basically, the chopper amplifier uses two square wave modulators to modulate the desired signal twice and modulate the noise once so that the desired signal is in the DC and the noise is on the high frequencies band, and a LPF can filter out the noise. The chopper technique does not need complex circuitry but only needs two square wave modulators totaling eight transistors to achieve flicker noise cancellation. Therefore, it is particularly suitable for small-are, low-power physiological signal acquisition IA applications. In practical applications, the chopping frequency needs to satisfy the following equation:

$$f_{corner} \ll f_{chop} \ll f_B \tag{3.2.8}$$

where f_{corner} is flicker noise corner, f_{chop} is chopping frequency, and f_B is unity-gain bandwidth of the amplifier.

But it is important to notice that chopper switches also have some disadvantages. First of all, if the chopper clock is not exactly 50% duty cycle, then the residual offset will be introduced. When the input square wave modulator is operating, the input impedance contributes extra thermal noise. Last but not least, amplifier gain at the chopping frequency typically be less than its DC gain because the modulated signal is not in the baseband.

In conclusion, auto-zeroing uses sampling to correct offset. Hence it is the discrete-time system, meanwhile, chopping uses modulation and demodulation, which is the continuous-time process system. Due to sampling, noise is fold back into the baseband, and thus, auto-zero has more in-band noise and requires more power for noise suppression. On the other side, the low-frequency noise of the chopper is consistent with their flat band noise. Although a large amount of energy is generated at the chopping frequency and its harmonics, the energy can be filtered using a LPF[25]. Therefore, to achieve low flicker noise, low integrated noise, and small area, the chopper technique is better for the low-power and low noise IA design.

3.3 Summary of this chapter

This chapter introduces the ultra-low-leakage switch, improved switch linearity operating in ultra-low-voltage, followed by a description of noise, offset, low-frequency interference, and its effect on IA performance. Finally, the two most commonly used noise cancellation methods are introduced, which are auto-zeroing and chopping. The advantages and disadvantages of the two methods are also compared. In the end, because of the requirement of low flicker noise in the physiological signal acquisition system, the chopping technique has been chosen. Combined with ultra-low leakage switch in square wave modulator to achieve low power consumption, small area, and good linearity chopper switch.

CHAPTER FOUR: THE FUNDAMENTAL OF ULTRA-LOW-POWER RAIL-TO-RAIL CHOPPER AMPLIFIER

4.1 Design Requirements

According to the previous discussion, the IA, as one of the essential modules in the physiological acquisition system, plays the role of amplifying recorded signals while canceling noise, offset and low-frequency interference, and suppression of common-mode and power supply interference. Hence, in low-voltage, low-power biomedical applications, the IA needs to meet several requirements.

Firstly, ultra-low-power physiological signal recording systems are generally used in long-term monitoring, even through invasive surgery to complete the sensor implantation. Therefore, unlike continuously powered devices, physiological signal acquisition sensors need to be powered by tiny batteries which means that their supply voltage cannot be very high. At the same time, implanted sensors in the body are unlikely to have their batteries replaced frequently and such devices usually need to be kept in operation for years or even decades.

Moreover, EEG, ECG, and EMG signals are typically in the range of DC to a few kHz and have very tiny amplitudes[26]. Unfortunately, the flicker noise also engulfs this band. To make matters worse, the physiological signals are usually feeble, and the flicker noise can seriously affect the signal to noise ratio. Therefore, the amplifier needs to be able to process the EEG, ECG, and EMG signals, span the frequency bands of these physiological signals, and at the same time needs to suppress flicker noise and prevent the effect of noise on the fundamental frequency signal.

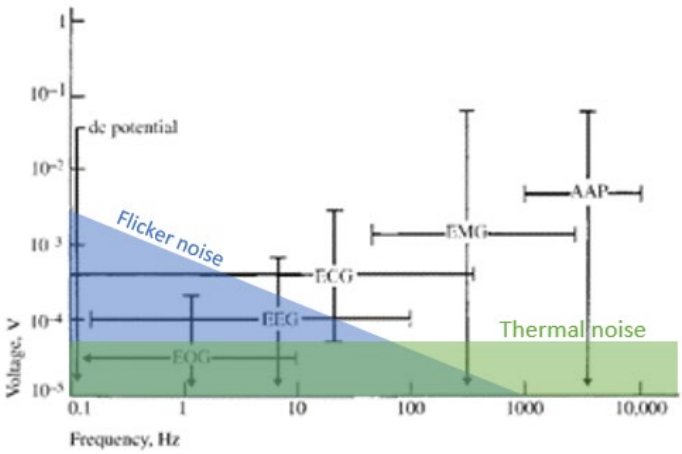

Fig. 4.1.1 Frequency ranges of electrooculography (EOG), EEG, ECG, EMG, and AAP physiological signals[26].

Fig. 4.1.2 shows a simplified electrocardiographic recording system, the operating conditions of dry electrodes usually consist of large impedance, if the input impedance of the amplifier is relatively small, the signal will be divided by the voltage divider, the signal develops an attenuation before it hit the amplifier. Therefore, the input impedance of the amplifier needs to be much larger than the impedance of electrodes.

Again, the IA also needs to meet a large enough CMRR because the human body is the coupler of external electromagnetic activity. Particularly, around 50Hz or 60Hz, the amplifier needs to be able to reject this through a common-mode rejection.

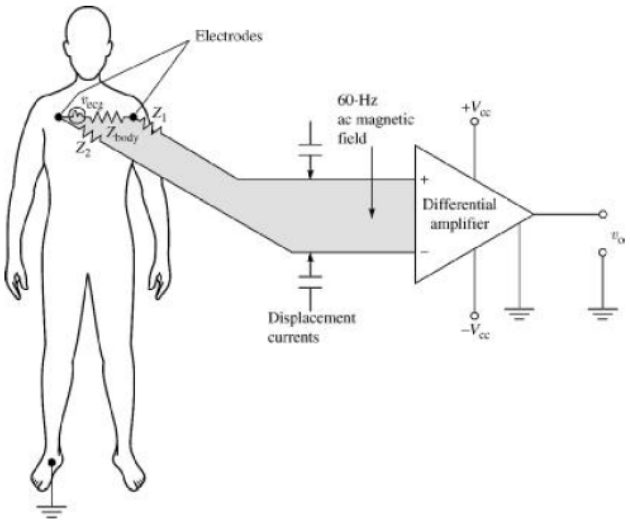

Fig. 4.1.2 Simplified electrocardiographic recording system [26].

Therefore, combined with the IA requirements presented in chapter 4.1, the IA needs to meet low-noise ($< 300nV/\sqrt{Hz}$), integrated noise ($< 10uV/\sqrt{Hz}$), large CMRR (>100dB), large input impedance, sufficient gain (>40dB), low power, low area.

Process	TSMC 65nm
Noise	$300nV/\sqrt{Hz}$
Int. noise	<10 uVrms
Bandwidth	DC- 2KHz
Rin	As large as possible
Gain (closed lop)	>40dB
Power	<3uW
Area	As small as possible
Rail-to-rail	Yes

(Output)	
VDD	0.4V
Current	<7.5uA As small as possible
CMRR	>100dB
PSRR	As large as possible

Tab. 4.1.1 IA design specifications.

4.2 Dynamic-threshold voltage MOS transistor

This chapter introduces a dynamic threshold voltage device that features reduced threshold voltage when the device is operating and reduced leakage current when the device is in the off-state. Next, DTMOS and CMOS were compared, and circuits are simulated in Cadence to analyze the advantages and disadvantages of the two different MOS transistors.

4.2.1 Background and why DTMOS

The body-biased CMOS technology makes it possible to use the fourth terminal, namely the bulk CMOS, which could forward-bias body-source junction, increase the drain-current, and scale down the threshold voltage. However, one issue needs to be considered here carefully while using the fourth terminal of a MOSFET. Increasing forward-biased voltage across body-source causes an increase in the body-current. The worst situation is more current flows into the body terminal when body-source becomes more forward biased, which is not desirable.

DTMOS was introduced by Chenming Hu and used in the SOI technology to overcome the disadvantages of body-biased CMOS technology[27] and satisfy the rapid growth of low-power and high-performance devices. The DTMOS technique has considerable merit due to as scaling down the threshold voltage, and raising the drain current, boosts device speed during on-state, and forces the threshold voltage to be high, decreasing the drain current and saving energy. More details are addressed in the following sections.

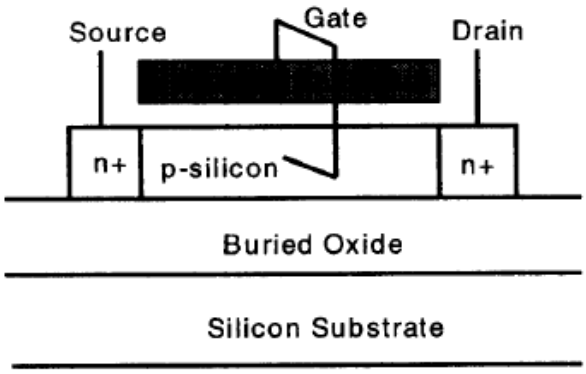

Fig. 4.2.1 Schematic of a SOI NMOSFET with body and gate [27].

4.2.2 The principle of DTMOS

The DTMOS technique is to tie the gate and bulk together. The threshold voltage of MOSFET can be defined as

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right) \tag{4.2.1}$$

where V_{T0} is the threshold voltage at zero body bias, γ is the body effect coefficient, $2\phi_F$ is the silicon surface potential at strong inversion, V_{SB} is the body-source voltage. Since the bulk and gate are tied together, when the transistor is on-state, V_{SB} becomes low, and V_T reduces, raising the switching speed, driving capability, and drain current. During off-state, body voltage gets back to zero, and V_{SB} increases its zero body bias value, Vt becomes high,

decreasing the drain current and saving energy. Due to the effective-normal field in the channel being lowered and the depletion charge is reduced, the DTMOS carries higher mobility[27]. Similar, the discussion can be done for the dynamic threshold-PMOS transistors. DTMOS devises implementation is shown in Fig. 4.2.2.

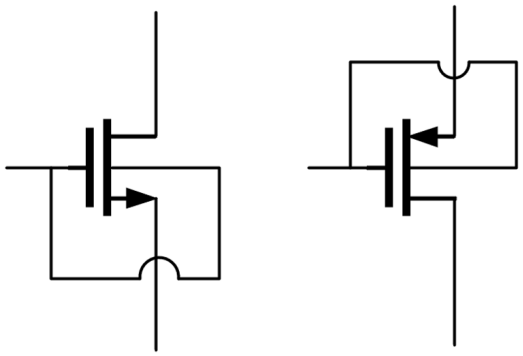

Fig. 4.2.2 (a) DT- NMOS transistor and (b) DT-PMOS transistor.

Conventionally IA is designed using bipolar process. However, with the requirement of lower power consumption applications, the CMOS process has become popular in the IAs design and is proliferating. Although DTMOS transistors were initially proposed for fabrication in the SOI process, as CMOS became more popular and the CMOS process continued to evolve, the fabrication costs has continued to drop leading to DTMOS getting adopted for IA designs. The most advanced CMOS process provides deep N-well devices that allows DT-NMOS transistors to have independent body bias terminals[28]. Fig. 4.2.3 shows the cross-section diagram of the triple-well CMOS.

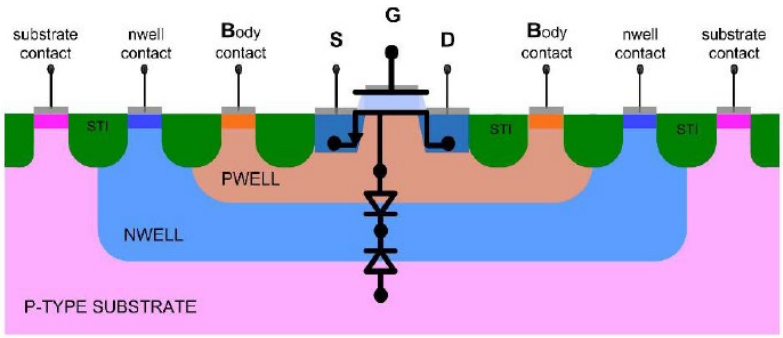

Fig. 4.2.3 The cross-section of the deep N-well NMOS transistor[28].

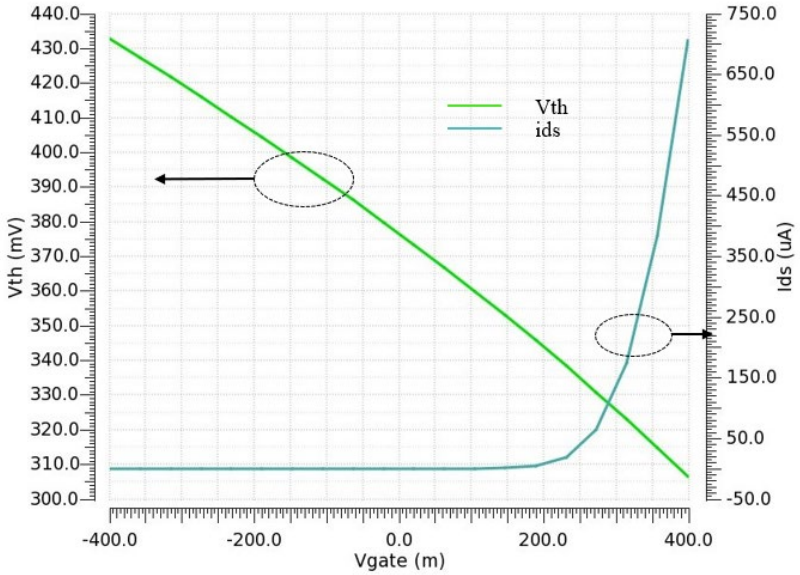

Fig. 4.2.4 Simulated result of the DTMOS threshold voltage and drain currents for various gate voltages.

From Fig. 4.2.3, it is easily to observe the ability to fabricate DT-NMOS devices in CMOS processes through deep N-well structures. DT-NMOS can be realized by connecting body directly to the gate with the N-well shorted to the ground. In contrast, for DTPMOS, there is no need for the triple-layer structure due to PMOS having a local N-well directly connected to the gate of PMOS. Fig. 4.2.4 shows the changes of threshold voltage and drain

current of DTMOS for various gate voltages. The threshold voltage decreases as the gate voltage becomes larger, and the drain current increases as the gate voltage increases after the DTNMOS is operating.

4.2.3 DTMOS vs conventional MOS transistor

In the previous section, we have introduced the characteristics and implementation of DTMOS. The following will describe how DT-NMOS compares to NMOS and what performance advantages DTMOS has. Fig. 4.2.5 shows the comparison of DTMOS and NMOS threshold voltage and drain current for different gate voltages.

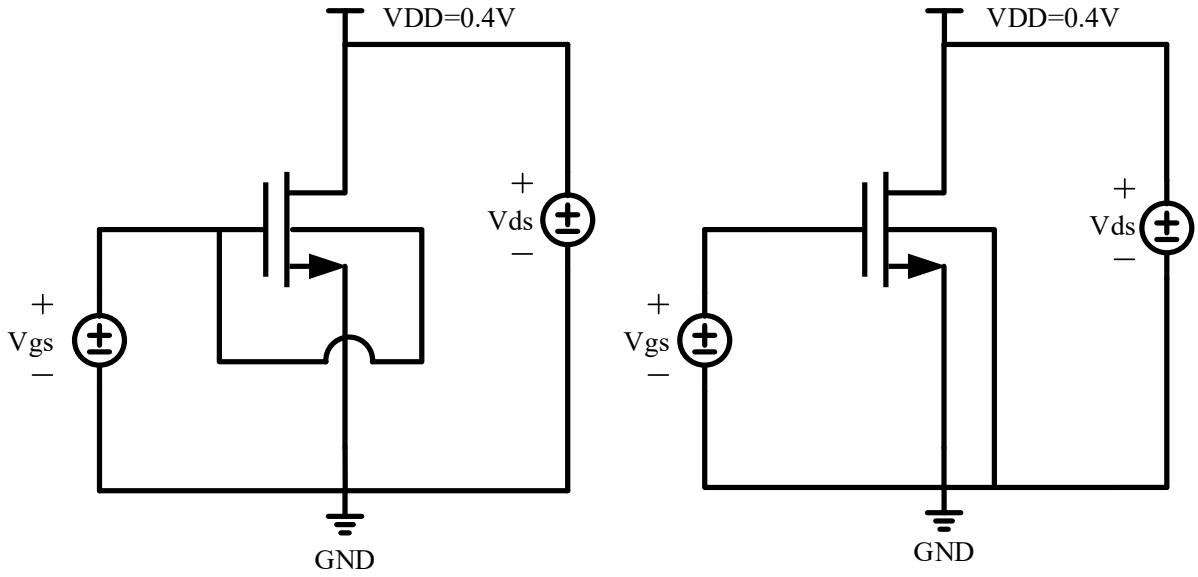

Fig. 4.2.5 DTNMOS and NMOS test bench used.

Compared to the DTMOS device, the threshold voltage of NMOS stays constant with varing gate voltage. Therefore, the larger threshold voltage leads to a reduction in the overdrive current, reducing the transistor's transconductance. For DTMOS, as the voltage rises from -400mV to 400mV, Vth drops from 430mV to 310mV, while ids increase from

0mA to almost 750μA. When the gate voltage is 250mV, the overdrive current of DTNMOS can be 178% of NMOS (Fig. 4.2.6).

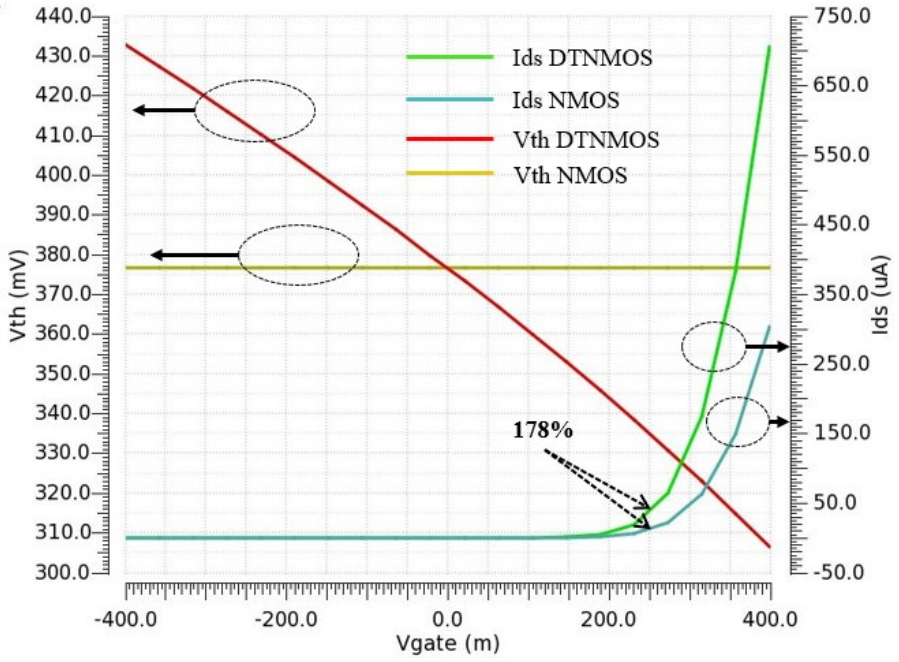

Fig. 4.2.6 Simulated result of the DTMOS and NMOS threshold voltage and drain current for various gate voltages.

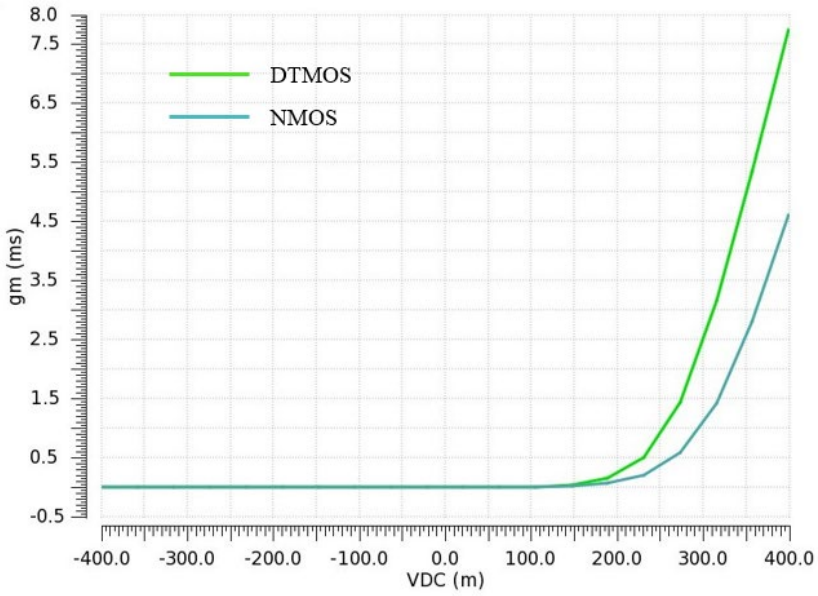

Fig. 4.2.7 Simulated results of the DTMOS gm for various gate voltages.

Fig. 4.2.7 shows simulated results of the DTMOS transconductance gm for various gate voltages. Due to the larger overdrive current, when the transistor is turned ON, the transconductance of DTMOS is larger than NMOS at the same gate voltage, and the difference between g_m of the two transistors gets larger as the gate voltage rises.

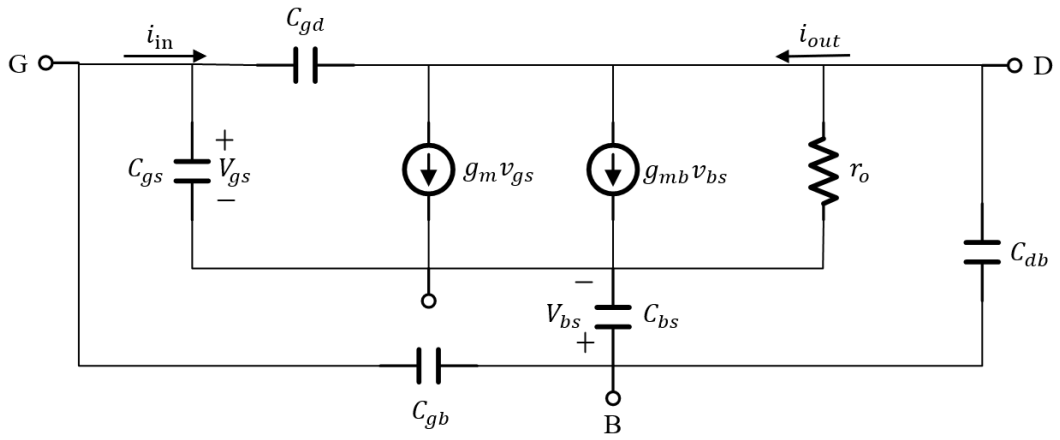

Fig. 4.2.8 Small-signal DTMOS transistor equivalent circuit

Fig. 4.2.8 shows the small-signal DTMOS transistor equivalent circuit. The small-signal input current i_{in} is

$$i_{in} = jw(C_{gs} + C_{gb} + C_{gd})V_{gs} \tag{4.2.2}$$

and output i_{out} is

$$i_{out} \approx g_m v_{gs} \tag{4.2.3}$$

the current gain can be written as

$$\frac{i_{out}}{i_{in}} \approx \frac{g_m}{jw(C_{gs} + C_{gb} + C_{gd})} \tag{4.2.4}$$

the frequency response can be defined as

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gb} + C_{gd}\right)} \tag{4.2.5}$$

DTMOS has gate tied to the body together, C_{gb} can be significantly reduced. On the other hand, we discussed that DTMOS has a larger transconductance compared to conventional NMOS. Therefore, by increasing transconductance and decreasing C_{gb}, DTMOS has wider bandwidth compared to conventional NMOS.

In summary, the DTMOS can be fabricated by the CMOS process using the deep N-well structure. Moreover, DTMOS can provide a smaller threshold voltage when the transistor is operating, increasing the overdrive current to increase the transconductance and bandwidth. It can also increase the threshold voltage when it is turned off, reducing the leakage current to save power.

4.3 DTMOS based OTA.

In the previous section, DTMOS devices are discussed and introduced compared to conventional NMOS. We observed that the DTMOS has a higher transistor drive and a smaller sleep current which saves more power during off-state than conventional NMOS.

In this section, a DTMOS based two-stage folded-cascode amplifier will be introduced. Secondly, the implementation of the chopper will be presented, and a new implementation method is introduced, allowing the improvement of the circuit mismatch. Next, the entire chopper amplifier will be used with the closed-loop IA, and this IA will be analyzed. Finally, why IA is commonly used with the pseudo resistor will be discussed. The bias network and 4-Transistors bandgap will be mentioned last in this subsection.

4.3.1 Open-loop op-amp design strategies

The design of the open-loop amplifier is a critical part of closed-loop IA design. The performance of the open-loop amplifier directly determines the stability of the closed-loop amplifier. The single-stage operational amplifier is an op-amp composed of one signal amplifier stage circuit, which has the advantages of simple structure, small area, fast speed, and low power consumption. Because of the larger gain and high swing demand of IAs, single-stage amplifier cannot meet both. Therefore, the two-stage amplifier is the preferred choice for IA in for physiological signal acquisition systems.

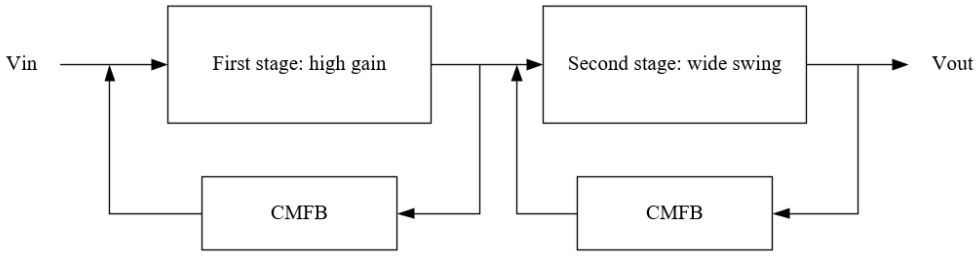

Fig. 4.3.1 General structure of two-stage IA.

Fig. 4.3.1 illustrates a common approach of a typical two-stage IA. The first stage usually consists of a differential amplifier as the input stage, implemented through a basic differential 5-transistors amplifier, telescopic amplifier, or a folded-cascode amplifier as required. The second stage, as an output stage, needs to provide a wider signal swing. Therefore, a two-stage op-amp structure is the best approach for designing a high gain and wide swing IA.

4.3.2 DTMOS based two-stage folded-cascode amplifier

The low-power, low-noise IA design specs have been discussed in the previous section, so high-performance IA designs cannot choose the classic 5-transistors differential amplifier for the first stage amplifier. Its performance does not meet the requirements of low noise, high gain, and high CMRR. How about telescopic and folded-cascode? Which one is better? Let us analyze telescopic topology at first.

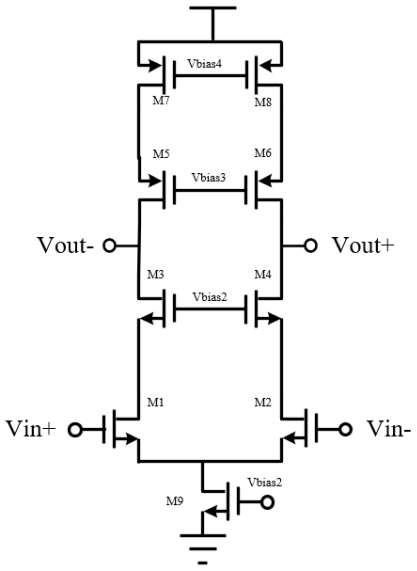

Fig. 4.3.2 Circuit schematic of telescopic amplifier.

Fig. 4.3.2 shows the circuit schematic of the telescopic amplifier. The first issue observed here is voltage headroom for each transistor. As the available maximum supply voltage required by the system is 0.4V, five transistors are stacked from power to ground terminal, such that maximum average Vds of each transistor does not exceed 80mV. In the subthreshold region, the transistor model satisfies the following relationship[29]

$$V_{gs} \leq V_{TH} \tag{4.3.1}$$

where Vgs is the voltage across gate-source, Vth is the threshold voltage of the transistor. And drain current can be written as

$$I_d = I_s e^{\left(\frac{V_{gs}-V_T}{nkT/q}\right)}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right)(1 + \lambda V_{DS}) \tag{4.3.2}$$

For

$$V_{ds} > \frac{3kT}{q} \approx 78mV \tag{4.3.3}$$

$$1 - e^{-\frac{V_{DS}}{kT/q}} \approx 1 \tag{4.3.4}$$

Hence, when V_{DS}> 3kT/q, Ids become independent of V_{DS}[30]. Again, the Vds of each transistor does not exceed 80mV for the telescopic amplifier, at the same time, the subthreshold region needs to satisfying V_{DS} for each transistor greater than 78mV. This very tiny headroom can make the design intricate.

Another problem here is the narrow input common-mode range. Equation 4.3.5 shows the common-mode input range of the amplifier in Fig. 4.3.2.

$$V_{ds9} + V_{gs1,2} < ICMR < VDD - V_{ds7,8} - V_{ds5,6} - V_{ds3,4} + V_{th1,2} \tag{4.3.5}$$

It is apparent that when VDD is only 400mV, the ICMR range can become very narrow. Changes in the common-mode input can easily lead to changes in the DC biasing point and tail current of M9, resulting in CMRR deterioration. Therefore, the telescopic structure is not a good choice for ultra-low voltage supply and high CMRR IA design.

Conversely, the folded-cascode amplifier has a higher common-mode input range and a larger CMRR than the telescopic amplifier. First, let us analyze the circuit of the folded-cascode amplifier, after that, the advantages and disadvantages of the folded-cascode amplifier can be visualized.

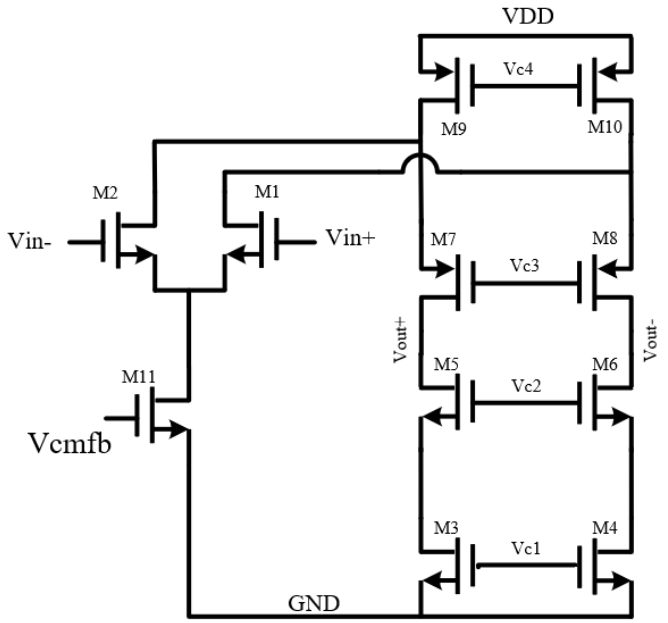

Fig. 4.3.3 Circuit schematic of folded-cascode stage.

Fig. 4.3.3 shows the circuit schematic of the folded-cascode amplifier stage. With the sub-0.4V power supply voltage, stacking four transistors becomes possible, and compared to the telescopic amplifier's average maximum Vds of 80mV per transistor, the folded-cascode topology can achieve an average Vds of 100mV for each transistor, ensuring that each MOSFET operates in the sub-threshold region.

The input common-mode range for the folded-cascode amplifier stage can be written as

$$V_{DS11} + V_{gs1,2} < ICMR < V_{DD} - V_{DS9,10} + V_{th1,2} \tag{4.3.6}$$

The Vds of only one folded transistor is subtracted from the VDD terminal, so the maximum ICMR is much larger than the telescopic stage. Larger common-mode input rage leads to the more stable DC bias point of the amplifier, resulting in larger CMRR. Because of fewer stacked transistors, the input signal swing is also improved. As there are more branches, more current and power is consumed.

The noise analysis of the folded-cascode amplifier can be written as follows. M1 and M2 output current can be written as

$$i_{1,2} = g_{m1,2} * V_{n1,2} \tag{4.3.7}$$

M9 and M10 output current can be written as

$$i_{9,10} = g_{m9,10} * V_{n9,10} \tag{4.3.8}$$

Similarly, M3 and M4 generates the output current is

$$i_{3,4} = g_{m3,4} * V_{n3,4} \tag{4.3.9}$$

At the same time, M7 and M8, M5 and M6, the four cascode transistors can be neglected at low frequencies. Hence the total input-referred noise density becomes:

$$V_{i,eq}^2 = \frac{2\left(i_{1,2}^2 + i_{9,10}^2 + i_{3,4}^2\right)}{g_m^2} = 2\left(V_{n1,2}^2 + \frac{g_{m9,10}^2 * V_{n9,10}^2}{g_{m1,2}^2} + \frac{g_{m3,4}^2 * V_{n3,4}^2}{g_{m1,2}^2}\right) \tag{4.3.10}$$

where $\overline{i_d^2} = \frac{8}{3} kT g_m$, and the RMS noise level will be the in-band integral of the input-referred noise. Therefore, we can find that reducing the in-band noise and the input-referred noise density increases the gm of the input transistor M1,2 and reduces the gm of the current source transistor M3,4,9,10.

In chapter 4, Fig. 4.2.7 has been introduced DTMOS has a significant improvement on transconductance gm, so the technique of using DTMOS on the input pair can improve the input transistor's gm and thus reduce the noise. A common source amplifier is selected for the second stage to increase the output signal swing.

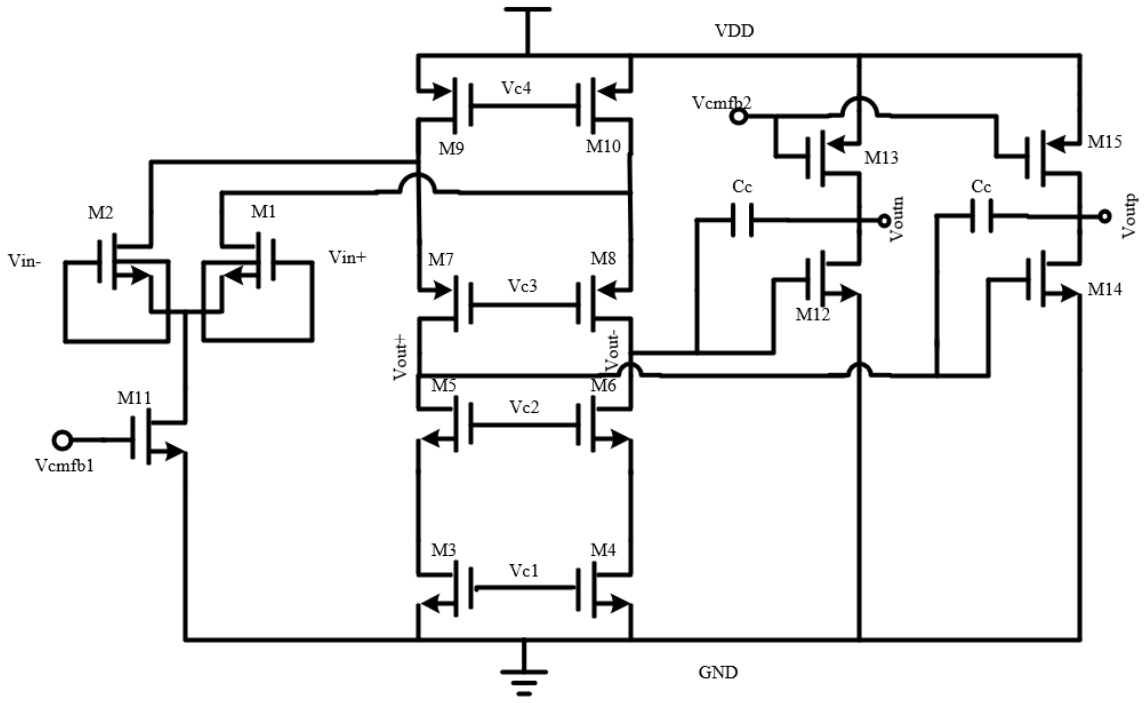

Fig. 4.3.4 Circuit schematic of folded cascode DTMOS based two-stage amplifier stage with miller compensation.

Because it is a two-stage amplifier, each gain stage produces a "dominant" pole, so the stability of the feedback system with multiple stages of points is crucial. The phase margin value can assess whether a multi-pole system is in an open-loop stable condition, so having a phase margin greater than 60° in the open-loop amplifier design can provide a more stable system [17]. Fig. 4.3.4 illustrates the two-stage folded-cascode amplifier with miller compensation. The miller capacitor is connected at the output of the first and second stages, pushing the dominant pole toward the lower frequency and the second dominant pole toward the higher frequency[31].

Fig. 4.3.5 shows the frequency response characteristics of the open-loop amplifier. Before Miller compensation, the phase margin was inferior due to the proximity of the two poles. After pole splitting, the phase margin reaches 70°. It can be observed that the open-loop gain

reaches 62dB and the phase margin achieves 70° because the right half-plane zero is pushed away from the unity-gain bandwidth. Hence, no compensation resistor, the chip area is saved.

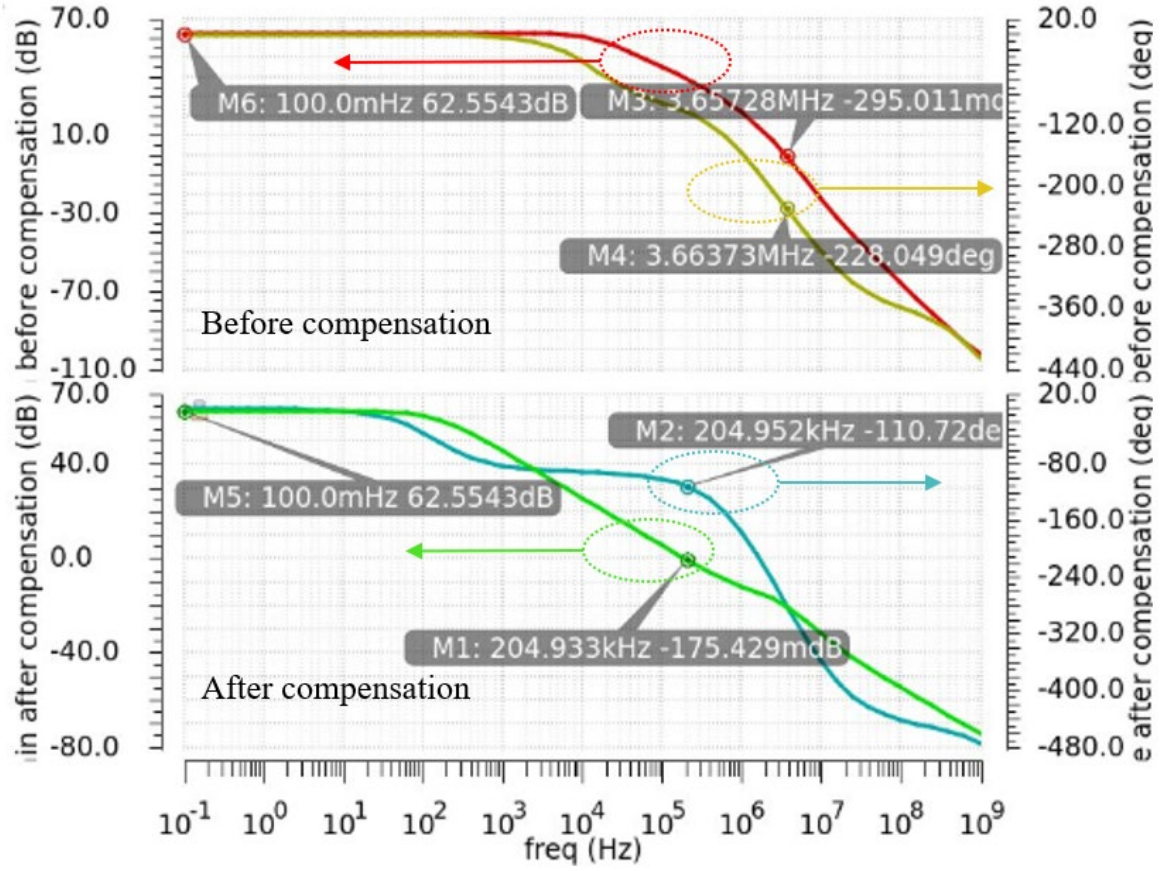

Fig. 4.3.5 Bode plot of open-loop DTMOS based two-stage amplifier before and after Miller compensation.

4.3.3 The chopper switch implementation

In chapter 3, the chopper switch has been introduced, this section will focus on how the chopper switch is implemented in the amplifier system. Fig. 4.3.6 illustrates the implementation of a conventional chopper amplifier. In the overall system, the first modulator is implemented before the first stage amplifier to modulate the input signal. After the signal passes through the second stage amplifier, it is demodulated back to the baseband. The drawback associated with

this structure is also obvious because the input signal and noise are simultaneously modulated to high frequencies and amplified. The amplification of noise is undesired, so the improved network is shown in Fig. 4.3.7.

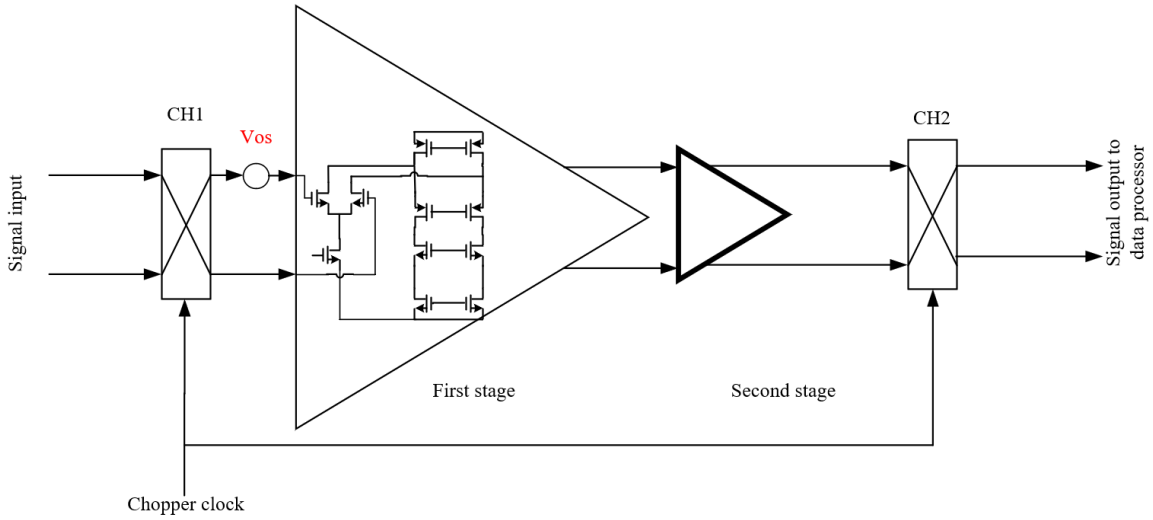

Fig. 4.3.6 Conventional chopper amplifier implementation.

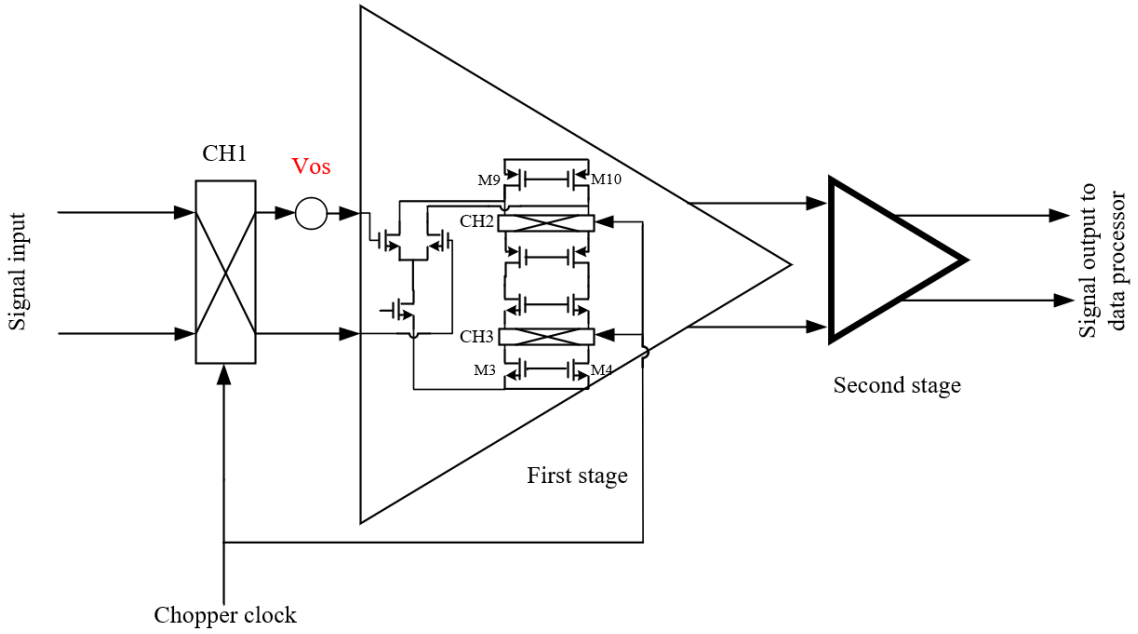

Fig. 4.3.7 Improved chopper amplifier implementation.

Improved chopper amplifier structure consists of three chopper switches[32]. Similarly, the first modulator CH1 is implemented at the input of the first stage amplifier, the output demodulator CH2 is implemented at the drain terminal of the PMOS current source M9, M10, while the NMOS current source M3, M4 also has an extra chopper switch to generate matched spikes. Due to the demodulator CH2 is chopping the current at the output, hence the chopped signal maintains large bandwidth and effective gain[33]. The desired signal is demodulated back to the baseband before the second stage amplifier, so the second stage amplifier does not amplify the modulated noise anymore. In summary, this structure provides better matching, lower noise, and greater signal bandwidth.

The charge injection mismatch in the signal path mainly contributes to the DC errors such as residual offset[34]. Therefore, in Fig. 4.3.7, the chopper CH1 and CH2 are two signal path modulators placed between amplifier I/O. The previous section introduces the clock-boosting switch that simultaneously improves on-state performance and reduces leakage. It reduces the effect of residual offset by lowering the switching threshold voltage at on-state. The residual offset voltage contributed by CH1 is defined as

$$V_{res,OS1} = \frac{2f_{CH}(|\Delta q|)}{\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})} \tag{4.3.11}$$

where f_{CH} is chopping frequency, and Δq is charge injection mismatches causes by four switches. The residual offset is proportional to the chopping frequency f_{CH}. Large f_{CH} needs smaller capacitance of clock boosting switch, occupying smaller area but larger residual offset, the f_{CH} trade-off will discuss later. By decreasing switch on-state V_{TH} of up-modulator CH1, the residual offset can be reduced. The residual offset voltage contributed by CH2 is defined as

$$V_{res,OS2} = \frac{2f_{CH}(|\Delta q|)}{g_m} \tag{4.3.12}$$

Where g_m is the first stage transconductance. DTMOS improved g_m of the folded-cascode stage, the output chopper CH2 contributes less residual offset. As indicated in the equation, smaller chopping frequency, and smaller charge injection mismatch leads to a total residual offset significant reduction.

4.4 The rail-to-rail common-mode feedback

In section 4.3, we have introduced the DTMOS-based 0.4V two-stage fully differential folded-cascode amplifier. A common-mode feedback circuit is needed to make the output common-mode level stable for a two-stage differential amplifier. The basic principle of common-mode feedback is shown in Fig. 4.4.1, where the conventional common-mode feedback consists of two sense resistors and an amplifier[35]. The sensing resistors need to be sufficiently large enough, specifically, much larger than the output impedance, to avoid the reduction of open-loop gain[17]. Next, the error amplifier compares the common-mode level with the reference voltage and returns the error value to the gate of the amplifier's current source.

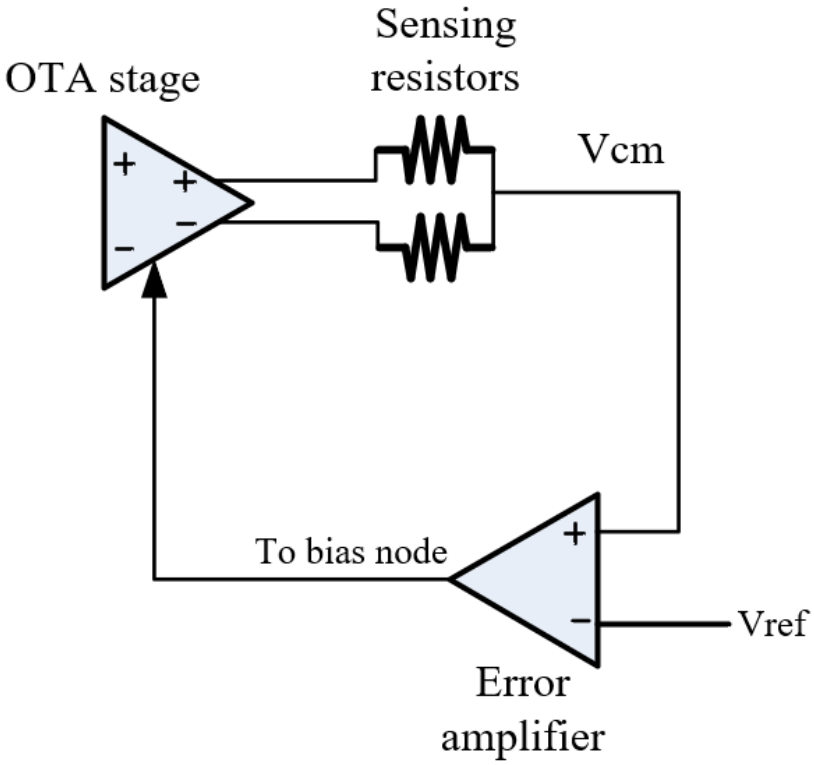

Fig. 4.4.1 Principle of the common-mode feedback circuit.

In this application, the maximum supply voltage is 0.4V, severely limiting the signal swing and leading to a degradation of the signal SNR. Usually, the bio-signal itself is so weak that the amplification signal swing at a higher voltage supply is not a big concern. However, at sub-0.4V supply voltages, the amplified physiological signal may have exceeded the circuit's limits, distorting the signal. Therefore, it is a new approach to improve SNR and output signal quality by rail-to-rail output CMFB. The idea of rail-to-rail common-mode feedback is shown in Fig. 4.4.2, the circuit is formed of a sensing circuit and an error amplifier circuit[36].

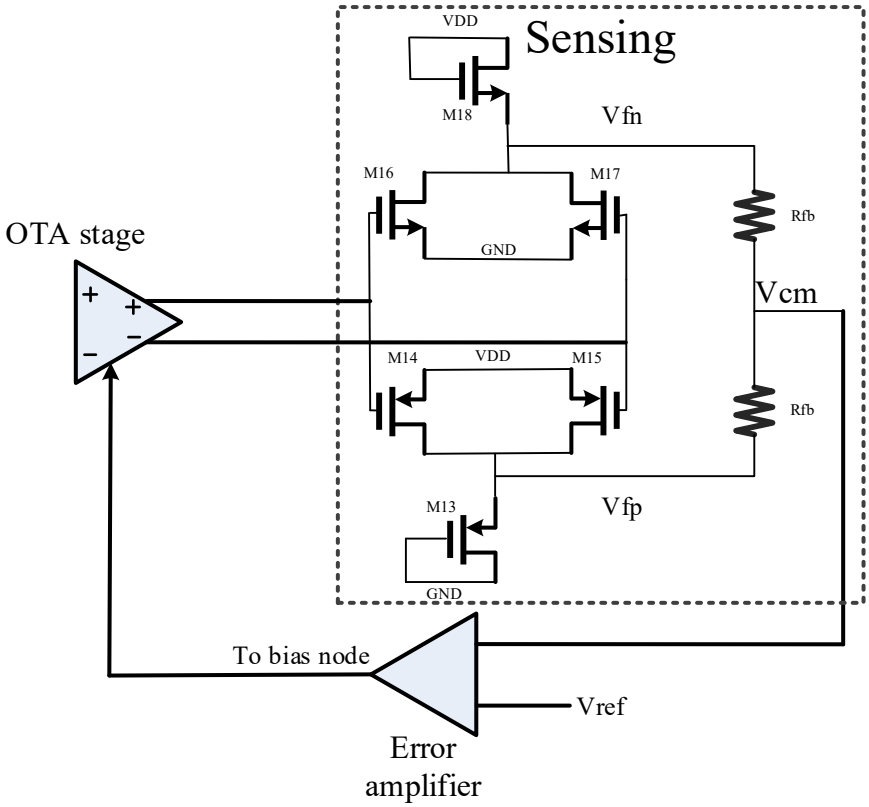

Fig. 4.4.2 The principle of the rail-to-rail common-mode feedback circuit.

This circuit consists of six transistors and two sensing resistors. M14-M17, as input pair transistors receive the output signal from the OTA stage. M13 and M18, as diode-connected load transistors. Unlike typical common-mode feedback with resistive sensing, due to the sensing resistor isolated OTA stage, the resistance does not need to be much greater than the output impedance of the OTA stage. The conventional sensing resistence (Fig. 4.4.1) needs to mach larger than folded-cascode (Fig 4.3.3) output impedance

$$R_{sensing} \gg \left[[g_{m8}r_{o8}(r_{o1} \parallel r_{o10})] \parallel (g_{m6}r_{o6}r_{o4})\right] \tag{4.4.1}$$

and the rail-to-rail sensing resistors (Fig. 4.4.2) is only

$$R_{fb} \gg \left((r_{o16} \parallel r_{o17}) \parallel r_{o18}\right) \tag{4.4.2}$$

It is apparent rail-to-rail sensing resistance can be much smaller than conventional sensing resistance. For NMOS sensing network M16-18, when the detected OTA output common-mode voltage increase, leads to the more current flow of M16-M18, and Vfn will be scaled down[36]. The node voltage V_{CM} can be defined as:

$$V_{CM} = \frac{V_{fn} + V_{fp}}{2} \tag{4.4.3}$$

Vice versa, the same discussion can be done by the complementary PMOS sensing circuit.

Assume

4.5 Closed-loop instrumentation amplifier.

So far, the open-loop amplifier has been introduced, and the bio-signal acquisition system requires the application of this open-loop amplifier to the closed-loop feedback circuit. In chapter 2.1, we have discussed that amplifier circuits based on resistive feedback loops rely heavily on matching. Therefore, it is better to choose capacitive feedback. The principle of AC-coupled closed-loop IA shows in Fig. 4.5.1. The high-pass frequency can be given by

$$f_{highpass} = \frac{1}{2\pi C_f R_f} \tag{4.5.1}$$

And the closed-loop gain given by

$$A_v = \frac{C_{in}}{C_f} \geq 40dB = 100 \tag{4.5.2}$$

When the gain of the amplifier is equal to 40dB which is the minimum requirement of this system, and the corner frequency is in the range of several to several tens of Hz, the value of the feedback capacitor roughly around several hundreds of fF to a couple of pF, and the feedback

resistor usually require the value of $G\Omega$. Which is tremendous for SoC, not easy to matching and integrate on the chip either. Hence, here we should use the large on-chip resistor.

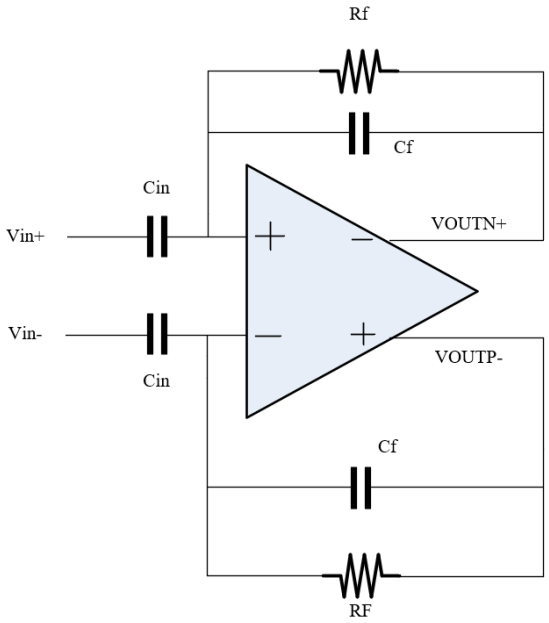

Fig. 4.5.1 Circuit schematic of the conventional AC-coupled closed-loop IA.

4.5.1 Pseudo-resistor

Pseudo-resistor is a way to achieve large on-chip resistors composed of diode-connected MOSFET and are usually placed back-to-back with two diode-connected MOSFETs to increase resistance further and reduce distortion (Fig. 4.5.2) [7]. Fig. 4.5.3 illustrates the effect of different W/L ratios on the resistance value. Fig. 4.5.4 shows that the resistance for varies voltage across Vi and Vo.

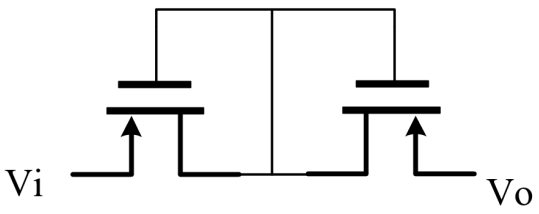

Fig. 4.5.2 Back-to-back pseudo-resistor.

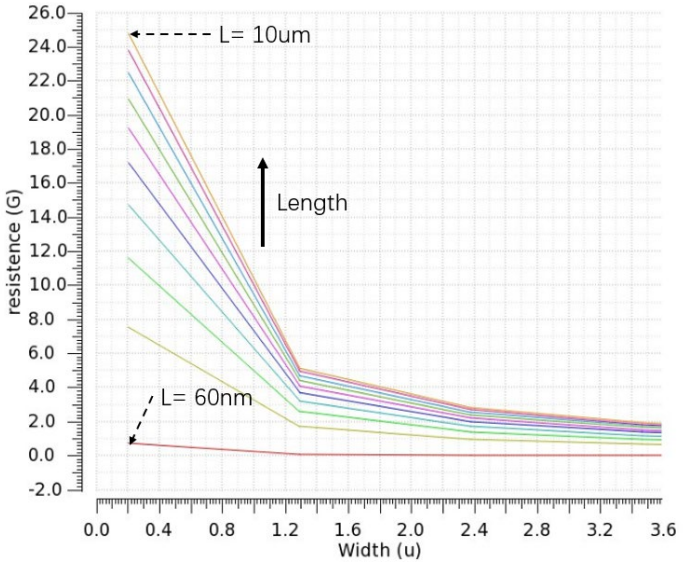

Fig. 4.5.3 Simulated resistance for varies W/L ratio.

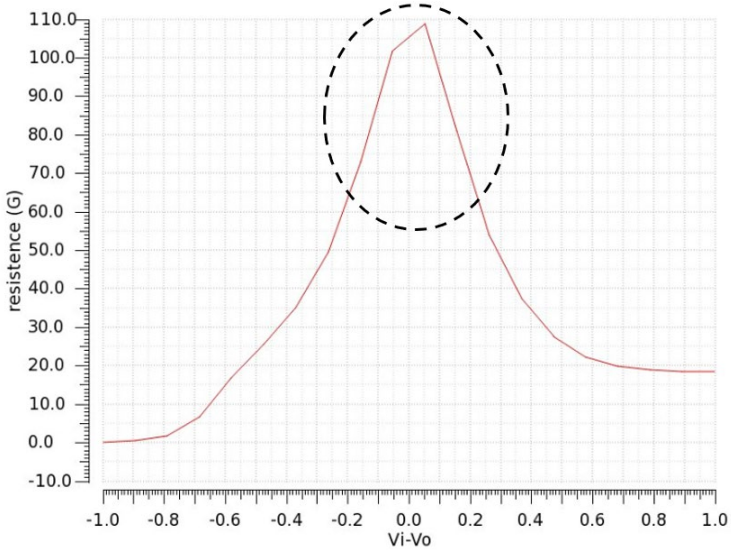

Fig. 4.5.4 Simulated resistance for various voltages across Vi and Vo.

It can be observed that we should increase the channel length and decrease the width as much as possible. When Vi and Vo are close to each other, the on-stage resistance reaches its maximum value, which can exceed $100G\Omega$.

4.5.2 Closed-loop chopper amplifier for the acquisition system.

Fig. 4.5.5 shows the amplifier of the physiological signal acquisition system. The amplifier uses the capacitive feedback network to increase the input impedance and reasonable capacitance matching. Because the capacitor is an AC-coupled device, the amplifier needs to be driven by a bias voltage, the bias circuit is designed by on-chip pseudo-resistors through an off-chip bias voltage. The input noise current of the pseudo-resistor is given by

$$i_{noise}^2 = \frac{4KT}{R_{pseudo}} \tag{4.5.3}$$

And input-referred noise can be written as follow

$$V_{in}^2 = \frac{4KT}{R_{pseudo}} * R_{in} \tag{4.5.4}$$

In the previous section, we have described the ability of pseudo-resistors to provide tremendous on-chip resistance. From Eq. 4.5.4, we can find that the input noise is inversely proportional to the resistance of the pseudo-resistor. Therefore, the enormous resistance can lead to a much smaller flat band. Afterward, the signal entered the DTMOS based folded-cascode amplifier and demodulated back to the baseband before filtering by the dominant pole. Next, the signal hit the second stage amplifier with Miller capacitor compensation to the output node. The negative feedback loop consists of feedback capacitors and another chopper switch.

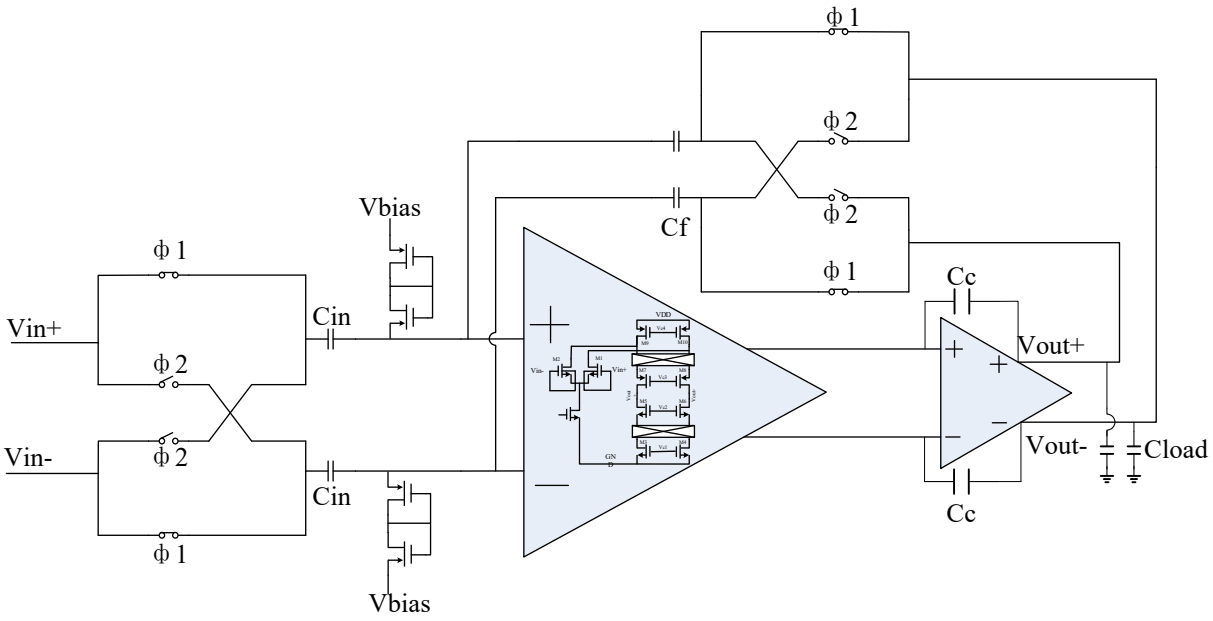

Fig. 4.5.5 Circuit schematic of physiological signal acquisition amplifier.

The amplifier takes the benefits of capacitor feedback, the input resistance has been significantly improved (Eq. 4.5.5). The electron charge is given by

$$Q = C_{in} * V_{in} \tag{4.5.5}$$

In one clock cycle, the capacitor is charged twice, in other words, the period used to charge capacitor Cin once fully is T/2. Therefore, the current consumption for charging capacitor Cin is given by

$$I = \frac{2Q}{T} = 2Q * f_{chop} = 2C_{in}V_{in}f_{chop} \tag{4.5.6}$$

And input impedance can be written as

$$R_{in} = \frac{V_{in}}{I} \approx \frac{1}{C_{in}f_{chop}} \tag{4.5.7}$$

Usually, the high input impedance is desired, and it can be observed that large input impedance requires smaller C_{in} and f_{chop}. From Eq. 3.2.8, the chopping frequency needs to be well above the corner frequency of the signal and well below the open-loop gain bandwidth of the amplifier. Fig. 4.5.6(a) shows an AC-coupled closed-loop amplifier input-referred noise, the flicker noise corner is located in the range of 100-3KHz. Considering from the perspective of input resistance, we desire lower chopping frequency, however, low frequency makes the area of the clock boosting circuit larger, and slower clocks require larger capacitors to maintain on-state gate voltages (Fig. 4.5.6(b)). To trade-off the area of the circuit and the input resistance, the chopping frequency was chosen to be 50kHz.

Moreover, the amplifier closed-loop gain is given by

$$A_v = \frac{C_{in}}{C_f} \tag{4.5.8}$$

Considering that Cin has to be much larger than Cf and the Cf cannot be too small, the value of Cf is 200fF, and Cin is 20pF. The size of the pseudo-resistor is 10um in length and 200nm in width. The capacitance value of Cc is 1.04pF to provide a sufficiently large phase margin.

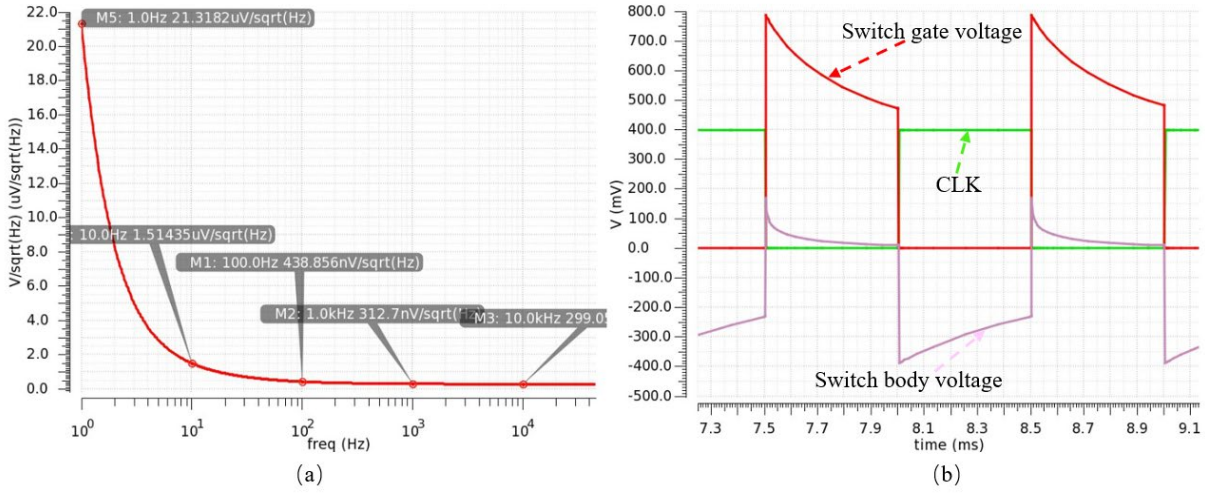

Fig. 4.5.6 (a) AC-coupled amplifier before chopping. (b)Lower chopping frequency leads to capacitor hold voltage fails.

The input-referred noise at the flat band is mainly contributed by the folded-cascode stage (Fig. 4.3.4), the pseudo-resistors, and the output stage. And it can be defined as

$$\overline{V_{n,in}^2} = 4\frac{4KT}{R_{pseudo}}\frac{1}{C_{in}f_{chop}} + \left[8kT\left(\frac{2}{3g_{m1,2}} + \frac{2}{3}\frac{g_{m3,4}}{g_{m1,2}^2} + \frac{2}{3}\frac{g_{m9,10}}{g_{m1,2}^2}\right) + \left(\frac{\frac{16kT}{3}(g_{m12}+g_{m13})}{\left[g_{m1}g_{m12}[[g_{m8}r_{o8}(r_{o1}\|r_{o10})]\|(g_{m6}r_{o6}r_{o4})]\right]^2}\right)\right] * \frac{C_{in}}{C_f} \quad (4.5.9)$$

as indicated in the equation, the pseudo-resistor thermal noise can be written as a multiplier noise current and input resistance. The sum of the thermal noise contributed by the first stage and the second stage needs to be multiplied by the closed-loop gain of IA for reference to the IA input terminal. In low noise design, large pseudo-resistors, high chopping frequency, and larger input pair transconductance are desirable.

The output SNR equals the ratio of signal power to noise power which is given

$$SNR_{out} = \frac{\left(\frac{V_{in}\left(\frac{C_{in}}{C_f}\right)}{\sqrt{2}}\right)^2}{\overline{V_{out,total}^2}} \quad (4.5.10)$$

where the numerator of the formula is the equivalent signal at the output of a sinusoidal signal of amplitude V_{in}. And $\overline{V_{out,total}^2}$ is integrated in-band RMS noise. A larger input signal swing and less in-band noise are desired to get a higher quality signal before the amplified signal hits the data processor. Again, in the sub-0.4V application, the output signal swing is severely limited by

the power supply voltage. Hence, the IA has rail-to-rail output swing becomes a significant design factor.

4.6 Overall system

The previous section introduces the closed-loop amplifier used for physiological signal acquisition, and so far, we have described the complete system and its auxiliary circuit modules. The entire system contains a non-overlapping clock generator, clock boosting circuits, a biasing network, a four transistors bandgap, and a CMFB circuit for each stage. The principle of the complete system is shown in Fig. 4.6.1.

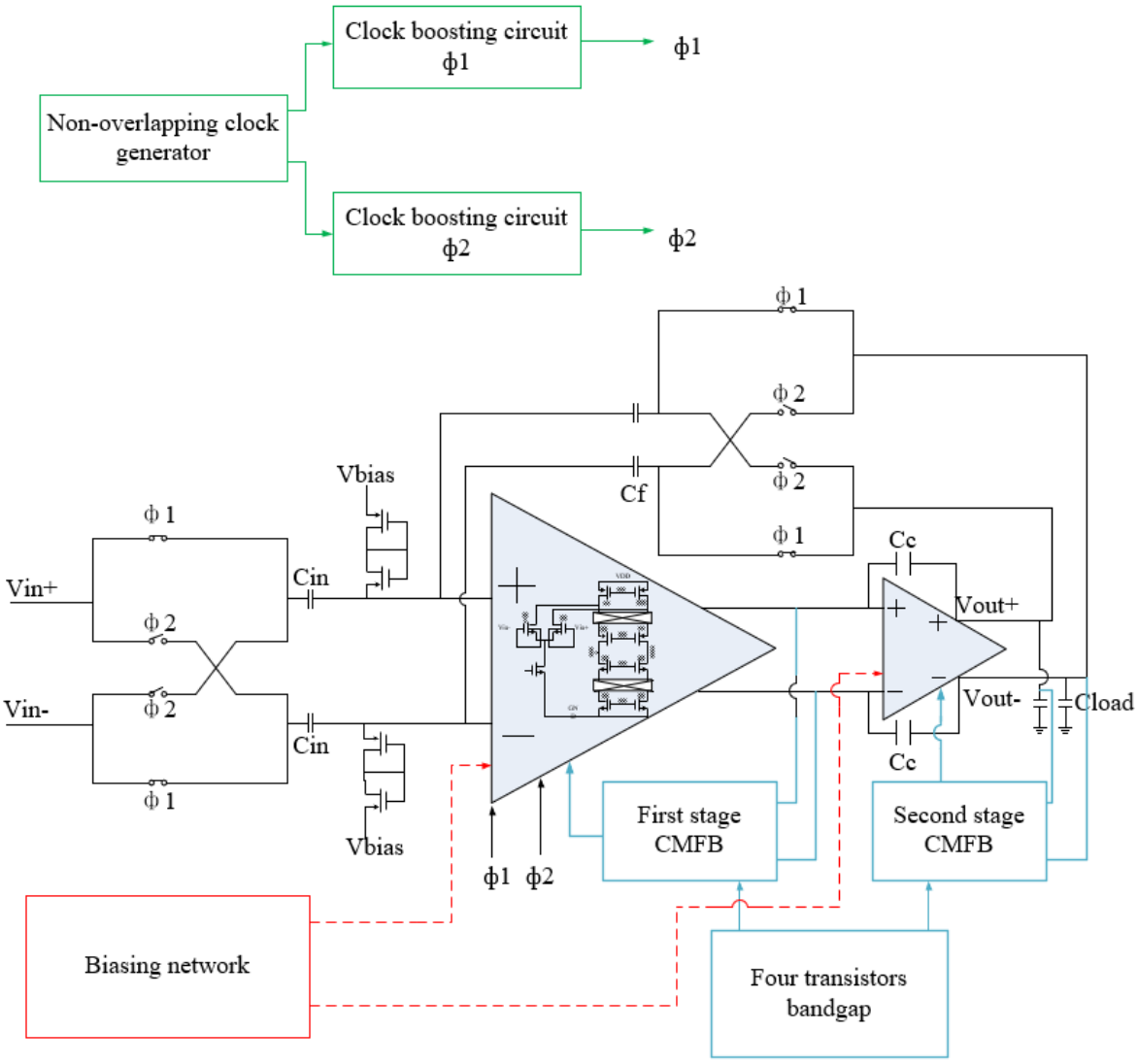

Fig. 4.6.1 Schematic diagram of the physiological signal acquisition system.

Non-overlapping clocks are generated by cross-coupled RS flip-flop (Fig. 4.6.2). The flip-flop consists of two NAND gates and five inverters, the principle is to use D-latch and buffers so that the two clock signals do not overlap each other. The TSMC65nm IP block generates the NAND gates and inverters.

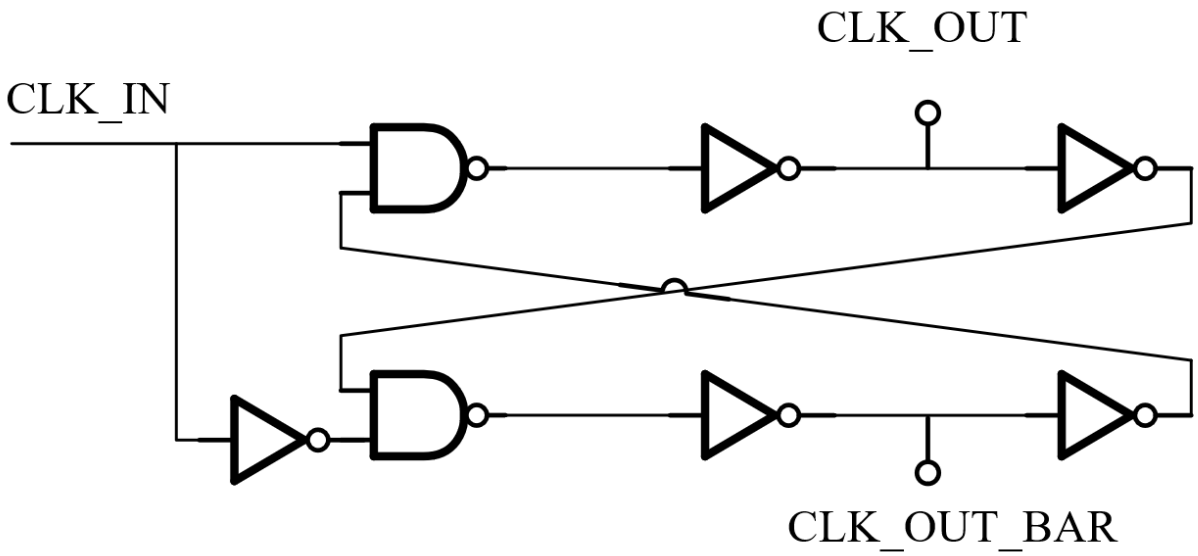

Fig. 4.6.2 Circuit schematic of the cross-coupled RS flip-flop.

Then, the two non-overlapped clock signals hit the clock-boosting switch circuit. And $\phi 1$ and $\phi 1$ are two boosted non-overlapping clock signals to drive the chopper modulator switch. The circuit schematic has been shown in chapter 3.1.3.1, the boosted clock signals and improved bulk signal are shown in Fig. 4.6.3.

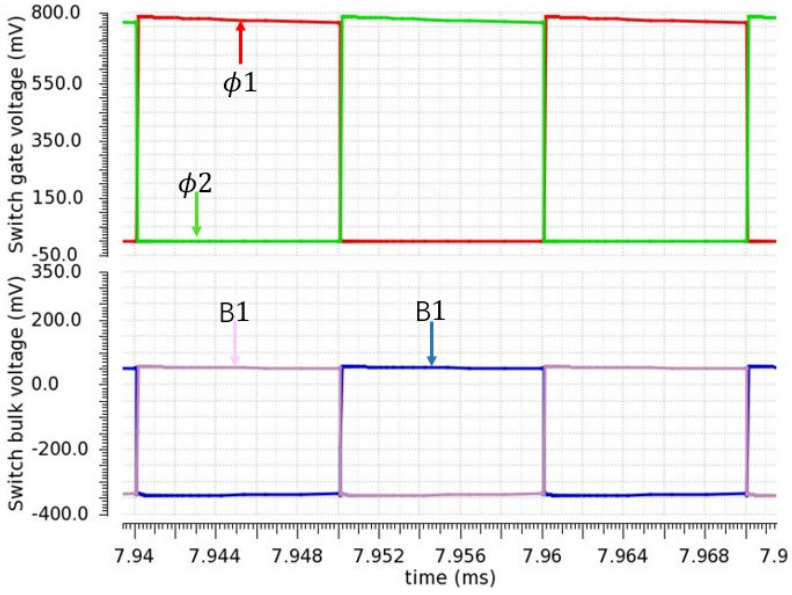

Fig. 4.6.3. The boosted clock signal and improved bulk signal.

Fig. 4.6.4 and Fig. 4.6.5 show the CMFB circuit and its DC operating point for the first and second stages.

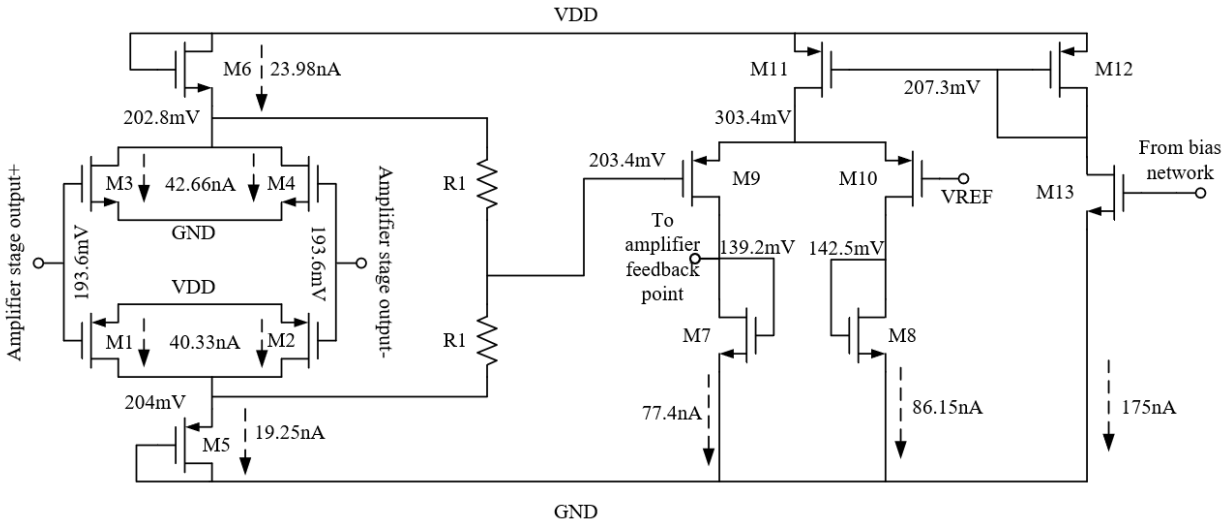

Fig. 4.6.4 Circuit schematic of the first stage CMFB and its DC operating points.

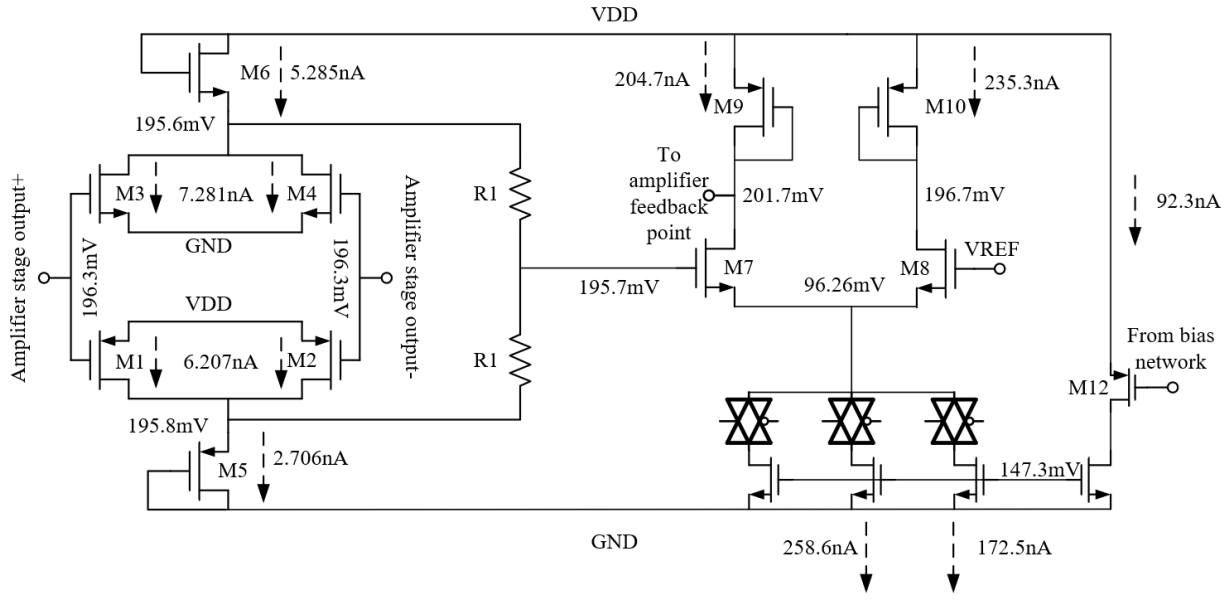

Fig. 4.6.5 Circuit schematic of the second stage CMFB and its DC operating points.

Again, the CMFB circuit consists of a sensing network and an error amplifier. The second stage CMFB circuit using the trimming technique to tuning the process corner of the second stage due to sensitivity.

Fig. 4.6.6 shows the amplifier stage and error amplifier bias circuit and its DC operating points.

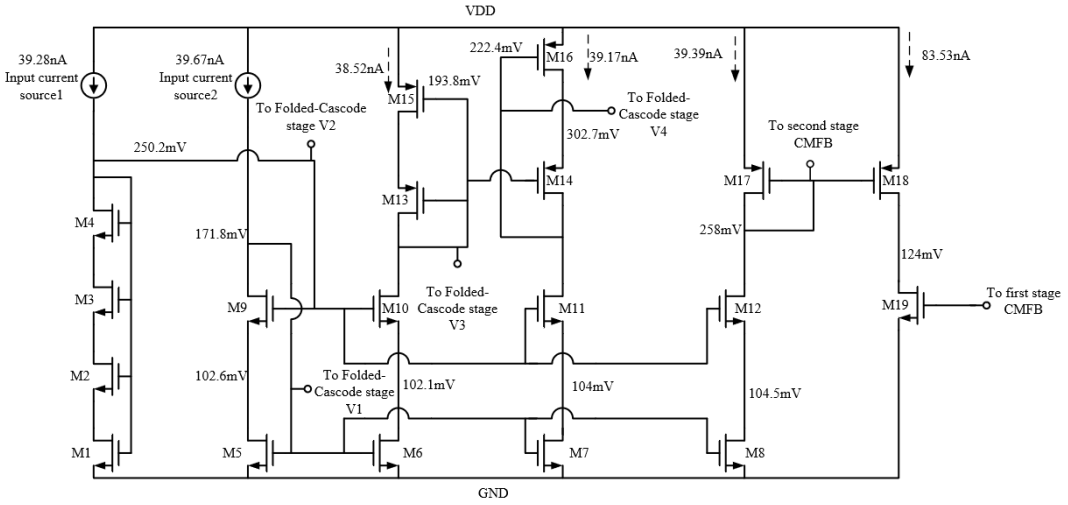

Fig. 4.6.6 Biasing network and its DC operating points.

The main stage of the amplifier and its DC operating point shows in Fig. 4.6.7.

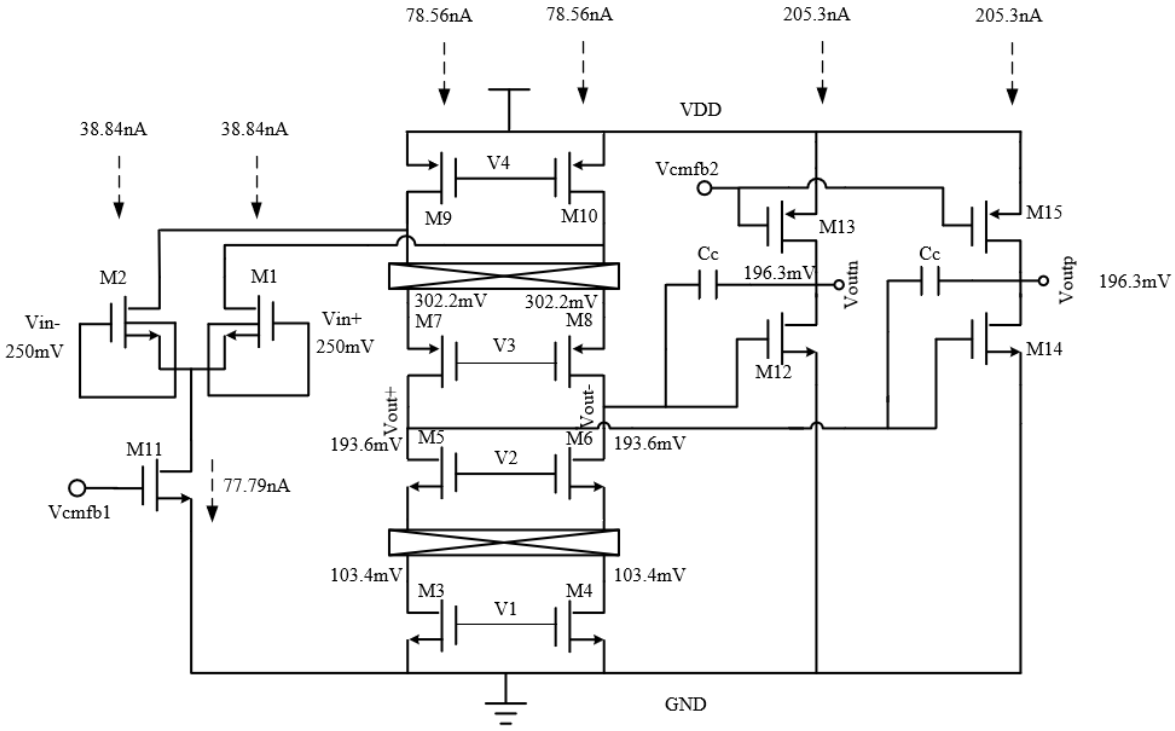

Fig. 4.6.7 DTMOS-based fully differential two-stage folded-cascode amplifier and its DC operating point.

Fig. 4.6.8 shows the four transistors bandgap and its DC operating points.

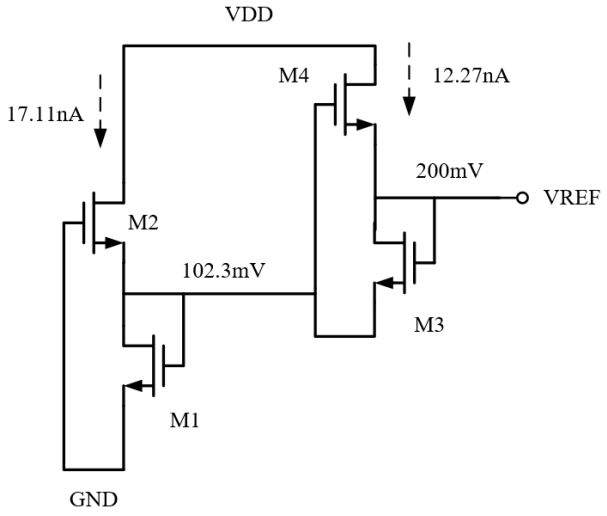

Fig. 4.6.8 Circuit schematic of four transistors bandgap and its DC operating points.

CHAPTER 5: LAYOUT CONSIDERATION AND POST-LAYOUT SIMULATION RESULTS

The circuit in this chapter was designed based on TSMC 65nm CMOS process, layout designed and simulated using Cadence Layout Editor. Symmetry and noise issues are fully considered in the layout design. Especially for deep N-well input pair, because each input MOSFET has a local body voltage, using ABBABAAB layout method consume a larger chip area than the common-centroid method. Chopper switch using common-centroid layout to reduce the switching spike. Filling the rest of the area with decoupling capacitors mitigates circuit instability caused by fluctuation in supply voltage. Fig. 5.1 shows the amplifier core layout.

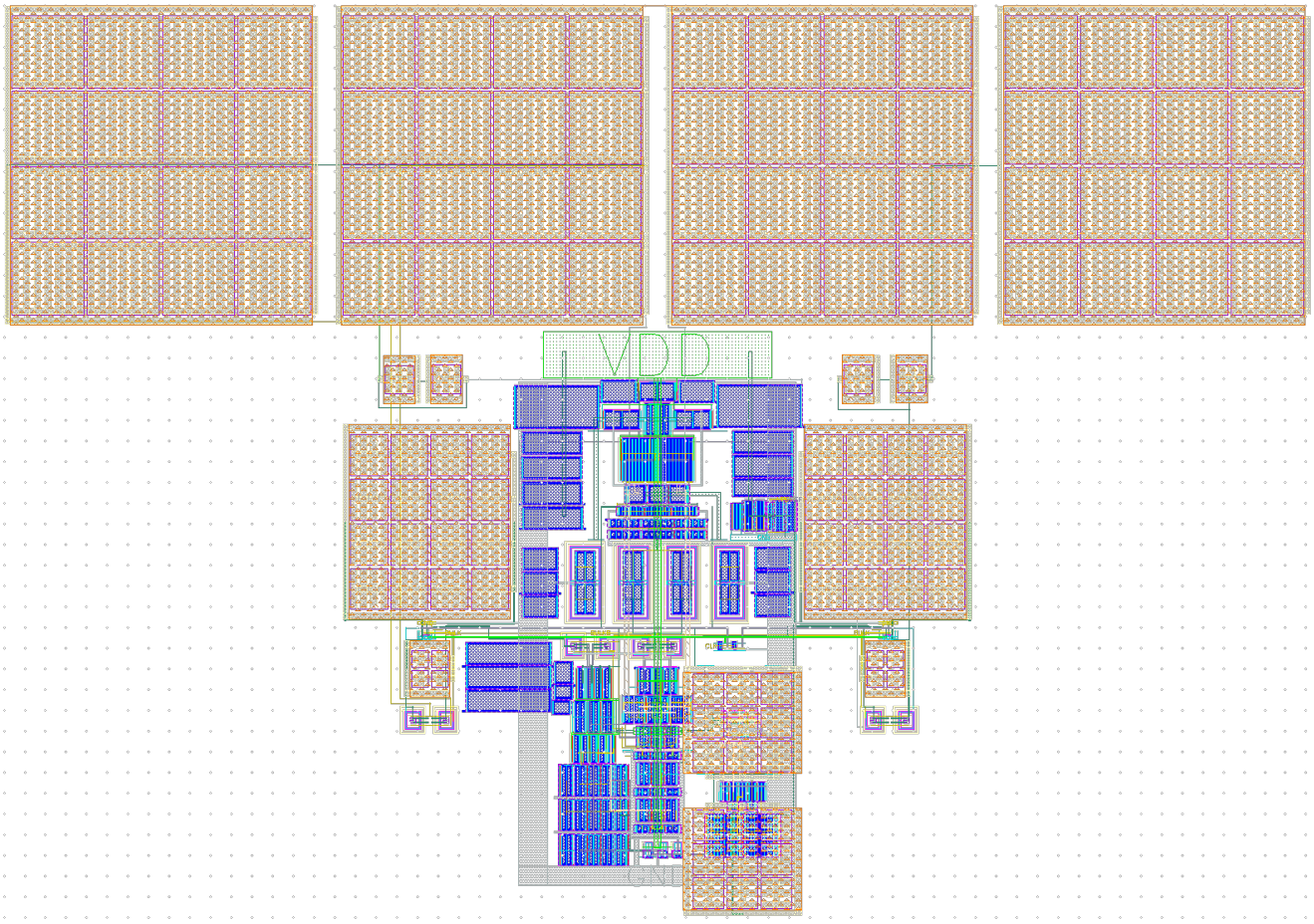

Fig. 5.1 Amplifier core layout.

The chapter presents the designed IA post-layout PSS, PAC, and Pnoise simulation. The simulated results show that the circuit consumes 2.02uA at 0.4V supply voltage, and the total power consumption is 0.808uW, which achieves low power requirements.

The post_layout simulation of this circuit at the tt corner achieves 44.9dB closed-loop gain, 2.08KHz cut-off frequency with 490kHz unity-gain bandwidth (UGBW. Because of the parasitic capacitors and resistors, the bandwidth is reduced but greater than the desired signal bandwidth. Compare to pre-simulation, 45.02dB gain with 2.19kHz cut-off frequency and 521.8KHz UGBW (Fig. 5.2). After chopping, the input-referred noise is shown in Fig. 5.3.

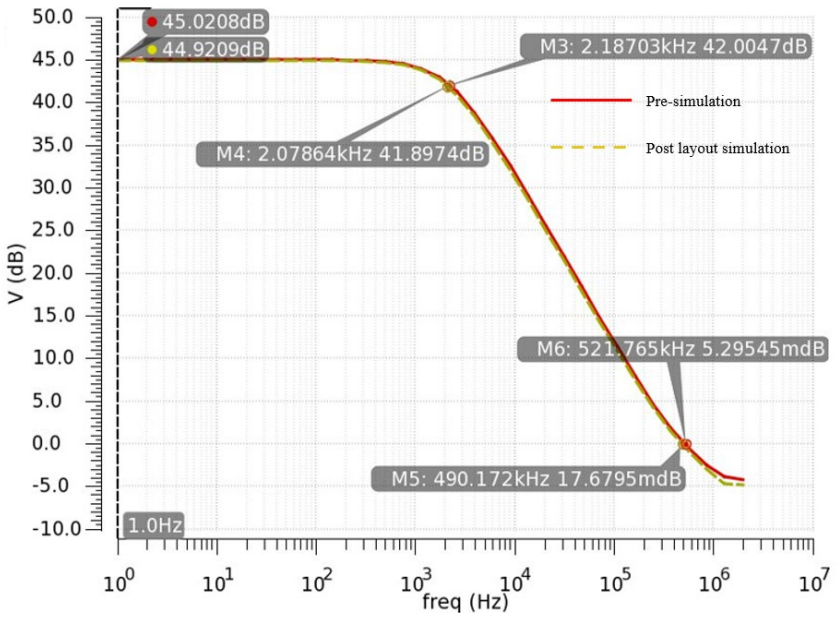

Fig. 5.2 Amplifier closed-loop gain at tt corner.

The pre and post-layout simulation results are shown in Fig. 5.3, and intput-referred noise is about 5% different caused by the CMFB symmetry issue. The post-layout simulation shows flat band input-referred noise is $140nV/\sqrt{Hz}$ with 30Hz flicker noise corner. And in band integrated noise is 5.8uVrms.

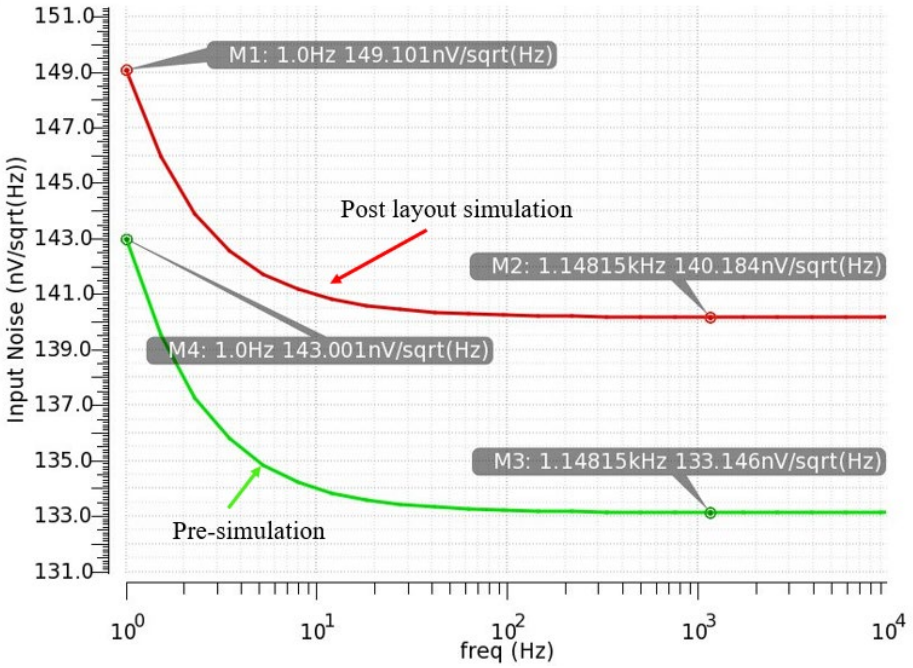

Fig. 5.3 Input referred noise Pre. and post-layout after chopping.

Fig. 5.4 and Fig. 5.5 show the post-layout simulation of CMRR and PSRR, respectively. The CMRR can reach 103dB, with 80dB PSRR. (200 Monte-Carlo simulated points)

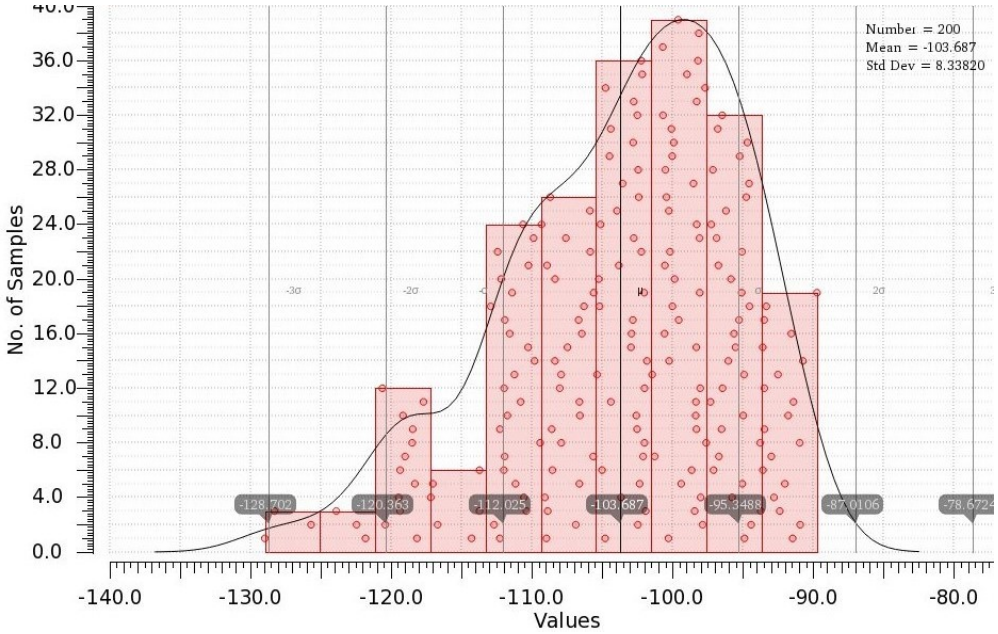

Fig. 5.4 Monte-Carlo simulation of CMRR.

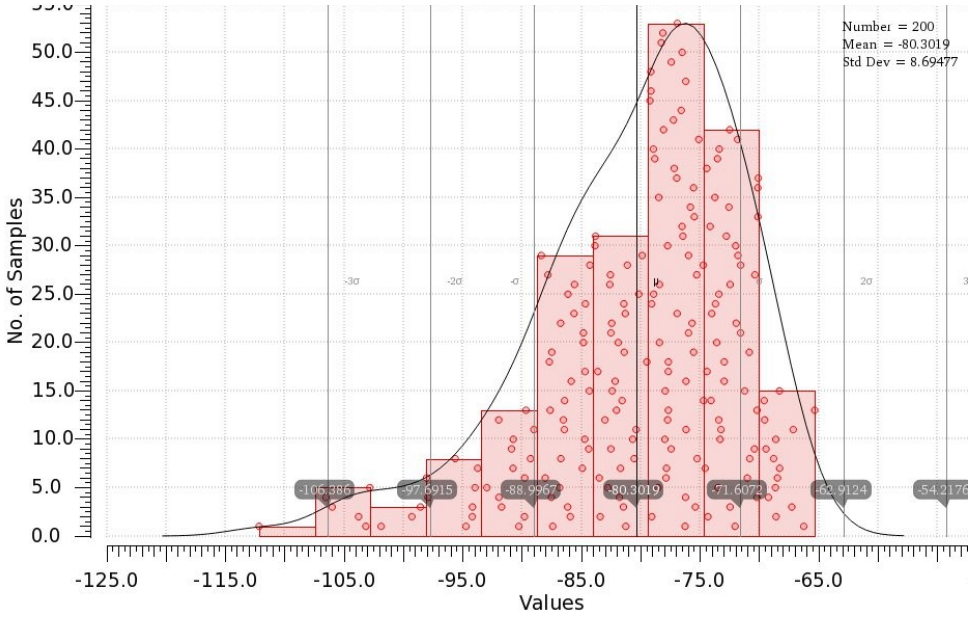

Fig. 5.5 Monte-Carlo simulation of PSRR.

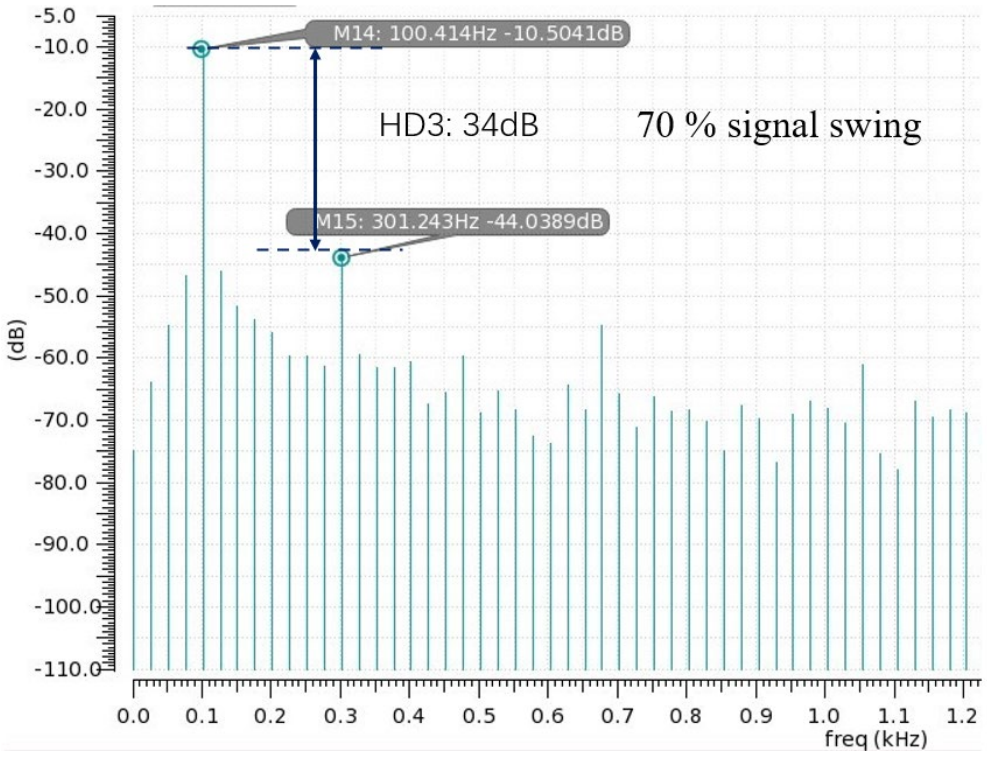

Fig. 5.6 Post_layout simulation of third harmonic distortion.

The third harmonic distortion can evaluate the linearly of the system. Fig. 5.6 shows third harmonic distortion (HD3), where HD3 achieves 34.5dB with 70% signal full swing. Fig. 5.7 shows the frequency response of the amplifier at different temperatures. The worst case is 39dB at 80°. The amplifier gain for various process corners is shown in Fig. 5.8. As you can see, the worst case is 39dB gain at 80° and 42.9dB gain at the ff process corner. Fig. 5.10 shows designed IA DTNMOS input pair transconductance efficiency compare to conventional NMOS input pair.

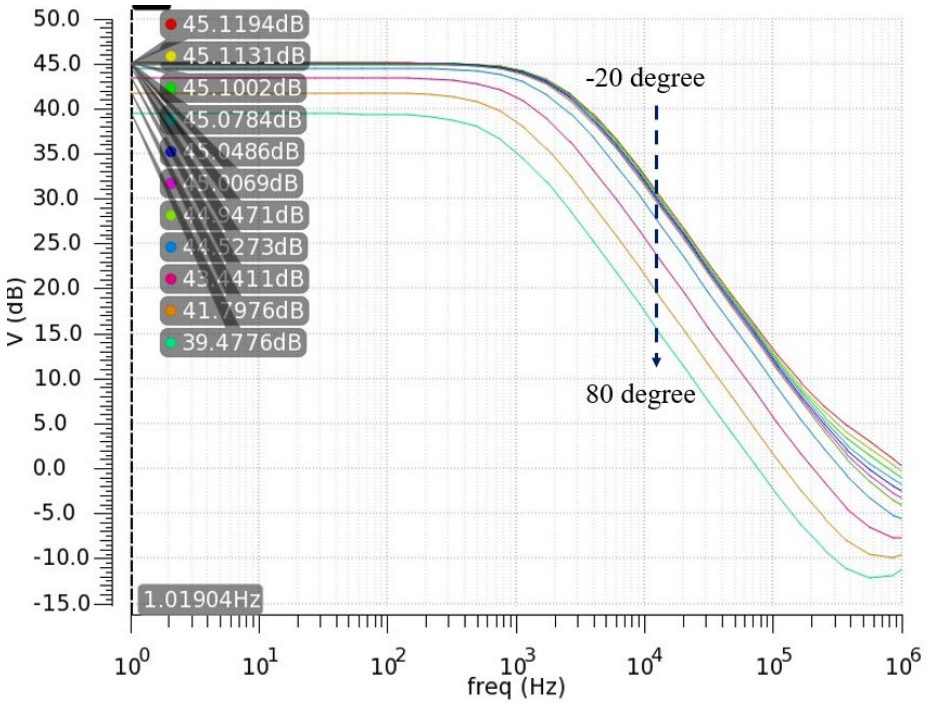

Fig. 5.7 Frequency response of the closed-loop IA at -20 to 80°.

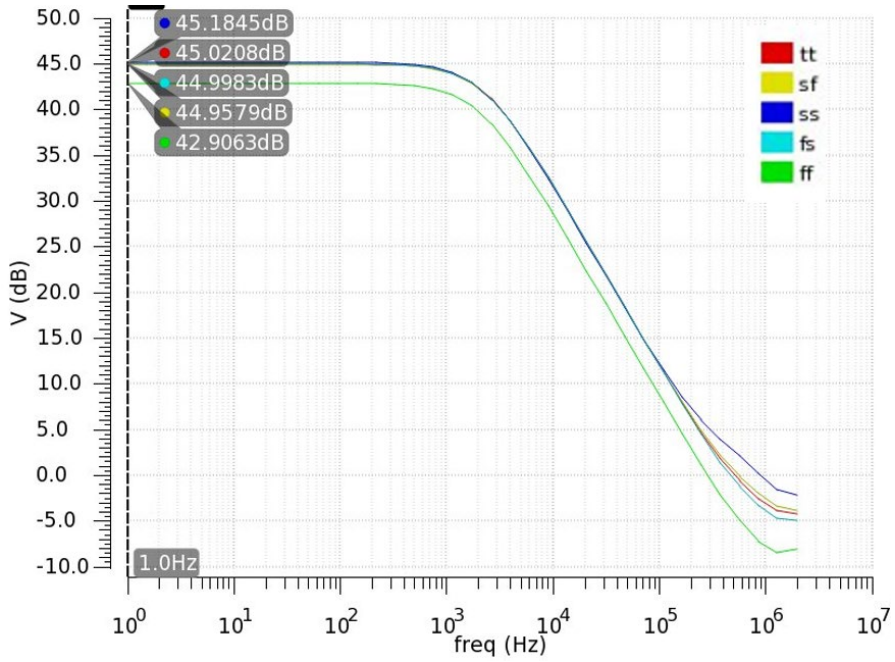

Fig. 5.8 Frequency response of the closed-loop IA at different process corners.

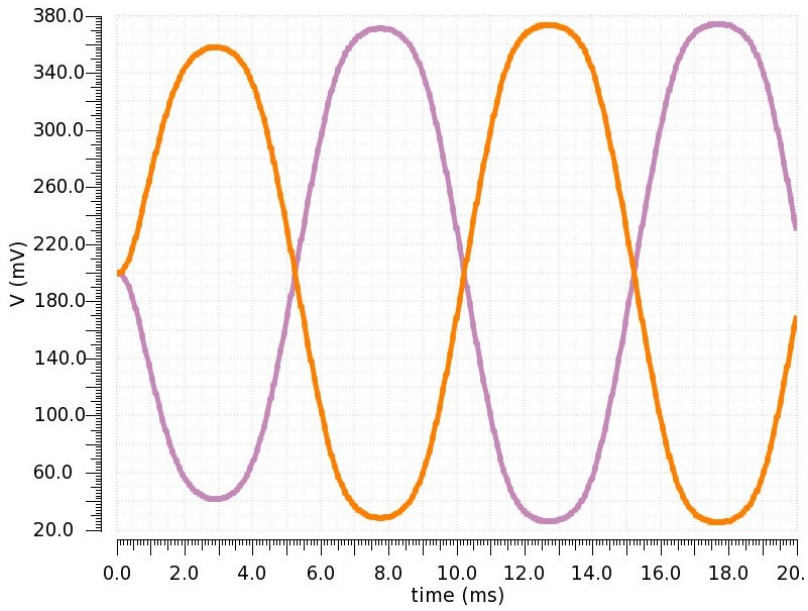

Fig. 5.9 Rail-to-rail output signal of designed IA

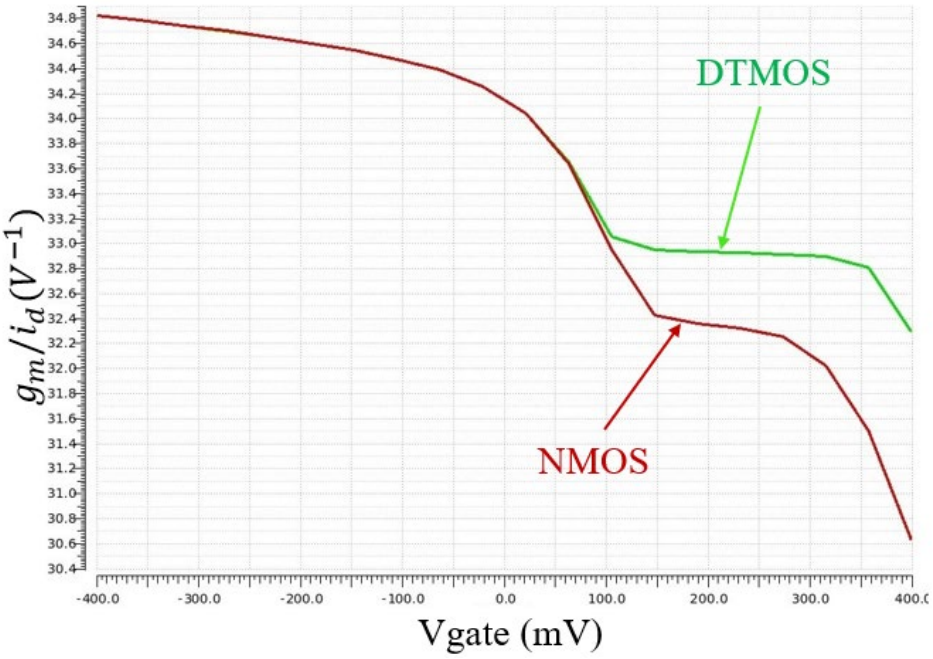

Fig 5.10 DTMOS and NMOS transconductance efficiency of designed IA (input pair).

The noise efficiency factor (NEF) and power efficiency factor (PEF) can be used to evaluate the efficiency of the amplifier, and the NEF and be defined as

$$NEF = V_{RMS}\sqrt{\frac{2I_{total}}{4kT * \pi * V_T * BW}} \tag{5.1}$$

And PEF can be defined as

$$PEF = \frac{2 * V_{RMS}^2}{4kT * \pi * V_T * BW} * P_{total} \tag{5.2}$$

Where V_{RMS} is the in-band integrated input-referred noise, V_T is the thermal voltage, BW is the efficive bandwidth of the amplifier. P_{total} and I_{total} are the total current and total power consumption. The system NEF is 7.27, and PEF is 21.16.

	[37]	[38]	[9]	[39]	[40]	This work

Process	40nm	180nm	28nm	130nm	65nm	65nm
Supply (V)	1.2	1.5	0.9	1.2	0.5	0.4
Area(mm^2)	0.071	0.013	1.14	0.3	0.025	0.06
Gain(dB)	26	47.6	106	40	27	45
BW(Hz)	150	0.5-500	5	0.6-2k	1-5000	2100
IRN (nV/$\sqrt{Hz}$)	130	120	27	47	58	140 @100Hz
Integr. IRN (uVrms)	1.3	2.24 (0.5-500Hz)	2.2	NA	NA	5.8 (0.1-2070)
CMRR (dB)	60	105.6	70	85	NA	103
PSRR (dB)	NA	NA	68	NA	NA	78
Rail-to-Rail	no	no	Input	No	No	Output
NEF	NA	2.91	8	3.9	4.76	7.27
Total Current (uA)	2.92	0.57	14.4	2.9	3.5	2.02
Power (uW)	3.5	0.855	26/72	3.48	3.5	0.8

Table 5.1 The performance of the IA designed in this paper compared with other works.

CHAPTER SIX: CONCLUSION AND FUTURE WORK

With the progress and development of technology, the instrumentation amplifier will become more and more widely used in the future. Unlike general-purpose amplifiers, instrumentation amplifiers need to be highly customized to meet the needs of low noise and high accuracy without performance overflow. Therefore, the study of instrumentation amplifiers of bio-signal acquisition systems is meaningful. And as time goes on, the noise and power consumption from the changes in its structure will become lower and lower. The IA designed in this paper, using TSMC 65nm process, consumes only 0.8uW of power at an ultra-low supply voltage of 0.4V, achieves 45dB gain, DC-1.9KHz bandwidth, 133$nV/\sqrt{Hz}$ (@100Hz) input-referred noise with 103dB CMRR and 80dB PSRR. The HD3 is 34dB, and the NEF can reach 7.27. It meets the low-power, low-noise physiological signal acquisition system requirements and satisfies all design specifications.

Because of the time, although the entire system meets the design needs, there are still many shortcomings and areas that can be improved. Due to the insufficient consideration of the input-referred noise, the IRN of the circuit can be further compressed. Few details need to pay more attention to layout, such as parasitic and mismatch. Although the input resistance of several tens of megohms satisfies most of the application scenarios, a positive feedback loop will be designed in the future to allow the input resistance of the circuit to increase further. Last but not least, the ripple reduction loop will be added to reduce the interference of ripple further, further enhance the performance of the circuit.

REFERENCES

[1] "World Population Ageing 2019: Highlights," p. 46.

[2] X. Li *et al.*, "Digital Health: Tracking Physiomes and Activity Using Wearable Biosensors Reveals Useful Health-Related Information," *PLOS Biol.*, vol. 15, no. 1, p. e2001402, Jan. 2017, doi: 10.1371/journal.pbio.2001402.

[3] S. Patel, H. Park, P. Bonato, L. Chan, and M. Rodgers, "A review of wearable sensors and systems with application in rehabilitation," *J. NeuroEngineering Rehabil.*, vol. 9, no. 1, p. 21, Apr. 2012, doi: 10.1186/1743-0003-9-21.

[4] "Membrane Potentials," *Chemistry LibreTexts*, Oct. 02, 2013. https://chem.libretexts.org/Bookshelves/Analytical_Chemistry/Supplemental_Modules_(Analytical_Chemistry)/Electrochemistry/Exemplars/Membrane_Potentials (accessed Jul. 02, 2021).

[5] D. R. Breuer, "Some techniques for precision monolithic circuits applied to an instrumentation amplifier," *IEEE J. Solid-State Circuits*, vol. 3, no. 4, pp. 331–341, Dec. 1968, doi: 10.1109/JSSC.1968.1049921.

[6] N. P. Albaugh and B.-B. Corporation, "The Instrumentation Amplifier Handbook," p. 116.

[7] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003, doi: 10.1109/JSSC.2003.811979.

[8] Y. Tseng, Y. Ho, S. Kao, and C. Su, "A 0.09 μ W Low Power Front-End Biopotential Amplifier for Biosignal Recording," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 5, pp. 508–516, Oct. 2012, doi: 10.1109/TBCAS.2012.2188029.

[9] A. Pipino, A. Pezzotta, F. Resta, M. Matteis, and A. Baschirotto, “A rail-to-rail-input chopper instrumentation amplifier in 28nm CMOS,” *2015 IEEE Int. Conf. Electron. Circuits Syst. ICECS*, 2015, doi: 10.1109/ICECS.2015.7440252.

[10] H.-S. Lee, V. N. Nguyen, X. L. Pham, J.-W. Lee, and H.-K. Park, “A 250-μW, 18-nV/rtHz current-feedback chopper instrumentation amplifier in 180-nm cmos for high-performance bio-potential sensing applications,” *Analog Integr. Circuits Signal Process.*, vol. 90, no. 1, pp. 137–148, Jan. 2017, doi: 10.1007/s10470-016-0853-7.

[11] S. Zhang, X. Zhou, C. Gao, and Q. Li, “An AC-Coupled Instrumentation Amplifier Achieving 110-dB CMRR at 50 Hz With Chopped Pseudoresistors and Successive-Approximation-Based Capacitor Trimming,” *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 277–286, Jan. 2021, doi: 10.1109/JSSC.2020.3010816.

[12] X. Yang, M. Zhao, Y. Dong, and X. Wu, “A 14.9μW analog front-end with capacitively-coupled instrumentation amplifier and 14-bit SAR ADC for epilepsy diagnosis system,” in *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct. 2016, pp. 268–271. doi: 10.1109/BioCAS.2016.7833783.

[13] G. T. Ong and P. K. Chan, “A Power-Aware Chopper-Stabilized Instrumentation Amplifier for Resistive Wheatstone Bridge Sensors,” *IEEE Trans. Instrum. Meas.*, vol. 63, no. 9, pp. 2253–2263, Sep. 2014, doi: 10.1109/TIM.2014.2308992.

[14] G. Huang, T. Yin, Q. Wu, Y. Zhu, and H. Yang, “A 1.3μW 0.7μVRMS chopper current-reuse instrumentation amplifier for EEG applications,” in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2624–2627. doi: 10.1109/ISCAS.2015.7169224.

[15] J. Wu, M.-K. Law, P.-I. Mak, and R. P. Martins, “A 2- $\mu\textW$ 45-nV/√Hz Readout Front End With Multiple-Chopping Active-High-Pass Ripple Reduction Loop and Pseudofeedback DC Servo Loop,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 63, no. 4, pp. 351–355, Apr. 2016, doi: 10.1109/TCSII.2015.2504944.

[16] X. T. Pham, D. N. Duong, N. T. Nguyen, N. Van Truong, and J.-W. Lee, “A 4.5 GΩ-Input Impedance Chopper Amplifier With Embedded DC-Servo and Ripple Reduction Loops for Impedance Boosting to Sub-Hz,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 68, no. 1, pp. 116–120, Jan. 2021, doi: 10.1109/TCSII.2020.3007934.

[17] B. Razavi, *Design of analog CMOS integrated circuits*, Second edition. New York, NY: McGraw-Hill Education, 2017.

[18] A. M. Abo and P. R. Gray, “A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter,” *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, May 1999, doi: 10.1109/4.760369.

[19] D. C. Daly and A. P. Chandrakasan, “A 6-bit, 0.2 V to 0.9 V Highly Digital Flash ADC With Comparator Redundancy,” *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3030–3038, Nov. 2009, doi: 10.1109/JSSC.2009.2032699.

[20] H. Huang, K. Ao, Z. Guo, and Q. Li, “A 0.5V rate-resolution scalable SAR ADC with 63.7dB SFDR,” in *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2013, pp. 2030–2033. doi: 10.1109/ISCAS.2013.6572270.

[21] Y.-W. Bai, W.-Y. Chu, C.-Y. Chen, Y.-T. Lee, Y.-C. Tsai, and C.-H. Tsai, “Adjustable 60Hz noise reduction by a notch filter for ECG signals,” in *Proceedings of the 21st IEEE Instrumentation and Measurement Technology Conference (IEEE Cat. No.04CH37510)*, May 2004, vol. 3, pp. 1706-1711 Vol.3. doi: 10.1109/IMTC.2004.1351410.

[22] K. Makinwa, “Dynamic Offset-Cancellation Techniques,” *Smart Sens. Syst.*, p. 42.

[23] F. Maloberti, *Data Converters*. Springer US, 2007. doi: 10.1007/978-0-387-32486-9.

[24] C. C. Enz and G. C. Temes, “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization,” *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996, doi: 10.1109/5.542410.

[25] “To Chop or Auto-Zero: That Is the Question | Analog Devices.” https://www.analog.com/en/technical-articles/to-chop-or-auto-zero-that-is-the-question.html (accessed Jul. 12, 2021).

[26] J. G. Webster, Ed., *Medical Instrumentation: Application and Design*, 4th edition. Hoboken, NJ: Wiley, 2009.

[27] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, “Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI,” *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414–422, Mar. 1997, doi: 10.1109/16.556151.

[28] Z. Wang, H. S. Savci, J. Griggs, and N. S. Dogan, “1-V Ultra-Low-Power CMOS LC VCO with Dynamic Body Biasing,” in *2007 International Symposium on Signals, Circuits and Systems*, Jul. 2007, vol. 1, pp. 1–4. doi: 10.1109/ISSCS.2007.4292649.

[29] E. A. Vittoz, “Weak inversion in analog and digital circuits,” Oct. 2003.

[30] H. Soeleman, K. Roy, and B. C. Paul, “Robust subthreshold logic for ultra-low power operation,” *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 9, no. 1, pp. 90–99, Feb. 2001, doi: 10.1109/92.920822.

[31] H. C. Yang and D. J. Allstot, “Considerations for fast settling operational amplifiers,” *IEEE Trans. Circuits Syst.*, vol. 37, no. 3, pp. 326–334, Mar. 1990, doi: 10.1109/31.52726.

[32] M. A. T. Sanduleanu, A. J. M. Van Tuijl, R. F. Wassenaar, M. C. Lammers, and H. Wallinga, “A low noise, low residual offset, chopped amplifier for mixed level applications,” in *1998 IEEE International Conference on Electronics, Circuits and Systems. Surfing the Waves of Science and Technology (Cat. No.98EX196)*, Sep. 1998, vol. 2, pp. 333–336 vol.2. doi: 10.1109/ICECS.1998.814893.

[33] T. Denison, K. Consoer, W. Santa, A.-T. Avestruz, J. Cooley, and A. Kelly, “A 2 $\mu\hboxW$ 100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials,” *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007, doi: 10.1109/JSSC.2007.908664.

[34] Y. Kusuda, “Reducing Switching Artifacts in Chopper Amplifiers,” 2018, doi: 10.4233/uuid:62585ae8-da35-459e-bf90-f53f7d0de32c.

[35] P. R. Gray, Ed., *Analysis and design of analog integrated circuits*, 5th ed. New York: Wiley, 2009.

[36] H. Maarefi, A. Parsa, H. Hatamkhani, and D. Shiri, “A wide swing 1.5 V fully differential op-amp using a rail-to-rail analog CMFB circuit,” in *The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002.*, Aug. 2002, vol. 1, p. I–105. doi: 10.1109/MWSCAS.2002.1187167.

[37] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, “A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System,” *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 804–816, Apr. 2010, doi: 10.1109/JSSC.2010.2042245.

[38] C.-J. Lee and J.-I. Song, “A Chopper-Stabilized Amplifier With a Tunable Bandwidth for EEG Acquisition Applications,” *IEEE Access*, vol. 7, pp. 73165–73171, 2019, doi: 10.1109/ACCESS.2019.2919607.

[39] J. Zheng, W.-H. Ki, L. Hu, and C.-Y. Tsui, “Chopper Capacitively Coupled Instrumentation Amplifier Capable of Handling Large Electrode Offset for Biopotential Recordings,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 64, no. 12, pp. 1392–1396, Dec. 2017, doi: 10.1109/TCSII.2017.2741348.

[40] R. Muller *et al.*, “24.1 A miniaturized 64-channel 225μW wireless electrocorticographic neural sensor,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 412–413. doi: 10.1109/ISSCC.2014.6757492.