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Case Study: Direct Conversion Transmitters for UMTS

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The presented thesis, consisting of seven papers and an extended summery, has been submitted for evaluation for an industrial PhD.

Industrial PhD Program
The presented thesis documents the research project completed as a part of the Danish industrial PhD education. This education is administrated by the Committee on Industrial PhD Fellowship under the Danish Academy of Technical Sciences (ATV), and is financially supported by the Danish Agency for Trade and Industry under the Ministry of Business and Industry.

Abstract

The research project investigates the use of a Q-enhanced LC resonators in monolithic UMTS transmitters, implemented in a standard CMOS process.

The project was started in the summer of 2000. At this time there was only limited available information about how to design transmitters for UMTS. UMTS transmitter performance is, among other things, specified by Adjacent Channel Leakage Ratio (ACLR) and Error Vector Magnitude (EVM). Relations between ACLR, EVM and various circuit imperfections are investigated through simulations and measurements using real UMTS signals and test equipment. The direct up-conversion transmitter is found to be the best architecture for integration on CMOS. However, it requires a bandpass filter with a pass band in the GHz range in order to meet requirements to noise in the downlink band.

It is investigated how such an RF bandpass filter may be implemented on CMOS. Passive on-chip resonators can only be implemented with low Quality factor (Q) because of losses in on-chip inductors. It is possible to compensate for these losses with active circuits. Such a circuit is implemented using a topology, where transistors and capacitors are used to generate a negative differential conductance. An expression for the differential admittance of this circuit is derived and verified through measurements.

The Q-enhancement circuit is used in an LC resonator designed for operation at 1950 MHz. The concept of Q-enhancement works fine, but the use of reactive components in the Q-enhancement circuit limits the freedom in the design of the resonator. The measured center frequency was 1850 MHz and the tuning range approximately 90 MHz. This could be recreated in simulations if measured data for Metal Insulator Metal (MIM) capacitors and varactors were used instead of the design kit provided by the foundry.

Preface

The research project document in this thesis was made at the RF Integrated Systems & Circuit (RISC) group at Center for TeleInFrastruktur (CTIF) at Aalborg University. The research within RISC covers system analysis, chip design and analysis of single devices.

The project was initiated in collaboration between Telital R&D Denmark, RISC and the Danish Academy of Technical Sciences (ATV). The project was planned to follow a line, starting with a thorough analysis how to design transmitters for UMTS. This system was chosen because Telital R&D Denmark was starting up the design of their first transmitter for UMTS when the project was planned. No system knowledge was available at the time and the project was hoped to remedy this. The official start of the project is 1st of August 2000. However, Telital R&D Denmark did not receive their transmitter tester for UMTS before the spring of 2001. This meant that the system analysis could not be backed up with measurements before this time. The measurements did in fact prove an initial expression for IQ phase offset to be wrong and therefore caused a new version to be derived. The system analysis investigated a transmitter architecture for implementation on CMOS. A critical block in this architecture was selected to demonstrate if and how it could be implemented on CMOS. The system analysis was finished in the early winter of 2002. The conclusion was that a direct up-conversion transmitter was the best immediate choice. It required an RF bandpass filter to meet requirements to noise in the downlink band. This filter was selected for implementation in CMOS. It was known that the RISC group needed to change CMOS process from the beginning of the project. A test chip was submitted in the new process in the late spring of 2001. However, when the PhD student was ready to start the design in the spring of 2002, it had not yet arrived and it was decided to use a different foundry. The choice of Q-enhancement circuit was therefore based on simulations conducted with the design kit provided by the new foundry, even though it was not known how well this design kit matched reality. Newer the less a 2nd order filter was designed and a layout containing this together with sub-circuits and test structures was submitted in the early summer of 2002. In the meantime Telital R&D Denmark got into financial difficulties. It was arranged that the PhD student could be transferred to Texas Instruments Denmark A/S in the summer of 2002. The first chip from the new foundry was received in the fall of 2002, but a manufacturing error meant that the transistors only had half the gain available in the design kit. Functional chips were received in December 2002. Investigations conducted during the spring and summer of 2003 revealed two major errors on the designed circuits that rendered the designed filter useless. After two more chip runs, the latest received in the fall of 2003, the Q-enhancement circuit was functional and the analysis presented in this thesis could be carried out.

The presented thesis contains seven publications and an extended summery. Chapter 1 gives a short introduction to each paper, while chapter 2 to 8 make up the extended summery. Chapter 2 gives an introduction to the project, its background, aim and areas where the author believes his research has made significant contributions. Chapter 3 sums up and updates the system analysis. It is based on work published in [6, 4, 7, 5]. Chapter 4 investigates how the desired filter may be implemented with special emphasis on required Q and tuneability of the resonators. Chapter 5 investigates how resonators may be implemented. This section relies heavily on literature studies. Chapter 6 describes the Q-enhancement circuit designed in this project. It is

based on [1, 2]. Chapter 7 describes an experiment where the Q-enhancement circuit is used in an LC tank, based on [3]. It also concludes on the usability of the proposed Q-enhancement circuit.

The road through this project has been long and bumpy. With the help and understanding from many persons it has, never the less, been possible to reach a point where the presented thesis can be submitted. First of all the student would like to thank Torben Amtoft, Telital R&D Denmark, Torben Larsen and Troels Emil Kolding, both from RISC, for starting this project, ATV for supporting it financially and Willy Bergstrøm for representing the project at ATV. The student would further more like to thank Torben Amtoft, Torben Larsen, Troels Emil Kolding, Jan Hvolgaard Mikkelsen and Jens Christian Lindof for being supervisors during the project. The student would like to thank Arne Bisgaard Kristensen and Jens Arne Hald at Telital R&D Denmark for arranging for the project to be continued at Texas Instruments Denmark A/S, when Telital R&D Denmark could no longer continue the project. The student would further more like to thank Finn Andersen and Jens Christian Lindof at Texas Instruments Denmark A/S for continuing the project there. Finally the student would like to thank former colleges at Telital R&D Denmark together with new colleges at Texas Instruments Denmark A/S and RISC for their support during the project.

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Contents

1 PUBLICATIONS

This chapter gives a short introduction to the publications made during the PhD project. The papers address the two major topics of this project, which are system analysis of UMTS transmitters and the design of a Q-enhancement circuit. The chapter contains seven sections named after the title of the paper they describe. The sections are arranged in the order in which the papers were submitted. The description only includes the authors scientific contributions to the papers.

1-1 RF Requirements for UTRA/FDD Trancievers

Authors:	Per Madsen, Ole Kiel Jensen, Torben Amtoft, Ragner V. Reynisson, Jan H. Mikkelsen, Søren Laursen, Cristian R. Iversen, Troels E. Kolding Torben Larsen and Michael B. Jenner
Place:	Wireless Personal Multimedia Communications (WPMC), Aalborg, Denmark
Time:	September 2001

The analysis of the transmitter is based on the authors work. Overall requirements to the transmitter are determined from several factors. The specifications set requirements to EVM, ACLR and out of band noise, but the receiver sensitivity and the isolation in the duplex filter sets a requirement to how much noise the transmitter may emit in the downlink band. Overall requirements to IQ balance, inband ripple, local oscillator feed through and phase noise are set-up from the requirements to EVM. The ACLR requirement is converted to a specification of a 1 dB compression point, as an simple relation between these parameters appeared to be present at the time of writing. A budget is set up for a direct conversion transmitter based on these requirements. It is found that an RF bandpass filter is required in order to suppress noise in the downlink band.

1-2 Simulating Overall Performance Requirements for Transmitters in IMT 2000 FDD User Equipment

Author:	Per Madsen
Place:	European Conference on Wireless Technology, London, England
Time:	September 2001

This paper investigates how a number of different circuit imperfections affect EVM and ACLR in transmitters for UMTS FDD. It sets up analytical expressions for these parameters in order to provide a simple means to make budgets. All the expressions are verified through measurements. The included parameters are: Quantization, IQ phase and amplitude imbalance, phase noise and linearity. It was found that phase and amplitude adjustments could improve EVM as function of IQ imbalance. Further more no simple relation between 3^{rd} order output intercept point or 1 dB compression points and ACLR were found.

The expressions for IQ imbalance has caused much interest in the public. So much in fact that the student later made a short document where the expressions were derived. This document was then handed to persons who made enquiries.

1-3 UTRA/FDD RF Transceiver Requirements

Authors:	Per Madsen, Ole Kiel Jensen, Torben Amtoft, Ragner V. Reynisson, Jan H. Mikkelsen, Søren Laursen, Troels E. Kolding, Torben Larsen and Michael B. Jenner
Place:	Wireless Personal Communications, Kluwer Academic Publishers
Time:	October 2002

The paper submitted to WPMC was selected for a reprint at Kluwer Academic Publishers: Journal of Wireless Personal Communications, special issue: Wireless Personal Multimedia Communications. Although the paper was a reprint it is shorter than the original paper. This meant that some adjustments had to be made to the contents. The major changes were made in the section describing the overall receiver requirements, which relies more on references in this paper. In the transmitter section an expression is presented, that describes how ACLR adds and the budget of 1 dB compression points is replaced with an ACLR budget. This was done after it was found that no simple relation between ACLR and 1 dB compression point could be established.

1-4 On the Design of a Differential Common Collector Negative Resistance

Authors:	Per Madsen, Torben Larsen, Jan H. Mikkelsen and Jens C. Lindof
Place:	21st Norchip Conference, Riga, Latvia
Time:	November 2003

This paper describes an experiment with a discrete implementation of a Q-enhancement circuit that the student believes to be very interesting for his application. Simulations indicated that the most often used Q-enhancement circuit would have difficulties in providing sufficient linearity for the desired application. Therefore a differential version of a circuit was implemented, whos single ended counter part in theory could be designed to perform better. However, the theory is based on simple representations of transistor parasitics. The paper presents an expression that includes more transistor parasitics to describe the differential admittance of this circuit. The paper focus on the verification of the expression. The circuit is therefore designed to operate at low frequencies and implemented using discrete components. This makes it possible to measure the components that are were used in the circuit with a high degree of accuracy. The new expression was found to be much more accurate than the more simple expression, whos equivalents are seen in the literature for single ended versions of the circuit. However, the match is not perfect.

1-5 Simulation of EVM Due to Circuit Imperfections in UMTS/FDD Transmitters

Authors:	Per Madsen
Place:	Nordic Matlab Conference 2003, Copenhagen, Denmark
Time:	October 2003

This paper address the same general issues that were addressed in: " Simulating Overall Performance Requirements for Transmitters in IMT 2000 FDD User Equipment", but being submitted to a MATLAB^{TM} conference, methodology and simulated results are also included. The paper includes effects of IQ phase and amplitude imbalance, phase noise, filtering and time offsets between phase and magnitude in polar modulators. It further more presents simulations of how several interferences combines. A new expression has been derived for IQ phase imbalance. The previous expression was based on an educated guess of the optimal phase compensation. The expression presented here uses an analytically calculated optimum. There were no significant difference between the results obtained with the two expressions.

1-6 An RF CMOS Differential Negative Resistance for Q-enhancement

Authors:	Per Madsen, Torben Larsen, Jan H. Mikkelsen and Jens
Place:	The 7th International Conference on Solid State and Integrated Circuit Technology, Beijing, China
Time:	October 2004

This paper presents an implementation of the differential Q-enhancement circuit, presented in: "On the Design of a Differential Common Collector Negative Resistance", on RF CMOS. The paper shows simulated and measured 2-port S-parameters and describes the steps necessary to obtain the reported fit. The paper further more reports the obtained differential admittance divided in conductance and equivalent capacitance. Here measured results are compared with simulations and estimates made using the more detailed expression presented in: "On the Design of a Differential Common Collector Negative Resistance". The circuit is capable of providing a differential conductance at -2.8 mS and an equivalent capacitance of approx 1 pF at 2 GHz with a current consumption of 32 mA. However, the most interesting result of the paper is that the described method enables the expression to estimate the admittance with less than 20 % error.

1-7 An RF CMOS Q-enhanced LC Resonator

Authors:	Per Madsen, Torben Larsen, Jan H. Mikkelsen and Jens C. Lindof
Place:	22nd Norchip Conference, Oslo, Norway
Time:	November 2004

This paper presents and example of how the Q-enhancement circuit presented in: "An RF CMOS Differential Negative Resistance for Q-enhancement" may be used in a on chip LC res-

onator. The resonator consists of an inductor, through which the active transistors are biased and a bank of varactors that provide tune-ability of the resonator frequency. The inductor is implemented with four windings and symmetry around the bias feed point. The differential inductance is in the order of 5.6 nH, while the conductance is 2 mS. It was found that a 3-port representation of the inductors was required to make simulated S-parameters fit measurements. The varactors were implemented with nFETs. The design kit was found not to simulate weak accumulation mode well, so measurements on stand alone circuits were used instead. This provided an accuracy of 3 MHz between simulated and measured resonance frequency. The Q-enhancement circuit was found to compensate the LC-resonator, while consuming a total of 6.9 mA. The Q-enhancement circuit is thus more than capable of compensating for losses in the resonator.

2 INTRODUCTION

The presented PhD thesis documents a project that was started in August 2000. At this time new standards for mobile telecommunications such as Universal Mobile Telecommunication Standard (UMTS), General Packet Radio Service (GPRS) and Enhanced Data rates for GSM Evolution (EDGE) were emerging. These standards enables high data transfer rates, which in tern enables new types of applications like video streaming, Moving Pictures Expert Group layer 3 (MPEG–3) sound, exchange pictures, etc. to run on mobile User Equipment (UE).

2-1 Background

The project conciders two major topics. System analysis and RF CMOS design. This section gives a short introduction to why these two topics were considered in the project.

The project was started as Telital R&D Denmark started the design of its first UMTS transmitter. The project was initiated in order to provide knowledge about how to design a transmitter for UMTS. Telital R&D Denmark had no experience with parameters like Error Vector Magnitude (EVM) and Adjacent Channel Leakage Ratio (ACLR), which are used to specify transmitter performance in UMTS [1]. It was therefore necessary to know how different circuit imperfections in the transmitter affect these parameters.

The ideal transceiver for design and manufacture of low cost mobile equipment would have to be implemented as one component. Such a transceiver would reduce time spent on Radio Frequency (RF) design and increase production yield. An increase in complexity is needed to support the new capabilities provided by the high-speed digital standards. One way to handle this increased complexity without an equivalent increase of complexity of the Printed Circuit Board (PCB) is to implement several types of circuits on the same chip. This is denoted System On Chip (SoC). SoC is excellent to combine digital circuits, but analog circuits can also be added. To obtain the full advantage of SoC, no external circuits, except for the relevant transducers like speaker, microphone, video camera, etc. and battery, should be required. This implies that the radio circuits are fully integrated on the chip with only one connection to the antenna. The project uses the design of a UMTS transmitter as a case study for RF circuit designs intended for SoC.

2-2 Research Topics

The research activities the project goes in two directions. (i) A thorough system analysis is made on the UMTS transmitter. It establishes how design parameters, such as phase noise, In-phase and Quadrature (IQ) imbalance, linearity, - etc. affect EVM and ACLR. This is used in an analysis of transmitter architectures in order to find out how a UMTS transimitter for Frequency Division Duplex (FDD) can be implemented. This part of the project is concluded with a specification of the blocks in an architecture that is believed to be suitable for SoC. (ii) The transmitter is expected to be implemented on Complementary Metallic Oxide Semiconductor (CMOS) as this is a relative cheap process that is well suited for digital circuits and hence SoCs. However component tolerances and poor quality in on-chip inductors make vital

RF circuits inefficient. In this project one circuit that is critical for the selected transmitter must be implemented on a standard CMOS process.

2-3 Scientific Contribution

The research contributions of this project are represented through the papers described in chapter 1. This section draws the up the areas in which the project, to the knowledge of the author, has provided scientific contributions.

EVM and ACLR were unknown to Telital R&D Denmark when the project was started. A search in the literature revealed only little material on this topic. Major scientific contributions from this work are the expressions that relate IQ amplitude and phase imbalance to EVM. The project tests expressions derived by both the author and others against measurements conducted with true W-CDMA signals and test-equipment. The latter is important in order to ensure that assumptions made on the signals are valid.

Telital R&D Denmark did not know how to make transmitters for UMTS, when the project was started. Vendors suggested heterodyne up-conversion, but this project has shown that direct up-conversion or polar modulation are probably better choices. It was found that the transmitter noise in the down link band is the major problem with direct (and heterodyne) up-conversion transmitters. An RF bandpass filter must be inserted before the Power Amplifier (PA) to meet requirements to this noise.

The RF bandpass filter was chosen for implementation in CMOS. Q-enhanced LC resonators were found to be best suitable for this application. The application in the transmitter sets particularly harsh requirements to linearity and this has caused the author to implement a Q-enhancement circuit that is not normally used in differential applications. A detailed expression for the differential admittance of this circuit has been set up and verified through measurements on implemented circuits.

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3 CASE STUDY: UMTS TRANSMITTERS

This chapter addresses system aspects of transmitters for UMTS. It is based on [16, 14, 17, 15] and demonstrates how a transmitter for UMTS can be designed. The analysis starts with an investigation of overall requirements the transmitter. These requirements are converted to specifications of the performance of individual blocks in a selected transmitter architecture. This investigation includes an analysis of how circuit imperfections affect measured parameters, such as EVM and ACLR [1]. The investigation is based on FDD steady state operation for UMTS-FDD transmitters for power class III band I [1], but some results may apply to other modes as well. The up-link band is defined from 1920 MHz to 1980 MHz and the down link band from 2110 MHz to 2170 MHz.

3-1 Overall Transmitter Requirements

This section describes the requirements to UMTS transmitters. These requirements are dictated by the specifications [1] together with the performance of the duplex filter and the receiver.

3-1-1 Duplex Filter

The UMTS-FDD system operates in full duplex. This means that the transmitter branch (Tx) and receiver branch (Rx) may be active at the same time. Therefore the two branches must have access to the antenna at the same time. A duplex filter allows this as illustrated in Figure 1. The duplex filter separates the two signals in the frequency domain with filters, but complete separation can not be achieved. Some Tx power will leak to the Rx branch, due to limited attenuation in filters and cross talk between the Rx and Tx traces. This is indicated with "Tx leakage" in Figure 1.

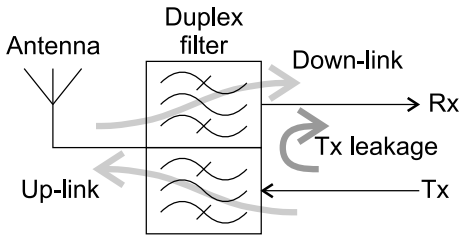

FIGURE 1: *Functionality of the duplex filter. Up-link and Down-link is separated, but some Tx leakage to the Rx branch can not be avoided.*

The isolation between Rx and Tx is important for the performance of the receiver, because both the high power up-link signal and transmitter noise in the Rx band interferes with the receiver [16]. However the isolation in the duplex filter has to be weighted against insertion loss. Table 3.1 lists the amount of insertion loss and isolation to be expected in duplex filters for UMTS [19, 3].

TABLE 3.1: *Specification of duplex filter.*

Frequency band	**Attenuation [dB]**
Tx - Antenna	
$1920\ MHz < f < 1980\ MHz$	< 2
Antenna - Rx	
$2110MHz < f < 2170MHz$	< 2
Tx - Rx Isolation	
$1920\ MHz < f < 1980\ MHz$	> 50
$2110\ MHz < f < 2170\ MHz$	> 44

3-1-2 Requirements at the Transmitter Output

The requirements to the transmitter output signal are based on the specifications for UMTS-FDD [1] and the requirement to transmitter noise leakage to Rx in [16, 17]. [16] presents a receiver noise budget, where the noise contribution in the Rx band is assumed to -111 dBm/3.84 MHz. It is assumed that a duplex filter can provide 44 dB isolation in the Rx band [19, 3]. The specifications allow the transmitter to leak -60 dBm/3.84 MHz to the antenna in the Rx band [1], but the transmitter must generate no more than -67 dBm/3.84 MHz in order not to degrade the receiver significantly [16]. Assuming that the duplex filter defined in Table 3.1 is used, the requirements to the steady state output signal of the transmitter are as presented in Table 3.2.

The spectrum emission mask is defined to match ACLR and requirements made by systems operating on neighbour frequency bands [5, 6, 4]. It is introduced to ensure co-existence with other systems, operating at bands where the ACLR measurement makes no sense [5, 6, 4]. If nothing is indicated, it is assumed that the spectral emission mask requirements are meet if the ACLR requirements are meet. This is in agreement with observations made during measurements on PAs.

Both EVM and peak code domain error describe the signal quality [1]. EVM describes the ratio between the averaged error power in the transmitted signal and the averaged power of the equivalent error-free signal as expressed by Eq. (5) in [15]. Peak code domain error expresses how the error is distributed in the code domain [12]. The error signal is de-spread with all codes in the domain [12]. Code Domain Error (CDE) is the ratio between the power of the error signal, de-spread with one code, and the power of the error free signal [12]. If the error signals are mutually uncorrelated and evenly distributed over all the codes, there is a simple relation between CDE and EVM [7, 23]:

$$\mathrm{CDE} = 10 \cdot \log_{10}\left(\frac{\mathrm{EVM}^2}{SF}\right) \tag{3.1}$$

where EVM is expressed in decimal scalars and SF is the spreading factor. Peak code domain error is specified as the largest of the CDE values, measured on a signal where the spreading codes are 4 chips long [1]. EVM is specified to 17.5 % so according to Eq. (3.1), CDE should be -21.2 dB. However the uplink spreading code are not completely orthogonal so some margin

TABLE 3.2: *Specification of output signal.*

Parameter	**Values**	**Unit**
Frequency of operation		
Min	1920	MHz
Max	1980	MHz
Signal power		
Max average power	> 26	dBm/3.84 MHz
Min average power	< -48	dBm/3.84 MHz
Signal Quality		
Average EVM	< 17.5	%
Peak Code Domain Error	< -15	dB
Spectrum emission mask		
$f_C \pm$ *2.5 MHz*	< -35	dBc/30 kHz
$f_C \pm$ *3.5 MHz*	< -35	dBc/1 MHz
$f_C \pm$ *7.5 MHz*	< -39	dBc/1 MHz
$f_C \pm$ *8.5 MHz*	< -49	dBc/1 MHz
$f_C \pm$ *12.5 MHz*	< -49	dBc/1 MHz
Or no more than:	< -55.8	dBm/1 MHz
Adjacent channel leakage		
$f_C \pm$ *5 MHz*	> 33	dB
$f_C \pm$ *10 MHz*	> 43	dB
Or no more than:	< -48	dBm/3.84 MHz
Inband spurious signals		
f>12.5 MHz	< -28	dBm/1 MHz
Out of band spurious emissions		
1805 MHz $< f <$ *1880 MHz*	<- 69	dBm/100 kHz
1893.5 MHz $< f <$ *1919.6 MHz*	< -39	dBm/300 kHz
2110 MHz $< f <$ *2170 MHz*	< -67	dBm/3.84 MHz

must be added [7]. Hence -15 dB is used [7], but this is approximately the same noise to signal ratio that is required to achieved an EVM of 17.5 %. This means that the requirement to peak code domain error is meet if the transmitter meets the EVM requirement, even if all the power in the error vector is projected on to one code. Peak code domain error is thus ignored in this analysis.

3-2 Transmitter Architectures

This section investigates which kind of transmitters may be used for UMTS and which requirements are made to the functional blocks in the particular transmitter. The signal modulation is a limiting factor, when it comes to choosing a suitable transmitter architecture. The W-CDMA up-link signal contains both amplitude and phase information. This means the modulation loop used for GSM can not be used, because it can not transfer the amplitude information. The most commonly suggested architectures for UMTS are direct up-conversion, heterodyne up-conversion, digital Intermediate Frequency (IF) and polar modulation [18, 24, 11, 22, 2, 20].

In the heterodyne transmitter up-conversion takes place in two stages. In-phase and Quadrature (IQ) components are modulated to some IF and then mixed to the desired frequency [18]. The use of an IF means that the modulator can work on frequencies lower than where the transmission takes place. This may improve the accuracy of the IQ phase offset, but bandpass filters are required both at IF and RF [18]. It is possible to design modulators for direct conversion with sufficient precision of IQ to meet the EVM requirements [24, 13]. The main advantage of the heterodyne transmitter is thus not relevant for the UMTS transmitter, and the use of an extra filter makes it less attractive than other architectures.

In the digital IF architecture, the signal is converted to analog at IF. This means that the modulation of the IQ components is done digitally [11, 22]. The digital approach has the potential of being more versatile and exact than the analog counter parts [11, 22], but the digital to analog converters (DAC)s need to run at high frequencies to keep aliasing products from appearing in the uplink band or neighboring bands, where requirements to noise are particularly harsh. The same aliasing products cause the need for an IF bandpass filter. As was the case for the heterodyne transmitter, the advantages of the digital IF architecture are not relevant for the UMTS transmitter.

The remaining two architectures are exposed to more thorough investigations.

3-2-1 Direct Up-conversion

The Direct up-conversion transmitter is illustrated in Figure 2. The IQ components are converted directly to the desired frequency in the Quadrature Up-Converter (QUC). The gain is adjusted at RF in a Variable Gain Amplifier VGA [2] and in some cases the PA. Some filtering is required before the PA in order to ease requirements to the duplex filter [16]. Finally the PA amplifies the signal to the desired level.

Compared to the heterodyne transmitter this architecture saves circuits, but it also sets more

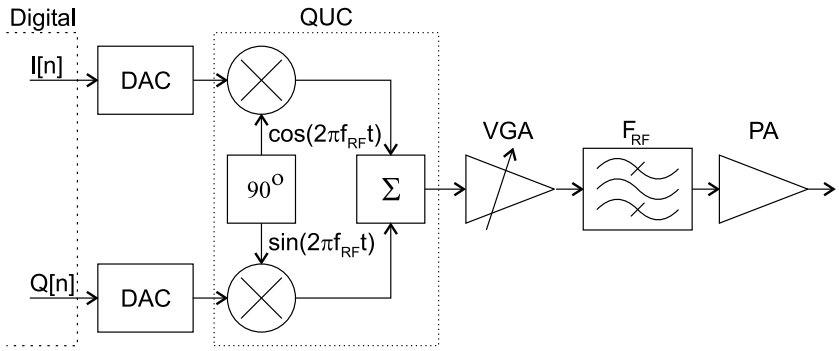

FIGURE 2: *Block diagram of a direct up-conversion transmitter.*

harsh requirements to the used circuits [2]. The 90° phase shift in the modulator must be made at RF, and the Local Oscillator (LO) should run a frequency outside the Tx band, to make it less sensitive to interference from the transmitted signal.

The following describes which kind of requirements ACLR, EVM and out of band spurious emissions sets to the blocks in the direct conversion transmitter. The presented work is based on material published in [16, 14, 13, 15] and additional work performed by the author. Budgets have been updated to fit reported state of the art performance.

All the circuits in the transmitter are non-linear and thus contribute to the overall ACLR. The PA will typically be the largest contributor, because the signal power is highest here. There is no simple relation between ACLR and the parameters most often used to describe non-linear performance [14]. Therefore ACLR is specified for each block [8, 21, 17]. Assuming that the contributions are mutually uncorrelated, the total ACLR generated by n cascaded circuits ($ACLR_T$) can be found from the ACLR of circuits $1-n$ ($ACLR_m|_{m=1,2,\ldots,n}$) using [17]:

$$ACLR_T = \frac{1}{\sum_{m=1}^{n} ACLR_m^{-1}} \tag{3.2}$$

where ACLR is represented in scalars. However, due to the nature of non-linear distortion, the clause that the contributions must mutually uncorrelated may not apply. The expression was therefore verified experimentally for different ranges of ACLR. IQ signals were converted to RF in a Signal Generator (SG) and then amplified with first one amplifier (AMP_1) and then two amplifiers in cascade (AMP_1 and AMP_2). The power into the amplifiers was controlled with attenuators and both ACLR at f_C±5 MHz ($ACLR_1$) and EVM were measured. $ACLR_1$ and EVM was also measured on each amplifier and the SG alone, while exposed to the signals faced during the tests. Eq. (3.2) is used to estimate the cascaded ACLR. In Table 3.3 the results are compared with cascaded measurements. ACLR is averaged from measurements on f_C +5 MHz and f_C -5 MHz.

It is seen that Eq. (3.2) is a good estimate for levels of ACLR up to the required 33 dB, while the estimate becomes worse as ACLR increases further. The error is still less than 1 dB and might originate from changing measurement setups for for individual amplifiers and cascaded

TABLE 3.3: *Cascaded ACLR.*

Case	1	2	3	4	5	6	Unit
Individual ACLR$_1$							
SG	42.2	42.2	36.7	36.7	33.1	33.1	dB
AMP_1	45.0	45.0	37.5	37.5	30.2	30.2	dB
AMP_2	–	49.7	–	42.6	–	27.3	dB
Combined ACLR$_1$							
Measured	40.1	40.2	34.2	33.5	28.7	24.3	dB
Eq. (3.2)	40.0	39.9	34.1	33.5	29.1	25.1	dB

configurations. Although it can not be concluded that the contribution to ACLR are mutually uncorrelated, Eq. (3.2) can be used to make a budget for ACLR. This is done in Table 3.5. The ACLR reported in [21] is used for the PA. The budget is made so that a total of 34 dB is obtained for ACLR_1 and 44 dB for (ACLR_2), which is defined as the ACLR at $f_C \pm 10$ MHz [17].

EVM combined by several parameters may be expressed in a similar manner [15]. If n contributors to EVM are mutually uncorrelated, the combined EVM (EVM_C) is [15]:

$$\text{EVM}_\text{C} = \sqrt{\sum_{i=1}^{n} \text{EVM}_i^2} \tag{3.3}$$

It has been demonstrated that Eq. (3.3) does not apply to very non-linear cascaded stages like hard limiters [10]. It is therefore investigated if the circuits in the transmitter are sufficiently linear for Eq. (3.3) to apply. EVM was measured during the experiment with cascaded power amplifiers described above. The results are listed in Table 3.4.

TABLE 3.4: *Cascaded EVM. The cases in this table refer to the cases in Table 3.3*

Case	1	2	3	4	5	6	Unit
Individual EVM							
SG	2.1	2.1	2.6	2.6	3.5	3.5	%
AMP_1	2.0	2.0	1.9	1.9	3.6	3.6	%
AMP_2	–	0.8	–	1.2	–	5.8	%
Combined EVM							
Measured	2.3	2.3	3.3	3.5	5.1	7.8	%
Eq. (3.3)	2.3	2.5	3.2	3.4	5.0	7.6	%

It is seen that Eq. (3.3) estimates EVM well, even when the requirements to ACLR are violated heavily as in cases 5 and 6. Cascaded ACLR can therefore be related to cascaded EVM. The work presented in [14, 15] is vital for budgeting EVM. EVM owing to IQ amplitude (EVM_AIQ),

phase imbalance (EVM_{PIQ}) and RMS phase noise (EVM_{PN}) can be expressed by [15]:

$$EVM_{AIQ} \approx \sqrt{\left| 2 - \sqrt{\frac{2}{A^2+1}}(A+1) \right|} \cdot 100\% \quad (3.4)$$

$$EVM_{PIQ} = \sqrt{1 - \left(\cos\left(\frac{\varphi}{2}\right)\right)^2} \cdot 100\% \quad (3.5)$$

$$EVM_{PN} \approx \sqrt{2 - 2\cos(\phi)} \cdot 100\% \quad (3.6)$$

where A is IQ amplitude offset ratio, φ is IQ phase offset from 90° and ϕ is the RMS phase error on the LO. There is a correlation between ACLR and EVM in a non-linear device [14]. For an ACLR of 33 dB, EVM is approximately 2.5 % [14]. [24] reports an A of 0.3 dB and a φ of 0.5 deg and the GSM specifications prescribes RMS phase noise of maximum 5 deg. This performance combines to an EVM of 9.25 % with phase noise being the largest contributor. The achieved EVM leaves a margin of 14.8 % for DACs and filtering, before the specified 17.5 % is reached.

Noise is the real killer in this architecture [16]. Requirements to the IF filter depends on the power delivered by the DACs. This is because noise power levels and not signal to noise levels are specified. Too much gain amplifies the noise floor to critical levels, even if the circuits were noise less. Duplex filters have improved compared to the one used in [16] and PAs with of 26 dB gain and a Noise Figure (NF) of 5 dB are reported [8, 21]. This means that the gain budget and hence filter requirements should be re-evaluated. In Table 3.5 new budgets for inband gain, noise and ACLR are set up for the direct up-conversion transmitter in Figure 2. It assumes that the DACs deliver -15 dBm of signal power. The noise requirement to the filter is adjusted to

TABLE 3.5: *Budgets for gain, noise and ACLR for the functional blocks in Figure 2.*

functional block	QUC	VGA	FI	PA
Gain [dB]	0	12	3	26
NF [dB]	10	4	10	5
ACLR ± 5 MHz [dB]	46	46	45	35
ACLR ± 10 MHz [dB]	53	50	50	48.5

ensure that the transmitter meets requirements to noise from 1805 MHz to 1880 MHz. In this budget the filter is required to attenuate the Rx and Rx-image bands by 15 dB compared to the inband gain, while the NF at these bands is less than 15 dB. Increased NF in any of the blocks must be compensated by either increased power from the DACs or attenuation in the filter. To omit the filter completely, the DACs must deliver -1 dBm of power, but this is assumed not to be realistic. The direct conversion transmitter therefore still requires a bandpass filter to meet requirements to noise in UMTS downlink, as concluded in [16, 17], but the requirements to the filter have been relaxed because of improved separation in the duplex filters.

3-2-2 Polar Modulation

In the polar modulator the amplitude information is applied at RF. The PA is the best place to apply the amplitude information, because it can be done power efficiently with a switched PA and the remaining RF parts only handle constant envelope signals [20]. This is illustrated in Figure 3, where a Voltage Controlled Oscillator (VCO) is used to apply the phase information to an RF signal. The figure employs an up-conversion loop well known from GSM today, but any control system that is capable of applying the phase information to the VCO should work. This is illustrated by including a part of the up-conversion loop in the digital block.

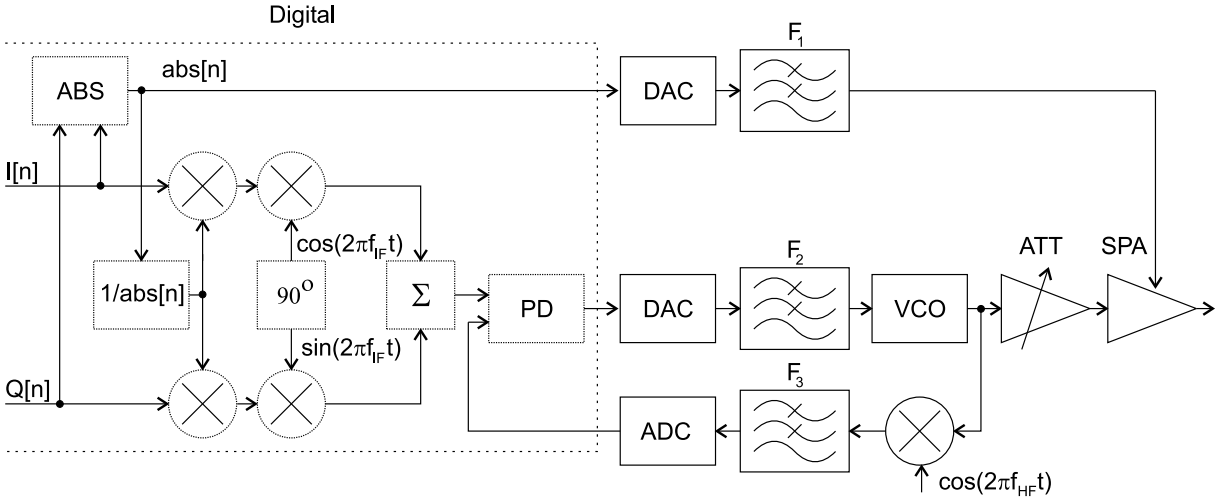

FIGURE 3: *Functional diagram of the polar modulation transmitter.*

The polar modulator is sensitive to the same errors as the direct up-conversion transmitter, but it has the advantage that a power VCO, also known from GSM, may be used. This means that only limited gain is needed at RF, which means that the output noise may be reduced. Further more the remaining circuits only add little to ACLR if the amplitude information is applied at the PA. However a timing offset between phase and amplitude information introduces non-linearity and hence affects ACLR [20, 9]. In order to investigate this an experiment was made, where phase information was separated from amplitude information and converted to RF in a signal generator. The amplitude information was then added using a VGA with a very short settling time. ACLR and EVM were measured using signals where different time offsets were introduced between phase and amplitude. The results for ACLR are shown in Figure 4, where they are compared to simulations conducted in MATLAB^{TM}. $ACLR_1$ is averaged from measurements on channels ± 5 MHz from f_C, while $ACLR_2$ is averaged from measurements on channels ± 10 MHz from f_C.

The simulations only includes timing offsets. It is seen that the simulations indicates close to ideal behavior when no timing offsets are applied. The measurements shows significant ACLR even at the optimal time offset, but as the time offset is increased, the measured $ACLR_1$ becomes increasingly close to the simulations. This indicates that the simulations are right, but that other factors than time offsets are significant in the measurements. It is also noticed that

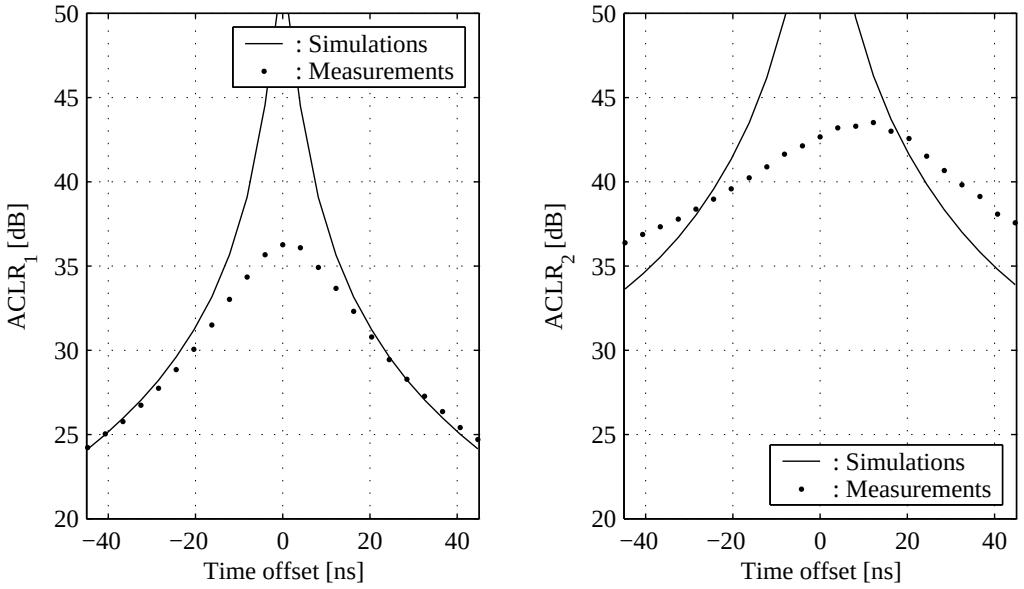

FIGURE 4: *Simulated ACLR as function of time offset between phase and magnitude information.*

the best time offset for $ACLR_1$ is not the best time offset for $ACLR_2$. It was found that $ACLR_2$ could be improved to 45.9 dB where $ACLR_1$ was largest, if the phase information was filtered with a 3^{rd} order Butterworth filter with a cut off frequency of 3.5 MHz, before it was applied to modulator.

An equivalent comparison between time offsets and EVM is made in figure 5. Here the match between simulations and measurements is also good.

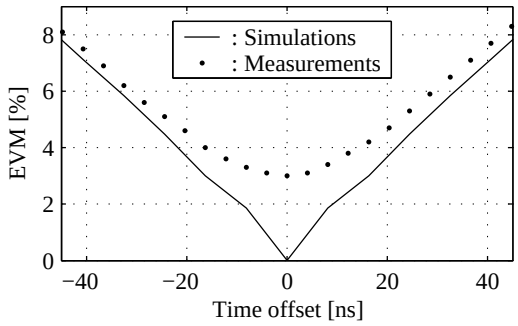

FIGURE 5: *Simulated EVM as function of time offset between phase and magnitude information.*

The Power Spectral Density (PSD) of the spectral regrowth caused by the time offset was different from that caused by intermodulation. In this case the PSD was distributed more evenly across the neighbor channels. This may cause problems with the spectral emission mask. An offset of 16.3 ns generated an $ACLR_1$ of 33.2 dB and an $ACLR_2$ of 43.9 dB in the simulations.

The resulting power spectrum (PS) is integrated over bands of 30 kHz or 1 MHz as specified in Table 3.2. In Figure 6 the integrated values are compared to the spectral emission mask defined in Table 3.2.

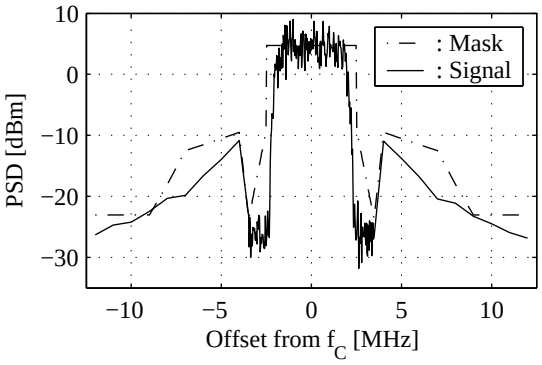

FIGURE 6: *Simulated spectrum mask with time offset of 16.3 nS, which makes $ACLR_1$ 33.2 dB and $ACLR_2$ 43.9 dB. f_C is the center frequency and the PSD is integrated over 30 kHz or 1 MHz, depending on the offset from f_C, as defined in [1].*

It is seen that the mask is violated at -9 MHz from f_C. This behavior means one should measure both ACLR and spectrum emission mask when dealing with polar modulators.

The experiment has demonstrated that timing offsets between phase and amplitude information cause spectral regrowth. However the envelope was applied at RF by changing the gain in a VGA in this experiment. The most power efficient way to apply the envelope is to use a switched PA [20]. Switching is known from GSM to cause spectral regrowth as well, but it remains to see how much noise power this generates in the downlink band.

3-3 Conclusion

The direct up-conversion transmitter and polar modulator have been investigated. The polar modulator has potential advantages when comes to output noise, but it remains to be seen how a switched PA behaves outside the desired band. The presented experiment indicates that more factors than time offsets are important. The author therefore assesses that more research needs to be done on polar modulators before all advantages and disadvantages with this architecture can be uncovered. The direct up-conversion transmitter requires an RF filter to meet the requirements to noise in the Rx band. Monolithic filters have been a subject of investigation for many years (see chapter 5). Therefore much information is available on this topic, although most of the publications aim at applications in receivers.

Even though the polar modulator may become a relevant alternative in time, the direct up-conversion transmitter is the architecture that is best suited for integration on CMOS at the time of writing. It is therefore decided to devote the remainder of the project to designing RF filters on CMOS for use in the direct conversion transmitter.

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4 FILTER TRANSFER FUNCTION

Chapter 3 investigates if direct conversion transmitter can be used for UMTS. It is found that an RF bandpass filter must be inserted in front of the PA to reduce transmitter noise in the UMTS Rx band. This chapter investigates how the required attenuation may be obtained. The UMTS Tx signal may mix with noise and create significant mixing products in the UMTS Rx band when passed through the PA [5]. The filter must therefore suppress noise in both the UMTS Rx band and the UMTS Rx image band. The UMTS Tx band is defined from 1920 MHz to 1980 MHz, while the UMTS Rx band is defined from 2110 MHz to 2170 MHz [1]. The UMTS Rx image band starts at 1670 MHz and ends at 1850 MHz. The filter must provide the gain and attenuation listed in Table 4.1 in these bands. The filter transfer function may also distort the transmitted signal and thus add to the resulting EVM [6, 4]. The budget for EVM made in chapter 3 allows the filter and the DACs to generate a combined EVM of 14.8 %. There is therefore plenty of margin for EVM, but being the result of two unknown contributions, this can not be used to specify a requirement to the filter alone. However, the EVM generated by the filter remains important and must be considered. The requirements to the filter are listed in Table 4.1.

TABLE 4.1: *Recapitulation of filter requirements.*

Parameter	**Requirement**	**Unit**
Gain at 1920-1980 MHz	> 3	dB
Attenuation at 2110-2170 MHz	> 12	dB
Attenuation at 1670-1850 MHz	> 12	dB
NF in the UMTS Tx band	< 10	dB
NF in the UMTS Rx band	< 15	dB
NF in the UMTS Rx image band	< 15	dB
ACLR $\pm$ 5 MHz	> 45	dB
ACLR $\pm$ 10 MHz	> 50	dB

Two different approaches to obtain the required attenuation are considered. Approach I involves maintaining the same filter transfer function no matter which Tx channel is used. This is illustrated in Figure 7a, where one filter transfer function is illustrated together with the PSD of modulated signals at three different center frequencies f_{C1-3}. In approach II the center frequency of the filter is tuned to match the Tx channel in use. This is illustrated in Figure 7b, where the PSD of the modulated signals from Figure 7a are repeated again. Here the center frequency of the filter is changed to match those of the signals.

In both cases some frequency adjustment may be necessary because of tolerances of on-chip components. The precision with which the frequency must be tuned may be different for the two approaches. This chapter investigates how the attenuation specified Table 4.1 can be obtained with the two approaches. Emphasis is put on:

- The number of resonators required to obtain the filter transfer function.
- The quality factor (Q) required in the resonators.

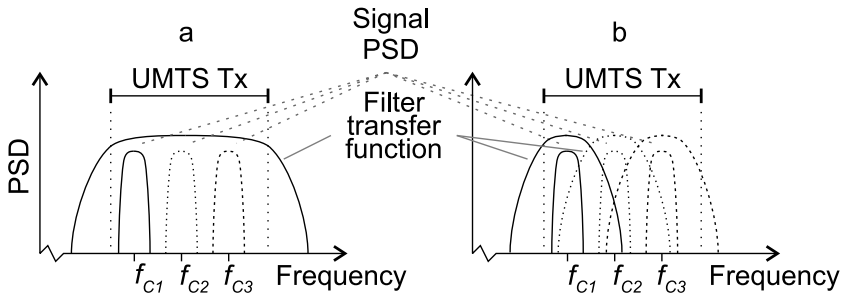

FIGURE 7: *Illustration of the two considered approaches. a: Approach I - the same filter transfer function is used for all transmit channels. b: Approach II - the filter transfer function is tuned to always provide maximal gain at the transmit channel.*

- The amount of EVM that results from the filter transfer function.
- Required frequency resolution and range of frequency adjustment.

In this thesis quality factor is defined as the ratio between center frequency and the half power bandwidth [2, 3].

4-1 Approach I

In approach I the same filter transfer function is used for all the Tx channels. It is possible to design filters with almost constant gain in the Tx band. However, such filters require higher order than filters with inband gain fluctuation to provide the required attenuation. Therefore 3 dB inband fluctuation is allowed in the filter transfer function although this may increase EVM. The fluctuation is specified by upper and lower limits to the inband gain. This is illustrated in Figure 8, where the maximum gain in the Tx band is increased to 6 dB and minimum gain is 3 dB as defined in Table 4.1. Figure 8 also shows the required 12 dB attenuation at the UMTS Rx and UMTS Rx image bands, but more attenuation is welcome here if available. The filter transfer function is therefore confined to the area marked with hatchings in Figure 8.

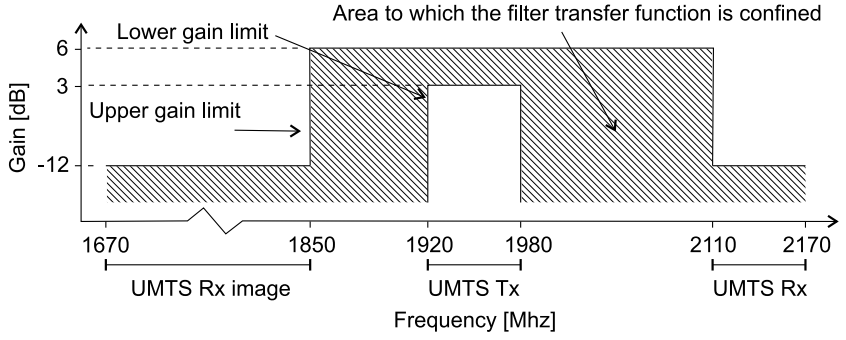

FIGURE 8: *Requirements to filter transfer functions designed for approach I.*

4-1-1 Required Number of Resonators

Design of filters with standard transfer functions is described very well in text books [2, 7]. The required order may be calculated from lowpass prototype transfer function approximations, that transforms to bandpass transfer functions as described in [2, p. 72-74]. The resulting bandpass transfer function is symmetric around the center frequency. In this work the transformation is used to obtain lowpass prototype transfer functions approximations based on the requirements in Figure 8. However, to make the bandpass transfer function symmetrical, 12 dB attenuation is assumed at 2050 MHz instead of 2110 MHz. The required order of Butterworth and Chebyshev approximations are found using the procedures in [2, p. 38-48], and verified in MATLAB^{TM}. The results are listed in Table 4.2. Since the filter transfer functions must be implemented with orders of integer numbers, the nearest integer above the calculated values are used.

TABLE 4.2: *Order required of lowpass prototype approximations to provide the desired attenuation.*

Approximation type	**Order according to [2]**	**Order according to MATLAB^{TM}**
Butterworth	$1.7 \approx 2$	2
Chebyshev	$1.5 \approx 2$	2

The 2nd order lowpass prototypes in Table 4.2 transform to 4th order bandpass filters. There are two ways of representing a bandpass transfer function in the s domain [2, 7]:

$$H(s) = G \prod_{n=1}^{2} \frac{s}{(s - p_n)(s - p_n^*)} = G \prod_{n=1}^{2} \frac{s}{s^2 + s\frac{\omega_{0n}}{Q_n} + \omega_{0n}^2} \tag{4.1}$$

where p_n and p_n^* are complex conjugate poles that describe the transfer function of one resonator. The n^{th} set of poles is obtained from the n^{th} pole in the lowpass prototype approximation. G is a constant that adjusts the filter gain, ω_{0n} - $2\pi f_{0n}$, where f_{0n} is the centre frequency and Q_n is the quality factor of the n^{th} resonator. Coefficients for the 2nd order lowpass prototype transfer functions are found in tables [2]. They are converted to the desired bandpass transfer function using MATLAB^{TM} implementations of the transformations described in [2].

4-1-2 Required Q and Tolerances on Centre Frequencies

Section 4-1-1 shows that both 2nd order Butterworth and Chebyshev approximations provide the required attenuation. The fact that the calculated order is not an integer, indicates that there is some tolerances on the filter bandwidth and centre frequency. This translates to tolerances on f_0 and Q in the resonators. The tolerances are investigated through the cases listed in Table 4.3, where the f_0 and Q required of each resonator is calculated for extreme cases using MATLAB^{TM}.

Case (a) to (e) are all Butterworth bandpass approximations. Case (a) is the target function. It is designed for a 3 dB bandwidth of 66 MHz. Cases (b) and (c) are designed for extremes of

TABLE 4.3: *f_0 and Q of the of resonators for the investigated filter transfer functions.*

Case	Center frequency [MHz]	3 dB BW [MHz]	f_{01} [MHz]	f_{02} [MHz]	Q_1	Q_2
a	1950	66.0	1927	1973	41.8	41.8
b	1950	60.0	1928.7	1971.1	45.9	45.9
c	1950	72.6	1924.3	1975.6	38	38
d	1953	66.0	1929.6	1976.2	41.8	41.8
e	1947	66.0	1923.6	1970.2	41.7	41.7
f	1950	≈ 61.0	1929.6	1970.2	31.5	31.5
g	1950	≈ 74.5	1923.6	1976.2	39	39

3 dB bandwidth. Cases (d) and (e) are designed for extremes of center frequencies. In cases (g) and (f) the frequency tolerances from cases (d) and (e) are applied, so f_0 of the two resonators are closest together (f) and furthest apart (g). In each case Eq. (4.1) is used to force the Q of the resonators to values that keep the transfer function in the area marked with hatchings in Figure 8. The gain characteristic of transfer functions (a), (f) and (g) are plotted in Figure 9 together with the limits defined in Figure 8.

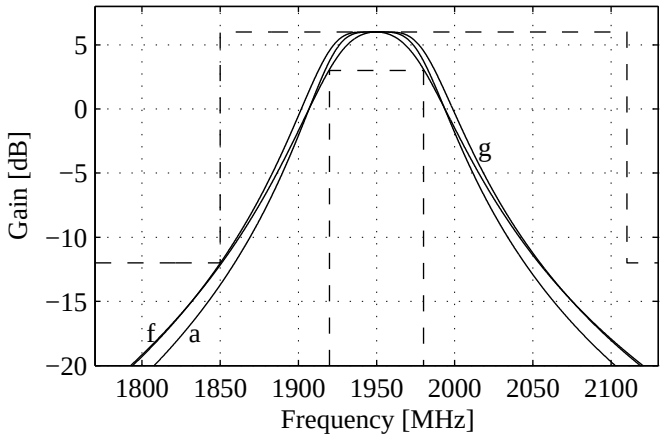

FIGURE 9: *Gain characteristic of transfer functions (a),(f) and (g) implemented in MATLAB^{TM}as specified in table 4.3. The dashed lines represent the limits for the transfer functions specified in Figure 8.*

The center frequency of the resonators changes approximately 6 MHz over the cases. This would indicate that the frequency should be adjustable within 6 MHz. However, the Q must be regulated between 31.5 and 46 with unity precision in order to keep the transfer function in the area marked with hatchings in Figure 8. The precision of Q may be relaxed if the precision of the center frequency is increased.

4-1-3 Estimated EVM

The transfer functions in section 4-1-2 are checked for EVM. The MATLAB^{TM} environment used in [4] is used to simulate EVM for these transfer functions. The transfer functions must meet the requirements at all extremes of f_0 and Q. The simulations must therefore include all the cases in Table 4.3. In UMTS the raster on f_C is 200 kHz [1]. Every possible value for f_C should be tested, but since the transfer functions change little over 200 kHz, the raster is increased to 1 MHz in this investigation. The largest EVM is obtained in case (c) for f_C equal to 1922 MHz. Here EVM is simulated to 2.9 % and estimated to 3.6 % using the approach described in [6]. Therefore approach I is not expected to cause any problems with EVM.

4-2 Approach II

Recall that the purpose of the filter is to attenuate noise in the UMTS Rx and UMTS Rx image bands. The most harsh requirements are made when the smallest obtainable duplex frequency is used. This happens when the transmitter operates at the highest Tx channel, while the receiver operates at the lowest Rx channel. In this case noise at 1850 MHz mixes to the Rx channel. In approach II it is acceptable to attenuate the part of the Tx band that is not used. This means that the 12 dB attenuation must be obtained 130 MHz from the pass band, in stead of 70 MHz as required in approach I.

4-2-1 Required Order

The concept of changing f_0 with the carrier frequency allows for the use of filters with one resonator of relative high Q or the use of several resonators with more moderate Q, operating close to the same frequency. The latter solution requires that the resonators are isolated from one another to work efficiently. To enable comparison with approach I, transfer functions with both one and two resonators are included in this investigation.

4-2-2 Required Q and Tolerances on Center Frequencies

The transfer function of a filter with one resonator may be expressed in the same manner as the transfer function with two resonators in Eq. (4.1). This representation enables the design of a transfer function from the knowledge of desired f_0 and Q alone. The transfer functions are designed in the MATLAB^{TM} environment used in section 4-1. The gain characteristics of several transfer functions with one resonator are shown in Figure 10. These transfer functions are designed with f_0 at (a) 1922 and (b) 1978 MHz. Tolerances of 3 MHz are added to f_0 at 1978 MHz. Both the gain and Q are adjusted so an average gain of 3 dB and the required attenuation is obtained. It appears that a Q of 45 is required to achieve this.

Transfer function (a) must provide at least 12 dB of attenuation at 1730 MHz. This is achieved with the suggested Q. Similar investigations are made for a filter transfer function that employs two resonators operating at the same frequency. Again a tolerance of 3 MHz is allowed on f_0 and Q are adjusted until the required attenuation is obtained for f_C equal to 1978 MHz. In this

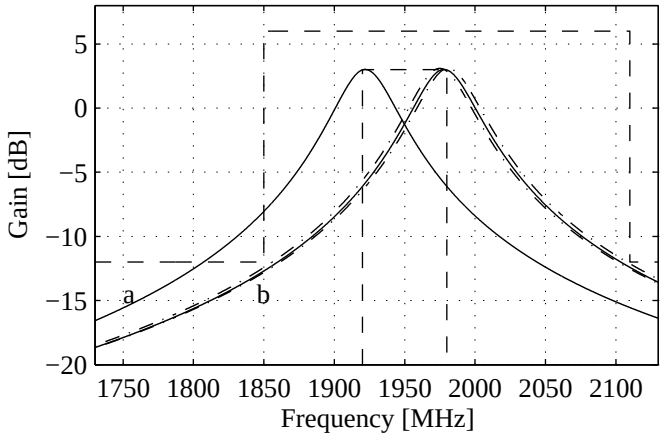

FIGURE 10: *Gain of transfer functions using only one resonator. Dotted lines indicated functions that implements tolerance on f_0. Dashed lines indicate limits specified in Figure 8.*

case a Q of 17.5 provides the required attenuation. The Q found for transfer functions with both one and two resonators represent minimum requirements. Less strict tolerances may be obtained if higher Q values are used.

4-2-3 Estimated EVM

The MATLAB^{TM} environment used in Section 4-1 is also used to estimate EVM of the transfer functions suggested here. The transfer functions do not change much in the desired band, as f_C is shifted. Significant differences in EVM are therefore only expected when frequency tolerances are applied. The simulations are therefore restricted to transfer functions designed for f_C of 1978 MHz. EVM is simulated and estimated to less than 1 % using [6] with 3 MHz frequency tolerances. This approach will therefore not cause significant contributions to EVM.

4-3 Conclusion

This chapter investigates the design of filter transfer functions that provide the attenuation required in the system analysis in Chapter 3. Approaches where the transfer function is kept constant and where it is tuned to match the carrier frequency are investigated. The first approach requires two resonators with Q up to 46. The second approach requires one resonator with a Q of 45. In both cases f_0 must be tunable with a precision better than 6 MHz. The second approach offers a solution that uses half the resonators. Requirements to noise and ACLR should therefore also be easier to meet with this solution. The penalty for is this tuning range. Both resonators must have tuneable center frequencies because of device tolerances, but the second approach has to add at least 60 MHz to that in order to follow the carrier of the signal. None of the approaches are expected to generate significant amounts of EVM. The choice must therefore be made according to the penalties for generating the required Q and what the tolerances are on the CMOS devices used in the resonators.

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5 RESONATORS

This chapter investigates the implementation of resonators for low noise and distortion applications. Chapter 4 concludes that a Q up to 46 is required in order to achieve the attenuation specified in chapter 3. The investigation presented here is based on a literature study and documents achievements so far. The literature considers gyration-C, recursive resonators and Q-enhanced LC resonators for use in radio frequency filters. First their functionality is described and then a comparison of theoretical dynamic range of the different resonator types is presented.

5-1 Implementation of resonators

This subsection presents the three types of resonators considered in the literature.

5-1-1 Q-enhancement

In Q-enhancement losses in resonators are compensated by adding a circuit with a negative impedance. Q-enhancement may be applied to single components or larger circuits like the one illustrated in Figure 11a. Ideally this resonator has infinitely high Q, but losses in the inductors and resistive loads limit the achievable Q. In Figure 11a losses are modelled with a parallel conductance G_0. Ignoring for a moment Y_{NE} the total impedance of the resonator circuit is [12]:

$$Z(\omega) = \frac{j\omega\frac{1}{C}}{(jw)^2 + j\omega\frac{G_0}{C} + \frac{1}{LC}} \tag{5.1}$$

where $\omega = 2\pi f$. The center frequency and Q in this LC resonator are found by [12]:

$$\omega_0 = \sqrt{\frac{1}{LC}} = 2\pi f_0 \tag{5.2}$$

$$Q_0 = \frac{\omega_0 C}{G_0} = \frac{1}{G_0\omega_0 L} \tag{5.3}$$

where $\omega_0 = 2\pi f_0$ and f_0 is the resonance frequency of the LC resonator. Assuming that Y_{NE} has the conductance: $-G_{NE}$ and no reactive part, the effective Q at f_0 can be found by substituting G_0 with $G_0 - G_{NE}$ in Eq. (5.3).

Literature reports implementations of Y_{NE} with transistors in the configurations illustrated in Figures 11b to h [9, 3, 17, 14, 8, 19, 16, 4, 21, 13, 5, 2]. FETs are used as in this section, but the circuits also work with BJTs. If only the trans-conductance (g_m) of the transistors is considered, the input admittance of the circuits in Figure 11b and c is [9]:

$$Y_{NE_{b,c}} = \frac{1}{Z_{NE}} = \frac{1}{Z_1 + Z_2 + g_m Z_1 Z_2} \tag{5.4}$$

It is seen that Z_{NE} has a negative real part if Z_1 and Z_2 have of the same type of reactance i.e. inductive or capacitive [17, 9, 3]. Although [3, 17] describe these circuits, actual implementations

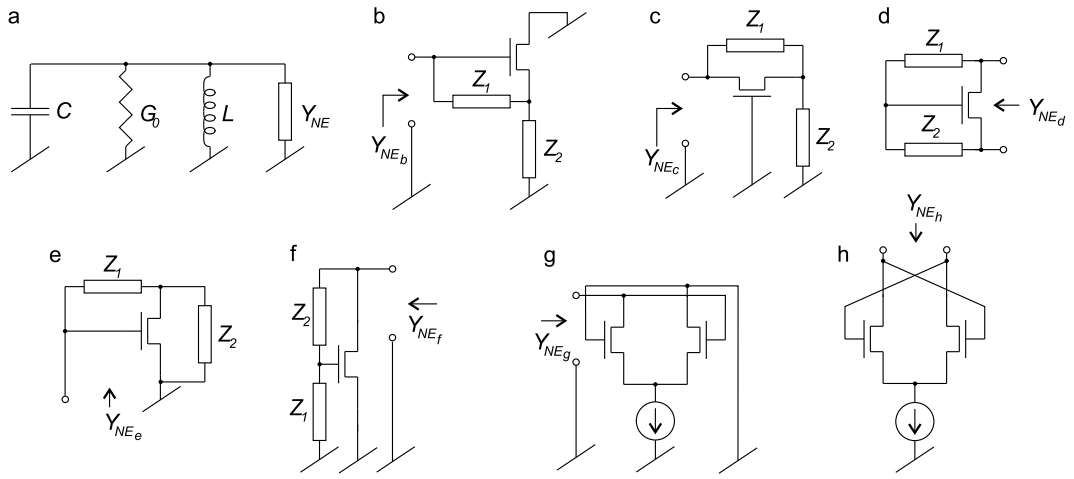

FIGURE 11: *a: LC resonator with losses and Q-enhancement. b to h: Examples of negative trans-conductance implemented using FETs [9, 3, 17, 14, 8, 19, 16, 4, 21, 13, 5, 2].*

are reported in [14, 8]. The admittance of the circuits in Figure 11d, e and f is [9, 8]:

$$Y_{NE_{d,c,e}} = \frac{1}{Z_1 + Z_2} + \frac{g_m Z_2}{Z_1 + Z_2} = [Z_1 + Z_2]^{-1} + \left[\frac{1}{g_m}\left(1 + \frac{Z_1}{Z_2}\right)\right]^{-1} \tag{5.5}$$

The circuits only produce negative conductance if Z_1 and Z_2 represent reactance of different types and if $|Z_1| > |Z_2|$.

The circuits presented so far use reactive components to help generate the negative admittance. This means that the admittance also has a reactive part and that the negative conductance changes with frequency. Figures 11g and h show examples of how a negative conductance may be obtained without the use of reactive components. Assuming that the two transistors are perfectly identical the admittance is [9]:

$$Y_{NE_{g,h}} = -\frac{g_m}{2} \tag{5.6}$$

While the circuit in Figure 11g implements a single-ended negative admittance, the circuit in Figure 11h implements a differential negative admittance. The circuit in Figure 11h is by far the most popular and different versions are found in [16, 4, 21, 13, 5, 2, 9]. Most of these references report performance of filters rather than LC-tanks. The center frequencies are 800 - 2400 MHz where Q of 50 - 400 are reported in single resonator filters, but only [21, 2] use CMOS. Here Qs of 80 at 830 MHz and 50 at 1800 - 2400 MHz are reported.

5-1-2 Gyration-C

Filters implemented using gyration-C (also referred to as g_m-C) resonators are quite popular in the literature [9, 10, 6, 11, 20, 22, 18]. The great advantage of this type of implementation is that no on-chip inductors are required. This saves die area and makes the circuit cheaper to manufacture than LC resonators. The inductive part is generated through impedance transformation of a capacitance. Figure 12 illustrates how a resonator may be designed from an ideal

gyration-C circuit. The gyration-C circuit is marked by the dashed box in Figure 12. It consists of minimum two trans-conductances, denoted g_{m1} and g_{m2}, and one capacitor denoted C_g. C is the capacitive part of the resonator and R_L is a resistive load.

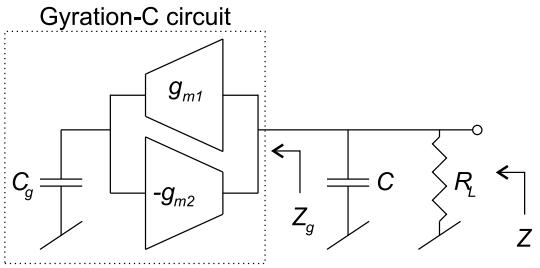

FIGURE 12: *Resonator circuit implemented using a simple gyration-C circuit. The dashed box marks the gyration-C circuit.*

The impedance of the gyration-C circuit is:

$$Z_g = \frac{j\omega C_g}{g_{m1}g_{m2}} \tag{5.7}$$

From Eq. 5.7 it is seen that the ideal gyration-C circuit generates an inductance L_g equal to $C_g/(g_{m1}g_{m2})$ and an infinitely high Q [22, 10]. The gyration-C circuit is sensitive to parasitics in the transistors [18, 22, 20] and un-intended phase shifts [10]. Such imperfections limit the achievable Q [18, 22, 10] and a possible resistive load decreases the Q of the resonator further. Assuming that the resistive load is the major contributor to Q degradation, the impedance of the resonator in Figure 12 is:

$$Z(\omega) = \frac{j\omega\dfrac{1}{C}}{(jw)^2 + j\omega\dfrac{1}{R_L C} + \dfrac{g_{m1}g_{m2}}{C_g C}} \tag{5.8}$$

and ω_0 and Q for a gyration-C resonator are therefore:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_g C}} \tag{5.9}$$

$$Q = \sqrt{\frac{g_{m1}g_{m2}}{C_g C}} C R_L \tag{5.10}$$

For $g_m = \sqrt{g_{m1}g_{m2}}$ and $C_g = C$, ω_0 and Q reduces to g_m/C and $g_m R_L$ respectively. The trans-conductance thus influence both the center frequency and Q in this resonator.

Reports of successful implementations are rare. [9] reports Q of 1000, achieved in a narrow band at 4.8 GHz using GaAs-MESFETs and a Q from 30-200 achieved from 1.5 GHz to 1.8 GHz in a GaAs HBT process. In both cases Q is calculated from the equivalents to Z_g in Figure 12, measured with S-parameters. No RF implementations on CMOS are reported, but [20] reports simulated Q of 41 at 900 MHz in a 0.35 μm CMOS process.

5-1-3 Recursive Filters

Recursive filters use feedback and gain stages to generate the transfer function of a resonator. Gain stages are most often represented with Operational Trans-conductance Amplifiers (OTAs) in the literature [7, 1, 15]. [7] holds an extensive analysis of Recursive filters implemented by OTAs. A difference OTA is defined as shown in Figure 13a [7, p 349]. Figure 13b-e show four different ways to implement a second order bandpass resonator using the OTA defined in Figure 13a. The resonator in Figure 13b employs a passive resonator circuit in the feedback path with an impedance of Z_R. The remaining resonators are all build from a general Tow-Thomas filter structure [7, p 354-356].

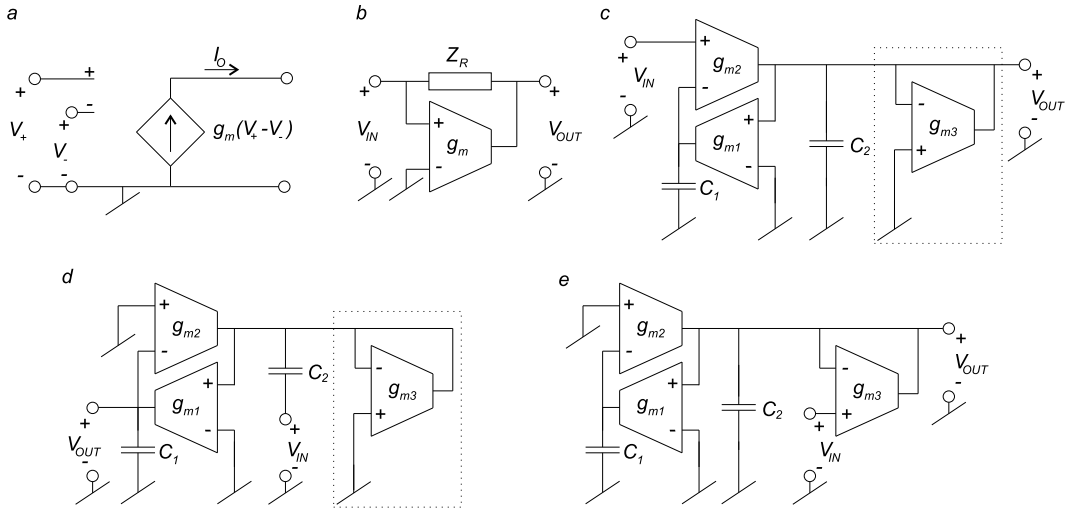

FIGURE 13: *a: simplified model for the used OTA. b-e: four examples of recursive filters implemented by OTA blocks.*

The transfer function of the resonator in Figure 13b is:

$$H_b(\omega) = \frac{V_{OUT}(\omega)}{V_{IN}(\omega)} = Z_R(\omega)g_m + 1 \tag{5.11}$$

If the non-compensated LC resonator, introduced in subsection 5-1-1, is used as feedback circuit, Z_R is equal to Eq. (5.1) and the transfer function is:

$$H_b(\omega) = \frac{(j\omega)^2 + j\omega\frac{1}{C}(G_0 + g_m) + \frac{1}{LC}}{(j\omega)^2 + j\omega\frac{G_0}{C} + \frac{1}{LC}} \tag{5.12}$$

It is not possible to obtain less than unity gain with $H_b(\omega)$. This means that attenuation only can be obtained with this filter, if it is applied before or after the resonator.

The problem of limited attenuation is not seen in the resonators in Figure 13c, d and e. The

transfer function for these implementations may be expressed by [7, p 356]:

$$H_n(\omega) = \frac{N_n(\omega)}{(j\omega)^2 + j\omega\frac{g_{m3}}{C_2} + \frac{g_{m1}g_{m2}}{C_1C_2}} \tag{5.13}$$

where n refers to the name of the circuit in Figure 13 and N_n for the respective circuits are:

$$N_c(\omega) = j\omega\frac{g_{m2}}{C_2}, \quad N_d(\omega) = j\omega\frac{g_{m1}}{C_1}, \quad N_e(\omega) = j\omega\frac{g_{m3}}{C_2}$$

According to [7], the nominator of circuit c should be the same as that for circuit b. However, analytical calculations verified in HP-ADS have shown that this is not the case. These circuits generate a bandpass transfer function with only one pole at $f = 0$. Notice the circuit in the dashed boxes in Figure 13c and d. This circuit is equivalent to a resistance of $1/g_{m3}\ \Omega$ [7, p 356]. In Figure 13c this circuit may be replaced by the load resistance R_L to ground. In this case g_{m3} may be replaced with $1/R_L$ in Eq. (5.13). Hereby the denominator in Eq. (5.8) is obtained. Since all the circuits share the same denominator, ω_0 and Q for all the circuits are:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{5.15}$$

$$Q = \frac{C_2}{g_{m3}}\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \tag{5.16}$$

Notice that $g_m = \sqrt{g_{m1}g_{m2}}$ and $C_1 = C_2$ means that $\omega_0 = g_m/C_{1,2}$ and Q $= g_m/g_{m3}$. This resembles ω_0 and Q of the gyration-C resonators described in subsection 5-1-2. Q is hence closely linked to the center frequency and gain of these filters.

The only literature found, that report implementations of recursive filters, use the type illustrated in Figure 13b [1, 15]. However, the feedback path consists of a more complicated circuit than the LC resonator used in the example above. [1] reports a Q of 14.9-16.6 in combination with a gain of 7.5-6.5 dB at 5.2-5.6 GHz in a 0.18 μm CMOS process .

5-2 Noise and Dynamic Range

Noise performance is important for the filters function in the transmitter. A noise budget is made in chapter 3, that specifies a maximal inband noise figure of 10 dB. The noise figure of a gyration-C resonator is [10, 9]:

$$NF_{gmC} = 1 + 4\gamma Q \tag{5.17}$$

if $g_{m1} = g_{m2}$, $C_1 = C_2$ and γ is the noise gamma effect of the transistors [9]. The noise figure for a Q-enhanced LC resonator is [9]:

$$NF_{Qenh} = 1 + 2\frac{Q}{Q_0}(1 + r_n, g_n) \tag{5.18}$$

where Q_0 is the un-compensated Q, and r_n and g_n are the relative noise resistance and admittance respectively of the Q-enhancement circuit [9]. They indicate how much noise the

circuit generates compared to a passive resonator with equivalent Q [9]. r_n and g_n depend on both the gamma effect in the transistors used on the Q-enhancement circuit and on how the Q-enhancement circuit is implemented [9].

So far the focus has been on noise. Another benchmark that is discussed in the literature is dynamic range. Although different approaches are used in the literature, the same major conclusions are reached. According to [6] the best dynamic range achievable in bi-quads, such as the ones used in gyration-C and recursive resonators in Figure 13c to e, is:

$$DR_{gmC} = \frac{v_{max}^2 C}{4kT\xi}\frac{1}{Q} \tag{5.19}$$

where v_{max} is the maximum non-saturated average voltage over the capacitors, k is Boltzman's constant, C is the total capacitance, distributed equally among C_1 and C_2, T is temperature in Kelvin, ξ is the noise factor of the gain stages, and Q is the loaded quality factor. An expression for the dynamic range of a Q-enhanced LC filter is reported as [11]:

$$DR_{Qenh} = \frac{v_{max}^2 C}{4kT\xi}\frac{Q_0}{Q} \tag{5.20}$$

The parameters are the same as used in Eq. (5.19), except for ξ, which in this case takes into account differences in implementation of the negative resistance. Furthermore the un-compensated Q in the LC circuit Q_0 is introduced.

The investigations presented in [6, 11, 10, 9] are all very superficial. They use a simple transistor model that combines all noise effects to one noise current source at the transistor output. The noise current depends on g_m in the transistor and the gamma effect, which takes into account differences in substrate and transistor type. Further more the upper limit of dynamic range is specified by some voltage, which is difficult to relate to specific linearity performance in the transistor. It is, however, beyond the scope of this work to remedy this. In spite of crude modelling, the reported investigations manage to show simple correlations between noise, dynamic range and Q.

5-3 Conclusion

This section investigates different types of resonators presented in the literature. Q-enhanced resonators or resonators with gyration-C inductors may both generate the required Q, while recursive filters may have difficulties in providing the required Q at the required frequency while maintaining a usable gain. This leaves the Q-enhanced LC resonator and the gyration-C resonator as suitable choices. Q-enhanced resonators are shown to have a theoretical noise performance that is superior to the gyration-C resonator. The Q-enhances LC resonator is therefore selected for the application in the UMTS Tx filter.

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6 Q-ENHANCEMENT CIRCUIT

Chapter 5 concludes that Q-enhanced LC resonators are the best way to implement high Q resonators in applications, where noise and linearity are important factors. Q-enhancement is achieved by compensating losses in passive LC resonators, using an active circuit that generates negative input impedance. This section describes a circuit that generates negative differential impedances.

An implementation of approach I in Chapter 4 was simulations using the design kit from the foundry. The filter was designed for 200 Ω differential source and load impedances and a 2.5 V power supply. Apart from two Q-enhanced resonators the filter consisted of three differential buffers implemented with FETs in common source configuration. Two buffers were used to isolate the resonators from the source and load impedances. The third buffer was used to isolate the resonators from each other. Capacitive coupling may be used for this [7, 1], but in this filter it would generate unacceptable losses. The simulations included noise and linearity. The requirements to noise figure in Table 4.1 were translated to average noise voltages in a 200 Ω load. Requirements to noise in the UMTS Tx band are thus 10 nV/$\sqrt{\text{Hz}}$ and for the UMTS Rx and Rx image bands: 1.4 nV/$\sqrt{\text{Hz}}$. The requirements to ACLR at ±5 MHz in Table 4.1 were translated to requirements to 3$^{\text{rd}}$ intermodulation suppression. The method used to estimate non-linear transfer functions in [6] translated the required ACLR to a 3$^{\text{rd}}$ intermodulation suppression of 37 dB. Type h in Figure 11 was the first choice of Q-enhancement circuit, but it was not sufficiently linear. Source degeneration with a small resistance improved linearity, but the fixed supply voltage limited the size of this resistance. A differential version of type b in Figure 11 appeared to offer better linearity at the cost of current consumption. The noise voltages were simulated to up to 13 nV/$\sqrt{\text{Hz}}$ in the Tx band and 2.4 nV/$\sqrt{\text{Hz}}$ in the Rx and Rx image bands. The target for noise are thus not full filled, but the simulations indicated that the output buffer was the largest noise source and this buffer may be omitted in a full integrated transmitter. Harmonic balance simulations indicated a harmonic suppression of 37 dB as desired.

It is necessary to know how the circuit reacts to factors like component size and biasing in order to make an efficient design. An expression equivalent to Eq. 5.4 was derived for the Q-enhancement circuit, but estimates didn't match simulations well. This chapter presents a more detailed expression for the differential admittance and investigates the effects of component size and biasing. Figure 14 shows a diagram of the differential circuit implemented with BJTs. The differential impedance is generated with C_1, C_2 and C_3 in combination with M_1 and M_2. L_1 and L_2 are not part of the circuit, but are included to illustrate how the bases of M_1 and M_2 are biased. M_3 and M_4 controls the current in the circuit and separates the emitters of M_1 and M_2 from ground. Although the circuit is shown with BJTs, it also works well with FETs.

The small signal representation of BJTs, shown in Figure 15, is used to simplify the analysis and help identify important impedances in the circuit.

This small signal representation is used to set up the equivalent small signal diagram for differential operation of the Q-enhancement circuit shown in Figure 16.

The small signal diagram includes Z_4 and Z_5, which represents parallel combinations of the

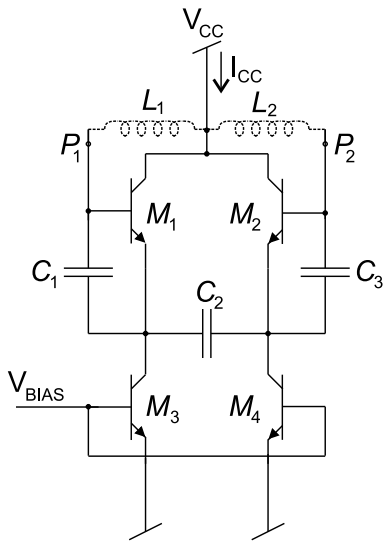

FIGURE 14: *Differential implementation of the type b Q-enhancement circuit shown in Figure 11, section 5.*

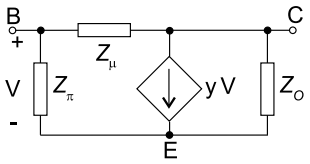

FIGURE 15: *Small signal representation of a BJT. The same basic representation is used for FETs.*

output impedances of the transistors. It will be shown later that these impedance are significant. The small-signal diagram is used to derive expressions for the differential admittance. Eq. (6.1) is a simplified expression, where Z_4 and Z_5 are omitted.

$$Y_{INs} = \frac{1}{(Z_{\mu M1} + Z_{\mu M2}) \parallel \left(Z_1 + Z_3 + Z_2 + \frac{1}{2}\left(Z_2 Z_1 y_{M1} + Z_2 Z_3 y_{M2}\right)\right)} \tag{6.1}$$

This expression has the level of detail reported in the literature for the single ended versions. If transistors are used, where only the trans-conductance g_m is significant and the circuit is symmetrical, the differential conductance at the frequency f reduces to: $-\frac{g_m}{2}\frac{1}{(2\pi f)^2 C_1 C_2}$, while the differential reactance reduces to a series connection of C_1, C_2 and C_3.

Eq. 6.2 is a more detailed expression for the differential admittance that includes Z_4 and Z_5 and hence the output impedance the transistors.

$$Y_{INc} = \frac{1}{(Z_{\mu M1} + Z_{\mu M2}) \parallel \left(Z_1 + Z_3 + \frac{Z_2\left(Z_4 + Z_5\right) + y_{M1} Z_1 Z_4 + y_{M2} Z_3 Z_5}{Z_3 + Z_4 + Z_5}\right)} \tag{6.2}$$

Refer to [4, 5] for details on how the small signal transistor representation is used in Eqs. 6.1 and 6.2. In the following the expressions are used to analyse the Q-enhancement circuit in

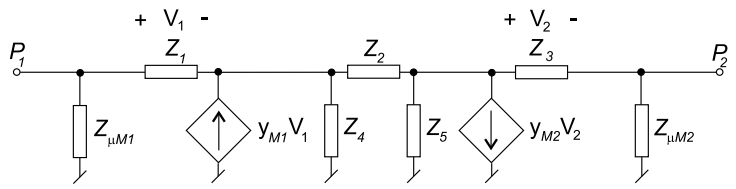

FIGURE 16: *Differential equivalent small signal diagram of the Q-enhancement circuit shown in Figure 14.*

Figure 14. The analysis includes a BJT implementation build from discrete components and a monolithic circuit implemented on a standard 0.25 μm CMOS process.

6-1 Low Frequency Experiment with Discrete BJTs

This section describes an experiment conducted with discrete components. The purpose of this experiment is validate Eq. (6.1) and Eq. (6.2) and investigate how the circuit reacts to changes in component size and biasing conditions. The circuit was implemented with discrete components. It was therefore possible to measure the used components individually to get the exact data for use in the expressions. The capacitors were implemented with standard 0402 components and the transistors were implemented with BC-847-S. The circuit was tested in the four configurations listed in Table 6.1. L_1 and L_2 were 220 nH during all tests.

TABLE 6.1: *Configurations used during the tests.*

Test	$\mathbf{C_1, C_2, C_3}$	$\mathbf{M_1, M_2, M_3, M_4}$
1	180 pF	BC-847-S
2	100 pF	BC-847-S
3	180 pF	2xBC-847-S
4	100 pF	2xBC-847-S

V_{BIAS} was increased from 0 V in steps of 0.1 V in each configuration of the circuit. 2-port S-parameters were measured at each biasing point and data measured on L_1 and L_2 was subtracted from the results. S-parameters were also measured the used capacitors and transistors. The transistors were biased as in the circuit during these measurements. This was done to determine the parameters in the small signal representation in Figure 15 for each biasing point.

6-1-1 Frequency Response

This section shows how well Eqs. (6.1) and (6.2) match measured results. Similar results are presented in [4] for selected bias voltages. The two cases listed in Table 6.2 are selected for further analysis.

Figure 17 shows the differential conductance between P_1 and P_2 in Figure 16 versus frequency. The measured differential conductance (G_{INm}) is calculated from the 2-port S-parameters measured on the circuit and compared with the real part of Y_{INs} calculated with Eq. (6.1) (G_{INs})

TABLE 6.2: *I_{CC} in Figure 14 in mA measured during the tests (adjusted via V_{BIAS} in Figure 14).*

Case	Test 1 & 2	Test 3 & 4
a	6.8	11.0
b	27.4	44.7

and the real part of Y_{INc} calculated with Eq. (6.2) (G_{INc}).

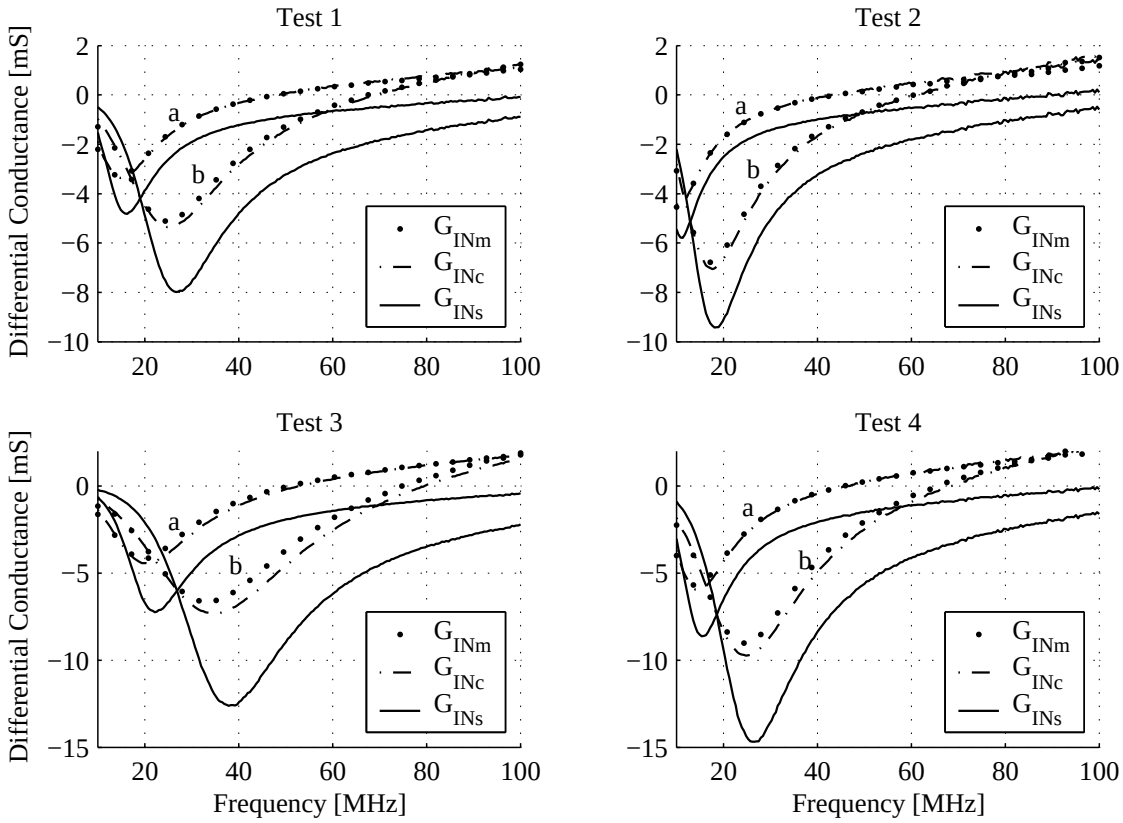

FIGURE 17: *Differential conductance between P_1 and P_2 in Figure 16 vs. frequency for tests 1 to 4 in Table 6.1. G_{INm} is the measured conductance, G_{INs} is estimated using Eq. (6.1) and G_{INc} is estimated using Eq. (6.2).*

It is seen that Eq. (6.1) estimates the differential conductance worse than Eq. (6.2) in all the tests. Z_4 and Z_5 are therefore significant in this circuit. It is further noticed that a distinct notch appears between 10 MHz and 40 MHz depending on biasing, capacitance and number of transistors. This notch appears because the transistor's trans-admittance has a significant reactive part.

6-1-2 Biasing

This section investigates how an increase of V_{BIAS} effects y and the differential conductance. This is done in order to see if there is an optimum value for trans-conductance in the transistors.

The trans-admittance of M_1 and M_2 in Figure 14 are measured and averaged for each bias point to form y. The measured and estimated differential conductance are plotted versus the magnitude of the trans-admittance $|y|$ in Figure 18. The plot is made at 40 MHz for all the tests defined in Table 6.1.

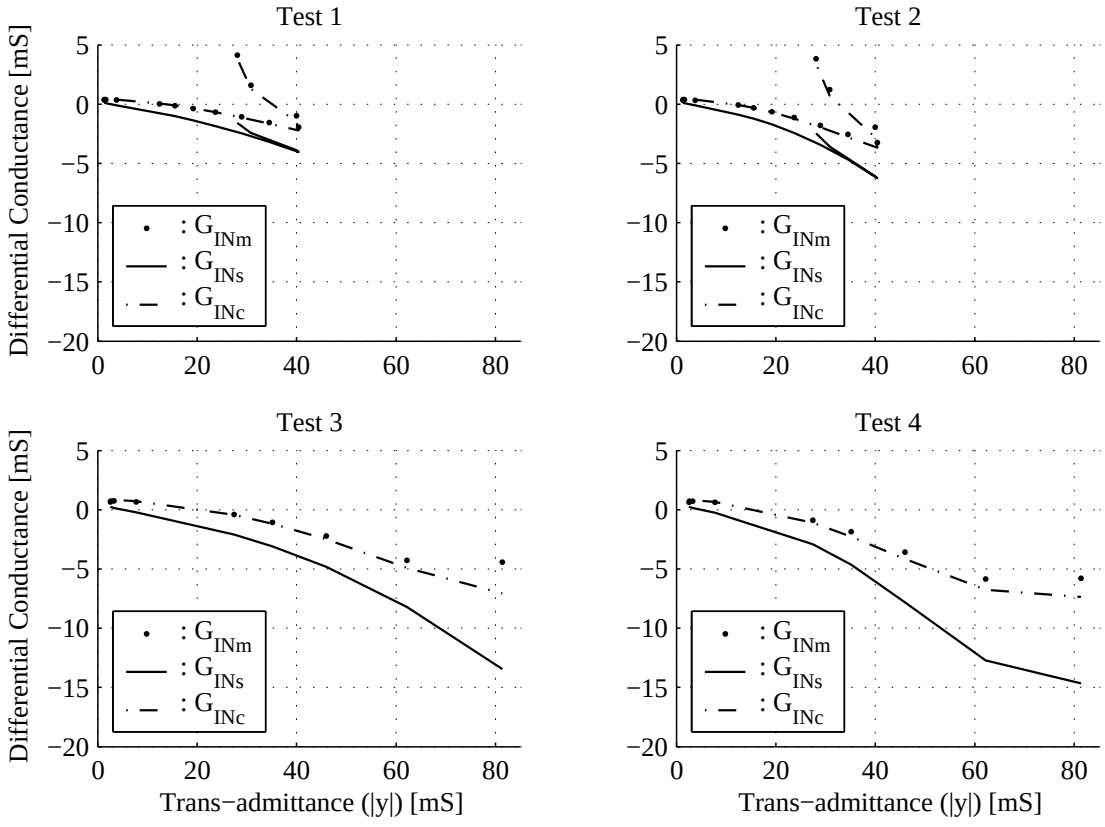

FIGURE 18: *Differential conductance between P_1 and P_2 in Figure 16 vs. $|y|$ of M_1 and M_2 for tests 1 to 4 in Table 6.1. G_{INm} is the measured conductance, G_{INs} is estimated using Eq. (6.1) and G_{INc} is estimated using Eq. (6.2).*

The trans-admittance is close to zero at V_{BIAS} = 0 V, but as V_{BIAS} increases so does $|y|$,- that is to a certain point, because in test 1 and 2 $|y|$ stops increasing when it reaches 40 mS. At this point V_{BIAS} is 0.9 V. It is seen that, with exception of the last measurement point, Eq. (6.1) returns to the conductance obtained previously as $|y|$ starts to decrease. The same is not the case for the measurements and Eq. (6.2). This indicates that Z_4 and Z_5 becomes increasingly significant in this region. Test 3 and 4 only includes eight biasing points. The bias voltage is not higher than 0.7 V and the transistors are therefore not operated in the region where $|y|$ started to decrease

in test 1 and 2. It is therefore concluded that decrease in differential conductance observed in tests 1 and 2 does not represent general behavior of the Q-enhancement circuit. Instead it is a result of the transistors being operated with decreasing efficiency.

6-1-3 Choice of Capacitance

This section investigates if one particular choice of capacitance is better than others. Although Eq. (6.1) overestimates the Q-enhancement capabilities, Figure 17 shows that it predicts the correct frequency of the notch. This indicates that the notch has something to do with the trans-admittance of M_1 and M_2. Eq. (6.1) is therefore used to establish a connection between trans-admittance (y) and capacitance. It is sufficient to use the average of the capacitance (C_a) together with y. A simplified expression for the differential conductance is:

$$G_{INe(f)} = \mathrm{Re}\left\{ -\frac{1}{\frac{y}{(2\pi f C_a)^2} + j\frac{3}{2\pi f C_a}} \right\} \tag{6.3}$$

$$= -\frac{(2\pi f C_a)^2 \,\mathrm{Re}\{y(f)\}}{(\mathrm{Re}\{y(f)\})^2 + (\mathrm{Im}\{y(f)\} + 6\pi f C_a)^2} \tag{6.4}$$

Eq. (6.2) is used to plot the differential conductance as a function of capacitance in [4]. Figure 19 repeats this and compares the notches with the results from Eq. (6.4) in order to shown that this expression estimates the notch correctly. The example uses the biasing conditions from table 6.2 and results are shown for operation at 40 MHz. As might be expected Eq. (6.4) estimates the differential conductance much lower than Eq. (6.2), but the largest magnitudes of the differential conductance are obtained with the same capacitances. Eq. (6.4) can therefore be used to determine the best choice of capacitance (C_{a_opt}) through an analysis of extremes. C_{a_opt} is found as:

$$C_{a\_opt}(f) = -\frac{|y(f)|^2}{6\pi f \mathrm{Im}\{y(f)\}} \tag{6.5}$$

Eq. (6.5) is used on the y measured on the transistors. The values of y and the resulting C_{a_opt} are listed in Table 6.3.

TABLE 6.3: *y and associated optimal capacitance.*

y	7.8-j13.4	18.7-j28.9	18.0-j30.2	33.5 - j52.4	mS
C_{a_opt}	23.7	54.2	54.1	97.6	pF

To test if these choices are in fact optimal, the differential conductance for different capacitances is calculated using Eq. (6.2) and Eq. (6.4). This is done with y parameters measured on the transistors in the cases listed in Table 6.3. The differential conductance obtained with the optimal capacitances from Table 6.3 is also calculated using Eq. (6.2) and Eq. (6.4). The results are marked with "$*$" and "x" respectively in Figure 19.

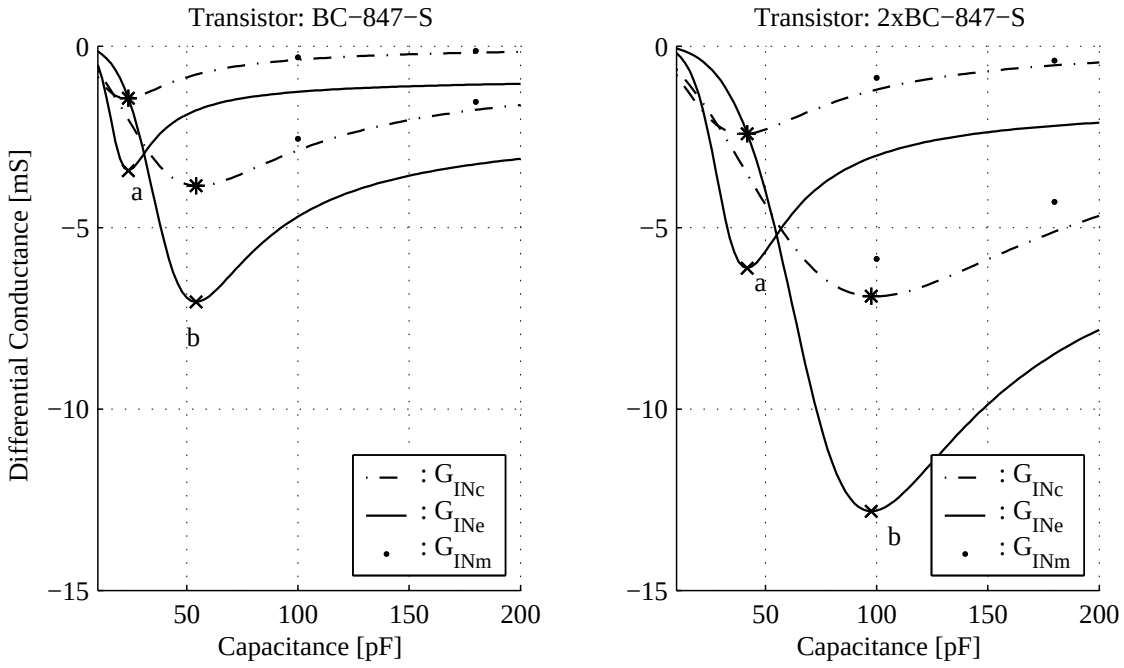

FIGURE 19: *Differential conductance at 40 MHz versus capacitance. a and b refer to biasing conditions in table 6.2. G_{INm} is the measured conductance, G_{INe} is estimated using Eq. (6.4) and G_{INc} is estimated using Eq. (6.2). "$*$" marks the conductance obtained with C_{a_opt} using Eq. (6.2) and "x" marks the ones obtained using Eq. (6.4).*

It is seen that at some point increasing the capacitance actually decrease the differential conductance. If larger magnitudes of differential conductance are required the only solution is to increase $|y|$ by either increasing the size of the transistors or changing the biasing.

The choice of capacitance was important because y had a significant reactive part. The used BJT had a transition frequency of 250 MHz [8], but the reactive part of y may be significant already at the cut-off frequency, which may be decades lower than the transition frequency. The reactive part of y was already significant at 10 MHz for the used transistor. A survey was made on commercially available RF BJTs. The transition frequencies of the transistors were between 20 and 70 GHz [9, 10, 11, 12], but S-parameters provided by the manufacturer revealed that the reactive part of y was significant at 1 GHz for all the transistor. The behavior observed in this section may therefore be critical for RF devices as well.

6-2 Monolithic RF CMOS implementation

This section describes a version of the negative resistance that has been implemented in a standard 0.25 μm 1 poly 5 metal layer CMOS process. Section 6-1 shows that the BJT implementation could be optimized through the choice of capacitance. This section investigates how the CMOS implementation reacts to changes in biasing and capacitor size, in order to establish if similar optimization can be done.

The supply voltage is 2.5 V. The circuit was initially design to compensate a 3 nH inductor with

a Q of 7.5 at 1950 MHz. The conductance G of an LC resonator with quality factor of Q and an inductor of L H is expressed by [3]:

$$G = \frac{1}{2\pi f_c LQ} \tag{6.6}$$

Since the inductor is likely to have much lower Q than the capacitor in a CMOS LC resonator, G is assumed only to belong to the inductor. The conductance of inductor is therefore 3.6 mS. Figure 20 shows a diagram of the implemented circuit as published in [5]. C_1, C_2 and C_3

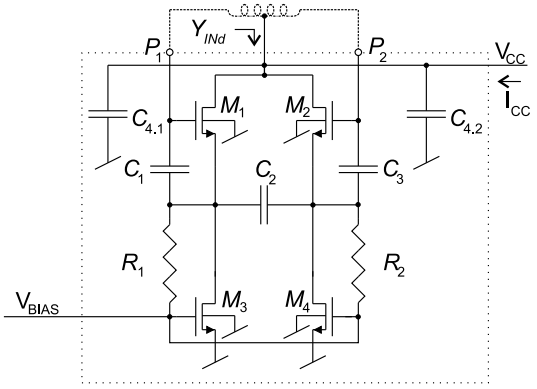

FIGURE 20: *Diagram of the Q-enhancement circuit that was implemented on the chip. The inductor was not implemented, but is included here to indicate that M_1 and M_2 were biased with V_{CC}.*

together with M_1 and M_2 generate a negative conductance between P_1 and P_2. M_3 and M_4 adjusts the biasing and R_1 and R_2 together with C_4 stabilize M_3 and M_4, which tended to oscillate at low frequencies. C_4 is implemented as two banks of capacitors to increase symmetry in the circuit. The reader is referred to [5] for more details of the implementation of this circuit.

The differential conductance is found for this circuit using the small signal diagram in Figure 16. However, Z_4 and Z_5 also includes R_1 and R_2 [5]. S_{11} and S_{22} exhibited the behavior seen in components with the potential for high Q operation. Exact measurements were therefore difficult to obtain. To obtain a best guess the measured differential conductance (G_{INm}) is averaged from several measurements. Since the circuit was implemented on a chip, it was not possible to measure the exact used components. Transistors, capacitors and resistors have been implemented in stand alone test fixtures on different lots and were measured there. 2-port S-parameters were measured in the transistors, which were implemented in common source configuration. The biasing conditions of the transistors were recreated as well as possible, but an exact match of conditions faced by M_1 and M_2 could not be obtained. The biasing voltages were estimated via the design tool kit provided by the foundry, which was found have accurate linear models of transistors [5].

6-2-1 Frequency Response

A simple expression for the differential conductance is needed to simplify the optimization of the circuit. However it must hold the information required to generate the observed behavior. This section investigates which level of detail is required to reproduce the behavior of the circuit. This is done in the frequency domain, based on the two cases defined in Table 6.4.

TABLE 6.4: *Biasing conditions of the two test cases*

Case	V_{BIAS} [V]	I_{CC} [mA]	Avg. Power consumption [mW]
a	0.6	8.3	20.8
b	0.8	32.2	80.5

A biasing point close to case a is used in chapter 7, where the circuit is used in an LC resonator. Case b is where the differential conductance was smallest. G_{INm} is shown in Figure 21 together with estimates made with Eq. (6.1) (G_{INs}) and Eq. (6.2) (G_{INc}). The conductance of the capacitors is important, while the reactance of y is small compared to the trans-conductance (g_m). The capacitors are of different sizes [5]. This is expressed by replacing C_2 with nC_1. The conductance is represented by the potential Q and the same value is used for all capacitors. The simplified version of Eq. (6.1) is:

$$Y_{INg(f)} = \frac{1}{\frac{2}{2\pi f C_1\left(\frac{1}{Q(f)}+j\right)} + \frac{1}{n2\pi f C_1\left(\frac{1}{Q(f)}+j\right)} + \frac{g_m(f)}{n\left(2\pi f C_1\left(\frac{1}{Q(f)}+j\right)\right)^2}} \tag{6.7}$$

The differential conductance $G_{INg(f)}$ is the real part of $Y_{INg(f)}$ as expressed by:

$$G_{INg(f)} = \frac{n\left(2\pi f C_1\right)^2\left(\left(g_m(f)+2\pi f C_1\frac{2n+1}{Q(f)}\right)\left(\frac{1}{Q(f)^2}-1\right)+4\pi f C_1\frac{2n+1}{Q(f)}\right)}{\left(g_m(f)+2\pi f C_1\frac{2n+1}{Q(f)}\right)^2+\left(2\pi f C_1(2n+1)\right)^2} \tag{6.8}$$

Eq. (6.7) is also included in Figure 21. C_1 and C_2 are estimated from measurements, averaged from 1 to 3 GHz. Eq. (6.7) use the same Q for both C_1 and C_2. The potential Q of the capacitors changed significantly over frequency. In Eq. 6.8 the used Q is the averaged of C_1 and C_2, calculated for each measured frequency.

Figure 21 shows that although Eq. (6.1) estimates larger magnitudes of differential conductance than Eq. (6.2), the relative error is not as large as in the experiments with BJT transistors. It is also seen that Eq. (6.7) estimates the notch at approximately the same frequency as Eq. (6.2). The important information is therefore maintained. The smallest differential conductance achieved at 1950 MHz is approx -2.8 mS. This is sufficient to enhance the Q of the intended inductor to 34.

6-2-2 Choice of Trans-Conductance

The experiment with BJTs showed that increasing the biasing voltage did not always increase the g_m in the transistors. This section investigates if the same effects are present in the CMOS implementation. To this end V_{Bias} was increased form 0 to 1.1 V in steps of 0.1 V. I_{CC} kept increasing during this sweep. 2-port S-parameters were measured at each biasing point. The differential conductance is calculated from these measurements and estimated from the measurements on the transistors. The results are shown in Figure 22 for 500 MHz (A) and 1950 MHz

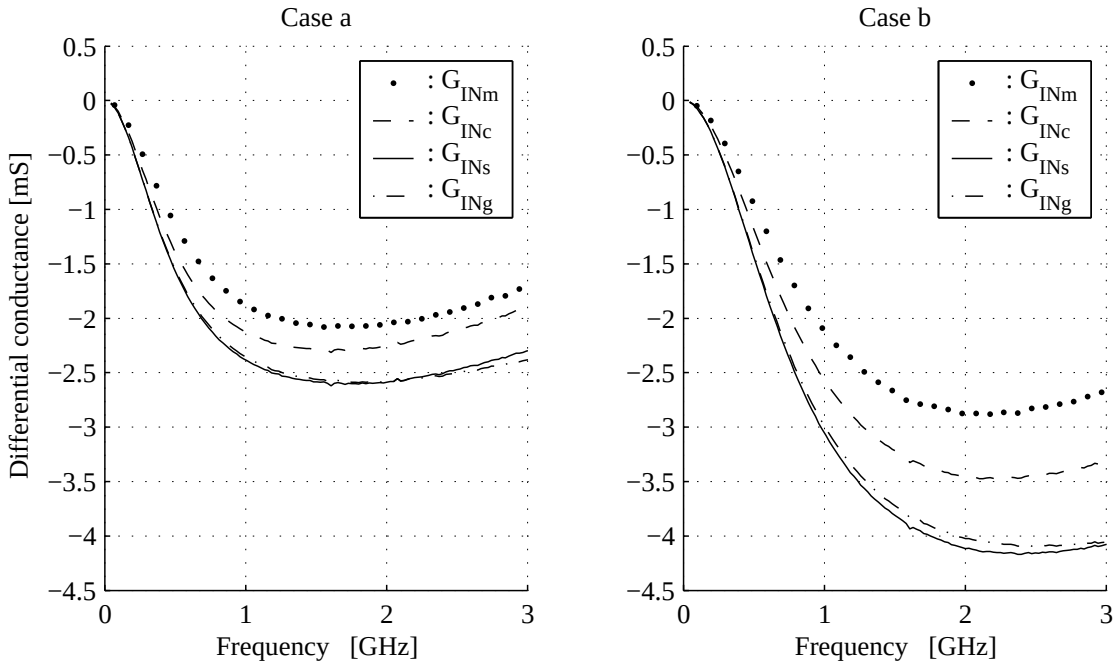

FIGURE 21: *Differential conductance versus frequency. Case a and b refer to Table 6.4. G_{INm} is estimated from measurements, G_{INs} is estimated from Eq. (6.1), G_{INc} from Eq. (6.2) and G_{ING} from Eq. (6.7).*

(B). The first point of G_{INm} is measured with all supplies off, resulting in a g_m equal to zero. The next point is measured with only the supply voltage on, but because of R_1 and R_2, the circuit is active and M_1 and M_2 presents a g_m of approx 10 mS. The remaining 7 measured points represent V_{BIAS} from 0.5 to 1.1 V in steps of 0.1 V. For some frequency f_s the optimum value of g_m $g_{m\_opt\_fs}$ is found through an analysis of extremes in Eq. (6.8):

$$g_{m\_opt\_fs} = \pm 2\pi f_s C_1 \frac{1 + Q(f_s)^2 + 2a + 2aQ(f_s)^2}{(1 + Q(f_s))Q(f_s)} \tag{6.9}$$

For Eq. (6.9) to apply Eq. (6.8) must be a good estimate of the differential conductance in the proximity of the notch. This is the case at 500 MHz, where the optimal conductance is estimated to 26 mS. The maximal achievable differential conductance is estimated from both Eq. (6.7) and Eq. (6.2). The results are marked by "x" and "$*$" respectively in Figure 22. At 1950 MHz $g_{m\_opt\_fs}$ is estimated to 103 mS, which is beyond the 46 mS achievable with the transistors. This point is therefore not included in Figure 22.

It is seen that Eq. (6.8) is close to Eq. (6.2) until g_m no longer increases with the biasing voltage. At 500 MHz the largest magnitude of differential conductance is obtained where g_m is 26 mS. This is close to the point estimated by Eq. (6.9). No measurements were made with the biasing that generated $g_{m\_opt\_fs}$. The differential conductance estimated with $g_{m\_opt\_fs}$ can therefore not be expected to appear exactly on the traces for G_{INc} and G_{ING}. At 1950 MHz the largest magnitude of differential conductance is obtained where the magnitude of the transadmittance is 45 mS. At this point g_m stabilizes even though V_{BIAS} is increased further. Here G_{INm} and G_{INc} starts to decrease while G_{ING} stabilizes. This indicates that the parasitics in-

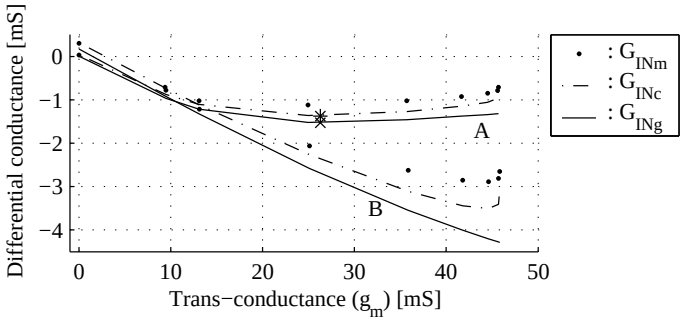

FIGURE 22: *Differential admittance versus the g_m at A: 500 and B: 1950 MHz. G_{INm} is estimated from measured S-parameters, G_{ING} is estimated from Eq. (6.7) and G_{INc} from Eq. (6.2). "$*$" marks the conductance estimated with $g_{m\_opt\_fs}$ in Eq. (6.2) and "x" marks the conductance estimated with $g_{m\_opt\_fs}$ in Eq. (6.7). Notice that "$*$" and "x" are lying almost on top of one another.*

cluded in Z_4 and Z_5 become more significant as the biasing voltage increases. Eq (6.8) does not include Z_4 and Z_5 and can thus not take this effect into account. The fact that an optimal choice for g_m is found in Eq (6.8) shows that increasing g_m alone will not always increase the magnitude of differential conductance.

6-2-3 Choice of Capacitance

Section 6-2-2 shows that an optimum exists for g_m on given frequency. This section investigates if an optimum exists for capacitance. Knowledge of the best choice of capacitance may help the designer to optimize the negative conductance of the circuit, if g_m for one reason or another, can not be changed. It is assumed that all the used capacitors have the same Q. This can be achieved if the capacitors are implemented as parallel connections of the same unit capacitor. The best choice of C_1, C_{1_opt}, is found through analysis of extremes in Eq. (6.8):

$$C_{1\_opt} = \frac{g_m Q}{6\pi f(2n+1)} \left(\frac{A-4}{Q^2+1} - \frac{3Q^2-1}{(Q^2+1)\,A} \right) \tag{6.10}$$

where

$$A = \sqrt[3]{27Q^4 + 18Q^2 - 1 + 3\sqrt{3\frac{27Q^4+10Q^2-1}{Q^2+1}}\,(Q^2+1)\,Q} \tag{6.11}$$

Figure 23 shows estimates and simulations of differential conductance as a function of capacitance at 1950 MHz. The test is conducted with a Q of 71 to get a value close the what has been measured on the capacitors. In order to provide measured data for this sweep, one circuit would have to be implemented for each measurement point. Instead capacitors are swept using the design kit provided by the foundry, as this was found to simulate the transistors well [5]. simulated values for differential conductance are denoted G_{INsim}. Finally G_{INc} and G_{ING} are calculated with the estimated C_{1_opt}. These are marked by "$*$" and "x" respectively and the one measured data point available for each bias point is marked by "$\cdot$".

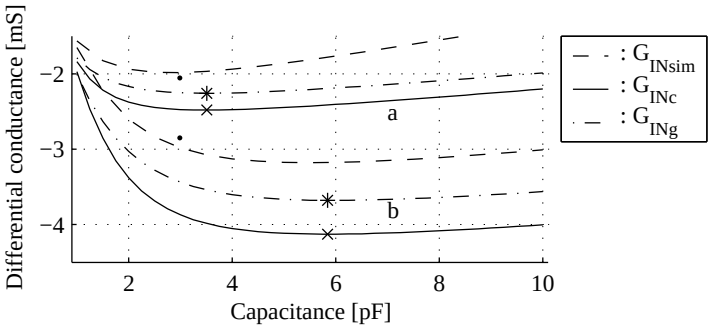

FIGURE 23: *Differential conductance as function of capacitance at 1950 MHz. a and b refer to the cases defined in Table 6.4. n is assumed to be 1. G_{INc} is estimated from Eq. (6.2) and G_{INg} estimated from Eq. (6.7), differential conductance estimated for C_{1_opt} using Eqs. (6.2) and (6.7), are marked with "$*$" and "x" respectively. The only available measured data is marked by "$\cdot$".*

The estimates of C_{1_opt} fits Eq. (6.2) well, but they are 0.5 - 1 pF larger than indicated by the simulations. The differential conductance changes slowly near the notch, so the resulting difference in the differential conductance is not significant. It may therefore be desirable to choose capacitances smaller than the optimal choice in order to save space and reduce the capacitive impedance of the Q-enhancement circuit.

6-3 Conclusion

This chapter investigates two implementations of a proposed Q-enhancement circuit. Both were found to have notches in the frequency domain, but the notches were caused by different factors. In the BJT experiment the reactive part of the transistors trans-admittance was the significant factor, while the conductance of the used capacitors was the significant factor in the CMOS implementation. In both cases the optimal choice of capacitance was estimated from simplified expressions and in both cases it was found that infinitely low differential conductance can not be obtained only by increasing the capacitance. The existence of an extreme in Eq. (6.8) shows that the same is the case for g_m in the CMOS implementation. Both experiments also showed that at some point, increasing the biasing voltage and hence DC current no longer increases the trans-admittance in the transistors. If this point is reached, the only option is to increase the size of the transistors, as done in the experiment with BJTs, but the extreme point found in Eq. (6.8) shows that even this has a limit in the CMOS implementation.

The scientific contributions provided through this part of the project are:

- Demonstration that the suggested differential circuit indeed can generate a negative differential conductance, both when implemented with discrete components and on a standard CMOS process.
- An analytical expression that describes the differential conductance of the circuit and includes transistor output impedances.

- Demonstration that the performance can be optimized through the right combination of capacitance and trans-admittance.

The Q-enhancement circuit was proposed because of its assumed potential for high linearity or low noise [2]. However this assumption was based of an analysis that did not include the transistors output impedances. This work has demonstrated that the transistor output impedances are significant for linear operation. These parasitics should therefore be included in analysis of noise and linearity.

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7 Q-ENHANCED RESONATOR

This chapter presents results obtained with an experimental implementation of a Q-enhanced monolithic LC resonator, using the Q-enhancement circuit described in Chapter 6. Although the literature holds may examples of monolithic resonators, none uses the Q-enhancement circuit presented here. The experiment reveals weaknesses and forces of this used Q-enhancement circuit. The resonator was designed to have a mid range center frequency (f_C) of 1950 MHz and a tuning range of approx 100 MHz using the design kit available form the foundry. However this was not obtained in the measurements. The simulated capacitors were 10 % smaller than measurements indicated. Further more errors of 100 % in the simulation of the capacitance in transistors in weak accumulation mode meant that the simulated tuning range was 10 MHz larger than measured. Although such errors might be expected, they are too large to for an efficient design of high Q resonators. In the following measured data are therefore used for these components in the simulations.

Figure 24 shows a diagram of the implemented circuit. The LC resonator consists of transistors M_1 through M_{10} with de-coupling capacitors C_1 through C_{10} and the inductor L_1. The Q-enhancement circuit consists of transistors M_{11} through M_{14}, capacitors C_{11} through C_{14} and the resistors R_1 and R_2. Refer to [4, 5] for more details on this circuit.

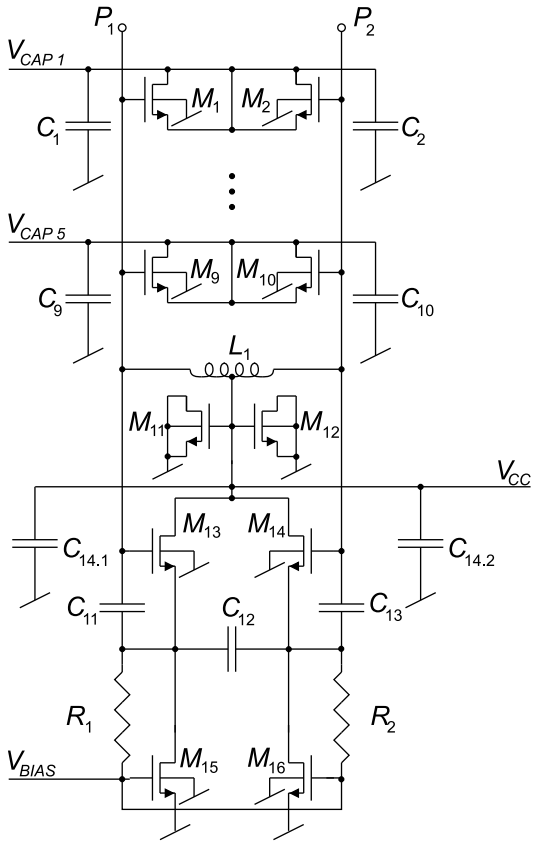

FIGURE 24: *Diagram of the implemented Q-enhanced LC resonator.*

7-1 Results

The inductor was measured to 5.6 nH and had a potential Q of about 7.5 [5] at 1850 MHz. From Eq. (6.6) the conductance of the inductor is found to be approximately 2 mS at this frequency. The varactors have a high potential Q and their conductance is thus insignificant. The Q-enhancement circuit is capable of compensating for up to 2.8 mS, so in this case it may be backed off. Compensation is achieved with a bias voltage of 0.58 V and a current consumption of 6.9 mA from a 2.5 V supply. The circuit therefore consumed 17.3 mW in this configuration. Figure 25 shows simulated and measured differential conductance and reactance on a frequency in the middle of the resonators tuning range. The reactance is zero at the center frequency of LC resonators [3]. The center frequency is thus approx. 1820 MHz. At this point the conductance was approx. 0.2 mS so the Q of the resonator was about 80. However, Q of this magnitude are difficult to measure in a 50 Ω system.

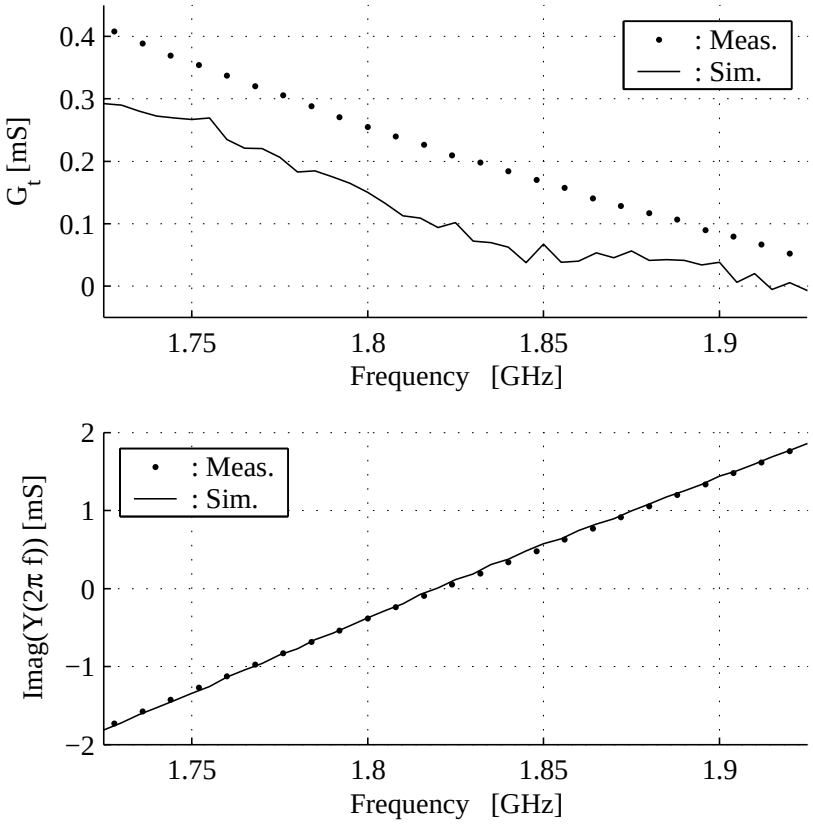

FIGURE 25: *Differential conductance and reactance when the resonator is operated at mid range. Dots are measured results and lines are simulated.*

Simulated and measured frequency range and Q are listed in Table 7.1. The frequency step size is between 2 and 4 MHz depending on whether it is measured in the upper or lower frequency ranges.

TABLE 7.1: *Simulated (sim.) and measured (meas.) corner and mid values for f_C and resulting Q factor.*

f_{Cc} **sim. [MHz]**	$Q_{\textbf{sim.}}$	f_C **meas. [MHz]**	$Q_{\textbf{meas.}}$
1776	87	1779	53
1825	153	1822	78
1872	298	1870	122

7-2 Discussion

The circuit is more than capable of compensating for the inductor used in the experiment, but f_C is not as expected. This is mainly because the implemented (MIM) capacitors were larger than the design kit estimated. The resonator is sensitive to tolerances on both capacitors and g_m in the transistors. Tolerances on g_m mainly influence the Q, while the capacitors influence both the Q and f_C. Automated tuning schemes such as voltage controlled filter tuning and voltage controlled oscillator tuning exists [1]. Such schemes may control both frequency and Q, but the required tuning range must be available in the resonator. The simulations presented here were conducted using data measured on stand alone implementations of the capacitors C_{11} and C_{12}. C_{11} was implemented on one lot and C_{12} on another. Although the statistical background is limited, the experiment indicated some repeatability in the MIM capacitors. Even though the measurements of the LC resonator were conducted on a 3$^{\text{rd}}$ lot, the data measured on the capacitors still provided a good match when used in the simulations. Simulations of weak accumulation mode of the FETs used in the varactor bank were also inaccurate, but f_C was more sensitive to errors on the capacitors than this error.

The use of measured data in the simulations provided a good estimate of f_C, but tolerances are not known. If the design was to be made for the tolerances in the design kit, the frequency tuning range of the resonator would have to be increased. This requires that a larger varactor bank is implemented, but since the varactors are capacitive in weak accumulation mode, this is not possible in the present configuration. The problem with the design is that the size of C_{11} to C_{13} and L_1 sets limits to how large a capacitance may be added in the varactor bank. However, there are several ways to remedy this:

- The center frequency f_0 of an LC resonator is [3]:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{7.1}$$

  By reducing the size of the inductor, the size of the capacitance may be increased. This means that the varactor bank may generate a larger percentage of capacitance, but on the other hand, it would also require a larger shift in capacitance to change f_0. The conductance in the LC resonator is inverse proportional with the used inductance as seen in Eq. (6.6). This means that the Q-enhancement circuit would have to provide a smaller differential conductance to compensate for the same Q and this in turn means higher current consumption.

- Figure 23 indicates that the Q-enhancement circuit can provide a differential conductance

of -2 mS with capacitors of 1 pF, when the transistors are biased for maximal g_m. This reduces the capacitance significantly, but it will also increase the current consumption.

- If the capacitors and transistors were ideal, the imaginary part of Eq. (6.1) would only be a series connection of C_{11}, C_{12} and C_{13}. In this case the overall admittance could be reduce by making one of these capacitors smaller and compensate for the lack of Q by increasing the others. The transistors are not ideal, but the capacitors are dominant so a similar effect is expected. However, this will also change the performance with respect to noise and linearity [2].
- The circuit could be scaled both in capacitance and transistor size. In this manner a more efficient operating point may be found for the transistors and smaller capacitors may be applied. However, this approach may also change the performance with respect to noise and linearity.

7-3 Conclusion

The Q-enhancement circuit has been used in a monolithic LC resonator. The circuit was more than capable of compensating for the losses in the used inductor, but this is not surprising as the circuit was not designed for that particular inductor. The LC resonator proved to be sensitive to tolerances particularly on the capacitors used in the Q-enhancement circuit. This means that a large tuning range is required to compensate for tolerances or poor models of the capacitors. The use of capacitors means that the circuit exhibits a significant capacitive differential impedance. This limits the size of the varactor bank and thus the frequency tuning range. An alternative is to use measured data in the simulations as demonstrated in this chapter. This approach has estimated the center frequency at 1850 MHz with an error of only 3 MHz, which is sufficient to make an efficient design, but it requires that the components have been implemented in stand alone fixtures before the design is made. It is always important not to apply more capacitance than necessary. The author believes that the analysis of optimization of the circuit presented in Chapter 6 may help the designer to make he best choice of capacitance.

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8 CONCLUSION

This conclusion first recollects the important results obtained during the Ph.D. project. Then the projects significant scientific contributions are listed and finally the author assesses which tasks remain, before the best approach to implement UMTS transmitters on CMOS can be identified.

8-1 Important Results

This section recollects the important results obtained during the project.

- At the time of writing, the direct up-conversion transmitter appears to be the best architecture for integration on CMOS.
- The UMTS receiver sets the most harsh requirement to the transmitter output spectrum. An RF bandpass filter must be inserted before the power amplifier to meet this requirement.
- The RF bandpass filter must provide 3 dB gain in the uplink band and 12 dB attenuation at frequencies 70 MHz below the uplink band. This must be achieved without adding significantly to output noise and ACLR.
- Two approaches to obtain the required attenuation are identified. Both can be implemented with resonators with a quality factor of about 46 and 6 MHz precession of the center frequency. The designer may chose between deploying two such resonators, with enough tuning range to compensate for tolerances, or one resonator with a tuning range at least 60 MHz wider than this.
- If noise and linearity are important factors, Q-enhancement is the best solution to implement resonators with high quality factors on CMOS.
- A Q-enhancement circuit is implemented on CMOS. It generates a differential conductance of -2.8 mS at 1950 MHz with a power consumption of 80 mW.
- An LC resonator with the Q-enhancement circuit described above is implemented on CMOS. The center frequency of the resonator can be tuned from 1780 MHz to 1870 MHz in steps down to 2 MHz. The Q-enhancement circuit improved the quality factor from 7.5 to beyond 50 with a power consumption of 17 mW. The center frequency was simulated with a precision of approximately 3 MHz.

The frequency range and quality factor required in the RF filter could be obtained. It is therefore assumed that the filtering required in the direct up-conversion transmitter for UMTS can be obtained on CMOS.

8-2 Scientific Contributions

The project has generated the following scientific contributions:

- An experimental analysis of how selected circuit imperfections affect EVM and ACLR in uplink signals for UMTS.
- Analytical expressions that relate EVM to amplitude and phase imbalance in the I and Q branches. The expressions take into account the phase and amplitude adjustments conducted during calculation of EVM.
- An analysis of requirements to functional blocks in direct up-conversion transmitters for UMTS user equipment.
- Demonstration that a differential circuit, based on BJTs in common collector configuration and capacitors, can generate negative differential conductance.
- An analytical expression for the differential admittance of the Q-enhancement circuit mentioned above, that takes the output impedances of the transistors into account.
- Demonstration that the Q-enhancement circuit also works on CMOS and that the analytical expression also improves estimates when applied to CMOS circuits.
- Demonstration that the Q-enhancement circuit does enhance the quality factor of an LC resonator.
- Demonstration that the center frequency of an LC resonator with a high quality factor can be simulated with great precision, using data measured on stand alone implementations of the used passive components.

The project has therefore made scientific contributions to the understanding of the UMTS systems and the design of Q-enhancement circuits for RF operation on a standard CMOS process.

8-3 Future Work and Research

Many questions concerning the implementation of transmitters for UMTS on a standard CMOS process have been answered during this project. However, many more questions need to be answered before the most efficient approach can be identified. This applies both to the architecture studies and design of Q-enhanced LC resonators.

The polar modulator was mentioned as a potential competitor to the direct conversion transmitter. This architecture is not mature so it will take some efforts before it is documented as well as the case is for the direct up-conversion transmitter at the time of writing. In the mean time the direct conversion transmitter appears to be the best choice. However, there is also work to be done on integration of filters on CMOS before the direct up-conversion transmitter can be integrated. An LC resonator with a center frequencies in the UMTS uplink band remains to be implemented. It is possible to simulate the frequency range to within 3 MHz of measurements and from the knowledge obtained on the design of the Q-enhancement circuit, the author thinks that an LC resonator with the desired center frequency can be designed. The Q-enhancement circuit was chosen for its potential noise and linearity performance. However, an analysis of noise and linearity that includes the transistor output impedances must be conducted for both this circuit and competing circuits in order to determine which one would be the best choice for the intended application.

RF Requirements for UTRA/FDD Transceivers

P. Madsen, O. K. Jensen, T. Amtoft, R. V. Reynisson, J. H. Mikkelsen, S. Laursen, C. R. Iversen, T. E. Kolding, T. Larsen and M. B. Jenner

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Aalborg, Denmark, pp. 197 - 202, September 2001.

RF Requirements for UTRA/FDD Transceivers

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Abstract

Unified RF requirements are derived for an UTRA/FDD compliant mobile transceiver. Consideration of system issues, multi-mode operation, and interfacing concerns leads to detailed receiver and transmitter calculations based on existing UMTS specifications. Finally, compliant and design-compatible transceiver requirements are derived.

Keywords

RF Transceiver, UTRA/FDD, transceiver requirements, direct up/down conversion.

1. Introduction

The UTRA/FDD mobile standard provides an improved platform for personal communications including voice, data, and multimedia services compared to current 2G systems. In order for UTRA/FDD to retain a competitive advantage, high-performance and low-cost *user equipment* (UE) must be made available to the general public. In this work, unified UTRA/FDD UE transceiver requirements are derived on block level, based on previous work for the receiver branch [1] and ongoing work for the transmitter branch [2].

2. Duplex Aspects

As UTRA/FDD is based on *frequency division duplex* (FDD), the required isolation between *transmitter* (Tx) and *receiver* (Rx) can only be provided by means of a duplex filter. The performance of the duplex filter is very important for the transceiver requirements and since the available physical size is limited, several design compromises apply:

- A low insertion loss in the Tx-band is difficult to combine with a high Tx-Rx isolation in the Rx-band.
- A low insertion loss in the Rx-band is difficult to combine with a high Tx-Rx isolation in the Tx-band.

The transmitter-induced noise level at the receiver input (Rx-band) is determined by the transmitter noise level and the duplexer isolation. A level of -111 dBm/3.84 MHz is shown in later sections to give an acceptable degradation of receiver sensitivity. To reduce insertion loss at Tx, the duplex filter should only attenuate noise generated by the *power amplifier* (PA) itself, while noise generated before the PA is filtered inside the Tx-chain. Assuming (i) a class 3 transmitter with a maximum output power of 24 dBm and (ii) a Tx-insertion loss of 2 dB, duplexer isolation of 37 dB is needed. Also, it need to be considered that a Tx-leakage signal may disturb the Rx-band because of receiver nonlinearities. With 50 dB of Tx-Rx isolation, the leakage level from a class 3 transmitter becomes -24 dBm which is realistic in combination with a 3 dB Rx-insertion loss. The assumed duplexer performance data is summarized in Table 1.

Parameter	Requirement
Tx-Ant attenuation (Tx-band) [dB]	< 2
Rx-Ant attenuation (Rx-band) [dB]	< 3
Tx-Rx isolation (Rx-band) [dB]	> 37
Tx-Rx isolation (Tx-band) [dB]	> 50

Table 1: Duplex filter requirements.

3. Receiver

To ensure that the receiver has adequate performance it must meet requirements for a number of tests defined in the UTRA/FDD standard [3]. For each of these tests, a BER of 10^{-3} must be achieved at a user bit rate of 12.2 kbps. To meet this, a $(E_b/N_t)_{\text{eff}}$ of 5.2 dB is needed [4]. A margin of 0.8 dB is suggested [4] to cover for baseband implementation imperfections. It is therefore decided to use 6 dB as the target value for $(E_b/N_t)_{\text{eff}}$. It is assumed that any disturbing signals, such as distortion products, may be treated as noise. This allows thermal noise and any distortion products to be combined in a single *power spectral density* (PSD), N_t. It is further assumed that any signal that is not on the desired channel is removed by filtering in the digital baseband part. In order not to overload the ADCs, such signals are attenuated to the power level of the desired signal before sampling takes place. Several disturbance mechanisms are active so a disturbance power budget must be chosen. Further, it should be noted that all Rx calculations relate to the Rx chain following the switch/duplexer arrangement, unless otherwise specified. This implies that power levels specified in the standard are adjusted for the loss in the duplexer. As an example, during sensitivity testing, a wanted signal of -117 dBm is specified. This value is adjusted to -120 dBm during calculations to take the estimated duplexer loss of 3 dB into account.

3.1. Noise Figure

The sensitivity requirement is specified for a data channel (DPCH) signal power, S_i. Based on the required $(E_b/N_t)_{\text{eff}}$ the acceptable noise and distortion power in a channel bandwidth,

P_{acc}, is calculated as

$$\begin{aligned} P_{acc} &= S_i - (E_b/N_t)_{\text{eff}} + 10 \cdot \log(PG) \\ &= -120 - 6 + 25 = -101 \text{ dBm}, \end{aligned} \quad (1)$$

where the processing gain, PG, is given as chip rate over bit rate. The chip and bit rates equals 3.84 Ms/s and 12.2 kbps, respectively. The actual bit rate that should be used is 15 kbps as this is the bit rate prior to the encoding. However, some degree of coding gain is expected and for that matter 12.2 kbps is used. The Tx-leakage signal with varying envelope results in distortion products located at baseband due to even-order nonlinearities in the receiver. As a result, P_{acc} consists of Rx-noise, $P_{Rx,N}$, Tx-noise, $P_{Tx,N}$, and distortion products due to Tx-leakage and Rx-nonlinearities. In the special case where the Tx-signal is turned off, $P_{Rx,N} = P_{acc}$ resulting in a Rx noise figure of 7 dB. To make room for any Tx-signal noise and distortion effects, the Rx noise figure must be reduced. As a compromise, a 1 dB reduction ($P_{Rx,N} = P_{acc}$ - 1 dB) is accepted. Allowing the remaining noise and disturbance power to be shared equally between $P_{Tx,N}$ and $P_{Tx,D}$, they must display disturbance powers less than -111 dBm/3.84 MHz. This disturbance budget leads to the power levels illustrated in Figure 1.

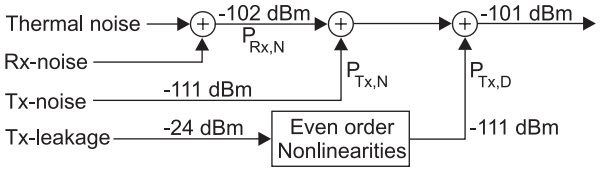

Figure 1: Illustration of the noise and disturbance power distribution.

In other tests, the Tx-power is reduced to 20 dBm for a power class 3 transmitter. This only gives a minor reduction in Tx-noise and is therefore neglected in the following calculations.

3.2. Second-Order Intercept Point

The presence of strong modulated signals with varying envelope is critical in baseband circuits since some even-order distortion products end up at baseband. To establish requirements to receiver linearity, the illustration on Figure 2 is useful. Figure 2 shows how to find the input-referred nonlinear response for an Nth order system with a given intercept point. Based on the relations given in Figure 2, the required Nth order intercept point is given as

$$iIP_N = \frac{N}{N-1} \cdot iP_{INT} - \frac{1}{N-1} \cdot iP_{DIS} \quad \text{[dBm]}, \quad (2)$$

where N is the order of the nonlinearity, iP_{INT} the input-referred power of the interferer, and iP_{DIS} the acceptable distortion level referred to the input. To use Eq. (2), the specific test scenario must be considered. During the in-band modulated blocker test, the wanted signal is at -114 dBm, which is 3 dB above the sensitivity limit. This results in a P_{acc} of -98 dBm. Referred to the output of the duplexer, the blocking levels are at -59 dBm, at an offset of $\pm$10 MHz, or at -47 dBm, at an offset of $\pm$15 MHz. The test scenario is shown in Figure 3. A disturbance budget allowing for 50% (-3 dB) receiver noise and Tx-disturbance and for 50% (-3 dB) noise from the second-order product is chosen. Based on Eq. (1) and the disturbance budget, both the maximum allowed noise power and second-order

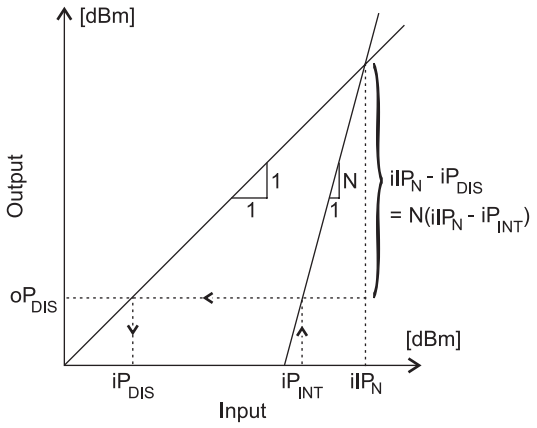

Figure 2: Geometrical interpretation of intercept point.

disturbance is -101 dBm. A significant part of the power of the second-order products is at baseband. However, high-pass filtering can be used to reduce this without significant signal degradation [5]. Further, as the spectra of the second-order distortion products are wider than the wanted signal spectrum, low-pass filtering also gives an improvement. In all, the combined reduction of second-order products is estimated to 6 dB. Using this, the second-order intercept point caused by the blocker at $\pm$10 MHz is found from Eq. (2) as

$$iIP_2 = 2 \cdot (-59) - (-101 + 6) = -23 \text{ dBm} \quad (3)$$

Using the same calculations the intercept point caused by the blocker at $\pm$15 MHz is found to 1 dBm.

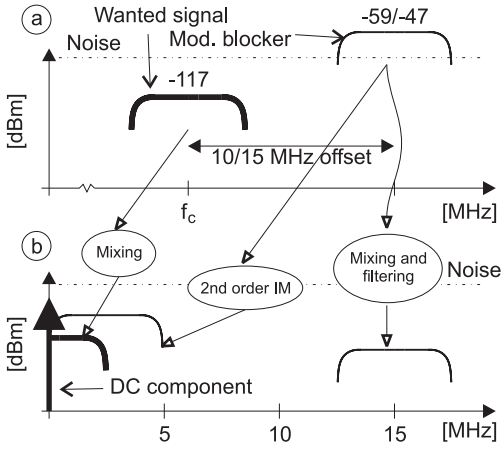

Figure 3: In-band modulated blocker test. (a) RF spectrum with wanted signal an offset modulated blocker. (b) Baseband spectrum with desired and disturbing signals.

During the sensivity test, the Tx-leakage signal acts as a modulated blocker. Second-order distortion is therefore a severe problem. The required second-order intercept point is found to

$$iIP_2 = 2 \cdot (26 - 50) - (-111 + 6) = 57 \text{ dBm}, \quad (4)$$

where 50 dB of Tx-Rx isolation is included. While this appears to be a very hard target value, it is by no means unrealistic. One approach could be to make use of a RF filter after the first LNA stage.

3.3. Third-Order Intercept Points

The in-band third-order intercept point is determined from the intermodulation test. The wanted signal is 3 dB above the sensitivity limit, corresponding to -117 dBm while the interfering signal scenario consists of a CW-signal at an offset of $\pm$10 MHz and a modulated signal at an offset of $\pm$20 MHz. Both interfering signals are at a power level of -49 dBm as Figure 4 shows.

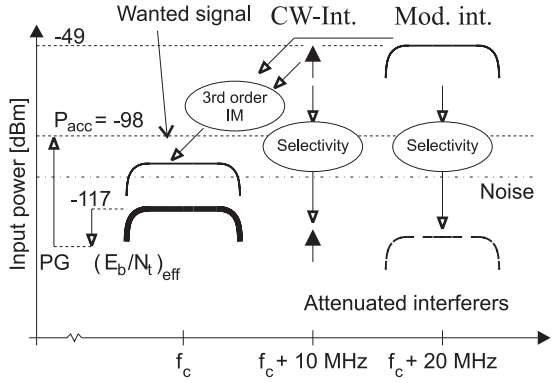

Figure 4: Intermodulation test.

A noise budget is set up as follows: Noise power: 50% (-3 dB), third-order IM-product: 50% (-3 dB). Combined, the disturbances must not exceed -98 dBm. Based on this disturbance budget, it is possible to calculate the required third-order intercept point from Eq. (2)

$$iIP_3 = \frac{3}{2} \cdot (-49) - \frac{1}{2} \cdot (-101) = -23 \text{ dBm} \qquad (5)$$

Because of Tx-leakage, the blocking tests described in [1] also sets demands to iIP_3. The out-of-band blocking test specifies that a CW-blocker is present with a level of -44/-30/-15 dBm at minimum distances from the Rx-band of 15/60/85 MHz, respectively, while the Tx output power is 20 dBm. Blockers at offsets of 85 MHz may generate intermodulation products. In this test the third-order IM-products is allowed generate 50 % of the interfering power. If the frequency of the CW-blocker is *above* that of Tx-leakage signal and the duplex filter offers 27 dB attenuation at offsets of 85 MHz from the Rx-band, the required iIP_3 is found by [1]

$$iIP_3 = \frac{1}{2} \cdot (-28 + 2 \cdot (-42)) - \frac{1}{2} \cdot (-101) = -5.5 \text{ dBm} \quad (6)$$

The requirement to iIP_3 is more harsh if the frequency of the CW-blocker is *below* that of the Tx-leakage signal. It is assumed that Eq. (6) still applies in this case. To obtain an iIP_3 of -5 dBm, 40 dB attenuation of the CW-blocker is required in the duplex filter.

3.4. In-band Selectivity

The selectivity demands are made from the philosophy that disturbing signals should be attenuated to the level of the desired signal in order not to overload the ADCs. A special test is set up for the selectivity for the first adjacent channel located at an offset of $\pm$5 MHz. Here, all signals are well above the noise level and no other disturbance mechanisms are active. The resulting selectivity requirement at $\pm$5 MHz offset is 33 dB [1]. Selectivity here includes any kind of filtering and frequency sensitivity of the demodulator. Several tests use interfering signals at offsets of $\pm$10 MHz. The harshest requirement to selectivity is made by the third-order IM test in which an interferer at -49 dBm is feed to the receiver. The requirement here is 49 dB attenuation. For the remaining Rx-band the blocking test makes a requirement of 51 dB attenuation. 85 MHz below the Rx-band the blocking test makes a requirement of 56 dB attenuation. Finally the sensitivity test makes a requirement of 77 dB attenuation in the Tx-band.

4. Transmitter

Transmitter requirements for the direct up-conversion architecture, illustrated in Figure 5, are derived from the transmitter tests prescribed in the UTRA/FDD standard [3].

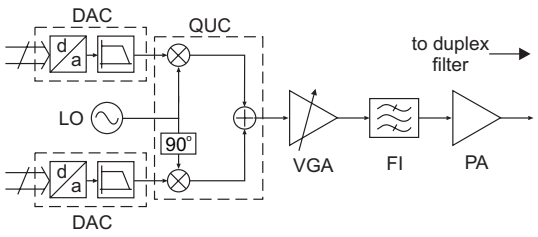

Figure 5: Block diagram of transmitter.

4.1. Input/Output Signals

The input signals are delivered by two DACs, each assumed to deliver an RMS power of -13 dBm. Each DAC is assumed to deliver a signal with the PSD illustrated in Figure 6.

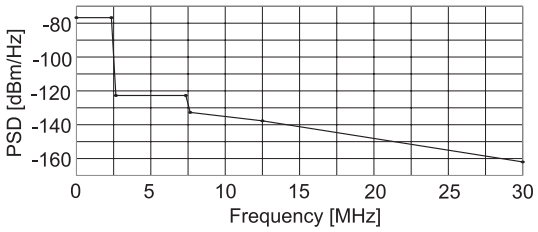

Figure 6: Power spectral density of the DAC.

The assumed PSD is such that no additional filtering of the DAC output is required. In the overall *RMS error vector magnitude* (EVM) budget for the transmitter, the DACs are allowed to contribute with 8 % due to filtering and I/Q imbalance. The output signal specification is based on the noise requirements presented in [3] and on the requirement to noise in the UTRA/FDD Rx-band, taking the duplex filter attenuation into account. The input and output signals for the Tx front-end are specified in Table 2. Three bands have been identified as critical for the spurious emission tests. These bands are band 1 = [1805 MHz – 1880 MHz], band 2 = [1893.5 MHz – 1919.6 MHz], and band 3 = [2110 MHz – 2170 MHz].

4.2. Spurious Requirements

Apart from the input signal spurious power, sources of undesired power are noise generated in the transmitter circuits and phase noise in the LO signal. The output noise is thus a sum of power contributions of each of these factors. In bands 1 to 3, the LO phase noise spectrum is assumed to be flat, meaning that

Parameter	DAC	Output
Power [dBm]	-13	26
EVM [%]	8	17.2
ACLR [dB]		
$f_c \pm$ 5 MHz	-43	-33
$f_c \pm$ 10 MHz	-53	-43
Spurious		
Band 1 [dBm/100 kHz]	-116	-69
Band 2 [dBm/300 kHz]	-79	-39
Band 3 [dBm/3.84 MHz]	-	-74

Table 2: Requirements to DAC and output signals.

the output signal SNR owing to LO phase noise corresponds directly to the phase noise specified at the LO output. The output phase noise power in the bandwidth *B*, $P_{OPH\,B}$, is found for a output signal of P_{OS} by Eq. (7).

$$P_{OPH\,B} = \mathcal{L}_{LO} + 10 \cdot \log(B) + P_{OS} \qquad \text{[dBm/B]} \quad (7)$$

Apart from the desired signal, the transmitter also amplifies DAC noise and phase noise introduced by the LO. It is assumed that the gain of the transmitter blocks is constant at frequencies up to $\pm$ 30 MHz from the Tx-band. Furthermore, PAs are notorious for making image mixing. Image mixing happens when the second harmonic of desired signal mixes noise that is offset $+f$ from the carrier to an offset of $-f$. Conversion gains in the range of 0 dB have been encountered in state-of-the-art PAs. This means that the power at both the positive and the negative offsets will appear in the same band. For the DACs this means that the sidebands indicated in Figure 6 are amplified with two times the in-band transmitter gain. In the most critical scenarios, noise at 12.5 MHz appears in band 2, while noise at 30 MHz appears in band 1. Assuming the noise performance of the DACs is given, the margin to the output noise power specified in Table 2 is used to specify white noise and LO phase noise. Circuit noise power requirements for bands 1 to 3 are listed in Table 3.

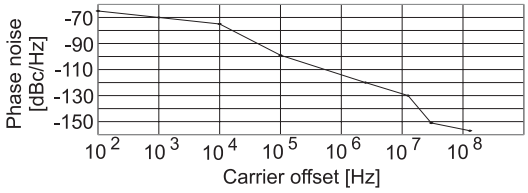

Figure 7: Tx LO phase noise requirement.

Figure 7 describes the phase noise of the LO used in the transmitter. For bands 1 and 2 phase noise power is specified at offsets of $\pm$ 30 MHz and $\pm$ 12.5 MHz. For band 3, the shortest distance from the carrier is 130 MHz. The LO phase noise is thus specified at an offset of $\pm$ 30 MHz.

4.3. Adjacent Channel Leakage Ratio (ACLR)

The ACLR test specified in [3] sets requirements to intermodulation products, phase noise, and noise in the DACs. With T_{OIMD} being the equivalent temperature of the intermodulation noise at the output, the equivalent noise temperature for adjacent channels is found from

$$T_{OT} = T_{OIMD} + T_{OPH} + T_{ODAC} \qquad \text{[k]} \quad (8)$$

From state-of-the-art devices it is found that especially third-order intermodulation is critical. Assuming that ACLR is due to third-order intermodulation only, an oIP_3 of 37.6 dBm is needed to obtain the ACLR required at $\pm$ 5 MHz [6]. Assume instead that DACs and LO are used that features the performance shown in Figure 6 and 7 respectively at frequencies and frequency offsets of $\pm$ 2.5 MHz. Then using Eq. (8) and [6] an oIP_3 of 37.7 dBm is found to provide the required ACLR. DACs and LOs with the indicated performance can thus be used at the cost of only 0.1 dB increase of the required oIP_3. ACLR has been observed to depend on the *output single tone 1 dB compression point* (CP_O) instead of the corresponding oIP_3, when PAs are operated near their CP_O. The transmitter simulated in [6] features a CP_O that is 10.6 dB below the corresponding oIP_3 [7]. The required CP_O is therefore 27.1 dBm.

4.4. Error Vector Magnitude

EVM of the output signal of the transmitter is a result of many factors that cause signal degradation. The total EVM (EVM_T) caused by N uncorrelated factors is found by

$$\text{EVM}_T = \sqrt{\sum_{n=1}^{N} \text{EVM}_n^2} \qquad [\,\%] \quad (9)$$

Which factors that contribute to EVM depend on the transmitter architecture. For a direct up-conversion transmitter, significant contributing factors are: DACs, in-band ripple, I and Q imbalance, phase noise, third-order intermodulation and LO leakage. The contributions from the DAC and the third-order intermodulation are already given. When amplifiers that meets the ALCR requirement are used, EVM in the range of 3 % have been observed. In the following the remaining contributors are specified so that a total of 17.2 % EVM is obtained at the output signal. In-band ripple is specified for the desired channel only. It includes in-band magnitude ripple compared to the RMS magnitude, and RMS phase ripple compared to the linearized in-band phase that causes minimum RMS error. Amplitude ripple of 0.4 dB results in an EVM of 4.7 % [8], while phase ripple of 4 deg. results in an EVM 7 % [8]. EVM is measured in time slots with a duration of 667 μs [3]. LO phase noise at offsets of less than one tenth of the frequency of the time slots is not detected by the receiver as phase error. The lower limit for the specification of LO phase noise is therefore 150 Hz. Figure 7 defines the phase noise of the LO used for the transmitter. The average in-band phase noise of this LO is 4 deg. The EVM caused be an RMS phase noise of 4 deg. is approximately 7 % [2]. An I/Q amplitude imbalance of 1.4 dB generates an EVM of 8.0 % [2], while a phase offset between the I and the Q signal of 5 deg. generates and EVM of 4.4 % [2]. A general expression that depends on LO leakage is *LO to signal ratio* (LSR). LSR is defined as the ratio between the average power of the LO signal, measured at the output of the *quadrature up converter* (QUC), and the average power of the desired signal, measured at the same place. LSR can be transferred directly to the output of the transmitter, which makes it suitable for specification of LSR induced EVM, EVM_{LO}, found by

$$\text{EVM}_{LO} = \sqrt{\text{LSR}} \cdot 100 \qquad [\,\%] \quad (10)$$

Eq. (10) defines LSR as a ratio. For specification purposes the required LSR is presented in dB. An LSR of -27 dB is found to generate an EVM of 4.5 %. When a gain budget exists for the transmitter, a specification of LO-leakage can be made. The

UTRA/FDD standard does not allow adjustments of DC offsets during EVM measurements. If this is allowed, LSR will have no effect on EVM.

5. Block Requirements for a Direct Up/Down Conversion Transceiver

The Rx and Tx requirements are summarized in Table 3.

Rx parameter	**Requirement**
Noise figure [dB]	≤ 6
In-Band selectivity [dB]	
1st adj. (5 MHz)	≥ 33
2nd adj. (10 MHz)	≥ 49
Remaining Rx-band	≥ 51
2025 – 1980 MHz	≥ 56
Tx-band	≥ 77
Intercept points [dBm]	
iIP_2 (10 MHz)	$\geq$ -23
iIP_2 (15 MHz)	≥ 1
iIP_2 (Tx)	≥ 57
iIP_3 (10/20 MHz)	$\geq$ -23
iIP_3 (Tx)	$\geq$ -5.5
iIP_3 (1730 – 1830 MHz)	$\geq$ -5
Tx parameter	**Requirement**
Circuit noise [dBm/Hz]	
Band 1	$\leq$ -124
Band 2	$\leq$ -107
Band 3	$\leq$ -140
1 dB compression points [dBm]	
CP_O	≥ 27.1
IQ imbalance	
Amplitude [dB]	≤ 1.4
Phase [deg]	≤ 5
In-band ripple	
Amplitude [dB]	≤ 0.4
Phase [deg]	≤ 4
LSR [dB]	-27

Table 3: Summary of transceiver requirements.

5.1. Receiver Block Requirements

In the recent years, direct-conversion receivers have emerged for GSM applications and many consider this architecture the proper choice for 3G systems. A particular nice feature is the fact that the large bandwidth makes W-CDMA systems less sensitive towards $1/f$ noise and DC offset problems inherent to homodyne receivers. An example of an UTRA/FDD direct-conversion receiver is shown in Figure 8.

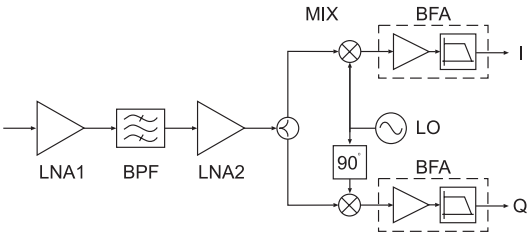

Figure 8: Direct-conversion receiver.

An interstage *bandpass filter* (BPF) is used to provide attenuation of the Tx-leakage signal. To meet the requirements, the BPF must attenuate the Tx-band and the band stretching from 1730 MHz to 1830 MHz at least 30 dB. Considering linearity, iIP_2 and iIP_3 is assumed to be of constant value for carrier offsets up to $\pm$380 MHz. iIP_2 is only critical for the *mixer* (MIX) and *subsequent base band blocks* (BFA). In spite of the extra filtering, the harshest demand to iIP_2 is made by the Tx-leakage signal. It is therefore not sufficient to specify iIP_2 for MIX and BFA from the requirements to iIP_2 in the Rx-band. MIX and BFA are specified so they generate an equal amount of noise power due to iIP_2. Tx-leakage also sets the harshest demand to iIP_3. However, in this case BPF lowers demands to the subsequent blocks, making only *Low noise amplifier number 1* (LNA1) critical to the Tx-leakage signal. The block requirements are listed in Table 4.

Block	**LNA1**	**BPF**	**LNA2**	**MIX**	**BFA**
Gain [dB]	15	-3	9	10	–
NF [dB]	4	3	4	16	31
iIP_2 [dBm]	–	–	–	27	37
iIP_3 [dBm]	-4	–	-6	0	10

Table 4: Receiver block requirements.

Some tolerances must be specified for all block gains to accommodate different variations. These tolerances require an additional margin to be put on the performance parameters listed in Table 4. Based on these block requirements, it is clear that meeting the test specifications listed in the UTRA/FDD standard is by no means unrealistic. Being able to operate LNA1 at a noise figure of 4 dB makes the design of this block less critical. In terms of linearity, the continuous presence of the Tx-signal sets the most stringent requirements to the receiver. This problem becomes less severe when an interstage bandpass filter is used.

5.2. Transmitter Block Requirements

The effect of LO phase noise on spurious and EVM depends on how gain and noise figure budgets are set up for the transmitter presented in Figure 5. The gain budget represents a compromise between noise figure and CP_O. Noise contributions in bands 1 to 3 are calculated using cascaded noise figures. When calculating the resulting output noise, image mixing in the PA, described in Subsection 4.2, has to be taken into account. A one to one conversion of the noise at the image band has been observed on a state-of-the-art PA running at the desired power level. It is therefore assumed that image mixing in the PA can be taken into account by doubling the effective noise-band-width. Table 5 lists the in-band gain, noise figure and CP_O performance required from each individual block.

Block	**QUC**	**VGA**	**FI**	**PA**
Gain [dB]	0	13	-2	25
NF [dB]	10	4	2	5
CP_O [dBm]	3.9	15.4	30	27.7

Table 5: Transmitter block requirements.

Figure 9 presents budgets for signal power, cascaded CP_O and noise in the critical bands. The large signal gain of the PA at band 1 and band 2 are expected to be the same as the in-band

gain i.e. 25 dB. At band 3, a gain of 23 dB and a NF of 7 dB is assumed.

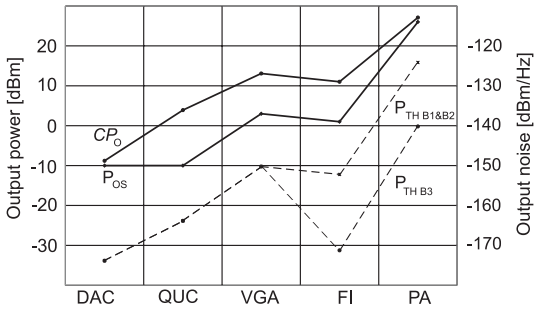

Figure 9: Budgets for signal power [dBm], cascaded noise power at band 1 and 2 $P_{\text{TH B1\&B2}}$ and band 3 $P_{\text{TH B3}}$ [dBm/Hz], and CP_O [dBm].

As was the case for the receiver, the Tx blocks has to be designed with some margin on NF and CP_O to take into account gain variations. It is found that 21 dB attenuation is needed in band 3. When the transmitter is operated at its highest channel, the UTRA/FDD Rx-band is offset 130 MHz from the carrier. However, the image is only offset 70 MHz from the lower edge of the Tx-band. Therefore the *filter* FI must provide 21 dB of attenuation $\pm$ 70 MHz from the Tx-band. The need for FI arose from the philosophy that the duplex filter should only attenuate as much power as was generated in the PA. If the duplex filter was to attenuate all the noise power generated by the transmitter in the Rx-band, the duplex filter would be required to attenuate the Rx-band by 49 dB. Assuming that the LO drives each mixer in the QUC with -6 dBm, a requirement for LO-leakage in QUC can now be made from the gain budget illustrated in Figure 9. Here the output signal power of QUC is -7 dBm and in Table 3 LSR is specified to -27 dB. The requirement to LO-leakage is thus -28 dB. A decrease in signal output power of the QUC or an increase in LO drive power, results in more harsh requirements to LO-leakage. Generally, the requirements relating to EVM does not seem critical for state-of-the-art devices. However, the requirement to output noise in band 1 sets harsh demands to the QUC. FI can not do any significant attenuation here, since the image may be in the Tx-band. The only way to allow for a significant increase in the QUC noise figure, is by attenuating band 1 in the duplex filter. If for example 8 dB attenuation was available here, the noise figure of the QUC could be as high as 20 dB. Obtaining such noise figures should not be a problem.

6. Conclusion

In this paper, UE transceiver requirements have been derived from the UTRA/FDD standard. Requirements found in recent specifications have been mapped into block requirements suitable for design. Based on the derived Rx requirements only, plausible block requirements result from using the direct-conversion architecture. It is important to notice that having the Tx-signal running at all times results in the harshest requirement to the Rx linearity. Tx specifications have been translated to overall requirements for a direct up-conversion transmitter. These have been translated to block requirements. It was found that because Rx and Tx is running at the same time, a bandpass filter is required in front of the PA if the specified duplex filter is used. It should be noted that requirements presented in this document are based directly on specifications. In practice, some margin need be included to take into account fabrication tolerances and other uncertainties. Also, it is worth noting that UTRA/FDD to a wide extent is an interference limited system where any additional performance surplus on the UE receiver side will lead to increased system capacity. Hence, network providers will prefer "good" UEs to increase their profit and thus UE manufacturers may wish to exceed specifications significantly in order to gain market shares.

7. References

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Simulating Overall Performance Requirements for Transmitters in IMT 2000 FDD User Equipment

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European Conference on Wireless Technologies
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Simulating Overall Performance Requirements for Transmitters in IMT2000 FDD User Equipment.

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KEYWORDS
EVM, ACLR, I/Q imbalance, Phase noise, third order inter-modulation, power amplifiers

ABSTRACT
This work analyses the effects that various overall non-ideal circuit parameters have on EVM and ACLR. The analysis includes (i) analytical expressions of EVM, (ii) simulations, and (iii) performance measured on an actual UTRA FDD transmitter. Results obtained through either analytical expressions or simulations are compared with measured data.

INTRODUCTION

Transmitters for IMT2000 FDD are specified by terms like RMS *Error Vector Magnitude* (EVM) and *Adjacent Channel Leakage Ratio* (ACLR). Both factors are relatively easy to measure, but they are not very suitable as design parameters for a *transmitter* (Tx) front-end. In order to set up a set of design parameters for a IM2000 FDD Tx front-end the effects that each design parameter has on EVM or ACLR must be known. This work investigates the effects of: (i) I/Q amplitude imbalance, (ii) performance of *Digital to Analog Converters* (DACs), (iii) I/Q phase imbalance, (iv) phase noise and (v) non-linear behaviour.

ANALYTICAL INVESTIGATIONS

Modulated by a carrier at frequency f_C, the ideal output signal *S(t),* is expressed by

$$S(t) = I(t) \cdot \cos(2\pi f_C t) + Q(t) \cdot \sin(2\pi f_C t) \tag{1}$$

Distortion may appear either at *I(t)* and *Q(t)* or at the carriers. Before EVM is measured, *S(t)* is converted to base-band. Assuming that down conversion is followed by a sharp low-pass filter, I(t) is recreated if *S(t)* is multiplied by a cosine at f_C, while *Q(t)* is recreated if *S(t)* is multiplied by a sine, also at f_C . If *S(t)* is distorted, the down converted signals may contain parts of that distortion. The down converted signal can be represented as a complex *BasebBand* BB signal.

$$S_{BB}(t) = \frac{1}{2}\left(I_D(t) + j \cdot Q_D(t)\right) \tag{2}$$

Defining time averaging as $\langle \bullet \rangle$ EVM is found by

$$EVM = \sqrt{\frac{\left\langle \left(I(t) - I_D(t)\right)^2 + \left(Q(t) - Q_D(t)\right)^2 \right\rangle}{\left\langle I^2(t) + Q^2(t) \right\rangle}} \cdot 100\% \tag{3}$$

Analytical expressions for EVM generated by I-Q amplitude and phase imbalance and phase-noise are listed in Table 1. The expression for DAC performance is derived for a signal that features a peak to average power level of 3 dB. In Table 1, $f(t)$ represents phase noise as function of time. If $f(t)$ exhibits small values and fluctuations, the cosine function is approximately linear. If the difference between average and RMS values further more is small, then $\langle \cos(f(t)) \rangle$ can be approximated by $\cos(f)$, where f is the RMS value $f(t)$. The effect of these factors have been measured according to 3GPP(1) and calculated. The results are shown in Figure 2, Figure 3, Figure 4 and Figure 5. In these figures, dashed lines indicate calculated data, while dots indicate measured data.

SIMULATION

This section concerns time domain simulations of non-linear effects in the transmitter. When concerning non-linear behaviour, the most critical component in the transmitter is the *Power Amplifier* (PA), because this component handles signals of the highest power in the transmitter. To increase talk time, the PA must be as power efficient as possible. Non-linear behaviour is especially critical for ACLR 3GPP(2), but it may also cause degradation of EVM. In the simulations presented here, ACLR is measured from powers that are averaged over one time slot. ACLR is therefore expressed from the average in-band power and the average power emitted on the adjacent channels. Through measurements on state-of-the-art power amplifiers it has been found that especially ACLR on the two channels closest to the desired channel is critical. The major contributor to noise power in this band is 3rd order inter-modulation distortion. The distorted signal $S_D(t)$ can be described by Eq: (4), which generates an in-band portion and 3rd order inter-modulation distortion at the channels closest to the desired channel.

$$S_D(t) = a_1 \cdot S(t) + a_3 \cdot S(t)^3 + a_5 \cdot S(t)^5 + \ldots \tag{4}$$

In Eq (4) the average power of the harmonic distortion components increases with the third power of the *average Power of the INput signal* (P_{IN}). α_3 is proportional to the *3rd order Intercept Point* (IP_3) and determines the 1 dB Compression Point of Eq. (4). Therefore the relation between IP_3 and the average power that appears at the channels closest to the desired channel is inherited Eq. (4). Measurements have revealed that this relation does not hold for state-of-the-art power amplifiers. Figure 1 shows a sketch of how the *average IN-Band output Power* (P_{INB}) and *the average Power at the nearest Adjacent Channel* (P_{AC}) have been observed to depend on P_{IN}. In this sketch the vertical distance between P_{INB} and P_{AC} expresses ACLR It is noticed that P_{AC} is not always increased by the third power of P_{IN} as inherited in Eq. (4). Instead P_{AC} has been observed to depend on P_{IN} by powers less than 3 for both low and high levels of P_{IN}. For low P_{IN} this phenomena might appear because bias conditions in the PA may be regulated in order to optimise power efficiency or because of feedback regulation. For higher levels of P_{IN} similar effects may take place, together with supply voltage power compression. Because of this behaviour, it is difficult to state any relation between one or more parameters and ACLR performance. In order to simulate such PAs Eq (4) has to be expanded. The expansion consists in the use of coefficients that depend on P_{IN} as shown in Eq (5).

$$S_D(t) = a_1(P_{IN}) \cdot S(t) + a_3(P_{IN}) \cdot S(t)^3 + \ldots \quad (5)$$

Through the theory behind Eq. (4) and knowledge about how P_{AC} relates to the average power generated in-band when *S(t)* is raised to the third power, a new set of α_1 and α_3 is generated for each average input power, so that Eq. (5) generates a set of specified P_{INB} and P_{AC}. This approach has been tested on a set of data for P_{IN}, P_{INB} and P_{AC} that are measured on a state-of-the-art PA. The results are shown in Figure 6. The measured data are shown as dots while the results of the simulation are shown as dashed lines. It appears that the specified levels are obtained for P_{INB} and P_{AC} when α_1 and α_3 are generated from average input power. This indicates that ACLR can be predicted from the average input power level, if the average 3rd order power of the signal is known. This indicates that a graph based on average powers like the one illustrated in Figure 1, resemble the actual performance of the PA with respect to ACLR. Further more, if the relation between P_{AC} and the third harmonic inter-modulation products are known, ACLR can be predicted through single or two tone tests. Because Eq. (5) is a time domain function that operates on the input signal, it is suitable for simulation of EVM performance as well as ACLR performance. During the simulations of adjacent power, EVM was also simulated. The results are shown in Figure 7 together with data measured on the same PA. Again the measured results are indicated by dots, while dashed lines indicate simulated results. Eq (5) is thus capable of predicting the EVM performance from P_{IN}, P_{INB} and P_{AC}.

MEASUREMENTS AND RESULTS

Measurements were conducted using a BB simulator that is capable of delivering analog I /Q signals to an UTRA FDD transmitter. EVM and ACLR are measured on a Tx-tester. The measured results are shown in Figure 2 to Figure 7. First EVM owing I/Q amplitude imbalance is measured. To reduce the complexity of the test set-up, the BB signals are fed directly to the Tx tester. In spite of low complexity, factors like imperfections in the Tx-tester, phase noise, phase offsets and quantization noise in the BB simulator distorts the signal. This sets a lower limit to the EVM that can be measured. The measured relations are shown in Figure 2. The total EVM, EVM_{TOT} obtained from *N* un-corelated sources of distortion is found by

$$EVM_{TOT} = \sqrt{\sum_{n=1}^{N} EVM_n^2} \quad (6)$$

Because EVM is added as root sum square, the weight of EVM caused by the imperfections becomes smaller as the I/Q amplitude offset becomes larger. It appears from Figure 2 that when the I/Q amplitude imbalance is 0 dB an EVM of approx. 1% is measured. This amount of EVM is attributed to the factors mentioned above. Assuming that phase noise and I/Q phase offset contributes equally to the major amount of EVM, each parameter contributes with 0.7% according to (6). To obtain these figures the I/Q phase imbalance should be about 0.8 deg. and the RMS phase noise 0.4 deg. Such errors are not unlikely for the BB simulator. It is noticed that as the I/Q amplitude offset is increased, the measured EVM converge towards the theoretical EVM found by Eq (7). The effect of quatization is also measured using this measurement set-up. The measured results are shown in Figure 3. It is noticed that (8) is not capable of making a perfect fit for combinations of low resolution and low over-sampling ratios. This indicates that these factors co-relate with one another in manners not described by Eq. (8). Eq. (8) is therefore only considered as an approximation. For state-of-the-art DACs the over-sampling ratio is in the rage of 8 and the effective resolution is also 8. In this range of over-sampling and resolution Eq. (8) is a good approximation. Next the effect of I/Q phase offset is tested. This measurement requires a more complex set-up, which includes two passive mixers, an adjustable phase shift and power-combiners. This extra complexity adds to the number of sources of distortion. New sources are I/Q amplitude imbalance and phase noise of the LO that is used for up-conversion in the mixers. Figure 4 shows measured results along with theoretical results obtained by Eq. (9). Again it is seen that as the effect under investigation becomes the significant contributor, The measured EVM converges toward the theoretical values. For

0 deg. offset an EVM of 1.7% is measured. The phase error of the signal generator used in this test was measured to 0.5 deg. Together with 1% EVM generated by the BB simulator, this accounts for 1.3% EVM. The remaining amount of EVM is attributed to distortion in the mixers and imperfect adjustment of the phase offset. The same set-up is used for measuring the effects of phase noise. However instead of adjusting the I/Q phase offset, phase noise is added to the LO. Measured results are shown in Figure 5 together with theoretical results obtained by Eq. (10). Again the measured results converge towards the theoretical values, as EVM, due to phase noise, becomes significant. Near zero degree phase noise, the measured EVM is in the range of what was measured for zero degree I/Q phase-offset. This indicates that the same errors are present here. Finally ACLR and EVM has been measured on a state-of-the-art PA. The measured data are shown in, Figure 6 and Figure 7. It is noticed that high values of EVM are measured where the simulated results indicate low values. The amount of EVM measured indicates that the same errors are present during this measurement, as was the case during measurement of RMS phase error and I/Q phase offset. It was found that an ACLR of 33 dB is obtained when the PA delivers 27.3 dBm in-band power. When 33 dB of ACLR is obtained, the PA's contribution to EVM is 3%. No relations were found between PA design parameters and ACLR during the simulations. However from measurements on various amplifiers, it appears that the ACLR requirement is met at output powers that are approx. 1 dB below the amplifiers 1 dB compression point.

CONCLUSION

The work presented here indicates cohesion between various design parameters and test parameters specified for transmitters for the IMT2000 FDD system. The influence that I/Q imbalance has on EVM has been derived and verified through measurements. Also the influence of phase noise on a local oscillator has been investigated and verified. It was found that co-relation exists between noise generated due to quantization and over-sampling, and that this correlation becomes significant when both the resolution and over-sampling ratio of a DAC are low.
An approach was devised that generates a predefined in-band signal power and power at the adjacent channels, by using coefficients of a 3rd order expression that depends on the average input power. The fact that this approach is valid indicates that ACLR can be found from averaged powers only, given that the average spectral density function of the third power of the input signal is known. The knowledge obtained in this paper is important when making budgets for EVM for UTRA FDD transmitters. Assume that a transmitter is build that uses 8 bit DACs running with an over-sampling-ratio of 8. Assume further that the modulator in the transmitter has an I /Q amplitude imbalance of 0.5dB and phase imbalance of 0.5 deg. and that a LO with a RMS phase error of 3.5 deg. is used. Finally assume that the PA described in this paper is used to deliver an average output power of 26 dBm. It can now be concluded that the combined EVM from these parts is 6.3% and that ACLR due to distortion in the PA is 35 dB.

ACKNOWLEDGEMENT

I would like to thank colleagues at Telital R&D Denmark A/S for helping out with measurements.

Table 1 Analytical expressions for EVM

I/Q amplitude imbalance A	$EVM_{IQA} = \sqrt{\left\|2 - \sqrt{\frac{2}{A^2+1}} \cdot (A+1)\right\|} \cdot 100\%$	(7)
Resolution n [Bit] and oversampling OS	$EVM_{DAC} = \left(\sqrt{\frac{1}{3/2 \cdot \left(2^{2 \cdot (n+1)}\right)}} + \frac{1}{(2 \cdot OS)^2} \right) \cdot 100\%$	(8)
I/Q phase imbalance j [deg]	$EVM_{IQP} = \sqrt{2 - 2 \cdot \cos\left(\frac{j}{2}\right)} \cdot 100\%$	(9)
Phase noise $f(t)$ [deg]	$EVM_{PHA} = \sqrt{2 - 2 \cdot \langle \cos(f(t)) \rangle} \cdot 100\%$	(10)

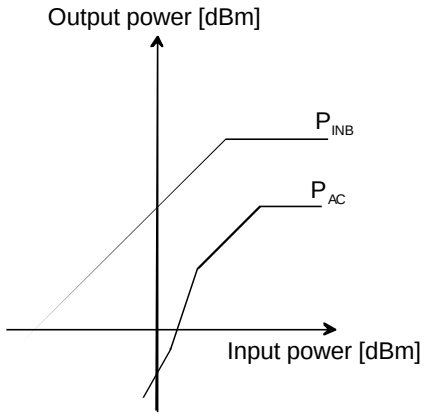

Figure 1 Indication of observed relation between P_{INB}, P_{AC} and average in-band power.

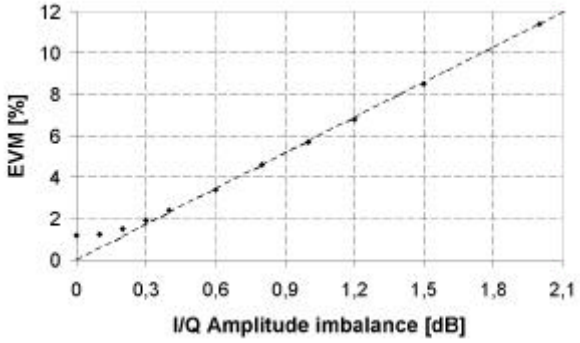

Figure 2 EVM related to I/Q amplitude imbalance.

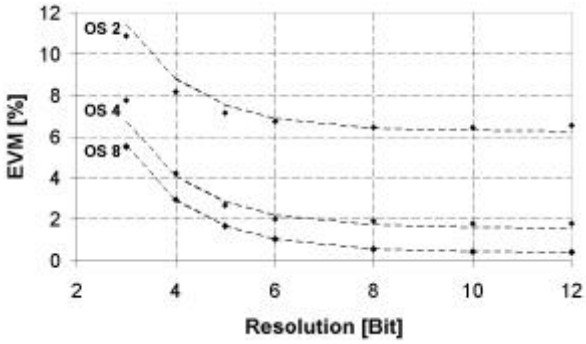

Figure 3 EVM related to quatization noise.

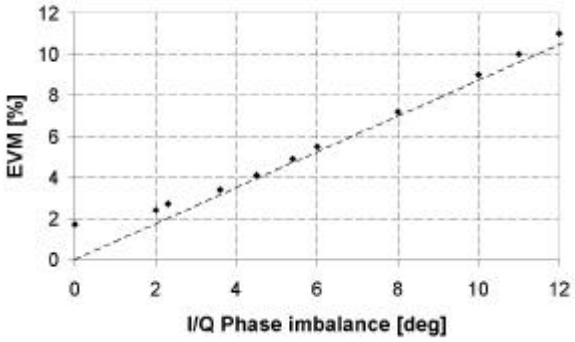

Figure 4 EVM related to I/Q phase imbalance.

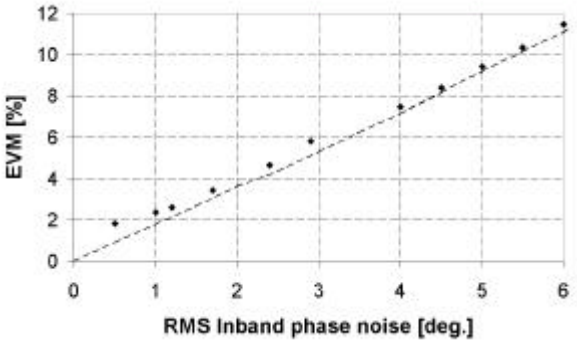

Figure 5 EVM related to phase noise.

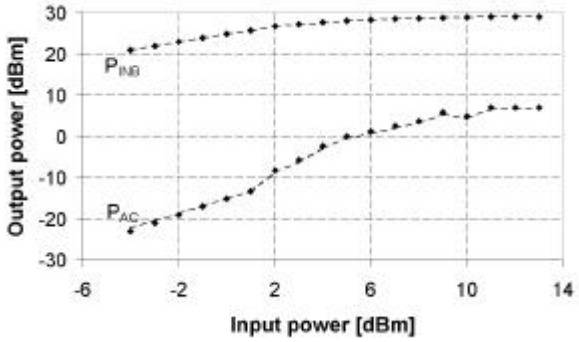

Figure 6 P_{INB} and P_{AC} related average input power

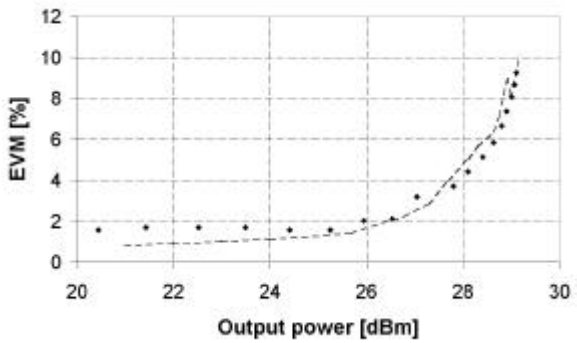

Figure 7 EVM related to output power.

(1) 3rd Generation Partnership project (3GPP), "radio transmission and reception (FDD), terminal conformance specification 34.121 v.3.4.0", March 2001.

(2) 3rd Generation Partnership project (3GPP), "UE radio transmission and reception (FDD), technical specification 25.101 v.4.0.0", March 2001.

UTRA/FDD RF Transceiver Requirements

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UTRA/FDD RF Transceiver Requirements

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Abstract. Unified RF requirements are derived for an UMTS Terrestrial Radio Access/Frequency Division Duplex (UTRA/FDD) compliant mobile transceiver. A set of transceiver requirements are proposed with consideration to system issues including duplex aspects. From these design-compatible requirements are proposed for each functional block in the transceiver.

Keywords: RF Transceiver, UTRA/FDD, transceiver requirements, direct up/down conversion, receiver, transmitter

1. Introduction

The UTRA/FDD mobile standard provides an improved platform for personal communications including voice, data, and multimedia services compared to current 2G systems. For UTRA/FDD to retain a competitive advantage, high-performance, low-cost *user equipment* (UE) must be made available to the general public. This paper proposes a set of specifications for functional blocks used in direct up/down conversion transceivers, corresponding to the UTRA/FDD interface specifications [1]. This paper is an update of previous work for the receiver branch [2] and ongoing work for the transmitter branch [3].

2. Duplex Aspects

As UTRA/FDD is based on *frequency division duplex* (FDD), the required isolation between *transmitter* (Tx) and *receiver* (Rx) is only practically obtainable using a duplex filter. The transmitter-induced

noise level at the receiver input (Rx-band) is determined by the transmitter noise level and the duplexer isolation. A level of -111 dBm measured in a single UMTS channel bandwidth (3.84 MHz) is shown in later sections to give an acceptable degradation of receiver sensitivity. To reduce the insertion loss at Tx, the duplex filter should only attenuate noise generated by the *power amplifier* (PA) itself, while noise generated before the PA should be filtered inside the Tx-chain. Measurements on a state-of-the-art PA indicate that -74 dBm of noise can be expected on a Rx channel. Also, it needs to be considered that a Tx-leakage signal may cause disturbance in the Rx-band because of receiver non-linearities. The proposed duplexer performance requirements are summarized in Table I.

Table I. Duplex filter requirements. [4].

Parameter	*Requirement [dB]*
Tx-Ant attenuation (Tx-band)	< 2
Rx-Ant attenuation (Rx-band)	< 3
Tx-Rx isolation (Rx-band)	> 37
Tx-Rx isolation (Tx-band)	> 50

3. Receiver

To ensure that the receiver has adequate performance it must meet requirements for a number of tests defined in the UTRA/FDD standard [1]. For each of these tests, a BER of 10^{-3} must be achieved at a user bit rate of 12.2 kbps and a chip rate of 3.84 Mc/s. To meet this, an $(E_b/N_t)_{\text{eff}}$ of 6 dB is needed, including a 0.8 dB implementation margin [7]. The down-link signal is protected by a unique scrambling code, which gives it noise-like qualities. The same is true for the modulated test signals and the up-link signal. Any disturbing signals, including distortion products, are therefore treated as white noise. It should be noted that all Rx calculations relate to the Rx chain following the duplex filter, unless otherwise specified.

3.1. Noise Figure (NF)

The sensitivity requirement is specified for a dedicated physical channel (DPCH) signal power, S_i. Based on the given required $(E_b/N_t)_{\text{eff}}$, the

acceptable noise and distortion power in a channel bandwidth, P_{acc}, is calculated as

$$\begin{aligned} P_{acc} &= S_i - (E_b/N_t)_{\text{eff}} + 10 \cdot \log(PG) \\ &= -120 - 6 + 25 = -101 \text{ [dBm]}, \end{aligned} \quad (1)$$

where PG is the processing gain (the ratio of chip rate to bit rate) and P_{acc} consists of Rx-noise($P_{Rx,N}$), Tx-noise in the Rx band ($P_{Tx,N}$) and distortion products due to Tx-leakage combined with Rx non-linearities ($P_{Tx,D}$). If the Tx-signal is turned off, $P_{acc} = P_{Rx,N}$ resulting in an Rx noise figure of 7 dB. To make room for any Tx-signal noise and distortion effects, the Rx noise figure must be reduced accordingly. If a 1 dB reduction in $P_{Rx,N}$ is accepted and the remaining noise and disturbance power is distributed equally between $P_{Tx,N}$ and $P_{Tx,D}$, the acceptable level of each is -111 dBm/3.84 MHz or less. This disturbance budget is illustrated in Figure 1. The maximum noise figure is then reduced to 6 dB. The Tx-leakage power level in Figure 1 is the power level of the Tx-signal at the Rx-output of the duplexer, i.e. the 26 dBm Tx output power attenuated by 50 dB.

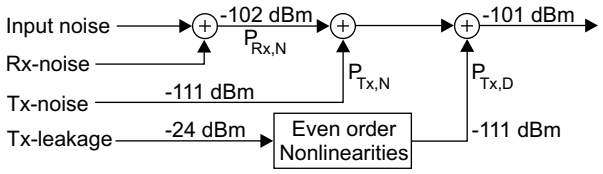

Figure 1. Illustration of the noise and disturbance power distribution.

3.2. Intermodulation

In [4], the power budgets for the different test scenarios from the UTRA/FDD specification are described. The different test scenarios are listed in Table II along with the resulting n'th order, two tone intercept point, iIP_n. Note that in many of the test cases, several disturbance mechanisms are active at the same time, reducing the acceptable disturbance power level for intermodulation. In Table II, f_c represents the carrier frequency. Although the Tx leakage signal results in a very high overall iIP_2, the frequency offset of the Tx means that requirements to the blocks where iIP_2 is critical may be relaxed using RF interstage filtering. The Tx leakage signal, together with the out-of band blocker also sets a harsh requirement to iIP_3 (-5 dBm). The requirement to iIP_3 is based on the assumption that blocking signals are attenuated by at least 40 dB in the duplex filter [4]. In a transceiver that supports variable transmit to receive frequency separation, this iIP_3 must be maintained from 1670 MHz to 2025 MHz.

Table II. Required iIP_n based on different test scenarios.

Test	iIP_2 [dBm]	iIP_3 [dBm]
In-band modulated blocker test		
$f_c \pm$ 10 MHz	$\geq$-23	–
$f_c \pm$ 15 MHz	$\geq$+1	–
Tx leakage	$\geq$+57	–
Intermodulation test	–	$\geq$-23
Out-of-band blocker		
1670 - 2025 MHz	–	$\geq$-5

3.3. In-band Selectivity

The selectivity requirements are defined so all unwanted signals and the desired signal appear with equal power at the ADC. The resulting requirements are derived in [4], based on the tests defined for inter-modulation, in-band and out-of-band blocking, and Tx-leakage. These requirements are summarized in Table IV, page 7.

4. Transmitter

Transmitter requirements for the direct up-conversion architecture are derived from the transmitter tests described in [1]. The requirements apply to the Tx chain, not including the duplex filter.

4.1. Input/Output Signals

The modulated signal is delivered to the transmitter as I and Q signals, that meet the signal quality requirements in Table III. The output signal specification is based on [1] and on the requirement to noise in the UTRA/FDD Rx-band. These specifications, including the effect of duplex filter attenuation, are also listed in Table III. The average power of the LO is assumed to be -6 dBm, and the limits for LO phase noise are proposed in Figure 2.

4.2. Spurious Requirements

Noise emissions are critical for the spurious emission test in [1] and noise in the UTRA/FDD Rx band. Three critical sources of noise power are found for the transmitter. These are the transmitter circuits, the LO and the I and Q signal. It is assumed that the LO phase noise spectrum

Table III. Requirements to I/Q and output signals.

Parameter	*I/Q signals*	*Output*
Power [dBm]	-13	26
EVM [%]	≤ 8	≤ 17.2
ACLR [dB]		
f_c ±5 MHz	≥ 43	≥ 33
f_c ±10 MHz	≥ 53	≥ 43
Spurious		
Band 1 (1805 MHz – 1880 MHz) [dBm/100 kHz]	$\leq$ -116	$\leq$ -69
Band 2 (1893.5 MHz – 1919.6 MHz) [dBm/300 kHz]	$\leq$ -79	$\leq$ -39
Band 3 (2110 MHz – 2170 MHz) [dBm/3.84 MHz]	–	$\leq$ -74

Figure 2. Limits for Tx LO phase noise.

is flat in bands 1 to 3, meaning that the SNR at the LO carrier is maintained at the output signal. It is further assumed that noise power at offsets up to ±30 MHz from the Tx-band is amplified with the inband gain. Third order intermodulation between the Tx signal and input noise has been observed on PAs. This has the effect that input power at $f_c - f$ is converted to $f_c + f$. Measurements on a state-of-the-art PA have indicated a conversion gain of the same magnitude as the gain at $f_c + f$. This means that the LO and input signals contribute at both $f_c - f$ and $f_c + f$. The resulting noise requirements for the transmitter circuits are listed in Table IV.

4.3. Adjacent Channel Leakage Ratio (ACLR)

ACLR may be generated from intermodulation in the transmitter, phase noise, and noise in the I and Q signals. Phase noise and noise in the I and Q signals is chosen so that ACLR generated by the transmitter must be 1 dB above the overall Tx requirements. The ACLR requirements to the transmitter are listed in Table IV. It is likely that the PA is allowed to generate most of the ACLR in the transmitter in order to improve power efficiency. If the PA is allowed to generate, say, 33.5 dB of ACLR at f_c ±5 MHz, the requirements to ACLR, generated

by the I and Q signals and phase noise, must be increased by 3 dB. Investigations of intermodulation in PAs have shown that the most suitable way to describe ACLR performance of such devices on a general level, is simply to specify ACLR [3]. Therefore, in this work, only the ACLR is specified.

4.4. Error Vector Magnitude (EVM)

EVM is generated by many different circuit imperfections, depending on which transmitter architecture is used. For a direct up-conversion transmitter, the significant factors are: Input signal, inband phase response and amplitude ripple, I- and Q-imbalance, phase noise, intermodulation and LO leakage. The relation between EVM and offset from the average gain, as well as the relation between EVM and the difference between the actual phase response and the ideal phase response are described in [5]. The effects of I- and Q-imbalance, inband phase noise and intermodulation are described in [3], which also explains how to combine uncorrelated contributors of EVM. In [4], LO leakage is described by the *LO to Signal Ratio* (LSR). No adjustments of DC-offsets is allowed during EVM measurements. If this is allowed, LSR will have no effect on EVM. The total amount of average EVM generated by transmitter must not exceed 17.2% rms. This leads to the requirements proposed in Table IV.

5. Block Requirements for a Direct Up/Down Conversion Transceiver

The Rx and Tx requirements are summarized in Table IV.

5.1. Receiver Block Requirements

In the recent years, direct-conversion receivers have emerged for GSM applications and many consider this architecture the proper choice for 3G systems. A particularly nice feature is the fact that the large bandwidth makes W-CDMA systems less sensitive towards $1/f$ noise and DC offset problems inherent to direct-conversion receivers. An example of a UTRA/FDD direct-conversion receiver is shown in Figure 3. An interstage *bandpass filter* (BPF) is used to provide attenuation of the Tx-leakage signal. The amount of attenuation required from this filter depends the difference in requirements to in-band and out-of-band linearity. The goal is to attenuate the Tx-signal such that requirements to iIP_2 and iIP_3 for the subsequent RF blocks are the same for both the Rx band and out-of-band. Assuming that the BPF has an insertion loss

Table IV. Summary of transceiver requirements.

Rx parameters		*Tx parameters*	
Noise figure [dB]	$\leq$ 6	Output noise [dBm/Hz]	
Selectivity [4] [dB]		Band 1	$\leq$ -124
1st adj. ch. (f_c $\pm$5 MHz)	$\geq$ 33	Band 2	$\leq$ -107
2nd adj. ch. (f_c $\pm$10 MHz)	$\geq$ 49	Band 3	$\leq$ -140
Remaining Rx-band	$\geq$ 51	ACLR [dB]	
1980 – 2025 MHz	$\geq$ 56	f_c $\pm$5 MHz	$\geq$ 34
Tx-band	$\geq$ 77	f_c $\pm$10 MHz	$\geq$ 44
Intercept points [dBm]		IQ imbalance [3]	
iIP_2 (f_c $\pm$10 MHz)	$\geq$ -23	Amplitude [dB]	$\leq$ 1.4
iIP_2 ($f_c$$\pm$15 MHz)	$\geq$ 1	Phase [deg]	$\leq$ 5
iIP_2 (Tx-band)	$\geq$ 57	Average offset [5]	
iIP_3 (f_c $\pm$(10 - 20) MHz)	$\geq$ -23	Amplitude [dB]	$\leq$ 0.4
iIP_3 (1670 - 2025 MHz)	$\geq$ -5	Phase response [deg]	$\leq$ 4
		LSR [4] [dB]	$\leq$ -27

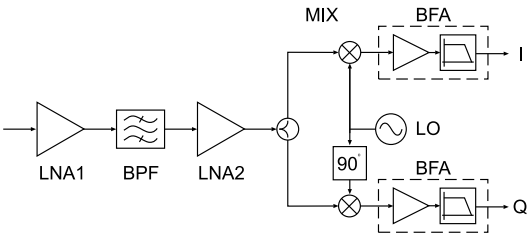

Figure 3. Direct-conversion receiver.

of 3 dB, the required attenuation must be at least 31 dB from 1670 MHz to 2025 MHz. The proposed block requirements are listed in Table V. The gain budget represents a compromise between NF and iIP_n and as such several budgets could be made resulting in different sets of NF and iIP_n. Requirements to NF are found using Friis's cascade formulae while requirements to iIP_3 are found using the cascade formulae described in [6]. The BPF is assumed to be passive and thus without significance when concerning linearity. Second order non-linearity is only critical for blocks operating at baseband and is therefore only specified for the *mixer* (MIX) and the *baseband filter and amplifier* (BFA). In this configuration, Tx-leakage only sets the requirements to *Low noise amplifier number 1* (LNA1). Requirements to iIP_2 represent compromises between how much distortion power the MIX and the BFA are allowed to generate. The budget in Table V allows MIX to

Table V. Receiver block requirements.

Block	*LNA1*	*BPF*	*LNA2*	*MIX*	*BFA*
Gain [dB]	15	-3	9	10	–
NF [dB]	≤ 4	≤ 3	≤ 4	≤ 16	≤ 31
Intercept points [dBm]					
iIP_2 (f_c ±10 MHz)	–	–	–	≥ 1	≥ 11
iIP_2 (f_c ±15 MHz)	–	–	–	≥ 23	≥ 39
iIP_2 (Tx)	–	–	–	≥ 23	≥ 39
iIP_3 (f_c ±(10 - 20) MHz)	$\geq$ -4	–	$\geq$ -6	≥ 0	≥ 10
iIP_3 (1670 - 2025 MHz)	$\geq$ -4	–	$\geq$ -6	≥ 0	≥ 10

generate most of the distortion power. At high frequency offsets, this means that seemingly harsh requirements are made to BFA. However, since the requirements to iIP_2 are based on interfering signals at 7 times the BFA cut-off frequency, this is not considered to be a critical design parameter. Some tolerances must be specified for all block gains to accommodate different variations. These tolerances require an additional margin to be put on the performance parameters in Table V. Based on these block requirements, it is clear that meeting the test specifications listed in the UTRA/FDD standard is by no means unrealistic. Being able to operate LNA1 at a noise figure of 4 dB makes the design of this block less critical. In terms of linearity, the continuous presence of the Tx-signal sets the most stringent requirements to the receiver. This problem becomes less severe when an interstage bandpass filter is used.

5.2. Transmitter Block Requirements

The direct up-conversion transmitter architecture is illustrated in Figure 4. When calculating the output noise, intermodulation in the PA

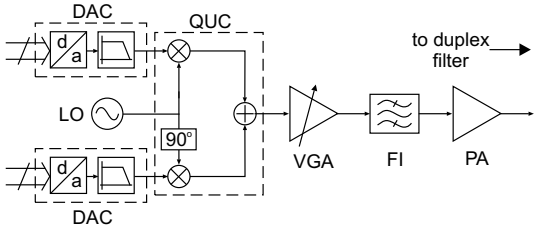

Figure 4. Direct up-conversion transmitter.

must be considered. It is assumed that the conversion gain is equal to

the actual gain and that this can be taken into account by doubling the effective noise bandwidth. A set of block requirements to in-band gain, NF and ACLR is proposed in Table VI. Noise and gain are assumed

Table VI. Transmitter block requirements.

Block	*QUC*	*VGA*	*FI*	*PA*
Gain [dB]	0	13	-2	25
NF [dB]	≤ 10	≤ 4	≤ 2	≤ 5
ACLR [dB]				
f_c ±5 MHz	≥ 43	≥ 45	–	≥ 35
f_c ±10 MHz	≥ 53	≥ 55	–	≥ 45

constant for all frequencies under observation, except for the PA, where a gain of 23 dB and a NF of 7 dB are assumed for band 3 and the image of this band. NF is specified so the overall requirement to noise in band 1 is met. To meet the more harsh requirement to noise in band 3, the *filter* (FI) must attenuate this band and the image with 21 dB. When the transmitter is operated at the highest frequency, the image may be offset 70 MHz from the lower edge of the Tx-band. Therefore, FI must provide 21 dB of attenuation at ±70 MHz offsets from the Tx-band. To omit FI the duplex filter must provide 49 dB of Tx-Rx isolation in the Rx band. The total ALCR generated by n circuits, $ACLR_T$, can be found from the ACLR of each circuit, $ACLR_m|_{m=1,2,\ldots,n}$, using Eq. 2, where all ACLR are represented in numbers.

$$ACLR_T = \frac{1}{\sum_{m=1}^{n} ACLR_m^{-1}} \tag{2}$$

As was the case for the receiver, tolerances on block requirements must be specified in order to accommodate different variations. The proposed gain budget means that the average output power of the *quadrature up-converter* (QUC) is -7 dBm. The proposed LO power is -6 dBm. To obtain the proposed LSR the LO-leakage must thus be -28 dB or less. If the LO power is increased, requirements to LO-leakage becomes more harsh. The requirement to output noise in band 1 sets harsh requirements to noise in the QUC. Image mixing in the PA prevents FI from removing this noise, because the image is inside the Tx-band. The only way to allow for an increase in the QUC noise figure, is to attenuate band 1 in the duplex filter.

6. Conclusion

In this paper, a set of UE transceiver requirements have been derived from the UTRA/FDD standard. Plausible block requirements for a direct-conversion receiver are proposed. FDD operation means that Rx and Tx may be active simultaneously. This results in a harsh requirement to Rx linearity. Tx specifications are translated to block requirements for a direct up-conversion transmitter. FDD operation means that an RF band-pass filter is required in the Tx chain to reduce Tx-noise in the Rx band. It should be noted that requirements proposed in this document are based directly on specifications. In practice, some margin must be included to take into account fabrication tolerances and other uncertainties. Also, it is worth noting that UTRA/FDD is an interference limited system to a wide extent, where any additional performance surplus on the UE will lead to increased system capacity. Hence, network providers may prefer UEs with better performance. UE manufacturers may therefore wish to exceed specifications to gain market shares.

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Authors' Vitae

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On the Design of a Differential Common Collector Negative Resistance

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On the Design of a Differential Common Collector Negative Resistance

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Abstract

Q-enhancement circuits are interesting to facilitate high quality on-chip filters for high performance personal mobile communication systems. This paper presents a detailed study of a differential Q-enhancement circuit, which presents analytical expressions for the input impedance based on a simple and a general transistor model. The theory is validated by comparative measurements on a BJT based circuit. The work also investigates the performance dependence of capacitance level in the circuit.

1. Introduction

The advent of low cost high speed CMOS processes has made RF system on chip an interesting topic for new standards for cellular telephones like EDGE and UMTS. Sharp filters are required in direct conversion receivers and transmitters for UMTS [1], but such filters are not very well implemented using on-chip passive components. The problem is that sharp filters require high Q components, but especially on-chip inductors have great losses and therefore offer low Q. The Q can be improved if a negative resistance is placed in parallel with the inductor. Several approaches for generating negative resistance exists. The most popular ones use positive feedback between two transistors [2], [3], [4] and [5], but single transistor solutions using one transistor together with reactive components have also been reported [3], [4] and [6]. Common for these publications is that only simple expressions are given to describe be basic functionality of the circuits, while effects of parasitics are ignored. This paper presents an analysis of a differential common collector negative resistance that includes transistor parasitics.

2. Differential Common Collector Negative Resistance

Single ended common drain Q-enhancement circuits are presented in [3] and [4]. A diagram of a differential version is shown in Figure 1. The transistors M_1 and M_2 comprise the active elements, while M_3 and M_4 are for biasing only. Both FET and BJT transistors can be used. The approach requires two reactive loads at each transistor. In Figure 1 the capacitors C_1, C_2 and C_3 provide the reactive loads, but theoretically they might as well be implemented as inductors, as long as all loads are of the same type. Capacitors are preferred in practice because they block DC providing an easier circuit topology. The negative resistance is created between the bases of M_1 and M_2. The Q-enhanced inductor

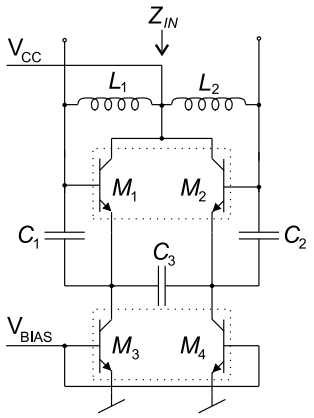

Figure 1: Diagram of the differential Q-enhancement circuit.

may therefore be used for biasing purposes as shown with L_1 and L_2 in Figure 1.

In [3] and [4] the resulting input impedance is expressed by a simple expression taking only the reactive loads and the transconductance of the transistors into account. Such expressions can provide an intuitive idea of the operation of the circuit. A simple expression can be found for the differential input impedance of the circuit in Figure 1, but for the expression to follow the behaviour measured on actual circuits, it is necessary to use the actual transadmittance y_{21} instead of the transconductance. Assuming the simple transistor model described above, identical transistors ($y_{21M1} = y_{21M2} = y_{21}$), and ignoring L_1 and L_2 give:

$$Z_{IN}(f) = -\frac{y_{21}}{4\pi^2 f^2 C_1 C_3} - \frac{j}{2\pi f}\left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right) \quad (1)$$

It should be noted that a requirement for the above is that $y_{21M1}C_2 = y_{21M2}C_1$ due to the made assumptions — otherwise Kirchoffs current law is violated. Although Eq. (1) may be sufficiently exact in some cases there are still parasitics in the transistors that are not taken into account. Especially the output impedance of the transistors may be significant and, being mainly resistive, degrade the potential Q-enhancement. To take into account more parasitics in the transistors, a more detailed transistor model is used. The used transistor π-model [7] for $M_1 - M_4$ is shown in Figure 2. Using this model means that transistor parameters are bias and frequency dependent.

The small signal diagram of the Q-enhancement circuit in Figure 1 can then be described as shown in Figure 3. In

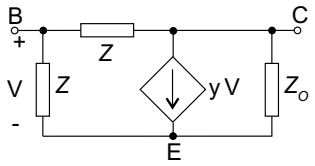

Figure 2: Small signal model of the transistors.

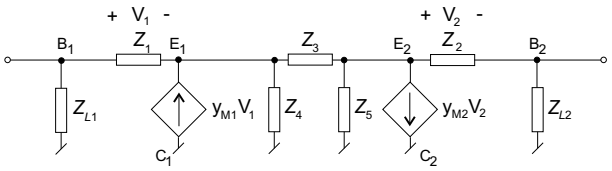

Figure 3: Small signal diagram of the negative resistor. B/E/C indicates Base/Emitter/Collector of the M_1 and M_2 transistors

Figure 3 the impedances are:

$$Z_{L1} = j2\pi f L_1 \parallel Z_{\mu M1} \quad (2)$$

$$Z_1 = \frac{1}{j2\pi f C_1} \parallel Z_{\pi M1} \quad (3)$$

$$Z_2 = \frac{1}{j2\pi f C_2} \parallel Z_{\pi M2} \quad (4)$$

$$Z_3 = \frac{1}{j2\pi f C_3} \quad (5)$$

$$Z_4 = Z_{oM1} \parallel Z_{oM3} \parallel Z_{\mu M3} \quad (6)$$

$$Z_5 = Z_{oM2} \parallel Z_{oM4} \parallel Z_{\mu M4} \quad (7)$$

$$Z_{L2} = j2\pi f L_2 \parallel Z_{\mu M2} \quad (8)$$

The input impedance seen into the B_1 and B_2 nodes on Figure 3 is:

$$Z_{IN} = (Z_{L1} + Z_{L2}) \parallel (Z_1 + Z_2 + Z_3(a+b) + c) \quad (9)$$

where:

$$a = \frac{Z_4}{Z_3 + Z_4 + Z_5} \quad (10)$$

$$b = \frac{Z_5}{Z_3 + Z_4 + Z_5} \quad (11)$$

$$c = y_{M1} Z_1 a + y_{M2} Z_2 b \quad (12)$$

3. Validation of Expressions

This section serves to validate Eqs. (1) and (9), giving an impression on the accuracy of the expressions. In order to validate the expressions, experiments were made with a discrete PCB implementation of the circuit working from 10 MHz — 100 MHz. This approach allowed for stand alone measurements on the components that were actually used, making good estimates of actual impedances possible.

Apart from the generic diagram shown in Figure 1, de-coupling capacitors of 1 μF were added to the supply and bias leads. When a differential signal is applied, these capacitors are at virtual ground and should not influence the differential impedance. Furthermore, the striplines, leading from the inductors to the remaining circuits on the PCB, were found to be critical at higher frequencies and are therefore included in the simulations of Eq. (9).

The circuit was tested in four configurations listed in Table 1. During all tests L_1 and L_2 were 220 nH. The 2xBC-847-S

Table 1: Configurations used during the tests.

Test	C_1, C_2, C_3	M_1, M_2, M_3, M_4
1	180 pF	BC-847-S
2	100 pF	BC-847-S
3	180 pF	2xBC-847-S
4	100 pF	2xBC-847-S

tests are with two single BC-847-S transistors in parallel. All the measurements were conducted with a supply voltage of 2.5 V. During all the tests, the bias voltage V_{BIAS} was changed to investigate the effects of changing operational points in the transistors. The individual measurements in the sweeps are distinguished by letters a-c as listed in Table 2. Voltages and supply current in the complete neg-

Table 2: Bias current in mA used during the tests (adjusted via V_{BIAS}).

Case	Test 1 & 2	Test 3 & 4
a	6.8	11.0
b	14.0	26.3
c	27.4	44.7

ative resistance circuit were measured during the sweeps. These data were used to recreate the biasing of each individual transistor during later measurements of parasitics and transconductance. L_1 and L_2 together with striplines on the PCB were measured, and their impedances subtracted from the impedances measured on the negative resistance circuit. This means that Z_{L1} and Z_{L2} in Eq. (9) in this case only include $Z_{\mu M1}$ and $Z_{\mu M2}$, respectively.

Impedances are derived from S-parameter measurements. Indices refer to the components on which the impedances are measured, and Z_π, Z_μ and Z_o refer to impedances in the π transistor model described in [7].

Since the negative resistance is to be placed in parallel with the inductor to be Q-enhanced, the admittance Y_{IN} rather than Z_{IN} is relevant. The estimated admittances are compared to the admittances measured on the negative resistance circuits, taking into account the effects of L_1, L_2 and the PCB.

First, the simplified model yielding Eq. (1) is considered. The results are shown in Figures 4 and 5. As seen there is quite some difference in measured and simulated results — even at low frequencies. The results predicted from Eq. (1) overestimated the obtainable negative conductance which is quite reasonable as Eq. (1) ignores significant parasitic losses in the transistors. Besides the numerical disagreement between estimated and measured results, it should be noted that the effect of an apparent optimum of negative resistance is both appearing in estimations and measurements.

Second, results from the more complicated Eq. (9) are compared with measurements. The measurement conditions are the same as for the previous presented case. The results are shown in Figures 6 and 7. The agreement between simulations and measurements is now very good — the relative difference is generally less than 4%. Similar conclusions can be drawn for the imaginary part of the input impedance although not shown here.

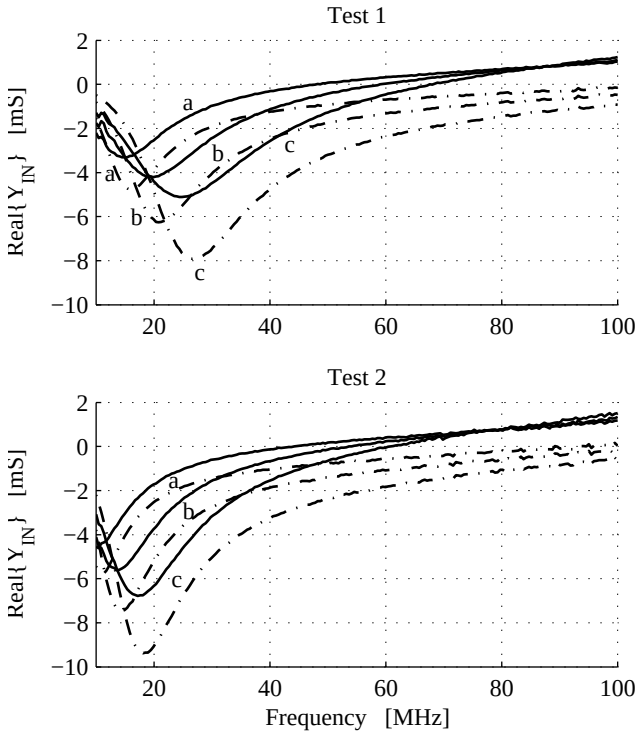

Figure 4: Real part of the input admittance versus frequency measured (Solid lines) and estimated from Eq. (1) (dashed lines). Letters a-c refer to the conditions in Table 2.

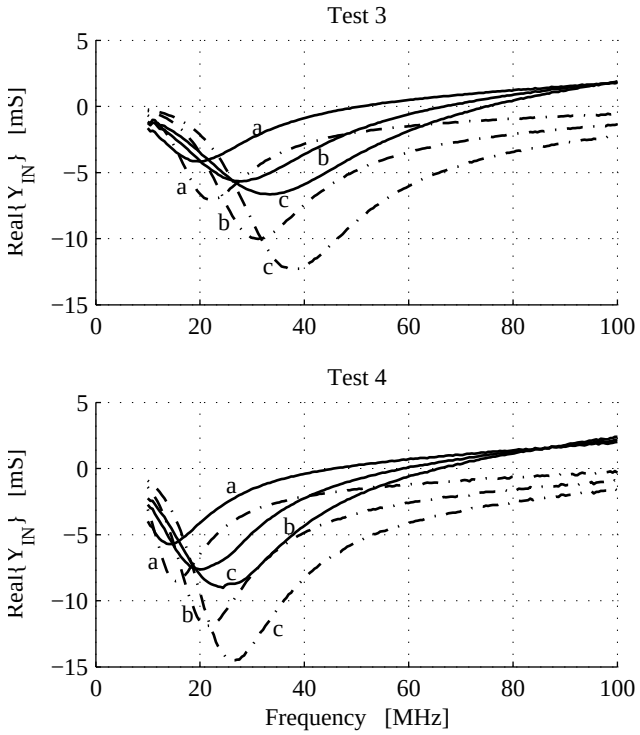

Figure 5: Real part of the input admittance versus frequency measured (solid lines) and estimated from Eq. (1) (dashed lines). Letters a-c refer to the conditions in Table 2.

4. Design Considerations

When viewing the results from Figures 6 and 7 it seems as if there is an optimum frequency where the real part of the input admittance is numerically largest. Apparently this optimum depends on both biasing and the capacitance level ($C_1 = C_2 = C_3$). Not surprisingly it seems as if a larger g_m of the transistors leads to a numerically larger maximum of the real part of the input admittance, but for low frequencies, the numerical value of the real part declines as g_m is increased. The dependence versus capacitance level may not be that obvious.

To investigate impact of the capacitance level on the real part of the input admittance, Eq. (9) is swept versus capacitance level for both types of transistors used. Everything except the capacitance level ($C_1 = C_2 = C_3$) is kept as was the case for the previous simulations. The results of this are shown in Figure 8 for the single BC-847-S transistor and in Figure 9 for the parallel transistor 2xBC-847-S. The frequency is in both cases 30.25 MHz.

The general pattern with a maximal numerical value of real admittance is recognised in Figures 8 and 9. This means that an optimal choice of capacitance exists for operation at some frequency.

5. Conclusions

A circuit that is usable for Q-enhancement of integrated inductors is investigated. Two expressions are derived for the input impedance of the Q-enhancement circuit. One expression is based on a very simple transistor model where only capacitors and the transadmittance of the active transistors are included. The other expression is for a full π-model of all transistors. Both expressions explain the overall behavior of the circuit, but the complicated expressions by far outperforms the simple one. The work is validated through a low frequency discrete design example. Even at the low frequencies (10-100 MHz) the parasitics are sufficiently important to reveal differences between the two expressions. Further analysis of the expression revealed that an optimal choice of capacitance level in the circuit exists.

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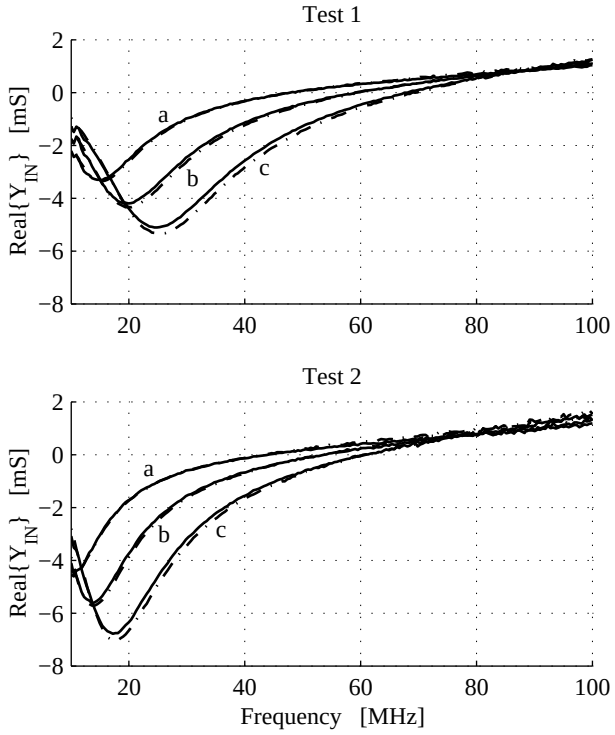

Figure 6: Real part of the input admittance versus frequency measured (solid lines) and estimated from Eq. (9) (dashed lines). Letters a-c refer to the conditions in Table 2.

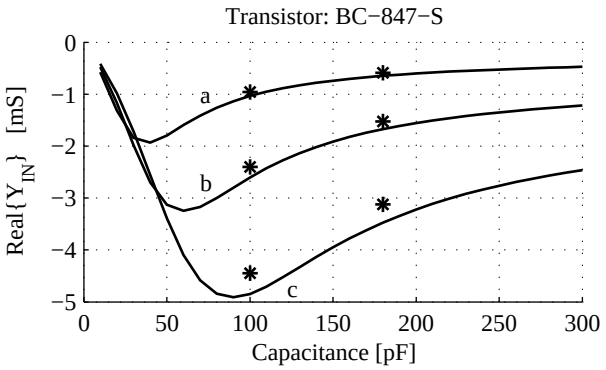

Figure 8: Real part of the input admittance versus capacitance level($C_1 = C_2 = C_3$) measured (*) and estimated from Eq. (9) (solid lines) for the BC-847-S transistor. Letters a-c refer to the conditions in Table 2.

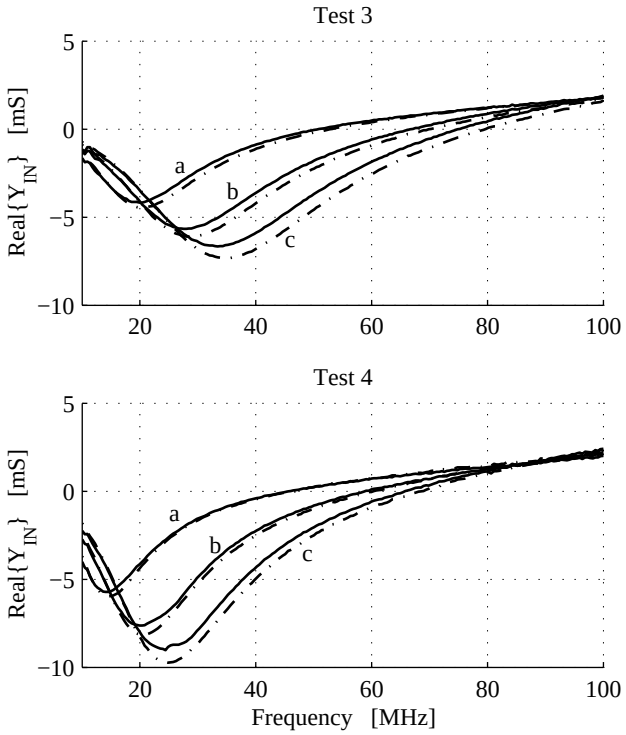

Figure 7: Real part of the input admittance versus fequency measured (solid lines) and estimated from Eq. (9) (dashed lines). Letters a-c refer to the conditions in Table 2.

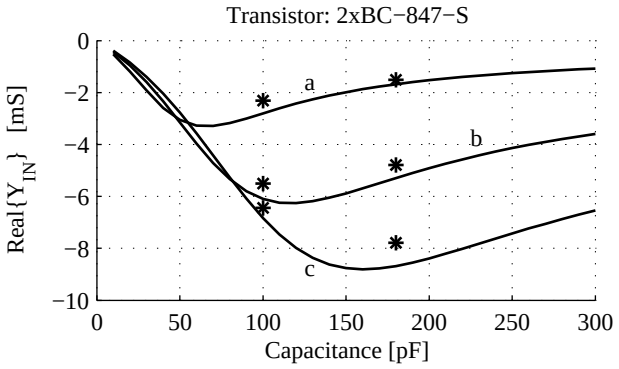

Figure 9: Real part of the input admittance versus capacitance level ($C_1 = C_2 = C_3$) measured (*) and estimated from Eq. (9). Letters a-c refer to the conditions in Table 2.) (solid lines) for the 2xBC-847-S transistor. Letters a-c refer to the conditions in Table 2.

Simulation of EVM Due to Circuit Imperfections in UMTS/FDD Transmitters

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Simulation of EVM Due to Circuit Imperfections in UMTS/FDD Transmitters

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Abstract

When a signal is passed through an analog circuit errors will be added to it due to circuit imperfections. This deteriorates the signal. In UMTS/FDD the quality of the transmitted signal is specified by the Error Vector Magnitude (EVM). This paper presents an analysis of the EVM that circuit imperfections, that may appear in UMTS transmitters, generate and gives a rough estimation of how several contributions combine. To aid this analysis a simulation environment is constructed in MATLAB. Results from the simulations are backed up by measurements and analytical estimations.

1. Introduction

During recent years, new standards for mobile telephony such as EDGE and UMTS have emerged. These standards offer higher data rate for mobile telephones than is available with today's versions of GSM. The new standards also introduce new specifications of transmitter performance. One such specification is Error Vector Magnitude (EVM), which is a measure for all the transmitter generated errors that affect the desired signal. To make the system design of a UMTS transmitter it is necessary to know how different circuit imperfections influence EVM. The literature contains many investigations of EVM, where some combines several effects [1], while others present single effects in specific systems, like channel imperfections [2] for UMTS or phase errors for other systems [3]. An analysis of how each of these parameters influence EVM, when measured as prescribed in the specifications [4], has not been found, and such knowledge is necessary to make a budget for a transmitter for UMTS/FDD handsets. An analysis, including analytical investigations, simulations and measurements of critical errors that might appear in a UMTS/FDD transmitter is presented here.

2. Signal Representation and EVM

The simulation system is illustrated in Figure 1. The modulator generates a test signal as specified for tests of UMTS/FDD handsets [4]. This signal is feed to an EVM calculator, where it is the reference for the EVM calculations, and exposed to some error that may be present in the transmitter. The erroneous signal is feed to the EVM calculator and the EVM caused by the error is calculated.

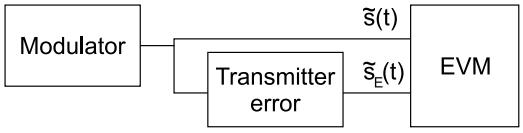

Figure 1: Illustration of simulation system.

2.1. Modulation

The modulation procedure is described in detail in [5]. A number of reference measurement signals for use in Tx-tests of handsets are defined in [4]. Only one is used and this is the signal with a 12.2 kbps information bit channel. It is important that particularly the right scrambling codes and weight of the channels in the signal are used. If this is not the case the simulated performance may differ from what is achieved during conformance tests of the mobile handsets. A signal with the length of one test frame is generated and saved in a file. This signal is used in both measurements and simulations. The modulation results in a In-phase and Quadrature (I/Q) part that are represented as the complex baseband signal defined by:

$$\tilde{s}(t) = I(t) + jQ(t) \tag{1}$$

-where the $\tilde{}$ nomenclature is used to defined the signal as complex baseband. The complex baseband representation allows us to project mathematical operations, that actually are taking place at some frequency (f_c), to baseband, but to derive analytical expressions for EVM it is sometimes necessary to start with a signal at f_c, which is represented mathematically by:

$$s(t) = I(t)\cos(2\pi f_c t) + Q(t)\sin(2\pi f_c t) \tag{2}$$

2.2. EVM Calculation

EVM measurements are made using UMTS transmitter test equipment, in this paper denoted Tx-tester, which

typically operates at f_c. The process of converting the signals to f_c and further manipulations of the signal in the analog transmitter chain introduces errors, either through distortion or addition of unwanted power, i.e. noise. Assuming that a signal, $s_E(t)$, equal to $s(t)$ plus an error function $e(t)$, is fed to the Tx-tester, we may obtain estimates of the erroneous I/Q signals $\widehat{I}(t)$ and $\widehat{Q}(t)$ from:

$$\begin{aligned} \widehat{I}(t) &= I(t) + e_I(t) \\ &= 2s_E(t)\cos(2\pi f_c t) \qquad (3) \\ \widehat{Q}(t) &= Q(t) + e_Q(t) \\ &= 2s_E(t)\sin(2\pi f_c t) \qquad (4) \end{aligned}$$

- if the signal is low pass filtered and: $\widetilde{e}(t) = e_I(t) + je_Q(t)$. With $< \bullet >$ denoting averaging over one time frame, EVM (as defined in [4]), may be found by:

$$\text{EVM} = \sqrt{\frac{< e_I(t)^2 + e_Q(t)^2 >}{< I(t)^2 + Q(t)^2 >}} \cdot 100\% \qquad (5)$$

During an EVM test, the Tx tester only knows $\widetilde{s}_E(t)$. According to [4] the reference signal $\widetilde{s}(t)$ should be estimated from this signal. The MATLAB system is simplified compared to this. $\widetilde{s}(t)$ is taken directly from the modulator and compared to $\widetilde{s}_E(t)$. It is important that the phase and time synchronization is maintained between the two signals.

EVM is calculated from one sample of every chip. Before EVM is calculated, both $\widetilde{s}(t)$ and $\widetilde{s}_E(t)$ are filtered with the pulse shaping filter [4]. This has the effect that only in-band error contributions of are included in EVM. Furthermore, frequency, timing, phase and amplitude of the signals may be adjusted so the smallest possible EVM is obtained.

The MATLAB simulation tool uses a trial and error approach to make the time adjustments. This is done by shifting the sampling time of $\widetilde{s}_E(t)$ in comparison with $\widetilde{s}(t)$, and then calculate EVM. This means that the resolution for time offsets depends on the sampling frequency. For each tested time offset the signal is down sampled to one sample per chip and adjustments are made so that $\widetilde{s}_E(t)$ and $\widetilde{s}(t)$ has the same averaged phase, and Root Mean Square amplitude.

3. Imperfections that Generate EVM

This section investigates different circuit imperfections's effects on EVM. A typical approach to up-conversion in UMTS transmitters is illustrated in Figure 2. It also illustrates most of the circuit imperfections that are considered in this paper.

3.1. I/Q Amplitude Offset

If the I/Q signals are converted to f_c with different amplitude weights, the difference in weight may be expressed by A and $s_E(t)$ may be expressed by:

$$s_E(t) = AI(t)\cos(2\pi f_c t) + Q(t)\sin(2\pi f_c t) \qquad (6)$$

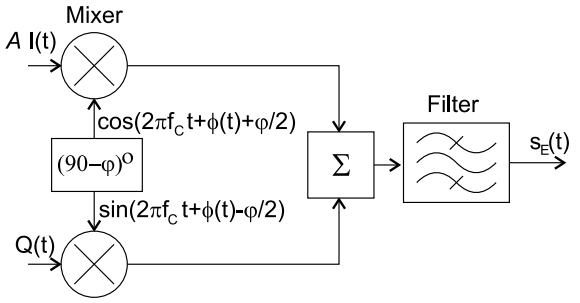

Figure 2: principal up-conversion approach in UMTS transmitters with sources of EVM indicated.

The complex baseband representation is obtained by down-conversion as described in Section 2:

$$\widetilde{s}_E(t) = AI(t) + jQ(t) \qquad (7)$$

This transmitter error function is implemented in MATLAB. The amplitude offset produces errors in both phase and power. It appears that the amplitude errors are most significant. Adjusting for equal average power and assuming that $< I(t)^2 >=< Q(t)^2 >$, an analytical estimate of EVM may be found by:

$$\text{EVM}_\text{A} \approx \sqrt{\left| 2 - \sqrt{\frac{2}{A^2+1}}\,(A+1) \right|} \cdot 100\% \qquad (8)$$

The effect is measured using a simple setup where $I(t)$ and $Q(t)$ are converted to analog and feed directly to an Anritsu MS 8609A Tx-tester. The setup generates an EVM of about 2 %. Figure 3 shows EVM_A. It is

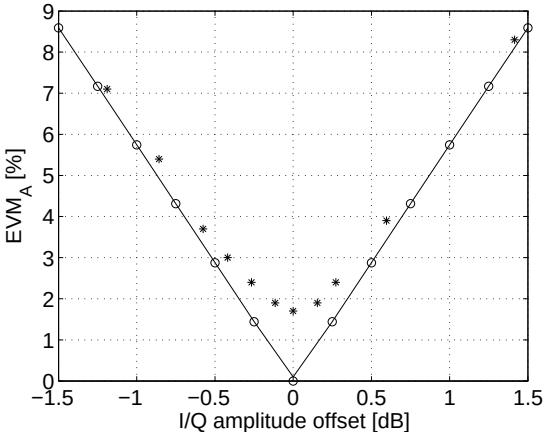

Figure 3: Solid lines are simulated values, circles are estimated from Eq. 8 and dots are measured values.

seen that both the MATLAB simulations and the analytical approximation in Eq. 8 estimate EVM well.

3.2. I/Q Phase Offset

There may be an offset in the phase of the I/Q parts. This may be represented by a phase offset in the single

tone signals that are used to up-convert the signal. The up-converted signal may be expressed by:

$$s_E(t) = I(t)\cos\left(2\pi f_c t + \frac{\varphi}{2}\right) + Q(t)\sin\left(2\pi f_c t - \frac{\varphi}{2}\right) \quad (9)$$

When $\widetilde{s}_E(t)$ is down-converted as described in Section 2, the complex baseband signal becomes:

$$\widetilde{s}_E(t) = I(t)\cos\left(\frac{\varphi}{2}\right) - Q(t)\sin\left(\frac{\varphi}{2}\right) + j\left(I(t)\sin\left(\frac{\varphi}{2}\right) + Q(t)\cos\left(\frac{\varphi}{2}\right)\right) \quad (10)$$

An analytical expression for EVM may be found from Eq. 10. Having applied a phase shift of $\pm\frac{\varphi}{2}$ to the I/Q carriers instead of φ at only one carrier, no phase offset should be necessary in the EVM calculations. The expressions contain the average of products of I(t) and Q(t), but if they are mutually uncorrelated, the average of the products is zero. The phase offsets cause changes in amplitude. Using the optimal amplitude regulation, EVM may be found analytically by:

$$\mathrm{EVM_{PIQ}} = \sqrt{1 - \left(\cos\left(\frac{\varphi}{2}\right)\right)^2} \cdot 100\% \quad (11)$$

In practice the amplitude adjustments only cause minor improvements in $\mathrm{EVM_{PIQ}}$. The MATLAB simulation of the transmitter error functions implements Eq. 10. Measusrements are conducted using a HP-E4433B signal generator to up-convert the I/Q signals to 1.95 GHz, which then is fed to the Tx-tester. The phase difference is generated using a built-in function in HP-E4433B. The EVM of the setup is approx 2 %. $\mathrm{EVM_{PIQ}}$ is shown in Figure 4. The measured

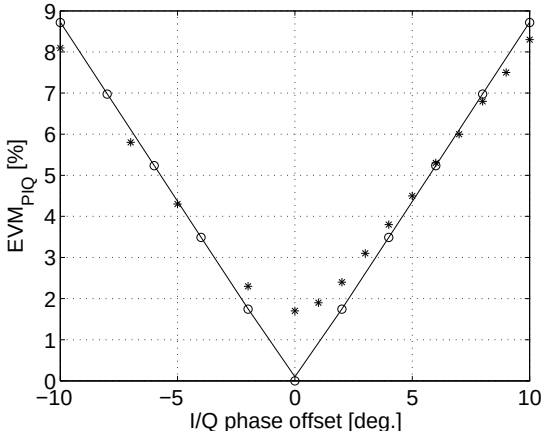

Figure 4: Solid lines are simulated values, circles are estimated from Eq 11 and dots are measured values.

$\mathrm{EVM_{PIQ}}$ tends to be smaller than simulated and estimated. However the difference is so small that it may be explained by tolerances in the phase offset in the signal generator.

3.3. Phase Noise

The carriers, represented by $\cos(2\pi f_c t)$ and $\sin(2\pi f_c t)$, may be covered with phase noise. Normally the carriers are originated from the same source. The phase noise in the carriers may therefore be described by the same noise function $\phi(t)$ as illustrated in Figure 2. The resulting up-converted signal, $s_E(t)$, becomes:

$$s_E(t) = I(t)\cos(2\pi f_c t + \phi(t)) + Q(t)\sin(2\pi f_c t + \phi(t)) \quad (12)$$

The down converted complex baseband representation is found to be:

$$\widetilde{s}_E(t) = I(t)\cos(\phi(t)) + Q(t)\sin(\phi(t)) + j(-I(t)\sin(\phi(t)) + Q(t)\cos(\phi(t))) \quad (13)$$

Having applied the same phase shift to I and Q, the average power is not changed. Assuming that $<\phi(t)>$ is zero, a constant phase offset will not minimize EVM, and an analytical expression for EVM, (assuming that I(t) and Q(t) are mutually uncorrelated) can be derived:

$$\mathrm{EVM_{PN}} = \sqrt{2 - 2 <\cos(\phi(t))>} \cdot 100\% \quad (14)$$

For a zero mean phase noise function $\phi(t)$ with small peak to average values, $<\cos(\phi(t))>$ may be approximated by the cosine of the Root Mean Square (RMS) value of $\phi(t)$, which is normally specified. Under these circumstances Eq. 14 may be expressed by:

$$\mathrm{EVM_{PN}} \approx \sqrt{2 - 2cos(\phi)} \cdot 100\% \quad (15)$$

- where ϕ is the RMS of $\phi(t)$. Eq. 15 is equal to expression 11 in [3]. Eq. 13 is implemented in MATLAB using random phase noise for $\phi(t)$. The obtained noise spectrum is flat and goes from DC to the sampling frequency, but due to the filtering in the EVM measurement, only in-band phase noise adds to $\mathrm{EVM_{PN}}$. This is compensated by multiplying the phase function by the square of the over-sampling ratio. During measurements the I/Q signals are fed to the signal generator which converts the signal to 1.95 GHz and adds noise. The RMS noise error is read from the Tx-tester. $\mathrm{EVM_{PN}}$ is shown in Figure 5. Good agreement is achieved between measured, theoretical and simulated results.

3.4. Imperfect Frequency Response

The circuits in the transmitter may change characteristics significantly over frequency. This means that amplitude and phase response may change for different parts of the signal as illustrated in Figure 6. Here the magnitude of the response changes by A_F over the signal's bandwidth, which means that different parts of the signal will be exposed to different gain. If the circuit has a constant group delay for all frequencies, the phase should depend on frequency in a linear manner

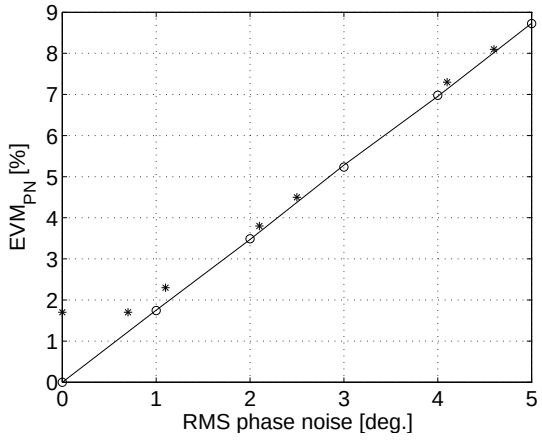

Figure 5: Solid lines are simulated values, circles are estimated from Eq 15 and dots are measured values.

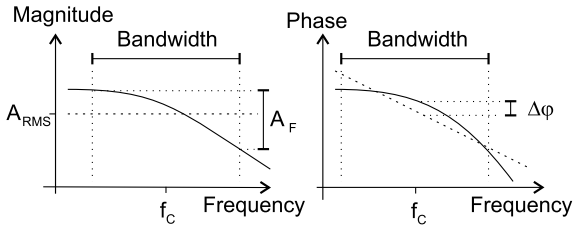

Figure 6: Illustration of frequency responses. Solid lines represent a non-ideal response and dashed lines an ideal response.

as illustrated by the dashed line. If this is not the case, further errors will be added to the signal.
Filters with a narrow bandwidth compared to the signal are good examples of circuits where non-ideal frequency responses may cause significant EVM. EVM due to imperfect filtering may be expressed by [2]:

$$\mathrm{EVM_F} \approx \sqrt{\Delta A_R + (\tan(\Delta\varphi_R))} \cdot 100\% \qquad (16)$$

where ΔA_R is the RMS magnitude error to the RMS magnitude in the band (A_{RMS} in Figure 6), and $\Delta\varphi_R$ is the RMS phase error, compared to the phase function that generates the smallest RMS phase error. The RMS values are only to be calculated within the band occupied by the signal.
If a complex frequency response of a filter is known, Eq. 16 may be used to estimate EVM. To test this the response of a band pass filter with a centre frequency of 380 MHz was measured using an S-parameter test set. A MATLAB routine that derives ΔA_R and $\Delta\varphi_R$ from the measured S_{21} values is made. Another MATLAB routine that simulates the filter using a modulated signal is also made. A few important notes on the simulations are presented here: I) The filtering is done in the frequency domain. The signal is represented in it's up-converted form, i.e as the Fourier transform of $s(t)$. II) The measured filter response is used, but it is offset so the centre frequency is at 10 MHz instead of 380 MHz. f_c of the signal is offset accordingly. III) A higher sample frequency in the filter response is obtained by estimating a set of coefficients for the filter, using the MATLAB function "INVFREQS". Together with an extended frequency axis, these are applied to "FREQS" to form an estimate of the filter response up to the desired sample frequency. IV) The filtered signal is compensated for the group delay and phase offset in the filter to maintain synchronisation. The compensation is estimated from the slope and constant of a first order function, fitted to the filter's phase response in the relevant band using "POLYFIT".
The effects of filtering are also measured. The test signal is converted to f_c using HP-E4433B and fed through the filter, after which EVM is measured. To see the effect of an increasingly bad channel, several values of f_c are tested. The resulting $\mathrm{EVM_F}$ are shown in Figure 7. A difference between Eq. 16 and the simulations is seen even for moderate EVM. Since the simulation uses estimates of the filter response, a complete fit can not be expected.

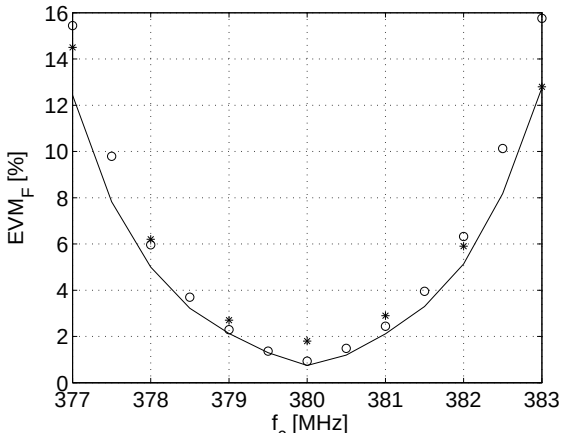

Figure 7: Solid lines are simulated by MATLAB, circles are estimated using MATLAB and Eq. 16, and dots are measured values.

3.5. Timing Offset Between Phase and Magnitude

The UMTS signal contains both amplitude and phase information. The up-conversion procedure illustrated in Figure 2 maintains the desired amplitude information thoughout the entire up-conversion, but in some cases advantages may be gained if the amplitude information is applied at f_c, as this allows the phase information to be up-converted using procedures that require constant envelope at f_c. This can be achieved using polar modulation. The functionality of a polar modulator is illustrated in Figure 8. The amplitude of the signal is represented by $A(t)$ and the phase by $\sigma(t)$. In this modulator there is a risk that phase and amplitude information become unsynchronized in time. This is illustrated by the time delay τ in Figure 8. The

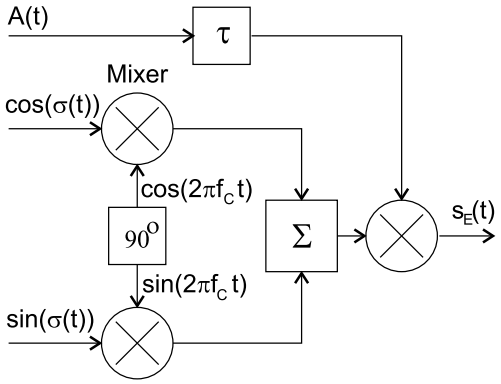

Figure 8: Basic up-conversion principle of the polar modulator.

resulting signal may then be expressed by:

$$\begin{aligned} s_E(t) &= A(t-\tau)\cos(\sigma(t))\cos(2\pi f_c t) \\ &\quad + A(t-\tau)\sin(\sigma(t))\sin(2\pi f_c t) \end{aligned} \quad (17)$$

and the complex baseband signal is:

$$\widetilde{s}_E(t) = A(t-\tau)\left(\cos(\sigma(t)) + j\sin(\sigma(t))\right) \quad (18)$$

When calulating EVM, a change in time synchronisation between the distorted signal and the reference signal is allowed. If the reference signal is changed by τ_R, the I/Q error functions may be found as:

$$\begin{aligned} e_I(t) &= A(t-\tau_R)\cos(\sigma(t-\tau_R)) \\ &\quad - A(t-\tau)\cos(\sigma(t)) \end{aligned} \quad (19)$$

$$\begin{aligned} e_Q(t) &= A(t-\tau_R)\sin(\sigma(t-\tau_R)) \\ &\quad - A(t-\tau)\sin(\sigma(t)) \end{aligned} \quad (20)$$

It is seen that the errors depend on how phase and magnitude change with time. As τ_R comes close to τ, the amplitude error decreases while the phase error increases. The choice of τ_R will be a compromise between optimising for amplitude error or phase error. Although not shown here, time offsets generate spectral re-growth, which indicates that the bandwidth of the error function $\widetilde{e}(t)$ is larger than that of the reference signal. A portion of the error power will therefore be removed by the filtering conducted before EVM is calculated. The error function therefore depends on the statistical properties of the signal, which will make an analytical expression for EVM complicated and not very general. Derivation of such expressions is therefore omitted here.

The effect of time offsets, are simulated in MATLAB. $\widetilde{s}_E(t)$ is generated by calculating $A(t)$ and $\sigma(t)$ from the modulated reference signal, and then shift the samples of $A(t)$ compared to $\sigma(t)$. The finite sampling rate allows for test points at $A(t \pm nT_S)$, where n is an integer and T_S is the time between samples.

Experiments are conducted using a system similar to the one shown in Figure 8. The phase information is feed to the signal generator, where it is converted to 1.95 GHz. Amplitude information is applied using a voltage controlled amplifier, which sensitivity to control voltage is known and accounted for in $A(t)$. The time offsets are achieved by shifting samples in the digital version of $A(t)$ before conversion to the analog domain. Measured and simulated EVM are shown in Figure 9. The measurement setup had a EVM of about

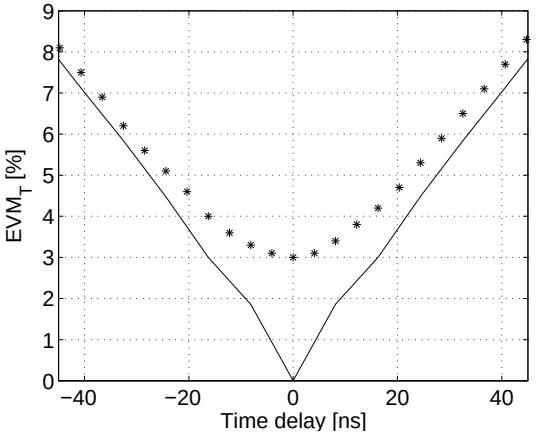

Figure 9: Solid lines are found by simulations in MATLAB and dots are measured values.

3 %. If this is submitted from the measured data, using Eq. 26 presented in Section 4, the fit becomes quite good.

4. EVM Budgets

The aim with the work presented so far is to be able to make a budget for EVM. To do this it is necessary to know how different contributions of EVM combine. Assuming that there are n effects operating on the signal $\widetilde{s}(t)$, the i^{th} contributor causes the EVM expressed by:

$$\mathrm{EVM}_i = \sqrt{\frac{< e_{Ii}(t)^2 + e_{Qi}(t)^2 >}{< |\widetilde{s}(t)|^2 >}} \cdot 100\% \quad (21)$$

- where i is an integer equal to or between 1 and n. The combined EVM, $\mathrm{EVM_C}$, may be expressed by each individual contribution by:

$$\mathrm{EVM_C} = \sqrt{\frac{< e_{Ic}(t)^2 + e_{Qc}(t)^2 >}{< |\widetilde{s}(t)|^2 >}} \cdot 100\% \quad (22)$$

- where:

$$e_{Ic}(t)^2 = \left(\sum_{i=1}^{n} e_{Ii}(t)\right)^2 \quad (23)$$

$$e_{Qc}(t)^2 = \left(\sum_{i=1}^{n} e_{Qi}(t)\right)^2 \quad (24)$$

If all the contributors to $\mathrm{EVM_C}$ produce mutually uncorrelated error functions, the average of their products

are zero and:

$$\sum_{i=1}^{n} < e_{Ii}(t)^2 + e_{Qi}(t)^2 > \quad = \quad < e_{Ic}(t)^2 + e_{Qc}(t)^2 > \tag{25}$$

The expression for $< e_{Ic}(t)^2 + e_{Qc}(t)^2 >$ may be inserted into Eq. 22 and $< |\widetilde{s}(t)|^2 >$ moved inside the resulting sum. The content of the sum may replaced by the square of Eq. 21 and $\mathrm{EVM_C}$ may be expressed by:

$$\mathrm{EVM_C} = \sqrt{\sum_{i=1}^{n} \mathrm{EVM}_i^2} \tag{26}$$

Eq 26 requires that the error functions are mutually uncorrelated. This assumption is investigated in the following. The MATLAB simulations presented so far only applied one imperfection at the time. Next simulations are conducted where several imperfections operate on the same signal, and in this way add several errors to the same signal. The combined simulated EVM, $\mathrm{EVM_{CS}}$, is calculated from this signal. To create a valid comparison, EVM from each imperfection is calculated and the combined EVM, $\mathrm{EVM_{CI}}$, is estimated from Eq. 26. Combinations of imperfections are listed in Table 1. The Resulting EVM from the individual imperfections are shown in Table 2 together with the combined EVM. It is seen that the estimates made from Eq. 26 are particularly inaccurate as soon as filtering is introduced together with phase noise. In these cases a relative error of approximately 7 % is seen. Although good for an initial guesses it must be concluded that Eq. 26 is not an exact expression. Simulations or measurements should always be made to back up the estimates.

Table 1: Combinations of sources of EVM.

Test	1	2	3	4	unit
A	0.50	0.50	0.50	1.00	dB
φ	3.00	3.00	3.00	6.00	deg.
$\phi(t)$	1.50	1.50	0	3.25	RMS deg.
f_c	379	–	379	378	MHz
τ	12.2	12.2	12.2	28.4	ns

Table 2: EVM originated from each contributor together with the combined EVM. $\mathrm{EVM_{CE}}$ is estimated using Eq. 26 and $\mathrm{EVM_{CS}}$ is simulated. All the data are in [%].

Test	1	2	3	4
$\mathrm{EVM_A}$	2.88	2.88	2.88	5.74
$\mathrm{EVM_{PIQ}}$	2.62	2.62	2.62	5.23
$\mathrm{EVM_{PN}}$	2.59	2.58	0	6.05
$\mathrm{EVM_F}$	2.13	–	2.13	5.00
$\mathrm{EVM_T}$	2.39	2.39	2.39	5.24
$\mathrm{EVM_{CE}}$	5.66	5.25	5.04	12.22
$\mathrm{EVM_{CS}}$	6.09	5.27	4.88	13.27

5. Conclusion

This paper has described efforts to simulate EVM in UMTS/FDD handsets in MATLAB. Three modules were implemented in MATLAB, one that generates a modulated signal, one that simulates circuit errors in the transmitter's analog circuits and one that calculates EVM. Simulated circuit errors included I/Q amplitude and phase imbalance, phase noise, non-ideal transfer functions and delays between phase and amplitude information. All the simulations were backed up by measurements conducted with the same signal. It could be concluded that the estimates made using MATLAB matched the measured results. Finally an expression that estimates the EVM combined from several errors was presented. The expression was verified through simulations using the same MATLAB system. It was found that the expression, when used on certain combinations of imperfections, estimated EVM with an error that was approximately 7 %, relative to the simulated EVM. The expression is therefore best suited for initial guesses, and should always be checked by measurements or simulations.

6. References

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An RF CMOS Differential Negative Resistance for Q-enhancement

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An RF CMOS Differential Negative Resistance for Q-enhancement

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Abstract

This paper presents a differential Q-enhancement circuit implemented in a standard 5 metal layer, 0.25 μm CMOS process. A differential conductance of -2.8 mS is obtained at 2 GHz. This allows the circuit to compensate for a resistance of approximately 360 Ω. The differential reactance at this frequency is equivalent to 1 pF. An analytical expression for the differential admittance is derived and compared with measurements and simulations. When no power is applied to the circuit, the simulations and estimates match the measured data well. However when supply and biasing are applied, the estimates become optimistic while the simulations and measurements still make a good match.

1. Introduction

System on chip is a promising way to shrink RF circuits in cellular telephones, allowing handsets to support several new standards like EDGE and UMTS. Sharp filters are required in direct conversion receivers and transmitters for UMTS [1], but such filters are not very well implemented with on-chip passive components, as they require resonators with high Q and losses in on-chip inductors limit the achievable Q in on-chip LC resonators. Q-enhancement is a popular way to compensate for this. Several implementations of Q-enhanced LC resonators are reported. Most are differential implementations with positive feedback, operating between 1 GHz and 2 GHz. Examples of such are presented in [2, 3, 4]. However solutions where one transistor is used together with reactive components are also reported [3, 5].
This paper presents an RF CMOS implementation of a differential design that use reactive components as well as transistors. The circuit is implemented in a 5 metal layer 0.25 μm 1 poly CMOS process.

2. Differential Admittance

The implemented Q-enhancement circuit is shown in Figure 1. The differential admittance of interest, $Y_{IN\,d}$, is generated between P_1 and P_2. Q-enhancement only requires that a negative conductance is present, but the circuit also generates a differential reactance that influences the centre frequency of the Q-enhanced LC tank.
M_1 and M_2 together with C_1, C_2 and C_3 generate the differential admittance. M_3 and M_4 are for biasing purposes only, while the inductor is used for biasing M_1 and M_2. The inductor may conveniently be part of the LC tank intended

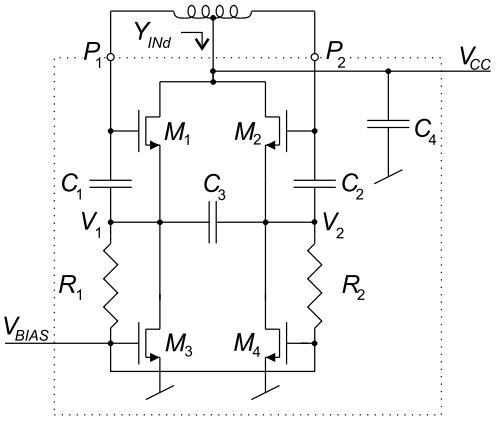

Figure 1: Q-enhancement circuit. The dotted box marks the components included on the chip. M_3, M_4, R_1, R_2, C_4 are not part of the active circuit, but they are needed for biasing and stabilisation.

for Q-enhancement, but it is not included on the chip. Simulations indicate that M_3 and M_4 are potentially unstable. To solve this R_1, R_2 and C_4 are added to the circuit.

A discrete low frequency version of the Q-enhancement circuit in Figure 1 is investigated in [6]. Here the simple small signal representation, shown in Figure 2, is used to describe each transistor. This transistor representation leads to the small signal diagram for differential operation of the entire circuit shown in Figure 3 [6].

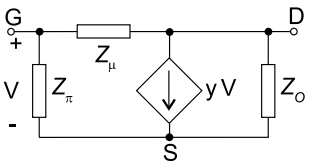

Figure 2: Simple transistor representation used in [6]. Notice that the trans admittance rather than the trans conductance is used.

An impedance analysis on this small signal diagram leads to the following expression for $Y_{IN\,d}$ [6]:

$$Y_{IN\,d} = \frac{1}{Z_5 + Z_4} + \frac{1}{Z_1 + Z_2 + Z_3(a+b) + c} \quad (1)$$

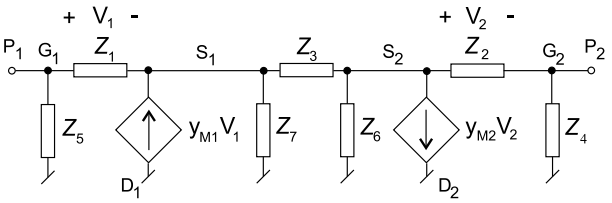

Figure 3: Small signal diagram representing the differential operation of the implemented Q-enhancement circuit [6]. G, D and S indicate the location of Gate, Drain and Source of M_1 and M_2.

where

$$a = \frac{Z_7}{Z_3 + Z_6 + Z_7} \quad (2)$$

$$b = \frac{Z_6}{Z_3 + Z_6 + Z_7} \quad (3)$$

$$c = y_{M1} Z_1 a + y_{M2} Z_2 b \quad (4)$$

Using the transistor representation in Figure 2 on M_1-M_4, the impedances in Eqs. (1-4) are expressed by

$$Z_1 = \frac{1}{j2\pi f C_1} \parallel Z_{\pi M1} \quad (5)$$

$$Z_2 = \frac{1}{j2\pi f C_2} \parallel Z_{\pi M2} \quad (6)$$

$$Z_3 = \frac{1}{j2\pi f C_3} \quad (7)$$

$$Z_4 = Z_{\mu M2} \quad (8)$$

$$Z_5 = Z_{\mu M1} \quad (9)$$

$$Z_6 = Z_{oM2} \parallel Z_{oM4} \parallel Z_{\mu M4} \parallel R_2 \quad (10)$$

$$Z_7 = Z_{oM1} \parallel Z_{oM3} \parallel Z_{\mu M3} \parallel R_1 \quad (11)$$

This allows for estimation of differential impedance from sets of component data without the need for simulations. Further more sweeps of capacitance quickly show the optimal choice for a selected transistor [6].
Figure 4 shows a die photo of the implemented circuit. The differential admittance is measured at the RF pads marked P_1 and P_2. Supply voltage is applied at the pad marked V_{CC} and bias voltage is applied at the pad marked V_{BIAS}. Table 1 lists the sizes of the implemented components.

Table 1: Implemented components.

Components	Size
C_1, C_3	2.7 pF
C_2	2.5 pF
C_4	10 pF
M_1, M_2	0.25,130 μm
M_3, M_4	0.25,410 μm
R_1, R_2,	2.5 kΩ

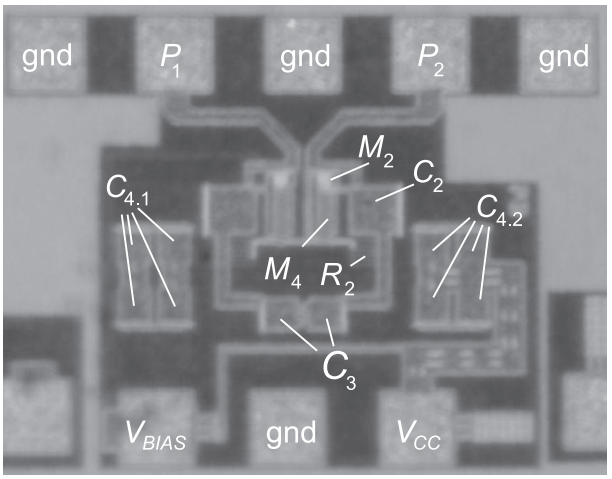

Figure 4: Photo of the implemented die. For symmetry two 1.25 pF capacitors are combined to form C_2, while eight 1.25 pF capacitors placed in two groups are combined to form C_4.

The traces leading from the Q-enhancement circuit to the RF pads have significant parasitics. The parasitics are estimated from process data supplied by the foundary. The resistance of a trace is estimated to 0.5 Ω and the capacitance to the substrate is estimated to 20 fF.

3. Estimates and Simulations

All the components used in the circuit were implemented individually in two port test fixtures and their S-parameters measured on-wafer. Shunt and series parasitics of the test fixtures were de-embedded with a combination of open pad de-embedding and step 1 in the 4 step de-embedding, both described in [7]. Passive components were measured without biasing. The de-embedded S-parameters were converted to admittances for use in the estimates of Z_1-Z_7 in Eqs. (5-11). Table 2 lists these admittances for selected frequencies.

Table 2: Measured admittances [mS].

Component	1 GHz	2 GHz	3 GHz
y_{C1}, y_{C2}	0.2+19i	1.0+40i	2.6+60i
y_{C3}	0.1+17i	0.3+40i	0.9+52i
y_{R1}, y_{R2}	0.4	0.4	0.4

The foundry has provided a design kit for the Advanced Design System (ADS) from Agilent, which is used to simulate both RF and DC operation of the Q-enhancement circuit. Knowledge of the DC voltages at V_1 and V_2 in Figure 1 is necessary to recreate the biasing conditions of the transistors. At some point increasing the trans conductance in the active transistors no longer increases the magnitude of the differential negative admittance [6]. In the implemented

circuit this point appears when the circuit is biased with approximately 0.8 V. Data are presented for zero volt operation and this biasing point. Simulated DC parameters are listed in Table 3. During the RF simulations all passive components were represented with measured and de-embedded S-parameters. Ideal components were used to simulate the parasitics in the traces leading to P_1 and P_2. The simulations indicated that S-parameters were sensitive to how the biasing network loaded M_3 and M_4. The load of both biasing and supply networks were therefore measured and included in the simulations.

Table 3: Included biasing points.

Measurment	V_{CC} [V]	V_{BIAS} [V]	I_{CC} [mA]	V_1,V_2 [V]
a	0	0	0	0
b	2.5	0.8	32	1.27

The transistors were measured with grounded sources i.e. in common source (CS) configuration. M_3 and M_4 are configured like that in the circuit, but all ports on M_1 and M_2 are at DC potentials different than the bulk. This means that the threshold voltage (V_T) may increase and parasitics to bulk may change, even though equivalent voltage drops are applied across the transistor [8]. The parameters in Figure 2 are estimated from CS measurements, but M_1 and M_2 are operated in common drain (CD) configuration. In the CS estimates, the parasitics from gate to bulk are included in Z_π, but in CD configuration they will be included in Z_μ. Further more the estimated Z_o includes parasitics from source to bulk. In CD configuration Z_o includes parasitics from drain to bulk. This means that estimates based on data measured on a transistor in CS configuration will have some error, even if the measurements are perfect.

The biasing points of the transistors were derived from the data in Table 3. Only one set of data is used for each pair of transistors. The transistor used for M_1 and M_2 was supplied with 1.2 V and the gate voltage was adjusted to compensate for the increasing V_T. Table 4 lists transistor parameters for selected frequencies as derived from the measured data.

Table 4: Transistor parameters from measurement b.

Component	1 GHz	2 GHz	3 GHz
$Z_{\pi M1}$, $Z_{\pi M2}$ Ω	19-860i	15-420i	12-290i
$Z_{\mu M1}$, $Z_{\mu M2}$ Ω	-5-2400i	-7-1200i	-5-760i
Z_{oM1}, Z_{oM2} Ω	340-170i	210-200i	140-180i
y_{M1}, y_{M2} [mS]	42-0.9i	42-2.0i	42-3.0i
$Z_{\mu M3}$, $Z_{\mu M4}$ Ω	-10-800i	-6-390i	-3-260i
Z_{oM3}, Z_{oM4} Ω	160-120i	80-100i	60-80i

4. Results

S-parameters were measured and simulated at P_1 and P_2 in Figure 1. Figures 5 and 6 show the magnitudes of the simulated and the measured and de-embedded S-parameters.

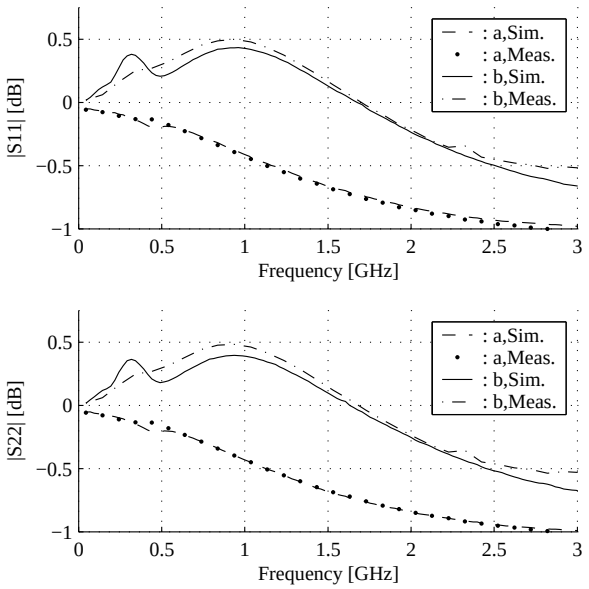

Figure 5: Magnitude of S11 and S22. Meas. and Sim. indicate measured and simulated data respectively.

Generally a good match is seen between measured and simulated S-parameters. This indicates that the design kit models the transistors well. However a deviation, expressed by notches in |S11| and |S22| and a general increase in |S12| and |S21|, appears at 200-500 MHz. The notches in |S11| and |S22| depend on the biasing network.
The differential admittance ($Y_{IN\,d}$) is calculated by converting the S-parameters to Y-parameters, which are used in

$$Y_{IN\,d} = \frac{y_{11}y_{22} - y_{12}y_{21}}{y_{11} + y_{22} + y_{12} + y_{21}} \qquad (12)$$

The measured and simulated differential admittance is compared to estimates from Eqs. (1-11). The differential conductance is shown in Figure 7.
The differential reactance is represented by an equivalent capacitance, calculated for all frequencies. Equivalent capacitance for the simulated, measured and estimated reactance is shown in Figure 8.
A good match is seen between the measured and simulated differential admittance. This indicates that the deviations observed in the S-parameters are common mode phenomena. Errors up to 20 % are seen in the conductance estimated from Eqs. (1-11) and even worse errors are seen in the equivalent capacitance. Some of this error appears because the active transistor was measured in CS configuration

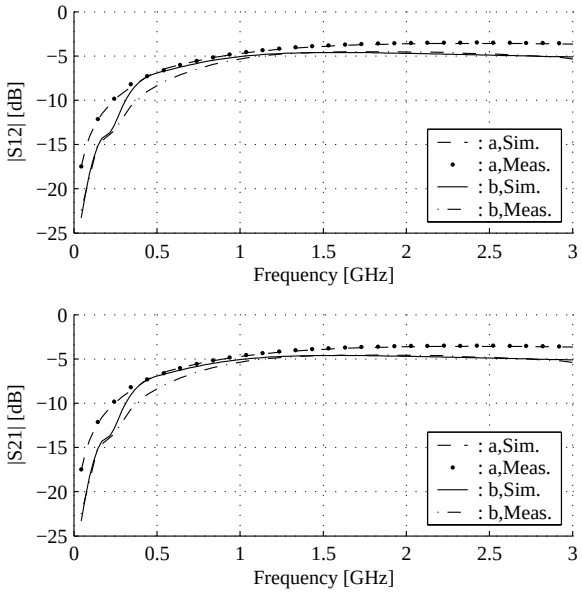

Figure 6: Magnitude of S12 and S21. Meas. and Sim. indicate measured and simulated data respectively.

and used in CD configuration, but lot to lot tolerances and measurement uncertainties are also important contributors.

5. Conclusion

A differential circuit has been designed and implemented in a 0.25 μm CMOS process from UMC. The circuit generates a differential conductance down to -2.8 mS at 2 GHz, which enables it to compensate for approximately 360 Ω of parallel resistance. It also generates a differential reactance equivalent to approximately 1 pF. Measured and simulated results are compared to estimates using a general expression presented in [6]. The expression is found to be usable, and even better results can be expected if the active transistor is measured in common drain configuration. In practice this means that the transistor has be measured in a three port test structure.

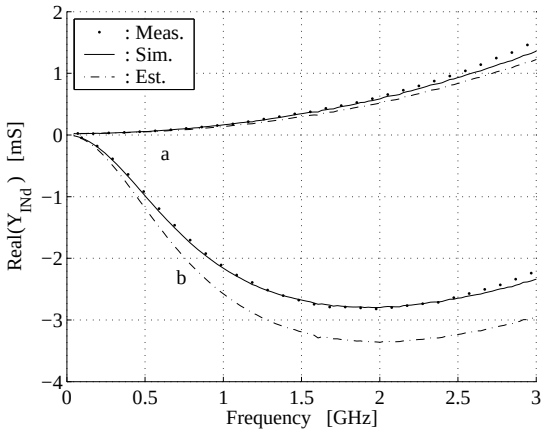

Figure 7: Differential conductance. Lines show simulated results. Dots show measured results and dashed lines show estimates from Eqs. (1-11).

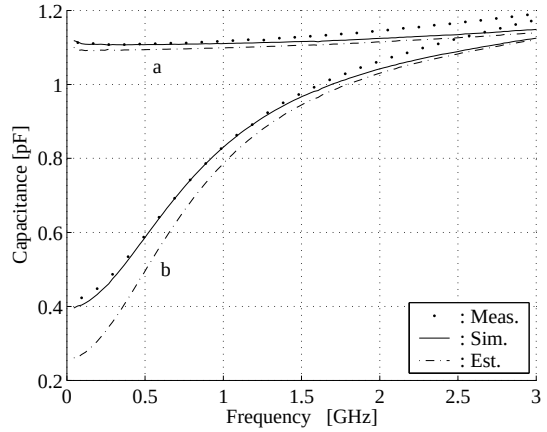

Figure 8: Equivalent differential capacitance. Lines show simulated results. dots show measured results and dashed lines show estimates from Eqs. (1-11).

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An RF CMOS Q-enhanced LC Resonator

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An RF CMOS Q-enhanced LC Resonator

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Abstract

This paper compares simulations and measurement results of a differential Q-enhanced LC tank operating at 1779 - 1870 MHz. Sensitive circuits and in-accurate models provided in-accurate simulations. S-parameters measured on components and sub-circuits were included in the simulations to provide an accuracy of 3 MHz in the estimates of the resonator centre frequency.

1. Introduction

Q-enhancement enables design of high-Q on-chip LC resonators using the low-Q inductors that usually are available in standard CMOS processes. Several implementations of Q-enhanced LC resonators have been reported in the literature [1, 2, 3, 4]. Differential implementations where a negative conductance is created using positive feedback between two transistors are most common [1, 2, 3]. However, solutions where a single transistor is used together with reactive components have also been reported [2, 4]. This paper presents a differential Q-enhanced LC resonator where the negative conductance is generated with a differential circuit that uses both transistors and reactive components. The circuit has been implemented in a 5-metal layer, single poly, 0.25 μm CMOS process.

2. The Q-enhanced Resonator

The resonator is shown in Figure 1. It is a parallel LC tank with tuneable Q factor and centre frequency. The centre frequency is controlled by a switched varactor bank, composed of five varactors. The varactors are implemented as pairs of nFETs (M_1 to M_{10}). All the FETs are 0.25 μm long but their width increases from 10 μm (M_1 and M_2) over 20, 40 and 80 μm to 160 μm (M_9 and M_{10}). The FETs are biased at the gates with 2.5 V and the varactor bank is controlled by DC voltages applied to drain and source of each FET through V_{CAP1} - V_{CAP5}. These voltages are either 0 or 2.5 V and forces each FET into inversion mode or weak accumulation mode respectively. The largest capacitance is obtained in inversion mode. The inductor is a tapped planer spiral device with four windings and symmetry around the tapping point. It is implemented in the two top metal layers and provides bias for both the varactor bank and the Q-enhancement circuit. The bias voltage is applied at the tapping point, where it is decoupled by two nFET capacitors configured in inversion mode (M_{11} and M_{12}). The negative conductance is generated by M_{13}, M_{14}, C_{11}, C_{12} and C_{13}, while M_{15}, M_{16}, R_1, R_2 and C_{14} are used for biasing and stabilisation. Refer to

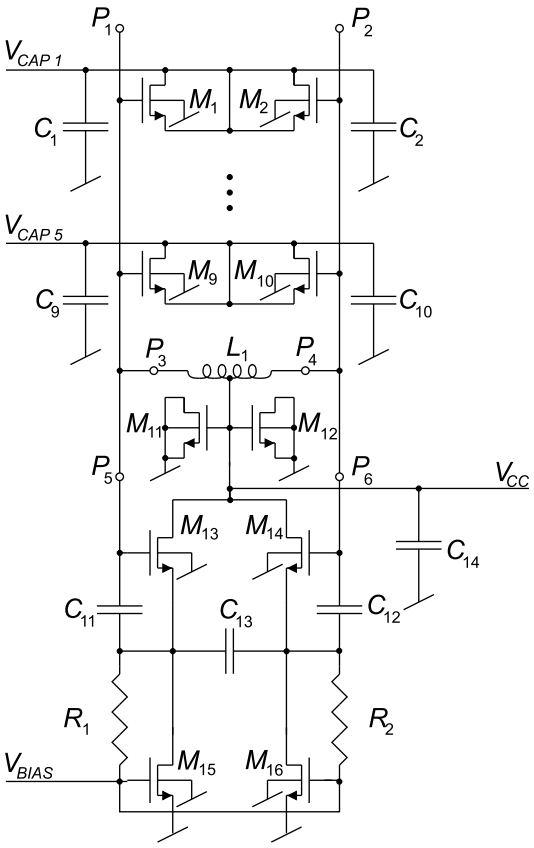

Figure 1: Implemented LC resonator with tuneable centre frequency and Q.

[5, 6] for a detailed description of this circuit. A die photo of the implemented circuit is shown in Figure 2.

3. Varactor Bank

Simulations, where models from the design kit are used in the varactor bank, estimates the upper frequency limit of the resonator significantly higher than measured. The match is quite good at the lower frequency limit. An analysis of a differential varactor build with 320x0.25 μm nFETs indicates that the design kit underestimate the capacitance in weak accumulation mode significantly. While this can explain the observed behaviour, it also implies that measured data need to be used for the varactors to obtain accurate estimates of the frequency from simulations. Unfortunately the varactor bank used in the resonator has not been implemented as a stand-alone structure, and can therefore not be measured. Instead measured data from the 320x0.25 μm

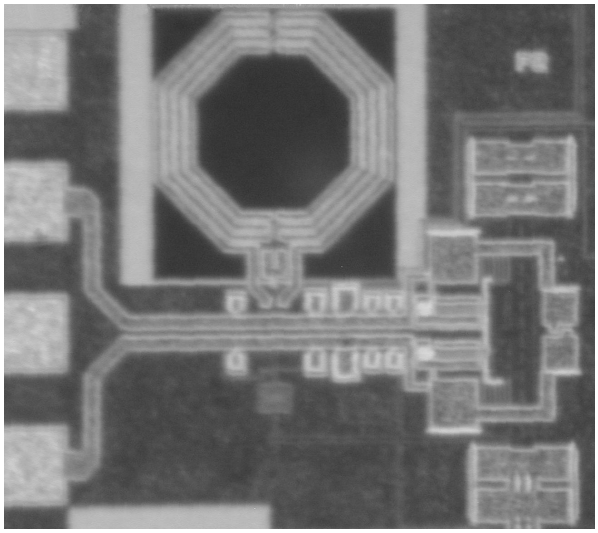

Figure 2: Die photo of the implemented resontor.

varactor is used to provide rough estimates of the varactor bank. The varactors are high-Q devices. This means that the real part of the measured impedance is small compared to the imaginary part. Relative small errors in the measurements may therefore translate to large errors in the estimates of the real part of the impedance. Only measurements on the 320x0.25 μm varactor, where the real part is larger than zero are accepted. The de-embedded and averaged S-parameters from these measurements are used to represent the varactors in the simulations presented in this paper. The varactor bank is divided in two sections. Section 1 includes transistors M_1 to M_8 while section 2 includes transistors M_9 and M_{10}. The differential capacitance of section 1 is estimated to 156 fF in inversion mode and 80 fF in weak accumulation mode. The equivalent capacitances are estimated to 170 and 87 fF for section 2.

4. Inductor

The inductor is an important part of the differential LC tank and in the presented implementation it is also important for the biasing. It is sufficient to know the inductor's 2-port characteristics at P_3 and P_4 for simulation of the resonator's differential impedance. To simulate the effects the supply network might have on the resonator S-parameters a 3-port representation is required. A 3-port may be represented by six impedances as illustrated in Figure 3.

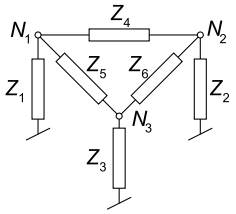

Figure 3: 3-port representation with six impedances.

In the simulations Z_3 is ignored to simplify later estimates of the five remaining impedances. These are estimated from measurements of two test structures; one where the inductor is open, as shown in Figure 4a, and one where the tap is shorted as show in Figure 4b. The equivalent 3-port representations are shown in Figures 4c and d.

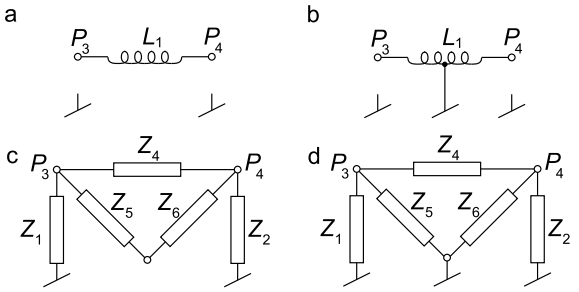

Figure 4: a and b: test structures with open and shorted bias points respecively. c and d: Their respective 3-port equivalents.

Both inductor test structures are implemented on a single lot (lot 1). Four chips were measured and the S-parameters are averaged after de-embedding. The equivalent Y-parameters are calculated and used for estimates of the relevant impedances as shown in Eqs. (1) to (5).

$$z_1 = \frac{1}{y_{11a} + y_{12a}} \quad (1)$$

$$z_2 = \frac{1}{y_{22a} + y_{21a}} \quad (2)$$

$$z_4 = \frac{-2}{y_{21b} + y_{12b}} \quad (3)$$

$$z_5 = \frac{1}{y_{11b} + y_{12b} - y_{11a} - y_{12a}} \quad (4)$$

$$z_6 = \frac{1}{y_{22b} + y_{21b} - y_{22a} - y_{21a}} \quad (5)$$

where the Y-parameters, obtained from the test structures in Figures 4a and 4b, are marked with a and b respectively.
The test structure in Figure 4a is implemented on three different lots including the one with the resonator (lot 3). This may be used to provide an overview of the repeatability of the data from lot 1. Table 1 lists the differential inductance, L, differential conductance, G_l, and the Q factor as measured for inductors from the different lots. The Q is calculated for $f_c = 1825$ MHz using [7]:

$$Q = \frac{1}{2\pi f_c L G_l} \quad (6)$$

Table 1: Measured differential Q, L and G_l for the 3-port inductor.

lot	Q	L [nH]	G_l [mS]
1	7.6	5.7	2.1
2	7.4	5.5	2.1
3	7.6	5.6	2

The values of inductance differ with 0.2 nH while the value of the conductance differ with 0.1 mS.

5. Q-enhancement

The Q-enhancement circuit is simulated and measured in stand-alone configuration with the same biasing conditions

as the resonator. Transistors are simulated using the design kit while resistors and fixed capacitors are represented with de-embedded 2-port S-parameters measured on stand-alone implementations of these components. To verify the Q-enhancement circuit, the die was mounted on a PCB. The supply and control voltages were applied through this PCB to ensured repeatable loads. The Q-enhancement circuit is found to be sensitive to probing. To evaluate the repeatability of the measurements, the circuit is measured a number of times. The test should thus provide very similar sets of S-parameters but instead a variance of up to 1 dB is observed. At 1.825 GHz this translates to a variation of 1.2 mS in the differential conductance and 20 fF in the equivalent capacitance. There is no way of telling if any of the measured sets of S-parameters have errors. An estimate is therefore obtained by averaging the measured and de-embedded sets of S-parameters. The parasitic resistance and capacitance of the traces leading from the circuit to the pad structures are estimated to 1 Ω and 10 fF respectively based on process data. These estimates are subtracted from the measured data to estimate the amount of Q-enhancement delivered to the LC tank. The resulting differential conductance and equivalent capacitance are shown in Figure 5.

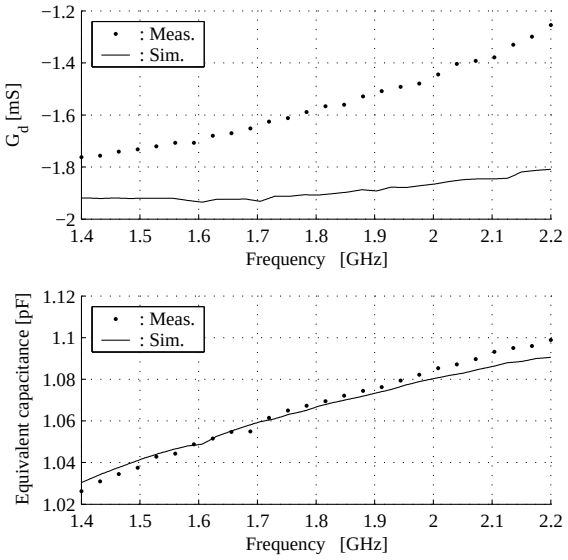

Figure 5: Differential admittance of the Q-enhancement circuit at points P_5 and P_6 in Figure 1. Top: conductance, bottom: Equivalent capacitance. Lines represents simulations while dots represent averaged sets of measured S-parameters.

At 1.825 GHz a differences of approx. 0.3 mS is seen in the differential conductance, while a difference of 7 fF is seen for the differential equivalent capacitance. The simulated values do thus not match the averaged measured data but are within the range of uncertainty due to probing.

6. Resonator Circuit

The setup used to simulate the Q-enhancement circuit is expanded to include M_{11}, M_{12}, the 3-port representation of the inductor and measurements of the varactors. Furthermore, the simulations include the impedance, mutual and ground capacitance of the traces estimated to 1.3 Ω, 9 fF and 53 fF respectively and 1-port S-parameter measurements of the supply trace on the PCB. Like the Q-enhancement circuit the resonator was measured on a die mounted on a PCB and the measurements were repeated several times. The data used in the following are obtained with varactor section 1 in weak accumulation mode and varactor section 2 in inversion mode. The resonator thus operates on a mid range centre frequency. The resonator was supplied with 2.5 V, V_{BIAS} was 0.58 V and it consumed 6.9 mA. The magnitude of the S-parameters are shown in Figures 6 and 7. A notch is seen in the magnitudes of S11 and S22 at approx. 1.7 GHz. The simulated frequency of this notch differs from the measured frequency. The frequency of the notch is found to be repeatable over a number of measurements. The differences therefore express true in-accuracies in the simulations.

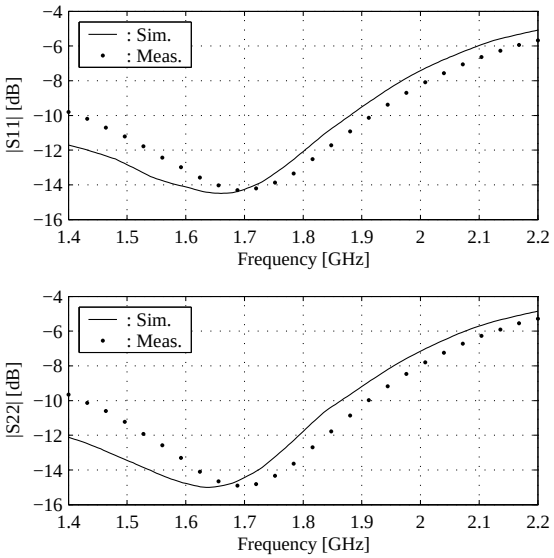

Figure 6: Magnitude of S11 and S22 of the resonator circuit. Lines represent simulated results. Dots represent averages over several sets of measured S-parameters.

The differential input admittance between P_1 and P_2 is calculated from both the simulated and measured S-parameters and compared in Figure 8. The error on the differential conductance is up to 0.1 mS. The differential conductance calculated from the sets of measured S-parameters only vary 0.002 mS. The error can therefore not be explained as probing uncertainties. The conductance simulated on the resonator matches the sum of the conductance simulated on the Q-enhancement circuit and the conductance measurements of the inductors on lot 1. The conductance measured on the resonator is approx. 0.2 mS smaller than what can be expected from the measurements of the Q-enhancement circuit and the inductor on lot 3. The admittance, $Y(j2\pi f)$, at the frequency f is expressed by [7]:

$$Y(j2\pi f) = G_t \left(1 + jQ\left(\frac{f}{f_c} - \frac{f_c}{f}\right)\right) \qquad (7)$$

,- where f_c is the centre frequency and G_t is the conductance. The reactance of the parallel resonator is thus zero at

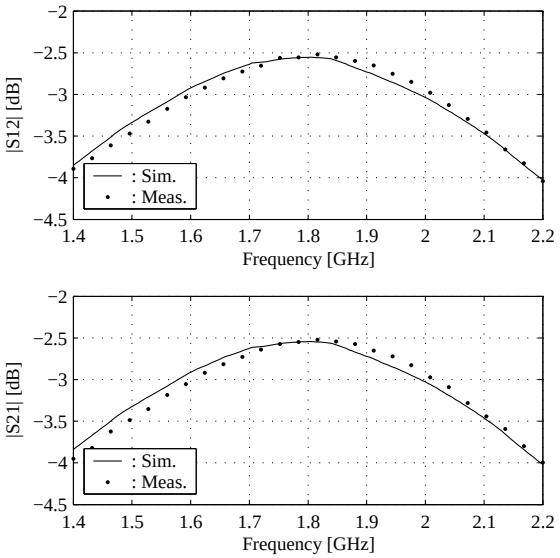

Figure 7: Magnitude of S12 and S12 of the resonator circuit. Lines represent simulated results. Dots represents averages over several sets of measured S-parameters.

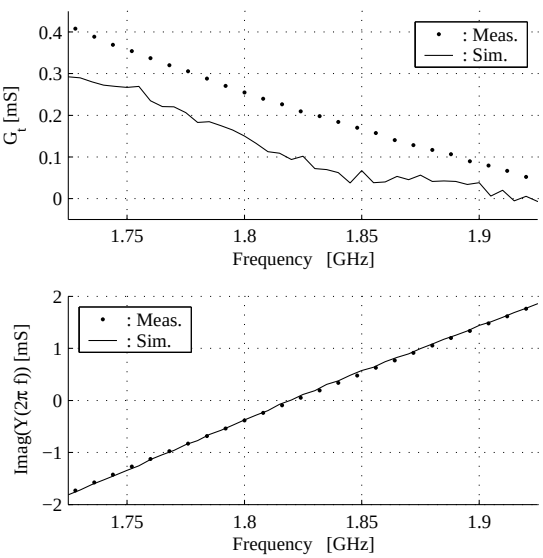

Figure 8: Differential admittance of the resonator. Top: Conductance, bottom: reactance. Lines are simulations and Dots averaged of several sets of measured S-parameters.

the centre frequency. The Q factor can be estimated form Eq. (6) if G_l is replaced by G_t. Table 2 lists simulated and measured corner and mid values for f_c together with estimated Q factors. The simulated Q factor is based on the inductance measured on lot 1 while the measured Q factor is based on the inductance measured on lot 3.

Table 2: Simulated (sim.) and measured (meas.) corner and mid values for f_c and resulting Q factor.

$f_c$sim.$[MHz]$	$Q_{\text{sim.}}$	$f_c$meas.$[MHz]$	Qmeas.
1776	87	1779	53
1825	153	1822	78
1872	298	1870	122

It is seen that the simulation estimates f_c within 3 MHz of the measurements. G_t is the main contributor to the differences in Q factor.

7. Conclusion

This paper compares simulation and measurements of a differential Q-enhanced LC tank, operating at 1779 - 1870 MHz. Data measured on capacitors, inductors, resistors and varactors are used in the simulation. Most of these components were measured in test structures implemented on other lots than the reference circuit. Even though this approach is sensitive to measurement errors and process tolerances, the centre frequency is estimated within 3 MHz. Less accuracy might be acceptable for most applications but for the high-Q resonator, less accuracy means that the tuning range has to be increased to compensate for the resulting larger uncertainties in the centre frequency.

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