Compensation of Laser Frequency Fluctuations and Phase Noise in 16-QAM Coherent Receivers

Pablo Gianni, Graciela Corral-Briones, Carmen Rodríguez, and Mario R. Hueda

***Abstract*— Frequency fluctuations caused by mechanical vibrations, power supply noise, and other mechanisms are detrimental to the phase estimator performance in high speed intradyne coherent optical receivers. In this letter, we propose the use of a low-latency parallel digital phase lock loop in combination with common feed-forward carrier phase recovery algorithms in order to compensate both the phase noise and laser frequency fluctuation effects on 16-quadrature amplitude modulation receivers. Numerical results demonstrate the excellent behavior of the proposed two-stage carrier recovery scheme.**

***Index Terms*— Carrier phase estimation, coherent systems, laser, local oscillator, parallel, vibration.**

I. Introduction

THE PROJECTED increase on the bandwidth demand (e.g., ≥100 Gb/s) has set the bases for the next generation of optical transport networks (OTN) and it has, therefore, renewed interest on coherent detection and spectrally efficient modulation techniques such as *M-ary* phase shift keying (*M*-PSK) and *M-ary* quadrature amplitude modulation (*M*-QAM) [1]. More precisely, the conjunction among intradyne coherent detection, polarization-division multiplexing (PDM) 16-QAM and electronic dispersion compensation (EDC) [2], [3] allows to reach a good tradeoff among complexity, spectral efficiency, minimization of nonlinear distortions and the possibility to completely compensate with zero penalty the main fiber channel impairments [2] (i.e., polarization mode dispersion (PMD) and chromatic dispersion (CD)). In other words, all of these aspects can be summarized in an improved receiver sensitivity in comparison to intensity modulation direct detection (IM/DD) schemes [4].

It has been recently shown that laser frequency instability caused by mechanical vibrations significantly degrades the performance of feedforward carrier phase recovery (CPR) algorithms [5]. Other effects such as power supply noise may also introduce laser frequency fluctuations which can be modeled as a frequency modulation with a sinusoid of large amplitude (e.g., ∼500 MHz) and low frequency (e.g., ≤ 35 KHz).

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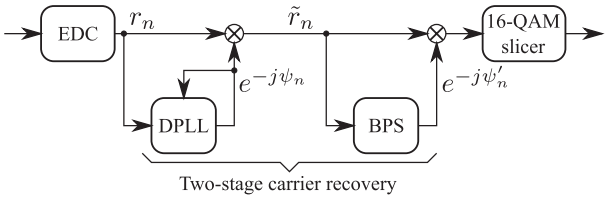

Fig. 1. Simplified block diagram of the coherent receiver with electronic dispersion compensation (EDC).

On the other hand, the high data and symbol rate requirements mandate the use of parallel processing techniques for the implementation of the receiver. Previous works have shown that a two-stage carrier recovery parallel architecture based on a low-latency parallel digital phase lock loop (DPLL) and the feedforward Viterbi–Viterbi (VV) CPR algorithm [6]–[8] offers an excellent tradeoff between complexity and performance for coherent receivers in the presence of laser phase noise, sinusoidal frequency jitter, and frequency offset.

In this letter we extend the previously introduced parallel carrier recovery algorithm [7] to the 16-QAM modulation scheme. Computer simulations will show the excellent behavior of the proposed two-stage carrier recovery scheme.

II. System Model

Fig. 1 shows a simplified block diagram of the 16-QAM coherent receiver considered in this letter. A first CPR stage is based on a low-latency parallel DPLL, which is used to compensate not only frequency offset but also frequency fluctuations. The second CPR stage is based on the well-known *blind phase search* (BPS) [9] algorithm, which operates on the signal demodulated by the DPLL. The second CPR stage is mainly used to compensate the laser phase noise.

The sample at the EDC output can be expressed as

$$r_n = a_n e^{j\alpha_n} + z_n \tag{1}$$

where a_n is the n^{th} transmitted 16-QAM symbol and α_n is the total phase noise. Component z_n represents the amplified spontaneous emission (ASE) noise sample, which is modeled as a white complex Gaussian random variable with power σ^2 [2]. The EDC output signal (1) can be rewritten as

$$r_n = |r_n| e^{j\theta_n} \tag{2}$$

where $|r_n|$ and θ_n are the magnitude and the phase of the complex sample r_n, respectively. The received phase θ_n can

be expressed as

$$\theta_n = \zeta_n + \Omega_c n + \Delta\Omega_n + \phi_n \tag{3}$$

where ζ_n is the phase of the transmitted symbol differentially encoded in quadrant, Ω_c is the angular carrier frequency offset given by $\Omega_c = 2\pi T f_c$, with f_c and T being the carrier frequency offset and the symbol duration, respectively. The term $\Delta\Omega_n$ represents the phase change generated by frequency fluctuations. We assume that the carrier is modulated by a sinusoidal interfering signal, as follows:

$$\Delta\Omega_n = \frac{A_p}{\Delta f_c}\sin(2\pi T \Delta f_c n) \tag{4}$$

where A_p and Δf_c are the amplitude and frequency of the modulation tone. Component $\phi_n = \phi_n^{(\text{laser})} + \phi_n^{(\text{ASE})}$ is the total phase noise given by the laser phase noise modeled as a Wiener process and the ASE generated phase noise, respectively.

III. New Parallel DPLL for 16-QAM

As mentioned before, the proposed two-stage carrier recovery algorithm is based on a DPLL followed by a traditional feedforward CPR. Parallel architectures for both stages must be provided for multigigabit applications. Feedforward phase estimation schemes such as VV or BPS are attractive to high-speed coherent receivers owing to their good laser linewidth tolerance and feasibility for parallel implementation. However, the low latency parallel DPLL proposed in [7] has been designed for QPSK. In the following subsection, we extend the scheme introduced in [7] for application to 16-QAM.

A. DPLL for 16-QAM

In a carrier recovery loop, the symbol information must be removed to compute the phase error signal. In QPSK systems, this operation can be easily carried out in the phase domain by using $\tilde{\phi}_n = (\theta_n)_{\frac{\pi}{2}}$, where $(.)_M$ denotes modulus M. In the absence of phase noise and frequency deviations (i.e., $\phi_n = 0\ \forall n$ and $f_c = \Delta f_c = 0$), notice that $\tilde{\phi}_n = (\zeta_n)_{\frac{\pi}{2}} = \pi/4\ \forall n$. A similar approach can be adopted for 16-QAM. In this case, note that the symbol phase ζ_n reduced to the first quadrant results in $(\zeta_n)_{\frac{\pi}{2}} \in \{atan(1/3), \pi/4, atan(3)\}$ (see Fig. 2).

Without loss of generality, we focus on a first-order DPLL as shown in Fig. 3. The phase at the numerically controlled oscillator (NCO) output can be expressed as

$$\psi_n = \psi_{n-1} + K_p \epsilon_n \tag{5}$$

where K_p and ϵ_n are the proportional gain and the phase error, respectively. The phase error is given by

$$\epsilon_n = \left(\tilde{\phi}_n - \psi_{n-1}\right)_{\frac{\pi}{2}} - \rho_n \tag{6}$$

where ρ_n is the symbol phase of the transmitted symbol reduced to the first quadrant, i.e., $\rho_n = (\zeta_n)_{\frac{\pi}{2}}$. Since the phase symbol is not known apriori at the receiver, and according to the technique proposed in [10], we use (see Fig. 2):

$$\rho_n \approx f(|r_n|, \tilde{\theta}_n) \tag{7}$$

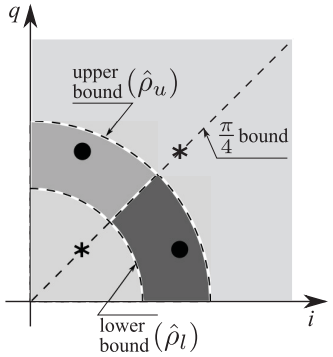

Fig. 2. 16-QAM constellation after modulus $\pi/2$ operation.

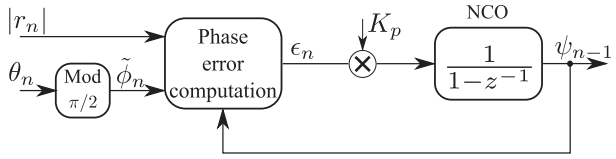

Fig. 3. Simplified block diagram of a phase domain DPLL for 16-QAM.

where

$$f(|r_n|, \tilde{\theta}_n) = \begin{cases} \pi/4 \text{ if } |r_n| \geq \hat{\rho}_u \text{ or } |r_n| \leq \hat{\rho}_l \\ \alpha_0 \quad \text{if } \hat{\rho}_l < |r_n| < \hat{\rho}_u \text{ and } \tilde{\theta}_n \leq \frac{\pi}{4} \\ \alpha_1 \quad \text{if } \hat{\rho}_l < |r_n| < \hat{\rho}_u \text{ and } \tilde{\theta}_n > \frac{\pi}{4} \end{cases} \tag{8}$$

with $\alpha_0 = a\tan(1/3)$, $\alpha_1 = a\tan(3)$, while

$$\tilde{\theta}_n = (\theta_n - \psi_{n-1})_{\frac{\pi}{2}} = \left(\tilde{\phi}_n - \psi_{n-1}\right)_{\frac{\pi}{2}} \tag{9}$$

is the phase of the demodulated received sample reduced to the first quadrant (note that $(a+b)_M = ((a)_M + (b)_M)_M$, therefore since $\tilde{\phi}_n = (\theta_n)_{\pi/2}$ we can get (9)).

B. Parallel Low Latency 16-QAM DPLL

Let P be the parallelization factor. Based on the technique described in [7], from (5) and (8) it is possible to derive a low latency parallel architecture for 16-QAM DPLL. The output of the m^{th} branch can be evaluated as

$$\psi_{n+m} \approx \psi_{n-1} + K_p \sum_{k=0}^{m} \hat{\theta}_{n+k} - K_p \sum_{k=0}^{m} f(|r_{n+k}|, \hat{\theta}_{n+k}) \tag{10}$$

where $m = 0, 1, \ldots, P-1$, and

$$\hat{\theta}_{n+k} = \left(\tilde{\phi}_{n+k} - \psi_{n-1}\right)_{\frac{\pi}{2}}. \tag{11}$$

Unfortunately, eq. (10) is still too difficult to be implemented with digital signal processors in one clock cycle for the state of the art 28 nm CMOS technology as a result of the complexity required to carry out the computation of the function $f(|r_{n+k}|, \hat{\theta}_{n+k})$ and then the last summation in (10). This problem can be mitigated if terms $f(|r_{n+k}|, \hat{\theta}_{n+k})$ are pre-computed by using the NCO output of the previous clock cycle, that is,

$$\hat{\theta}_{n+k} \approx \left(\tilde{\phi}_{n+k} - \psi_{n-1-P}\right)_{\frac{\pi}{2}}. \tag{12}$$

Based on this approximation, note that fast adders (e.g., Wallace tree and carry save adder [7]) are required to quickly

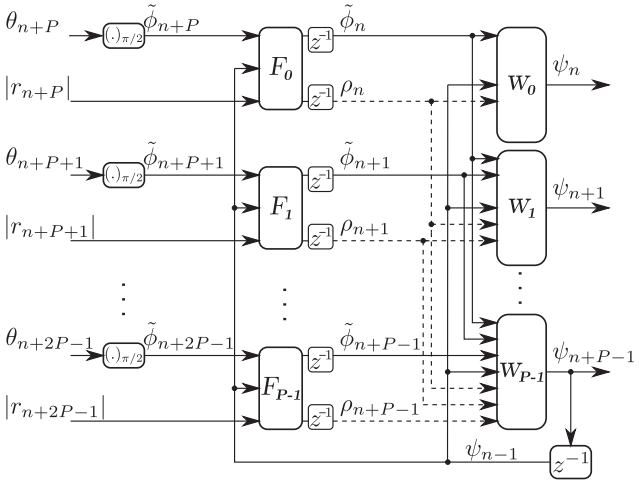

Fig. 4. Block diagram of the parallel type I phase domain DPLL for 16-QAM.

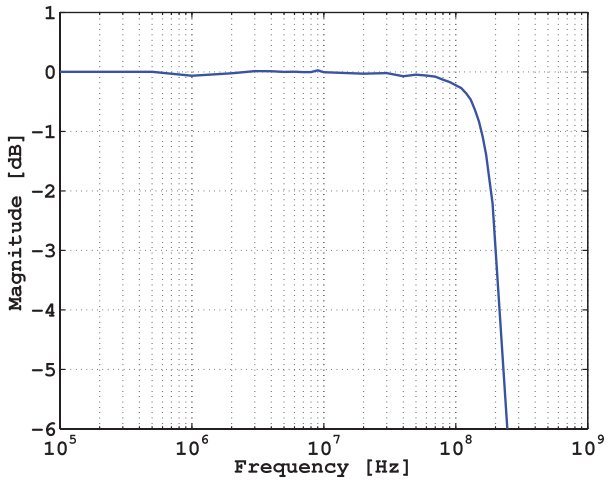

Fig. 5. Frequency response of the proposed parallel DPLL with $f_{clock} = 400$ MHz, $P = 80$, $L_w = 1$, and $K_p = 2^{-6}$.

calculate the NCO output (10). As we shall show later, the performance degradation caused by (12) is negligible in practical situations (e.g., $P \leq 80$). This behavior can be understood from the facts that 1) only the non-diagonal symbols use $\hat{\theta}_{n+k}$ (see (8) and symbols with circles in Fig. 2), and 2) laser frequency fluctuations are slow compared to the baud rate.

A parallel implementation of the proportional loop can be derived from (10) and (12) as shown in Fig. 4. Block "F_k" ($k = 0, 1, \ldots, P-1$) computes $\hat{\theta}_{n+k}$ given by (12) and then $f(|r_{n+k}|, \hat{\theta}_{n+k})$, while block "$W_k$" evaluates (10). The proportional gain is assumed to be a power of 2 (e.g., $K_p = 2^{-N_K}$ with N_K being a positive integer). In this way, multiplications are reduced to simple bit shift operation. Note that all additions in (10) are modulus 2π. Finally, we realize that the procedure described here can be easily adopted to implement a parallel type II second-order DPLL as described in [7].

C. Implementation of the DPLL

The clock frequency in a dual-polarization (DP) QPSK/QAM DSP-based receiver is $f_{\text{clock}} = \frac{1}{PT}$, where $1/T$ is the baud rate per polarization. Let L_w be the number of clock cycles of frequency f_{clock} required by blocks "W_k" to compute all the operations defined by (10). Factor L_w must be kept as low as possible (i.e., $L_w = 1$) in order to reduce the performance degradation caused by the loop latency. Blocks "W_k" have been implemented with $L_w = 1$ in a 50 Gb/s, DP-QPSK transceiver (i.e., $1/T = 12.5$ Gs/s) by using 40 nm CMOS technology with $f_{\text{clock}} = 781$ MHz (i.e., $P = 16$) [8].

Here we consider an application specific integrated circuit (ASIC) implementation of the proposed DPLL in a 256 Gb/s DP-16-QAM receiver (i.e., $1/T = 32$ Gs/s). As we will show in Section IV, a parallelization factor of $P = 80$ provides a good tradeoff between complexity and performance. In this context, the clock frequency is $f_{\text{clock}} = \frac{1}{PT} = 400$ MHz. The frequency response of the parallel DPLL with $P = 80$, $L_w = 1$, and $K_p = 2^{-6}$ is depicted in Fig. 5.

Fig. 6 shows an implementation architecture for the most critical NCO branch, $P - 1$. We multiply both members of (10) by K_p^{-1}, thus,

$$K_p^{-1}\psi_{n+P-1} \approx K_p^{-1}\psi_{n-1} + \sum_{k=0}^{P-1}\left(\tilde{\phi}_{n+k} - \psi_{n-1}\right)_{\frac{\pi}{2}} + \overline{\boldsymbol{\rho}}_{P-1} \tag{13}$$

where $\overline{\boldsymbol{\rho}}_{P-1}$ is the two's complement of $\boldsymbol{\rho}_{P-1}$ defined by

$$\boldsymbol{\rho}_{P-1} = \sum_{k=0}^{P-1}\rho_{n+k} = \sum_{k=0}^{P-1} f(|r_{n+k}|, \hat{\theta}_{n+k}), \tag{14}$$

with $\hat{\theta}_{n+k}$ given by (12). Since ψ_n is modulus 2π, from (10) note that all the additions in (13) are modulus $2\pi K_p^{-1}$.

Let N_ψ be the number of bits used to represent the phases ψ_n and θ_n with $\psi_n, \theta_n \in [0, 2\pi)$[1]. Taking into account that 1) $K_p = 2^{-N_K}$ and 2) the additions in (13) and (14) are modulus $2\pi K_p^{-1}$, notice that $N_\psi + N_K$ bits are required to represent $K_p^{-1}\psi_{n+P-1}$ in (13)[2].

On the other hand, it is simple to verify that $\tilde{\phi}_n = (\theta_n)_{\frac{\pi}{2}}$ and $(\psi_n)_{\frac{\pi}{2}}$ can be easily obtained by keeping only the $N_\psi - 2$ least significant bits (LSBs) of θ_n and ψ_n, respectively. Therefore,

$$\left(\tilde{\phi}_{n+k} - \psi_{n-1}\right)_{\frac{\pi}{2}} = \tilde{\phi}_{n+k} \oplus \left(\overline{\psi}_{n-1}\right)_{\frac{\pi}{2}}, \tag{15}$$

$$\hat{\theta}_{n+P+k} = \tilde{\phi}_{n+P+k} \oplus \left(\overline{\psi}_{n-1}\right)_{\frac{\pi}{2}}, \tag{16}$$

where $\overline{\psi}_{n-1}$ and $\oplus$ denote, respectively, the two's complement of ψ_{n-1} and the overflow adder operation. We want to highlight that $N_\psi - 2$ bits are required to represent not only $\tilde{\phi}_{n+k}$ but also $\left(\overline{\psi}_{n-1}\right)_{\frac{\pi}{2}}$, $\tilde{\phi}_{n+k} \oplus \left(\overline{\psi}_{n-1}\right)_{\frac{\pi}{2}}$, and $\hat{\theta}_{n+P+k}$. Each block "F_k" computes (16) and then $f(|r_{n+P+k}|, \hat{\theta}_{n+P+k})$ given by (8). The latter can be easily implemented with two comparators, an *AND* gate, and a simple look-up table (details are omitted here due to space limitation). Samples $|r_{n+k}|$ are represented by N_r bits.

[1]For example, 5-bit resolution has been suggested in [9] to represent angles in the range $[0, \frac{\pi}{2})$ with 16-QAM. Hence $N_\psi = 7$ for the range $[0, 2\pi)$.

[2]Note also that the carry generated in the two's complement operation of $\boldsymbol{\rho}_{P-1}$ is not needed to evaluate (13). Therefore, only the $N_\psi + N_K$ least significant bits of $\overline{\boldsymbol{\rho}}_{P-1}$ are used in (13).

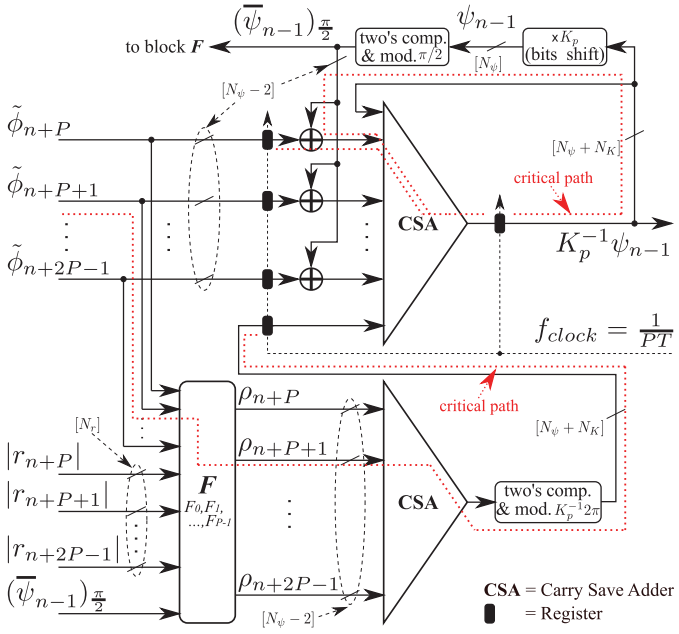

Fig. 6. Hardware implementation architecture of the NCO branch $P-1$. Terms "[.]" indicate number of bits.

The implementation architecture shown in Fig. 6 with $P = 80$, $f_{\text{clock}} = 400$ MHz, $N_\psi = 7$ bits, $N_r = 11$ bits, and $K_p = 2^{-6}$ (i.e., $N_K = 6$) has been successfully synthesized (i.e., no timing issues) by using 28 nm CMOS technology with standard voltage threshold (SVT) transistors. Therefore, the feasibility to implement the proposed DPLL with $L_w = 1$ in 256 Gb/s DP-16-QAM receivers with current CMOS technology is demonstrated.

IV. Numerical Results

Next, we investigate the performance of the proposed two-stage CPR in the presence of laser phase noise and frequency fluctuations. We consider a baud rate per polarization of $1/T = 32$ Gs/s, a type II second-order DPLL, and a BPS algorithm with filter length $M = 21$ and $B = 32$ test phase values (see [9] for more details). The loop parameters (i.e., the proportional and integral gains) are adjusted to maximize the loop bandwidth with a maximum peaking of 0.5 dB. The loop latency of all blocks "W_k" is $L_w = 1$.

Fig. 7(a) shows the optical signal-to-noise ratio (OSNR) penalty versus the frequency modulation tone amplitude, A_p. This figure considers the serial DPLL (S-DPLL) and the modified low latency parallel DPLL (P-DPLL) combined with BPS CPR for several values of the parallelization factor P. It is interesting to highlight the important degradation caused by the frequency fluctuations in the solution solely based on the BPS algorithm. In contrast, the two-stage architecture DPLL+BPS performs close to zero penalty along the considered range.

The tolerance to the laser phase noise in the presence of a modulation frequency tone with $A_p = 140$ MHz and $\Delta f_c = 35$ kHz, is analyzed in Fig. 7(b). As it can be observed, the modified P-DPLL+BPS architecture performs close to the ideal S-DPLL+BPS configuration for a wide range of $\Delta\nu T$, even for higher parallelization factor values.

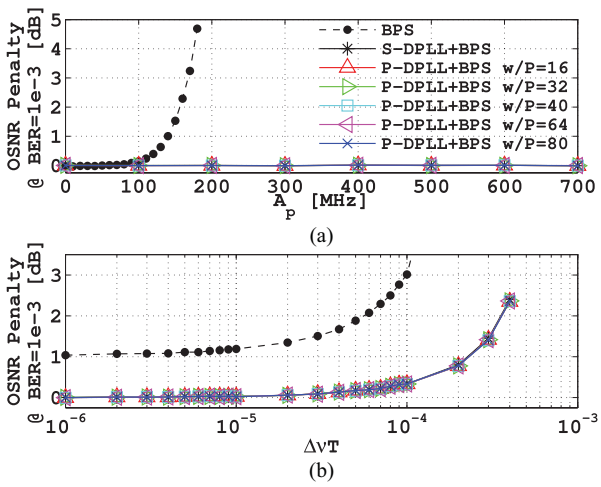

Fig. 7. (a) Effects of the parallelization factor on the performance of the new P-DPLL + BPS in the presence of frequency fluctuations for $\Delta f_c = 35$ kHz and $\Delta\nu = 250$ kHz. (b) Laser linewidth tolerance of the P-DPLL + BPS in the presence of vibration-induced frequency fluctuations for $\Delta f_c = 35$ kHz and $A_p = 140$ MHz. In all the cases, $1/T$ = 32Gs/s, $M = 21$, and $B = 32$.

V. Conclusion

The proposed two-stage carrier recovery architecture based on a low-latency parallel DPLL and a feedforward phase estimator BPS, offers a low complexity, high performance, integral solution to the frequency and phase compensation in coherent optical systems. This solution outperforms previously proposed architectures when *all* optical channel impairments present in real applications, including laser phase noise, sinusoidal frequency jitter, and frequency offset, are accounted for in the modeling.

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