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Experimental demonstration of a noise-tunable delay line with applications to phase synchronization

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ABSTRACT

In this paper we propose and demonstrate a discrete circuit capable of generating arbitrary time delays dependent on noise, either added externally or already present in the signal of interest due to a finite signal-to-noise ratio. We then go on to demonstrate an application to phase locking of signals by means of a standard Phase-Locked Loop (PLL) design, where the usual Voltage-Controlled Oscillator (VCO) is replaced by the noise-tunable delay line.

1. Introduction

Recent works have been exploring various schemes to transmit [1–3], store [4–6], and process information [7,8] that either are able to perform their intended function only in the presence of noise, or can operate in robust fashion in disadvantageous noisy conditions. The general context lies on limitations foreseen given the exponential growth, first noticed by Moore [9], of the density of components in ICs that process and store information. These growing densities come at the expense of having to cope with higher levels of heat dissipation, and thus enhanced thermal noise [10]. In turn, by lowering the amplitude of the signals of interest, heat dissipation can be circumvented at the expense of having to deal with a scenario of degraded signal-to-noise ratios. As such, Stochastic Resonance (SR) comes to mind. SR can be succinctly characterized as a phenomenon in a nonlinear system where noise helps, an otherwise weak signal, to induce transitions between states of stable equilibrium. It was first introduced in the context of climate dynamics to explain the almost periodic occurrence of ice ages [11], and has since been reported in a large number of areas. For a general review of the rich area of stochastic resonance we refer the reader to Ref. [12].

Tunable delay lines, *i.e.*, elements that can equalize information arrival times and, as such, be used as arbitrary phase filters, pervade applications in very many areas of signal processing. In the context of noise-aided circuit elements, refs. [13,14] showed, in theoretical fashion, that a chain of bistable oscillators can act as a noise-tunable delay line. However, as far as we know, there has not been an experimental demonstration up to now.

In this paper we propose and demonstrate a discrete circuit capable of generating arbitrary time delays dependent on noise.

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2. Experimental setup and results

In Fig. 1 we show the proposed scheme for the implementation of a noise-tunable delay line. It is based on a *shift register* circuit, specifically a sixteen-register IC. This IC comprises a chain of sixteen in-series flip-flops that take an input logical state that is copied onto the next flip-flop each time a clock signal is applied, thus generating a delay given by the traverse time, which in turn is controlled by the clock frequency. The basic idea consists of feeding the clock input of the shift register with a stochastic signal. We generate this signal by driving a Schmitt trigger (ST), *i.e.*, a bistable comparator, with a sub-threshold drive signal, incapable by itself of making the ST switch its output state. However, if the sub-threshold signal is contaminated with noise, there is a non-zero probability that the driving signal will make the ST change its output. Indeed, noise-aided synchronization of input and output of the ST in the sub-threshold regime were thoroughly studied in Ref. [15] and it can be considered as an example of stochastic resonance in Schmitt triggers, first studied in experimental fashion in Ref. [16]. The output of the ST is then fed into the clock input of the shift register.

In Fig. 2 we show results for the measured delay as a function of the noise amplitude of the clocking signal. The deterministic sub-threshold signal had an amplitude of 200 mV, mean value of 400 mV and frequency f_{clk} = 1 kHz. This signal drove an ST with upper and lower thresholds set at 0 and 800 mV, respectively. As in Ref. [15], three different regimes of operation can be readily observed, depending on the signal-to-noise ratio (SNR) of the stochastic clocking signal. For a large SNR, the sub-threshold signal does not bear enough amplitude to trigger the shift register IC, thus producing an infinite delay, *i.e.*, the output of the shift register IC remains fixed at one of the two possible logical states. As the signal-to-noise ratio decreases, random sparks act as clocking signals, thus yielding a measurable time delay for the traversing data signal. For an optimal noise amplitude, the stochastic clocking signal behaves as its deterministic underlying sub-threshold signal, and thus the shift register yields a delay given by $16/f_{clk}$, *i.e.*, the number of registers times the clock period. However, past this point, the clocking signal starts to be dominated by noise and, as such, clocking occurs in a random fashion ultimately depending on the noise correlation time, always yielding shorter delays as compared to the supra-threshold deterministic case. It is noteworthy that jitter, represented as error bars in Fig. 2, is much smaller than the mean delay even for large noise amplitudes. This fact will be the basis of the Noise-controlled Phase-Locked Loop (NPLL) put forth in the following section.

Experimental results on the dependence of the delay as a function of the noise bandwidth (proportional to the inverse of the correlation time) are shown in Fig. 3. Noise correlation time is controlled by low-passing large-bandwidth Gaussian noise. We confirm that decreasing correlation times, *i.e.*, uncorrelated noise, leads to ever decreasing delays as expected from Rice rate formula [10,17]. As delay is proportional to the mean time of crossing the clock threshold, we fit our results with the Rice formula and found a very good agreement between experiment and theory. Note, however, that the delay does not tend to zero. The reason is that the various electronic components in the setup act as low-pass filters due to their finite slew rates. In the next section we shall discuss an application of the noise-tunable delay line to the phase locking of signals.

3. Noise-controlled Phase-Locked Loop

Phase-Locked Loops (PLLs) are widely used for the synchronization, detection, and measurement of data signals [18]. Basically, a PLL consists of a Phase Detector (PD), a Low-Pass Filter (LPF), and a Voltage-Controlled Oscillator (VCO). An incoming periodic signal with amplitude A_{sig} and frequency f_{sig} mixes in the PD with a harmonic reference signal of (controllable) amplitude A_{ref} and frequency f_{ref}, producing components at $f_{sig}+f_{ref}$ and $f_{sig}-f_{ref}$, with amplitudes proportional to $A_{sig}\,A_{ref}\,\cos(\phi_{sig}-\phi_{ref})$. The high-frequency components can then be removed by the low-pass filter, and its output used to drive a VCO. The loop is closed by feeding back the VCO output (control signal) that is used to adjust the phase of the reference signal, in such a way to maximize the output of the PD. When this condition is met, the signal of interest becomes synchronized with the reference signal.

In this work, we replace the VCO with the noise-tunable delay line, introduced in the previous section, working in the low-SNR regime. A diagram of this configuration is shown in Fig. 4. For this particular experiment, a sub-threshold square signal (±700 mV, 10 kHz) mixed with noise (of variable amplitude) drove an ST (±1 V, upper and lower thresholds, respectively). The ST output served as clocking signal for a 128-bit shift-register IC. The shift register was fed with a reference signal (5 V, 20 Hz and 20% duty cycle) and its output was mixed with the signal of interest (an arbitrarily delayed copy of the reference) in a PD and low-pass filtered. The ensuing control signal was fed back to the amplifier that set the noise amplitude. Phase detection, low-pass filtering and gain control, $G(V_{ctrl})$, were performed by a computer via a data acquisition board. However, all these steps can be implemented with discrete electronic devices [19]. In Fig. 5 we show the evolution of the

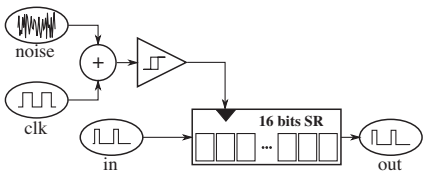

Fig. 1. Noise-tunable delay line.

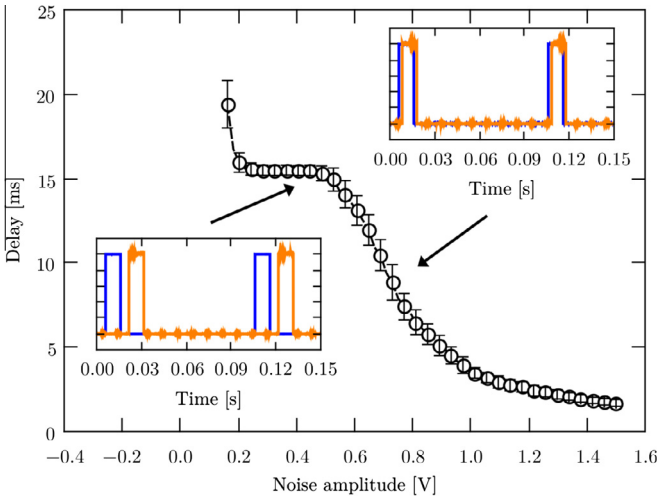

Fig. 2. Delay as a function of rms noise amplitude. Inset: input (blue) and delayed (orange) signal for different noise amplitudes. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

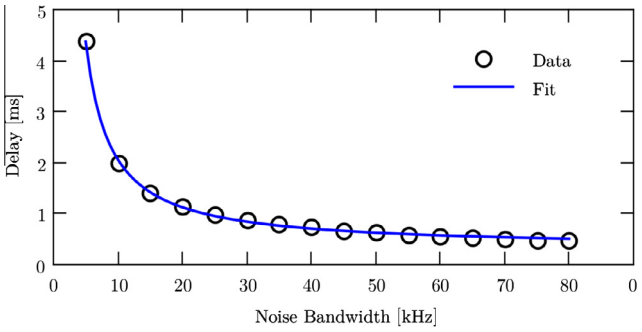

Fig. 3. Delay as a function of noise bandwidth. Experiment (circles) and theory (solid line) show a very good agreement.

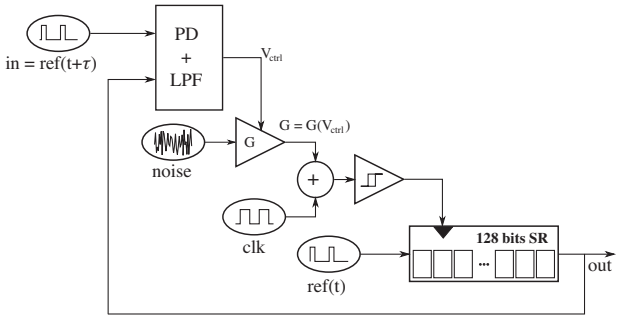

Fig. 4. Noise-controlled PLL (NPLL).

control signal and how the relative delay between the signal and the reference is brought to zero, and therefore both signals become synchronized.

It is interesting to note that noise need not be added to the signal, but instead be already present in a signal of interest due to a finite signal-to-noise ratio. As such, one can envision an application where the goal is to measure a given SNR and the problem is mapped into the measurement of a time delay between an arbitrary reference and a delayed copy of this reference that traverses the noise-tunable delay line. By clocking the shift register with the signal whose SNR is to be measured, the delay between the reference and its copy can be conveniently calibrated and used to provide a quantitative measure of the SNR of the signal of interest. Since time delays can be easily measured with a very high resolution, this method may lead to a high accuracy measurement of the SNR.

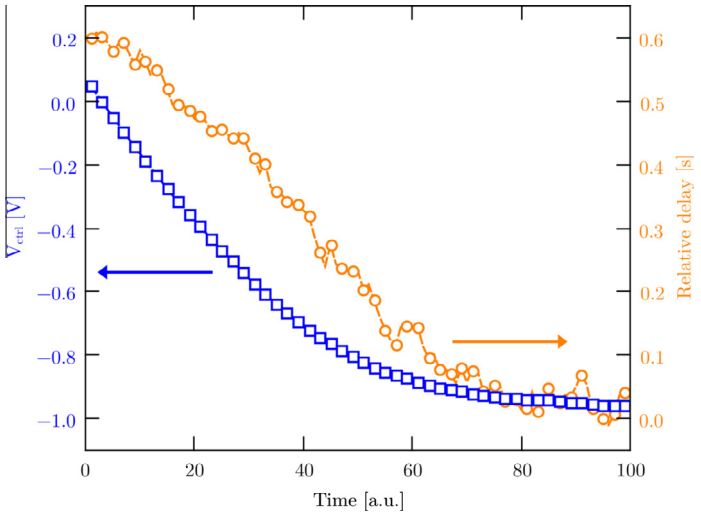

Fig. 5. Control voltage of the NPLL and phase difference between output and reference signals as a function of synchronization time.

4. Conclusions

In this paper we proposed and demonstrated a noise-tunable delay line, *i.e.*, a circuit capable of generating arbitrary time delays dependent on noise. This was achieved by clocking a shift register circuit with a sub-threshold signal. In our demonstration noise was added *ad hoc* to the sub-threshold signal, and we studied the dependence of generated delay on the noise amplitude. We observed two regimes: one regime where the delay line behaves in deterministic fashion and, another regime, where the delays are essentially dominated by the noise correlation time.

We then went on to demonstrate an application to the phase locking of signals by means of a standard Phase-Locked Loop design, where the usual voltage-controlled oscillator was replaced by the noise-tunable delay line.

Finally, we suggested the possibility of mapping the problem of measuring a signal-to-noise ratio of interest to the measurement of a delay between an arbitrary reference signal and its delayed copy. The implementation of an SNR measurement unit using this idea is a matter of future work.

Acknowledgements

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