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A polaronic stacking fault defect model for $CaCu_3Ti_4O_{12}$ material: an approach for the origin of the huge dielectric constant and semiconducting coexistent features

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Abstract

This paper proposes a polaronic stacking fault defect model as the origin of the huge dielectric properties in $CaCu_3Ti_4O_{12}$ (CCTO) materials. The model reconciles the opposing views of researchers on both sides of the intrinsic versus extrinsic debate about the origin of the unusually high values of the dielectric constant measured for CCTO in its various forms. Therefore, by considering stacking fault as the origin of the high dielectric constant phenomena, it was shown that the internal barrier layer capacitance mechanism is enhanced by another similar, but different in nature, mechanism that operates in the nanoscale range due to polaron defects associated with stacking fault, a mechanism that was referred to as nanoscale barrier layer capacitance (NBLC). The NBLC approach explains the origin of the CCTO's huge dielectric constant coexisting with semiconducting features.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The perovskite-derivative calcium copper titanate, $CaCu_3Ti_4O_{12}$ (CCTO), has a body-centred cubic crystal structure with slightly tilted [TiO_6] octahedra facing each other [1, 2]. This material shows a huge dielectric constant [2], sometimes larger than 50×10^3, over a wide temperature range, i.e. from 100 to 400 K [1, 3–5]. As expected, since the first reports by Subramanian *et al* [4], there is a strong debate about the intrinsic or extrinsic origin of this unusual dielectric property.

Most researchers attribute the remarkably high permittivity values to Maxwell–Wagner relaxation as a result of semiconducting properties inside the grains and insulating properties at the grain boundaries [6] or electrode interface [7, 8]. However, very few works address the semiconducting properties of CCTO materials. The semiconducting features cannot be suppressed regardless of the synthesis process used or the value of dielectric constant found. This fact challenges our understanding of this material.

Whangbo and Subramanian [9] proposed the existence of twinning parallel (1 0 0), (0 1 0) and (0 0 1) planar defects [9]. According to them, changes in the local electronic structure act as insulating barriers, contributing to the dielectric properties of CCTO. The proposed twinning defects or crystalline displacements are sustained by evidence of huge dielectric constants in CCTO single crystals [10]. It is important to note, however, that twinning defects always exist in much lower concentrations when compared with crystalline displacements such as stacking faults.

Another interesting feature observed in CCTO ceramics is the existence of a nonlinear current–voltage characteristic [11, 12]. This non-Ohmic behaviour was considered to be due to Schottky-type electrostatic barriers at the grain boundaries [11, 13], as confirmed by surface potential microscopy and Kelvin probe microscopy [11]. These results seem to support the idea of an extrinsic origin for the ultrahigh dielectric properties [14]. Furthermore, other studies suggest that conductive grains and insulating grain boundaries could offer

a plausible explanation for the high dielectric constant [6]; domain barriers having their origin in twinning defects could play a similar role to that of grain boundaries [10, 15–17]. This latter picture is analogous to the traditional internal barrier layer capacitance (IBLC) model, even though the internal barriers are formed by unspecified junctions existing inside the grains [15, 16].

As an attempt to confirm the extrinsic origin of the dielectric properties, it has been suggested, based on a comparative structural and spectroscopic analysis between polycrystalline and single-crystal materials, that the ultrahigh dielectric constant of CCTO is controlled mainly by internal domain boundaries [15, 16].

Dielectric or capacitance spectroscopy analyses have shown that the grain boundaries indeed participate in the dielectric behaviour; however their contribution represents only about 25% of the total dielectric response [18], showing that the grain boundaries *per se* cannot account for the ultrahigh dielectric properties [18].

In this paper we propose a model that reconciles the opposing views of researchers on both sides of the intrinsic versus extrinsic debate about the origin of the unusually high values of dielectric constant measured for CCTO in its various forms (single crystals, polycrystalline samples and films). Furthermore, the model accounts for the influence of processing conditions [19–22] on the current–voltage behaviour, dielectric constant values, for the impedance and dielectric spectroscopy curves and it is also in agreement with x-ray photoelectron spectroscopy (XPS) results for polycrystalline CCTO samples. As shall be seen, the model has an IBLC similar approach, but operates complementarily in the nanoscale range with a different chemical and physical nature. It was then herein named nanoscale barrier layer capacitance (NBLC) model.

2. Experimental procedure

The stoichiometric CCTO and CCTO/CTO (no stoichiometry) polycrystalline samples were prepared by solid-state reactions. All the starting materials used were of analytical grade: $CaCO_3$ (Aldrich-99.99%), TiO_2 (Aldrich-99.8%) and CuO (Riedel-99%), using appropriate molar mixing to reach CCTO stoichiometry or CCTO/CTO, i.e. $Ca_{0.25}Cu_{0.75}TiO_3$ for CCTO and $Ca_{0.5}Cu_{0.5}TiO_3$ for the CCTO/CTO system. These oxides were milled in alcohol for 24 h with zirconia balls inside a polyethylene bottle. The slurry was dried and heat-treated at 900 °C in an ambient atmosphere for 12 h. The heat-treated powders were uniaxially pressed (1 MPa) into discs of 12 mm diameter and 1 mm thickness followed by isostatic pressing at 210 MPa. The discs were sintered at 1100 °C for 3, 12, 24, 48 and 72 h in a conventional furnace in an ambient atmosphere with heating and cooling rates of 5 °C min^{-1}. The sintered samples were polished until the faces became plane and parallel. Gold contacts were deposited by sputtering on the samples' surfaces for electrical characterization.

Current-tension measurements were carried out with a high voltage source-measure unit (Keithley Model 237). The switching electric field (V_s) was obtained at 1 mA cm^{-2} current density. Numerical values for the nonlinear coefficient α were obtained by a linear regression of the log J versus log E plot within the 1–10 mA cm^{-2} range. The leakage current was determined at an electric field equal to 80% of the breakdown field. Impedance and dielectric spectroscopy measurements were performed with a frequency response analyzer (HP 4294A) in the frequency range from 100 Hz to 15 MHz.

The sintered samples were characterized by x-ray diffraction (XRD, Rigaku 20-2000) and the microstructure was studied with a scanning electron microscope (SEM, Zeiss DSM 940A) using samples thermally etched for 5 min at 50 °C below the sintering temperature. The samples were single-phase (CCTO) under x-ray resolution. The average grain size of the sintered samples was determined by the interception method. The Ti, Cu and Ca x-ray photoelectron spectra (XPS) of CCTO and CCTO-CTO sintered and polished samples were registered by means of a VG-Escalab spectrometer. The results were processed with CasaXPS software and the binding energies were corrected using the component of C, from hydrocarbons adsorbed onto the samples' surfaces, fixed at 285.0 eV. The registered data were plotted along with the spectral decomposition of the Ti 2p, Cu 2p and Ca 2p bands into Gaussian–Lorentzian (G–L) components in which solid lines stand for curve fits.

3. Result and discussion

3.1. The defect model

In a perfect CCTO crystal, Cu^{2+} ions are coordinated by four oxygen atoms leading to a square planar arrangement bonded to Ca^{2+} (coordinated by 12 oxygen atoms) in such a way that an alternating Cu/Ca network extends in three different directions [9]: [1 0 0], [0 1 0] and [0 0 1], as schematically drawn in figure 1. Furthermore, these Cu and Ca atomic layers are intercalated by Ti^{4+} ions coordinated by 6 oxygen atoms.

The simple creation of planar defects, as described, would generate a number of imbalances that would in turn precipitate other structural changes in order to address the increase in lattice energy. The formation of point defects (oxygen vacancies and metal valence changes) would bring about a more defective structure, albeit not necessarily energetically stable structure (indeed, all processing conditions indicate that the chemistry defect that controls the dielectric features in CCTO materials is metastable [19, 20]).

The defect proposed here as responsible for the dielectric and semiconducting properties of CCTO is a stacking fault. It can easily be visualized by imagining a sliding motion by half a unit cell of one atomic plane against the other along the [1 0 0], [0 1 0] or [0 0 1] directions. The most favourable plane is (2 2 0), as indicated in figure 2(*a*). The original structure and the result of such displacement can be seen in the drawing shown in figure 2.

The smaller distances between Ca atoms in adjacent unit cells, for example, is energetically unfavourable. It should be accompanied by oxygen vacancies, which would in turn lead to the formation of TiO_5 clusters and sub-coordinated Ca atoms, to reach higher stability. Therefore, the local charge

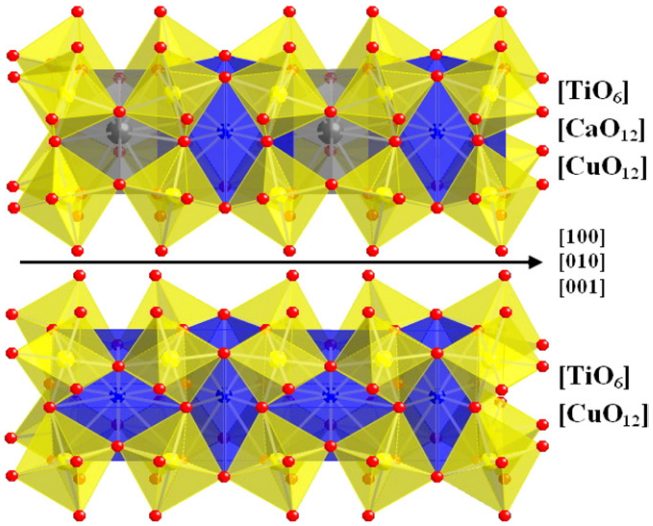

Figure 1. CCTO substructures illustrating the two atomic chains of Ca^{2+} and Cu^{2+} occupying dodecahedral sites and TiO_6 clusters.

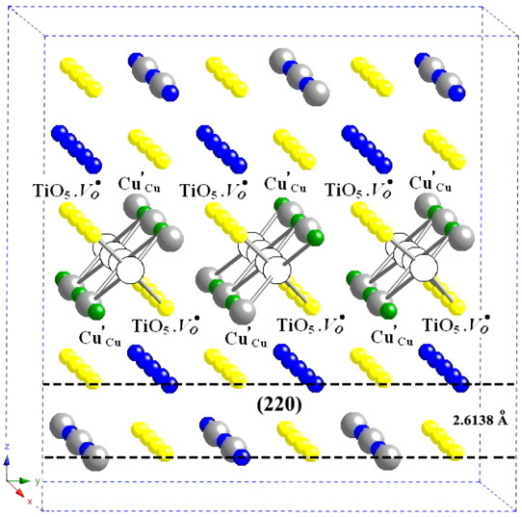

Figure 3. Stacking fault represented according to the presence of Ti and Cu atoms. Note that the oxygen vacancies are a prerequisite for this kind of defect chemistry in CCTO.

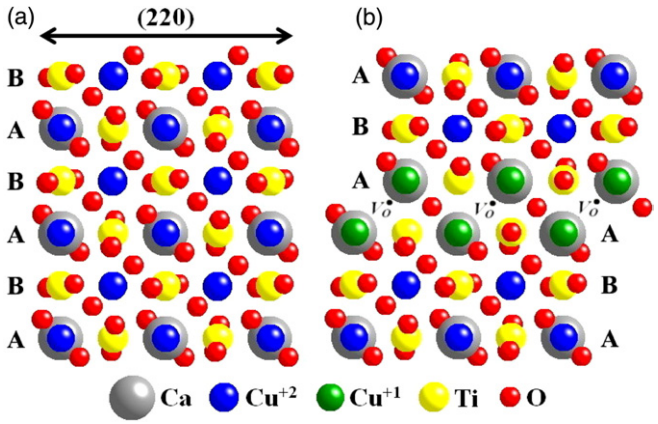

Figure 2. (*a*) Ideal crystalline structure of CCTO. (*b*) Sliding motion by half a lattice parameter, leading to a defective structure based on stacking fault formed in CCTO materials.

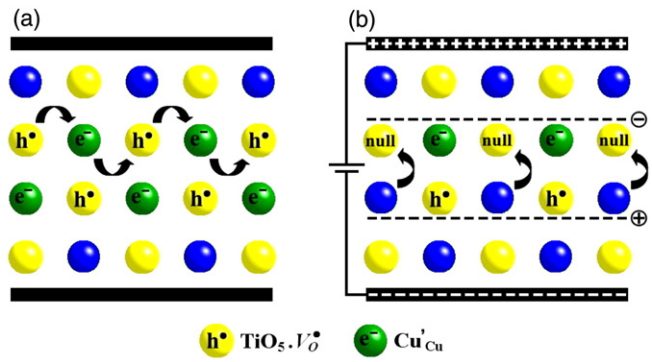

Figure 4. (*a*) Schematic representation of the electrical conduction through charge transfer between occupied and unoccupied polaron units along the structural planar defects. (*b*) Capacitive direction perpendicular to the planar defects. The mechanisms represented in the figure are based on the stacking fault defect chemistry.

neutrality would be kept by the reduction of Cu^{2+} to Cu^{1+} and the formation of oxygen vacancies. The oxygen vacancies would be easily accommodated in the TiO_5 local substructure. In summary, the stacking fault defect chemistry is composed of Ca atoms sub-coordinated, Cu^{1+} and TiO_5 cluster substructures with oxygen vacancies valences as illustrated in the four unit cells of figure 3, where the oxygen atoms were omitted for clarity.

An important byproduct of the electron transfer between Ti clusters and Cu ions across the stacking fault interface is likely the creation of polaron electronic defects ($TiO_5 \cdot V_o^{\bullet}$–$Cu'_{Cu}$) in which electrons from $TiO_5 \cdot V_o^{x}$ ($TiO_5 \cdot V_o^{\bullet} + e^-$) clusters would jump to Cu^{2+} ions, i.e. Cu^{x}_{Cu} (Cu'_{Cu}+$h^{\bullet}$). In other words, the negatively charged TiO_5 clusters of the stacking fault substructure will form a polaronic defect with adjacent Cu^{2+} atoms that are capable of receiving electrons through reduction to Cu^{+}. The dynamic of polarons can be described by electron transfer through $TiO_5 \cdot V_o^{\bullet} - Cu'_{Cu}$ to $TiO_5 \cdot V_o^{x} - Cu^{x}_{Cu}$ and vice versa.

3.2. Implications of the model

The existence of polarons in CCTO is a plausible explanation for the huge dielectric constant associated with induced dipolar structures possessing low relaxation times (high frequencies). Polarons would be able to sustain the high dielectric constant up to frequencies in the megahertz range, as already suggested by Zhang and Tang [23]. The conductivity along the plane of the stacking fault is significantly enhanced by electron transfer between $TiO_5 \cdot V_o^{\bullet}$–$Cu'_{Cu}$ and $TiO_5 \cdot V_o^{x}$–Cu^{x}_{Cu} levels, i.e. TiO_5 and Cu^{+2} adjacent structures (see figure 4(*a*)). On the other hand, perpendicular to this plane there is a conduction barrier since the charges will be confined into planar structures (see figures 3 and 4(*b*)). As a result, the properties in the bulk (grains) of the CCTO polycrystalline samples would depend not only on nanometre internal barriers but also on the electronic conduction paths. This leads to huge dielectric properties combined with high dielectric loss, especially at low frequencies, as evidenced by combined impedance and dielectric spectroscopy measurements.

Table 1. Dielectric constants for CCTO isostructural systems. The applied frequency for $SrCu_3Ti_4O_{12}$ was not reported; all the other samples were measured at 100 kHz.

CCTO isostructures	Dielectric constant	Reference
$CaCu_3Ti_4O_{12}$	>10 286	[4, 11, 18]
$CdCu_3Ti_4O_{12}$	409	[4]
$La_{2/3}Cu_3Ti_4O_{12}$	418	[4]
$Sm_{2/3}Cu_3Ti_4O_{12}$	1665	[4]
$Dy_{2/3}Cu_3Ti_4O_{12}$	1633	[4]
$Y_{2/3}Cu_3Ti_4O_{12}$	1743	[4]
$Bi_{2/3}Cu_3Ti_4O_{12}$	1871	[4]
$SrCu_3Ti_4O_{12}$	200	[24]
$CaCu_3Ge_4O_{12}$	34	[25]
$CaCu_3(Ti_{3,8}Cr_{0,2})O_{12}$	88	[26]
$CaCu_3(Ti_{3,8}Fe_{0,2})O_{12}$	87	[26]
$Ca_{0,9}Sr_{0,1}Cu_3Ti_4O_{12}$	~1000	[27]
$Ca_{0,8}Sr_{0,2}Cu_3Ti_4O_{12}$	~200	[27]
$Ca_2Cu_2Ti_4O_{12}$	~1500	[12]

In contrast to what happens in ferroelectric materials, there is no crystallographic phase transition activated by temperature in CCTO [5, 28, 29]. The stacking fault defect is able to explain the dielectric properties at temperatures lower than 100 K since there will be dipolar freezing accompanied by a decrease in electronic mobility [2]. At temperatures around 600 K the dielectric constant drastically decreases due to the fact that at this temperature there is enough energy to promote electrons to the conduction band through shallow donors caused by mixed metal valence states, bringing about a consequent increase in the dielectric losses. As the energy is also enough to enhance electronic mobility in all crystalline directions, the dielectric property is also suppressed.

Other perovskites with the same type of crystalline structure have much lower dielectric constants than CCTO, probably because they are unable to accommodate the type of structural defects described herein (see table 1). For instance, in the case of $CaCu_3Ge_4O_{12}$, the Ge^{3+} atoms will not be energetically stable [25] in the network as Ti^{3+} (i.e. TiO_5 clusters) in CCTO. On the other hand, in $SrCu_3Ti_4O_{12}$, Sr has an atomic radius bigger than Ca, making it more difficult to accommodate in alternate Sr/Cu layers [24]. Therefore, changing the atoms in Ca or Ti sites probably prevents the formation of the kind of defects proposed. Table 1 shows dielectric constant values for CCTO isostructures found in the literature.

The conflicting views about intrinsic and extrinsic mechanisms can be reconciled by considering the polaronic stacking fault defects as the main source of the high dielectric constant phenomena in CCTO. In this way, a similar phenomenology to the well-known IBLC mechanism can still be present. Indeed, the stacking faults are the main and originally intrinsic chemical defects contributing to CCTO huge dielectric features, in spite of the extrinsic phenomenology of the process. Therefore, it will be shown herein that a complementary phenomenological IBLC similar effect occurs as a consequence of this polaronic stacking fault defect. In terms of phenomenology, the basic difference between the proposed phenomenon, referred to as NBLC, and IBLC, is the (much smaller) scale of action. Furthermore, regarding physical and chemical nature, they are totally distinct.

The possibility of distinguishing the polarization due to space charges trapped at the grain boundaries from that due to dipolar relaxations has recently been demonstrated by complex dielectric/capacitance analysis in CCTO/$CaTiO_3$ (CCTO/CTO) composites [30]. The non-Ohmic properties of CCTO/CTO were even demonstrated to be very similar to the highest values for single-phase polycrystalline CCTO [12, 30]. However, the dielectric response falls in the range of traditional $ATiO_3$-type perovskites, about 10^3, i.e. at least two orders of magnitude lower than the one for single-phase CCTO. Therefore, a direct relationship between the non-Ohmic features and the ultrahigh dielectric response cannot be easily established [12, 18, 30].

Using the same type of reasoning applied to CCTO isostructural materials, one can assume that the type of defect proposed in this paper is not present in CCTO when the concentration of Ca atoms is either lower or higher than the stoichiometric composition. Most likely, the stacking faults and their associated defect chemistry in CCTO materials are metastable defects formed at high temperature during processing [20]. This assumption is supported by the fact that higher cooling rates lead to an increase in the dielectric constant in polycrystalline CCTO samples.

3.3. The nonlinear current–voltage behaviour

The non-Ohmic behaviour of a polycrystalline material, in the majority of situations, is described by insulating electrical behaviour when the sample is subjected to a voltage below its characteristic switching voltage [31] (also referred to as breakdown voltage or breakdown electrical field). In this situation, only a leakage current is expected to pass through the material's polycrystalline microstructure. When the voltage or electrical field exceeds the switching voltage (V_s) or switching electrical field (E_s), the material becomes very conductive and the current experiences a sudden increase. In general, when the applied voltage returns to values lower than the switching voltage, the device returns to its highly resistive state. In this way, the switching voltage is a macroscopic parameter that marks the boundary between a low field region, in which the current–voltage behaviour is expected to be Ohmic, from a high field region in which the current–voltage behaviour is highly nonlinear. For the majority of non-Ohmic systems, V_s is related to the microscopic features of polycrystalline materials by means of the following simple expression [31]:

$$v_b = V_s/p \tag{1}$$

in which v_b is defined as the voltage per barrier and p is the number of active barriers between electrodes.

Obviously, equation (1) carries the implicit assumption that the majority of electrostatic potential barriers at the grain boundaries contribute to the non-Ohmic behaviour of the system. This implies that tailoring the switching voltage for a device is simply a matter of fabricating a sample with an appropriate number of grains in series between the electrodes. In order to achieve a given switching voltage, one

Table 2. Values for the nonlinear coefficient obtained in traditional current ranges (α), switching electrical field (E_s), leakage current at 80% of the breakdown field (I_l), average grain size ($\overline{d}$) and dielectric constant (ε) measured at 100 kHz for CCTO ceramic samples. ST stands for sintering time.

ST (h)	α	E_s (V cm^{-1})	I_l (μA)	$\overline{d}$ (μm)	ε
3	11	1576	103	14	8550
12	8	1007	115	18	13 900
24	2	24	249	22	161 300
48	3	9	180	24	349 900
72	3	12	172	27	389 000

can change the thickness of the sample (for a fixed grain size) or, alternatively, vary the grain size to increase the number of barriers keeping a constant device thickness. In either case, equation (1) can be rewritten as follows [31]:

$$V_s = v_b L/\overline{d}, \tag{2}$$

in which L is the space between the electrodes or the sample thickness and $\overline{d}$ is average grain size.

According to equation (2), for a fixed thickness, an increase in the mean grain size must lead to a linearly proportional decrease in the switching voltage. These equations can successfully be applied to classical non-Ohmic materials such as SiC, ZnO, SnO_2, TiO_2 and $SrTiO_3$ [31]. However, in these systems the dielectric constant ranges only from about 100 to 1000, even for polycrystalline systems presenting high nonlinear coefficient values [31].

Regarding the nonlinear current–voltage behaviour of CCTO, table 2 gives us specific data, including the nonlinear coefficient values (α values). It is important to point out that generally, for traditional non-Ohmic devices (varistors), α values are calculated using current densities starting at 1 mA cm^{-2} and ranging up to 10 mA cm^{-2}, which was the same methodology used in this work [12, 31]. Figure 5 shows the plots of J–E measurements as a function of sintering time.

As one can see in the results presented in table 2, the α values obtained for these CCTO samples are very low when compared with those from other works. However, the dielectric constants measured can reach really large values depending on the sintering time [11] or stoichiometry [12].

Both table 2 and figure 5 show that equation (2) is not obeyed in the case of CCTO samples due to the presence of defects that act as potential barriers inside the grains, not only determining the dielectric properties, but also influencing the non-Ohmic behaviour. This is because equation (2) derives from the well-known block model, in which the grains are considered to be conductive regions and the grain boundaries capacitive regions due to potential barriers [31]. The most remarkable departure from equation (2) can be observed in the sudden decrease in the switching voltage (or switching electric field) when the sintering time is increased from 12 (1007 V cm^{-1}) to 24 h (24 V cm^{-1}).

Figure 6 shows the complex impedance and capacitance diagrams as a function of sintering times. In figure 6(a) one can notice a decrease in resistance coupled to a decrease in

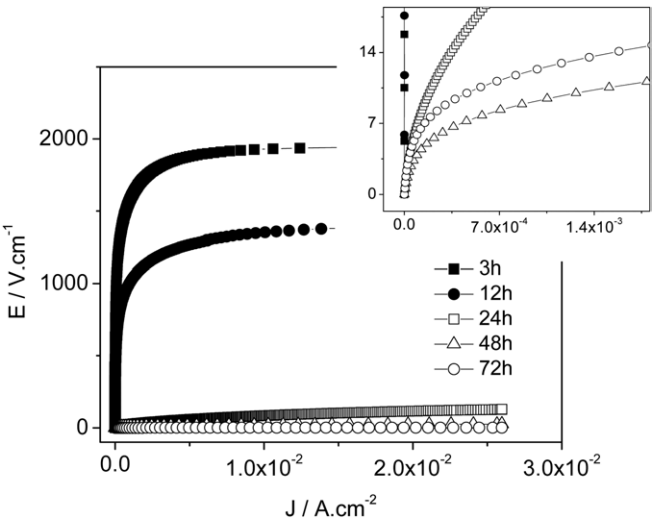

Figure 5. J–E curves for CCTO ceramics as a function of sintering time showing the abrupt decrease in switching voltage for sintering times greater than 12 h. The inset shows details in the low voltage region.

switching voltage and an increase in the dielectric constant. One can infer from the complementary results shown in figures 5 and 6 that the switching voltage obtained from current–voltage plots is strongly influenced by barrier layer structures inside the grains.

Figure 6(b) shows the complex capacitance diagrams for CCTO ceramics as a function of sintering time. The dipolar relaxation showing a near-Debye pattern associated with the intrinsic (bulk) dielectric properties is visible in the higher frequency region expanded in the insets. This kind of relaxation in the CCTO samples has already been reported and discussed previously [18, 30].

Since the dielectric properties may be strongly related to multi-junction domains, it would not be fully appropriate to use parameters such as dielectric permittivity or susceptibility, since it would be almost impossible to know enough about the dimensions of the particular regions involved. That is why we prefer to express the dielectric response in terms of complex capacitance (C^*) instead of complex dielectric form (ε^*). However, it should be noted that all the samples have very similar dimensions (1 mm thickness and 12 mm diameter) and therefore their results can be directly compared.

The changes in capacitance and capacitive loss as a function of heat treatment time (sintering time), plotted against the frequency of measurement in figure 7, clearly show the abrupt change in dielectric properties for longer sintering times. This Bode representation makes it easier to observe that the increase in the dielectric constant comes with a simultaneous increase in dielectric loss. The higher dielectric loss is related to the increase in leakage current and decrease in switching voltage displayed by the same samples in table 2. Apparently, the Debye-type dielectric relaxation (see figures 6 and 7) observed in the high frequency region is the same as that reported by Zhang *et al* [5], who studied its dependence on temperature. This high frequency region was also already described by us previously [18, 30].

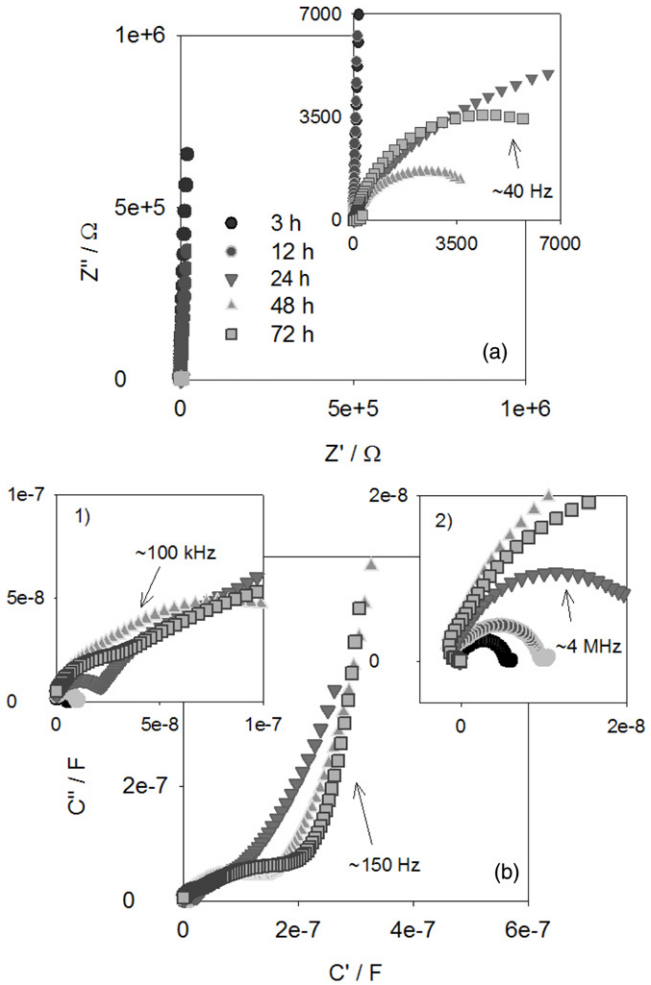

Figure 6. Complex (*a*) impedance and (*b*) capacitance diagrams for CCTO samples as a function of sintering time, showing the overall relaxation pattern. The higher frequency region exhibits a near-Debye relaxation related to the bulk dielectric features. The insets are magnifications of the high frequency region of each diagram. Insets (1) and (2) are two different magnifications of the data in (*b*). (2) is the highest frequency region.

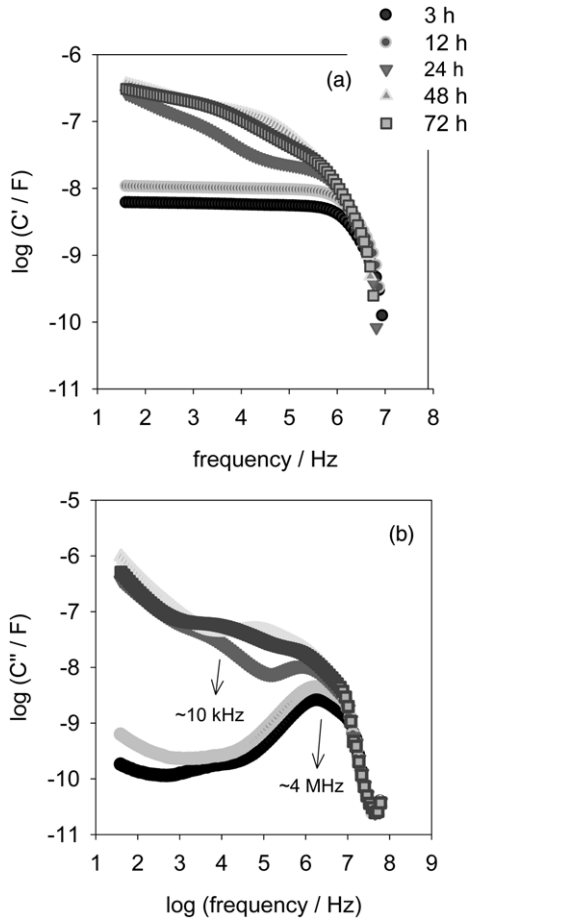

Figure 7. Bode capacitive diagrams, (*a*) real (C') and (*b*) imaginary (C'') parts for CCTO samples as a function of sintering time. Only the exponents of the decimal logarithmic scale were represented.

3.4. The phenomenology of the NBLC model

By analysing the electrical measurements in the light of the defect model proposed, one could reason that the stacking faults and any defect chemistry associated with polaronic effect (conduction in one plane and insolating perpendicularly) could lead to a kind of nanosized barrier layer capacitance (NBLC).

The capacitance for a monocrystal is then given by

$$C = k\varepsilon_0 A/L, \tag{3}$$

in which A is the area of the electrode and L is the distance between electrodes. ε_0 is the vacuum permittivity. k is the dielectric constant of the monocrystal. Traditionally, in the case of the IBLC model, the number of potential barriers between electrodes is given by $p = L/\overline{d}$, in agreement with equations (1) and (2). Therefore, for a polycrystalline material with conductive grains, the capacitance is dictated by the micrometre scale (each grain acts as a capacitor), so that individual capacitance is

$$C = k\varepsilon_0 A/\overline{d} = k_{\mathrm{ef}_{(\mathrm{IBLC})}}\varepsilon_0 A/L. \tag{4}$$

By comparing equations (3) and (4), it is possible to demonstrate that the polycrystalline geometric effect increases the total capacitance about an order of 10^2 to 10^3 (which is normally the effect expected when the IBLC phenomenon operates), i.e. by a ratio around $L/\overline{d}$, which means an increase controlled by the number of barriers introduced between the electrodes. This number is in the microscale range since $\overline{d}$ is a microstructure parameter. This explains why varistor systems always present IBLC behaviour caused by potential barriers so that the V_s parameter is controlled by p, or is inversely proportional to $\overline{d}$ [31].

According to this picture, the effective dielectric constant is now given as

$$k_{\mathrm{ef}_{(\mathrm{IBLC})}} = \frac{L}{\overline{d}}k. \tag{5}$$

Indeed, it is also important to emphasize that the potential barrier located at the grain boundaries controls the increasing of the capacitance and switching voltage exactly by the same microstructure dependent ratio, i.e. by $p = L/\overline{d}$.

Now, it is possible to demonstrate that the effect of the nanoscale dielectric layer (NBLC) introduced by polaronic

stacking faults defects is not controlled by $L/\overline{d}$ but by $L/\overline{n}$ (a detailed physical aspect of this phenomenon shall be presented in a future work), where $\overline{n}$ is the mean distance between stacking faults. Hence, now if k is the intrinsic dielectric constant of CCTO, the system's capacitance shall be given by

$$C = k\varepsilon_0 A/\overline{n} = k_{\mathrm{ef}_{(\mathrm{NBLC})}}\varepsilon_0 A/L, \tag{6}$$

and now, following a similar phenomenology, the effective dielectric constant is given by

$$k_{\mathrm{ef}_{(\mathrm{NBLC})}} = \frac{L}{\overline{n}}k \tag{7}$$

and by comparing equations (5) and (7), it takes that

$$k_{\mathrm{ef}_{(\mathrm{NBLC})}} = \frac{\overline{d}}{\overline{n}}k_{\mathrm{ef}_{(\mathrm{IBLC})}}, \tag{8}$$

i.e. the effective dielectric constant is increased by a factor of $\overline{d}/\overline{n}$ from IBLC to NBLC effect (which is the number of internal barriers inside the grain caused by stacking fault defects). As $\overline{d}$ is in the micrometre range and $\overline{n}$ in the nanometre range, the $\overline{d}/\overline{n}$ factor will cause an enhancement of the dielectric constant of about 10^3 over that effect caused by IBLC. Therefore, the overall dielectric constant enhancement expected due to the NBLC effect is about 10^5 to 10^6 (a detailed physical analysis is underway and will be presented in a future work). It is important to note that both phenomena were, therefore, considered to operate concomitantly, i.e. the IBLC traditional mechanism (operated by potential barrier in the grain boundaries region) and the NBLC mechanism (operated by polaronic stacking fault inside the grain).

The NBLC phenomenon introduces the $\overline{n}$ parameter in the general capacitance function. Therefore, essentially the IBLC and NBLC models operate complementarily in CCTO material, although the origin of the capacitance barriers is different in each case (IBLC is caused by space charge region at the grain boundary and the NBLC by intrinsic polaron characteristics associated with stacking fault inside the grains). This picture of the origin of the CCTO's huge dielectric constant shows us the essential aspect of the literature's contradiction which was finally resolved by the proposed model.

The CCTO perovskite isostructures listed in table 1 have dielectric constant values ranging roughly from 10 to 1000. If we assume they are free from the type of defects present in CCTO (polaronic stacking fault), we can now understand the discrepancy. The $\overline{d}/\overline{n}$ factor would enhance the dielectric constant making them reach the levels normally found in CCTO samples. The above mechanism could also be used to interpret the results for CCTO/CTO composites. Their dielectric constant at ambient temperature is around 1500. In this case, only the depletion layer at the grain boundaries contributes to the dielectric constant, the grains are more conductive and the non-Ohmic properties more pronounced, with nonlinear coefficients (α) reaching values larger than 50.

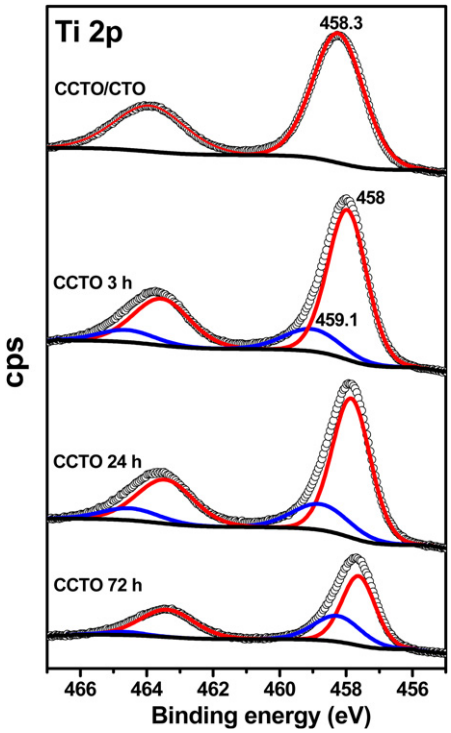

Figure 8. XPS results showing the Ti 2p region of CCTO/CTO and CCTO samples sintered for different periods. (○) Experimental value. Blue (dark grey) and red (light grey) lines are the contribution of each valence component, i.e. TiO_6 or TiO_5 clusters. Note that there is only one environment for Ti atoms in CCTO/CTO, reinforcing the non-existence of polaronic stacking fault defects, suppressing operation of the NBLC. (Colour online.)

3.5. X-ray photoelectron spectroscopy analysis

To reinforce and support the NBLC approach and associated stacking fault defect, XPS measurements were carried out over the CCTO and CCTO/CTO sintered samples reported in this paper. Figures 8 to 10 show the registered XPS curves. The Ti 2p spectrum in figure 8 shows that the Ti $2p_{3/2}$ peak has an asymmetric shape, indicating the presence of different valence states. The binding energies of the signals can be assigned to TiO_5 clusters (459.1 eV) and TiO_5 (458.0 eV). The XPS results presented herein is in agreement with the one discussed by Deng *et al* [32], showing the existence of two different Ti clusters, basically TiO_6 and TiO_5.

Analysing now the Cu 2p spectrum, it is possible to note that the Cu $2p_{3/2}$ peak consists of three components, which were attributed to different Cu–O coordination sites. Accordingly, the lower energy component corresponds to Cu^+, i.e. Cu_2O. The intermediate energy component was assigned to species involving Cu^{2+} (i.e. CuO), and the higher energy component is associated with Cu^{2+} coordinated by 6 oxygen atoms similarly to copper hydroxides and carbonates.

The defect model proposed here also predicts Ca with low coordination numbers due to the oxygen vacancies, which should also be identified by XPS. In the analysis of Ca 2p it is possible to observe the asymmetric Ca $2p_{3/2}$, an uncommon higher energy bonding component which cannot be related to the oxidation state. Therefore, this component is possibly due to the presence of different Ca coordination sites. Asymmetric

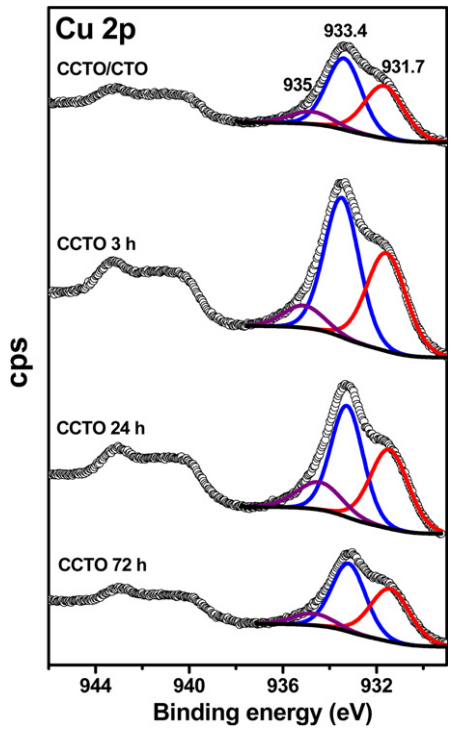

Figure 9. XPS results showing the Cu 2p region of CCTO/CTO and CCTO samples sintered for different periods. (○) Experimental value. Blue (dark grey), red (light grey) and violet (mid-grey) lines are the identification of Cu valences and environments, according to what was discussed in the text. (Colour online.)

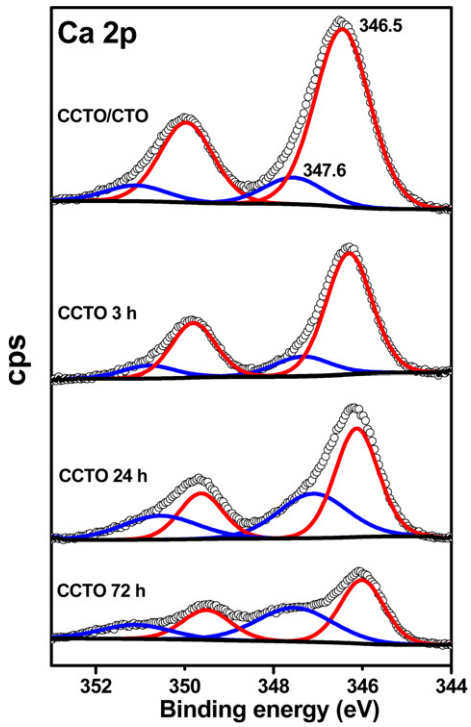

Figure 10. XPS results showing the Ca 2p region of CCTO/CTO and CCTO samples sintered for different periods. (○) Experimental value. Blue (dark grey) and red (light grey) lines are the contribution of each distinct Ca environment. (Colour online.)

Ca $2p_{3/2}$ peaks were reported in the literature for $CaTiO_3$ compounds. They were attributed to the Ca bonding energy variation related to Ca superficial atoms. Probably, Ca is precipitated at the grain boundary regions and then two types of energy would be due to bulk and superficial Ca atoms. The XPS analysis of this paper is in agreement with that performed recently by Deng *et al* [32]. However, although the XPS results are in agreement with the discussion conducted previously by Deng *et al* [32] in terms of Ti, Cu and Ca atomic defects, the polaronic stacking fault model proposed here provides new insights into the huge dielectric properties which were not discussed in a complementary way in the literature, especially with regard to the fact that the the model proposed here links the polaronic effect to stacking fault and to the phenomenology of the IBLC model in the nanoscale. Therefore, the model considers that stacking faults generate associated polaron defects that in the nanoscale range lead to the huge dielectric phenomenon. The model still explains how the IBLC phenomenology fits the apparent huge dielectric constant when polaronic defects originate from stacking faults and complementarily give us a phenomenological explanation by means of equations (6) to (8) for the huge dielectric phenomenon in CCTO materials. Furthermore, the model also explains how the semiconducting properties are adequate to the CCTO huge dielectric phenomenon. In this way, the model is suitable because it reconciles the opposing views of data and interpretation, giving a complete scenario and plausible explanation of the CCTO dielectric and semiconducting properties.

Furthermore, higher CCTO sintering times may increase the concentration of stacking faults. Then, a 48 to 72 h treatment would lead to the highest values, increasing concomitantly the polarons' concentration as evidenced by an increase in the dielectric loss, i.e. figure 7(*b*), and dielectric constant. Therefore, the connections between polarons generate conduction paths, increasing the CCTO conductivity, as evidenced by J–E measurements and also by dielectric loss (figure 7(*b*)) and impedance spectroscopy (figure 6(*a*)).

Finally, it is important to note that the CCTO/CTO composite showed only one environment for Ti, e.g. only TiO_6 clusters without mixing valence. This is evidence that, probably, the stacking faults are not present (at least, not in significant concentration). In this way, the traditional IBLC controls the dielectric constant by means of grain boundary barriers, as usually expected for polycrystalline materials that present both high non-Ohmic behaviour and dielectric properties around 1000 [12, 31]. Both IBLC and NBLC phenomenological models operating in a combined way are able to lead to a huge dielectric constant in CCTO-type compounds.

4. Conclusions

In conclusion, the NBLC mechanism proposed reconciles the opposing views of researchers on both sides of the intrinsic versus extrinsic debate about the origin of the unusually high values of dielectric constant measured for CCTO in its

various forms. The essence of the model is the existence of stacking faults accompanied by polaronic structures, leading to nanoscale barrier layer capacitors, a nanoscale effect on the capacitance or effective dielectric constant of the system. The approach is capable of explaining in a simple way how huge dielectric constant coexists with high dielectric loss, providing an explanation of the dielectric and semiconducting features in CCTO materials.

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