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A Sub-Nanosecond Gate Bias-Switching Circuit for GaN RF Power Amplifiers

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***Abstract*—In this letter, we present a design of a fast gate-switching power amplifier (GSPA) aimed at reducing its power consumption. This GSPA features a dedicated fast gate switching circuit that commutates the gallium nitride (GaN) transistor between a nominal gate bias voltage (GSPA ON) and a strong negative voltage (GSPA OFF), thereby generating two discrete output power levels in an RF-PWM fashion. A fast gate switching circuit, including a commercial digital voltage isolator, is designed to switch between two gate bias voltages. The gate stability resistor and transmission line (TL) are carefully placed and designed to reduce the GSPA parasitic bias line and enable fast switching. Measured results provide a rise and fall time of 750 ps and 950 ps, respectively, and achieved RF pulse widths as narrow as 5.88 ns, thus corresponding to a 170 MHz bandwidth.**

***Index Terms*—Gate-switching circuit, power amplifier, pulse width modulation, power consumption reduction.**

I. INTRODUCTION

IN the current digital age, the extensive deployment of 5G networks is inevitably given the substantial improvement in wireless connection experience owing to the massive operation bandwidth and ultra-low latency [1]. However, this comes at the cost of astounding electricity expenses. It has been investigated that the power amplifier (PA) consumes up to 38% of the energy in 5G base stations [2]. The performance of the PA dictates the entire wireless system design, and consequently, developing energy-efficient PAs is urgent for energy consumption reduction in a communication system.

An interesting technique capable of 100% theoretical efficiency at any output power level is the push-pull class-D power amplifier with radio frequency (RF) pulse-width modulation (PWM) proposed by F. Raab in [3]. However, achieving GHz carrier frequencies with a class-D push-pull configuration is challenging given the absence of high-side drivers and complementary (P-MOS) devices with comparable performance to the low-side RF device. Additionally, achieving fast switching times poses another significant challenge. For GHz frequencies, it is necessary to employ a conventional PA topology such as a class-F or class-E and perform the PWM control on the PA gate or drain so that the RF transistor performs the RF-PWM mixing. Designers often prefer drain switching PA (DSPA) due to the wider dynamic range achievable at the PA output [4]–[6]. However, wideband modulation signals such as IEEE 802.11ax require 160 MHz bandwidth [7]. Developing fast drain modulators to operate switching signals at the sub-nanosecond level can be challenging as it requires high figure-of-merit switches with low series resistance and low capacitances/parasitics to minimize conduction and switching losses. This problem can be alleviated by using gate switching where the ideally zero PA gate current at DC enables the use of high-speed transistors optimized for fast switching [8]. Moreover, using up-to-date gallium nitride (GaN) high-electron-mobility transistors (HEMT) allow extremely low gate parasitics thus enabling very high PWM switching rates. Meanwhile, the gate-modulated switching circuit is becoming less affected by concerns of gate modulators around safe operating voltage and thermal performance owing to the higher breakdown voltage and thermal conductivity of the GaN technology [9], [10].

In this letter, we present an ultra-fast gate-switching PA (GSPA) capable of ~800 ps switching transients using a commercial high-speed digital isolator. The novel approach involves repositioning the gate stability resistor and incorporating a gate bias line to mitigate the isolator RC loading. In this work, stability is studied *including* the gate driver and bypass network. This GSPA efficiently amplifies the signal modulated by ON-OFF keying signals with a constant envelope. Other possible applications for this high-speed switching PA include 1) highly-performance PAs based upon RF PWM; 2) pulsed radars that require quick PA on/off switching to transmit short pulses [9], [11]; 3) base station transmitters perform symbol-level PA shutdown to decrease DC consumption [12]; and 4) cognitive radio network periodic spectrum sensing and access for spectrum handoff operation [13], [14].

II. GSPA DESIGN

The main contribution of this letter is on the gate driving circuit, which includes: 1) gate stability resistor positioned between the gate isolator and supply; 2) stability analysis including the isolator parasitics; 3) gate bias line design with reduced low-frequency parasitics. To this aim, a 10 W inverse class F PA using a GaN transistor operating at f_c = 1.5 GHz is used as a device under test (PA) to demonstrate the fast gate switching which is performed by a digital isolator (Texas Instruments ISO722M) for fast operation with a switching rate of up to 170 MHz. A gate bias voltage alternates between -3 V to switch on the PA and -8 V to switch it off.

If either the input or output port impedance has a negative real part, the PA can exhibit instability and chaotic response

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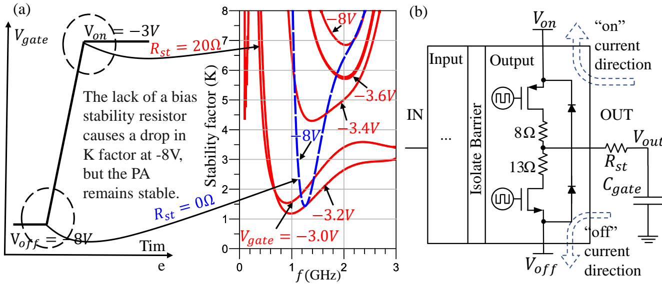


Fig. 1. PA stability analysis at on-off states: (a) The gate voltage V_{gate} switches from "off" at -8 V to "on" at -3 V. The stability factor (K) results by sweeping V_{gate} from -8 V to -3 V with R_{st} = 20 Ω (red lines) and at the -8 V with R_{st} = 0 Ω (blue line); (b) Equivalent output schematic of the ISO722M digital isolator and the current flow directions at the "on-off" states.

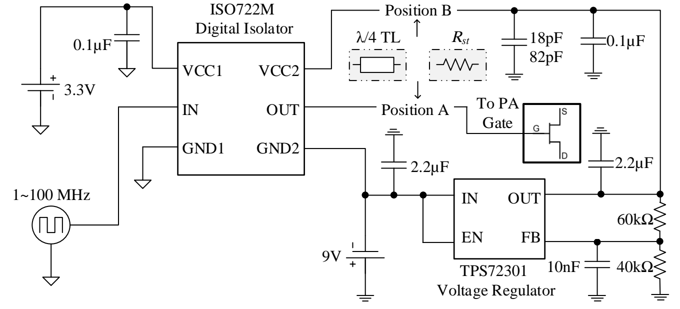
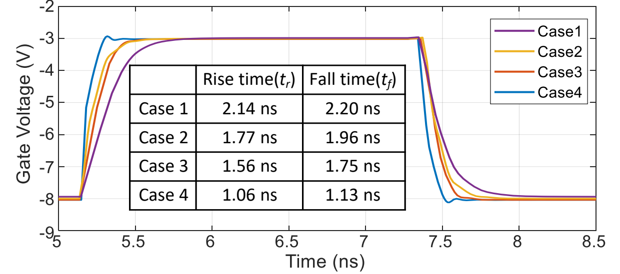


Fig. 2. The schematic of the proposed gate switching control circuit, where $\lambda/4$ TL and the stability resistor R_{st} can be located at either position A or B.



	Rise time(t_r)	Fall time(t_f)
Case 1	2.14 ns	2.20 ns
Case 2	1.77 ns	1.96 ns
Case 3	1.56 ns	1.75 ns
Case 4	1.06 ns	1.13 ns

Fig. 3. PSpice simulation of the 10-90% rise and fall time results are compared among four different cases: In case 1, both $\lambda/4$ TL and R_{st} = 40 Ω are at position A; In case 2, both $\lambda/4$ TL and R_{st} = 20 Ω are at position A; In case 3, $\lambda/4$ TL is at A, while R_{st} = 13 Ω is at position B; In case 4, both $\lambda/4$ TL and R_{st} = 13 Ω are at position B. The load of gate switching control circuit is modeled through an equivalent circuit in PSpice.

with oscillation [15]. Therefore, an external resistance is often introduced to stabilize the PA in the gate bias line. The DC feed line, which is usually a $\lambda/4$ is used to minimize RF leakage to the RF gate short. Employing gate switching with such a design would result in low performance mainly caused by the RC time constant of the stability resistor and gate capacitance. In this design, the gate stability resistor is placed after the gate isolator to reduce this detrimental RC time constant and achieve fast switching rates. However, stability analysis needs to be performed, including the gate driver, and the results are shown in Fig. 1(a). First, we note that stability is an issue only when the PA is at the "on" state. As the PA is switched off without amplification, the stability margin becomes larger, and the PA is unconditionally stable even if the stability resistor is removed in this designed PA. The "off" state stability margin can be reduced to increase the PA switching speed. Introducing a commercial digital isolator separates the output resistors in the gate driver circuit so that different stability resistors R_{st} can be connected to stabilize the PA separately for "on" and "off" states. The schematic of our chosen ISO722M digital isolator is shown in Fig. 1(b). It creates two paths for both "on" and "off" states, such that R_{st} at two states can be minimized individually. We also note the ISO722M has internal resistances for PA stability.

As shown in Fig. 1(b), the gate capacitance C_{bias} and R_{st} constructs a resistor-capacitor lowpass filter to smooth the fast switching pulse signal, where output voltage V_{out} is given by

$$V_{out} = V_{in}\frac{X_c}{\sqrt{R_{st}^2 + X_c^2}}, \tag{1}$$

where

$$X_c = \frac{1}{2\pi f_{sw} C_{bias}}. \tag{2}$$

It can be concluded that the V_{out} shrinks if the switching speed f_{sw} increases from (1) and (2). A practical approach to improving f_{sw} is to minimize R_{st} at the circuit design process. The gate capacitance C_{bias} is derived from

$$C_{bias} = C_{in} + C_{TL}, \tag{3}$$

where C_{in} is the intrinsic gate capacitance in the GaN HEMT, which is estimated by tuning the input port voltage reflection coefficient between the transistor model and its gate bias equivalent circuit in simulation software. It is also possible to minimize TL capacitance C_{TL} at the bias line, which basically shortens its length. C_{bias} minimization will also benefit the gate energy loss P_{gate}, which owing to the charging and discharging of the gate capacitance given by [16]

$$P_{gate} = \frac{1}{2}Re[V \cdot I^*] = 2\pi f_{sw} V_{gate}^2 C_{bias}. \tag{4}$$

The switching circuit converts the control signal output to the corresponding gate bias voltage. We designed a gate-switching circuit using the high-speed digital isolator and voltage-regulation control circuitry. Fig. 2 shows a schematic of the gate switching control circuitry. The primary design consideration of this circuit is its switching speed. Generally, the stability resistor's position is close to the transistor gate terminal (position A in Fig. 2). However, these stability resistors and intrinsic capacitance slow down the control signal. To achieve high gate switching speed, the stability resistor can be minimized by fine-tuning the R-C parallel circuit at the input load line. Additionally, the stability resistor and TL can be relocated to position B instead of A.

Based on the analysis above, we use the Cadence PSpice simulation to verify the switching performance. an equivalent cascaded LC circuit is used to model the GaN PA gate where the impedances seeing into the PA gate bias line are identical. The result is shown in Fig 3. From the comparison between case 1 and case 2, the value of the resistor will influence the switching speed. It is demonstrated that the switching speed is faster when the resistor is located at position B rather than position A from the comparison between case 2 and 3. Also, case 4 verifies that the switching speed is even faster when we posit the $\lambda/4$ TL at position B. It is worth noting that

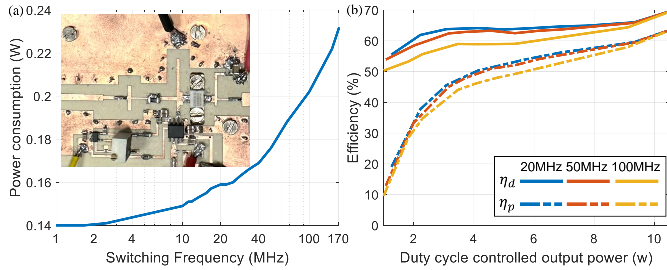


Fig. 4. Measurement result comparison. (a) The photograph of the fabricated switching circuit in GSPA and its measured power P_{gate} dissipation concerning the switching frequency f_{sw}. (b) Drain efficiency and PAE are compared for different duty cycles controlling the output power while sweeping the switching frequencies among 20 MHz, 50 MHz, and 100 MHz.

the $\lambda/4$ TL and stability resistor are relocated. However, the RF impedance is still infinite at the bias line. As a result, the gate-switching circuit does not affect the RF power efficiency. The switching control circuit also includes a subsystem that can generate the -3 V on-state voltage from the main -8 V off-state DC voltage. As shown in Fig. 2, the solution is to utilize a low-dropout (LDO) negative voltage regulator.

To maximize the efficiency of GSPA, a highly efficient PA is required. Class-F PA is generally regarded as one of the most efficient PA. The experimental results show that the inverse class-F PA's power added efficiency (PAE) is 10% higher than the class-F PA [17]. An inverse class F PA is designed where the second harmonic impedance is close to infinity while the impedance of the third harmonic is close to zero. From the simulation, the peak PAE of the designed PA is 73%.

III. Experiment

The photograph in Fig. 4(a) shows the fabricated GSPA using Wolfspeed GaN CG2H40010F transistor with an embedded gate-switching circuit operating at 1.5 GHz. The gate-switching dissipated power P_{gate} is used to drive the circuit switching between -8V and -3V. The value is obtained by multiplying the measured current and voltage from the gate-biased power supply. P_{gate} is rising with the increment of the switching frequency f_{sw}, which is in agreement with the equation in (4). Fig. 4(b) shows the drain efficiency (η_D) and the PAE (η_P) with respect to the different output power of the PA. The η_P in GSPA is defined as

$$\eta_P(f_{sw}) = \frac{P_o - P_{in}}{P_{DC} + P_{gate}(f_{sw})}. \quad (5)$$

The average output power P_o is regulated by the pulse duty cycle, which is independent of the switching speed, i.e., frequency bandwidth. As the GSPA always works at its peak efficiency or switches off, the η_D is almost flat with an P_o range from 3 W to 10.7 W. The η_D drops when the P_o is lower than 3 W since the power that is dissipated at the switching transition period becomes significant. The η_P performance is inferior due to the constant P_{in} and P_{gate}. The switching speed also slightly affects power efficiency. Generally, higher switching speeds result in lower η_D and η_P. The average η_D over the whole P_o range for different switching speeds are 63.9% (20 MHz), 62.7% (50 MHz), and 58.9% (100 MHz). By fully switching on the GSPA with peak P_o of 10.7 W, the peak η_P of 70.2% can be achieved.

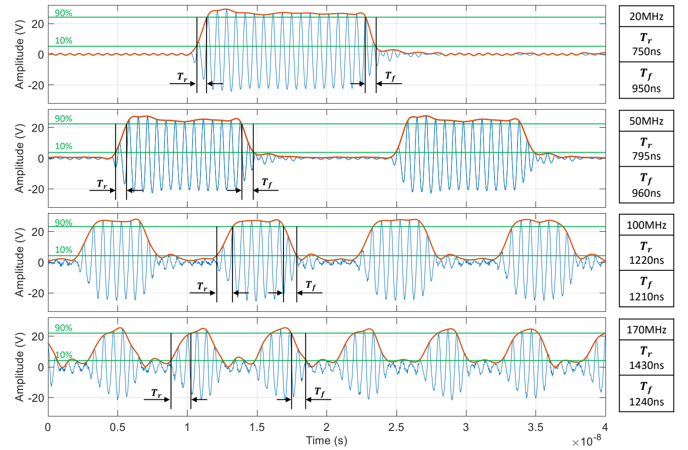


Fig. 5. Measurement of the output RF waveforms, envelopes, and switching speed comparison from the oscilloscope.

TABLE I
Performance Comparison of State-of-the-Art Switching PAs

Tech.	Type	f_c(GHz)	P_o(dBm)	t_r(ns)	t_f(ns)	η_P(%)
SiGe [18]	Class-E PA	0.4	19	14	18.5	44
CMOS [19]	Switch PA	2.4	0	1.5	3.3	40
CMOS [20]	Class-AB PA	2.4	1.2	20	10	32
GaAs [21]	DSPA	5.35	41.4	116	102	14.9
GaN [22]	Hybrid	9.5-10.4	50	12.5	11.1	28.2
GaN [23]	GSPA	3.5	8	70	30	
GaN This work	**Class-F^{-1} GSPA**	**1.5**	**40.3**	**0.75**	**0.95**	**65.4**

Fig. 5 shows waveforms and envelopes obtained from the oscilloscope for different switching frequencies: 20 MHz, 50 MHz, 100 MHz, and 170 MHz. When switching at 20 MHz, average 10%-90% rise time t_r from -8 V to -3 V is 750 ps, while average 90%-10% fall time t_f to switch off the GSPA is 950 ps. The measured result is slightly better than the simulation in Fig. 3, which might be attributed to the inaccuracy of the transistor gate intrinsic impedance in simulation. However, it was noticed that the time required for switching slightly increases as the switching speed goes up.

The waveform ringing becomes significant when approaching the commutation speed 170 MHz, the PA doesn't completely switch off, and the rise/fall time tends to slow down. Consequently, the designed GSPA has a maximum switching frequency of 170 MHz when driven by a square pulse wave. Table I compares this work with the current state-of-the-art. The rise/fall time and efficiency of this work exceeds that of cutting-edge switching PAs. To the best of the authors' knowledge, this is the first published work to achieve sub-nanosecond switching speed for RF GaN PA.

IV. Conclusion

This letter presents a gate-modulated switching PA for power efficiency enhancement with a peak switching frequency of 170 MHz. The dedicated modulated circuit enables the GaN transistor for fast on-off switches, with a rise time and fall time of 750 ps and 950 ps, respectively. This GSPA is used to amplify the constant envelope signals. From the measurement result, this GSPA reaches 65.4% average drain efficiency with an output power range of 0.3 W to 10.7 W.

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