Selective Area Growth of GaAs Nanowire and Micro-Platelet Arrays on Silicon by Hydride Vapor Phase Epitaxy

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Abstract

In this work, we demonstrate the growth of vertically-oriented GaAs nanowires (NWs) and micro-platelets directly on patterned SiO_2/Si(111) substrate by hydride vapor phase epitaxy (HVPE). Direct condensation of GaAs on Si was achieved through a critical surface preparation under As-controlled atmosphere. GaAs NWs were grown along the $<111>_B$ direction with hexagonal cross-section when the hole opening diameter (D) in the SiO_2 mask was below 350 nm. Larger apertures ($D \geq 500$ nm) resulted in uniform micro-platelets. The study highlights the capability of HVPE for selective-area growth of GaAs directly on Si and thus the potential of HVPE as a generic heterointegration process for III-V semiconductors on silicon.

1. Introduction

Monolithic integration of III-V semiconductor devices [1–3] with silicon still remains a major strategic challenge, driven by the demand for data processing and transmission[4]. Indeed, planar epitaxy of high-quality dislocation- and crack-free III-V layers on Si is difficult because of the ~ 4.2% crystal lattice mismatch between GaAs and Si. However, the nanowire (NW) geometry is suitable to integrate free-standing and high performance III-V semiconductors with the low-cost Si technology[5,6]. The NW high aspect ratio and small NW/substrate contact surface allow an efficient strain relaxation. Thus, mechanical, optical and electrical properties of NWs can be exploited to

develop chemical or biological sensors, light-emitting diodes, laser diodes and photovoltaic cells on a Si-platform[7–14].

Several growth methods have been developed to grow GaAs NWs on Si with a high material quality. The most common one is the Vapor-Liquid-Solid (VLS) method in which gold (Au) is used as metal catalyst[15–19]. However, Au is known to act as an impurity which creates deep-level recombination centers, degrading the properties of the material[20]. Consequently, effort has been devoted to grow gold-free GaAs NWs by implementing self-catalyzed VLS growth, where Ga is the catalyst seed ensuring without foreign catalyst[21–23]. Nevertheless, the random nucleation process leads to inhomogeneity of NWs in terms of diameter, length, position and growth direction, which induces inhomogeneity of electronic and optical properties, making the fabrication of devices difficult. An alternative based on selective area growth (SAG) was developed to produce periodic NW arrays on patterned substrates, where growth occurs on pre-determined sites. This approach allows the integration of NWs into large-scale arrays with homogenous properties[24,25]. SAG of GaAs NWs on Si(111) and GaAs$(111)_B$ substrates has been demonstrated by molecular beam epitaxy (MBE) and metal-organic vapor phase epitaxy (MOVPE)[26–32]. Some groups have proven that arsenic (As) pretreatment of the Si(111) surface to form the $(111)_B$-like surface, is mandatory to ensure the vertical growth of GaAs and InAs NWs [32,33]. Several studies have shown a strong relationship between the pattern hole size and the final shape of the GaAs crystal grown on GaAs $(111)_B$ and Si(111) substrates[28,33]. H. Yoshida et al. have reported that the morphology of the GaAs crystal evolved from an hexagonal NW to a truncated tetrahedral shape when the aperture diameter is higher than ~ 100 nm[28]. These findings were also confirmed experimentally and supported by a theoretical model based on the Gibbs free energy variation by K. Ikejeri et al.[34]. The 1-D geometry during SAG depends not only on the growth conditions (temperature and vapor phase composition), but also on the opening diameter.

Hydride vapor phase epitaxy (HVPE) is a low-cost process known for its high intrinsic selectivity because of the low sticking coefficient of the III-chloride precursors on dielectric masks[35]. In addition to specific growth kinetics, it has shown remarkable results on the selective epitaxy of III-nitride nanorods[36–38] and InAs NWs[39]. The Au-catalyst assisted synthesis of pure cubic Zinc Blende (ZB) GaAs NWs has been demonstrated by HVPE through the VLS process[17–

[19,23] with a fast record growth rate[17]. To date, no studies have demonstrated the possible direct condensation of GaAs on silicon by HVPE, which is indeed an essential step toward catalyst-free SAG of NWs. In this paper, we report on the selective epitaxy of well-aligned GaAs NWs grown directly on Si(111) substrate by HVPE. We show that the Si surface preparation is a key step to ensure the direct nucleation of GaAs seeds. We demonstrate that we can tune the final crystal shape from wires to perfectly faceted platelets by coupling the growth conditions and the pattern aperture size. Structural and optical characterizations of NWs and micro-platelets are discussed.

2. Experimental

Selective growth of GaAs was performed on (111)-oriented Si substrates. Silicon oxide (SiO_2) with a thickness of 80 nm, deposited by plasma-enhanced chemical vapor deposition (PECVD), was used as dielectric mask. The pattern consisted of periodic hexagonal arrays of circular openings with different diameters varied from 200 nm to 1 µm defined by electron beam lithography. The patterned Si(111) substrates were chemically etched in a 5% aqueous hydrofluoric solution (HF) for 15 seconds to remove the native SiO_2 layer. Samples of 1 x 1 cm^2 were then loaded in a custom hot-wall HVPE reactor working at atmospheric pressure with H_2 as carrier gas. Gallium chloride (GaCl) gaseous species was produced by reacting HCl gas with liquid gallium at 760 °C in an upstream zone of the reactor. Arsine gas (AsH_3) was introduced in a downstream central zone heated at higher temperature, to ensure a homogeneous mixing of the gas phase and reduce parasitic nucleation upstream of the substrate, since the reactions involving chloride molecules are exothermic. AsH_3 is totally decomposed into As_4/As_2 species when introduced into the hot-wall reactor. One of the specific attributes of HVPE is that the substrate surface interacts with a complex vapor composed of GaCl, HCl, H_2 and As_4/As_2, with the last two species being considered at equilibrium. The substrate was placed in a downstream growth zone that was kept at lower temperature than the central zone. The partial pressures of GaCl, HCl, As_4 and As_2 (H_2 pressure was 1 atm) above the substrate were calculated as a function of the input flows (in sccm) of AsH_3, HCl (above the liquid Ga source) and H_2, the kinetics of decomposition of gaseous AsH_3 into As_4 and As_2[40], and the thermodynamic equilibrium constants of intermediate chemical reactions, by taking into account the temperature gradient along the reactor. The partial pressures of As_4 ranged from 3.6 x 10^{-4} atm to 7.2 x 10^{-4} atm, while the partial pressure of GaCl was varied from 1.6 x 10^{-3} atm to 3.3 x 10^{-3} atm. The samples were heated from 740 °C to 785 °C for GaAs deposition. The

growth time was 15 min for all the samples. The as-grown structures were characterized by scanning electron microscopy (SEM). A Titan 80-300 HB scanning TEM (STEM) operating at multiple accelerating voltages has been used for the structural characterizations. μ-PL measurements were performed in a Janis ST-500 continuous flow cryostat. The samples were located by CCD imaging, while μ-PL excitation and collection were performed through a microscope objective with numerical aperture of 0.7, providing a spot diameter of about 1 μm. The excitation was provided by the 488 nm line of an Ar+ laser with a 130 mW power. μ-PL spectra were collected by a 0.55 m Horiba Jobin Yvon spectrometer and detected by a liquid nitrogen cooled Si CCD camera.

3. Results and discussion

Several growth conditions of temperature and partial pressures were tested to achieve the direct condensation of GaAs crystal on patterned Si substrates, initially inspired by previous works dealing with the growth of GaAs nano- and microstructures[41–45]. In each run, dozens of Si(111) substrates with different hole diameters (D) and pitches (P) were tested (see Figure 1(a)). A reference patterned $GaAs(111)_B$ substrate was also introduced for each experiment to compare the nucleation of GaAs on GaAs and on Si. Figure 1(b) shows an array of GaAs nanostructures selectively grown on patterned $GaAs(111)_B$ template with a hole diameter of D = 200 nm and a constant pitch of P = 1.5 μm. The growth temperature was 740 °C and the partial pressures were 1.6×10^{-3} atm for GaCl and 7.2×10^{-4} atm for As_4. Here, the growth time was reduced to 30 s due the high axial and lateral growth rates of GaAs on GaAs which causes coalescence. Growth was perfectly selective on a large area of the substrate and consisted of hexagonal nano-platelets delimited by six equivalent {110} lateral facets and the $(111)_B$ top facet. However, no GaAs growth occurred on the Si substrate whatever the pattern and growth conditions. This further confirmed that the direct condensation of GaAs on Si is not achievable in standard growth conditions without specific preparation of the Si surface.

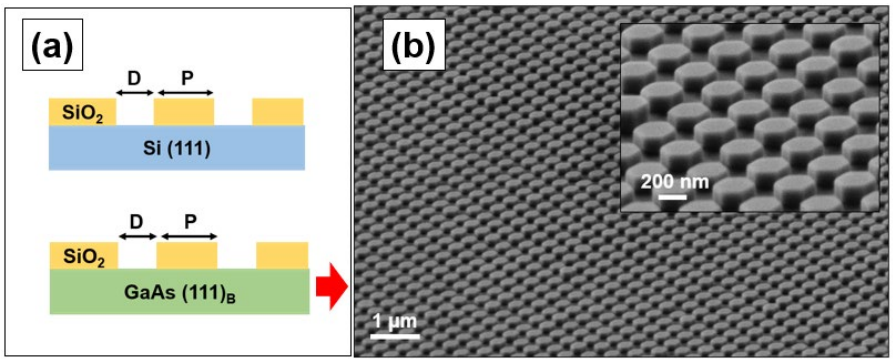

Figure 1. (a) Schematic view of patterned Si(111) and GaAs(111)$_B$ substrates used in this work. D is the hole diameter of 200 nm and P is the pitch of 1.5 µm. (b) Tilted-view SEM image of GaAs nano-platelets selectively grown on patterned GaAs(111)$_B$ substrate. The SAG of GaAs on GaAs(111)$_B$ at the nanoscale is achieved.

We can consider that the first stage of GaAs nucleation on Si by HVPE is the limiting step. In brief, the growth of GaAs in the HVPE process is initiated with the adsorption of gaseous As_4 molecules on vacant V sites of the surface, on which gaseous GaCl molecules are adsorbed to form a layer of AsGaCl. The final step is the chlorine desorption from AsGaCl ad-species by H_2. These growth reactions are summarized as follows:

$$2As_{2(g)} \rightleftarrows As_{4(g)} \quad (1)$$

$$4V+As_{4(g)} \rightleftarrows 4\ As \quad (2)$$

$$As+GaCl_{(g)} \rightleftarrows AsGaCl \quad (3)$$

$$AsGaCl+\frac{1}{2}H_{2(g)} \rightleftarrows GaAs_{(c)}+HCl_{(g)} \quad (4)$$

where index g is assigned to gaseous molecules; index-free species are adsorbed molecules or atoms; and index c is for crystalline species. Therefore, the GaAs deposition can be summarized by the global reaction:

$$\frac{1}{4}As_{4(g)}+GaCl_{(g)}+\frac{1}{2}H_{2(g)} \rightleftarrows GaAs_{(c)}+HCl_{(g)} \quad (5)$$

The most important feature is the build-up of a stable chemisorbed AsGaCl on the substrate. For instance, the growth of GaAs on GaAs(111)$_B$ surface is much easier. The vacant sites of stable As atoms on the surface are already available for GaCl adsorption to form stable AsGaCl ad-molecules. However, the direct adsorption of group V elements and/or group III elements on Si is

unfavorable at usual growth conditions of GaAs by HVPE. This requires additional steps to prepare the Si surface to ease the nucleation. Actually, direct growth of Ga-related material on Si is difficult for VPE processes. The solution is to saturate the Si surface with As atoms. According to Tomioka et al., the Si(111) surface can be modified into a $(111)_B$-like oriented plane under AsH_3 treatment at low temperature (400 °C): the topmost Si atoms are replaced by As atoms to form an As-adsorbed Si(111) 1 x 1 surface[32,33]. A GaAs buffer layer is then grown at low temperature to prevent the thermal desorption of the adsorbed As atoms during the annealing ramp up to the final growth temperature. All in all, the authors implemented a seven-step growth to obtain vertical GaAs NWs on Si.

In the present work, an additional surface preparation step of the Si(111) substrate under As_4 atmosphere was introduced during the pre-growth heating ramp. A high input partial pressure of $As_4 \sim 7.2 \times 10^{-4}$ atm was necessary to compensate the significant desorption rate of As atoms from the surface as the temperature rises. Once the As atoms are available on the Si surface, the growth of GaAs can easily be initiated. Figure 2(a) and (b) show tilted-view and top-view SEM images of regularly arranged and vertically aligned GaAs NWs grown on patterned Si(111) substrate with 350 nm-diameter holes and a pitch of 1.75 µm under optimized growth conditions (conditions 1 in Table 1). The growth temperature was 785 °C and the input partial pressures of GaCl and As_4 were 3.3×10^{-3} atm and 7.2×10^{-4} atm, respectively. These NWs were grown at approximatively 6.4 µm/h and exhibited a perfect hexagonal shape with a constant diameter. Si is nonpolar and growth on its (111)-oriented directions could result in both vertical and tilted 19.6° oriented GaAs structures. According to Ref.[32], the observation of strictly vertical NWs on the whole Si substrate implies that the NWs were all grown along the $<111>_B$ direction. This confirms that As was incorporated on Si sites of the Si(111) surface following the As_4 surface treatment.

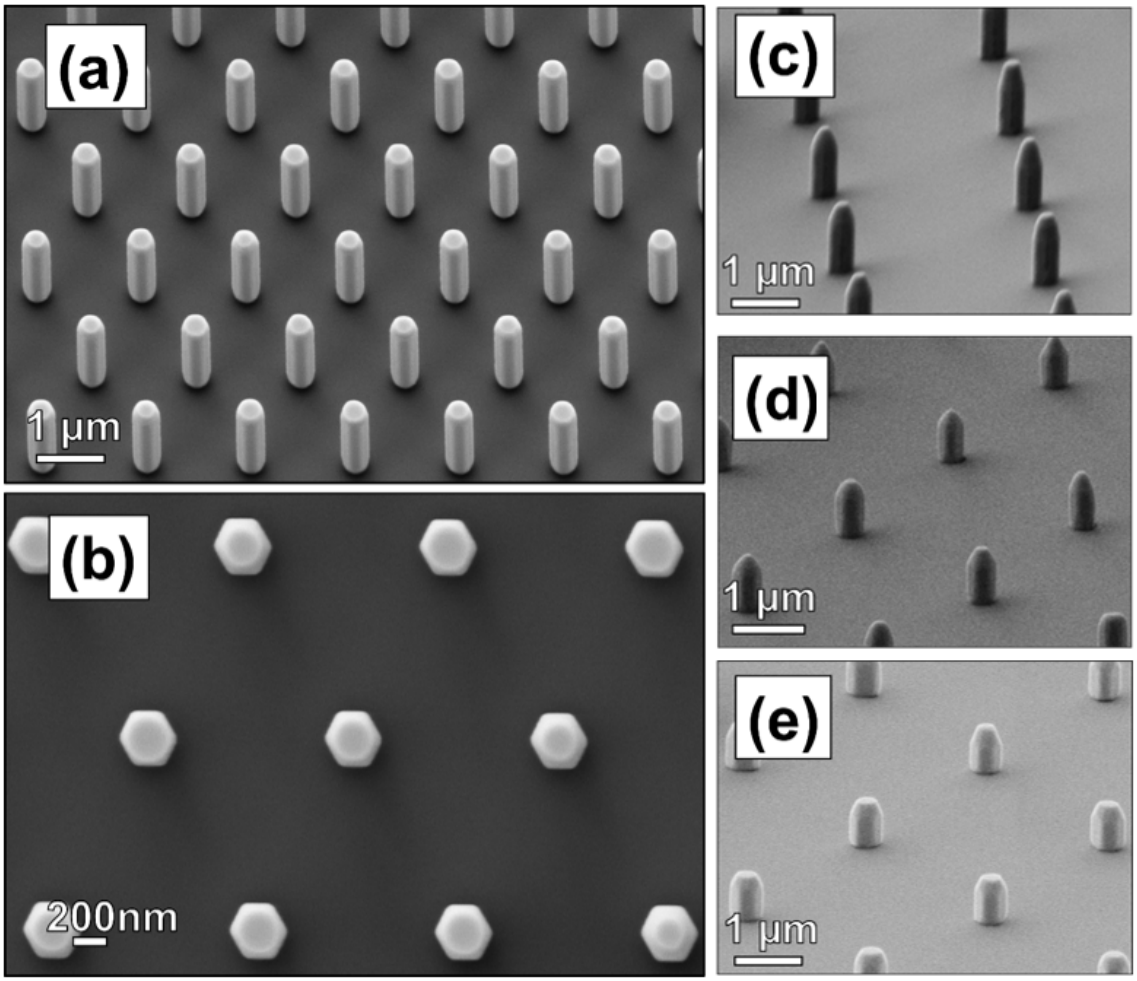

Figure 2. (a) Tilted-view and (b) top-view SEM images of well-ordered and vertically aligned GaAs NW arrays grown on Si(111) substrate under optimized growth conditions (conditions 1 in Table 1). The diameter of the circular holes is 350 nm and the pitch is 1.75 µm. Tilted-view SEM images of samples obtained under (c) conditions (2), (d) conditions (3) and (e) conditions (4) showing the morphological changes with growth conditions of GaAs NWs on patterned Si(111) substrate with 350 nm-diameter holes and a pitch of 3.5 µm.

Table 1 summarizes some growth conditions explored in this work to grow regular arrays of vertical GaAs NWs on patterned Si(111). All experiments were performed after the surface preparation described above.

Table 1. Summary of the growth conditions of GaAs NWs discussed in this work.

	Growth temperature (°C)	Partial pressure of GaCl (atm)	Partial pressure of As_4 (atm)	NW length (µm)	NW diameter (µm)	Figure
Conditions 1	785	3.3×10^{-3}	7.2×10^{-4}	1.6	0.4	2(a, b)
Conditions 2	785	3.3×10^{-3}	3.6×10^{-4}	1.0	0.4	2(c)
Conditions 3	785	1.6×10^{-3}	7.2×10^{-4}	0.7	0.4	2(d)
Conditions 4	760	3.3×10^{-3}	7.2×10^{-4}	0.6	0.4	2(e)

Figures 2 (c), (d) and (e) display examples of the evolution of GaAs NWs morphologies with the growth conditions for a fixed pattern. With respect to MBE and MOVPE, where selectivity depends on the growth temperature and the vapour phase composition[46,47], selectivity is fully ensured by HVPE regardless of the growth conditions, because of the low even null sticking coefficient of the chloride precursors on the mask. As a consequence, HVPE allows to freely study the evolution of the morphology of nanostructures as a function of a wide range of growth parameters. Under all tested growth conditions, no misoriented NWs were obtained and the NWs exhibited a pencil-like shape delimited by a (111)-top facet and six equivalent {110}-side facets (Figure 2). Nevertheless, the (111)-top facet tends to disappear when either the As partial pressure (conditions 2) or the Ga partial pressure (conditions 3) decrease, with respect to conditions 1 (at the same growth temperature of 785 °C). On the basis of convex growth rules, the fast-growing facets of a crystal disappear in favour of the slowest ones. Then, these latter slow facets define the final morphology of the micro- or nano-structure. In-depth and comprehensive studies of the evolution of the intrinsic growth anisotropy of GaAs, performed on patterned substrates of various orientations by HVPE, can be found in Refs [41–44]. The authors have shown that HVPE growth is mainly governed by surface kinetics: the kinetics of adsorption and desorption fluxes of As (reaction 2) and GaCl (reaction 3), and the kinetics of dechlorination (reaction 4). Based on these reviews, it is assumed that the growth rate of the {110} facets, which consist of rows of Ga-As, is usually very low over a wide range of HVPE conditions because of low adsorption of As and GaCl on the surface even at low growth temperature. Coming back to our present study, it can be said that the growth rate of the {110}-side facets decreases more rapidly than the growth rate of the (111)-top facet when decreasing As or Ga supply. As a result, the {110}-side facets appear and limit the NWs length.

As general trends, dechlorination is a temperature-assisted process. When decreasing growth temperature (conditions 4), the growth rates of all facets decrease, then shorter NWs are obtained. At an optimum temperature of 785 °C (conditions 1 as reference), the growth rates decrease with decreasing As supply (conditions 2) or Ga supply (conditions 3). We can observe that a decrease of Ga is more efficient in reducing the growth rates, then the length of the NWs, than a decrease of As.

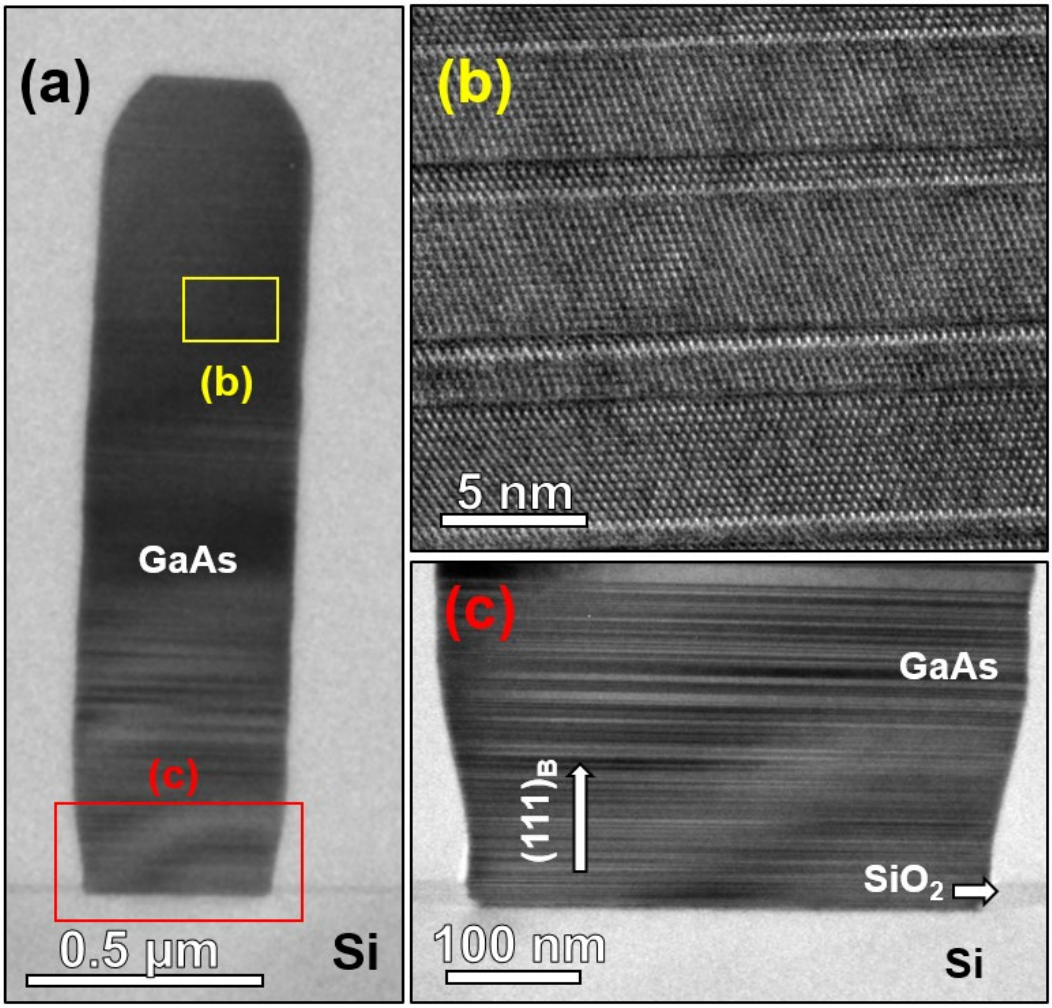

Figure 3: (a) Low resolution cross-sectional TEM image of GaAs nanowire grown on Si(111) substrate (conditions 1). (b) HR-TEM image taken from the top part of the NW showing the Zinc-Blende crystalline structure of GaAs with twinning and stacking faults. (c) HR-TEM image taken from the bottom part of the NW showing the interface with Si (patterned substrate with 350 nm-diameter hole and a pitch of 3.5 µm).

Structural characterization by HR-TEM was carried out to check the crystalline quality of the as-grown GaAs NWs grown in conditions 1. A vertical cross-section perpendicular to the [110] direction was prepared by Focused Ion Beam (FIB). In Figure 3, one can find cross-sectional TEM (a) and HR-TEM images of selected GaAs NWS taken at the top of NWs (b) and at the interface with the substrate (c). The NW diameter is about 0.4 µm with a length of 1.6 µm. High density of structural defects can clearly be found along the $[111]_B$ growth direction, in particular twinnings, as can be seen in close up in Figure 3 (b).

Polytypism is also observed at the bottom part of the NW near the substrate interface. These alternate stackings between Zinc-Blende (ZB) and Wurtzite (WZ) are commonly observed during the growth of GaAs NWs along the [111] direction. Their appearances are attributed to the small difference in the internal formation energy between the two phases, which comes mainly from the electrostatic interaction between the third-nearest-neighbor atoms [30,48,49]. Some authors have reported that the crystal phase of III-V NWs grown by a VLS process can be monitored by controlling the supersaturation in the catalyst droplet and its radius, after tuning growth conditions[50–52]. Few studies have properly shown the possible control of the crystal phase of GaAs NWs grown along the [111] direction through a VS process. Here, and according to the work of Liu et al. [53,54], the formation of structural defects is probably induced by the high partial pressure of As_4 needed to grow GaAs on Si in HVPE.

On the other hand, the morphology of the growing GaAs crystal depends heavily on the pattern. Several authors showed that the axial and radial growth rates of GaAs NWs grown by SAG-MBE or MOVPE were strongly dependent on the pitch and the collection area, as they are supplied by the diffusion of adatoms on the mask[55]. We can assume that there is almost no diffusion of ad-precursors on the mask in HVPE as they do not adsorb on dielectric surfaces at usual high growth temperature[35]. The evolution of the shape of the structures as a function of the aperture size is rather due to initial nucleation issues by HVPE. Figure 4 shows SEM images of GaAs structures grown by SAG on Si(111) substrates patterned with 500 nm-diameter holes under conditions 4. We can see a large epitaxial lateral overgrowth on the mask (at a rate of ~ 16 µm/h), so that the structures evolve into micro-platelets. The axial growth rate is slightly reduced from 2.6 µm/h to 2.0 µm/h when the aperture size increases from 350 nm (Figure 2(c)) to 500 nm (Figure 4). Such decrease of the axial growth rate of GaAs NWs with the aperture size has already been

observed[33,56]. In this study, once the aperture diameter was greater than 0.50 µm, the structures were indeed no longer hexagonal NWs, but moved to well-faceted micro-platelets in all studied growth conditions.

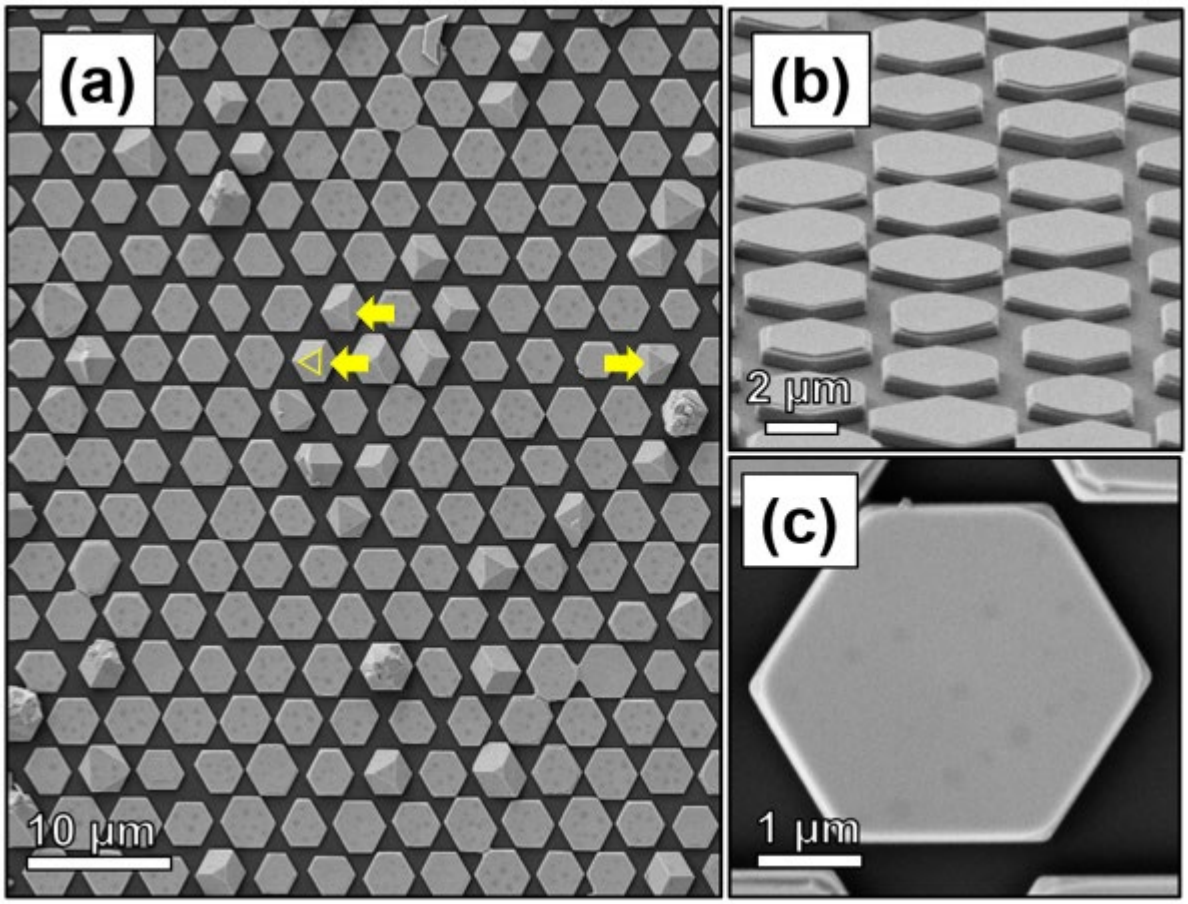

Figure 4. (a) Top-view and (b) tilted-view SEM images of hexagonal GaAs micro-platelets grown on Si(111) substrate under growth conditions 4. The arrows indicate triangular thin mesa surrounded by {−1−10} facets. (c) Closer top-view SEM image on a selected micro-platelet showing a perfect hexagonal morphology. The diameter of the circular holes is 500 nm, and the pitch is 2.50 µm.

Similar platelets were obtained on patterned GaAs$(111)_B$ substrates with 50 nm-diameter holes[30]. The growth of such structures, even at small opening diameters, was attributed to the formation of stable As-trimers following the surface reconstruction under high partial pressure of element V, thus supressing axial growth along the $(111)_B$ direction. However, the formation of stable As-trimers may not be the cause for the micro-platelets grown in this work. If As-trimers formation was involved, we would expect the micro-platelet morphology even for the substrate pattern with small 350 nm-diameter hole (where NWs are indeed grown). For Tomioka et al. [33],

the size openings determine the number of 2D islands during initial nucleation. The coalescence of these islands with rotational twins results in the generation of 3D islands. The further coalescence of the 3D islands in the large apertures (D > 600 nm) generates three-fold-symmetry as well as unexpected lateral facets. Smaller openings (D < 400 nm) promote the formation of one 2D island per aperture that stimulates the growth of hexagonal GaAs NWs. These findings are supported by Ikejri et al. through a thermodynamic model of the variation of Gibbs free energy[33]. The authors show that the transition from a tetrahedron with three-fold-symmetry facets, which corresponds to the first nucleation step, to a perfect hexagonal shape is more favourable and faster in the case of smaller openings. Larger apertures involve intermediate shapes between tetrahedral and hexagonal with twin development (as indicated by yellow arrows in Figure 4 (a)). The formation of twinning during this intermediary stage promotes the appearance of new side facets. All these trends are in full agreement with our experimental observations and sustain the transition from a perfect hexagonal wire to non-symmetrical platelet as a function of the aperture size of patterned silicon substrate.

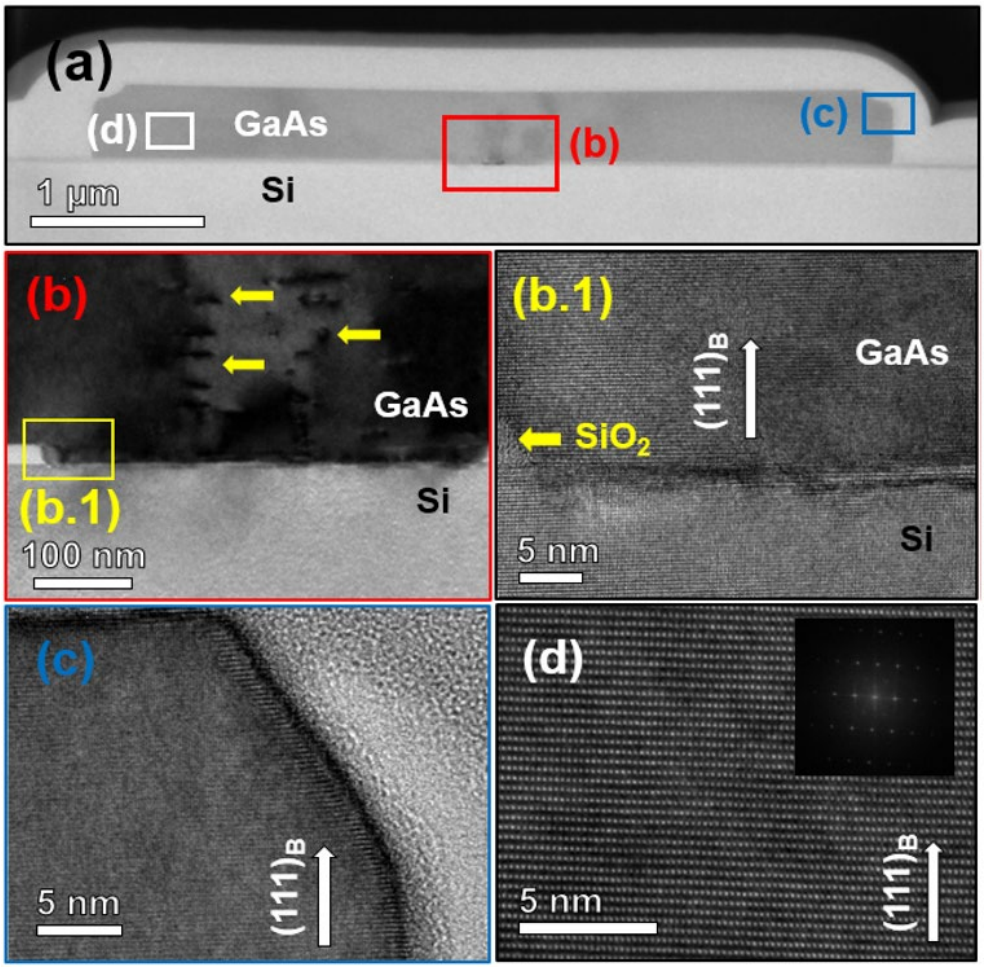

Figure 5. (a) Low-resolution HAADF-STEM investigation on the cross section of a selected GaAs micro-platelet grown on Si(111) in conditions 4. (b) Observation of dislocations located in the lower center of the GaAs structure highlighted by arrows and (b.1) High-resolution image close to the mask edge. (c) High resolution- image showing the end facets of GaAs platelet exhibiting a smooth $(111)_B$ surface. (d) High resolution image shows that the GaAs crystal is mostly defect-free. The inset is the corresponding FFT pattern of a pure GaAs ZB crystal.

Cross-sectional TEM images of a selected GaAs micro-platelet are given in Figure 5 to illustrate the crystal quality. The platelets were initially prepared by FIB for cross-sectional images in a direction perpendicular to [110]. The HR-TEM image of Figure 5 (b) taken in the opening area reveals the presence of few structural defects, such as dislocations, as indicated by the yellow arrows. Such defects can appear after coalescence of different GaAs islands, which nucleate predominantly at the aperture edges exhibiting different level of strain relaxation. The contrast formation in the Figure 5 (b) could be attributed to dislocations formed upon the merging of the initial nanowire seeds within the aperture. The interface between the GaAs platelet, the Si substrate

and SiO_2 mask exhibits a good crystalline quality, confirming that direct epitaxy was achieved. The entire crystal is ZB and otherwise free of crystalline defects (see Figure 5 (c) and 5 (d)). To our knowledge, this is the first demonstration of such regular and high-quality GaAs micro-platelets grown using HVPE on Si. PL measurements were performed to further confirm the optical quality of both GaAs NWs and micro-platelets grown on Si. Figure 6 depicts representative PL emission spectra of GaAs micro-platelet (red curve) and GaAs NW (blue curve) recorded at low temperature (10 K). Compared to NWs, the micro-platelets exhibited significantly higher PL intensity as expected due to their larger volume and good crystalline quality. It is further seen that the emission peak of micro-platelets is centered around 1.49 eV which is slightly lower than the excitonic emission in bulk GaAs (1.51 eV) [57], whereas two peaks around 1.51 eV and 1.49 eV are observed in the case of NWs. The peak position near 1.49 eV corresponds to neutral donor to neutral carbon acceptor (D_0, C_{As}) emission as reported in reference[58]. These acceptors may probably be due to non-intentional carbon incorporation[19,59]. Indeed, organometallic p dopants used in HVPE setups induce a residual carbon level. As C can act as an acceptor in GaAs, this suggests that the GaAs material contains a density of free-holes, which means that the GaAs material is potentially unintentionally p-type. The reason why the platelets do not exhibit the excitonic peak may be that they present a higher C doping level than the NWs. In fact they exhibit a larger GaAs(111)B surface with respect to their volume compared to the NWs. GaAs(111)B surfaces are known to incorporate C atoms more easily than the other GaAs facets[60]. More detailed PL measurements will be published in a forthcoming publication.

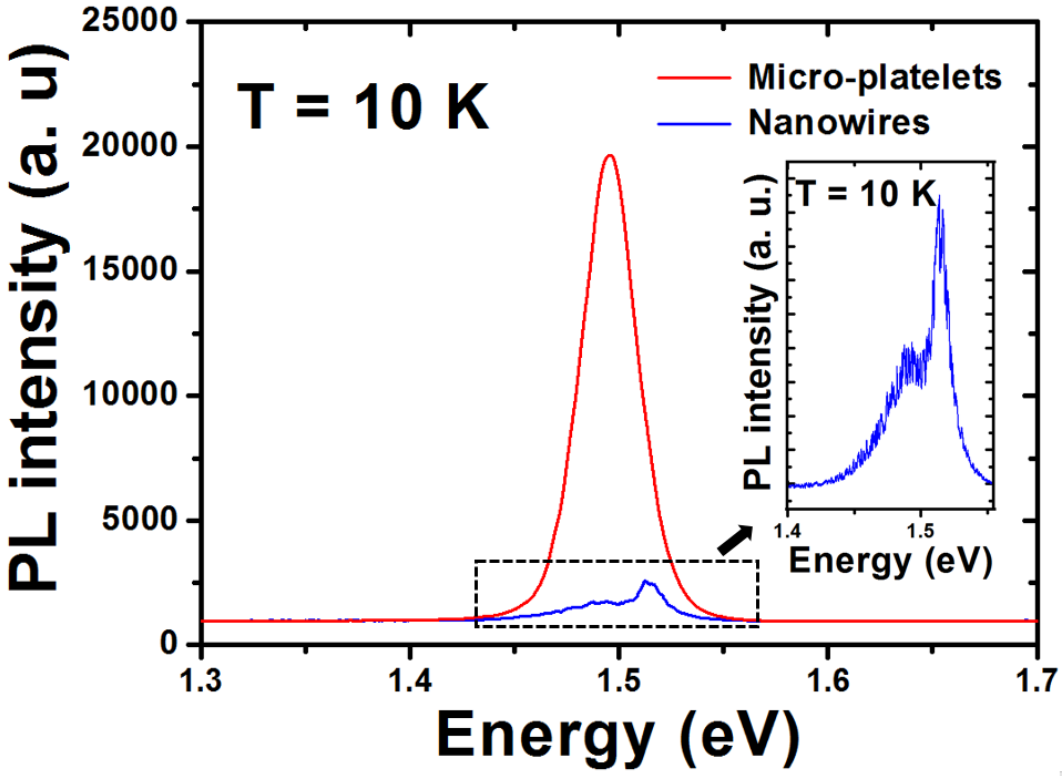

Figure 6. Low temperature (10 K) PL spectra of GaAs nanowires (in blue) and micro-platelets (in red) arrays grown on silicon substrate.

4. Conclusion

We have demonstrated the selective growth of arrays of well-oriented GaAs NWs directly on masked Si(111)substrates. The NWs were grown along the $(111)_B$ direction and exhibited hexagonal shapes. A Si(111) surface preparation under a high partial pressure of As_4 is needed to ensure direct condensation of GaAs on Si. The growth mechanisms were identified and the control of the shape of the NWs as a function of the experimental growth parameters and mask pattern was discussed. The NW morphology is promoted at smaller aperture diameter ($D < 350$ nm), while larger apertures ($D \geq 500$ nm) result in the formation of regular arrays of GaAs micro-platelets with ZB crystalline quality. Overall, HVPE of III-Vs is a promising method for selective area growth on silicon which stands out compared to MBE and MOVPE due to its exceptional selectivity, high growth rates and low cost.

Author contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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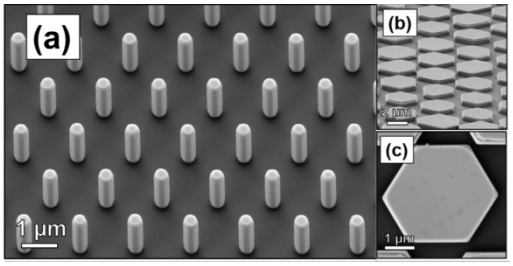
Selective Area Growth of GaAs Nanowire and Micro-Platelet Arrays on Silicon by Hydride Vapor Phase Epitaxy

TOC graphic



Synopsis

The growth of vertically-oriented GaAs nanowires (NWs) and micro-platelets on patterned SiO_2/Si(111) substrate by hydride vapor phase epitaxy (HVPE) is demonstrated. It is achieved through a surface preparation under As-controlled atmosphere. $<111>_B$ oriented GaAs NWs are obtained when the hole diameter (D) in the SiO_2 mask is below 350 nm. Micro-platelets are obtained in larger apertures ($D \geq 500$ nm).