Decoupling the dark count rate contributions in Ge-on-Si single photon avalanche diodes

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ABSTRACT

Single Photon Avalanche Diodes (SPADs) are semiconductor devices capable of accurately timing the arrival of single photons of light. Previously, we have demonstrated a pseudo-planar Ge-on-Si SPAD that operates in the short-wave infrared, which can be compatible with Si foundry processing. Here, we investigate the pseudo-planar design with simulation and experiment to establish the spatial contributions to the dark-count rate, which will ultimately facilitate optimisation towards operation at temperatures compatible with Peltier cooler technologies.

Keywords: Single photon avalanche diode, Ge-on-Si, device simulation, Si Photonics

1. INTRODUCTION

There has recently been significant interest in Single Photon Avalanche Diodes (SPADs) operating at short-wave infrared (SWIR) wavelengths, with applicability to numerous emerging applications such as Geiger mode LiDAR,[1] imaging through obscurants,[2,3] Quantum-Key Distribution (QKD)[4] and quantum information processing.[5] Previously, we have demonstrated Ge-on-Si SPADs with a pseudo-planar design[6] that enabled single photon counting up to 175 K[7] and demonstration of LiDAR at 1450 nm wavelength.[8] This is a technology that has the potential to benefit from Si foundry compatibility and can therefore be significantly lower cost than III-V devices such as InGaAs/InP SPADs. The Ge-on-Si platform also has the benefit of reduced afterpulsing compared to InGaAs/InP devices (when operated in nominally identical conditions),[9] due to the use of high quality Si avalanche layers with low defect densities compared to InP, which can ultimately enable operation with high repetition rates. In order to reduce the dark-count rate (DCR) in our devices, significant cooling was required to reduce thermally generated carriers, and as such devices have performed optimally at cryogenic temperatures. To be competitive with InGaAs/InP however, devices need to be operational at $\sim$ 220 K, where low-cost Peltier cooler technology can be used. In order to facilitate this optimisation, DCR of the devices has to be reduced. Previous results have indicated that scaling the technology can reduce the DCR,[7] and that a reduction in the bulk E-field in the Ge can further reduce the effects of trap-assisted tunneling.[10] In this work, we compare simulation and experimental results to decouple the dark-count rate contributions in the pseudo-planar design to validate the device dynamics, and to understand the geometric considerations of the detector design that may also contribute to DCR.

2. BACKGROUND

For a number of years, Ge-based absorber layers have been investigated to extend the absorption wavelength of Si SPAD technology to the short-wave infrared, in separate absorption charge and multiplication structures (SACM).[11–13] In SACM structures, a charge-sheet layer is typically required to mediate the electric field, ensuring that the multiplication region (in this case Si) can be biased above breakdown, while keeping only a moderate E-field in absorber layer designed to sweep out photo-generated carriers. Previously, Ge-on-Si SPAD devices used

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in-situ doped charge-sheet layer that extended across the wafer structure,[12] and the device was defined entirely by an etch step, i.e. a mesa geometry. Such designs typically have a high electric field at etched sidewalls and can suffer from effects such as preferential edge breakdown. In recent years, we have demonstrated a pseudo-planar design, where the charge-sheet layer is locally implanted using ion-implantation prior to the growth of Ge absorber layers. This local charge-sheet layer, in conjunction with a local etch of the p+Ge contact layer, reduces the E-field at etched sidewalls, Fig 1a, which are required for lateral device isolation. This design yielded single photon detection efficiencies (SPDEs) of up to 38 % at $\lambda = 1310$ nm,[6] and a noise equivalent power (NEP) down to 7.7 $\times 10^{-17}$ $W/\sqrt{Hz}$; over a two order of magnitude improvement compared to a similarly sized mesa device.[14] Here we use device simulation techniques, as well as varying passivisation techniques to probe the role of the device sidewalls, and validate if the surfaces have indeed been fully decoupled from the active area of the device.

3. SIMULATION

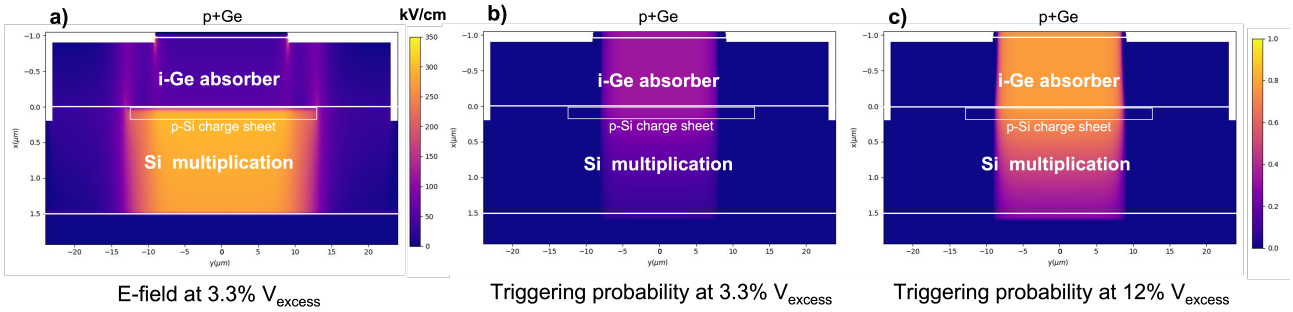

Figure 1. a) Simulated E-field of a pseudo-planar Ge-on-Si SPAD. b,c) Corresponding triggering probability maps calculated using McIntyre's model for varied excess bias (V_{excess}).

Initially, pseudo-planar geometry designs were simulated using finite element modelling packages. As shown in Fig 1a, there is a reduced E-field at the sidewall and the field is localised by the charge-sheet layer and p+Ge contact layer. From E-field analysis alone, however, it is challenging to gain an insight into the dominant aspects of the design in defining the DCR contributions. In order to assess this more accurately, we use custom python code to solve McIntyre's equations[15] along E-field lines, in order to produce a triggering probability map, Fig 1b, which indicates the probability that a carrier generated at a given point will produce a self-sustaining avalanche current. The model, unlike a Monte Carlo approach, does not take into account the motion of individual carriers, and can therefore slightly underestimate the width of the triggering probability region,[16] however it is significantly less computationally intensive than Monte Carlo approaches, and has been used extensively to give good agreement with experiments across multiple material platforms.[17–19] It is clear that in the pseudo-planar geometry, the p+Ge diameter appears to dominate when defining the active region of the detector, with slight broadening observed at increased excess bias, Fig 1c. This simulation suggests that any carriers generated on etched sidewalls should not contribute to DCR.

4. EXPERIMENT AND RESULTS

In order to assess this experimentally, we compare the DCR performance of SPAD chips with varying surface passivation, using devices fabricated in the James Watt Nanofabrication Centre. Both chips used material from the same wafer, which included ion-implanted charge-sheet layers, and a 1.5 μm thick i-Si multiplication layer and a 2 μm thick Ge absorber (processing and material details can be found in[6,7,20]). The devices compared here have a charge-sheet diameter of 50 μm. Standard electron-beam and photo-lithography techniques were used for fabrication of devices, a schematic for which can be seen in Fig 2a. Isolation trenches are etched 10 μm away from the edge of the charge-sheet prior to oxidation of the Ge surface. A Si_3N_4 layer is used to cap the GeO_x layer, while simultaneously closing over the trench to planarise the structure. The first device was passivated using a

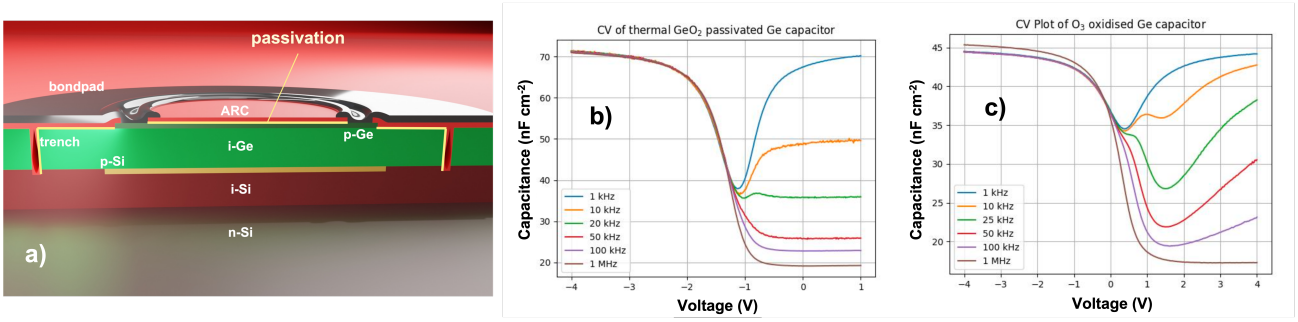

Figure 2. a) Schematic of SPAD device showing the region of the detector that is passivated. b,c) Capacitance-voltage measurements of the thermally oxidised and ozone oxidised MOS capacitors respectively.

thermally grown GeO_2 technique that has previously demonstrated effective passivation of Ge surfaces,[21] while the second device variant uses a room temperature ozone tool to oxidise the Ge surface. Capacitance-voltage (CV) measurements were taken using Ge MOS capacitor structures with these respective dielectric layers; the results of which are shown in Fig 2b,c. It is clear that particularly for the ozone passivated surface, there is increased frequency dispersion and the presence of distinctive 'bumps' in the CV curve going from accumulation to depletion, which are indicative of a high level of mid-gap trap states.

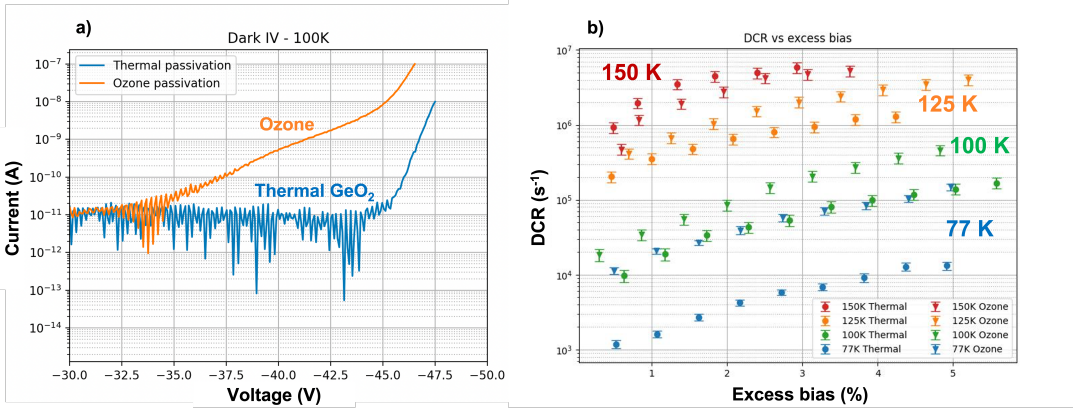

Figure 3. a) Current-voltage measurement of SPADs with varying passivation. b) Dark-count rate of SPADs with varying passivation for multiple measurement temperatures.

Devices were subsequently measured in a cryogenic probe station at the University of Glasgow including current voltage (IV) and DCR measurements. Dark-count rate measurements are taken using a gated technique; devices are biased below breakdown using an source measurement unit (SMU) and an electrical gate is AC-coupled through a bias-tee from a pulse-generator. An electronic counter with a trigger threshold is used to measure the fraction of gates that trigger, allowing the calculation of DCR. DCR results are plotted as a function of excess bias, which is the percentage bias above the breakdown voltage, V_{BD}. As shown in Fig 3a, IV results demonstrate significantly higher leakage from the ozone passivated SPAD compared to the thermally oxidised device, which is consistent with CV results and indicative of a sidewall leakage mechanism. When examining the DCR, Fig 3b, there is discrepancy in the DCR, which is particularly evident at 77 K with $\sim$ 1 order of magnitude difference shown. The discrepancy, however, is always substantially less than suggested by the leakage comparison. Furthermore, when measuring at 150 K the results are significantly closer between the two device variants, with overlapping DCR at higher excess biases. In order to further decouple the surface contributions, a further experiment was run using thermally oxidised devices with a varied buffer space, defined as the distance between the implanted charge-sheet layer and the etched isolation sidewall, Fig 4a. The corresponding DCR

is shown in Fig 4b, for devices with a 10 μm and 20 μm buffer size respectively. It can be observed that the DCR is extremely consistent between both devices, highlighting the negligible contribution of the etched sidewall and validating the effects of the pseudo-planar design. Unfortunately, device failure prohibited further measurements at lower temperatures and this will be measured in future work. The extreme similarity of the devices with varying buffer size does however imply that the difference in DCR for varied surface passivation likely stems from the top surface of the device. Carriers generated at the top surface are in an un-depleted p-doped Ge region, and therefore collection of such carriers into the device active area are limited by diffusion of electrons. It is suggested here that the observed difference in the DCR between devices with varying passivation is therefore due to carriers that can diffuse from the surface above the p+Ge region; this is consistent with a larger discrepancy at lower temperatures due to the fact that diffusion lengths can increase with lower temperatures.

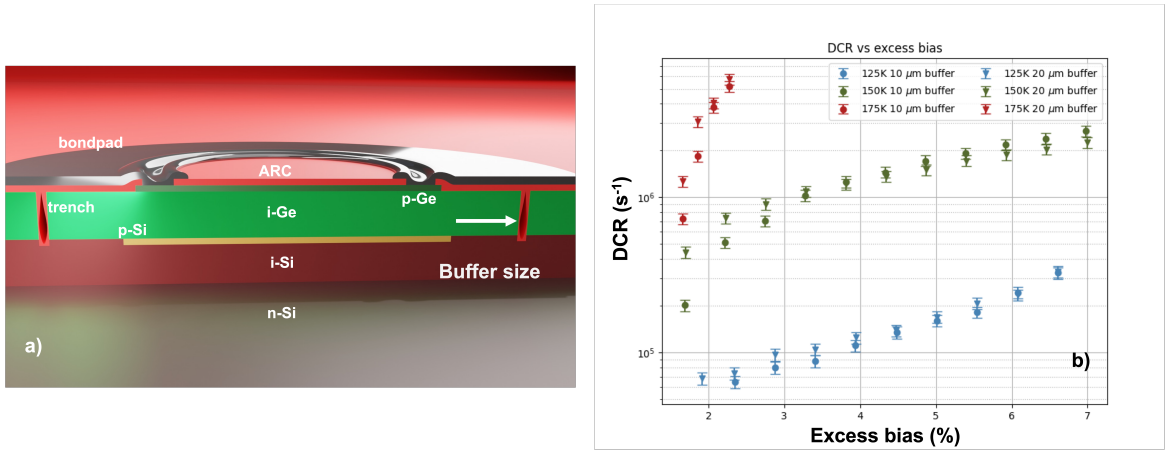

Figure 4. a) Schematic of psuedo-planar SPAD highlighting the buffer dimension, i.e. the distance between the edge of the charge-sheet and the isolation etch. b) Dark-count rate for devices with 10 and 20 μm buffer sizes respectively.

5. CONCLUSION

We have investigated the pseudo-planar design for Ge-on-Si SPADs, with an aim of understanding the device dynamics and the spatial contribution to DCR. Experimental results have demonstrated that we have successfully decoupled the the active area of the SPAD from etched sidewalls, highlighting that further optimisation of the passivation layer is unlikely to aid in a significant reduction in DCR. These results are therefore consistent with the McIntyre model but suggest that the use of a Shockley-Read-Hall generation rate model alone is not sufficient to calculate DCR accurately at low temperatures,[22] and that diffusion currents need to be included from finite element models. In future work, a larger range of buffer gaps will be investigated with an aim of maximising fill-factor in arrays, while maintaining an effective decoupling of sidewalls from the device active area, which will in turn give an insight into the diffusion lengths at low temperatures. Furthermore, measurement of SPDE is required with time-correlated single-photon counting experiments to provide a complete analysis. Further device optimisation will include a detailed investigation into the relative scaling of the p+Ge and implanted charge-sheet layers. Preliminary results indicate there is a complex interplay between these layers that influences the screening of E-field hot-spots in the p+Ge region, which through simulation appear to be capable of overlapping with the triggering probability region at higher excess biases when using McIntyre's model. The accurate modelling of E-fields around etched surfaces can be challenging and therefore this will be evaluated experimentally. The insights gained from these experiments, and the results demonstrated here, will aid the optimisation of the technology towards operation at 220 K for compatibility with low-cost Peltier coolers.

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