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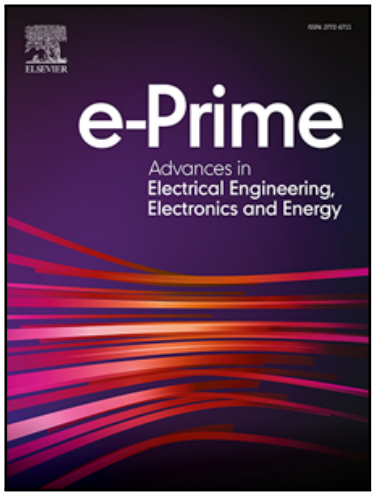

A 3.2-3.8 GHz Low-Noise Amplifier for 5G/6G Satellite-Cellular Convergence Applications

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A 3.2-3.8 GHz Low-Noise Amplifier for 5G/6G Satellite-Cellular Convergence Applications

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Abstract

The rapid evolution of wireless communication systems towards 5G standards has imposed stringent requirements on the performance of radio frequency front-end components. Among these, the Low-Noise Amplifier (LNA) plays a pivotal role in determining the overall noise figure and sensitivity of the receiver chain. This paper presents a comprehensive design and analysis of a 3.2-3.8 GHz LNA tailored for 5G applications, employing a 0.3 µm gate length Gallium Arsenide (GaAs) pseudomorphic high electron transistor (pHEMT) technology process. The proposed LNA design focuses on achieving a low noise figure (NF), high gain, and robust linearity to accommodate the dense signal environment and wide bandwidth of 5G networks. The design leverages advanced matching networks and feedback topologies to enhance stability and reduce the noise contribution from the active devices. Simulation results predict a noise figure of 1.3-1.4 dB, a gain of 20-21 dB across the band of interest, and an input-referred third-order intercept point (IIP3) of 18 dBm. The LNA demonstrates excellent performance in a 5G testbed, showing a significant improvement in the signal-to-noise ratio and the potential to enhance 5G receiver sensitivity. The research substantiates the LNA's viability for integration into 5G base stations and user equipment, underscoring its potential to contribute to the efficient and reliable operation of next-generation wireless networks. This LNA can be used for 5G New Release (NR) band of n77 and n78 (3.5-3.7 GHz)

Keywords: 5G, Low-Noise Amplifier, Radio Frequency, Noise Figure, Linearity, Wireless Communication.

1. Introduction

The advent of the fifth generation (5G) of wireless communication systems represents a paradigm shift in the way data is transmitted and received, promising unprecedented data rates, reduced latency, enhanced reliability, and increased network capacity [1]. As a cornerstone of this new era, the radio frequency (RF) front-end plays a critical role, where the performance of its components is pivotal in achieving the overall system's objectives [2], [3]. Among these components, the Low-Noise Amplifier (LNA) is of particular importance, serving as the first amplification stage in the receiver chain [4], [5]. It amplifies the received signal while minimizing the addition of noise, which is crucial in a high-density signal environment where maintaining signal integrity is paramount [6], [7], [8], [9].

The 3.2-3.8 GHz range, falling within the C-band spectrum, is strategically significant for next-generation wireless networks. This band strikes a balance between wide coverage and high data throughput capabilities, making it ideal for applications that require both extensive reach and high-speed data transmission. As the global telecommunication paradigm shifts towards a seamless integration of terrestrial and non-terrestrial networks, the importance of this band has escalated, necessitating the development of specialized RF components that can operate efficiently within this range. This frequency range offers a balance between coverage and capacity, serving as a key enabler for wide-ranging 5G applications [10], from enhanced mobile broadband (eMBB) to massive machine-type communications (mMTC) [11], [12], [13]. However, designing LNAs that operate effectively at these frequencies necessitates meticulous consideration of noise performance, linearity, and power efficiency [14], [15].

Designing an LNA that caters to the specific requirements of 5G/6G satellite-cellular convergence presents a set of unique challenges. These include ensuring wideband operation, high linearity, low power consumption, and integration compatibility with existing system architectures. Innovations in semiconductor technology, circuit design, and manufacturing processes are imperative to address these challenges. For instance, with the advent of post-quantum cryptography designed to secure cryptographic algorithm against an attack by a quantum computer, more processing power and bandwidth due to their complex mathematical structures compared to traditional cryptography is required [16]. This could indirectly affect LNA-related systems if the increased computational load or altered signal characteristics impact the

design parameters or operational requirements of communication systems, particularly in terms of bandwidth and signal processing capabilities [17], [18]. The authors in [19] and [20] however caution against relying solely on AI-generated codes for security-critical applications without proper vetting by cryptographic experts. Furthermore, 5G networks utilize network slicing to allocate resources dynamically, necessitating flexible and secure methods for authentication and access control. PQC provides a robust framework for securing these dynamic networks against sophisticated quantum and classical attacks [18]. The ideal LNA design for this application would therefore need to leverage cutting-edge materials, sophisticated design methodologies, and advanced fabrication techniques.

This paper introduces a novel LNA design optimized for operation at 3.2-3.8 GHz, aiming to meet the stringent requirements of emerging 5G applications [21], [22]. The proposed design is crafted using gallium arsenide (GaAs), which is known for its high electron mobility and low noise characteristics, making it an ideal choice for high-frequency amplifiers [23]. The LNA leverages advanced impedance matching techniques, feedback structures, and stability enhancements to deliver superior performance [24]. Through this work, we address the inherent trade-offs between noise figure (NF), gain, and linearity, which are intensified by the high frequency and wide bandwidth demands of 5G signals [25], [26], [27], [28].

We begin by reviewing the current landscape of LNA designs for 5G applications, discussing the limitations of existing approaches and the necessity for advancements in noise reduction and efficiency. Subsequently, we elucidate the methodology adopted for the LNA design, emphasizing the simulation models used and the rationale behind component selection [29]. The incorporation of noise-reduction techniques [30], [31], such as the use of high-Q inductors and optimised transistor sizes, is also explored [32], [33], [34].

In detailing the design process, we highlight how the LNA achieves a balance between low NF and high gain without compromising on linearityan essential characteristic for handling the complex modulation schemes used in 5G [35], [36], [37], [38]. Furthermore, we discuss the LNA's power consumption considerations, an aspect critical for battery-powered devices and sustainable network deployments [39].

The design's novelty is accentuated by its emphasis on integration compatibility, ensuring that the LNA can be incorporated into diverse 5G hardware platforms, including base stations, repeaters, and user equipment. The work presented here underscores the LNA's adaptability to various opera-

tional scenarios in 5G networks, ranging from urban to rural deployments, and its potential to bolster the network's robustness against interference.

The remainder of this paper is structured as follows: Section II outlines the proposed LNA design methodology, in the domain of LNA designs for 5G. Simulation results and discussions are presented in Section III, and the paper concludes in Section IV.

2. Design Methodology

The primary objective of the LNA design was to achieve a low noise NF while maintaining a high gain and satisfactory linearity across the 3.5 GHz frequency range [40]. To align with the 5G new radio (NR) standards, the LNA was required to support a 500 MHz bandwidth, with a target gain of 20-22 dB and a noise figure below 2 dB. Linearity, measured by the third-order intercept point (OIP3), was targeted to be better than 18 dBm. Additional considerations included power consumption, as lower power draw is critical for portable and remote applications.

The Advanced Design System (ADS) stands at the forefront of electronic design automation (EDA) software, offering a sophisticated suite of tools for the simulation and optimization of electronic systems. Recognized for its prowess in addressing complex design challenges, ADS provides an integrated platform that supports a wide range of activities, from schematic capture to full-wave electromagnetic simulations.

In our paper, ADS played a pivotal role in both the design phase and the simulation of the LNA's performance. By leveraging ADS's comprehensive environment, we were able to meticulously model the LNA's behaviour under various operational conditions, ensuring that our design met the stringent requirements necessary for 5G applications.

2.1. Technology Selection

The 0.3 µm gate length GaAs pHEMT technology by Agilent Technologies was chosen for its excellent high-frequency characteristics and noise performance following a comparative examination of the various semiconductor technologies. It can function at frequencies that are far greater than what silicon-based transistors can achieve. It demonstrates intrinsically low noise performance, which is essential for amplifying weak received signals without substantially increasing the amount of noise. This technology is chosen because:

- GaAs pHEMT Technology: pHEMT technology, leveraging the high electron mobility of Gallium Arsenide, is renowned for its excellent high-frequency performance. The 0.3 m gate length in these transistors allows for operation at very high frequencies, which is essential in various applications like telecommunications, radar, and defense systems.

- 0.3 m Gate Length Advantages: The shorter gate length translates to faster electron transit times, which is crucial for high-speed and high-frequency applications. It enables the device to operate with higher efficiency and lower noise figures at frequencies that are challenging for standard silicon-based technologies.

- Applications in RF and Microwave Systems: Agilent's GaAs pHEMTs are particularly suitable for Radio Frequency (RF) and microwave applications. They can be used in components such as Low Noise Amplifiers (LNAs), power amplifiers, oscillators, and mixers, which are integral to systems in satellite communications, radar, and advanced wireless networks.

- Advantages Over Silicon-Based Technologies: The GaAs pHEMTs offer several advantages over silicon-based transistors, including higher electron mobility, better noise performance at high frequencies, and greater resistance to radiation - a critical factor in space applications.

2.2. Circuit Topology and Component Selection

The circuit topology chosen for the LNA was a common-source configuration with inductive degeneration for optimal noise performance. A nonlinear model of the 0.3 µm GaAs pHEMT was utilized, with its parameters extracted from foundry data. Passive components were designed to balance quality factor and size, employing RF MEMS, transmission lines for tunability and integration. Fig. 1 shows the schematic of the designed two-stage LNA.

From Fig. 1, $C1$ and $C8$ serve as coupling capacitors, thus preventing the transmission of any direct current (DC) voltage originating from the supply voltage. These capacitors serve the purpose of preventing distortion of the RF signal caused by the presence of DC voltage. Bypass capacitors, denoted as $C2$, $C3$, $C4$, $C6$, $C7$, and $C9$, are employed for the purpose of grounding AC signals, hence eliminating any AC noise that could be present in a DC

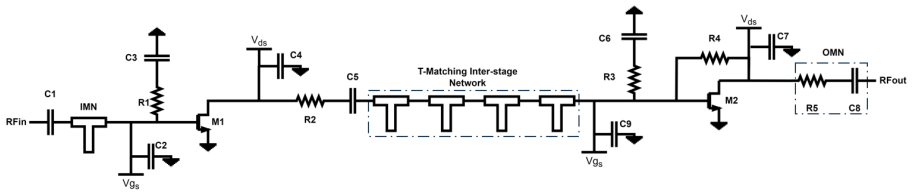

Figure 1: Two-stage schematic of the LNA and corresponding key components

transmission. Capacitors $C3$ and $C5$ are also incorporated for stability of the LNA overall system.

Stability considerations were paramount, given the potential for oscillations at high frequencies. Stability analysis was conducted using the k-factor and mu-factor methods, ensuring unconditional stability throughout the operating bandwidth. Bias networks were designed to set the quiescent point for optimal NF and linearity, incorporating self-biasing for temperature and process compensation. Resistor $R2$ is added at the output of the first stage transistor to increase the stability of the active device.

The Low-Noise Amplifier (LNA) operates at the frequency range of 3.2-3.8 GHz in the electromagnetic spectrum. The design characteristics, including forward transmission gain, minimum noise figure, S-Parameter extraction, noise resistance, input and output isolations, were acquired under certain bias conditions.

The bias gate-source voltage, V_{gs}, was set to -0.4 V, while the drain-source voltage, V_{ds}, was set to 3 V. The centre design frequency observed in this particular design was determined to be $f_d = 3.5$ GHz. MIM capacitors find application in several areas such as DC blocking, RF bypassing, and system matching networks.

Fig. 2 shows the simulated maximum stable gain (MSG) and NFmin versus bias voltages for a single transistor at 4 V (Sky blue), 3 V (Pink), 2 V (Blue) and 1 V (Red). Maximum Stable Gain (MSG) is a parameter used in electronics, specifically in the design and analysis of amplifiers and radiofrequency (RF) circuits. MSG, or Maximum Stable Gain, is a quantitative measure of the maximum attainable amplification that may be achieved from a device, such as a transistor, while it is working in a linear and stable manner. Ensuring stability is crucial to prevent oscillation or instability when the circuit is run at its full potential gain. A very important parameter in electronics and telecommunications is the Minimum Noise Figure (NFmin).

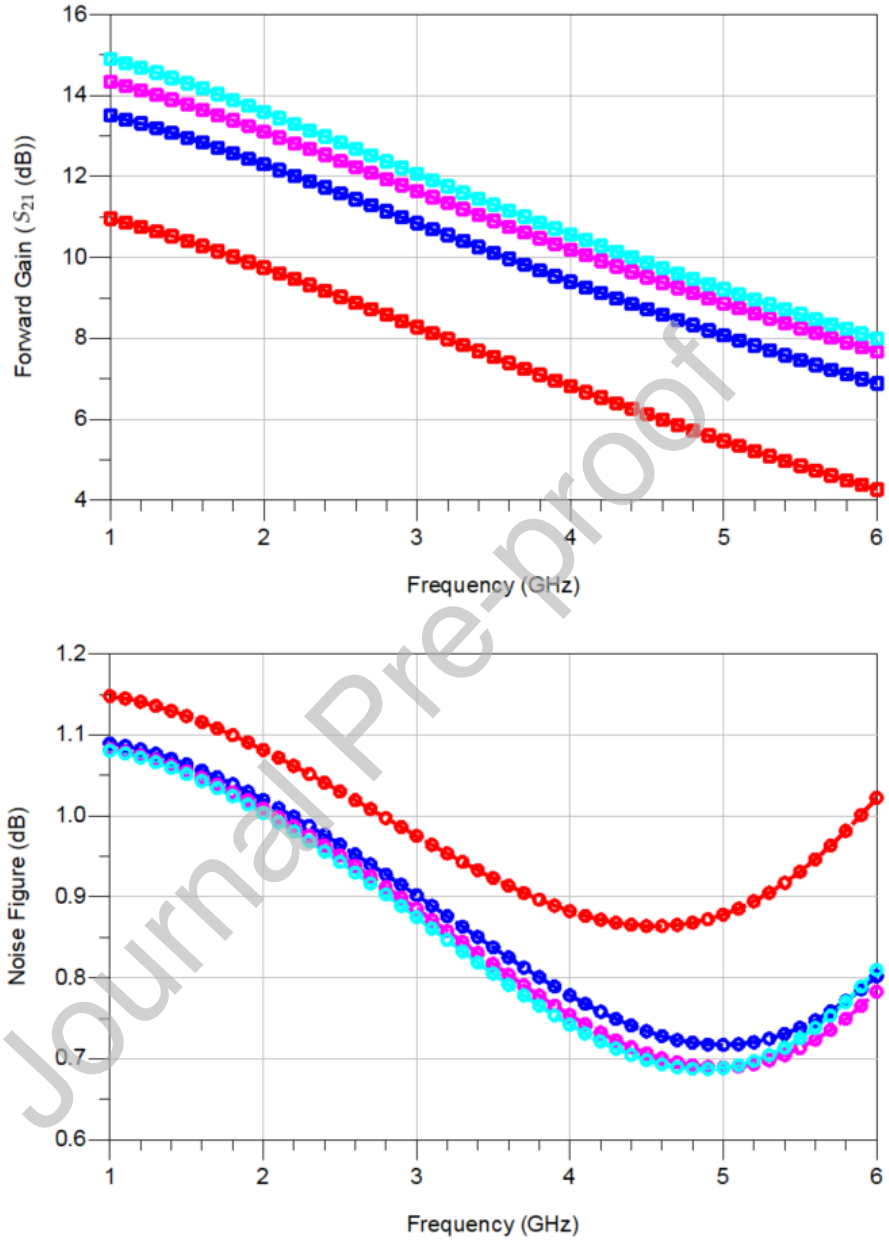

Figure 2: Simulated maximum stable gain (MSG) and NFmin versus bias voltages for a single transistor at 4 V (Sky blue), 3 V (Pink), 2 V (Blue) and 1 V (Red)

This is the lowest achievable noise figure of a device (like an amplifier) under optimal impedance matching conditions. It represents the best possible noise performance of the device.

- Stage one: The first stage transistor output is balanced with a resistor for stabilisation. This drives the optimum noise match closer to the optimum gain match, presenting the optimum match, Γ_{opt} over the operating frequency to the gate of the first stage transistor with a 50 Ω input source.
- Stage two: The second stage interstage matching network was designed to transform the output impedance of stage one transistor to the input impedance of the second stage transistor for maximum stable gain. Resistive feedback between the input and output of the second stage transistor is introduced for gain flatness [41].

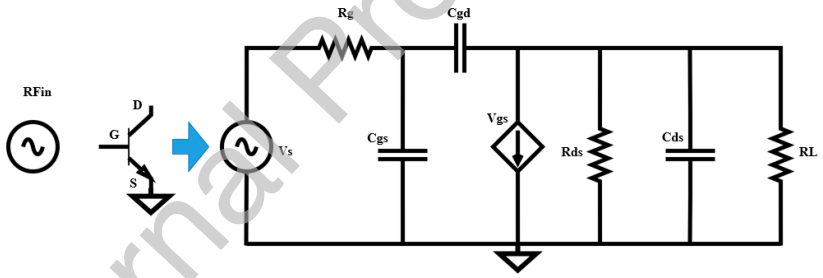

Figure 3: The small-signal equivalent circuit of the common source amplifier.

2.3. Impedance Matching

The input and output matching networks were designed to achieve conjugate matching at the centre frequency of 3.5 GHz, utilizing a combination of microstrip lines and reactive components. The Smith chart and EM simulations were used to optimize the impedance for minimal reflection and maximum power transfer. The transmission line matching network is used to obtain noise and input matching simultaneously [42]. From Fig. 1, the RF signal is transmitted by the inter stage blocking capacitor, $C5$.

Fig. 3 displays the small-signal circuit model that corresponds to the common-source amplifier [43]. The gain roll-off characteristic of transistors plays a significant role in determining the bandwidth of the amplifier [44], [15], [8]. The utilisation of a common-source technique is employed to provide substantial amplification across a broad range of frequencies. The non-uniform gain in broadband due to the gain roll-off of the transistor is deemed undesirable in the construction of a broadband LNA. Authors in [43] examined the impact of gate-drain parasitic capacitance (C_{gd}), source-drain parasitic capacitance (C_{ds}), and gate-source parasitic capacitance (C_{gs}) using the small-signal equivalent circuit model of the common-source amplifier.

The parasitic capacitance, C_{gd} is expressed as:

$$Z_{gd} = \frac{1}{j\omega C_{gd}} \tag{1}$$

where ω is the angular frequency. The parameter C_{gd} gives rise to a feedback mechanism that connects the output to the input, hence influencing the reverse isolation as the frequency increases [43], [45]. The drain current, denoted as i_{ds}, may be mathematically represented by applying Miller's theorem:

$$i_{ds} = g_m i_s \frac{1}{j\omega(m_1 C_{gd} + C_{gs})} \tag{2}$$

where i_s is the input current, g_m is the transconductance of the transistor, M1, and m_1 is the Miller multiplication factor.

For the interstage matching, a series T-matching network is used (Fig. 1) for both stability and a wideband realization.

2.4. Noise Characterisation and Reduction Techniques

Noise is a significant parameter in microwave design that serves as a metric for evaluating the quality of a system [46]. It refers to the presence of an undesirable signal introduced by various components within the system, resulting in a degradation of the performance of transmitted signals. The semiconductor device is subject to three primary forms of noise, namely thermal noise, shot noise, and flicker noise.The noise figure, denoted as F, serves as a key metric for characterising the performance of a system. It quantifies the relationship between the signal-to-noise power ratio at the input and the signal-to-noise power ratio at the output.

$$F = \frac{S_i/N_i}{S_o/N_o} \tag{3}$$

To determine the noise figure of the cascaded system, we rely on the performance matrices of the LNA, mixers, and oscillators located at the front-end of the receiver, as per the noise coefficient formula. The formula for the noise figure can be explained as follows:

$$F = \frac{P_{N_o}}{P_{N_i} G_A} \tag{4}$$

The variables P_{N_o}, P_{N_i}, and G_A represent the total available noise power at the output of the amplifier, the total available noise power at the input of the amplifier, and the available power gain, respectively. The expression for the overall noise figure of a multistage amplifier system is given by:

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} + \frac{F_3 - 1}{G_{A1} G_{A2}} + \ldots + \frac{F_n - 1}{G_{A1} G_{A2} \ldots G_{A(n-1)}} \tag{5}$$

In order to mitigate the effect of noise, the design implemented an optimal noise match network and optimised the device dimensions to get the lowest possible noise figure using transmission lines. Considerable emphasis was placed on optimising the physical arrangement in order to mitigate the adverse impacts of parasitic phenomena and cross-coupling.

2.5. Link Budget Simulation Parameter

5G/6G Satellite-Cellular Convergence depends on the Link Budget design parameters (Table 1) for seamless transmission of information [36]. A radio link budget based on theoretical assumptions is presented in Table 1 showing system design parameters and requirement used for simulation of 5G/6G satellite-cellular convergence.

3. Simulation Results and Discussion

A summary of the designed LNA performances is given in Table 2. The LNA S-parameters are shown in Fig. 4. It can be observed that the output and input return losses are greater than 10 dB for the entire band.

The LNA is stable across the entire band up to cut-off frequency as shown in Fig. 5. The stability factor (B1) is above 1 for the band of interest while the stability factor (K) is also above 1 for the band of interest.

Table 1: 5G-LEO link budget simulation parameters

Design Parameter	Value	Unit
SNR_{min}	10	dB
Bandwidth	600	MHz
5G terrestrial distance	10-150	m

Table 2: LNA Requirements and Performance at 3.5 GHz Design Frequency

Design Parameter	Requirement	Performance
$S_{11}(dB)$	$\leq$ - 10	- 19
$S_{21}(dB)$	$\geq$ 20	20 - 21
$S_{22}(dB)$	$\leq$ - 10	- 17
NF (dB)	< 2	1.3 - 1.4
K	> 1	5
$B1$	> 0	1
$P1dB(dBm)$	> 8	9.6
$OIP3(dBm)$	> 17	18
In-band Ripple (dB)	≤ 3	1

The gain (Fig. 6) was between 20-21 dB with a ripple of 1dB across the required band while the minimum output noise, $nf(2)$, at the centre design frequency of 3.5 GHz was 1.3 dB (Fig. 8).

The layout of the designed LNA is shown in Fig. 7. From our simulated design, a 20-21 dB gain in an LNA means it significantly amplifies the signal. For sensitive applications like radio receivers or radar systems, where the received signals are often very weak, such amplification is crucial for subsequent processing and interpretation. So, a gain of 20 dB implies that the output power is 100 times the input power.

The derived noise figure (1.3 dB) is used to determine the noise floor

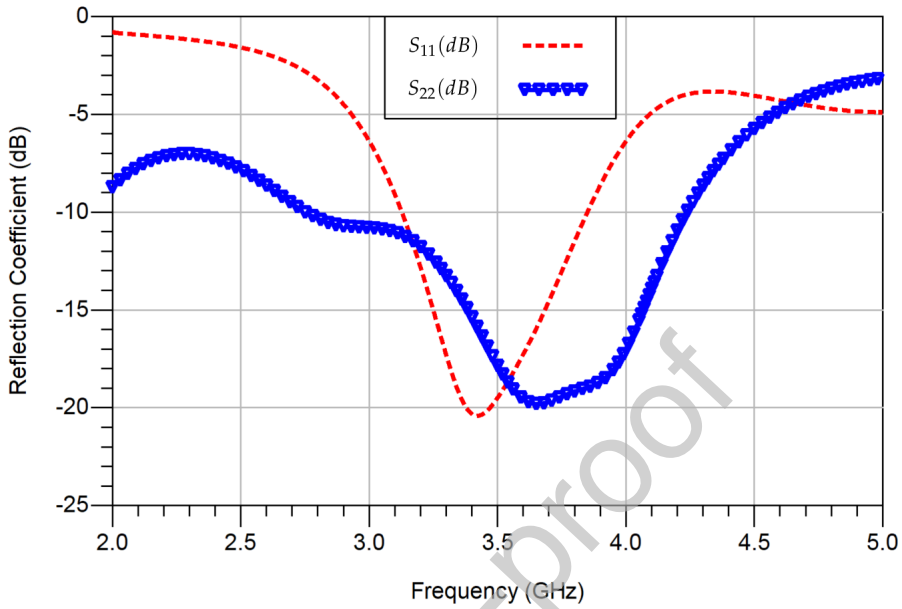

Figure 4: Simulated Input (Red) and Output (Blue) reflection coefficient of the 3.2-3.8 GHz LNA

of the LNA. The noise floor of the LNA directly impacts the sensitivity of the receiver system. In radio frequency (RF) and microwave systems, the sensitivity determines the minimum signal strength that can be effectively detected and processed. A lower noise floor in the LNA allows the system to detect weaker signals, which is critical in long-range communication, deep-space communication, and applications involving weak received signal detection like radio astronomy. The noise floor is calculated as:

$$NoiseFloor = -174dBm + NF + 10logBW \tag{6}$$

From the result gotten for the noise figure (1.3 dB) and design bandwidth (600 MHz), the noise floor is calculated to be -84.9 dBm. A noise floor of -84.9 dBm means that any signal with a power level higher than this can be distinguished from the noise. It's a critical parameter in designing systems like receivers, where detecting low-level signals is essential. This value directly influences the sensitivity of a receiver system. The lower the noise floor, the better the system's ability to detect weak signals (Fig. 9).

The receiver sensitivity is crucial in various applications such as wireless communications, radar systems, and astronomical observations. High sen-

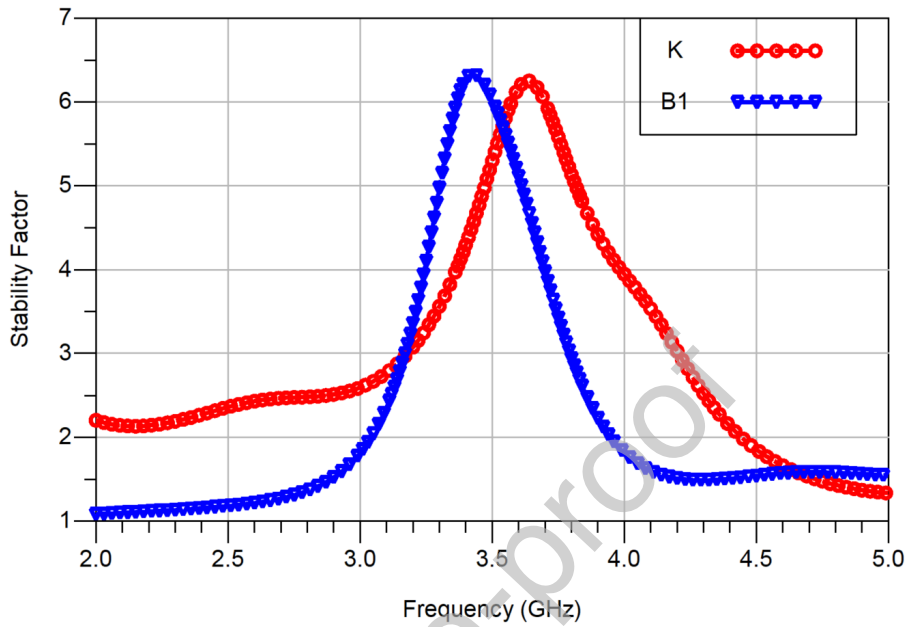

Figure 5: Simulated Stability Factor of the 3.2-3.8 GHz LNA (Stability factor (K) is shown with the red line. Stability measure (B1) is shown in the blue line)

sitivity allows for longer communication ranges, lower transmission power requirements, and the ability to detect faint or distant signals. Mathematically, sensitivity is defined as:

$$Sensitivity = NoiseFloor + SNR_{min} \tag{7}$$

From Fig. 9, the sensitivity of the LNA is -75 dBm at a channel bandwidth of 600 MHz.

The blocking dynamic range is a parameter that defines the range over which a receiver can effectively process incoming signals. It is specifically concerned with the receiver's ability to handle a strong undesired (blocking) signal while still being able to detect and process a weaker desired signal. The blocking dynamic range (BDR) is defined as:

$$BDR = P1dB - NoiseFloor - SNR_{min} \tag{8}$$

From our calculated values, the BDR is 84.6 dB

Spurious free dynamic range (SFDR): The input power range over which third order inter-modulation products are below the minimum detectable

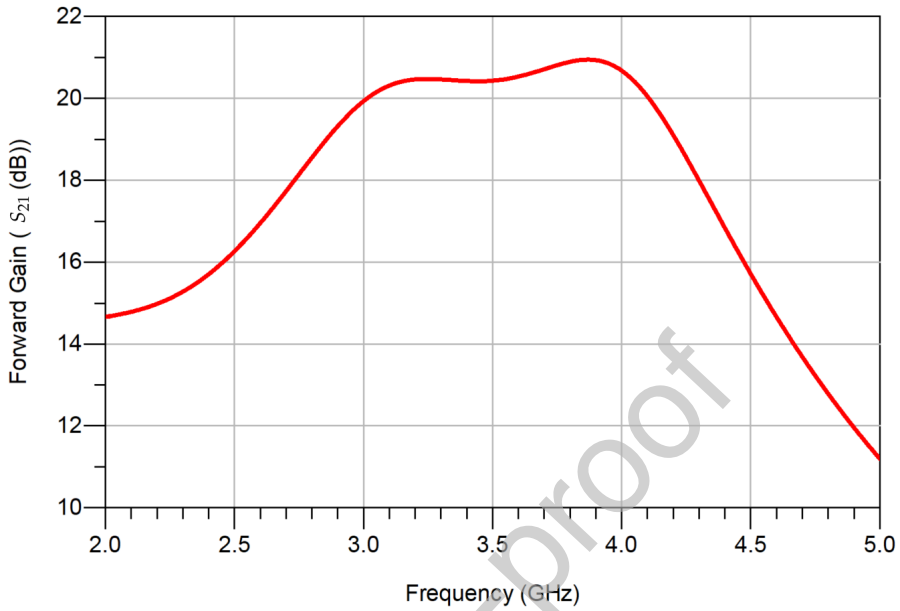

Figure 6: Simulated Gain of the 3.2-3.8 GHz LNA

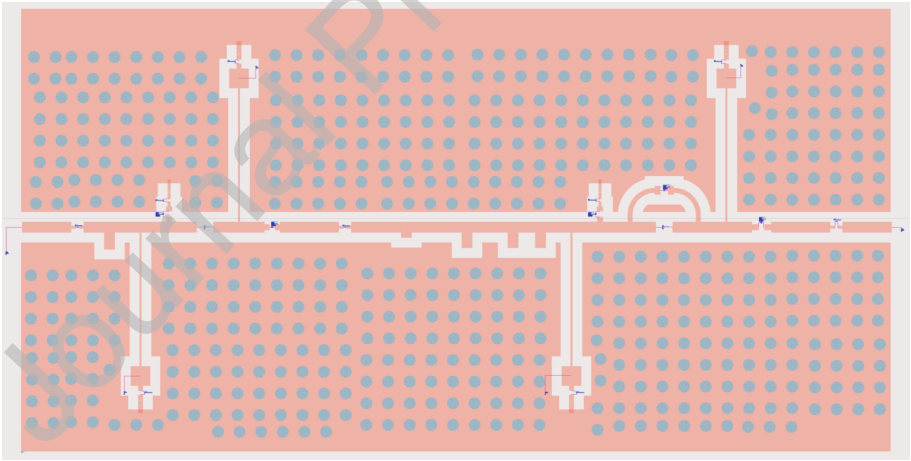

Figure 7: Co-simulated Layout of the 3.2-3.8 GHz LNA

signal level. Mathematically, the SFDR is given by:

$$SFDR = 2/3(P1dB - NoiseFloor) - SNR_{min} \tag{9}$$

From our calculated values, the SFDR is 53 dB

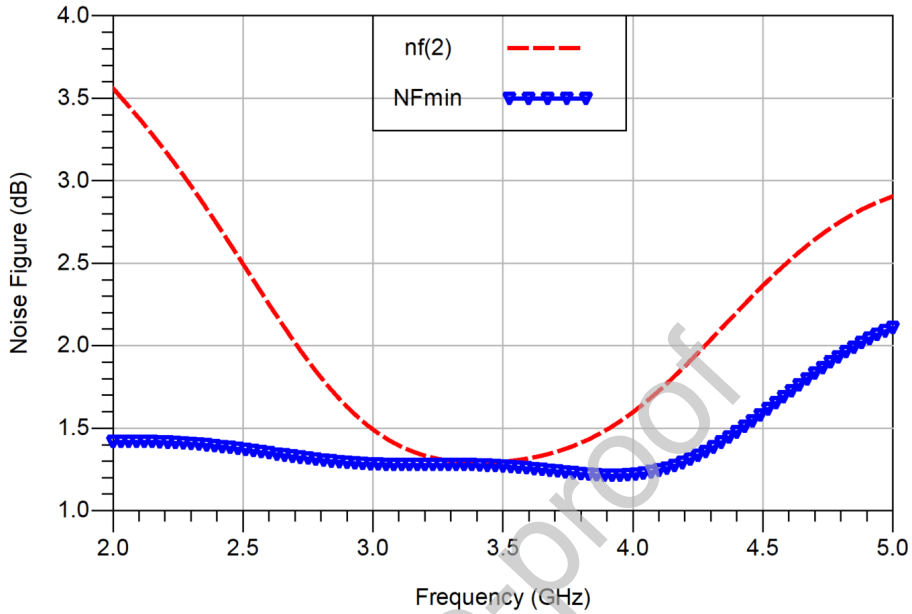

Figure 8: Simulated Noise Figure of the 3.2-3.8 GHz LNA

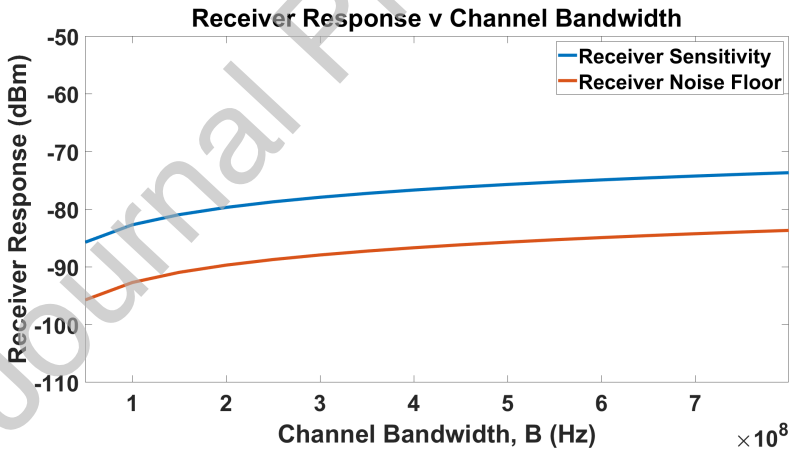

Figure 9: Sensitivity and Noise floor response

Fig. 10 shows the 1-dB compression point of the LNA. The 1-dB compression points at the input and output are determined to be -10 dBm and 9.6 dBm, respectively, at a frequency of 3.5 GHz. When these thresholds are passed, the amplifier begins to compress and eventually saturates. Any

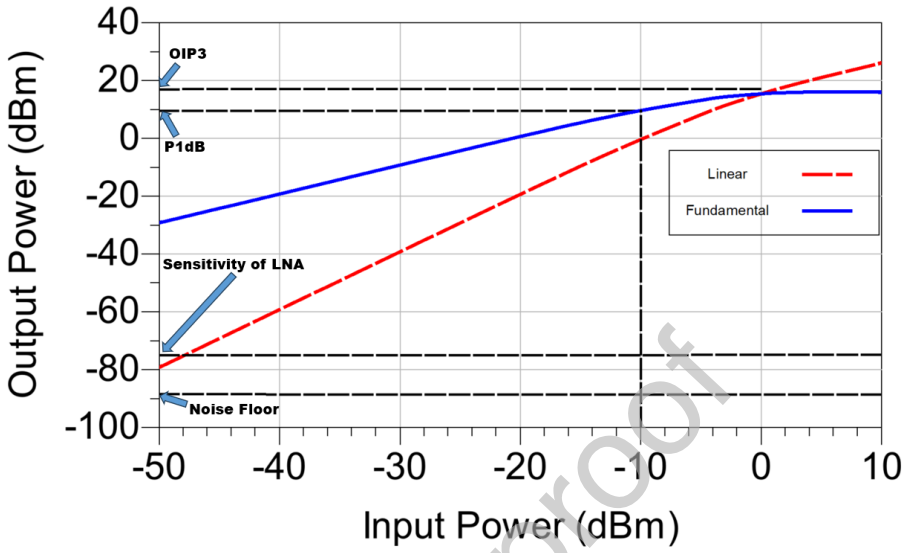

Figure 10: Input and output characteristics of the designed LNA.

further increase in the input power leads to no further output power growth. The amplifier response becomes non-linear and produces signal distortion, harmonics, and perhaps intermodulation products beyond this compression limit.Also from Fig. 10, we can see the values for the $OIP3$, $P1dB$, sensitivity and the noise floor as calculated from our equations.

The designed and presented LNA can be integrated into a channel-aware satellite-cellular receiver frontend [1], [3], [14], [5] with a single-input and single-output reconfigurable impedance matching networks (IMNs) for the antenna, bandpass filter bank and LNA [5], [12], [6], [25]. The IMNs are varactor-based designs to provide control bit settings for each multi-RF LNA band of interest [4], [36], [23]. Each LNA band has a bit that is dynamically and deterministically set to configure all IMNs for band-specific optimum noise figure, linearity, reflection coefficients, stability, gain and beamforming performance metrics [4], [47]. This enables the designed 600 MHz bandwidth LNA to deliver the best system-level performance metrics possible in a compact MMICs package for 5G/6G Satellite-cellular communication convergence use cases and/or applications [3], [1], [35]. This results in the lowest cost, size, weight and power (C-SWaP) reconfigurable and dynamic receiver frontend architecture possible.

The novelty of a reconfigurable LNA design approach lies in its ability

to obviate multiple shortcomings of conventional multiband receiver frontend designs. The prominent benefit is the removal of a band-select switch at the LNA output. For satellite-cellular convergence communication uses cases and/or applications, this sets the receiver temperature margin at 6 K and reduces the transceivers output loss by 0.81.0 dB, yielding a better performance over the conventional design techniques. The presented LNA supports independently tuned band-specific receivers implementations with an optimum load impedances and smart switch placement to accommodate beamforming as well [35], [23]. A reconfigurable LNA closely approximates these performance metrics and hence, holds a great promise in future integrated satellite-cellular telecoms networks [14], [6].

In a wideband LNA design, load impedance is often designed to operate below the optimum load target to accomplish high output network bandwidth [4]. Wideband LNAs have reduced forward transmission gain and noise figure [4], [8]. The designed narrowband LNA realises performance metrics that can only be achieved with a reconfigurable LNA architecture [35], [4]. Hence, the capability to synthesise operational optimum load impedances is key to a reconfigurable LNA design [35], [15]. Consequently, this LNA design approach can increase the periphery of the amplifiers field-effect transistor and maximise the output gain within thermal limits [23], [46]. The future receiver frontends will favour mostly digitally-assisted reconfigurable ultra-sensitive passive receiver frontend subsystems architectures with multimode, multi-source hybrid wireless energy harvesting capabilities [38], [44], [13].

If integrated into a reconfigurable LNA design, the presented LNA can support a dynamic RF receiver sensitivity [8] and beamforming [29], [48], [49] improvement technique that addresses the following satellite-cellular RF communication system architecture customer requirements on-the-fly [4], [5], [12], [25] viz:

- How many stages to use (single- or multi-stage designs);
- What type of stages are required (design for low-noise, high gain, stability and gain flatness, inter-stage couplings, high power added efficiency, high linearity, etc.);
- Parameters for each stage (transistor size, bias settings, impedance matching, performance metrics, component values, etc.);
- Real-time circuit performance enhancements technique (digitally-assisted reconfigurable impedance matching circuitry(s) via varactors;

- field-effect transistor-based high-speed single-pole double throw tuning; and digital optimisation, etc.);
- Order of each stage (components arrangement e.g., a low-noise amplifier is placed before or after a bandpass filter, etc.) [4], [8], [15].

Table 3 shows a comparison of the existing simulated LNA topologies with our reported designed spanning the 3.2-3.8 GHz band.

4. Conclusion

This paper presented the design, and simulation of a 3.2-3.8 GHz LNA specifically tailored for 5G wireless applications. The proposed LNA design exhibits compelling 5G radio access communication performance metrics including noise figure of 1.3-1.4 dB; forward transmission gain of 20-22 dB; and OIP3 of 18 dBm.

The LNA's performance can be attributed to the careful selection of GaAs technology and the employment of a common-source topology with inductive degeneration, which is known for its favourable noise characteristics at high frequencies. The input and output networks were meticulously designed and tuned to achieve optimal impedance matching, which is reflected in the LNA's S-parameters.

The research advances the current understanding of LNA design for the mid-band spectrum of 5G networks and provides a concrete foundation for future work in this area. Our methodology and findings can serve as a valuable reference for other researchers and practitioners seeking to optimize RF front-end components for next-generation wireless communication systems.

Furthermore, the presented LNA design not only meets the present-day benchmarks of 5G RF performance but also offers the flexibility for scaling to future advancements in wireless technologies. The approach to stability and noise optimization, in particular, will remain relevant for subsequent evolutions in high-frequency amplifier design.

In conclusion, the LNA design has successfully balanced the trade-offs between gain, noise figure, and linearitycritical parameters for the RF front-end in 5G communication systems. Its deployment is anticipated to enhance the reliability and efficiency of 5G networks, facilitating the delivery of high-speed, low-latency communications to end-users. Future work will focus on further miniaturization, cost-reduction, and integration with full transceiver

Table 3: Simulation Comparison of Designed LNA at 3.2-3.8 GHz Frequencies

Ref.& Year	Process	Freq.(GHz)	Gain (dB)	Noise (dB)	Power (mW)
[50] 2022	28 nm CMOS	1.7-3.6	31.5	3.4-4.8	17.8-38.2
[51] 2023	0.18 µm CMOS	2.89-4.58	14.19	2.6	14.4
[30] 2021	28 nm CMOS	0.02-4.5	15.2	2.2	4.5
[52] 2022	40 nm CMOS	2-12	16.5-19.5	3.2-5.2	9
[24] 2023	0.5 µm AlGaAs/GaAs pHEMT	4.2-5.2	27.6	0.58-0.72	45.6
[53] 2011	0.5 µm AlGaAs/GaAs pHEMT	2.5-5	17	2.4-3.0	16.5
[54] 2007	0.5 µm InGaAs pHEMT	3.3-3.6	16.7	1.8	11.4
[55] 2017	0.5 µm AlGaAs/GaAs pHEMT	1-4	23	1.8-2.3	250
[41] 2023	0.15 µm GaAs pHEMT	1-12.5	23.6	1.5-2.4	87.5
[43] 2023	0.15 µm GaAs pHEMT	0.5-24	24.7	1.7-2.8	212
[56] 2022	65 nm CMOS	0.-3.5	17	2.1-2.9	6.6
This Work	0.3 µm GaAs pHEMT	3.2-3.8	20-22	1-1.3	142

systems, aiming to contribute to the global deployment of accessible and high-performing 5G infrastructure.

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Highlights

1. The proposed LNA design focuses on achieving a low noise figure (NF), high gain, and robust linearity to accommodate the dense signal environment and wide bandwidth of 5G networks.
2. Simulation results predict a noise figure of 1.3-1.4 dB, a gain of 20-21 dB across the band of interest, and an input-referred third-order intercept point (IIP3) of 18 dBm.
3. The LNA demonstrates excellent performance in a 5G testbed, showing a significant improvement in the signal-to-noise ratio and the potential to enhance 5G receiver sensitivity.
4. The research substantiates the LNA's viability for integration into 5G base stations and user equipment, underscoring its potential to contribute to the efficient and reliable operation of next-generation wireless networks.
5. This LNA can be used for 5G New Release (NR) band of n77 and n78 (3.5-3.7 GHz).

Declaration of interests

☒The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

☐The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

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Mr Stephen Alabi (MIET) is the founder and Managing Director of SmOp Tech and has overall responsibility for its operational performance. Stephen is also the driving force behind SmOp's strategic plan. He holds a BSc in Engineering Physics and an MSc in Advanced Process Design for Energy from The University of Manchester, UK. He has a background in the scientific aspects of the Company's project which has aided product delivery and knowledge transfer. Stephen's involvement in setting the strategic direction of the business and authority to commit resources to support Research and development projects make him the ideal candidate to act as Senior Business Employee. Mr Alabi was the Technical Programme Chair at the Second International Adaptive and Sustainable Science, Engineering and Technology (ASSET) Conference 2023 held in Manchester, UK and spoke on "Hybrid Wireless Power Transfer for Passive Electronic Appliances." He has five refereed technical publications and 10+ peer-reviewed articles on "green energy development for future-generations telecoms infrastructure" in preparation.