Three-phase Resonant DC-link Converter

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Three Phase Resonant DC Link Converters

Analysis and Simulation

Ph.D. Thesis, report no. 1/2

by
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Abstract

The purpose of the project is to develop a three-phase resonant converter suitable for standard speed drives. The motivation for working with resonant converters is found in the problems of the standard converter type used today.

In standard converter type Pulse Width Modulated-Voltage Source Inverter, PWM-VSI, the switches are subject to high current and voltage stress during switching, which causes losses. The fast switching of modern switches reduces switching losses. Unfortunately this produces increased dv/dt and the size of the input/output filters of the PWM-VSI must be increased. The high speed of the switches cannot be fully utilized.

By using a parallel resonant converter the switching happens at low or zero voltage which reduces switch losses. The dv/dt is controlled by the resonant circuit, and it is therefore reduced significantly. The perspective using a resonant converter is high switching frequency combined with a high converter efficiency and low dv/dt.

In the first report several resonant converters are investigated to find a resonant converter that can compete with the standard PWM-VSI converter. Four converters were selected for the theoretical analysis, and the converters are simulated. An evaluation of the resonant converters is made, and one converter is selected for realization.

In the second report the realization of the selected resonant converter is described. This includes analysis, design and test of the converter.

A new control principle, using no additional power electric components, is eliminating the high voltage peaks associated with the resonant circuit. The resonant link voltage peaks are limited below 2.1 times the DC link voltages.

A new principle eliminating former resonant converter stability problems are proposed, implemented and tested. A resonant converter efficiency of 97 [%] was measured. The low dv/dt of the converter makes it possible to drive long cables without filtering. A successful test with a 300 [m] long cable and an induction machine load was carried out.

It is concluded that a stable, high efficiency and high switching frequency three phase parallel resonant converter is realized.

Preface

This report is the first of two reports which are the basis in my attempt to obtain the Ph.D. degree. The reports are a part of the project named 'Resonans Konverter for Elektrisk Energi-omformning' initiated February 1, 1993 and ended April 7, 1997.

The project is financed by the 'Danish Technical Research Council' and also in part by the foundation 'Det Obelske Familiefond'. The project is carried out at Aalborg University, Institute of Energy Technology (IET).

During writing several people have contributed to the report. Four supervisors followed the project and they have made an invaluable contribution, they are Head of Institute, Associate Professor John K. Pedersen and Associate Professor, Ph.D. Frede Blåbjerg from the Institute of Energy Technology, IET and Ph.D. Paul Thøgersen and B.Sc. Ulrik Jæger from Danfoss Drives A/S. I would also like to thank Danfoss A/S who supported the project by a VLT 3008 frequency converter.

I stayed four memorable months in Aachen at 'Institut für Stromrichtertechnik und Elektriche Antribe', where Oscar Apeldoorn and Franz-F. Protiwa were a great source of inspiration, and I thank them and people at ISEA for the very pleasant visit.

At Aalborg University, I would like to thank all the people at IET. In particular all the Ph.D. students and research assistants for interesting discussions, and Birthe Johansen for general help with the text editing. Technician Walter Neumayer has done a lot of laboratory work. During the last phase student Jacob Buck was helping in the laboratory. A special thanks to Ph.D. Peter Nielsen, now employed by Danfoss, for interesting discussions and pleasant company.

Aalborg University April 1997

Stig Munk-Nielsen
M.Sc. EE.

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1

Introduction

In this chapter first an introduction to power electronics and variable speed drives is made. Next the standard converter used in the variable speed drives is described. The converter performance is discussed and then the resonant converter is introduced. Finally, a description of the report structure is made.

1.1 Introduction to power electronic and converters

Electronics has for many years been in rapid development with the result that electronic components are capable of conducting high currents and blocking high voltages. The components are controlled with low voltage signals and often direct from a micro chip with a powerful calculation unit. Combination of easy controlled power components and powerful calculation chips has emerged a new field of electronics called power electronic.

The new generations of power electronic components are characterized by: smaller size, higher current and voltage levels, easy control and integration with micro electronic.

Today power electronics is widely used to convert electrical energy, and it is used in places as household, industry and utility systems. The power range is from a few VA to hundreds of MVA. Conversion of electrical energy using power electronics is of course not ideal, but it offers so great advantage that the application area is still increasing. Power electronic converters replace mechanical converters, and the development of power electronic itself results in new converters that replace older generations.

A major application area of power electronic converters is speed drives. This type of drive is typically available in the power range from 1-500 [kVA] and used in the industry. In 1993 the estimated world market value of converters was £7bn /7/. The power used by power electronics drives world-wide was estimated to 35 [GW] in 1993. Converters used in open loop and servo drives had a value of 61 % from world market value.

More than 50% of the applications used standard induction machines. The market of speed drives is growing fast. From 1993 to 2000 the open loop drive market value is expected to grow 100% and the servo drives 150% /7/.

Variable speed drives are found in industry for mills, winders, hoists, fans, and pumping applications. The most used machines in speed drives today are induction machines. Other types of three-phase machines might be popular, but many of them are controlled by the same type of speed drive as induction machines.

The induction machine dominates the market today, and in the near future no other machine is seemed to take over. The resonant converter application is therefore selected to be a variable

speed drive used for controlling standard induction machines. The drive is shown in Fig. 1.1.

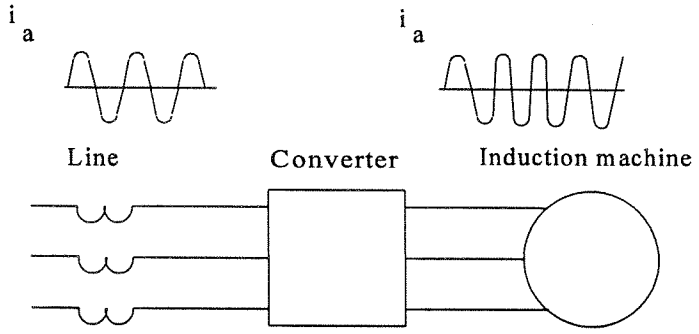


Fig. 1.1 View of speed drive system with induction machine load

The converter type dominating today consists of a rectification unit, a stiff DC link voltage, and an inverter(PWM-VSI[1]), and it has been the same over more than two decades. The converter is today considered mature. However, despite the development of the converter it has some undesirable qualities. There are limitations of switching frequency due to switching loss and high level of electromagnetic interaction due to high dv/dt.

1.2 Undesirable interaction between converters and environment

There are two undesired main interactions between the converter and its environment, one is the heat flow and the other arises from electromagnetic interaction.
Main reasons of heat flow are:

Converter losses
- switching losses in power electronic components
- conduction losses in power electronic components

Losses in load machine generated by converter
- non-sinusoidal converter output voltage

Losses in electrical network generated by converter
- non-sinusoidal converter input currents

Main reasons of electromagnetic interaction are:

Distorted converter input current

Conducted and radiated emission from the converter

Because high EMI[2] can cause disturbance or mal function of other electrical equipment connected to the electrical network, there are made EMI regulations. The sources of EMI are many and interference level is depending on converter topology selection, layout, and operation mode/33/.

One source of importance is the capacitive coupling between switching elements and ground. The capacitive coupling generates common mode currents, i_c:

$$i_c = C\frac{dv}{dt} \qquad (1.1)$$

[1] Pulse Width Modulated Voltage Source Inverter, PWM-VSI

[2] ElectroMagnetic Interaction, EMI

The capacitance should be minimized, and the dv/dt limited, to lower the level of common mode current.
A summarization of the above discussion and statements covering the most used converter type in electrical machine drives today is showed in Table 1.1. The converter is a PWM-VSI.

Desired converter improvement	**How to improve**	**Future importance**
low switching loss	increase switching speed of components	increase due to higher energy costs
low conduction loss	use low on state voltage components	
near sinusoidal input/output voltage	increase converter switching frequency and components switching speed	increase due to increased energy costs and attention towards low harmonic content
low dv/dt, low EMI	decrease component switching speed	increase due to new EMI regulations

Table 1.1 Desired converter improvements for the PWM-VSI converter, and how to improve performance. And expected further importance of each performance parameter.

From Table 1.1. it can be seen that the improvement of PWM-VSI converter performance includes both a decrease and an increase of power electronic component switching speed. This contradiction creates a dilemma. The problem has been present from the beginning of power electronics, but due to the increased attention to harmonic content, energy costs, and EMI, it gets harder to make PWM-VSI converters for speed drives that have satisfactory performance.

1.3 Introduction to resonant converters

Much research has been done to increase the performance of the PWM-VSI converter by adding auxiliary circuits, but none of them has been satisfactory. In 1986 a new type of converter was proposed by D.Divan "The Resonant DC-Link Inverter - A New Concept in Static Power Conversion" /1/. This converter uses the principle of zero voltage switching for the power electronic components which means that the switching loss ideally is zero, and the dv/dt is low compared to PWM-VSI. The zero switching loss allows high switching frequency, and in fact the switching frequency can be raised a factor of ten compared to the PWM-VSI.

Table 1.2. shows a performance comparison between PWM-VSI and the resonant converter proposed in /1/.

Desired converter performance improvement	Relative performance of converters	
	PWM-VSI	Resonant converter
low switching loss	-	+
low conduction loss	+	-
near sinusoidal input/output voltage	0	0
low dv/dt, low EMI	-	+

Table 1.2 Performance comparison between PWM-VSI and resonant converters.
Rating: 0 no difference, + better, - worse.

Table 1.2. shows that resonant converters have potential to be a competitor with the PWM-VSI, and this is the basis for further investigation of the resonant converter.

1.4 Structure of report

In the project a resonant converter is chosen for realization, and in this report the selection is done. This involves an investigation of different resonant converter topologies carried out using papers as source. The very broad view obtained is used to select a particular converter topology which is the parallel resonant converter topology, and this is done in Chapter 2. The resonant converter performance must compete with the standard PWM-VSI performance, and there is made a set of specifications that the resonant converter must fulfil. The resonant converter specifications are described in Chapter 3. Next step is a theoretical analysis and simulation of four selected parallel resonant converters which is done in Chapter 4, 5, and 6. In Chapter 7 a PWM-VSI converter is simulated so its performance can be compared with the resonant converters. In Chapter 8 the modulation strategies used in the resonant converters are described. In Chapter 9 the converter performance parameters are put into tables that makes it easier to compare the converter performance. In Chapter 10 the converters are compared and one converter is selected for realization. The realization and further work are described in the second project report.

1.5 Conclusion

In this chapter an introduction to power electronics and the application area is given. An important application is variable speed drives, low and medium power range. Improvement of power electronic components increases the variable speed drives performance and this increases the application areas. Expectations of a growth of 100% on the open loop drive marked value are expected from 1993 to 2000. Increasing energy costs and EMI demands increase the need of high converter efficiency and low distorted input and output voltage. A relatively new type of converter, the resonant converter, has potential performance improvement, relative to the standard PWM-VSI converter. The fact that the resonant converter has the potential to be a superior competitor, to the PWM-VSI, is the basis for further investigation of the resonant converters.

2

SELECTION OF CONVERTERS FOR DETAILED STUDY

This chapter gives first a short introduction to soft switching and then describes different resonant converters. The purpose of the description is to select a few resonant converters that seem the most useful, in low to mid. power range area, variable speed drive applications. The selected converters are described later in the report. A detailed description of all the resonant converters reported in papers would be overwhelming time-consuming, and therefore the different converters are sorted in groups of converters that shear a particularly fundamental circuit configuration. Then by evaluating the different particular circuit configurations the number of converters to be looked at is reduced. Four fundamental circuit topologies are described:

Parallel resonant DC link:	Serial resonant circuit is energized by DC voltage source and the resonant circuit is placed in the converter link.
Series resonant DC link:	Serial resonant circuit is energized by DC current source and the resonant circuit is placed in the converter link.
Pole commutated DC link:	A resonant commutating circuit is connected to the centre of each converter leg which is energized by a DC voltage source.
AC resonant link converter:	The link voltage and current are AC quantities and serial or parallel resonant circuit can be used.

When the topology is selected, a few converters are selected for a comprehensive study, and a more specific list of performance and characteristic parameters can by set up in the next chapter.

2.1 Basic resonant switching principle

A resonant converter has one or more resonant circuits, a circuit could be a L-C serial or a parallel circuit. Using resonans it is possible to obtain ZCS[1] or ZVS[2], and compared with HS[3] the switching losses and dv/dt or di/dt are lower. But there are higher conduction losses, and the circulating energy of the resonant circuit causes losses. A serial resonant circuit is shown in Fig. 2.1.

With correct initialization values of the components the voltage above the capacitor v_{do} is oscillating between 0 and $2V_d$, the time domain equations of the circuit are shown in appendix A. If the voltage is fed into an inverter bridge and the inverter switching happens, then the resonant voltage reaches zero, the switching loss is ideally zero. The switching trajectories of ZCS, ZVS, and HS are shown in Fig. 2.2.

[1] Zero Current Switching, ZCS

[2] Zero Voltage Switching, ZVS

[3] Hard Switching, HS

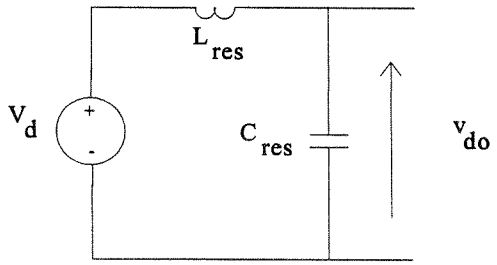


Fig. 2.1 Serial resonant circuit

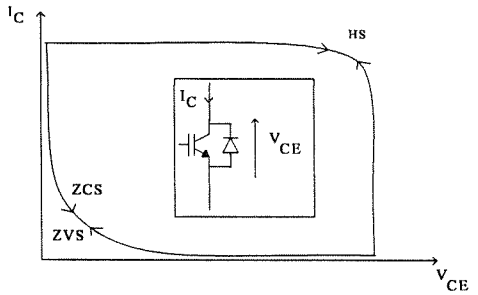


Fig. 2.2 The switching trajectories of ZCS, ZVS and HS.

The switching trajectories shown imply that there are switching losses using ZCS and ZVS. This problem is not considered in this report. It is assumed that the ZCS and ZVS are without loss. If hard switching is used it assumed the switching time is infinite small and loss less.

2.2 Parallel resonant DC link

The parallel resonant DC link converters have an oscillating link voltage that oscillates between zero voltage and a peak voltage. During the zero voltage period the converter switches can be turned on and off without switching loss. Fig 2.3 shows a parallel resonant converter without any link voltage clamp circuits. The switches in the converter must be

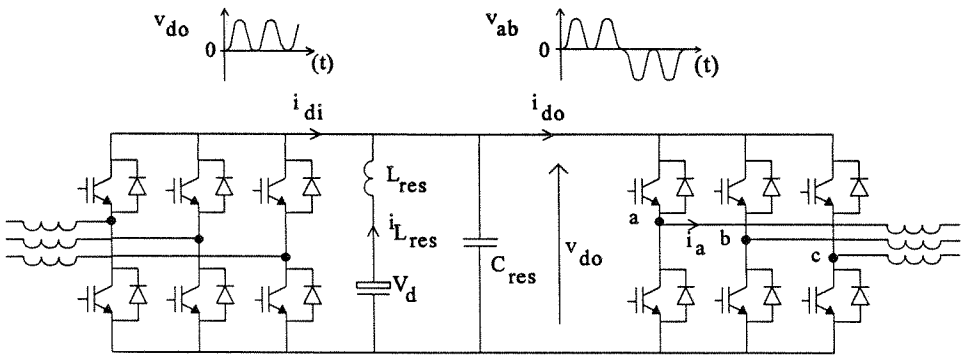


Fig. 2.3 Parallel resonant DC link converter

synchronized with the link zero voltage periods. This strategy eliminates the possibility of regular PWM[4], and instead a discrete pulse modulation DPM[5] must be used. In /1/ DPM is described, and it is concluded that the DPM theoretically has a performance comparative with PWM-VSI if the resonant switching frequency is more than 4 times higher. The spectral performance of the resonant converter is worsened because the link frequency is dependent on the link current.

Fig. 2.4 shows the resonant link voltage v_{do} and inductor current i_{Lres}. The figure shows an example of an increase in the resonant capacitor energy due to link current changes.

The result of the energy increase is a higher resonant link voltage amplitude. The energy is removed from the resonant components (inductor L_{res}) by the antiparallel diodes in the converter bridge, and the energy removal introduces an increased zero voltage interval. The zero voltage

[4] Pulse Width Modulation, PWM

[5] Discrete Pulse Modulation, DPM

interval also increases when the resonant inductor energy is increasing as shown in Fig. 2.4. The resonant switching frequency is often chosen to be higher than 20 [kHz]. By the resonant frequency is meant the average switching frequency of the inverter switches. The loss less switching has been reported using IGBT with a switching frequency of 65 [kHz] /35/.

The spectral performance of the resonant converter is dependent on the modulation index $m=\hat{V}_{ab}/V_d$. When a comparison of total harmonic distortion, THD, is done in /2/ it shows that DPM converter's spectrum performance is decreased at lower voltages.

Compared to hard switching converters with a stiff DC voltage link, the voltage peak to peak amplitude could be more than twice the DC voltage. The peak voltage is often limited by an auxiliary circuit/35/. A high peak voltage across the terminals has several disadvantages:

- High voltage rating of converter switches
- Stress on machine insulation which causes breakdown

The converters with link voltage clamp circuits typically have a clamp level of 1.3-1.5 relative to the DC link voltage. The active devices in the clamp circuits are typically the most stressed components in the converter. They have to work very close to the resonant frequency of the resonant components, whereas the switching frequency of the converter switches is lower. Clamp circuits without active components have been designed /22/ where the clamp level is 2.1 times Vd. Therefore, high voltages are still impressed on the inverter switches and machine insulations if the active clamp is avoided.

Resonant inverters which use soft switching could easily have a dv/dt lower than 500 [V/μs] and low values of dv/dt for diodes turning off. Hard switching of IGBT has dv/dt easily greater than 2 [kV/μs] and diode turn off has even higher dv/dt. Diode dv/dt higher than 10 [kV/μs] has been measured in the laboratory.

Low dv/dt is a desirable feature, /11/ advices a dv/dt lower than 1300 [V/μs] for inverter feeding standard 400 [V] induction machines.

2.3 Series resonant DC link

The series resonant DC link converter uses the principle of ZCS where loss less switching is obtained. The converter is closely related to the thyristor converter and the link voltage is bipolar which demands switches with symmetrical voltage blocking capability. The DC link current is oscillating between zero and minimum twice the DC link current, which is supplied by a DC-inductor, L_d. The converter must always form a current path for the inductive DC link current and inductive loads demand a capacitor filter. Fig 2.5 shows the series resonant DC link converter.

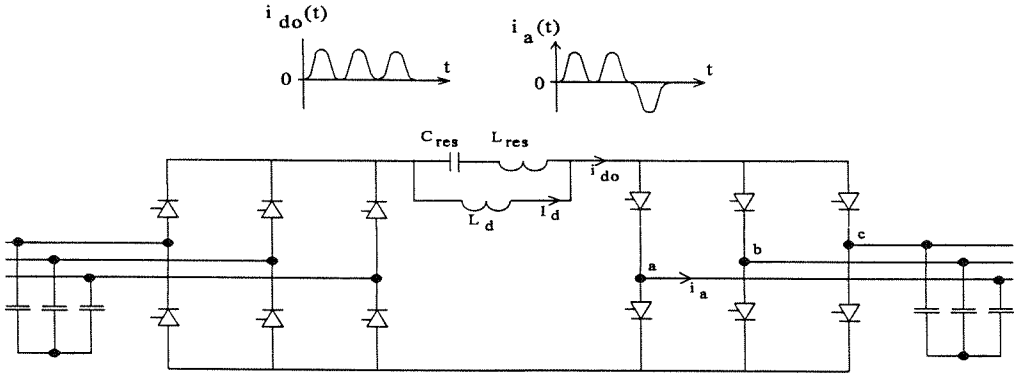


Fig. 2.4 Series resonant DC link converter.

One advantage is the low number of active components compared to the parallel resonant

topology. The converter is born with the possibility of rectification with unity power factor and bi directional power flow. When using a parallel resonant topology, the AC voltage rectification is often done by diodes that eliminate the controlled switches, the bidirectional power flow and the unity power factor correction options. Only 12 thyristors are needed for a full bridge three-phase AC to AC conversion while using a parallel resonant converter 12 transistors and 12 diodes are used.

The firing of the thyristors must be synchronized with the link zero current periods and again DPM is used. Spectral performance is dependent of the switching frequency. Normally the switching frequency is limited to 30 [kHz] due to relative slow switching times of thyristors /24/. Modern high speed thyristors have a turn off time around 10 [μs] /25/.

The link current stress is minimum twice the DC inductor current and the conduction loss is then relatively high compared to parallel resonant converters.

One general drawback of the serial converter is the necessary filter capacitance on the AC sides /26/. The interaction of the filter capacitance and the motor load inductance cause high frequency oscillations on the load current. Further on the ac capacitor is bulky. A passive 1st order filter can be used to reduce the high frequency oscillation to an acceptable level at the expense of extra components and ohmic power dissipation/26/. This solution makes the size of the converter very dependent on the load.

2.4 Pole commutated DC link

The pole commutated converter has a voltage stiff DC link, but the converter switches are switched under zero voltage conditions, and therefore low switching losses are obtained. To obtain ZVS an auxiliary resonant circuit is used. Each converter branch uses one circuit and the auxiliary circuit has three terminals, two are connected to the DC link terminals and the third terminal is connected to the branch terminal. The name 'pole' appears from that. An auxiliary pole resonant commutated converter/27/ is shown in Fig. 2.6.

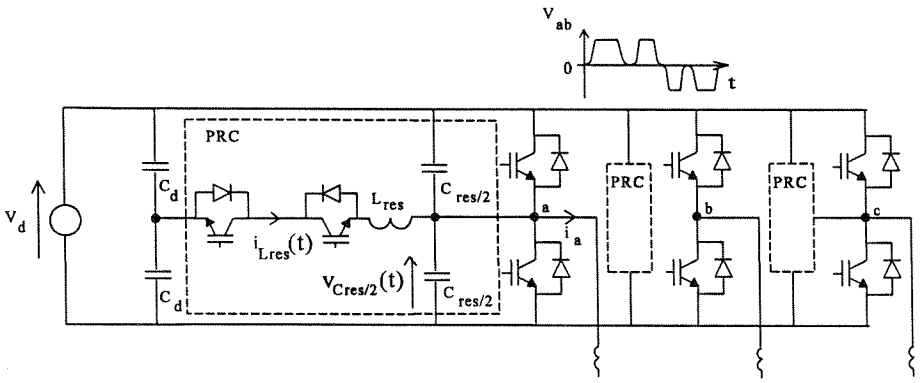


Fig. 2.5 Auxiliary pole resonant commutated converter

Unlike the parallel and series resonant DC link converters the pole commutated converter is able to perform PWM. Another advantage is that the main load current is not flowing through the resonant elements, and in this way the current stress on the resonant inductor is relatively small. On the other hand the resonant frequency must be high to yield a good PWM modulation band width. This is explained in the following paragraph.

The auxiliary commutation circuit must be synchronized with the switching of the converter switches, and the auxiliary commutation circuit which forms a resonant circuit has three main states ensuring ZVS of the converter switch. The states are:

State 1. Initialization of resonant circuit

State 2. A resonant cycle changing the branch potential from zero voltage to dc link voltage or opposites from dc link voltage to zero voltage

State 3. The resonant inductor discharges to zero current.

The total time required for the three states sets a minimum and maximum pulse width time and this sets a limitation of the PWM performance. Compared to hard switching converters the voltage stress on the converter switches is the same and the dv/dt of the output voltage is smaller.

There is a trade off between a low dv/dt and a small minimum, pulse width duration. An increased resonant frequency given by L_{res} and C_{res}, increases the dv/dt but lowers the minimum pulse width. This will give a better spectral performance. The pole commutated converters obtain a spectral performance close the to PWM-VSI for a given switching frequency/27/.

2.5 AC resonant link

The AC resonant link has a serial or a parallel resonant circuit operating at high frequency. The link voltages and currents are both AC quantities, and therefore bidirectional converter switches are necessary. The bidirectional switch in one package is not available yet. Today, it has to be buildt from several discrete devices, and often it is necessary to add snubbers to make the switch work properly /30/. The converter switches are turned on at ZCS or ZVS to obtain small switching losses. Fig 2.7 shows a serial AC resonant link.

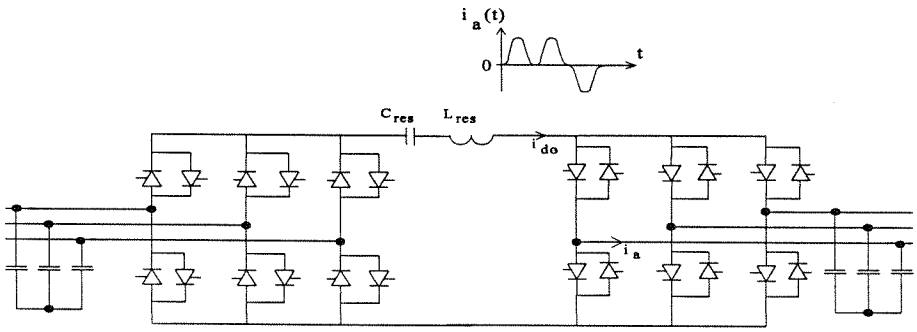


Fig. 2.6 Series resonant AC link converter.

Using an AC link decreases the amount of energy stored in the link. The DC link capacitor or inductor used in the earlier described topologies is eliminated, but the resonant components must handle the total power flow through the converter. A high VA rating is needed for the components /4/. The AC link converter must be operated in such a way that the energy demand of the load side is supplied by the input converter. The energy flow control through the converter must ideally be controlled instantly. In the real world this is not possible, but with fast signal processors and a high link frequency the energy flow can be controlled satisfactorily/31/. The coordination of rectifier and inverter is complex and the large number of switches to be controlled makes the realization of the converter difficult.

2.6 Survey of converter topologies

The topologies performance and characteristics are put into Table 2.1 and Table 2.2. The tables offer a comparison between the topologies and the PWM -VSI hard switched converter.

Table 1. High level properties

Converter topology	Input converter	Output converter	Link type	Device number		Link device count		Input filter	Output filter
				Switches	Diodes	Switches, diodes	Passive components L,C	Passive components L,C	Passive components[*2]
Parallel res. DC link	Diode or DPM	DPM	Voltage res. DC link	6 12	12 12	min. 0	1L,2C	3L	0
Series res. DC link	DPM	DPM	Current res. DC link	12[*1]	0	min. 0	2L,1C	3C	3C
Aux. Pole commutated DC link	Diode or PWM	PWM	DC voltage	12 24	18 24	0	6L,14C 3L,14C	3L	0
AC serie res. link	DPM	DPM	AC current	24[*1]	0	0	1L,1C	3C	3C
Sinusoidal PWM-VSI	Diode or PWM	PWM	DC voltage	6 12	12 12	0	1 L 1 C	3L	0

[*1] Use thyristors

[*2] Inductive load assumed

Table 2. Medium level properties

Converter topology	Input converter	Typical switch elements	Switch type	Main switch switching	Typical switching frequency [kHz]	Converter power level*3	Control complex-ness	Max. output voltage*1	Approx. main switch V stress *2	Approx. main switch I stress *2
Parallel res. DC link	Diode DPM	IGBT, MOS-FET	Uni-directional	ZVS	20-60	middle	moderate complex	<=1	1.3-2	1
Series res. DC link	DPM	Thyristor	Uni-directional	ZCS	<30	middle, high	very complex	current	1.2	>2
Aux. Pole commutated DC link	Diode PWM	IGBT	Uni-directional	ZVS	<20	middle, high	moderate complex	1	1	1
AC serie res. link	DPM	Thyristor	Bi-directional	ZCS	<30	middle, high	very complex	current	na	na
Sinusoidal PWM-VSI	Diode PWM	IGBT, MOS-FET	Uni-directional	Hard	1 - 18 kHz	middle, high	simple	1	1	1

*1 The output voltages are normalised using the DC link voltage as base value
*2 The voltage/current stress is relative to the sinusoidal PWM-VSI
*3 Power level: middle 1-100 [kVA], high > 100 [kVA]

2.7 Discussion

In this section a discussion of the topologies presented in this chapter is made.

Serial resonant AC link

The AC serial resonant link converter has no suitable bidirectional switches and the realization of bidirectional switches must be done by discrete components. /29/,/30/ use additional snubber circuits for the switch realization. The snubber causes high losses /29/. Comparing the converter size, then the AC resonant link eliminates the need of energy storage that ensures a voltage or current offset. With no energy storage the rectifier must deliver the needed power that is demanded by the inverter. This control strategy of the AC resonant link converter is complex to realize. If the same control strategy is applied to a DC parallel resonant link converter, the capacitance of the DC link capacitor is reduced considerably /15/. It seems that the size advantage of the AC serial resonant link is small, if any at all. No further investigation of AC resonant link converter is done.

Serial resonant DC link

The serial resonant DC link converter uses more filter components than the parallel resonant DC link converter, and with inductive loads there are problems with resonance between the load and filter /24/. To eliminate the resonans a 1st order filter could be used /26/ at the expense of loss and extra components. The serial resonant DC link has a relatively low number of switches and diodes because thyristors are used. However, this switch type limits the link frequency to 30 [kHz]. The converter seems promising for high power applications using thyristors /24/, but for medium power applications with demands of low THD a parallel resonant seems to offer a better performance. The need of a capacitive output filter and the problems of resonant with inductive loads are a major drawback, no further investigation of serial resonant DC link converters is done.

Pole commutated DC link converter

The pole commutated DC link converter has a spectral performance close to hard switched VSI-PWM and no additional voltage stress. Therefore , it has superior performance compared to the parallel resonant DC link converter performance. Comparing the component number in the converters the pole commutated DC link converter uses twice the number of switches and diodes. The number of passive components is increased too. In /28/ a combination of the pole commutated DC link and parallel resonant DC link converter is proposed. A converter that uses three switches and three diodes is made. The converter has good spectral performance and does not use extremely many components relative to the PWM-VSI. This converter is disregarded here due to high component count. For high power application the pole commutated DC link converter must be reconsidered.

Parallel resonant DC link

The parallel resonant DC link converter is very similar to the PWM-VSI converter comparing the number of components used. It is the DC voltage link converter of the resonant converters that uses the smallest number of components. The main disadvantages are the high link voltage amplitude that is twice the link voltage of the PWM-VSI converter. If the high link voltage is not accepted, there must be added auxiliary circuits to clamp the voltage amplitude, or there must be found new ways to limit the link amplitude voltage without using clamp circuits.

The switching frequency must be at least four times higher than the PWM-VSI switching frequency to obtain the same output voltage and current quality. Further on is the spectral performance more dependent of the load conditions that PWM is. At low modulation index is the spectral performance of the resonant converter decreased somewhat compared to PWM. The

resonant converter has little switching loss and therefore the switching frequency is usually higher than 20 [kHz]. Using a switching frequency of 20 [kHz] the resonant converter spectral performance should be equal to a 4-5 [kHz] PWM converter.

2.8 Selection of resonant converters

Some basic requirements to the selected converter are:
- Voltage link
- Low DC link voltage peaks
- Good spectral performance for low and high modulation index
- Low number of devices

The voltage link is preferable to current link because it eliminates capacitive filters.

Of the resonant converter topologies described here the parallel resonant converter topology is judged to be closest to the desired requirements. This is of course a subjective opinion. It is discussed how good the fundamental circuit configuration of the parallel resonant converter in 2.2 fulfils the basic requirements, and from this a few converters are selected to work further on.

Voltage link : All the converters have a voltage link.

Low DC link voltage peaks: It is shown that the fundamental circuit configuration in Fig. 2.1 has a load dependent peak link voltage which is undesirable. The link voltage must be controlled in order to limit the voltage ratings of the converter components and to keep the link voltage peak amplitude constant to avoid sub-output voltage harmonics.

Good spectral performance for low and high modulation index: It is mentioned in several papers that the DPM converter has a relative worse output voltage quality than the PWM converter, at low modulation indexes.

Low number of devices: The fundamental circuit configuration in Fig. 2.1 only adds two extra components relative to the standard PWM and this is a desirable feature. It is desired to keep the number of power electronic auxiliary components low, but as it will be shown, the number of components is increasing with the desire of fulfilling the upper requirements.

In Fig.2.8 the different converters that have been described in the papers used in this chapter are shown, and there are added two converters that have not been found described in any paper. They are described later. Under the Figure there is an explanation of the concentrated names

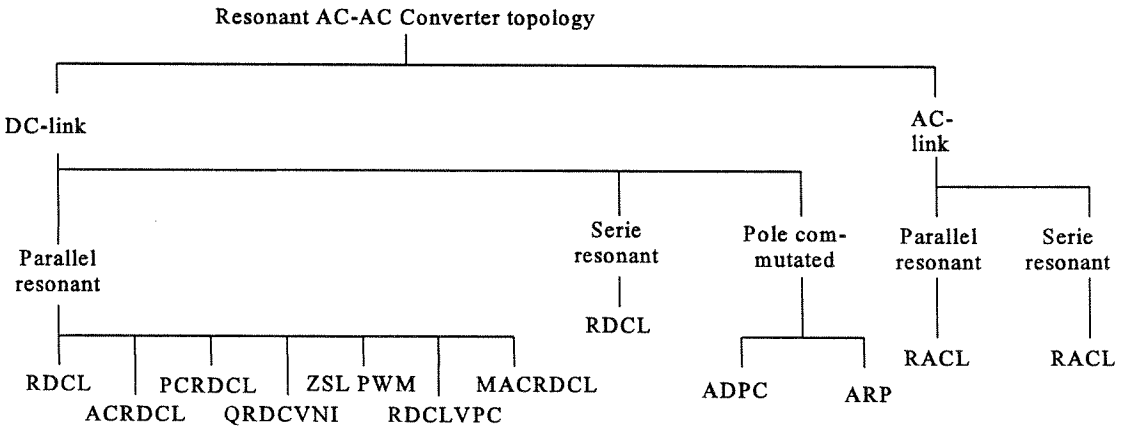


Fig. 2.7 Overwiew of converters dealt with in this report

Parallel resonant converters

RDCL: Resonant DC Link,/1/

ACRDCL: Active Clamped Resonant DC link,/35/,/23/

PCRDCL: Passive Clamped Resonant DC link,/22/

QRDCVNI: Quasi Resonant DC link Voltage Notch Inverter,/5/,/14/

ZSLPWM: Zero Switching Loss PWM,/15/

RDCLVPC: Resonant DC link Voltage Peak Control

MACRDCL: Modified Active Clamped Resonant DC Link

Serial resonant converters

RDCL: Resonant DC Link,/24/,/26/

Pole commutated converters

ARCP: Auxiliary Resonant Commutated Pole,/27/,/28/

AC resonant link converters

RACL: Resonant AC link,/30/,/29/,31/

The following converters of the parallel resonant converter are selected for a detailed study including a theoretical description and a converter simulation, and there is a short explanation why the converter is selected:

RDCL: Is the fundamental converter the parallel resonant converters.

RDCLVPC: Eliminates the need of link clamp components while maintaining control of peak link voltage, the control principle is new. A high efficiency is expected.

ACRDCL: Has the lowest resonant peak voltage.

MACRDCL: Is a modified ACRDCL resonant converter which is pulse width modulated and expected to have superior output voltage quality.

The parallel resonant converters shown in Fig. 2.8, which is not simulated, are only described briefly, due to the time a deeper analysis takes. The standard PWM-VSI is simulated in order to compare the performance of the resonant converters.

2.9 Conclusion

Initially in the chapter the basic resonant switching principle is described. Then four different resonant converter topologies are described, the purpose is to select a topology for further work. The selection of topology is based on a paper study. This is a fast way to obtain a general overview. On this very general knowledge the parallel resonant converter topology is selected for further study. Seven parallel resonant converters are described in the following chapters. Because it is very time-consuming to make a full analysis (based on idealized components) and simulation of the converters, only four converters retrieve this treatment. The remaining converters are only described very briefly. The four converters' performance is compared to each other. As the intention with the report is to find a converter with a superior performance relative to the PWM-VSI converter, the PWM-VSI converter is also simulated. A comparison of the resonant converters is made on the basis of the specifications found in the next chapter. The highest rated converter is going to be realized.

3

Resonant converter specifications

In the next chapters an investigation of the resonant converters selected in chapter 2 is done. The investigation of the resonant converters must give a picture of each converter's performance. In this chapter the performance and the characteristic parameters used in the evaluation of the resonant converters are chosen.

The resonant converter is, as described in chapter 2, used in a variable speed drive, and the load is a standard induction machine. There is, in this chapter, made an investigation of which type of converter output voltages there should be applied to the induction machine. The investigations are used to specify the demands to the resonant converters' performance.

3.1 Resonant converter load specification of DV/DT and maximum terminal voltage

Since the introduction of speed drives that generate high voltage pulses and dv/dt in the output voltage, there has been an increasing need of knowing what level of voltage stress induction machines can withstand. The allowable level of voltage stress has been discussed in /11/ where is is referred to investigations made at the Technical University of Dresden, initiated by ZVEI[1]. Their results show from a questionnaire to machine manufacturers that standard low voltage electrical machines can be stressed by output phase-phase voltage peak values of 1300 [V] and dv/dt of 1300 [V/μs]. The results from /11/ are shown in Fig. 3.1, and curve 1 is according to DIN VDE 0530 Part 1. Supplementary sheet. Curve 2. is according to a manufacturer questionnaire and curve 3,4 is special machine designs for high voltage.

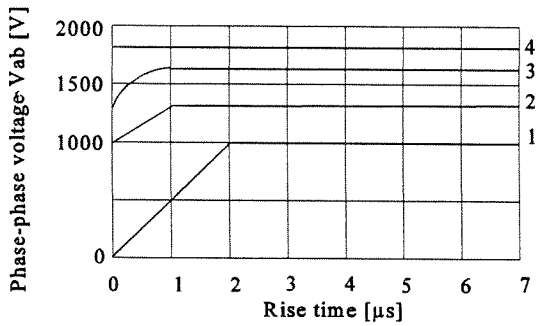


Fig. 3.1 Phase-Phase voltage peaks versus voltage rise time /11/.

Curve 1 is in /11/ judged as too pessimistic and this curve is therefore not used as reference. From the results shown in Fig. 3.1 curve 2 the resonant converter should generate phase-phase voltage peaks less than 1300 [V] and with a dv/dt lower than 1300 [V/μs], this curve is used as

[1] Zentralverband Elektrotechnik- und Elektroindustrie, ZVEI

reference. Lower dv/dt can be desirable where long cable can cause voltage reflections.

3.2 Resonant converter specification

One important feature of the PWM-VSI drives is the simplicity of the converter, only few components besides the switches are necessary. The main current paths in the converter are kept short to decrease stray inductance. Switching speed is set by the converter switches and drive circuits. Examples of rise times and fall times of modern IGBT's aregiven in /10/. Voltage rise times are measured from 70-400 [ns] and fall times from 100 - 1000 [ns] depending on drive circuits of the tested IGBT's. The antiparallel diodes generate also high dv/dt during turn off, and it can be higher than the dv/dt generated by the IGBT. dv/dt of 10 [kV/μs] has been measured in the laboratory. The dv/dt is minimized by choosing soft turn off diodes.

Short rise times can give voltage reflections and long cables amplify this effect/11/. Some ways of overcoming these problems are:

- An output filter reduces cable loss and insulation stress /12/.
- Integrate the converter as part of the machine /9/.
- Lower the dv/dt generated by the converter voltage

The first solution has some disadvantages, it creates losses and uses space. Second solution solves the problem with voltage reflections due to long cables, but the machine windings are still subject to high dv/dt. Third solution eliminates the problem of VSI converters by designing a converter that generates low dv/dt.

The resonant converter is well-suited for the third solution because it generates low dv/dt. The sinusoidal wave form of the resonant converter makes the combination of switching frequency higher than 20 [kHz] and low dv/dt possible.

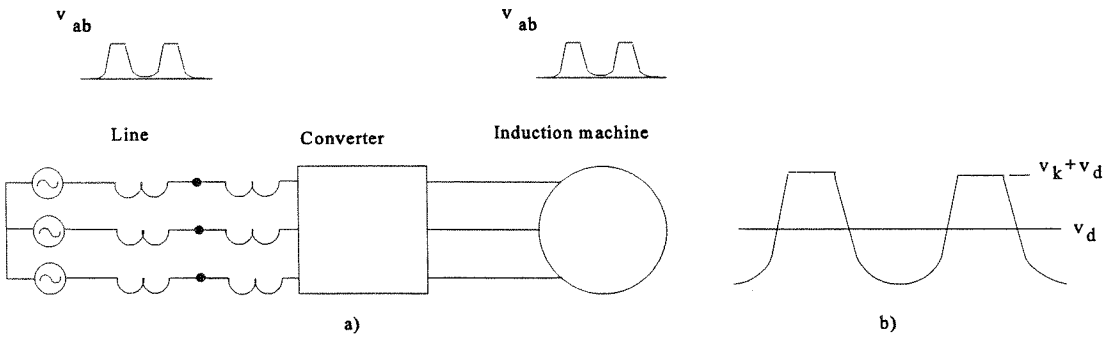


Fig. 3.2 **a** Shape of voltage wave form of parallel resonant speed drive.
b Zoom on resonant voltage wave form.

Typical voltage wave forms of the clamped parallel resonant converter are shown in fig. 3.2.a and 3.2.b. The peak voltage is a sum of the clamp voltage and the DC voltage level of the DC link. Clamp voltage V_k will vary somewhat, in practice from $0.3V_d$ to $1.2V_d$,depending on the converter type, Vd is the link DC link voltage. $V_d = 1.1V_{ab}\sqrt{2}$, $V_d = 620$ [V], $V_{ab} = 400$ [V] allowing 10 % overshoot.

Selection of resonant link frequency

It is desirable to have a high switching frequency keeping the voltage quality of the resonant converter competitive with the hard switched PWM converter. The PWM converter switching frequency is often limited by the power dissipation in the power electronic components. A PWM

converter switching frequency of 5 [kHz,] is considered close to the switching frequency used in industrial converters in the power range of 10 [kVA].

The resonant converter must have a link frequency, $f_{res,}$ at least seven time higher than the PWM- VSI switching frequency, f_{sw}/38/ to have a comparative performance. A factor of f_{res}/f_{sw}=ten should ensure, the resonant converter using Delta Modulation, a superior output voltage quality at higher modulation index. The demand to the resonant converter is a resonant link frequency of least 50 [kHz].

The converter output dv/dt is determined by the resonant frequency. Is it assumed the resonant circuit is ideal and not loaded, then the maximum output dv/dt is easily calculated. Dv/dt is obtained by differentiating the voltage equation found for the resonant capacitor in appendix A.

$$\frac{dv}{dt} = V_d 2\pi f_{res} \qquad (3.1)$$

Using a V_d= 620 [V] and a maximum dv/dt = 1300 [V/μs] the resonant link frequency can be 333 [kHz]. Using a resonant frequency of 50 [kHz], the dv/dt=195 [V/μs].

Specification

One should expect superior performance from the resonant converter considering dv/dt and switching losses compared to the PWM converter. On voltage and current quality, expressed by DF and THD, defined in App. E, the resonant converter should have almost similar performance as the PWM converter.

The desired specifications for a resonant converter are

- Output voltage, V = 400 [V] RMS
- Link voltage, V_d = 620 [V] including 10% overshoot of input voltage
- Peak output voltage maximum 1300 [V]
- Dv/dt < 1300 [V/μs]
- Resonant link frequency, f_{res} in the area of 50 - 333 [kHz]
- Distortion factor of inverter output voltage, DF similar to a PWM converter working a 5 [kHz] if the resonant converter link frequency is 50 [kHz].

The selection of converters is done on basis of the fulfilment of the given specifications. Besides this, a set of characteristic parameters is used. The performance and characteristic parameters of converters are plotted into a table in chapter 9. In chapter 10 the table and gained experience are used to select a resonant converter realization.

3.3 Conclusion

In the chapter a set of specifications for a resonant converter is selected. The purpose of the specifications is to enable a judgement of the resonant converters, selected for analysis. There is a problem of finding specifications, because the converter application, a speed drive for induction machines, is not very specific. The specifications are found in papers dealing with inverter output voltage influence on induction machines. There are made specifications of DC link voltage level, output voltage dv/dt, resonant link frequency and the output voltage DF should be equal to a 5 [kHz] PWM-VSI.

4

Non clamped parallel resonant converters

This chapter describes two converters, the first is proposed by Divan /1/ in 1989 and it is called RDCL[1]. Earlier in chapter two, this converter was found to possess a promising approach of applying zero voltage switching in three-phase converters.

The RDCL converter operation is described and the link resonant circuit operation is analyzed. The analysis of the RDCL results in a new converter, the new converter is the second converter described in this chapter. With the second converter it is possible to limit the peak output voltage to two times the DC link voltage and to make the link peak voltage load undependent. The new converter does not introduce extra power devices, the name of the converter is RDCLVPC[2].

4.1 Parallel resonant DC link converter (RDCL)

Parallel resonant DC link converters have an oscillating link voltage as shown in Fig. 2.3. The frequency of the link voltage is ideally given by the natural resonant frequency of the resonant circuit. To obtain zero switching loss of the converter switches, the switches are restricted to switch at the instant the link voltage is zero. To secure zero voltage switching there must be a synchronization between the link oscillations and the inverter switches.

The resonant link oscillation must be sustained over time. If the link oscillation is not sustained, the link voltage v_{do} might not reach zero voltage, and the zero voltage switching ability is lost. It is necessary to be aware of the factors that influence on the resonant link oscillation.

The resonant link oscillation can be altered by removing or adding energy to the resonant link components. If sufficient energy is removed from the oscillating resonant link, the v_{do} does not reach zero voltage.

Resonant link energy is changed if the link current i_{do} changes. If i_{do} is decreasing, the resonant link energy increases, the resonant link energy could decrease during a resonant period due to the load current. The difference in time constants between the load and the resonant link is huge. Because of the big difference in time constant the i_{do} only changes little during the resonant period, the increase of resonant link energy due to decreasing load current is small. The resonant link is discharged if the i_{do} is increasing. Here one must ensure that the resonant link contains enough energy to complete a resonant cycle where v_{do} reaches zero voltage.

The real world circuit always has losses. The resonant link must therefore be added energy to ensure that the v_{do} reaches zero voltage. The resonant link energy is normally added in the zero voltage period, and this is done by short circuiting the converter bridge. During the short circuit

[1]Resonant DC Link converter, RDCL

[2]Resonant DC Link Voltage Peak Control converter, RDCLVPC

the resonant inductor L_{res} is charged.

The huge changes of resonant link energy happen due to the converter switching. The converter switching can impress huge current on the resonant link and this could result in very high v_{do} amplitudes. The high v_{do} could be damaging to converter switches and load. The load situations are therefore dealt with in the following paragraphs.

Analyzing the resonant circuit, a time solution of the second order differential equations that describe the voltage and current is often used. Another method is to use the phase plane analyze. Phase plane analy makes it easier to discover general patterns of behaviour. Both the time solution and phase plane analysis are used in this report.

4.1.1 Link operation of the RDCL

No Load Condition

Looking at no load condition, it is the behaviour of the DC link that is at concern. The equivalent circuit used is shown in Fig. 4.1. At no load steady state operation the impact of initial conditions is investigated. An investigation of the initial conditions could lead to a way of controlling the resonant link voltage of the RDCL converter.

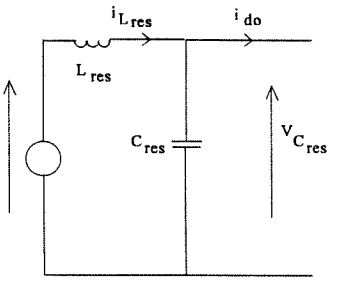


Fig. 4.1. An equivalent circuit of the RDCL.

The circuit is subjected to a step voltage V_d and the initial conditions are given by $I_{0_{Lres}}$ and $V_{0_{Cres}}$. In the phase plane the trajectory describes a circle with a radius V_{res}:

$$V_{res} = \sqrt{\left(V_{0_{cres}} - V_d\right)^2 + \left(Z_{res}\, I_{0_{res}}\right)^2} \qquad (4.1)$$

in steady state. If a loss element is present, the phase plot trajectories describe a spiral with a shrinking radius.

Fig. 4.2.a shows different phase plots at different $I_{0_{Lres}}$ and $V_{0_{Cres}} = 0$. The trajectories begin at $(v_{Cres}, i_{Lres} Z_{res}) = (0, I_{0_{Lres}} Z_{res})$.

If the absolute value of $I_{0_{Lres}}$ increases, the energy absorbed by the resonant circuit increases. It is not possible to decrease V_{res} to a value lower than V_d by altering $I_{0_{Lres}}$.

Fig. 4.2b shows different phase plots at different $V_{0_{Cres}}$ and $I_{0_{Lres}} = 0$. The trajectories begin at $(v_{Cres}, i_{Lres} Z_{res}) = (V_{0_{Cres}}, 0)$, the amplitude of $V_{0_{Cres}}$ determines the amplitude of V_{res}.

If $V_{0_{Cres}}$ is positive, the amplitude of V_{res} is decreasing because there is less energy in the resonant circuit. Otherwise, if $V_{0_{Cres}}$ is negative, the V_{res} is increasing.

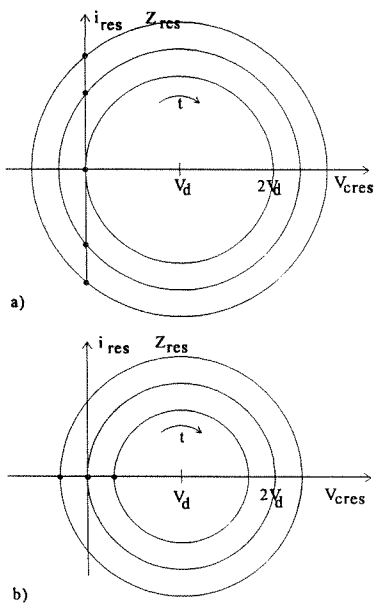


Fig. 4.2. Phase plane plots for steady state operation and different initial conditions.
a) Different initial current
b) Different initial voltage

In steady operation the trajectories are centered on V_d at the horizontal axis. In a steady state load situation the trajectories are symmetric around $i_{do}Z_{res}$, here i_{do} is zero.

Load Condition

What happens in load situations of the resonant DC link converter link? The three-phase inductive load is assumed to have a time constant so large that the load current is considered constant during a few oscillations of the DC resonant link voltage. The single phase equivalent circuit considered is shown in Fig. 4.3.

A load current I_{do} is impressed on the resonant cycle. The current change happens at zero voltage ($v_{Cres} = 0$). The component values of the DC voltage and resonant circuit are shown in Table 4.1.

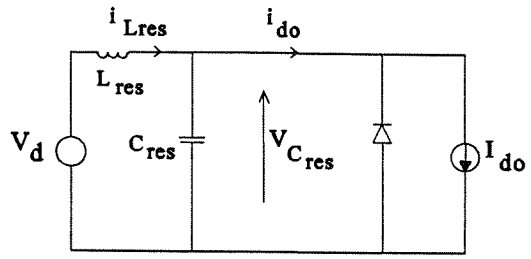


Fig. 4.3. Single phase equivalent of RDCL with load.

V_d Resonant capacitor (C_{res}) Resonant inductor (L_{res})	600 [V] 100 [nF] 150 [μH]
Load current (I_{do})	40 [A]
Resonant impedance (Z_{res}) f_{res}	38.7 [Ω] 41 [kHz]

Table 4.1. Specification of parameter values used in simulation shown in Fig. 4.4.

A simulation result is shown in Fig. 4.4a and Fig. 4.4b. It shows i_{Lres} and v_{Cres} and a phase-plane plot that shows i_{Lres} versus v_{Cres}.

The resonant cycle is divided into seven modes. Initially in mode 1 the resonant circuit is impressed V_d. The final mode number 7 is identical to mode 1. Between the two modes a current pulse (I_{do}) is impressed.

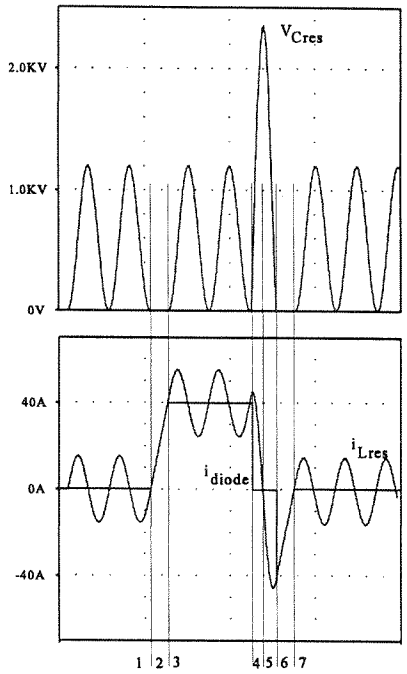


Fig. 4.4a. A load change in the resonant circuit. Time plots of V_{cres}, i_{diode} and i_{Lres}

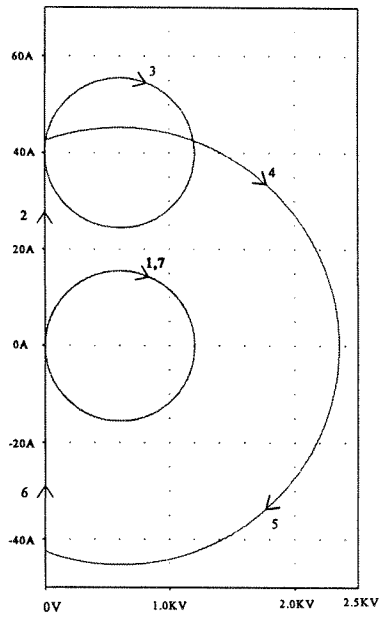


Fig. 4.4b. Phase plane plots of i_{Lres} versus V_{cres}

Mode 1 Steady state operation current amplitude value is V_d/Z_{res}. Voltage amplitude is $2V_d$ [V]. Phase displacement is $\phi = \pi/2$ [rad].

Mode 2 When the load current is impressed, the diode D1 forms a current path. $V_{C_{res}}$ is zero and $i_{L_{res}}$ is built up at a current rate $di_{L_{res}}/dt = V_d/L_{res}$ Fig. 4.5 show the components conducting current. The link circuit is no longer forming a resonant circuit. The inductor current increases until it equals the I_{do} current. Energy is moved from V_d to L_{res}, $E = \frac{1}{2} L_{res} I_{do}^2$.

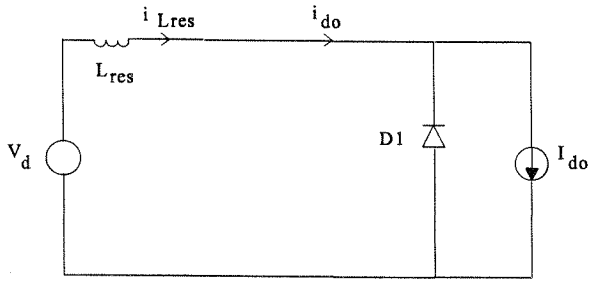


Fig. 4.5. Commutation interval of the resonant circuit.

Mode 3 Then D1 stops conduction, V_d is across L_{res}. The y-coordinate of the new circle center is increased to $I_{do} Z_{res}$. The phase displacement is given by $\phi = 2\pi\ I_{do}/V_d$ [rad].

Mode 4 I_{do} changed to a zero value. The initial conditions for the resonant cycle are $(I_{0_{Lres}}\ Z_{res} = I_{do}\ Z_{res})$, $(V_{0_{res}} = 0)$. Energy stored in L_{res} is moved to C_{res}, the capacitor is charged and id V_{res} increased.

Mode 5 Energy is moved from C_{res} to L_{res}.

Mode 6 Diode D1 begins to conduct, energy in C_{res} is zero. Energy $E = \frac{1}{2} L I_{do}^2$ earlier absorbed from the source, V_d is transferred back. Fig. 4.5 shows the components conducting. Note $I_{do}=0$.

Mode 7 Diode D1 stops conducting and a steady state trajectory with $V_{res} = V_d$ is obtained.

4.1.2 Simulation of RDCL and introduction to SABER

The chapter contains a brief introduction to the simulator and how to build simulation programs. Next a description of the implementation of the RDCL is presented in the simulation program. Simulation results are shown and parameters are extracted.

Simulation of the resonant converter shown in Fig.2.3 is limited to the resonant link and the inverter part. The used simulator deals with models that can describe the real world component behaviour closely. Due to the complexity of the component models, long simulation times are required. The objective of simulation is to gain knowledge about the converter behaviour, adequate to make a comparison to other converter technologies.

It is chosen to use the basic component models in this report. Switches and diodes are equivalent to variable resistors. The three-phase load is a R-L load.

The simulation program, SABER, offers the user a possibility of building a simulation program from modules. The modules contain standard components and the users own algorithms and control actions. Very often different converter topologies consist of the same modules. Some modules are even the same at different converters. When developing the converter simulation program, each converter is divided into modules in such a way the modules can be used in other converters. The RDCL converter is shown in Fig. 4.6 using the modules implemented in the simulation program.

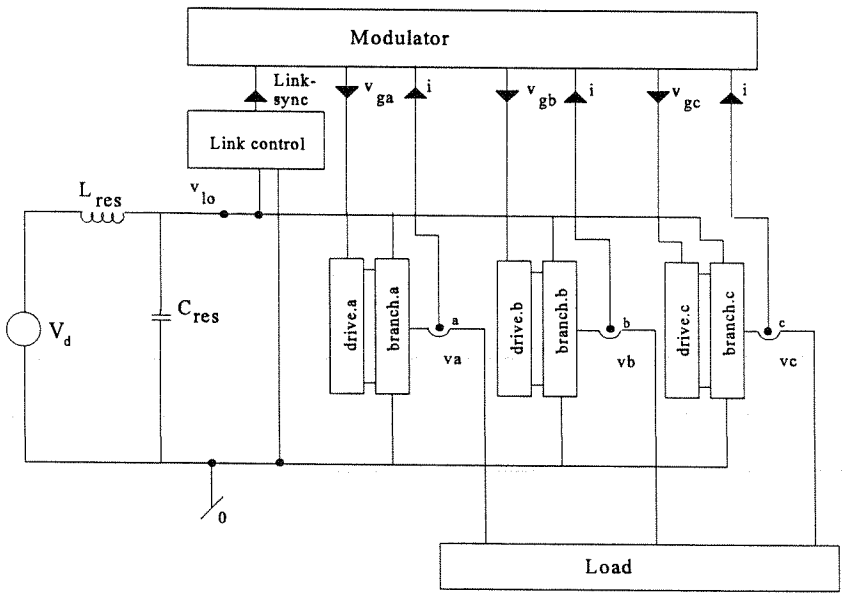


Fig. 4.6. Components and modules used in simulation of the RDCL converter .

The function of each module is described. The link_control module generates the signal that synchronizes the zero voltage link state with the switching of the inverter switches. The drive modules have the same function as a real drive circuit. The ideal switches can easily be replaced by an advanced IGBT model.

The implemented modulation is an ASCM[3] described in 8.1.2. Fig. 4.7 shows the modulator module.

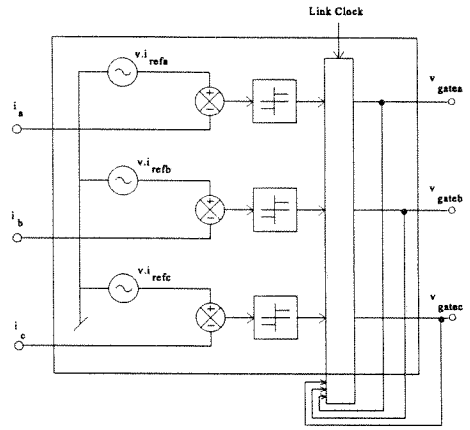


Fig. 4.7. Current regulated delta modulator module.

The converter data for the simulation are shown in Table 4.2.

V_d	620 [V]
Load impedance	7.6 [Ω]
Resonant capacitor (C_{res})	150 [nF]
Resonant inductor (L_{res})	60 [μH]
Resonant impedance (Z_{res})	20 [Ω]
f_{res}	53.5 [kHz]
f_1	50 [Hz]

Table 4.2 Converter data used in simulation of RDCL

The resonant link component values are selected in appendix B.

The RDCL converter is simulated for two fundamental periods of 50 [Hz]. The simulation time of 40 [ms] was about 25 [min]. The simulation was carried out on an HP735-99 [MHz] work station.

The modulation index $m = \hat{V}_{ab}/V_d$ is changed from 0.1 to 1.05, with the load impedance of 7.6 [Ω] there is the following realationship between the phase current and modulation index.

$\hat{I}_a$ [A]	4.7	11.7	23.6	35.4	47.1	49.5
m	0.1	0.25	0.5	0.75	1.0	1.05

[3]Adjacent State Current Modulator, ASCM

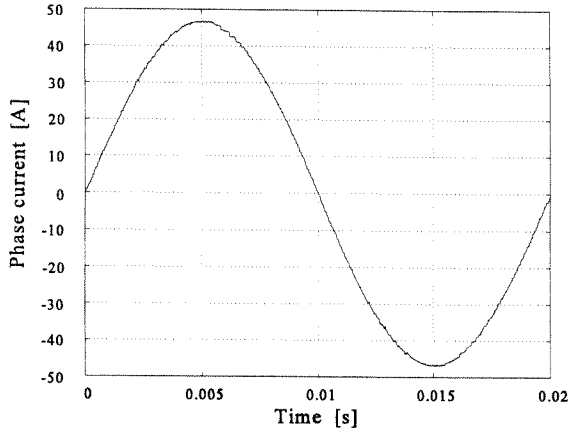


Fig. 4.8 Phase current of RDCL converter

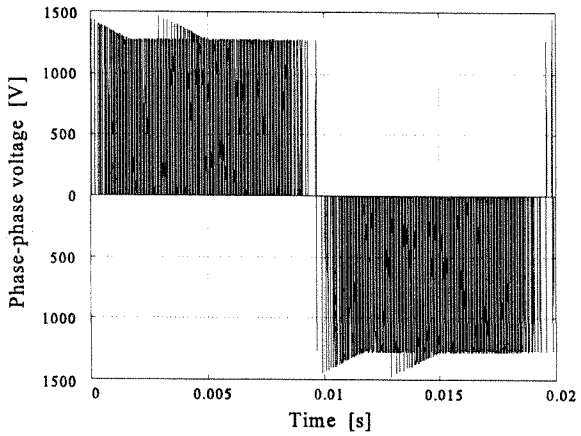
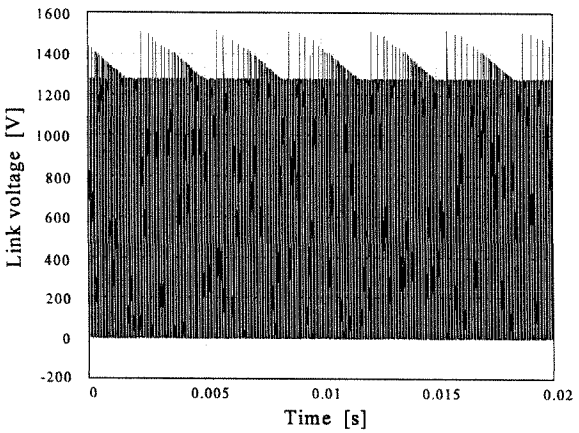


Fig 4.9 Phase-phase voltage of RDCL converter



4.10 Link-voltage of RDCL converter

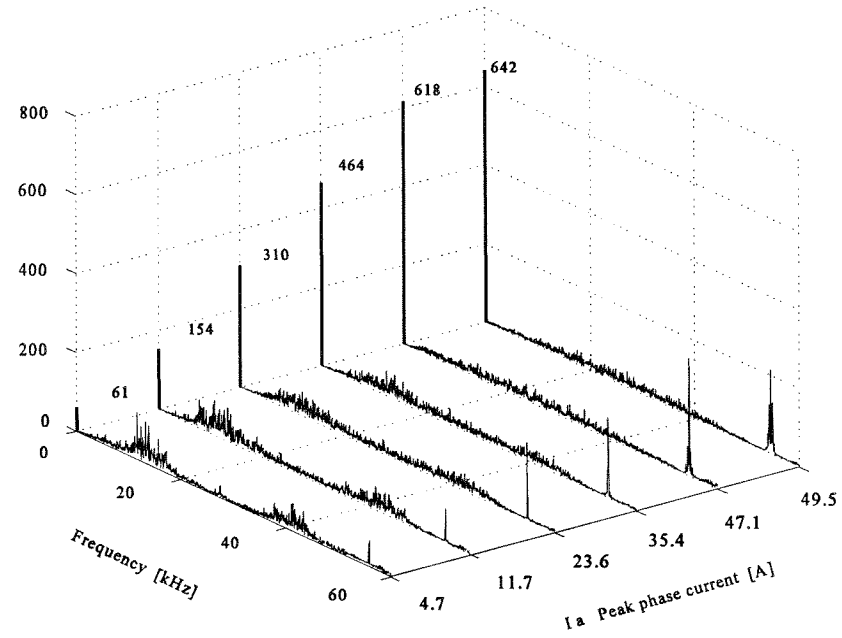


Fig 4.11 Phase-phase voltage amplitude spectrum of RDCL converter

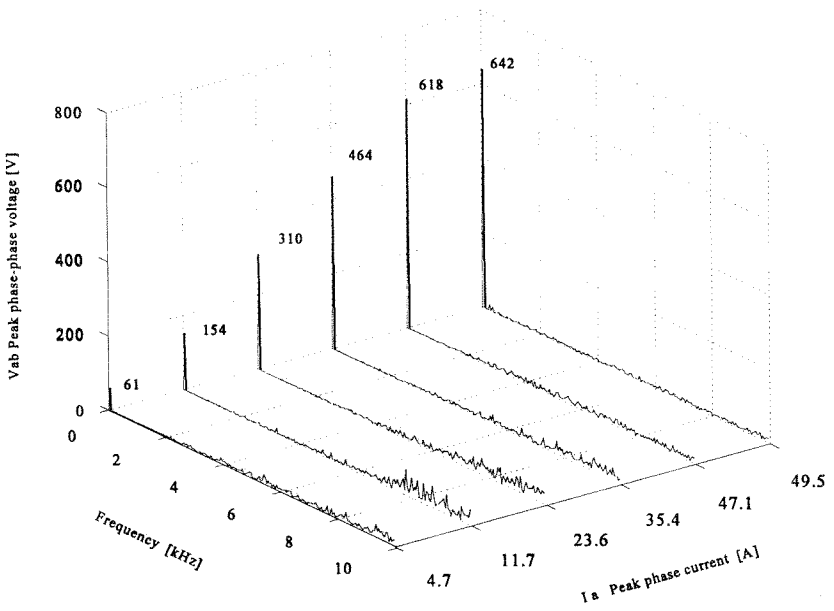


Fig. 4.12 Phase-phase voltage amplitude spectrum of RDCL converter

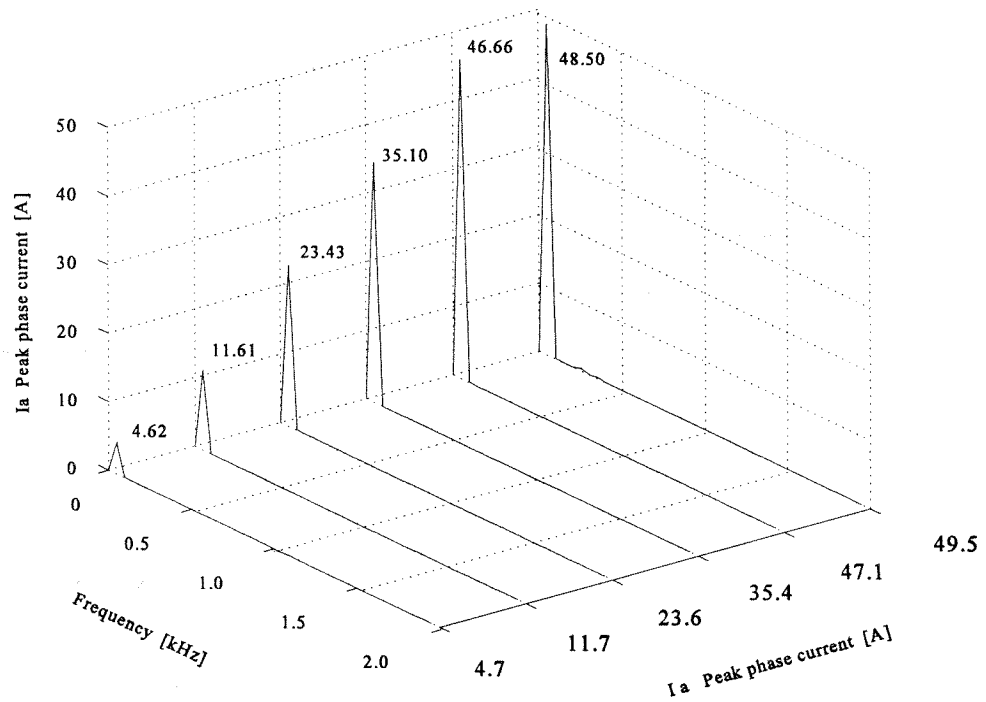


Fig. 4.13 Peak phase current amplitude spectrum of RDCL

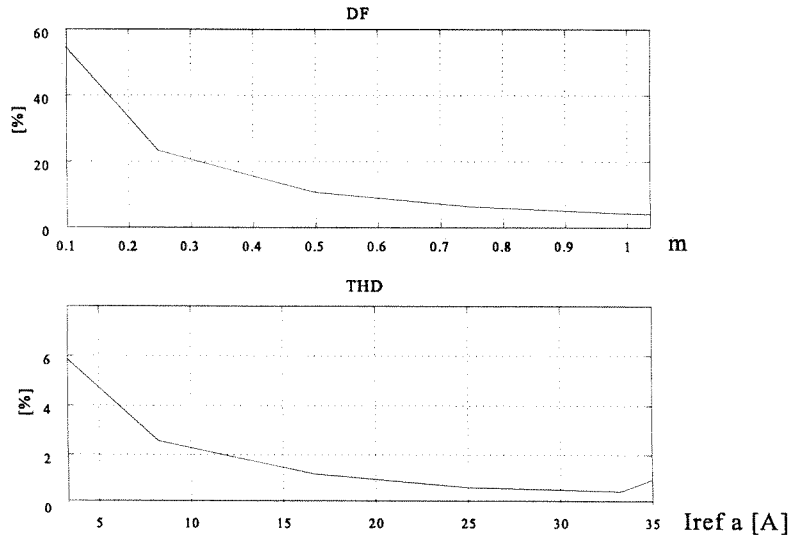


Fig. 4.14 DF and THD of the RDCL as function og modulation index and the effective phase current.

I_{eff} phase a	33.01 [A]
I_{eff} phase a ref.	33.30 [A]
$V_{(1)}$ fundamental of v_{ab}, V_d = 620 [V]	618 [V]
V_{lo} peak link voltage amplitude	1519 [V]
DF	4.28 [%]
THD	0.54 [%]
Cos (ϕ)	0.8

Table 4.3 Calculated key numbers from the converter simulation.

4.1.3 Discussion

The description of the RDCL converter link has shown that at no load the resonant link voltage oscillates between 0 and $2V_d$ using the proper initial conditions. This gives the opportunity of turning the inverter switches on/off at zero voltage and in this way eliminating the switching losses. If the resonant link is loaded, it is still possible to obtain the zero voltage condition but the peak voltage is dependent on the load current. A high load current change generates a high resonant voltage peak which for the simulated converter was 1519 [V] at nominal current. It is desirable to make the link voltage peak undependent of the load current. The peak voltage can be limited by selection a low resonant impedance but peak current is then increased. It is discovered that a way to control the link voltage is to select proper initial conditions of the resonant capacitor voltage. This way of controlling the link voltage peak is investigated further in the chapter 4.2. The RDCL output voltage load dependency is properly also generating subharmonic due to the voltage changes, but due to the long simulation time this is not investigated further. The frequency spectrum of the output voltage shows that there are switching frequencies below 3 [kHz], and this is quite typical for this type of modulator used, but considered the average switching frequency is around 20 [kHz], this is not good compared to PWM converters. Therefore, in chapter 6 the possibility of making a resonant PWM converter is investigated.

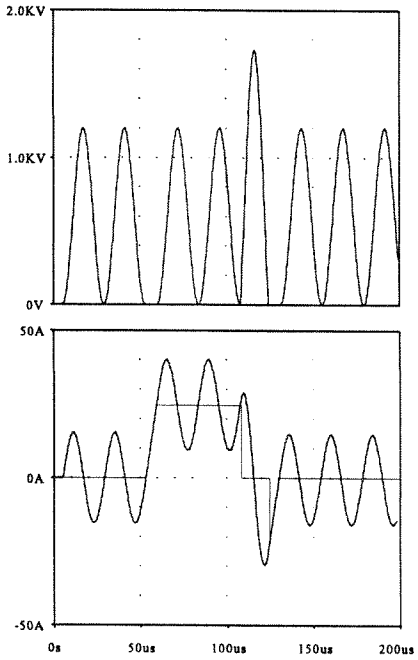
4.2 Parallel resonant DC link converter with link voltage peak control (RDCLVPC)

The resonant DC link converter described in section 4.1 has a load dependent link voltage amplitude. If the converter is not loaded, the link voltage peak is ideally two times the DC link voltage, but loaded the voltage peak can be much higher. The normal way to limit the link amplitude is to clamp the voltage and the link voltage clamp can be active or passive. The active link voltage clamp uses additional switches, diodes, and capacitors, and the passive one adds a transformer and diodes. Here a new way of controlling the link peak voltage without additional power electronic components is proposed, and this is done by adjusting the initial conditions of the resonant circuit.

4.2.1 Operation principle of the RDCLVPC

In order to control the resonant link voltage amplitude, it is necessary to control the resonant circuit energy. The resonant circuit energy is transferred to the resonant capacitor when the link current decreases, which is shown in Fig 4.4.a., mode 4. The only way to stop the increases in the link voltage amplitude is to insure that the changes in link current don't increase the resonant capacitor energy. Already in section 4.1.1 is described how resonant capacitor energy can be decreased. The result of this is non-zero voltage switching.

The following describes how the link amplitude can be controlled when there are no bounds by the zero voltage switching condition. It is allowed that the converter switches are turned on or off shortly before or after the zero voltage condition. This means the load current I_{do} is impressed before or after the zero voltage condition.



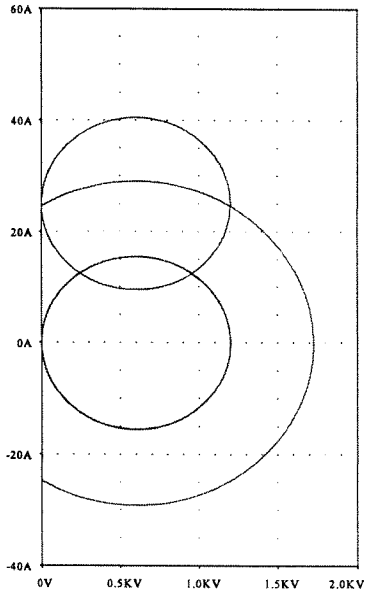


Fig. 4.15a A load change in the resonant circuit. Time plots of V_{cres}, i_{diode} and i_{Lres}

Fig. 4.15b Phase plane plots of i_{Lres} versus V_{cres}

Fig. 4.15 shows the amplitude of voltage v_{Cres} earlier shown in Fig. 4.4 when the link current is changed.

The trajectories after the load current is impressed have the following properties:

- The center of the circle, given by the trajectories, is $(V_d, I_{do}Z_{res})$.
- The radius of the circle is the distance from where the old and the new circle collide to the center of the circle.

Given those properties it is easy to determine the trajectory given by a load current. At the same time it is possible to control the amplitude of V_{Cres} at different loads, simply by selecting a proper instant to impress the load current.
In Appendix C an expression for the time instant a load change should be impressed. This ensures that the V_{Cres} always oscillates between 0 and twice V_d. The reference of the time instant (t_{im}) is the time at zero voltage of V_{Cres}.

The expression is:

$$\sin(\alpha) = \frac{I_{do} Z_{res}}{2 V_d} \qquad \textbf{(4.2)}$$

where

α : The angle, before V_{Cres} reaches zero voltage, indicates the time instant the load current change should be impressed on the DC-resonant link .

The voltage amplitude, at the instant the DC link load current is changed, is given by

$$\Delta V = V_d(1 - \cos\alpha) \qquad \textbf{(4.3)}$$

Fig. 4.16 shows the voltage amplitude when the converter transistor is turned on and off, using the proposed control strategy, denoted voltage peak control.

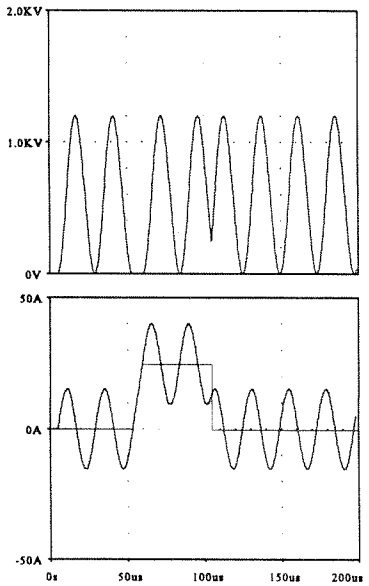


Fig. 4.16a. A load changes in the resonant circuit using VPC. Time plots of V_{cres} and i_{Lres}

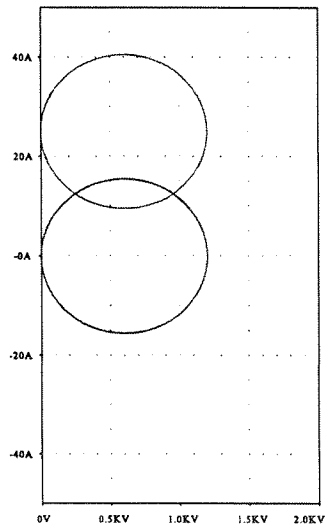


Fig. 4.16b. Phase plane plots of i_{Lres} versus V_{cres}

4.4.2 Simulation of RDCLVPC

Except for the VPC strategy is the simulation program identical to the one used for the RDCL and no component values has been changed. The converter data for the simulation is shown in table 4.4

V_d	620 [V]
Load impedance	7.6 [Ω]
Resonant capacitor (C_{res})	150 [nF]
Resonant inductor (L_{res})	60 [μH]
Resonant impedance (Z_{res})	20.0 [Ω]
f_{res}	53.05 [kHz]
f_1	50 [Hz]

Table 4.4 Converter data used in simulation of RDCLVPC

The modulation index $m = \hat{V}_{ab}/V_d$ is changed from 0.1 to 1.05. With the load impedance of 7.6 [Ω] there is the following relationship between the phase current and modulation index.

$\hat{I}_a$ [A]	4.7	11.7	23.6	35.4	47.1	49.5
m	0.1	0.25	0.5	0.75	1.0	1.05

The RDCLVPC converter is simulated for one fundamental period. In tables 4.5 key numbers for the converter are extracted.

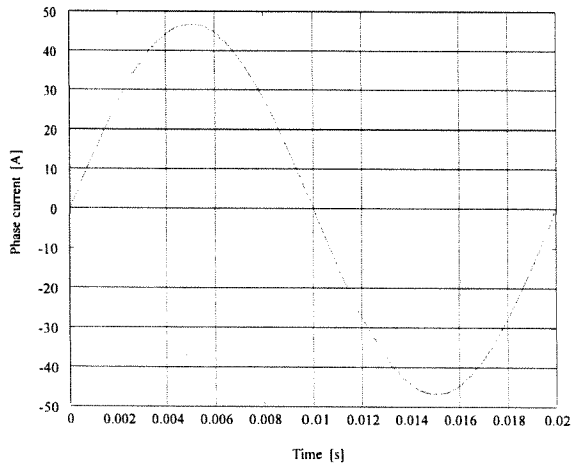


Fig. 4.17 Phase current of RDCLVPC converter

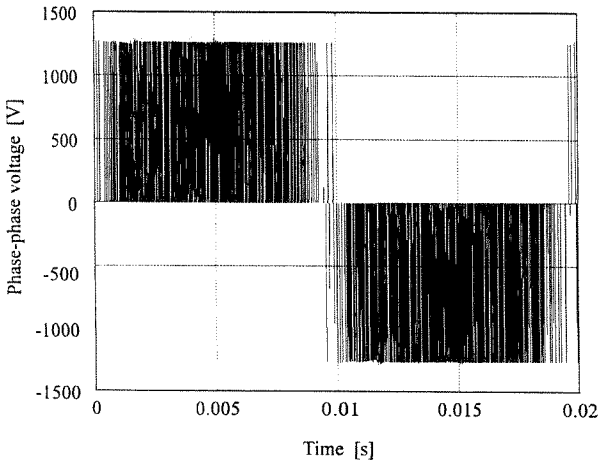
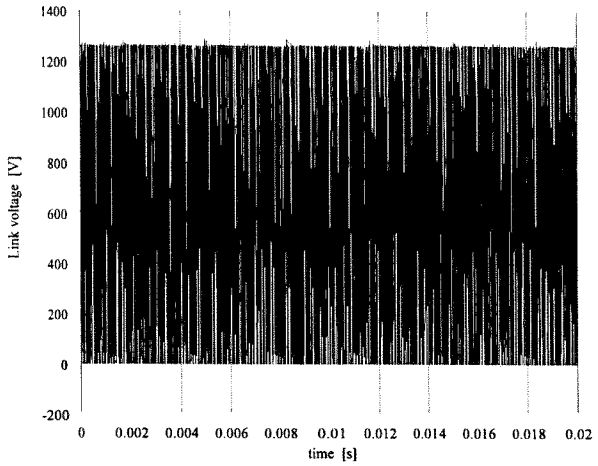


Fig 4.18 Phase-phase voltage of RDCLVPC converter



4.19 Link-voltage of RDCLVPC converter

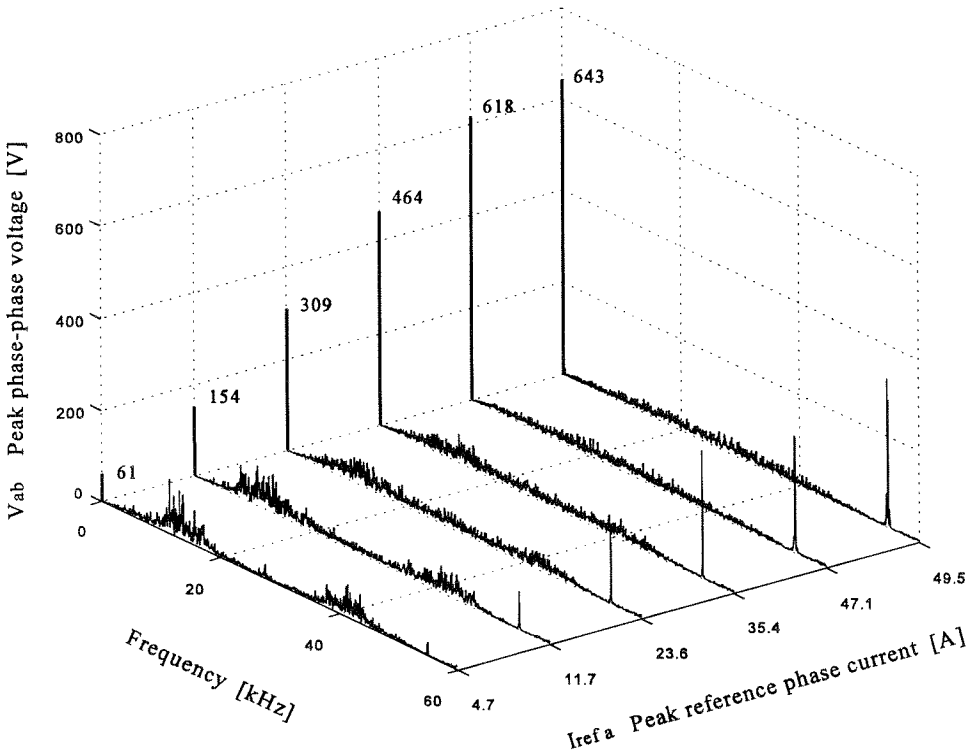


Fig 4.20 Phase-phase voltage amplitude spectrum of RDCLVPC converter

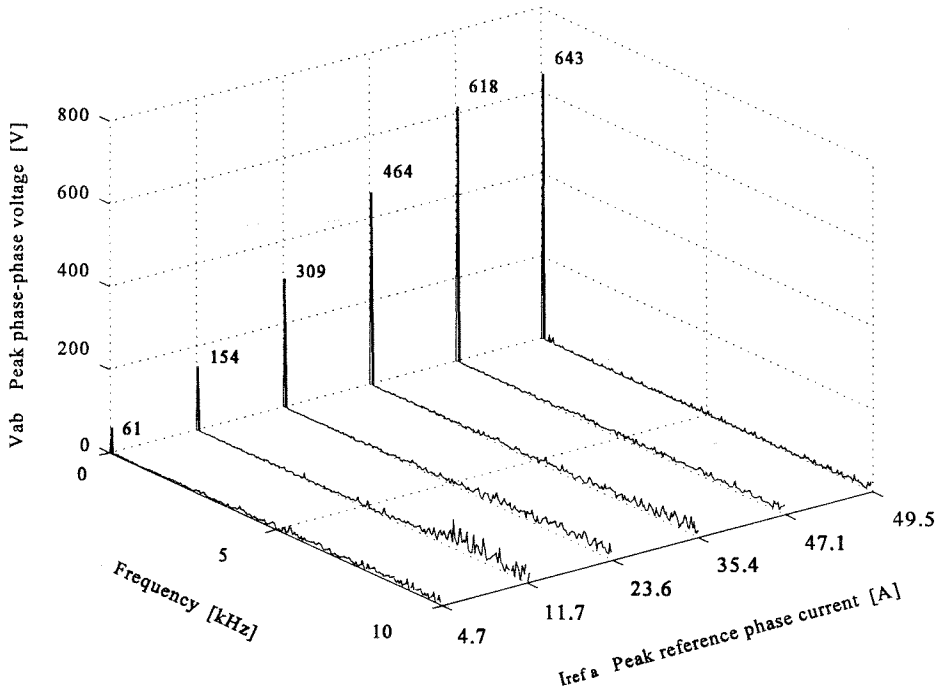


Fig. 4.21 Phase-phase voltage amplitude spectrum of RDCLVPC converter

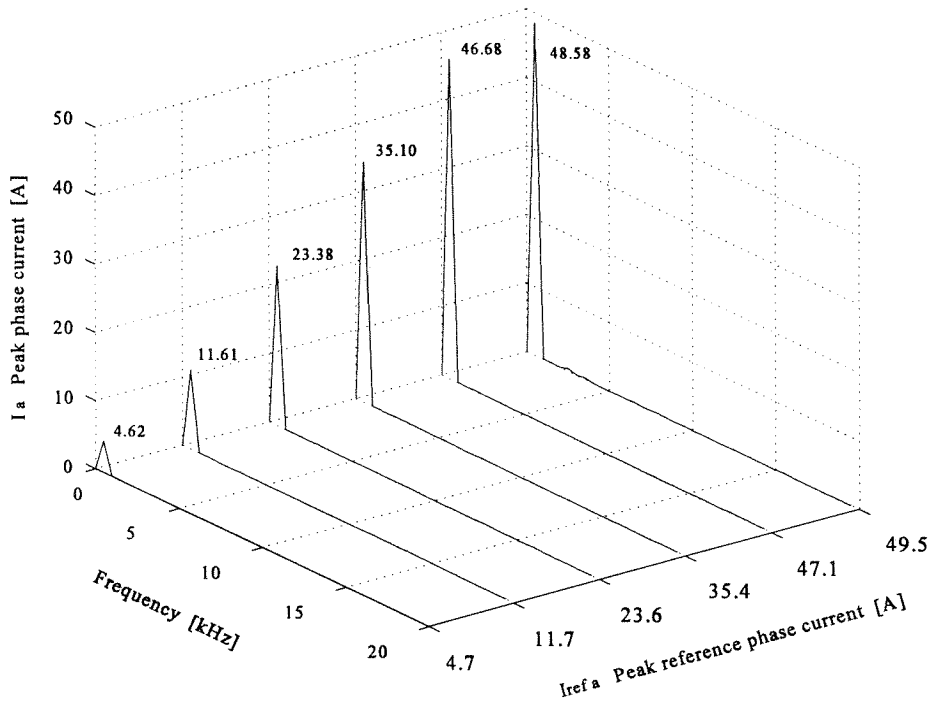


Fig. 4.22 Peak phase current amplitude spectrum of RDCLVPC

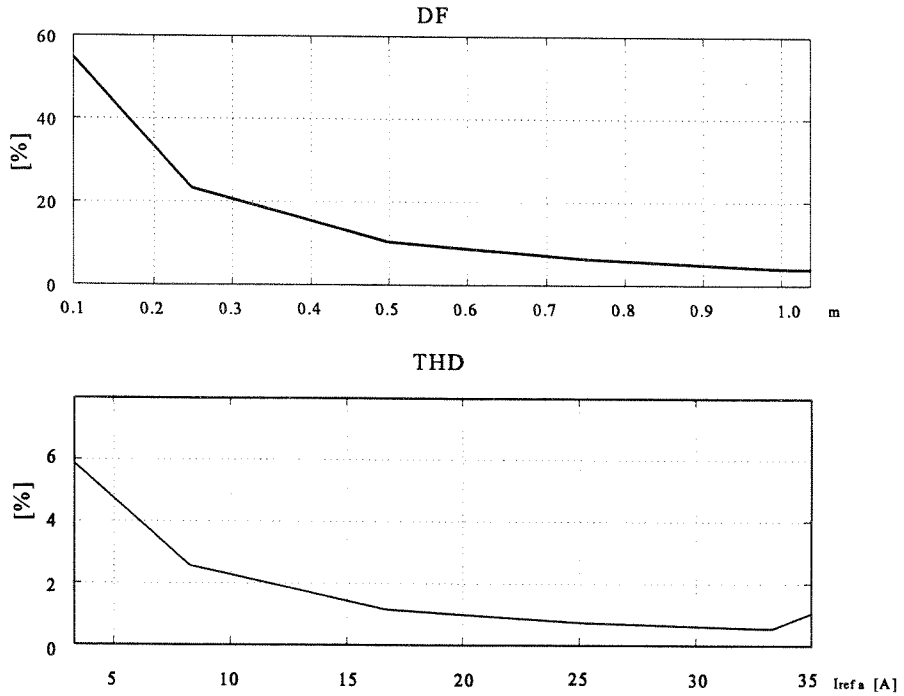


Fig. 4.23 DF and THD of the RDCLVPC

I_{eff} phase a	33.02 [A]
I_{eff} phase a ref.	33.30 [A]
$V_{(1)}$ fundamental of v_{ab}, V_d = 620 [V]	618 [V]
V_{lo} peak link voltage amplitude	1289 [V]
DF	4.17 [%]
THD	0.54 [%]
Cos (ϕ)	0.8

Table 4.5 Simulated key numbers from the converter simulation

4.2.3 Discussion

It has been shown in theory that it is possible to control the resonant DC link voltage to oscillate between 0 and 2 V_d when it is impressed load currents with out the use of clamp circuits. The control strategy is called voltage peak control and it is used in a simulation of a three-phase converter. The simulation shows that the resonant link voltage is well controlled. The voltage peak level is kept below 2.08 times the DC link voltage and this is 1290 [V] using a 620 [V] link voltage. Without the proposed converter control strategy the voltage peak level is 2.80 times the link voltage, giving a link voltage amplitude of 1736 [V].

The selected values of the link impedance have not been optimized. It is expected that an optimization would lower the link voltage amplitude below 2.08 times of the link voltage, the improvement is expected to arrive from a more efficiency control of the converter switches.

The disadvantages using this control method are that some resonant link switching is no longer done at zero voltage. This introduce hard switching losses as in the standard PWM-VSI.

The energy dissipated in the resonant converter switches is limited because at the moment the hard switching occurs, the voltage is low, and the number of lossy switching is low.

The Fourier spectrum of the phase-phase voltage is very similar to that of the RDCL converter, but due to the almost constant voltage peaks the subharmonic content is expected to be small compared to the RDCL.

4.3 Conclusion

In section 4.1 is dealt with the RDCL converter proposed by Divan/1/. The link voltage of the converter proposed by Divan is unfortunately load dependent. In the non-loaded case the link voltage amplitude is twice the DC link voltage, in load change situations the link voltage amplitude could be much higher. This high link voltage amplitude is a server disadvantage. To solve the problem Divan and Mertens/35/ have proposed a clamp circuit that reduces the link voltage amplitude to about 1.3 times the DC link voltage. There are numerous suggestions besides Divan's proposal to solve the voltage amplitude problem, but common to all of them is that they use extra link components. Clearly the link components create losses. If switches are used in the resonant link, they are subjected to relative high stress because they have to work at the link frequency.

In section 4.2 a converter is proposed that limits the link voltage amplitude to 2.08 times the DC link voltage and without the use of extra link components. The converter is named resonant DC link converter with link voltage peak control, RDCLVPC, the converter circuit is analyzed and the converter is simulated using a resistive-inductive load. The simulation shows the proposed control strategy works well.

5

Clamped parallel resonant DC link converters

This chapter investigates resonant converters that limit the output voltage by clamping the link voltage. The clamp circuit can be active or passive. Two converters are described, one active and one passive.

The active clamped resonant converter is analyzed. First the operation of the active clamped resonant link is described, and a simulation of the converter is done. In the analysis all components are idealized and the active components are modeled by variable resistors. In the simulation of the active converter the same resonant component values are used as in chapter 4, which describes the parallel resonant DC-link converters. The passive clamped resonant converter is described briefly.

5.1 Parallel active clamped resonant DC link converter

In the active clamped resonant DC link converter the link voltage amplitude, v_{do}, is limited below two times V_d by a clamp circuit. The ACRDCL[1] is shown in Fig. 5.1.

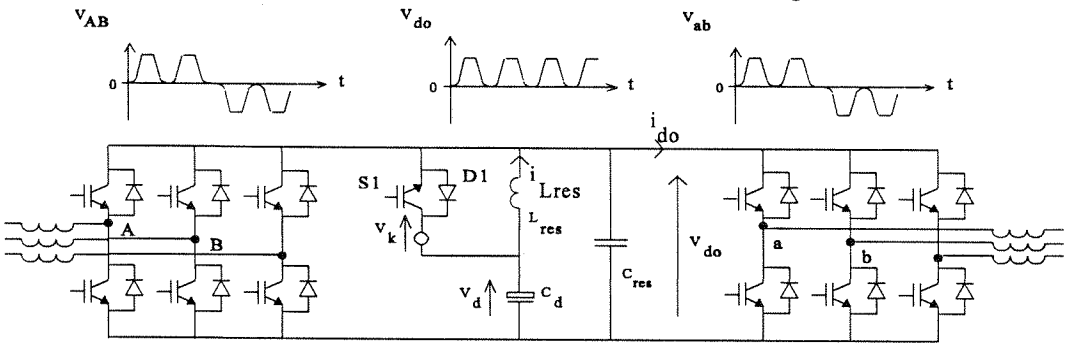


Fig. 5.1 Active clamped resonant DC link converters in AC-AC converter.

The link voltage amplitude v_{do} is clamped by the voltages V_k+V_d if the diode D1 conducts. During the period diode D1 conducts, the inductor L_{res} discharges. In order to enable the next resonant cycle to reach zero voltage, the inductor L_{res} must be recharged. Switch S1 is turned on during the recharge of the inductor.

A simple control strategy of the active clamp is found by an energy consideration. Energy flowing into the clamp source V_k must be equal to the energy flowing out. Assuming V_k to be constant the control strategy only needs one current sensor. The current sensor measures the current through the clamp circuit.

[1] Active Clamped parallel Resonant DC Link converter, ACRDCL

The active clamp circuit uses an ideal voltage source, which is done for the convince of simulation simplicity. In a realization of the clamp circuit voltage sources are often avoided, due to the circuit complexity and costs. In /34/ several suggestions from the literature describe how to realize the clamp circuit using a capacitor.

5.1.1 Link operation of the ACRDCL

No load change condition of active clamped resonant link

Compared to the parallel resonant converters described in chapter 4, the voltage clamp circuit has added new states. Fig. 5.2 shows a phase plot of the resonant inductor link current versus link voltage.

The clamp circuit is active in state 2 and state 3. During state 2 the resonant inductor discharges, and during state 3 the resonant inductor recharges. The resonant inductor current changes in such a way a condition for a new resonant state 4 is obtained.
The circuit analyzed is shown in Fig. 5.3. The DC link current i_{do} is zero, the equivalent diagram of the inverter bridge is found in Appendix F. Simulation results are shown in Fig. 5.4.a and 5.4.b.

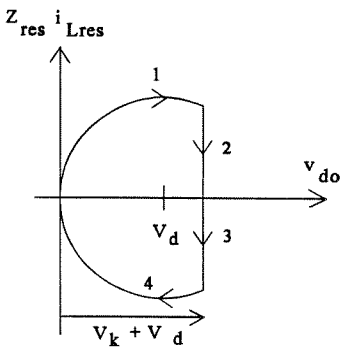


Fig. 5.2 Phase plane plot of the active clamped resonant DC link

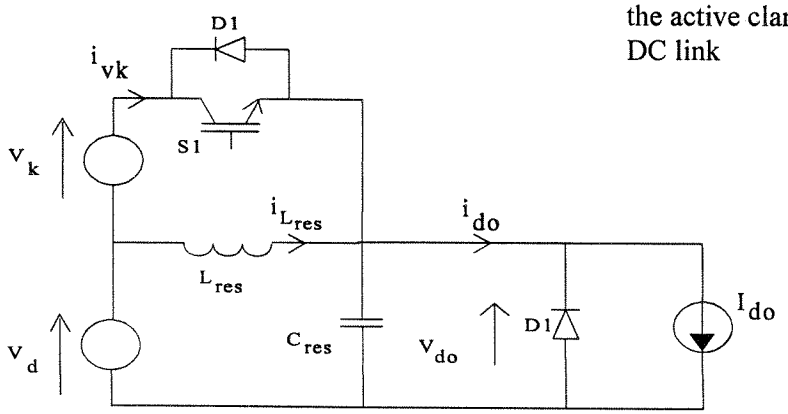


Fig. 5.3 Equivalent diagram of active clamped DC link converter.

State 1 After the voltage step V_d a resonant cycle begins.

State 2 v_{do} reaches the voltage clamp level ($V_d + V_k$). Inductor L_{res} discharges through the diode D1. $\Delta i_{L_{res}} = \frac{V_k}{L_{res}} \Delta t_2$.

State 3 The switch S1 conducts and the inductor L_{res} is charged. $\Delta i_{L_{res}} = \frac{V_k}{L_{res}} \Delta t_3$.

State 4 A resonant cycle can begin: v_{do} changes from ($V_k + V_d$) to zero

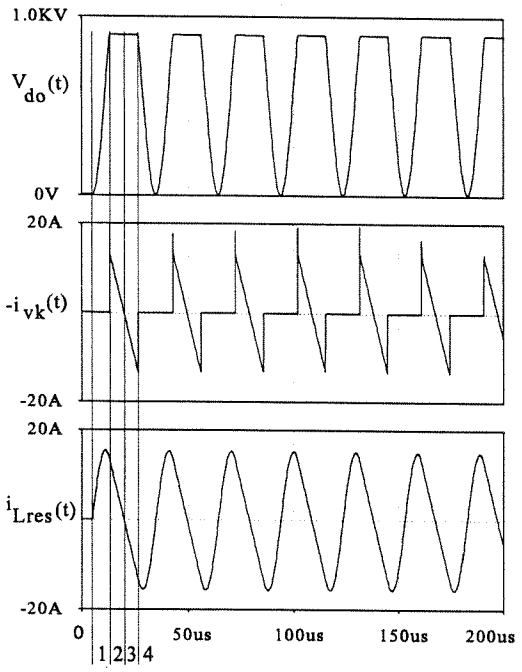


Fig. 5.4a Simulated curves of the circuit shown Fig. 5.3. Curves are v_{do}, i_{vk} and i_{Lres}.

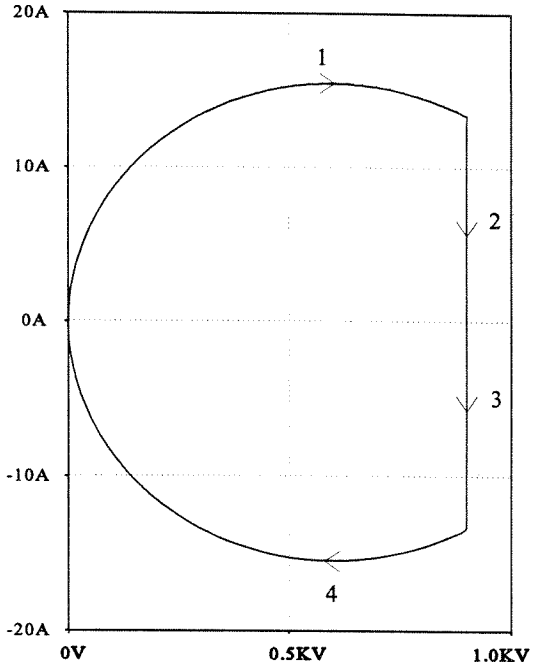


Fig. 5.4b Phase plane plot of i_{Lres} versus v_{do}.

In chapter 4, which describes the RDCL, the resonant link frequency is dependent on the resonant frequency of the resonant tank and the duration of the zero voltage interval. In the ACRDCL the link frequency is also dependent on duration of the clamping interval of state 2 and 3. The duration of the clamping interval is dependent on clamp voltage V_k, Δi_{vk} and the resonant inductor L_{res}. A decrease in clamp voltage decreases the resonant link frequency. The link frequency dependency of the clamp voltage is shown in Fig 5.5.

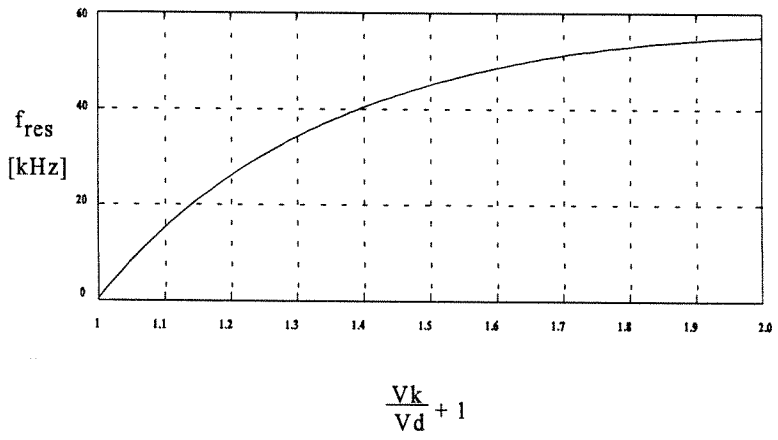


Fig 5.5 Link frequency dependency on clamp factor at fixed resonant component values

The maximum link frequency shown in Fig 5.5 depends on $1+V_k/V_d$, and ω_{res}. The ratio V_k/V_d is changed from 0 to 1. The ω_{res} is determined by L_{res}=53 [uH] and C_{res}=158 [nH] and the values are the same as used in the simulation of the ACRDCL shown later.

If the link is not clamped, the link frequency is 55 [kHz]. In the simulation of the ACRDCL the link voltage is limited to $1.4V_d$. With this clamp level the resonant link frequency is decreased from 55 to 40.4 [kHz]. The resonant link frequency decrease has a negative influence on the converter output voltage harmonic performance.

From the function (D.14) in App. D, the average value of the resonant link voltage, v_{do}, was found independent of the clamp voltage level. The average value of v_{do} is V_d .

Load change condition of active clamped resonant link

The circuit shown in Fig 5.3 is loaded by a pulse current of I_{do}=25 [A]. The load condition and the influence of load changes are considered. The simulation results are shown in Fig. 5.6.a and 5.6.b. The current spikes on i_{vk} and i_{do} are due to simulation errors.

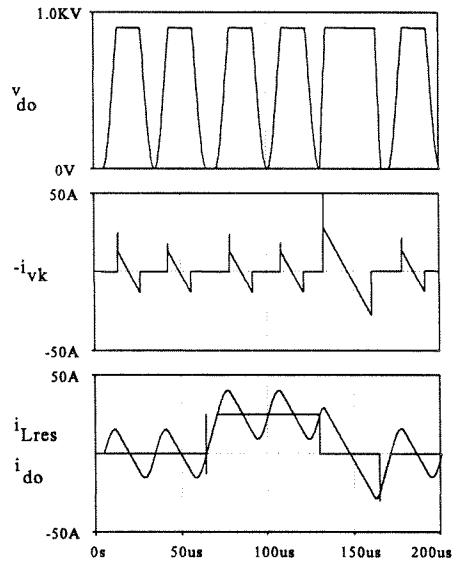


Fig. 5.6a Simulated curves of the circuit shown Fig. 5.3. Curves are v_{do}, i_{vk}, i_{Lres} and i_{do}.

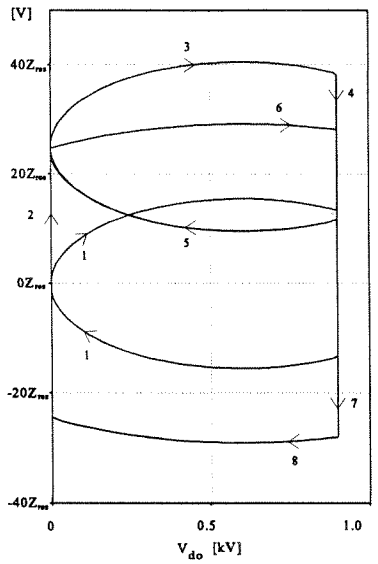


Fig. 5.6b Phase plane plot of $i_{Lres}Z_{res}$ versus v_{do}.

State 1 After the voltage step V_d a resonant cycle begins. Similar to no load situation.

State 2 A current (I_{do}) is impressed on the resonant circuit. D1 conducts until $i_{L_{res}}$ reaches I_{do}.

State 3 A new circle with the radius $V_{res} = V_d$ is drawn by the resonant trajectory in the phase plane.

State 4 v_{do} reaches the clamp voltage level. The voltage clamp time is. $\Delta t_4 = \frac{L_{res}}{V_k} 2\ \Delta i_{vk}$

State 5 This state is similar to State 3.

State 6 The impressed current is removed at $V_{do} = 0$ [V]. A third circle trajectory in the phase plane with a radius $V_{res} = \sqrt{V_d^2 + (Z_{res}\ I_{inv})^2}$ is started.

State 7 The clamp voltage level is reached, and the clamp time is. $\Delta t_7 = \frac{L_{res}}{V_k} 2\ \Delta i_{vk}$. Time interval Δt_7 is longer than the time intervals given by State 4, and the current stress is higher.

State 8 A resonant cycle brings V_{do} to zero voltage. The excess energy absorbed by the resonant circuit by State 6 is removed from the inductor. This is done through diode D1.

Compared to the RDCL converter described in chapter 4, there is no difference in the resonant states when the load current is impressed. The impressed load current increases the resonant inductor energy with $W_{Lres}={}^{1}/_{2}L_{res}I_{do}{}^{2}$. In the situation when the load current decreases, the resonant inductor energy is decreased. In the RDCL the inductor energy is transferred to the resonant capacitor and this generates a link voltage amplitude higher than two times V_d. In the ACRDCL the resonant inductor energy is also transferred to the resonant capacitor, but the clamp circuit prevents that the link voltage amplitude increases above V_d+V_k. The clamp circuit energy is increased, the duration of the clamp interval increases, and the link frequency decreases. The increased duration of the clamp interval has a negative influence on the output voltage spectral performance. It is noted that the load change increases the ${}^{dv}/_{dt}$ of the link voltage.

5.1.2 Simulation of the ACRDCL

The DC-AC part of the AC-AC converter shown in Fig. 5.1 is simulated. The load is an RL network and the parameters used in the simulation are shown in table 5.1.

V_d	620 [V]
V_k	248 [V]
Resonant capacitor C_{res}	158 [nF]
Resonant inductor L_{res}	53 [μH]
$1+V_k/V_d$	1.4
Load impedance	7.6 [Ω]
$\cos(\phi)$	0.8
Resonant impedance Z_{res}	18.3 [Ω]
Resonant frequency f_{res}	55 [kHz]
Fundamental frequency of current reference f_1	50 [Hz]

Table 5.1 Converter data used in simulation of ACRDCL.

The converter is controlled by an adjacent state delta current modulator, described in chapter 8.1.2. The converter control part is identical to the ones used in the simulation of the RDCL and RDCLVPC converters. The active clamp circuit is controlled in such a way the energy flowing into the active clamp is equal to the energy flowing out. The modulation index $m = \hat{V}_{ab}/V_d$ is changed from 0.1 to 1.05. With the load impedance of 7.6 [Ω] there is the following relationship between the phase current and modulation index:

$\hat{I}_a$ [A]	4.7	11.7	23.6	35.4	47.1	49.5
m	0.1	0.25	0.5	0.75	1.0	1.05

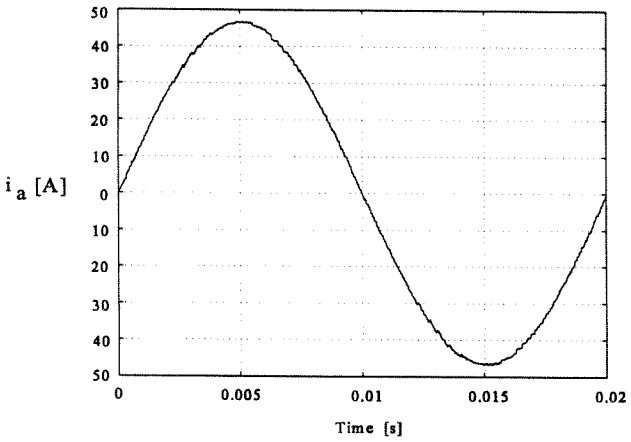


Fig 5.7 Phase current of ACRDCL converter

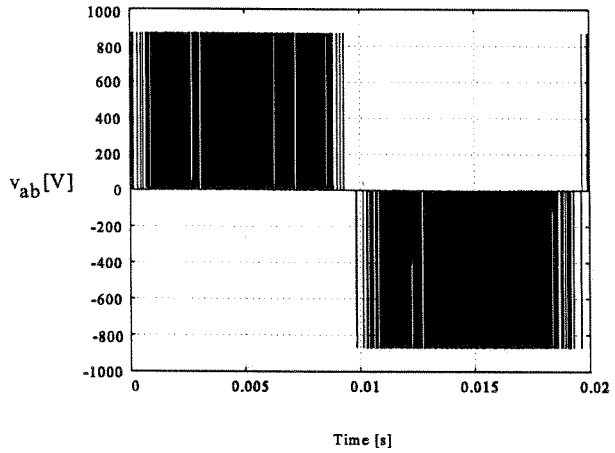


Fig 5.8 Phase-phase voltage of ACRDCL converter

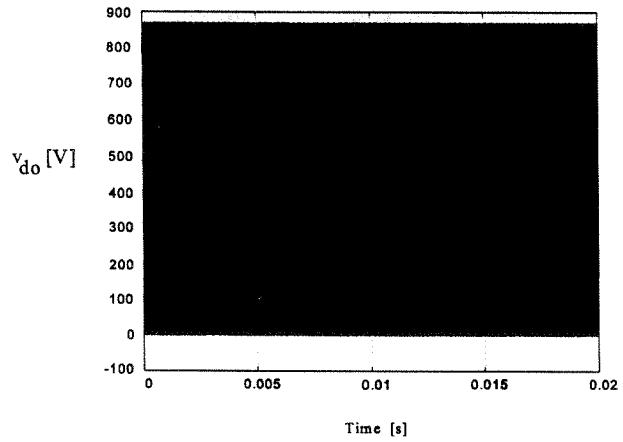


Fig 5.9 Link voltage of ACRDCL converter

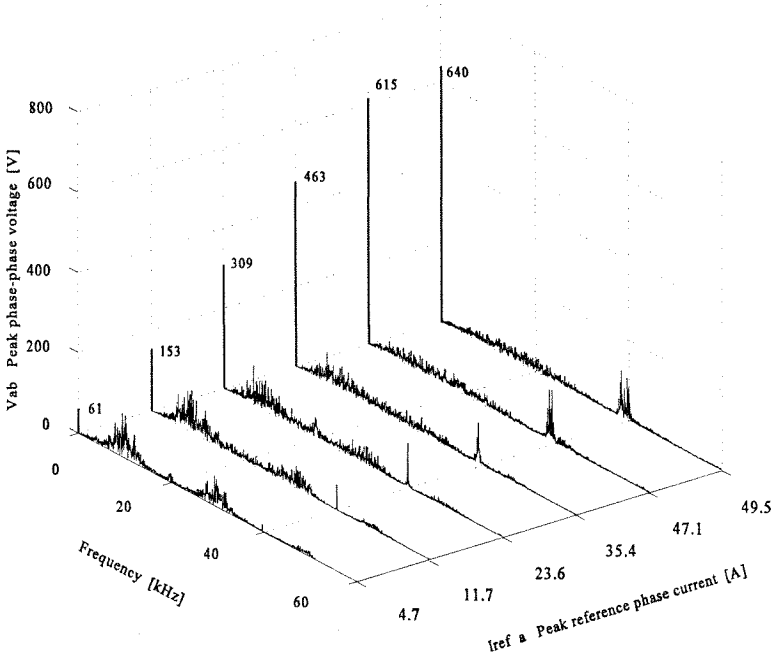


Fig 5.10 Phase-phase voltage amplitude spectrum of ACRDCL converter

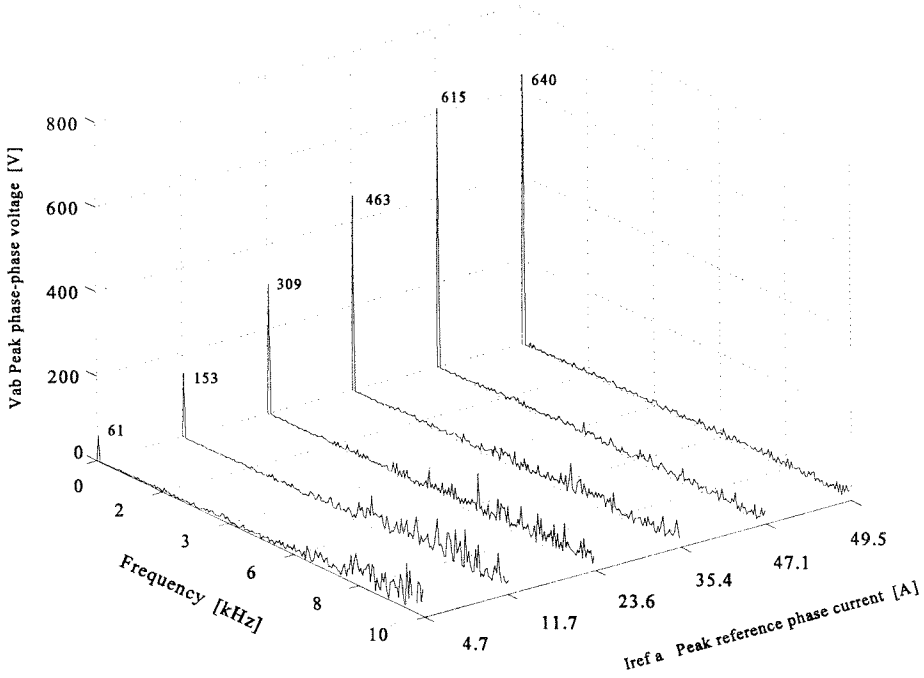


Fig. 5.11 Phase-phase voltage amplitude spectrum of ACRDCL converter

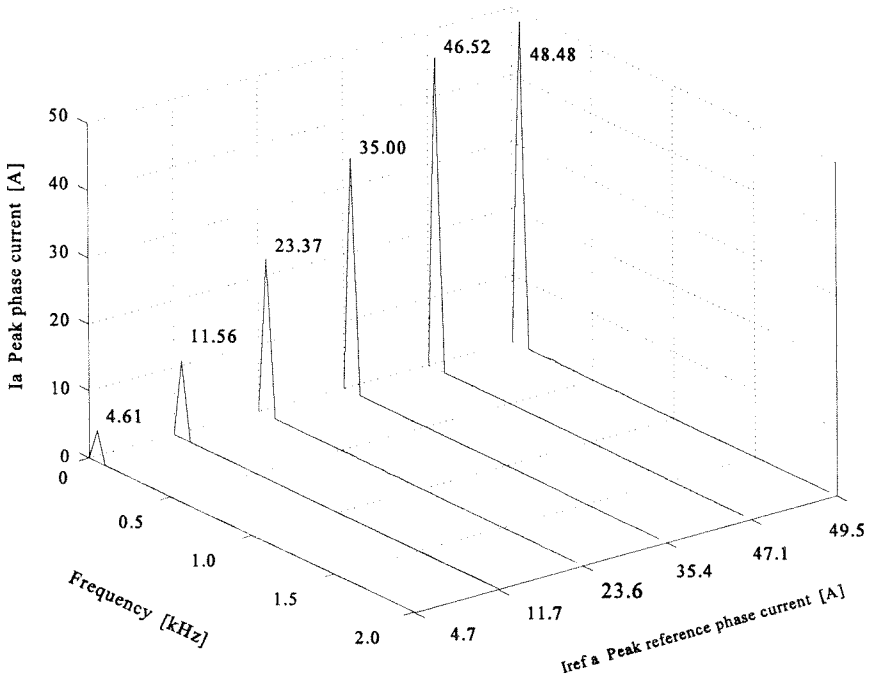


Fig 5.12 Peak phase current spectrum of ACRDCL converter

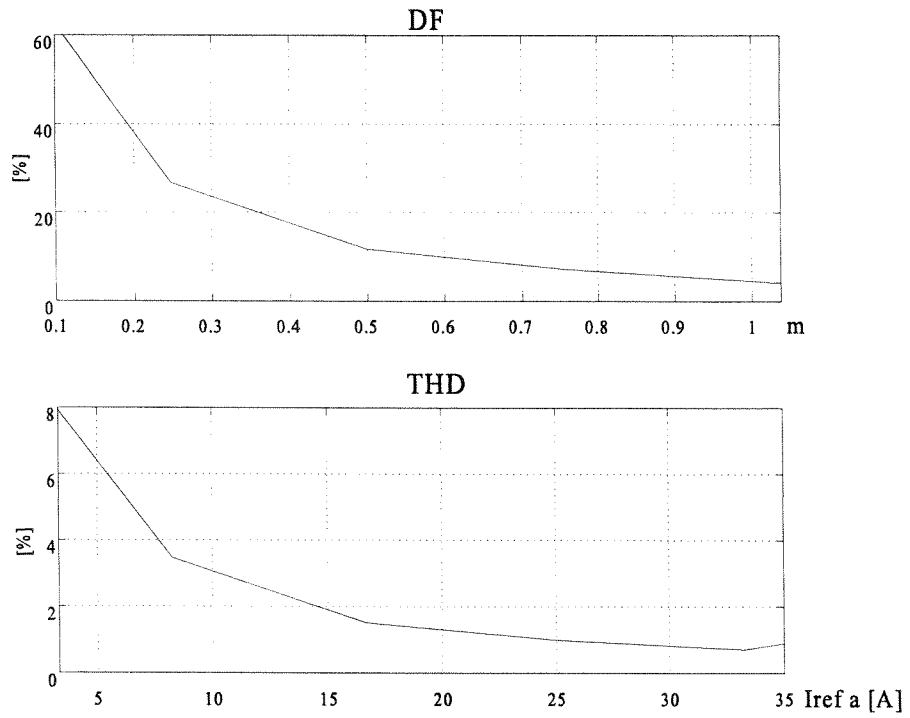


Fig. 5.13 DF and THD index of the ACRDCL converter as a function of modulation index m and the effective phase current.

I_{eff} phase a	32.9 [A]
I_{eff} phase a ref.	33.3 [A]
$V_{(1)}$ fundamental of v_{ab}, V_d = 620 [V]	615 [V]
V_{lo} peak link voltage amplitude	868 [V]
DF	4.5 [%]
THD	0.7 [%]

Table 5.2 Simulated key numbers from the converter simulation with modulation index m=1.0.

5.1.3 Discussion

The ACRDCL converter operation is described at no load change situation, and a formula describing the link frequency dependency, on clamp factor, is derived. The average link voltage is found to be V_d, and independent of the clamp level. With the chosen values of L_{res}, C_{res}, and a clamp level equal to 1.4, it is calculated that the link frequency of v_{do} is decreased from 55 [kHz], which is the natural resonant frequency of the resonant circuit, to 40.3 [kHz]. The simulation of the ACRDCL verifies that the link frequency is close to 40 [kHz].

The ACRDCL converter link operation is described, in load change situations, and it is shown that a load current step decreases the link frequency. The simulation of the ACRDCL shows the link frequency decreases at higher load currents.

Comparison of ACRDCL converters DF and THD indexes with the RDCL and RDCLVPC converters shows worse performance. The higher DF and THD values of the ACRDCL are due to the relatively lower link frequency. The simulation of the ACRDCL, RDCL and RDCLVPC was done with the same resonant circuit components. To improve ACRDCL performance the natural frequency of the resonant circuit must be increased. The dv_{do}/dt of the ACRDCL would be relatively high and it is shown that the dv/dt is load dependent.

The clamp level of the ACRDCL is K=1.4. With a link voltage V_d of 620 [V] the link voltage amplitude of v_{do} is 868 [V]. This is substantially lower than the link voltages amplitude of 1520 [V] for the RDCL with K=2.45 and the link voltage amplitude of 1290 of the RDCLVPC converter with K=2.08.

5.2 Passively clamped parallel resonant DC link converter

The passively clamped parallel resonant DC link converter is described in /22/. The link clamp circuit is a transformer with an diode as shown in Fig 5.14, the clamp is regenerative. The transformer clamps the link voltage v_{do} to a clamp level of 2.02. The clamp energy is transferred back to V_d.

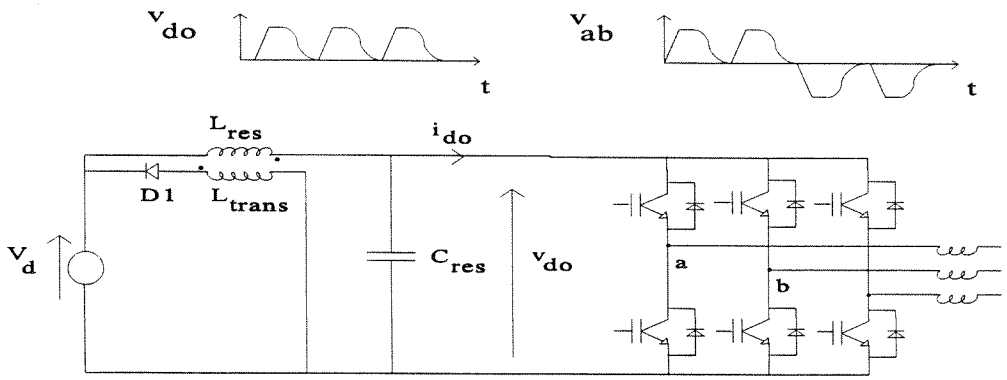


Fig 5.14 Passively clamped parallel resonant DC link converter

The lowest link voltage clamp factor obtained in /22/ is 2.02. The link voltage amplitude is 1252 [V] with a link voltage V_d =620 [V]. The converter is interesting due to its apparent simplicity compared to the ACRDCL. In /22/ the design of the clamp transformer is described as complex. The clamping level is close to the clamping level of the RDCLVPC and the RDCLVPC uses fewer components.

5.3 Conclusion

In the chapter the actively clamped resonant DC link converter is described. The advantage of this converter is a low peak phase-phase voltages around $1.4V_d$. It has been shown that the clamp level has influence on the link frequency, a lower clamp level gives a lower link frequency. The resonant link frequency must be increased in order to have a spectral performance equal to the non-clamped resonant converter. The clamp circuit uses one switch and diode and one capacitor, the switch is subjected to high stress/35/ because it works at the resonant frequency that is much higher than the frequency of inverter switches. Instead of the active clamp a passive clamp circuit with only a transformator and a diode/22/ is proposed.. By using a well-designed transformator it is possible to obtain a clamp factor of 2.02. However, in/22/ the transformer design is described as complex and it is decided not to deal with the passively clamped parallel resonant DC link converter further.

6

Parallel resonant PWM converters

This chapter deals with the type of resonant converters which uses PWM and has zero voltage switching of the main switches. Three converters which combine PWM and soft switching abilities are presented, 'Notch commutated three-phase PWM converter' /5/, /14/, 'Zero switching losses PWM converter with resonant circuit' /15/, and the 'Modified ACRDCL converter for PWM operation'. The last converter is not seen presented in any paper.

The two first converters are described briefly, and the third converter, the 'Modified ACRDCL converter for PWM operation', is analyzed. First the link operation is described then a simulation of the converter is done. All converter components are assumed ideal and the active components are modeled by simple switches. The PWM strategy of the modified ACRDCL converter is described in 8.2. In the end of the chapter there is a discussion of the three converters.

6.1 Notch commutated three-phase PWM converter

The 'Notch Commutated Three-Phase PWM Converter' is presented in /14/ and is able to generate PWM pulses and zero voltage switching of the converter switches. In the delta modulated converter described in chapter 4 and 5 the converter switching was synchronized with the zero voltage periods of the link. Now the zero voltage periods do not happen at discrete instants but are syncronized with a pulse from the pulse width modulator. The syncronization pulse, from the pulse width modulator, is commanded a short time before the converter switches change to a new state. In this way the resonant link circuit can decrease the link voltage to zero and the converter switching happens at zero voltage. Fig. 6.1 shows the converter.

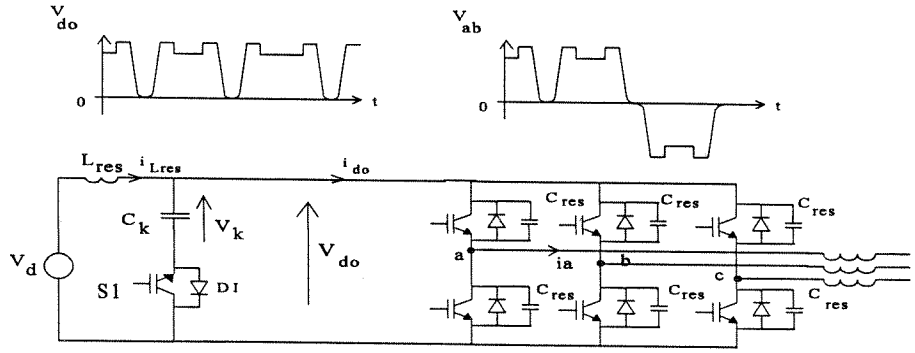


Fig. 6.1 Notch commutated PWM converter

The converter link circuit makes a synchronization with the converter switches possible. Until a commutation is wanted, the switch S1 is off. Then S1 turns on and decreases the resonant inductor current to an initial value which ensures a resonant period with ZVS. The time it takes to reach the initial current is determined by the clamp voltage, V_k, and the size of the inductor L_{res}.

The inductor value is limited by the trade off between a low resonant current, and the clamp

voltage V_k must be somewhat low due to a lossy turn on of S1. The energy in C_{res} is dissipated in S1 at turn-on, and the clamp level is therefore low. In /14/ the clamp level is about 1.2.

The converter has the desirable features of PWM, but there are turn-on losses when S1 is turned on due to a discharge of the C_{res} capacitors. Therefore, this topology is not investigated further.

6.2 Zero switching loss PWM converter with resonant circuits

This converter offers PWM and zero voltage switching as the notch commutated converter described earlier, but the voltage stress on the converter components is lower. The converter is presented in /15/. Fig. 6.2 shows the converter.

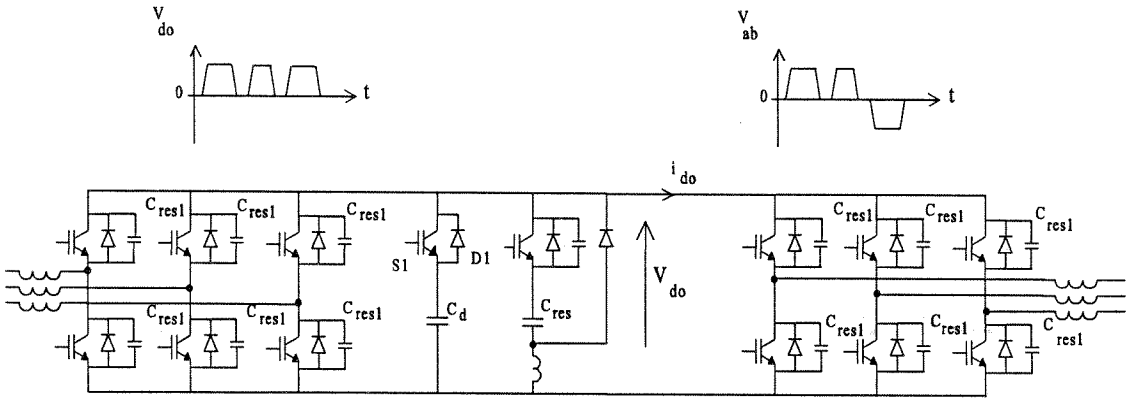


Fig. 6.2 Zero switching loss PWM converter with resonant circuits.

The voltage stress on the converter switches is similar to PWM-VSI, but the topology requires 2 switches and 3 diodes compared to the notch converters' 1 transistor and 1 diode.
The resonant circuit is different from the other resonant circuits described. It uses two resonant states, determined by changing the resonant capacitor value. Changing a resonant state makes a link oscillation possible without any DC-link voltage overshoot ($V_k = 0$). However, there is a higher current stress on the converter components. Due to the high number of switches and the current stress on the devices, the topology is not investigated further.

6.3 Modified ACRDCL for PWM operation

This converter offers zero voltage switching of the converter switches and PWM operation of the converter. It is an extension of the ACRDCL described in chapter 5.1, with an extra switch and diode. Fig. 6.3 shows the converter.

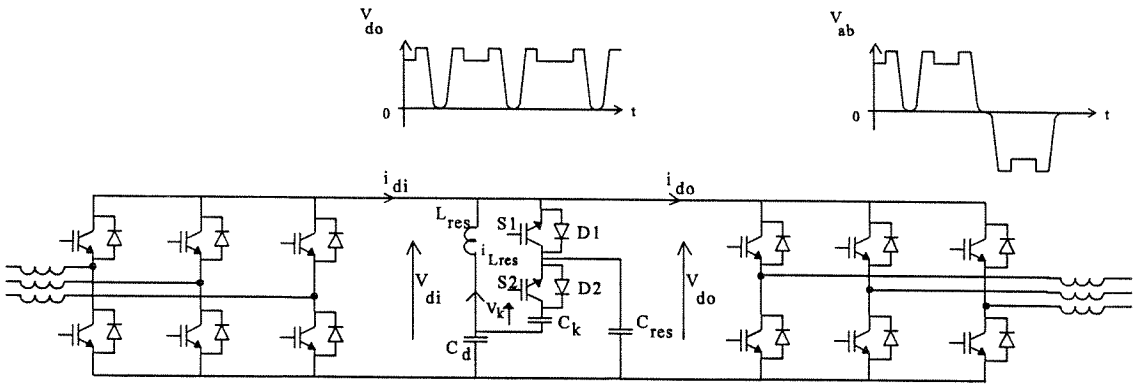


Fig. 6.3 Modified ACRDCL for PWM operation.

The voltage stress on the converter switches is limited to V_d, until a converter switching is needed. Before a converter switching takes place, the energy of the resonant inductor L_{res} must increase. The resonant inductor energy is supplied from the clamp source V_k. During the charging interval of the resonant inductor the link voltage $v_{do} = V_d + V_k$.
Finishing the resonant cycles it is necessary to clamp the voltage at $V_d + V_k$. During this clamp interval is the energy applied during the charging interval of the inductor transferred back, to the clamp circuit.

In this paragraph an analysis of the converter is done. First, the link operation is described and simulations of the converter at the load side are shown.

6.3.1 Link operation of the MACRDCL

No load change condition of MACRDCL

Operation of the PWM MACRDCL is described by a single phase equivalent circuit derived in app. F of a three-phase converter.

The three-phase inductive load is assumed to have a time constant so large that load current is considered constant during a few switching of the DC link voltage. The circuit described is shown in Fig. 6.4.

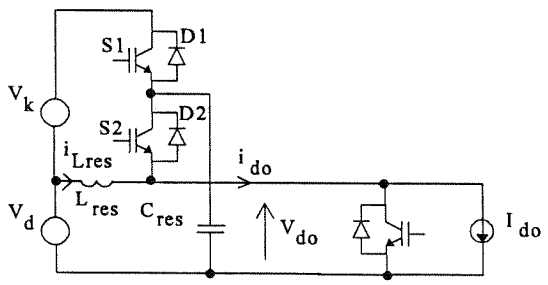


Fig. 6.4 Equivalent of PWM MACRDCL converter with load.

Simulation results are shown in Fig. 6.5.a and 6.5.b.

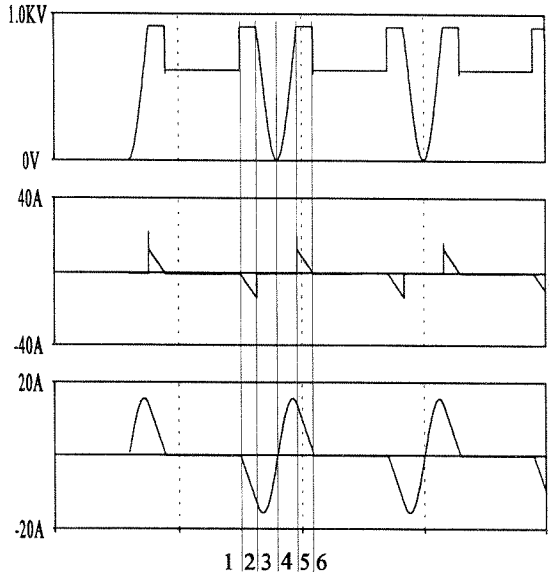


Fig. 6.5a Simulated curves of the circuit shown in Fig. 6.4.

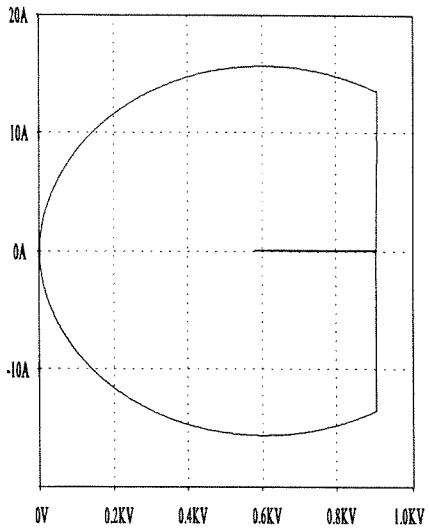


Fig. 6.5b Phase plane plot of i_{Lres} versus v_{do}.

State 1: Steady state operation, link voltage v_{do} is V_d and no resonant action happens. The voltage above C_{res} is $V_d + V_k$ because S1 is on.

State 2: S2 turns on under ZCS conditions. Link voltage v_{do} is raised to $V_d + V_k$ and energy is transferred to L_{res}. The energy of L_{res} increases to a level which ensures that the resonant cycle oscillates v_{do} to zero voltage.

State 3: S1 turns off, and the link is now able to resonate v_{do} to zero voltage. Ensuring zero voltage switching of the converter switches.

State 4: Diode 2 conducts, and the voltage v_{do} increases until the clamp level $V_d + V_k$ is reached.

State 5: D1 and D2 conduct, and S1 is turned on and S2 is turned off. Energy is transferred back to the clamp voltage source, and when L_{res} is discharged, D1 and D2 stop conducting.

State 6: Is similar to state 1.

During the switching interval no other switching can take place and this has a negative effect on the converter performance. A resonant converter switching has a relative long time duration compared to hard switching converters. The influences of the resonant switching on the output voltage amplitude are discussed now, and in the simulation of the MACRDCL the influence on the voltage quality is shown. The converter output voltage is described by the modulation index m that is defined as $m=2V_a/V_{do}=V_{ab}/V_{do}$. V_a is the amplitude of the converter branch potential and V_{ab} is the amplitude of the phase-phase voltage.

A PWM strategy is chosen in chapter 8.2. The scheme has a minimum number of DC link switching relative to the converter switching frequency. Fig. 6.5 shows that a certain distance between each zero link voltage interval is necessary. Unfortunately, the necessary distance between the zero link voltage intervals limits the PWM operation, and the result is a limited range of the modulation index of the converter. There is a lower limit of the modulation index m given by:

$$m_{min} = \frac{2t_{min}}{T_{sw}} \qquad (6.1)$$

t_{min} is the time duration of the clamping interval eg. state 2 or state 5 in Fig. 6.5 and T_{sw} is the converter switching time. Formula (6.1) is found from Fig 6.6a showing time t_1 and t_2 for a 60 [°] period. They are calculated from the modulation function shown in chapter 8.2. The times t_1 and t_2 are used to calculate the duty cycles. Branch potential at branch a and b is shown in fig. 6.6b. The branch potential v_a is proportional to $t_1 + t_2$ shown in Fig. 6.6a in the interval of 0-60 [°] and $mT_{sw} = t_1+t_2$.To ensure the necessary distance between two zero link voltage intervals the low values of t_1 and t_2 are limited to t_{min}.

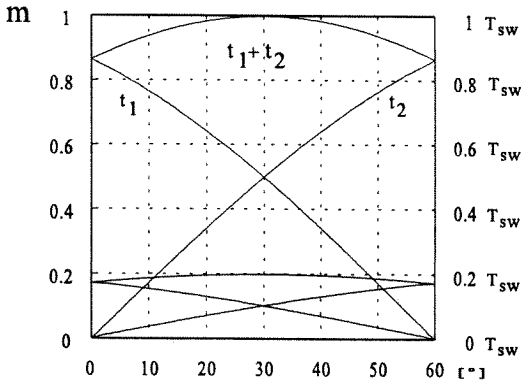


Fig. 6.6a PWM duty cycle times for a 60° interval.

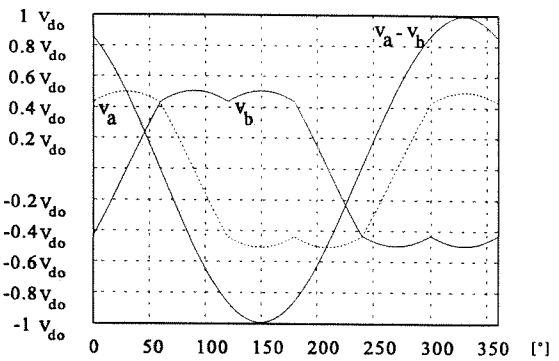


Fig. 6.6b Branch potentials of converter and phase-phase voltage shown in Fig. 6.3.

In fig 6.6a t_1 and t_2 are shown for a modulation index of m=0.2. If t_1 and t_2 had a lower boundary of t_{min} the lower limit of the modulation m is given by (6.1).

At modulation indexes near 1 it is also necessary to limit the duty cycle. In Fig 6.6a $t_1 + t_2$ are shown, and it must be ensured that $t_1 + t_2$ always is smaller than $T_{sw} - 2t_{min}$ to prevent two resonate switching intervals to collide. This gives a maximum modulation index that is smaller than 1. A solution is to set the duty cycle of converter branch a to 1 and just control the duty cycle of branch b. This solution introduces harmonics, but the output voltage amplitude is not reduced. The actual limitation of modulation index is described in the simulation of the MACRDCL converter.

Load change condition of PWM MACRDCL

The circuit shown in Fig 6.4 is loaded by a pulse current of $I_{inv} = 25$ [A]. The influence of the load is considered. The simulation results are shown in Fig. 6.7.a and 6.7.b.

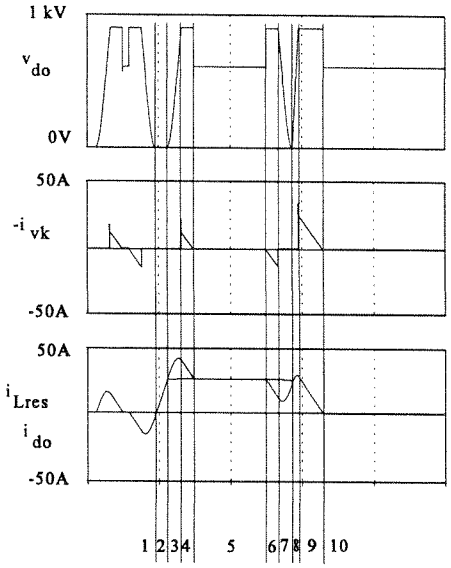


Fig. 6.7.a Simulated curves of the circuit shown in Fig. 6.4.

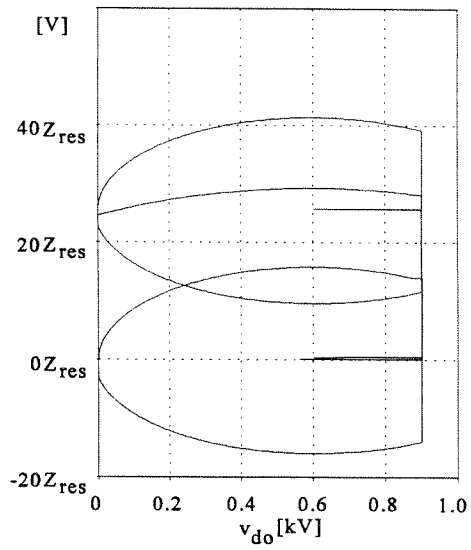


Fig. 6.7.b Phase plane plot of i_{Lres} versus v_{do}.

State 1: Last action was the turn off of S1 and the link is now able to resonate V_{do} to zero voltage.

State 2: V_{do} reaches zero voltage and a load current is impressed on the link circuit. The anti parallel diode turns on and V_{do} is clamped to zero voltage until i_{Lres} reaches the value of i_{do}. A resonant cyclus commence.

State 3: Diode 2 conducts. The voltage V_{do} increases resonant until the clamp level $V_d + V_k$ is reached.

State 4: D1 and D2 conduct, and S1 is turned on and S2 is turned off. Energy is transferred back to the clamp voltage source, and when L_{res} is discharged, D1 and D2 stop conducting.

State 5: Steady state operation, link voltage v_{do} is V_d and no resonant action happens. The C_{res} voltage value is $V_d + V_k$ because S1 is on.

State 6: S2 turns on under ZCS conditions. Link voltage v_{do} is raised to $V_d + V_k$ and energy is transfered to L_{res}. The energy of L_{res} increases to a level that ensures that$_{do}$ v oscillates to zero voltage.

State 7: S1 turns off and the link is now able to resonate V_{Cres} to zero voltage. Ensuring low zero voltage switching of the converter switches.

State 8: The impressed load current changes to zero current and C_{res} is chaged.The trajectory of the new circle in the phase plane is $V_{res} = \sqrt{V_d^2 + (Z_{res}\, I_{do})^2}$.

State 9: is similar to state 4.

State 10: is similar to state 5.

In the ACRDCL converter described in chapter 5 it was possible to control the energy flow into the clamp circuit, the clamp voltage source could therefore be replaced by a capacitor. Using the MACRDCL it is also possible to control the energy flow. The energy can be moved between the clamp and link source through the resonant inductor. The resonant inductor L_{res} stores clamp source energy in eg. state 6 and transports the energy to the link source V_d during the short circuit interval shown in state 2 fig. 6.7.a.

6.3.2 Simulation of the MACRDCL

The DC-AC part of the AC-AC converter shown in Fig. 6.3 is simulated. The load is a RL

network and the parameters used in the simulations are shown in Table 6.1.

V_d	620 [V]
V_k	248 [V]
Resonant capacitor C_{res}	250 [nF]
Resonant inductor L_{res}	15 [μH]
$1+V_k/V_d$	1.4
Load impedance	7.6 [Ω]
$\cos(\phi)$	0.8
Resonant impedance Z_{res}	7,75 [Ω]
Resonant frequency f_{res}	82 [kHz]
Fundamental frequency of current reference f_1	50 [Hz]

Table 6.1 Converter data used in simulation of MACRDCL

The converter is controlled by a PWM strategy described in chapter 8.2, and the simulation was carried out in SABER.

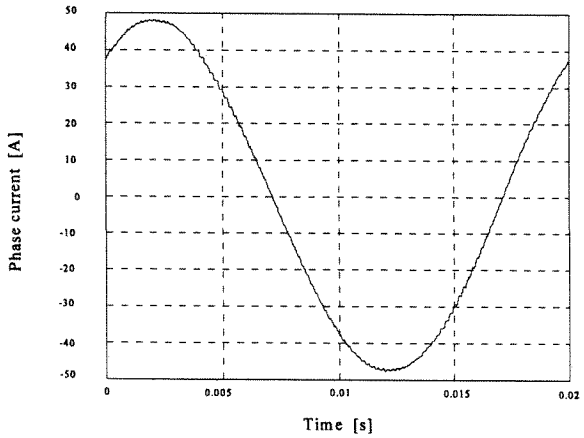


Fig. 6.8 Phase current of MACRDCL converter

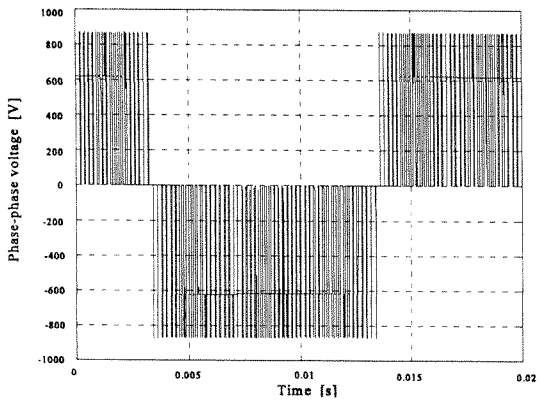


Fig. 6.9 Phase-phase voltage of MACRDCL converter

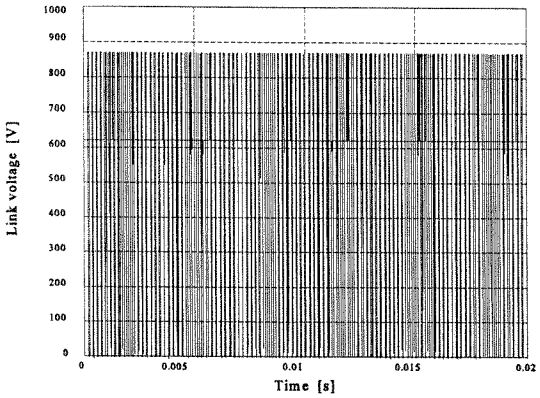


Fig. 6.10 Link-voltage of MACRDCL converter

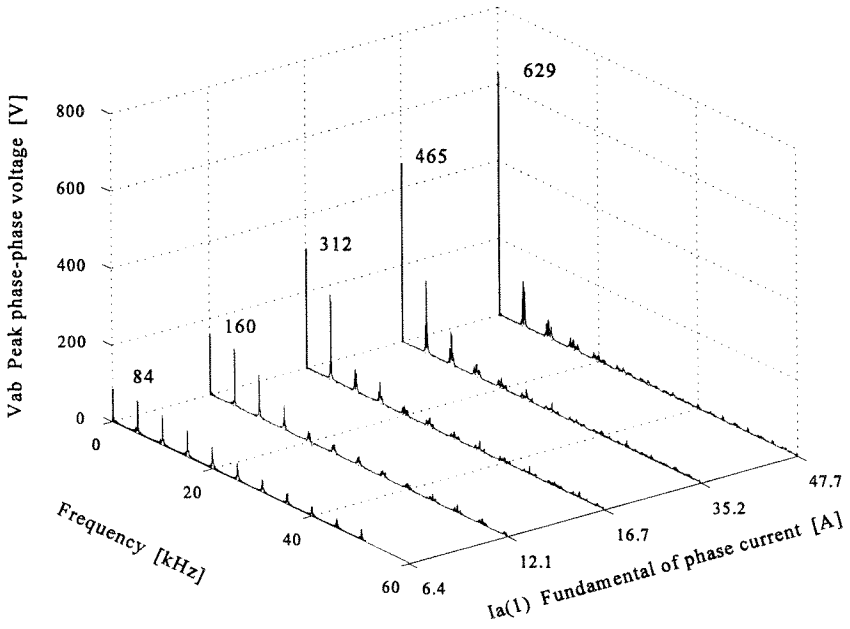


Fig. 6.11 Phase-phase voltage amplitude spectrum of the MACRDCL converter

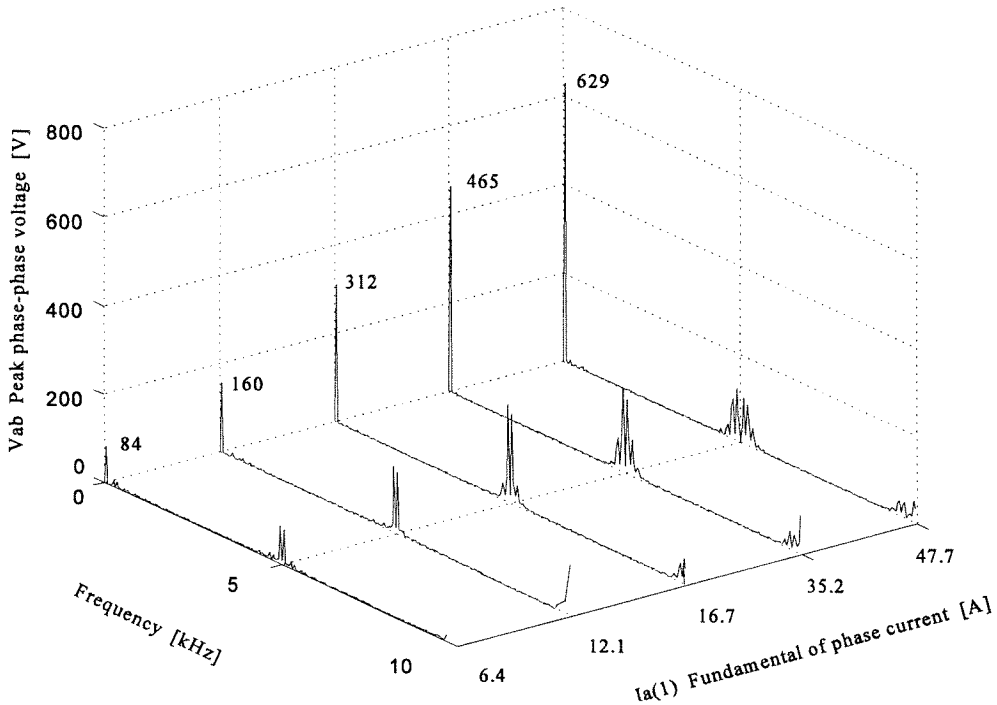


Fig. 6.12 Phase-phase voltage amplitude spectrum of MACRDCL converter

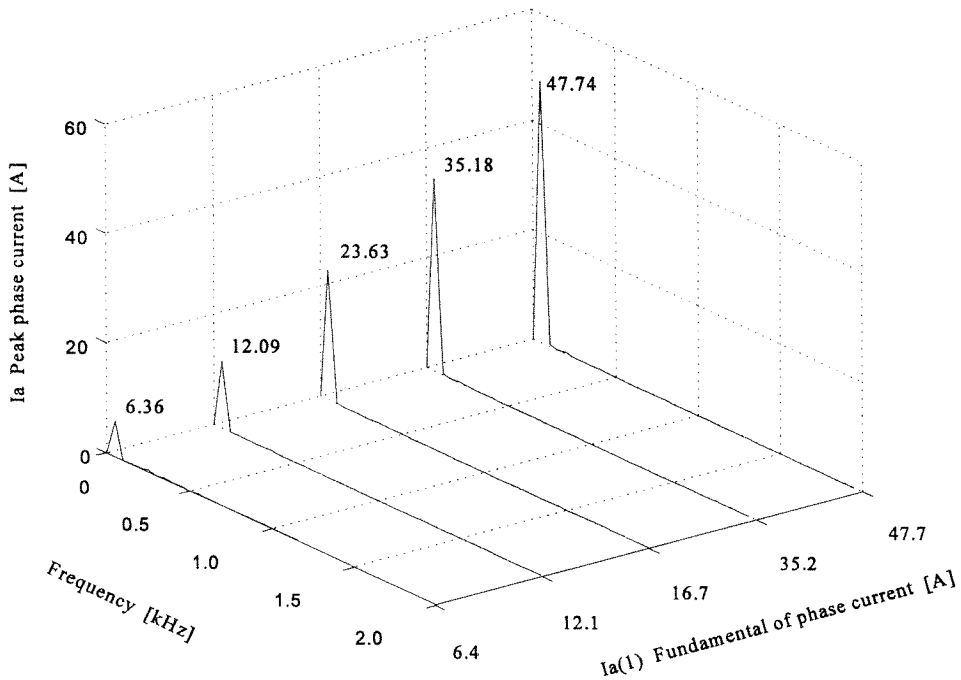


Fig. 6.13 Peak phase current spectrum of MACRDCL converter

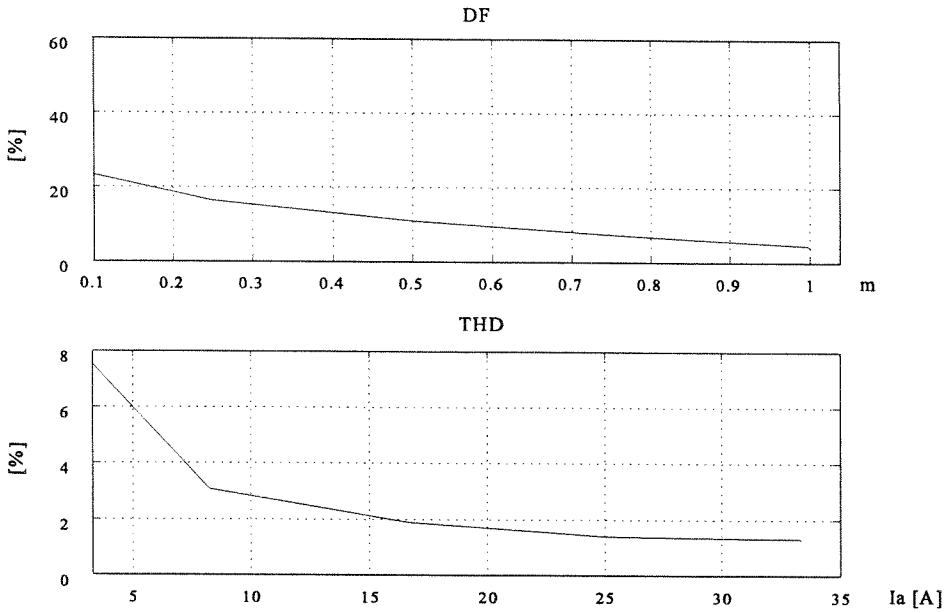


Fig. 6.14 DF and THD index of the ACRDCL converter

I_{eff} phase a	33.75 [A]
$V_{(1)}$ fundamental of v_{ab}, V_d = 620 [V]	629 [V]
V_{lo} peak link voltage amplitude	868 [V]
DF	4.60 [%]
THD	1.32 [%]

Table 6.2 Simulated key numbers from the converter simulation with modulation index m=1.0.

6.3.3 Discussion

The 'Modified ACRDCL for PWM Operation' is a modification of the ACRDCL so that it can perform PWM operation. The modification is done by inserting an extra switch in the active clamp circuit. Compared to the second converter the current stress is lower, but the voltage stress of the converter switches is higher than the voltage stress for ACRDCL resonant converters. There is high dv/dt due to engagement and disengagement of a clamp voltage source.

A general problem of all PWM converters combining a resonant dc link is the time the resonant circuit needs to complete a full resonant cycle. The resonant cycle ensures zero voltage switching at converter branch switch over, but during a resonant cycle no other branch switch over can happen.

6.4 Conclusion

The first converter 'Notch Commutated Three-Phase PWM' /14/ uses a relatively low number of components in the link, one switch and one diode. Unfortunately, the converter has a link switch working with high losses which causes indirect limitations of the switching frequency. Due to this disadvantage is the converter considered unusable in this project.

The second converter 'Zero Switching Loss PWM Converter with Resonant Circuits' /15/ uses

two link switches and two diodes, but it poses a very desirable feature having a zero clamp voltage. This means the voltage stress on converter switches is similar to a hard switched PWM converter. One disadvantage of this converter is the link transistor placed in the main current path which causes high conduction loss. The converter possesses desirable properties, but the link switch in the main current path is considered as such a drawback that the converter is considered unusable in this project.

The third converter 'Modified ACRDCL for PWM Operation' is a modification of the ACRDCL so it can perform PWM operation. The modification is done by inserting an extra switch in the active clamp circuit. Compared to the second converter the current stress is lower, but the voltage stress of the converter switches is higher than the voltage stress for ACRDCL resonant converters. There is high dv/dt due to engagement and disengagement of a clamp voltage source. This undesirable property is also found in the first converter.

A general problem of all PWM converters combining a resonant dc link is the time the resonant circuit needs to complete a full resonant cycle. The resonant cycle ensures zero voltage switching at converter branch switch over, but during a resonant cycle no other branch switch over can happen.

The time used on a converter branch switching could easily take 10 % of the switching period time due to the resonant cycle, and this gives limitations of output voltage amplitude.

7

PWM-VSI converter

This chapter describes a PWM-VSI[1] converter, which is today the most used converter in variable three phase speed drives. The converter technology has been developed for more than two decades and it is considered mature. The design of the converter is described in most power electronic books and the special hardware used to build the converter is available from many manufactures. The two dominating modulation techniques for the VSI are a sinusoidal function with third harmonic injection and stator flux oriented modulation. Both are popular, but they are derived in different ways, the sinusoidal modulation with third harmonic injection is derived by considering how the converter output voltage can be generated as close as possible to a sinusoidal voltage. The first modulation derived in this way was called a sinusoidal modulation, but that modulation had the disadvantage of reduced output voltage. Then it was modified by adding a third harmonic, and by this way the output voltage was boosted, and the voltage gain of the converter is unity. The stator flux orientated modulation is found from direct consideration of optimizing the machine flux pattern, and it has been shown that the stator flux orientated modulation called SFAVM has a superior performance/18/, compared to the sinusoidal modulation with third harmonic injection. The modulation considered here is a stator flux orientated modulation strategy. Considering the implementation of the two different modulation strategy types in a microcontroller there is not much difference. Both modulation strategies are often implemented by using a look-up table which is simple to implement.

The converter is used in applications from a few 100 [VA] to 500 [kVA]. One huge benefit of the PWM-VSI is that the design procedure of the converter of low power compared to higher power is almost the same. The control logic for the low power converter is equal to the high power converter .There has to be taken special considerations of the power electronic layout. The PWM-VSI converter is introduced and then it is simulated using the PWM strategy called SFAVM described in chapter 8.2.1.

7.1 PWM converter

The converter has a relative simple link circuit consisting of a capacitor and it is assumed the capacitor is large enough to ensure a low ripple DC voltage v_{do}. The converter is shown in Fig. 7.1.

[1] Pulse Width Modulated Voltage Source Inverter, PWM-VSI

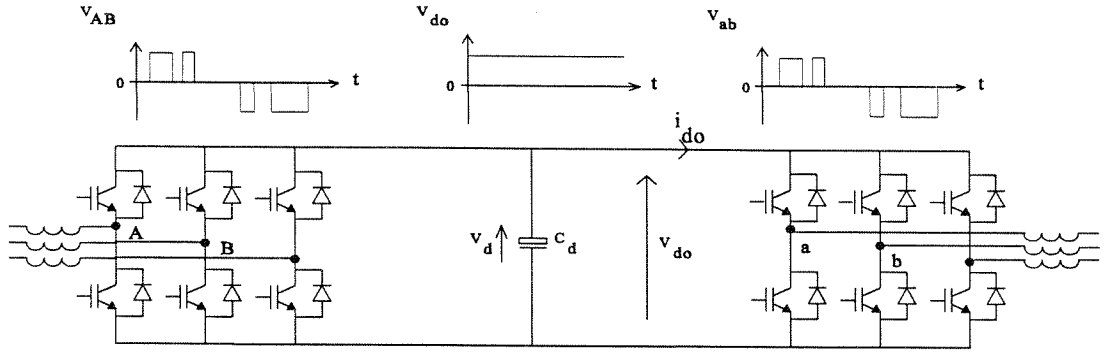


Fig. 7.1 Parallel DC link PWM converter in AC-AC converter

With an ideal converter the maximum voltage stress on the load is only V_d, but the converter switches turn on and off with V_d impressed. This is hard switching and the losses it causes in the non-ideal switches are a limiting factor of the switching frequency. In /10/ there is made an investigation of IGBT's and their behaviour in hard switching. It is concluded that the switching losses can be minimized by selecting a proper switch gate drive and switch technology. This subject is interesting, but in this report the switches are considered ideal whereas the second report in the project deals more with the subject.

7.2 Simulation of PWM-VSI

The DC-AC part of the converter shown in Fig. 7.1 is simulated, and the modulation strategy SFAVM is used. The switching sequence used in the first 0-60 [°] period is

000->100->110->111->111->110->100->000

Further information of the derivation of the SFAVM is found in /18/,/19/ and in chapter 8.2. The load is an RL network and the parameters are shown in table 7.1.

V_d	620 [V]
Load impedance	7.6 [Ω]
cos(ϕ)	0.8
f_{sw}	5.0 [kHz]
Fundamental frequency of current reference f_1	50 [Hz]

Table 7.1 Converter data used in simulation of PWM converter

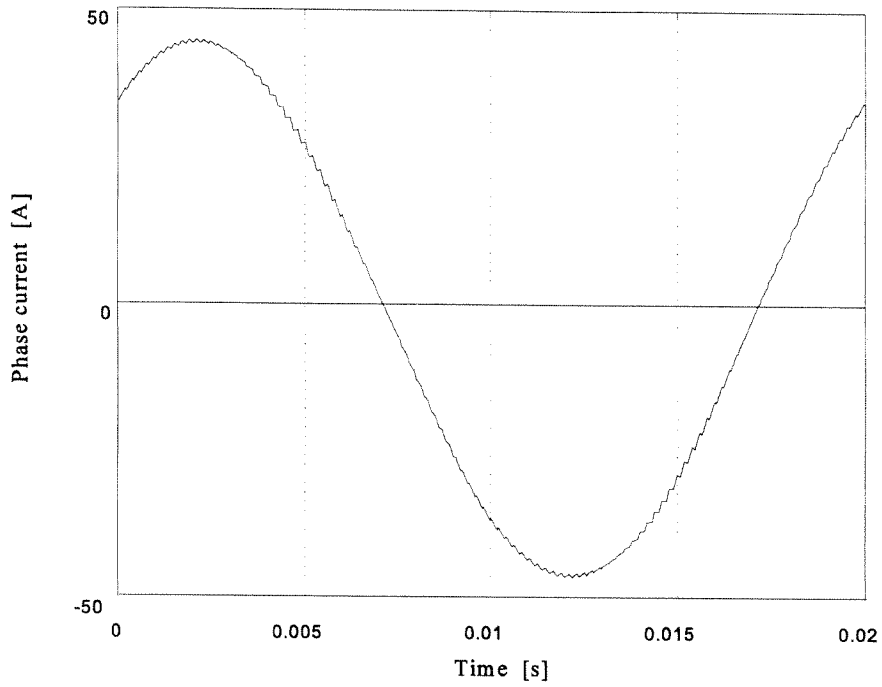


Fig. 7.2 Phase current of PWM converter

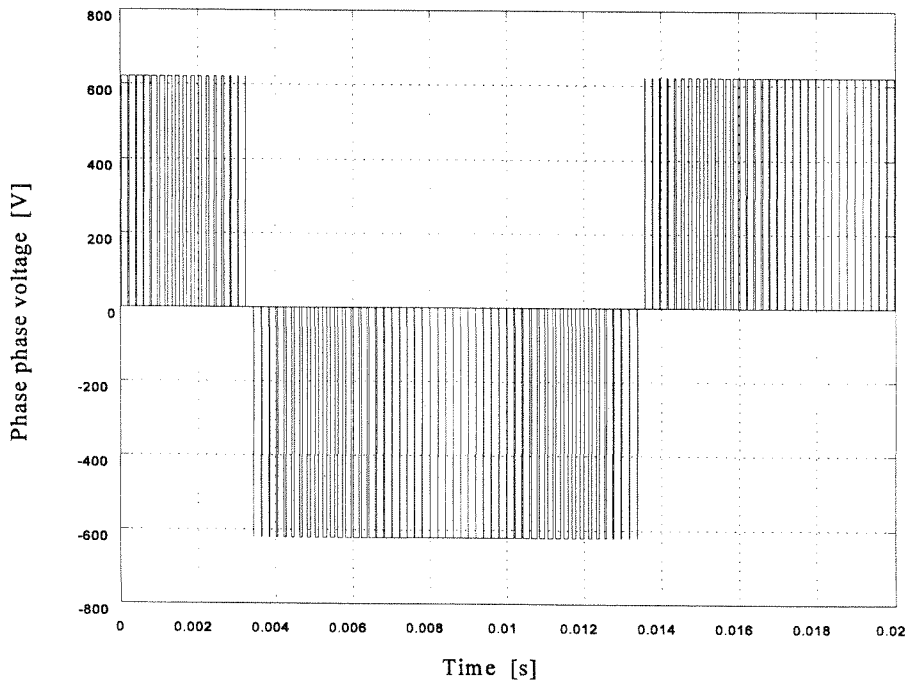


Fig. 7.3 Phase phase voltage of PWM converter

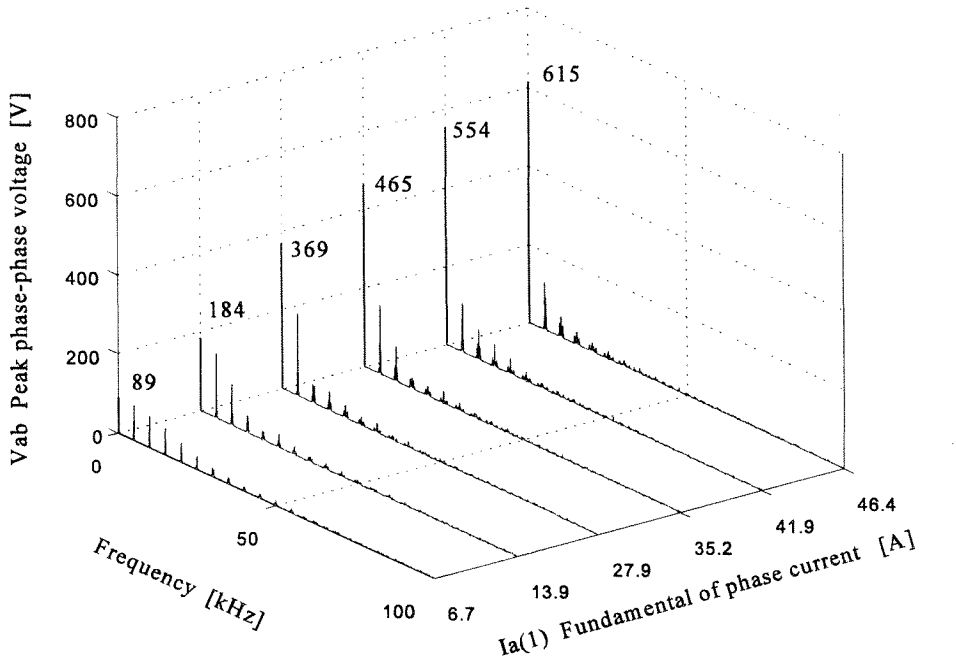


Fig. 7.4 Phase phase voltage amplitude spectrum of the PWM converter

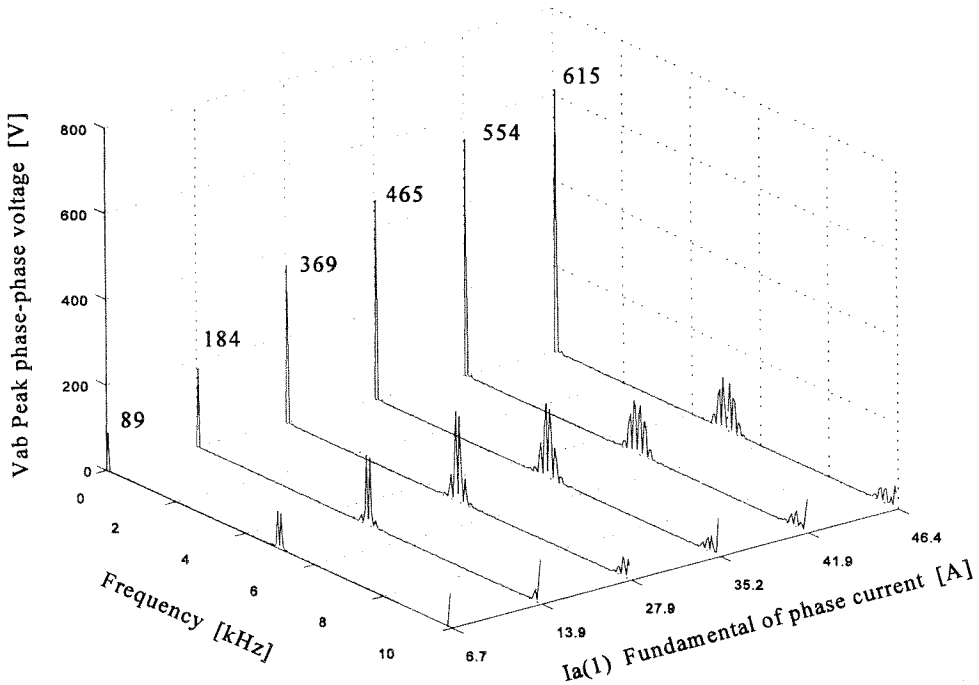


Fig. 7.5 Phase phase voltage amplitude spectrum of PWM converter

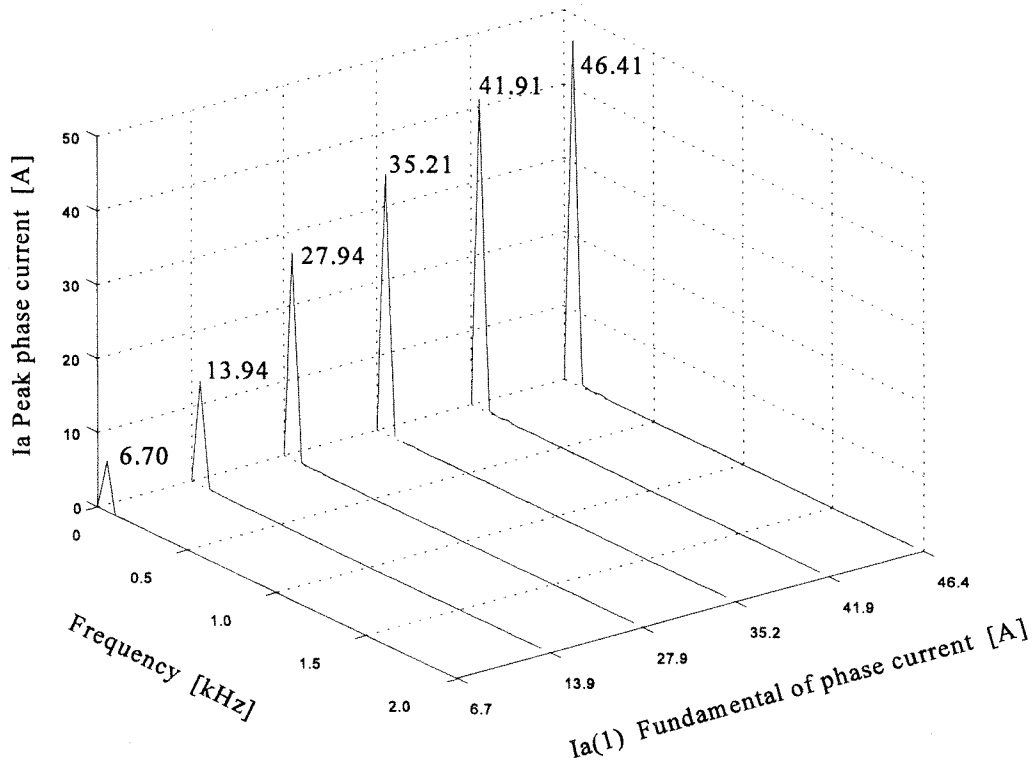


Fig. 7.6 Peak phase current spectrum of PWM converter

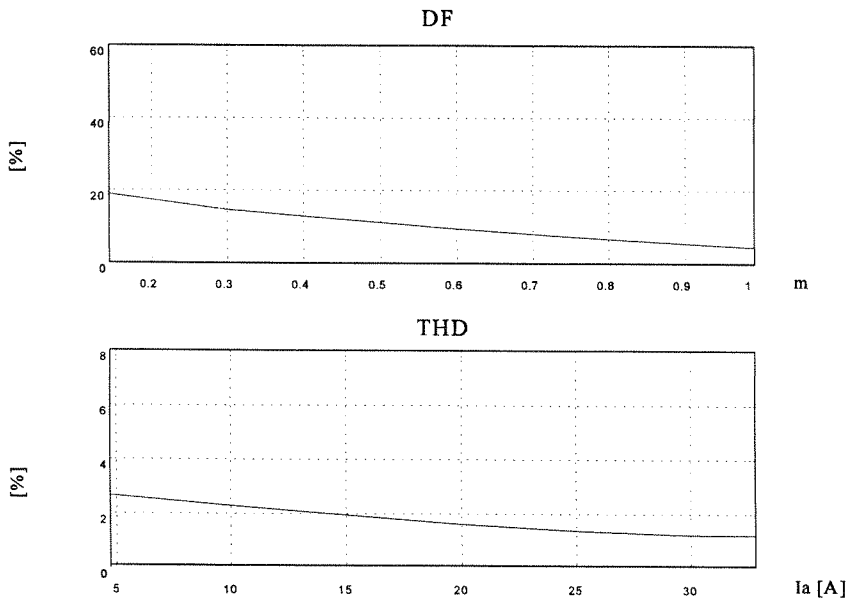


Fig. 7.7 DF and THD index of the PWM converter as function of modulation index m and the effective phase current.

I_{eff} phase a	41.8 [A]
$V_{(1)}$ fundamental of v_{ab}, V_d = 620 [V]	615 [V]
DF	4.57 [%]
THD	1.21 [%]

Table 7.2 Simulated key numbers from the converter simulation with modulation index m=1.0.

The fundamental of v_{ab} is for modulation index m= 1 not equal to V_d but it is 5 [V] below. This is due to the conduction voltage of the switches and diodes. The conduction voltage drop is given by the internal resistance in the diode and switch and on-state voltage used in the simulation. The modulation indexes in the simulations are m= 0.1, 0.3, 0.6, 0.75, 0.9, 1.0.

7.3 Conclusion

The PWM converter is simulated with a switching frequency of 5 [kHz], and the SFAVM strategy is used. The voltage frequency spectrum of the converter shows that the harmonic content is concentrated in narrow bands around multiple of the switching frequency. The spectrum is deterministic opposite the delta modulated converters which have a random spectrum. Using a PWM strategy in machine drives gives a distinct noise with a frequency equal to the switching frequency. With the energy concentrated at multiple of the switching frequency it is advisable to avoid hitting mechanical resonant points. Another factor to be considered where humans are present, is noise. It is often considered unpleasant. For the convince of the user the switching frequency should be high enough to be in an area where the human ear is not so sensitive.

8

Converter modulation strategies

In this chapter different modulation strategies are described, first the DPM[1] and then the PWM[2] strategy. Four different DPM strategies are described briefly and one is selected to be used in the simulation of the converters. The PWM strategy used in the hard switched converter which is simulated in chapter 7 is described. The PWM strategy is modified to be used in the zero voltage switching converter described in chapter 6.

8.1 Delta modulation

This paragraph contains a description of commonly used DPM strategies, and one of them is selected to be used in the simulation of the RDCL, RDCLVPC, and ACRDCL converter.

When using DPM the resonant converter switch is synchronized with the resonant link. The switching of the converter switches should happen at discrete instants in synchronization with the link voltage zero interval. The most wide spread modulators are described in /23/,/34/, and /37/.

8.1.1 Delta current modulator

The Delta current modulator is a single phase modulator with zero hysteresis comparator. Because of the zero hysteresis comparator the modulator does not generate zero voltage vectors /37/. Then the active vectors are changed. There is more than one BSO[3]. Therefore, the phase-phase voltage changes polarity relatively often compared to PWM. PWM usually only allows one BSO between two succeeding active vectors. The resonant link current changes polarity often, therefore the link stress is relatively high.

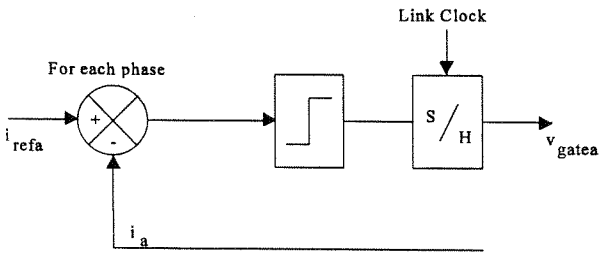


Fig. 8.1 Delta current modulator

[1] Discrete Pulse Modulation

[2] Pulse Width Modulation

[3] Branch Switch Over, BSO

8.1.2 Adjacent state current modulator

The adjacent state current modulator is a modification of the delta current modulator. The adjacent state modulator allows only the converter to generate succeeding active vectors which are adjacent vectors.

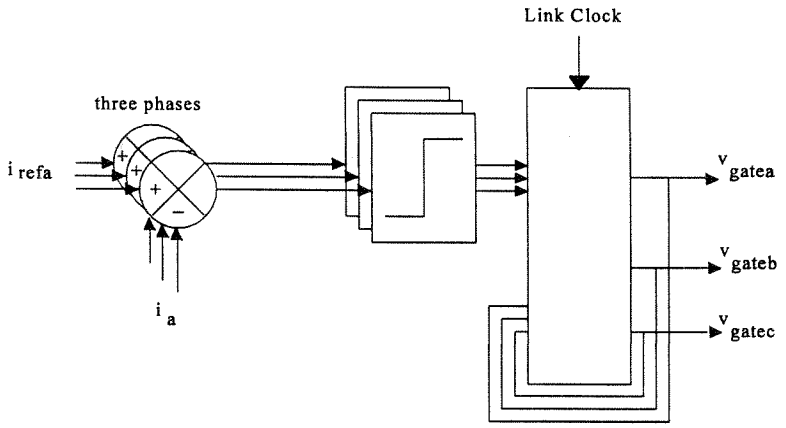


Fig. 8.2 Adjacent state current modulator

The vector sequence 100->110->010 is allowed, but the vector sequence 100->010 is not allowed. If the succeeding vector to an active results in more than one BSO, a zero voltage vector is selected. The zero voltage vector which is closest to the proceeding vector is selected/34/. In this way the switch stress is distributed more equally.

The use of zero voltage vectors limits the link stress considerably because the link current reversals are eliminated. In /34/ it is claimed that the current performance is much better than the delta current modulator. In /23/ a more moderate judgement of the current performance is stated. At low current /23/ the ASCM[4] performance claims to be worse than the DCM[5].

8.1.3 Sigma delta modulator

Sigma delta modulators are more simple to realize than the DCM and ASCM because it only needs a voltage reference and no feed back current from the load. The sigma delta modulator has a low dynamic performance compared to the DCM and ASCM, but it has superior THD performance /34/. SDM[6] is a good choice for open loop control of induction machines /34/.

[4]Adjacent State Current Modulator, ASCM

[5]Delta Current Modulator, DCM

[6]Sigma Delta Modulator, SDM

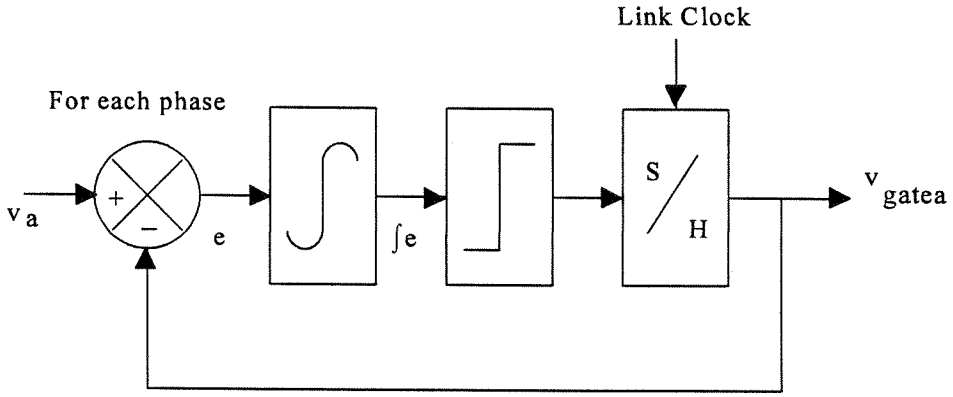


Fig. 8.3 Sigma delta modulator

8.1.4 Selection of modulation strategy

The modulators described here could be extended to more advanced modulators, like the synchronous reference frame versions/34/, but this is not done here because the main purpose is to realize a resonant converter, and a close study of modulation stragies is a huge project. For further study in this report a converter with high dynamical performance is wanted and the link current stress should be low. Therefore, the adjacent state current modulator is chosen to be used in the simulations of the resonant converters.

8.2 Pulse width modulation

This chapter describes a PWM strategy called SFAVM[7] which is used in the hard switched converter simulated in chapter 7. The SFAVM strategy is described in detail which is done because the strategy is modified also to be used in the zero voltage switching converterter MACRDCL simulated in chapter 6.

The modification of the SFAVM strategy for the MACRDCL is done to optimize the ratio of link frequency zero periods versus converter switching frequency and the chosen strategy is called LOSFAVM[8].

8.2.1 Stator flux oriented asynchronous vector modulation

Introduction to voltage vectors and flux polygons:

The converter output voltage is transformed by Park transformation, from the three-phase system to the stator fixed ab-system /21/.

$$\mathbf{V}_s = \frac{2}{3}(v(t)_a + v(t)_b e^{j2\pi/3} + v(t)_c e^{j4\pi/3}) \qquad (8.1)$$

[7] Stator Flux Oriented Asynchronous Vector Modulation, SFAVM

[8] Link Optimized Stator Flux orientated Asynchronous Vector Modulation, LOSFAVM

The voltage vector is the stator voltage vector, and time functions v_a, v_b, v_c are the branch potentials of the converter. It can be shown that branch potentials and phase voltages have identical voltage vectors, the vector $\mathbf{V}_s$ hence is a stator phase voltage vector. The constant 2/3 adjusts the length of $\mathbf{V}_s$ so it has the amplitude of the fundamental phase voltages.

The converter branch potentials are determined by the branch switch positions and with three branches there are 8 different branch potentials each given by a particular state of the converter switches. The branch potential with reference to the midpoint of DC link voltage can be equal to the half link voltage ($V_d/2$) or minus half the link voltage ($-V_d/2$). A convenient representation is described by a one bit operator. '1' means the branch potentials are $V_d/2$, and '0' means $-V_d/2$. Three branches are represented by a tree bit number.

Nr.	v_a	v_b	v_c	$\underline{V}_s$	bits
0	$\frac{v_d}{2}$	$\frac{v_d}{2}$	$\frac{v_d}{2}$	0	111
1	$\frac{v_d}{2}$	$-\frac{v_d}{2}$	$-\frac{v_d}{2}$	$\frac{2}{3}v_d$	100
2	$\frac{v_d}{2}$	$\frac{v_d}{2}$	$-\frac{v_d}{2}$	$\frac{2}{3}v_d e^{j\pi/3}$	110
3	$-\frac{v_d}{2}$	$\frac{v_d}{2}$	$-\frac{v_d}{2}$	$\frac{2}{3}v_d e^{j2\pi/3}$	010
4	$-\frac{v_d}{2}$	$\frac{v_d}{2}$	$\frac{v_d}{2}$	$\frac{2}{3}v_d e^{j\pi}$	011
5	$-\frac{v_d}{2}$	$-\frac{v_d}{2}$	$\frac{v_d}{2}$	$\frac{2}{3}v_d e^{j4\pi/3}$	001
6	$\frac{v_d}{2}$	$-\frac{v_d}{2}$	$\frac{v_d}{2}$	$\frac{2}{3}v_d e^{j5\pi/3}$	101
7	$-\frac{v_d}{2}$	$-\frac{v_d}{2}$	$-\frac{v_d}{2}$	0	000

Table 8.1 Connection between the eight different branch potentials and voltage vectors.

The voltage vectors are impressed on an induction machine having a smooth air gab. In /21/ there is a set of differential equations for the machine. The stator flux can be found by integration.

$$\mathbf{V}_s = R_s\mathbf{I}_s + \frac{d\Psi_s}{dt} \qquad \textbf{(8.2)}$$

For convenience the stator resistance R_s is neglected, and the stator flux is

$$\Psi_s = \int \mathbf{V}_s dt \qquad \textbf{(8.3)}$$

Impressing the 8 voltage vectors in an appropriate way a stator flux trajectory is built up, and

in steady state the trajectory describes a polygon that deviates a little from a circle circumference. Two of the 8 voltage vectors are the zero vectors '111' and '000' and they do not change the flux. The other six called active vectors change the flux.

Stator Flux Oriented Asynchronous Vector Modulation, SFAVM

In /19/ general demands of vector based modulation strategy are formulated . In steady state the stator flux vectors must describe a flux polygon, centered around origo in the ab-plane, while the angle deviation to the reference circle flux must be kept with in an acceptable level by impressing active and zero voltage vectors in changing order.' Further on in /19/ there are suggested 4 different vector sequences that could be used in a modulation strategy. The vector sequences do not use more than one branch switch over, then the next vector is impressed. One example is

000->100->110->111

The reasons for allowing only one BSO between the voltage vectors are

1: Using two BSO's between a zero and an active vector increases the switching losses.

2: If there are two BSO's between two active vectors, a voltage reversal happens and dc-link current changes polarity causing increased reactive power circulation. This problem is known from DPM. While two BSO's give a 120° turn of the flux trajectory instead of a 60°, this will give an unnecessarily increased amplitude and angle error.

It is shown in /19/ that the flux vector angle error in most cases is minimized if the active vectors are centered in the switching period. This is important if the ratio of switching and fundamental frequency are low. This is seen from Fig 8.4 and equation 8.4.

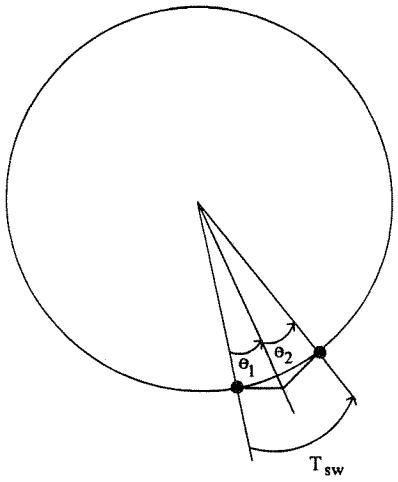


Fig. 8.4.a Unsymetrical flux trajectory

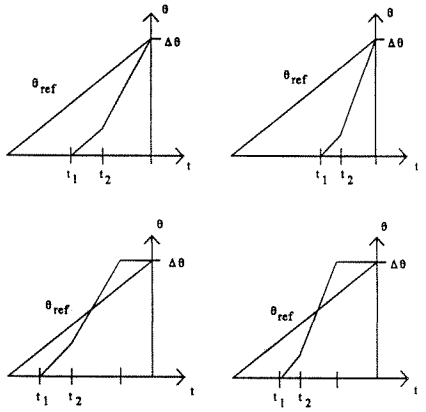


Fig. 8.4.b Angle error at not centered active vectors at top and angle error at centered active vectors at bottom.

Fig 8.4.a shows a flux trajectory and the angles change due to two active vectors, and Fig 8.4.b shows the reference angle and angle from the flux trajectory. The two top figures show the angel error at non- centered active vectors in the switching period. The two bottom figures show the angle error for centered active vectors in the switching period. In equation 8.4 the angle change for a switching period is shown, and it is seen that a high ratio of f1/fsw must minimize the angle error shown in fig. 8.4.b.

$$\Delta\theta = 2\pi\frac{f_1}{f_{sw}} \qquad (8.4)$$

Equation 8.4 shows the angle change for a switching period, and it is seen that a high ratio of f1/fsw must minimize the angle error shown in fig. 8.4.b.

From Table 8.1. the active vector sequences are found as shown in Table 8.2, and the pulse pattern is shown in fig 8.5.

0 - 60°	100 -> 110
60-120°	010 -> 110
120-240°	010 -> 011
240-300°	001 -> 011
300-360°	001 -> 101
360- 0°	100 -> 101

Table 8.2 Active vector sequences used in PWM modulation stragegy.

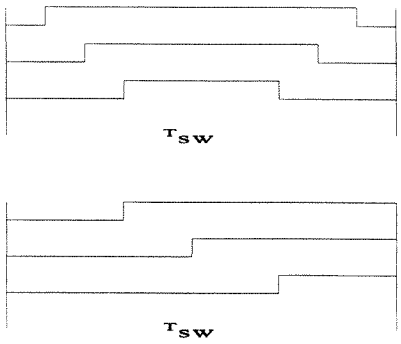


Fig 8.5 The top pulse pattern consist of an vector sequence and an reversed vector sequence and the bottom only by one vector sequence.

The pulse pattern shown in Fig 8.5 at the top has the advantage to have the same number of BSO's as the bottom pulse pattern, but average flux amplitude error is smaller.

The SFAVM is optimized with respect to the number of flux turns per switching period and a minimized angle error and a low number of BSO's. In /19/ the vector sequence of a switching period of the first 0-60 [°] of a voltage vector V_s using SFAVM is

000 -> 100 -> 110 -> 111

This sequence is found not to be optimum in the MACRDCL converter because then there is needed a high number of link zero voltage intervals. The next paragraph describes the modulation sequence used in the MACRDCL.

8.2.2 Link optimized stator flux oriented asynchronous vector modulation, LOSFAVM

A modulation strategy used in the MACRDCL should have a minimum number of link zero voltage periods. In other words, the link frequency should be minimum for a given converter switching frequency.

The reason to keep the link frequency low is that the resonant link circuit must be activated to make the link voltage to go zero. After the zero voltage interval the link voltage is changed back to the DC link voltage. The whole cycle needed to obtain the zero voltage interval takes time, and this time is a limit of how close two BSO[9]'s can appear. There should be as few BSO's per switching as possible.

For the PWM converter it is desirable to have a low DC link frequency, and the minimum link frequency strategy is called LOSFAVM.

[9] Branch Switch Over, BSO

Selection of modulation strategy

Equation 8.4 shows the angle change for a switching period, and it is seen that a high ratio of f_{sw}/f_1 decreases the angle error. This is used to make the following assumption:
For a high swithcing frequency 10-20 [kHz] with a $f_{1\,MAX}$ = 50 [Hz] is the angle error at non-centered active vectors is considered acceptable, and two BSO's between a zero and active vectors are acceptable.

The active vectors don't have to be centered in the switching period, and the number of BSO's is not critical having zero voltage switching. It is decided to avoid current reversals in the link and there is therefore only allowed one BSO between two active vectors. Changing from a zero vector to an active or opposite it is allowed that there is more than one BSO.

The active vector sequence shown in table 8.2 is used, but the zero vectors must be placed with respect to a minimum number of DC link switchings per switching period.
Table 8.3 shows four vector sequences, number 1-2 is from /18/,/19/.

DLS: Dc Link Switching per switching period, BSO: Branch Switch Over per switching period.

Vector sequence	DLS	BSO	Number of V_{avg} pr. T_{sw}
->000->100->110->111->	4	6	2
->000->100->110->111->111->110->100->000->	6	6	4
->111->100->111->111->110->111->	4	6	2
->000->100->110->	3	4	2

Table 8.3 Vector sequence combinations and there is searched for a minimum number of DLS for a given switching frequency.

In the beginning of chapter 6.3.1 it was stressed that the link frequency must be low. The vector sequence with the lowest DLS has the lowest link frequency and number of BSO's. The selected vector sequence is:

$$\underset{t_0}{000} \rightarrow \underset{t_1}{001} \rightarrow \underset{t_2}{011}$$

By simple geometry /18/,/19/ the time of each active vector is found. t_1, t_2, and t_0 are

$$t_1 = T_{sw}\, m\, (\frac{\sqrt{3}}{2}\cos\theta - \frac{1}{2}\sin\theta) \qquad \textbf{(8.5)}$$

$$t_2 = T_{sw}\, m\, \sin\theta \qquad \textbf{(8.6)}$$

$$t_o = T_{sw} - (t_1 + t_2) \qquad \textbf{(8.7)}$$

Fig. 6.9 shows the modulation curve and branch potential, phase-phase voltage and a fourier spectrum of phase-phase voltage, the dc link voltage is constant.

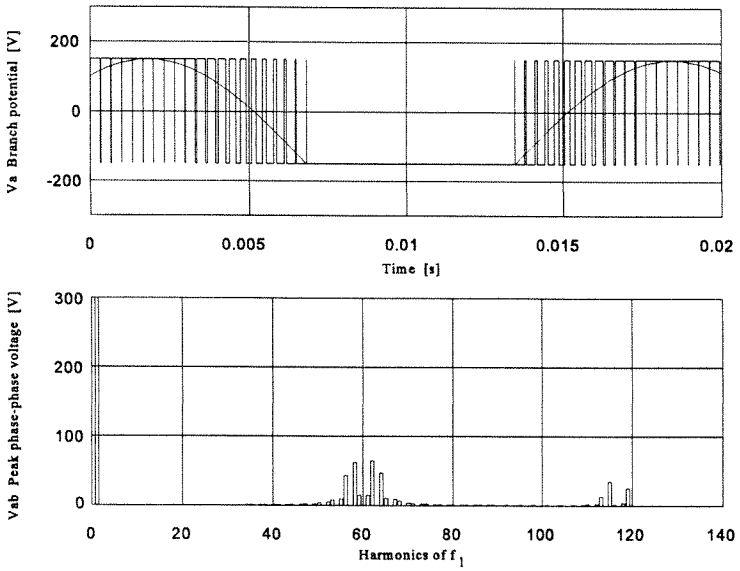


Fig. 6.9 Modulation curve, branch potential and phase-phase voltage fouier spectrum using the LOSFAVM strategy.

The modulation strategy is used in the MACRDCL converter simulated in chapter 6.

8.2.3 PWM used in resonant link converters with oscillating link

Using the delta modulation technic has the disadvantage of variable swithcing frequency, and this makes the PWM spectral performance superior at particular lower modulation indexes. Here a small investigation is made to see if it is realistic to use PWM in resonant link converters with discrete voltage pulses.

If PWM is used in a resonant link converter, the resonant link frequency must be high to obtain satisfactory pulse width resolution, in typical PWM-VSI the pulse width resolution is higher than 128. The pulse width resolution is defined as the ratio.

$$\text{pulse resolution} = \frac{\text{PWM timer frequency}}{\text{converter switch frequency}} \tag{8.8}$$

The pulse width resolution using a resonant converter

$$\text{pulse resolution} = \frac{\text{link frequency}}{\text{converter switch frequency}} \tag{8.9}$$

With a pulse resolution of 128 and a switch frequency of 5 [kHz] the resonant link frequency should be 640 [kHz]. With this resonant link frequency the dv/dt is about 2000 [V/μs] which value is close to the values obtained in hard switched PWM converters, the IGBT switches used in converters have a maximum switching frequency about 100 [kHz].

Generation of PWM patterns using a resonant link needs a resonant link with a very high resonant frequency, and considering that this generates high dv/dt, the subject is not dealt with further.

8.3 Conclusion

The modulation technics most often used in resonant and VSI converters are described. For the resonant converters having discrete switching zero voltage instants a simple delta current modulator is selected which is synchronized with the DC link zero voltage instants. There is selected a PWM strategy called SFAVM for the PWM-VSI converter and for the modified resonant converter where the DC link zero voltage instants can be initiated almost arbitrary. There is seleced a modified SFAVM strategy which minimizes the DC link switchings for a given switching frequency. The strategy is called LOSFAVM. Finally, it is considered if a PWM strategy with benefit could be used in a resonant converter with discrete zero voltage instants, but it is concluded that the DC link resonant frequency has to be very high. And such a high resonant frequency generates dv/dt similar to the standard PWM converter. The switches typically used in medium power converters do not switch fast enough so this possibility is disregarded.

9

Performance and characteristics of converters

The performance and characteristic parameters are divided into three categories: High level properties, describing simple observations. Medium level properties, describing more specific parameters. Low level properties, describing a particular configuration of converters in detail, the properties are found by simulation. Converter topologies investigated are particular for motor drive applications, but with the investigation it should be possible to select a topology for other applications. UPS, and AC power supplies.

Table 1. High Level properties

Converter type	Input converter	Output converter	Link type	Link device count		Input filter	Output filter
				Switches, diodes	Passive compo-nents L,C	Passive compo-nents L,C	Passive com-ponents[*1]
RDCL	Diode or DPM	DPM	voltage res. DC link	0	1L 2C	3L	0
RDCLVPC		DPM	voltage res. DC link	0	1L 2C		
ACRDCL		DPM	voltage res. DC link	1S 1D	1L 2C		
MACRDCL		PWM	DC voltage	2S 2D	1L 1C		
PWM-VSI		PWM	DC voltage	0	1 C		

[*1] Inductive load assumed

Table 2. Medium level properties

Converter type	Switch type	Main switch switching	Average switching frequency [kHz]	Link control complex-ness	Max. output voltage*1	Approx. main switch V stress *2	Approx. main switch I stress *2
RDCL	IGBT, MOS-FET Uni-directional	ZVS	~20	simple	<1	2.8>V>2	1
RDCLVPC		ZVS, Hard	~20	very complex	<1	2.08>V>2	1
ACRDCL		ZVS	~18	complex	<1	1.4 = V	1
MACRDCL		ZVS	5	complex	<1	1.4>V>1	1
Sinusoidal PWM-VSI		Hard	Hard	middle, high	simple	1	11

*1 The base of comparison max. output voltages is six-step operation, $V=1.273*V_d/2$
*2 The base of comparison is the voltage stress in the sinusoidal PWM-VSI

Table 3 Low Level properties

Converter type	Inverter Device	Link device	DF [%]	THD [%]
	Voltage peak switch [V]	Voltage peak clamp switch [V]	m=1	m=1
RDCL	1519	-	4.28	0.54
RDCLVPC	1289	-	4.17	0.54
ACRDCL	850	148	4.50	0.70
MACRDCL	850	148	4.60	1.32
PWM-VSI	620	-	4.57	1.21

Fig 9.1. shows the distortion factor, DF /39/ and the total harmonic distortion,THD /8/ for the converters

$$DF = \frac{100}{V_{(1)}}\sqrt{\sum_{n=3}^{\infty}\left(\frac{V^2_{(n)}}{n}\right)}$$

$$THD = \frac{100}{I_{(1)}}\sqrt{\sum_{n=2}^{\infty} I^2_{(n)}}$$

And the converters are:

A ACRDCL
M MACRDCL
R RDCL
V RDCLVPC
P PWM-VSI

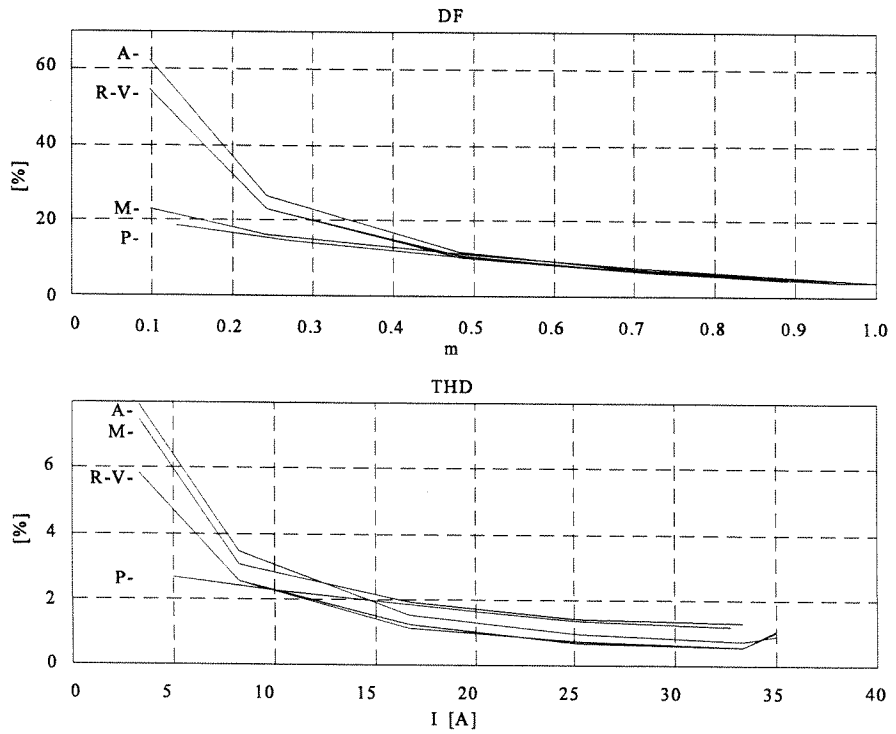


Fig. 9.1 Spectral performance of simulated converters. Note that $m = V_{(1)ab}/V_{d,}$ and I is the effective value of the fundamental phase current.

10

Conclusion

In this chapter a revision of the initial problem leading to this report is made. Then there is made an evaluation of four selected resonant converters. The evaluation is based on the analysis and simulation of the converters. Finally, there is selected one resonant converter for further work.

10.1 Revision of the initial problem

In this report is dealt with analysis and simulation of resonant converters, used in three-phase speed drive systems. The motivation for the work is the problems with switching losses, and high dv/dt, generated by the standard converter PWM-VSI used today. Today the switching frequency of the medium power standard converter is limited below 20 [kHz]. This is due to the increase of switching losses and dv/dt at higher switching frequencies. By using resonant converters the problems can theoretically be solved, and switching frequencies higher than 20 [kHz] are easily obtained. But the resonant converter increases voltage and current stress of the converter components and load machine. Several resonant converters are investigated to find a resonant converter that is able to compete with the standard converter used today.

10.2 Evaluation

There are suggested many resonant converters and all cannot be evaluated in the period of the project. From a study of the paper literature is it decided to investigate the parallel DC link converters further. There are selected four parallel DC link converters to be subjected to a deeper analysis and simulation.

The four selected converters are named RDCL, RDCLVPC, ACRDCL, and MACRDCL and from the analysis and the simulation results there is selected a converter for implementation in laboratory. To be able to compare the resonant converters' performance with the widely used PWM-VSI. That converter is also simulated.

The evaluation of the converters RDCL, RDCLVPC, ACRDCL, and MACRDCL is first done by comparing the converters to the specification given in chapter 3. The desired specifications for a resonant converter are repeated:

- Phase-Phase voltage, V = 440 [V] RMS for link voltage, V_d = 620 [V]
- Phase-Phase peak output voltage maximum 1300 [V]
- Dv/dt < 1300 [V/μs] , a dv/dt = 200 [V/μs] is desirable
- Resonant link frequency, f_{res} in the area of 40 - 150 [kHz]
- Distortion of inverter output voltage, DF similar to a PWM-VSI converter working at 5 [kHz] for a resonant link frequency of 50 [kHz]

Converter	Max. Phase-Phase voltage,RMS m=1 [V]	Peak Phase-Phase voltage [V]	dv/dt [V/µs]	f_{res} [kHz]	DF similar to PWM-VSI
RDCL	438	1519	> 200	54	yes
RDCLVPC	438	1289	~ 200	54	yes
ACRDCL	438	850	> 200	54	yes
MACRDCL	438	850	> 500	100	yes

Table 10.1. Converter performance of four investigated converters

The RDCL converter is seen to have the highest peak phase-phase output voltage. The peak phase-phase output voltage amplitude is a serious disadvantage, the output voltage is high, and the peak voltage is heavily load dependent. The only way to decrease the peak phase-phase voltage is to decrease the impedance of the resonant link circuit, but this gives higher reactive losses. It cannot be expected that standard induction machines, as the ones described in chapter 3.1, can withstand this high voltage without insulation breakdown. The amplitude of the peak phase-phase voltage disqualifies the RDCL converter form further investigation.

The RDCLVPC converter has also the problem of high peak phase-phase output voltage, but compared to the RDCL the voltage is much lower and it is not load-dependent. The peak phase-phase output voltage amplitude is not higher than standard 1700 [V] IGBT can be used, and the voltage is within the specification limits of 1300 [V].

It has the lowest number of additional power electronic components of all the resonant converters, and because the peak link voltage amplitude is relatively constant and not clamped, the dv/dt would be close to 200 [V/µs] for a link circuit resonant frequency of 54 [kHz], except for the hard switched turnoffs at relatively low voltage. The other converters could under load change operation states have dv/dt somewhat higher, like 500 [V/µs]. Compared to the other resonant converters there is no additional components in the link than the resonant circuit.

The control of the link voltage amplitude is done by the converter switches, and it is possible to control the resonant circuit energy by turning the converter switches on a little time before the zero voltage condition. Turning the converter switches on a little time before the zero voltage condition gives hard switching and high dv/dt. The design of the problem of the RDCLVPC is to minimize the link voltage at the instant the converter switches are turned off.

Despite the simplicity of the power electronic circuit one must consider that the control of the RDCLVPC converter is quite complex and requires very fast control electronics.

The ACRDCL converter introduces a switch in the DC link circuit to clamp the output voltage. The link switch is working at relatively low voltage, but is working at the link frequency and therefore believed to have high losses. This is described in /35/. Comparing the output voltage quality with the other converters it is seen that the converter is performing worse. This is due to the fact that the link frequency is dependent on the clamp level. A low clamp level gives a lower link frequency and to increase the voltage quality the resonant link component frequency must be increased. Resonant frequency can be increased by decreasing L or C. If L is decreased, this decreases the resonant impedance and the peak current increases. If C is decreased, the resonant impedance increases, but the inverter switches are going to be more stressed. The total loss is

therefore properly rising when the resonant frequency in the ACRDCL converter increases, but a final judgement is impossible to make without knowledge of which type of switches is used and the data for the resonant components. The converter has a lower output voltage peak compared to the RDCLVPC but at the expense of a switch. The control of the converter is considered not as complicated as the RDCLVPC. The ACRDCL converter control is simpler because the control of the link switch can be done quite independent on the inverter switching state.

The MACRDCL converter combines PWM and zero voltage switching and does this by a link circuit using two switches. It is shown that the output voltage quality is quite similar to the one the standard PWM-VSI converter produces. This means the voltage quality at lower modulation index is better than the other resonant converters described. It must, however, be noted that the modulation is limited by the time it takes to initiate the resonant link circuit and make the resonant cycle. The way to have a wide modulation area is to have a high resonant circuit frequency.

MACRDCL is the converter that uses most additional components in the resonant link. It uses two switches and diodes more than the RDCL and the RDCLVPC converter do. On the other hand it offer the best modulation quality because it uses PWM.

10.3 Selection of converter for further work

The three converters to be considered selected for further work are the RDCLVPC, ACRDCL, and MACRDCL. It is concluded they all are within the specification limits and it is decided to make a choice based on two qualities:

High efficiency
High output voltage quality

It is considered that the RDCLVPC has the potential of the highest converter efficiency, due to the minimum number of power electronics components used, and it is shown the modulation quality at high modulation indexes must be considered good. The MACRDCL converter is considered to offer the potential of highest output voltage quality, at a broad modulation index range because it uses a PWM strategy. The ACRDCL is between these two converters' performance, and it is decided not to consider that converter further. The choice is between the MACRDCL and the RDCLVPC. It is believed that the RDCLVPC is complicated to control, but due to the quite advanced custom designed chip available today, it is hoped that the control can be implemented in such a chip. The converter power circuit would then be quite simple, almost as simple as the PWM-VSI converter, and therefore and due to the expected high efficiency the RDCLVPC is selected for further study and implementation in laboratory.

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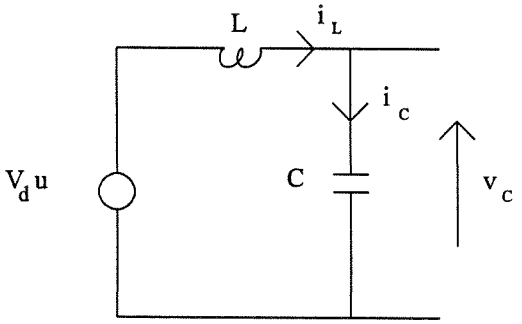
App. A

Basic serial resonant circuit

In this appendix the time domain equations of the series resonant circuit are derived. The circuits are assumed ideal.



$$V_d u - v_L - v_C = 0 \tag{A.1}$$

$$V_d u - L\frac{d_{iL}}{dt} - \frac{1}{C}\int_0^t i_C dt - v_C(0\_) = 0 \tag{A.2}$$

takes the Laplace transformation and then takes the inverse Laplace transformation

$$i_L = i_{L_0}(0\_)\cos\omega t + \frac{1}{Z}V_d - v_C(0\_))\sin\omega t \tag{A.3}$$

and using

$$v_C = V_d - v_L \tag{A.4}$$

$$v_L = L \frac{d_{iL}}{dt} \tag{A.5}$$

is found

$$v_C = V_d - (V_d - v_C(0\text{-})) \cos \omega t + Z\, i_L(0\_) \sin \omega t \tag{A.6}$$

where $Z = \sqrt{\frac{L}{C}}$

and $\omega = \frac{1}{\sqrt{LC}}$

App. B

Selection of resonant link components

The resonant link component values are selected and they are used in the simulated converters the RDCL, RDCLVPC, ACRDCL, and the MACRDCL The three first converters use the same resonant link values for the purpose of comparison, but the MACRDCL cannot function properly with a switching frequency of 5 [kHz] and use the same resonant component values. There are selected particular resonant component values for the MACRDCL converter.

In chapter 3 specification for the resonant converters were found. The specifications used in the selection of converter L_{res} and C_{res} components are repeated in Table B.1.

Link voltage amplitude max.	1300 [V]
Resonant link frequency	50 [kHz]

Table B.1 Desired specification for a resonant converter

The selection of the resonant link component L_{res} is based on an experience rule given in /35/, the criteria are low current ripple, low resonant circuit loss, and low switching loss. Guidelines are that the resonant inductor current should increase to about one quarter to one third of the maximum output current, during a shortening interval. During the shortening interval the resonant inductor energy increases. The purpose is to compensate energy loss in the real world components. If the loss in the real components is higher than the energy stored in the inductor during the shortening interval, the link voltage of the next resonant cycles does not reach zero voltage.

The DC link voltage is Vd= 620 [V], the shortening interval is ts=2 [μ], the link output current is set to i_p=60 [A], form /35/

$$L_{res} = \frac{3V_d \cdot t_s}{i_p}$$

and with f_{res} = 50 [kHz]

$$f_{res} = \frac{1}{2\pi} \frac{1}{\sqrt{L_{res} C_{res}}}$$

the following values are found:

L_{res} = 60 [μH]	C_{res} = 150 [nF]	Z_{res} = 20 [Ω]	f_{res} = 53.1 [Ω]

The chosen value of Z_{res} is seen to give substantial higher link voltage than the desired 1300 [V] specified in Table B.1. The Z_{res} could be changed to a lower value and limit the link voltage amplitude, but as seen from fig 4.7 the link impedance should be very low.

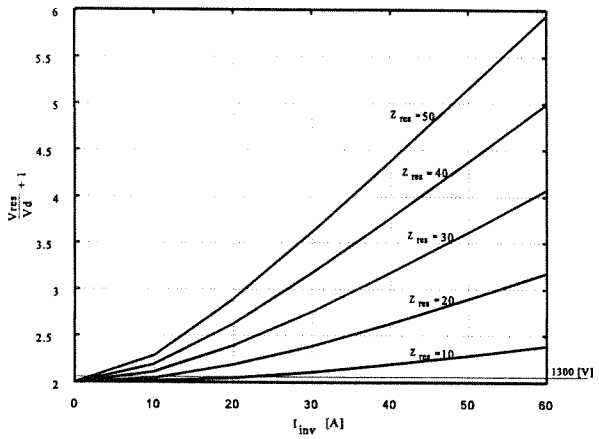


Fig B.1 Link voltage amplitude as function of different values of Z_{res} and load change currents (I_{inv}).

The resonant link components influence the current ripple, a large Z_{res} decreases the resonant inductor current, but the resonant link voltage amplitude increases. If Z_{res} is made smaller, the current ripple increases and the loss increases. Fig B.1 shows the link voltage amplitude as function of different values of Z_{res} and load change currents (I_{inv}). The curves are calculated from $V_d = 620$ [V] and $V_{res}^2 = V_d^2 + (Z_{res} I_{inv})^2$.

A Z_{res} which limits the DC link peak voltage below the 1300 [V] introduces high resonant currents. The value of Z_{res} could not be chosen to give acceptable amplitudes of link current and voltages for the RDCL converter. But for the RDCLVPC and the ACRDCL converters the Z_{res} value is realistic. For the sake of a performance comparison of the three converters the resonant circuit values are kept equal.

The fourth converter MACRDCL cannot work properly with the selected resonant component values. The converter is pulse width modulated, and therefore the link has two modes, a resonant mode and a non-resonant mode with constant DC link voltage. The resonant mode is initiated shortly before the inverter is changing switching state and the DC link voltage oscillates down to zero voltage. In this way the switching takes place under a zero voltage condition, but due to the resonant cycle there is a limitation on the switching of inverter switches. The inverter switches cannot be switched during the resonant cycle and this limits the modulation range of the converter. In order to make the limitation on the modulation index small, the resonant circuit frequency must be high. The MACRDCL resonant circuit components are selected to be:

$L_{res} = 60$ [μH]	$C_{res} = 150$ [nF]	$Z_{res} = 20$ [Ω]	$f_{res} = 53.1$ [Ω]

App. C

Derivation of voltage peak control algorithm used in the RDCLVPC converter

In this appendix the derivation of the voltage peak control strategy is done. The idea is to impress current changes on the resonant converter link in such a way that the voltage above the resonant capacitor does not exceed two times the DC link voltage.

The resonant circuit shown in Fig. C.1 is an equivalent circuit of the RDCLVPC converter.

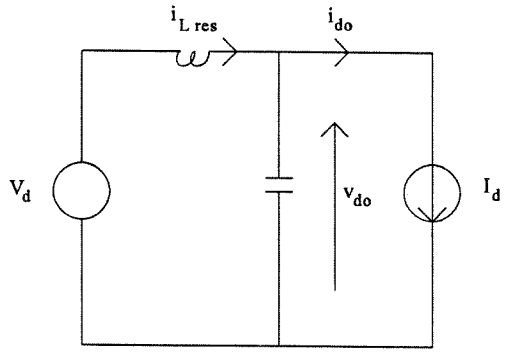


Fig. C.1 Equivalent circuit of the RDCLVPC converter.

V_d is the DC link voltage source and the ideal current source I_d is an equivalent of the inverter bridge and the load. i_{do} is assumed constant over time.

The resonant circuit components are assumed ideal, and in this way the equation for the serial resonant circuit found in Appendix A can be used here.

The VPC strategy is derived from the plot of the resonant inductor current versus the resonant capacitor voltage.

Fig. C.2 shows the resonant circuit phase plane plot when the current i_{do} is impressed on the resonant circuit and the current changes happen when the link voltage v_{do} is zero.

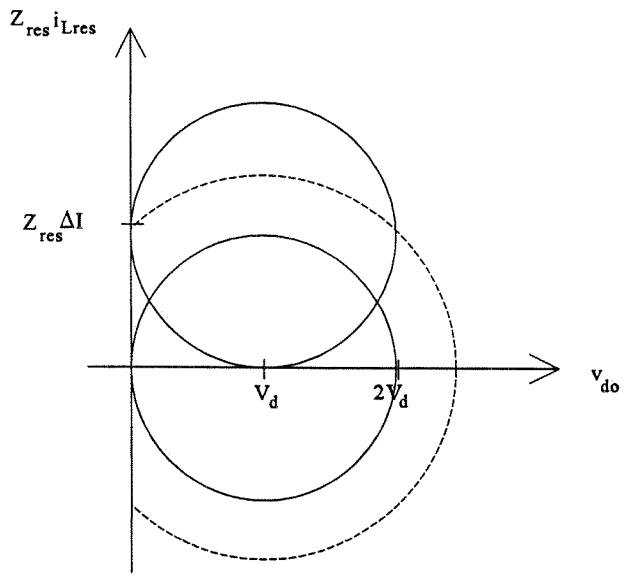


Fig. C.2 Phase plane plot of the resonant link circuit current $Z_{res}I_{Lres}$ and voltage v_{do}, when the current i_{do} is impressed on the resonant circuit.

The dotted line in Fig. C.2 shows the overvoltage due to an undesired increase of the resonant capacitor energy. This overvoltage can be eliminated by impressing the negative current change ΔI on the resonant circuit when the two full line circles collide. The circles collide at a low voltage and high voltage, the current change must be impressed at the low v_{do} voltage. By impressing the load current change a little time before the zero voltage condition ($v_{do} = 0$) it is possible to maintain a constant resonant peak voltage at twice the DC link voltage (V_d). The relationship between the time instant the negative current change ΔI should be impressed and the magnitude of ΔI is found in the following equations. The equations for the two full line circles are

$$(v_{do}, Z_{res} i_{Lres}) = V_r(1 - \cos\alpha) + j V_r \sin\alpha \qquad (C.1)$$

$$(v_{do}', Z_{res} i_{Lres}') = V_r'(1 - \cos\alpha') + j(Z_{res} \Delta I + V_r' \sin\alpha') \qquad (C.2)$$

putting $V_r = V_r'$ and $\alpha = -\alpha'$ is found considering the imaginary port of (C.1) and (C.2).

$$\sin\alpha = \frac{Z_{res} \Delta I}{V_r} + \sin\alpha'$$

$$\sin\alpha = \frac{Z_{res} \Delta I}{V_r 2}$$

and V_r is desired to be V_d and $\alpha = \omega_{res}$.

$$t_{off} = \frac{1}{\omega_{res}} a\sin\left(\frac{Z_{res} \Delta I}{V_d 2}\right) \qquad (C.3)$$

With (C.3) it is possible to calculate at which time (t_{off}) the negative current change ΔI should be impressed on the resonant circuit in order not to cause an overvoltage.

App. D

ACRDCL converter link frequency dependency on clamp factor

In this appendices is the link frequency and the average value of the link voltage calculated as function of the clamp factor and the resonant circuit components L_{res} and C_{res}. In the calculation are assumed:

- zero voltage time duration is zero
- ideal components
- no load change condition ($i_{do} = 0$)

The link waveform v_{do} of the ACRDCL is drawn in Fig. D.1.

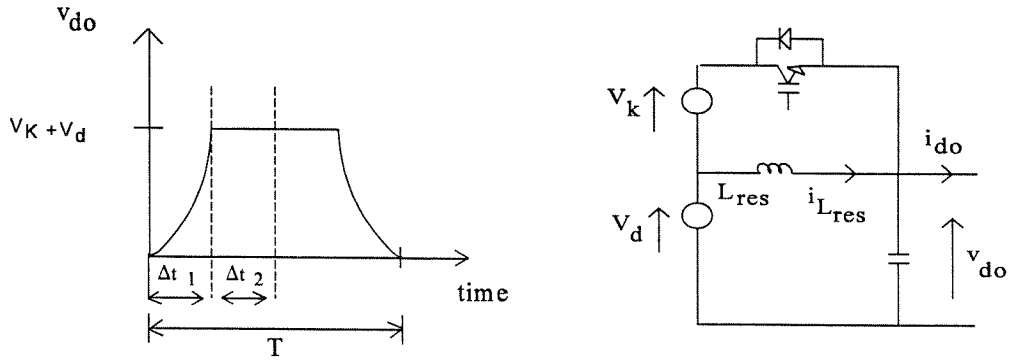


Fig. D.1 Link voltage v_{do} and the link circuit of the ACRDCL converter.

The average value of the link voltage v_{do} is

$$V_{do} = \frac{2}{T} \int_{0}^{T/2} v_{do}\, dt \qquad \textbf{(D.1)}$$

The integral is dived into two sections.

$$V_{do} = \frac{2}{T}\int_{0}^{\Delta t_1} v_{do}\,dt + \frac{2}{T}\int_{\Delta t_1}^{T/2} v_{do}\,dt \qquad \textbf{(D.2)}$$

where

$$V_{do} = \begin{cases} V_d(1 - \cos\omega_{res} t) & 0 \le t \le \Delta t_1 \\ V_d + V_K & \Delta t_1 < t \le T/2 \end{cases} \qquad \textbf{(D.3)}$$

and

$$\omega_{res} = \frac{1}{\sqrt{L_{res}\, C_{res}}} \qquad \textbf{(D.4)}$$

and

$$\frac{T}{2} = \Delta t_1 + \Delta t_2 \qquad \textbf{(D.5)}$$

D.1 Calculation of Δt_1

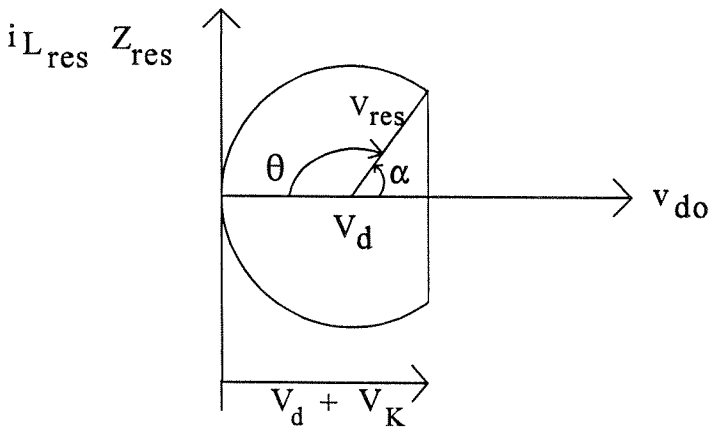


Fig. D.2 Phase plane plot of $i_{Lres}Z_{res}$ versus v_{do}.

From the phase plane plot shown in Fig. D.2 is a equation of Δt_1 found

$$\omega_{res}\,\Delta t_1 = \theta \qquad \textbf{(D.6)}$$

$$\omega_{res}\,\Delta t_1 = \pi - \alpha \qquad \textbf{(D.7)}$$

$$\omega_{res}\,\Delta t_1 = \pi - \sin^{-1}\left(\frac{\sqrt{V_{res}^2 - V_k^2}}{V_{res}}\right) \qquad \textbf{(D.8)}$$

$$\Delta t_1 = \frac{\pi - \sin^{-1}\left(\frac{\sqrt{V_{res}^2 - V_K^2}}{V_{res}}\right)}{\omega_{res}} \tag{D.9}$$

D.2 Calculation of Δt_2

From Fig. D.1 is found

$$\Delta t_2 = \frac{L_{res}}{V_K}\Delta I \tag{D.10}$$

and from Fig. D.2 is found

$$\Delta I = \frac{\sqrt{V_{res}^2 - V_K^2}}{Z_{res}} \tag{D.11}$$

$$Z_{res} = \sqrt{\frac{L_{res}}{C_{res}}} \tag{D.12}$$

and Δt_2 is

$$\Delta t_2 = \frac{\sqrt{V_{res}^2 - V_K^2}}{V_K\,\omega_{res}} \tag{D.13}$$

Using D.2, D.3, D.9 and D.13 a expression of the average link value V_{do} is found. Is assumed that $V_{res} = V_d$ is V_{do} in D.14 found to be V_d. The average link voltage V_{do} is indpendent of the clamp level and the resonant circuit values.

$$V_{do} = \frac{2}{T}V_d\left[\Delta t_1 - \frac{\sin\omega_{res}\Delta t_1}{\omega_{res}} + \left(\frac{T}{2} - \Delta t_1\right)\left(1 + \frac{V_K}{V_d}\right)\right] \tag{D.14}$$

$$V_{do} = V_d \tag{D.15}$$

The resonant link voltage v_{do} period T is

$$T = \frac{2}{\omega_{res}}\left[\pi - \sin^{-1}\left(\frac{\sqrt{V_d^2 - V_K^2}}{V_d}\right) + \frac{\sqrt{V_d^2 - V_K^2}}{V_K}\right] \tag{D.16}$$

App. E

Definition of performance index DF and THD

Definition of distortion factor, DF /39/ and the total harmonic distortion,THD /8/ used to evaluate the converter output voltage.

$$DF = \frac{100}{V_{(1)}}\sqrt{\sum_{n=2}^{\infty}\left(\frac{V^2_{(n)}}{n}\right)}$$

$$THD = \frac{100}{I_{(1)}}\sqrt{\sum_{n=2}^{\infty} I^2_{(n)}}$$

App. F

Single phase Equivalent circuit of three-phase converter

In this appendix a simple equivalent circuit of the three-phase converter bridge is found. The equivalent circuit is used in the analyzation of the resonant link converter. The converter switches and diode are assumed ideal.

The symbol of the ideal switch is an IGBT symbol. Fig. F.1 shows the converter from which an equivalent circuit is found.

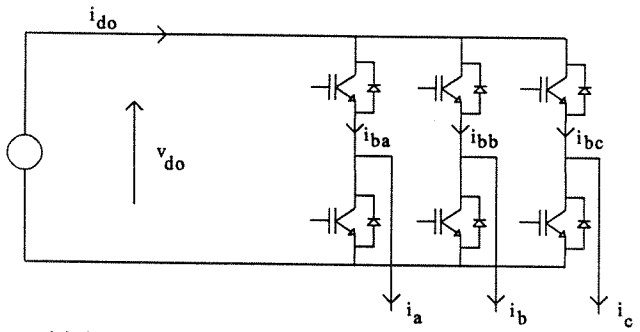


Fig F.1 Converter from which the equivalent is found.

The link current i_{do} is

$$i_{do} = i_{ba} + i_{bb} + i_{bc} \qquad \textbf{(F.1)}$$

i_{do} is determined by the current i_{ba}, i_{bb} , and i_{bc} that is controlled by the converter switch states. There are eight states of the output switches, and they are conveniently expressed by a switch vector $\underline{V}_{SW}$. In the converter branches only one switch conducts a time. If an upper switch conducts, it is symbolized by the number 1. If a lower switch conducts, the number is 0. A switch vector sequence could be $\underline{V}_{SW}$=100.

There are three branches and the switch vector $\underline{V}_{SW}$ has three elements. The link current is described as a function of $\underline{V}_{SW}$ and i_{ba}, i_{bb}, i_{bc} in eq. F.2. In eq. F.3 the converter voltage vector is described as a function of $\underline{V}_{SW}$ and v_{do}

$$i_{d0} = \underline{V}_{sw} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{F.2}$$

$$\underline{V}_s = \frac{2}{3} \begin{bmatrix} 1 \\ a \\ a^2 \end{bmatrix} \left(\underline{V}_{sw} - \frac{1}{2} \right) v_{do} \tag{F.3}$$

.

Using a resonant link circuit it is necessary to shorten the link. The short circuit happens if the converter antiparallel diodes or switches conduct. It is assumed that all the diodes or switches are turned on/off at the same time. The shortening state introduces a state number nine $\underline{V}_8$. In state $\underline{V}_8$ is v_{do} zero. Table F.1 shows the 9 states.

$\underline{V}_s$	$\underline{V}_{sw}$	i_d
$\underline{V}_0$	000	0
$\underline{V}_1$	100	i_a
$\underline{V}_2$	110	$i_a + i_b$
$\underline{V}_3$	010	i_b
$\underline{V}_4$	011	$i_b + i_c$
$\underline{V}_5$	001	i_c
$\underline{V}_6$	101	$i_a + i_c$
$\underline{V}_7$	111	0
$\underline{V}_8$	xxx	0

In Table F.1 i_{d0} is found from 1 and 2.

The link current i_d is modeled by one current source, in state $\underline{V}_8$ the short circuit is modeled by a switch and a diode. The equivalent of the converter showed Fig. F.1 seen from the link side and the equivalent circuit of the converter seen from the three-phase side is shown in Fig. F.2.

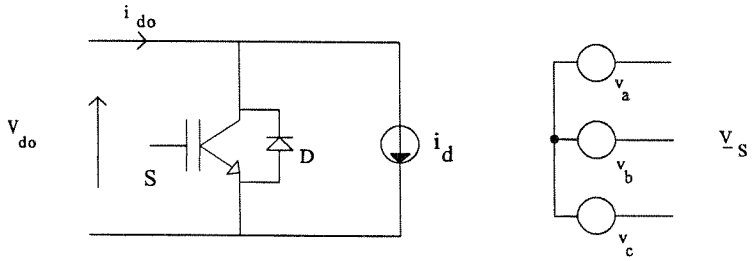


Fig. F.2 Link side equivalent circuit and AC side equivalent circuit of a three-phase converter

English summary

This is the first of two reports in the Ph.D thesis. Today the 'de facto' standard of converters, used in three-phase electrical speed drives, is the pulse width modulated voltage source inverter. The converter has a stiff DC link voltage, and using the pulse width modulation control of the inverter switches is it possible to obtain an output voltage with low harmonic content. The inverter switches are turned-on and turned-off at DC link voltage level, and this generates switching losses and high dv/dt. Both are undesirable. Another type of converter called resonant converters is using a resonant link where the link voltage and the current are oscillating, and in this way it is possible to turn the inverter switches on and off at zero voltage or zero current. By using a resonant converter it is possible to reduce the switching losses and to lower the dv/dt considerably and in this way to operate the inverter switches at higher frequencies and at increased output voltage quality. Many resonant converters have been proposed, but here the detailed description is limited to four resonant converters, and they are analyzed and simulated. One of the converters is selected for realization as the next step in the Ph.D. thesis. In order to compare the resonant converters with the pulse width modulated voltage source converter the converter is also simulated.

The first converter is the RDCL converter that is the most simple parallel resonant converter. Its resonant link consists only by the resonant LC circuit. Using this converter there are problems with high DC link voltage peaks which must be limited.

The second converter is the RDCLVPC which uses a control of the DC link voltage peak that has not seen being described in any earlier paper. The converter controls the DC voltage peak by turning the inverter switches off a little before the zero voltage condition, and in this way it is possible to control the DC link voltage peak. The converter link is identical to the RDCL converter and by introducing hard switching of the inverter switches the link voltage peak can be controlled.

The third converter is the ACRDCL converter. The DC voltage peak is controlled by a clamp circuit, and this circuit limits the link voltage peak below what is obtainable with the RDCLVPC converter. The clamp circuit consists of a capacitor, a diode, and a switch. The converter is modulated by a discrete pulse modulation strategy. This strategy is used because the DC link voltage hits the zero voltage condition at an almost constant frequency, and the inverter switches must be switched at the zero voltage instant. A pulse width modulation scheme is not realistic to use for a converter with a constant frequency oscillating DC link voltage, and this is unfortunate because the pulse width modulation performance is better than the discrete pulse modulation when lower modulation indexes are used.

The fourth converter solves the problem of applying PWM to a resonant converter by only initiating a resonant cycle when an inverter switch changes state. To initiate a resonant cycle that ensures zero voltage switching takes a short time. During this time no other inverter switches can change state and this limits the modulation range. By using a high resonant frequency the modulation range can be made quite wide.

The fourth converter is called MACRDCL. The DC link voltage peak is similar to the third converter and it is shown by simulation. The output voltage quality is quite similar to the standard pulse width modulated voltage source inverter.

There is made a detailed evaluation of the four converters, and the RDCLVPC converter is chosen for further work. The converter is going to be realized in the laboratory.

Danish summary

Dette er et referat af den første af to rapporter som udgør Ph.D projeketet. Standard 'Pulse Width Modulation-Voltage Source Inverter' PWM-VSI vekselrettere brugt i trefasede frekvensomformere har en, ideelt set, konstant DC mellemkredsspænding. Vekselretter-transistorerne arbejder ved fuld DC mellemkredsspænding, hvilket medfører switchtab og høj dv/dt. Switchtab og høj dv/dt er uønskede. Inden for de sidste 10 år har der været stor forskningsaktivitet omkring resonanskonvertere, med hvilke switchtabet og dv/dt kan reduceres kraftigt.

Mange forskellige resonanskredsløb er blevet foreslået. En analyse af dem alle, inden for projekttidsrammen, er ikke realistisk. Der foretages en udvælgelse af parallelresonanskonverterne til yderligere analyse baseret på et artikelstudium. For grundigere analyse og simulation vælges fire konvertere ud, herefter evalueres de på baggrund af et sæt specifikationer, og en konverter udvælges til realisering.

Den første konverter er RDCL konverteren, som er den simpleste parallelresonanskonverter. Komponentantallet i mellemkredsen forøges kun med resonanskredsen, realativt til PWM-VSI vekselretteren. Konverteren genererer høje udgangsspændingspeaks, og det er nødvendigt at begrænse dem for ikke at skade invertertransistorerne og den tilkoblede elektriske maskine.

Den anden konverter er RDCLVPC konverteren, og den kontrollerer mellemkreds-peakspændingen. Det sker ved at slukke vekselrettertransistorerne et lille øjeblik, før mellemkredsspændingen bliver nul volt. Mellemkredsen er identisk med RDCL konverterens mellemkreds, og konverteren er på denne måde meget simpel.

Den tredje konverter er ACRDCL konverteren. Mellemkredsspændingspeakene er kontrolleret med et hjælpekredsløb, og det begrænser peakene til en lavere værdi, end det er opnåeligt med RDCLVPC konverteren. Hjælpekredsløbet består af en kondensator, diode og transistor.

ACRDCL og de to forrige konvertere er moduleret med diskret pulsmodulation. Diskret pulsmodulation er anvendt som følge af, at mellemkredsspændingen oscillerer med næsten konstant frekvens, og invertertransistorerne skal switche i nul-volts perioden. Denne form for modulationsstrategi genererer lidt dårligere udgangsspændingskvalitet end PWM ved lave moduleringsindex. Det er derfor ønskeligt at have en PWM resonanskonverter. Den fjerde konverter løser dette problem ved kun at initiere en mellemkredsresonanscyklus, når en vekselrettertransistor ændrer status. På denne måde skal vekselrettertransistorerne ikke tænde og slukke på diskrete tidspunkter, og der kan anvendes PWM. Den fjerde konverter kaldes MACRDCL. Mellemkredspeakspændingsniveauet er det samme som for ACRDCL konverteren, og udgangsspændings kvaliteten er tæt på at være lig med udgangsspændingskvaliteten fra PWM-VSI vekselretteren.

Der laves en detaljeret analyse af de fire konvertere, og de simuleres. Der vælges at arbejde videre med RDCLVPC konverteren, som realiseres i laboratoriet. Realiseringen beskrives i RKEE projekt rapport nr. 2.