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Original Citation

Sibley, Martin J.N., Unwin, Rodney T., Smith, D., Boxall, B.A. and Hawkins, R.J. (1985) A monolithic common-collector front-end optical preamplifier. Journal of Lightwave Technology, 3 (1). pp. 13-15. ISSN 0733-8724

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A Monolithic Common-Collector Front-End Optical Preamplifier

MARTIN J. N. SIBLEY, RODNEY T. UNWIN, DAVID R. SMITH, BRUCE A. BOXALL, AND RICHARD J. HAWKINS

Abstract—**A monolithic transimpedance preamplifier has been developed having a common-collector cascode configuration with shunt feedback, using an advanced bipolar IC process. The measured sensitivity was −35.0 dBm at 140 Mbit/s for an error rate of 10^{-9} and a p-i-n photodiode responsivity of 0.5 A/W.**

IN BIPOLAR optical preamplifiers it is common practice to employ a common-emitter front end or, where Miller capacitance is to be eliminated, a cascode input [1]. These configurations do, however, have a disadvantage in that the preamplifier −3-dB bandwidth depends on the base–emitter capacitance of the front-end transistor ($C_{\pi 1}$). In addition, the base-spreading resistance (r'_{bb_1}) can significantly affect the preamplifier transfer function, and may even result in a two-pole frequency response if r'_{bb_1} is high enough [1]. Both of these disadvantages are overcome, together with the elimination of Miller capacitance, if a common-collector front end is employed. A previous paper [2] has demonstrated the usefulness of this type of preamplifier input in obtaining a receiver with a wide-band response. A common-collector common-emitter feedback design was constructed in discrete component form and was found to be suitable for 140-Mbit/s operation.

This paper describes a directly coupled preamplifier based on a common-collector, cascode design which is also suitable for a 140-Mbit/s receiver. The complete receiver is shown in Fig. 1 and the components shown within the dotted box have been fabricated in monolithic IC form at BTRL. This design, unlike the earlier one [2], has a single-pole response which would also enable the receiver to operate at bit rates in excess of 140 Mbit/s by employing simple equalization techniques.

The design was fabricated in monolithic IC form in order to produce a low-cost optical receiver for high-speed data bus systems, and for optical local-area networks. The monolithic IC preamplifier has given reduced stray capacitances, resulting in an improved frequency response. In addition, the circuit has been fabricated using a proven bipolar IC process to give a high reliability compared to conventional p.c.b. or hybrid designs.

The cascode stage (T_2 and T_3) is biased by an emitter follower (T_4) fed from the diode chain T_5, T_6, and T_7. The emitter currents in this part of the circuit are designed to be

Manuscript received March 12, 1984; revised April 24, 1984.

M. J. N. Sibley and R. T. Unwin are with the Department of Electrical and Electronic Engineering, The Polytechnic, Huddersfield, HD1 3DH, England.

D. R. Smith, B. A. Boxall, and R. J. Hawkins are with British Telecom Research Laboratories, Martlesham Heath, Ipswich, Suffolk, England.

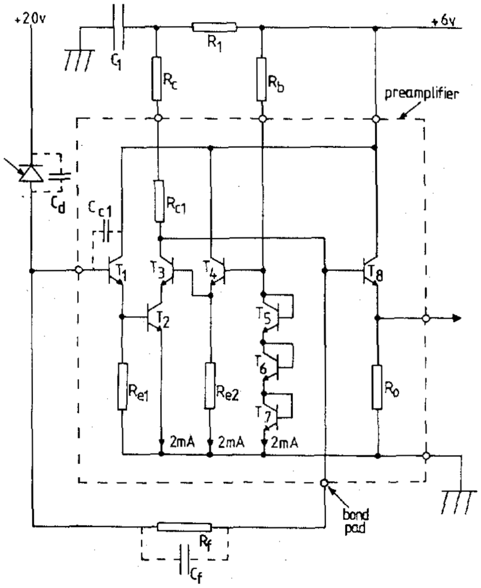

Fig. 1. Optical receiver.

2 mA to ensure identical V_{be} values. The voltage gain of the cascode may be externally adjusted by varying R_C. Resistor R_1 ensures that the cascode bias current (and hence the second-stage open-loop voltage gain) is close to the design value regardless of the exact V_{be} values of the transistors.

The closed-loop pole due to the cascode stage is sufficiently high (220 MHz) so as not to affect the preamplifier −3-dB bandwidth. Thus the closed-loop bandwidth is governed by a single open-loop time constant given by (1)

$$\tau_{in} = (R_{in} \| R_f)\, C_{in} \qquad (1)$$

where

R_{in} open-loop input resistance of the receiver,
$= r'_{bb_1} + r_{\pi 1} + h_{fe1}\,(R_{e1} \,\|\, (r'_{bb_2} + r_{\pi 2}))$,
r_π element in the hybrid-π transistor model,
C_{in} $= C_d + C_s + C_{c1} + C_f$,
C_s bond pad to substrate capacitance.

We also define A_1 and A_2 as the first- and second-stage open-loop mid-frequency voltage gains, respectively, and A_0 as the closed-loop mid-frequency voltage gain between T_1 base and T_3 collector. The closed-loop transimpedance $Z_c(s)$ between these nodes is given by (2), where A_0 can be taken to equal

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TABLE I
DESIGN PARAMETERS

T_1					
I_{c_1}	= 0.64 mA	R_{e_1}	= 1.2 kΩ	R_{e_2}	= 800 Ω
h_{fe_1}	= 185	R_{c_1}	= 88 Ω	R_b	= 1.8 kΩ
$r_{bb'_1}$	= 415 Ω	R_c	= 220 Ω	R_o	= 250 Ω
f_{T_1}	= 2 GHz	R_1	= 1.9 kΩ	R_f	= 9.4 kΩ
C_{c_1}	= 0.15 pF	C_d	= 0.8 pF	C_1	= 100 nF
C_s	= 0.3 pF	C_f	= 0.1 pF		
A_1	= 0.96	A_2	= 21.07	A_o	= 20.16

$A_1 A_2$

$$Z_c(s) = \frac{-A_0 R_{\text{eff}}}{1 + sR_{\text{eff}}(C_d + C_s + C_{c1} + (1 + A_0)C_f)} \tag{2}$$

where $R_{\text{eff}} = R_{\text{in}} || (R_f/(1 + A_0))$.

By using the design details given in Table I the preamplifier -3-dB bandwidth is calculated from (2) to be 107 MHz. As a comparison, the closed-loop transimpedance for an equivalent cascode input design, having a single pole response, is given by

$$Z_c(s) = \frac{-A_0 R_{\text{eff}}}{1 + sR_{\text{eff}}(C_d + C_s + C_{c1} + C_{\pi 1} + (1 + A_0)C_f)}. \tag{3}$$

In general, $C_{\pi 1}$ has the effect of reducing the -3-dB bandwidth considerably.

At optimum bias, the S/N ratio at the output of the predetection filter is at a maximum (3). In this design, T_1 has a base current of 3.4 μA as opposed to an optimum value of 2.5 μA. This only incurs a small noise penalty particularly as the thermal noise from R_f is dominant in determining the receiver sensitivity.

The emitter length of T_2 is twice that of T_1 and this results in a relatively low base spreading resistance of 153 Ω. This value of r'_{bb}, together with the second stage shot noise, degrades the sensitivity by 0.3 dB. This degradation could be reduced by optimizing the IC process for lower values of r'_{bb}.

The advanced bipolar process uses a double diffused structure with a 0.15-μm basewidth. The small feature sizes (3-μm emitter, 2-μm base contacts, 1.5-μm recut emitter contacts, and 2.4-μm-wide titanium–gold metallization) were all defined by electron-beam lithography [4]. Care was taken in routing the metallization tracks within the IC in order to minimize the capacitance to ground at the input node. The IC was mounted in an 18-pin chip carrier, and the complete receiver constructed on PCB using chip resistors and an HP 5082-4205 Si p-i-n diode having a responsivity of 0.5 A/W.

The p-i-n was irradiated by an 850-nm GaAlAs laser and the bandwidth calculated from rise-time measurements was 100 MHz. The optical dynamic range was measured to be 20 dB.

Fig. 2 compares the computer predicted and measured transimpedance versus frequency responses, and also shown are the spectral densities of the input equivalent noise current ($S_{eq}(\omega)$). The measured frequency response was obtained by irradiating the p-i-n with an unmodulated high-intensity edge-emitting GaAlAs LED (such that the p-i-n diode shot noise was far in excess of the preamplifier noise). Under this condition, the output of the preamplifier, as measured using a spectrum analyzer, corresponds to the transimpedance versus frequency response. As can be seen from Fig. 2 the bandwidth obtained by this method correlates well with the bandwidth found from the rise-time measurement. The input equivalent noise current spectral density was found by dividing the measured output noise voltage by the measured transimpedance.

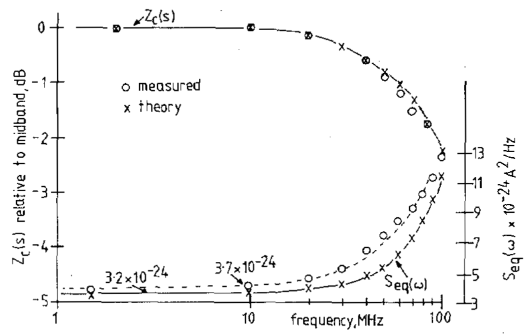

Fig. 2. Transimpedance and input equivalent noise current spectral density as a function of frequency.

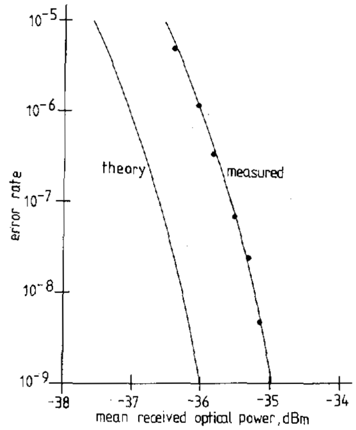

Fig. 3. Measured and predicted error rate as a function of mean received optical power for a data rate of 140 Mbit/s.

Fig. 3 compares the predicted and measured error-rate performance. The predicted curve was obtained by applying Personick's theory [5] to the measured noise characteristic in Fig. 2, assuming an ideal raised cosine predetection filter.

In conclusion, we have demonstrated a monolithic IC preamplifier based on a common-collector cascode configuration. The receiver has a single-pole frequency response making subsequent equalization and operation beyond 140 Mbit/s possible. The receiver has an optical dynamic range of 20 dB and a measured sensitivity of -35.0 dBm at 140 Mbit/s.

ACKNOWLEDGMENT

The authors wish to thank the UK SERC for the CASE award studentship at The Polytechnic, Huddersfield. We also wish to thank the Director of Research, BTRL, for permission to publish this paper, and members of the R2 VLSI Technology Division for circuit fabrication.

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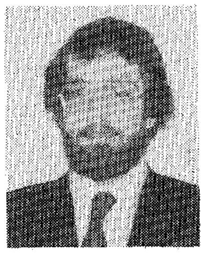

Martin J. N. Sibley was born in Hertfordshire England, in 1959. In 1981 he received the B.Sc.(Hons) degree in electrical and electronic engineering from The Polytechnic, Huddersfield. He is currently undertaking research into the design of high-speed optical receivers, in the same Department, for the degree of Ph.D.

Mr. Sibley holds a U.K. SERC CASE studentship with the collaborating body being BTRL.

*

Rodney T. Unwin was born in Derbyshire, England, in 1941. He received the M.Sc. degree in electronics from the University of Southampton, England, and Ph.D., from the University of Salford, Salford, England.

He joined the Post Office Engineering Department (now British Telecoms), Manchester Area, as a trainee in 1958 and left in 1963 to join the C.E.G.B. where he held the post of Assistant Engineer, Technical Services (Telecommunications) in the S.E. Region. In 1972 he joined the Department of Electrical and Electronic Engineering, The Polytechnic, Huddersfield, where he is at present a Principal Lecturer.

David R. Smith was born in England in 1949. He received the B.A. and M.A. degrees in natural sciences from Christ's College, Cambridge University, England in 1971 and 1976, respectively.

In 1971, he joined the British Post Office Research Department (now known as British Telecom Research Laboratories, Martlesham Heath, England) where he has been engaged in research on optical-fiber systems and components. He is presently Head of the Optical Receivers and New Optical Components Group.

Mr. Smith is a member of the Institution of Electrical Engineers.

*

Bruce A. Boxall was born in London, England in 1949. He received the B.Sc. degree in electrical engineering science from the University of Salford, Salford, England, in 1971. Further work on the translational properties of magnetic bubble domains led to a Ph.D. degree from Imperial College, London, England in 1975.

He then joined the British Telecom Research Laboratories, Ipswich, England, where he is now head of the bipolar technology group in the VLSI technology division. During the last three years he has presented a series of lectures at the University of Essex on the fabrication of integrated circuits.

*

Richard J. Hawkins was born in Bristol, England, in 1944. He received the B.Sc. degree in physics from the University of Bristol, Bristol, England, in 1966, and the Ph.D. degree from the University of Southampton, Southampton, England, in 1970 on current noise in field-effect transistors.

After a further period at Southampton as Junior Research Fellow in the Department of Electronics he joined the Microelectronics Division of British Telecom Research Laboratories, Ipswich, England, where he is now head of the bipolar IC design group. He is the author of a number of papers on low and high-frequency noise and the measurement and modeling of high-frequency transistors.