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Hardware-in-the-loop setup for enhanced modular multi-level converter with reduced circulating currents

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ABSTRACT

Owing to its essential features, such as modularity and exceptional power quality, the modular multilevel converter (MMC) emerges as the optimal converter topology for high-voltage direct current (HVDC) applications. Traditionally, MMCs are controlled through a method called nearest level modulation (NLM), which generates N+1 AC output voltages, where N represents the number of sub modules (SMs) per arm. In this paper, we introduce a modified NLM technique designed to yield 2N+1 and 4N+1 levels, with a focus on efficiently controlling internal dynamics. The proposed MMC is evaluated using a hardware-in-the-loop (HIL) environment to obtain real-time simulation outcomes. This MMC topology demonstrates a reduction in circulating currents and capacitor voltage ripple.

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1. INTRODUCTION

Modular multilevel converter (MMC) is a promising and dominant topology for high-voltage direct current (HVDC) applications. Among all other high-power voltage source converters, MMC is preferred for HVDC applications due to its modularity and fault-blocking capability features [1]. The MMC also offers several other notable benefits, such as reduced DV/DT stress, lower total harmonic distortions (THD) in output waveforms without the need for filters, and improved efficiency [2]. Essentially, MMC is composed of cells or sub modules (SMs) like unipolar cells (half-bridge), symmetrical bipolar cells (full-bridge), and asymmetrical bipolar cells (hybrid cells) [3]. The half-bridge-based MMC is the most commonly used topology because of its simpler structure, fewer switches, superior efficiency, and reduced cost [4].

The literature suggests various pulse width modulation (PWM) techniques for controlling MMC, such as sinusoidal pulse width modulation (SPWM), space vector PWM, selective harmonic elimination (SHE), and nearest level modulation (NLM) [5]. NLM is preferred among all PWM techniques due to its salient features, such as operating at the fundamental switching frequency (reducing switching losses) and being easy to implement for a higher number of SMs [6], [7]. Furthermore, it offers attractive advantages, such as a natural voltage balancing algorithm and not involving complicated mathematical calculations as in the case of SHE. The conventional NLM method is shown in Figure 1, while (1) and (2) can be used to calculate the number of SMs to be inserted in the upper and lower arms. The sinusoidal reference waveforms are converted to staircase waveforms using the round function, and then, by employing the sorting algorithm, the SMs are inserted and bypassed accordingly.

$$N_U = round_{0.5} \frac{V_{dc}}{2V_d}(1 + m\cos(wt)) \quad (1)$$

$$N_U = round_{0.5}\frac{V_{dc}}{2V_d}(1 - m\cos(wt) \quad (2)$$

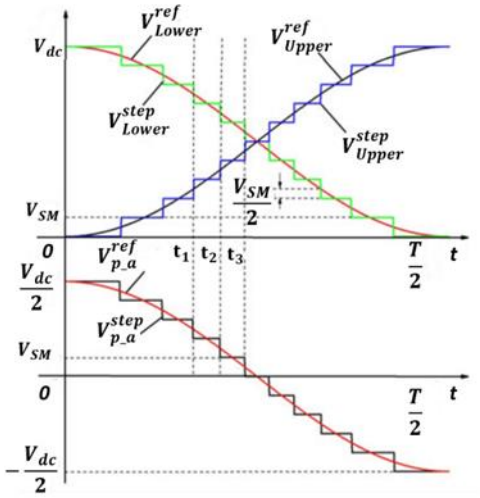


Figure 1. Conventional NLM method for MMC

2. COMPARISON WITH PREVIOUS RESEARCH

In the conventional NLM-based MMC, the output waveform consists of N+1 levels, where N represents the number of SMs inserted in the upper and lower arms [2]. As a result, the conventional NLM requires a higher number of SMs to increase the number of levels in the output waveform. This leads to an increased number of power switches and passive components (inductors and capacitors) as well as more complex gate drive circuitry. Consequently, the overall complexity and footprint of the MMC station increase.

A review of the literature indicates a need for the development of an enhanced MMC with a reduced number of cells, lower harmonic content, decreased circulating currents and minimized capacitor voltage ripple. Alexander and Thathan [8] suggested binary, ternary, and modified MMC configurations to achieve better power quality and reduced circuit complexity. However, the proposed research work suffers from increased THD and involves complex mathematical calculations. In research works [9], improved NLM with fewer SMs has been proposed. Nonetheless, the research lacks experimental verification, and the THD is higher compared to our proposed method. The research works [10]–[13] proposed MMCs with improved power quality and a reduced number of cells, but their proposed method cannot be extended to achieve 4N+1 levels. The research in [1], [2] has proposed enhanced MMCs with improved power quality and a reduced number of cells compared to the aforementioned research works. However, the studies presented did not focus on circulating current, arm currents, and capacitor voltage ripple problems; results were only limited to the output voltage and current of the MMC. Therefore, there is an urgent need to implement a modified NLM-based enhanced MMC with reduced circulating current and capacitor voltage problem.

Circulating current suppression and capacitor voltage balancing approaches have been the subject of extensive investigation. Ishfaq *et al.* [14] propose an adaptive proportional integral (API) controller strategy to regulate MMC's circulating and output currents by adapting control parameters in real-time based on operating conditions. This adaptive approach optimizes MMC performance, stability, and efficiency under various scenarios. Simulation results show the method's effectiveness in handling MMC circulating currents, outperforming traditional control techniques like the PR controller. Ud Din *et al.* [15] propose an integral back stepping (IBS) controller to regulate the output and circulating currents of grid-connected MMCs, improving overall performance and stability. Based on Lyapunov stability theory, simulation results demonstrate the controller's effectiveness in managing MMC internal dynamics under various conditions.

In a study [16], sliding mode control (SMC) is introduced as a method for regulating output and circulating currents in MMC. The proposed controller enhances the stability and efficiency of MMC, with simulation results demonstrating its superior performance in comparison to PR based control technique. In study [17], a novel control strategy for reducing circulating current in MMC is proposed, utilizing model predictive control (MPC) combined with a genetic algorithm (GA). This approach aims to minimize circulating current by optimizing the switching angles of MMC modules. The MPC algorithm predicts the

MMC system's future state, while the GA algorithm optimizes the switching angles. Simulations evaluate the proposed strategy, demonstrating its effectiveness in circulating current suppression control (CCSC) and enhancing the MMC system's performance.

However aforementioned research papers [14]–[17] depend on simulation-based findings and do not provide experimental validation to support its claims. Additionally, implementing API, SMC, and MPC for suppressing circulating currents requires the use of high-performance hardware, such as digital signal processors (DSPs) or field-programmable gate arrays (FPGAs). Compared to the aforementioned techniques, the proposed PI-based control for suppressing circulating current is easier to implement and best suited for small to medium power applications in MMC. Various strategies for addressing the MMC circulating current under unbalanced grid situations have been presented in literature [18]–[21]. However aforementioned research work has major limitations such as conventional NLM or SPWM technique is used and experimental verification is not performed.

The major contributions of this research work include an enhanced MMC with a modified NLM featuring a reduced number of cells and harmonic content is proposed. Real-time simulation results for the modified NLM in the enhanced MMC are presented. The circulating current suppression control strategy for reducing circulating current has been applied to the modified NLM in the enhanced MMC. Detailed switch modeling (DSM) is considered the most accurate model among all modeling approaches, as it replicates the actual MMC behavior, switching dynamics, and electromagnetic transients. Unlike average or aggregate MMC modeling approaches, DSM is best suited for studying the internal dynamics of MMC, such as SM capacitor voltage, circulating current, and SM faults. Therefore, the enhanced MMC has been realized using the DSM approach.

3. PROPOSED LABORATORY SETUP AND MODIFIED NLM METHOD

Computer-based simulations, which utilize various software tools such as MATLAB, PSCAD/EMTDC, LabVIEW, Multisim, and PSIM, are known as offline simulations. These simulations have become popular for evaluating the performance of electrical circuits due to their cost efficiency and reduced effort requirements. Nevertheless, offline simulations may not accurately reproduce the true behavior of electrical circuits, leading researchers to approach their results with caution. To address this issue, researchers employ hardware-in-the-loop (HIL) setups to achieve real-time simulation outcomes. In contrast to offline simulations, real-time simulations using HIL more closely represent the actual behavior of electrical circuits. Figure 2 demonstrates the close resemblance between the outcomes of physical/experimental prototypes and HIL setups.

Compared to computer simulations (offline simulations), real-time simulations offer more deterministic results and replicate the actual behavior of the converter [22]. Literature reviews suggest that real-time simulation results closely resemble the actual physical system [23]. There are known HIL setups available from different companies such as RTDS®, OPAL-RT®, Typhoon®, and dSPACE® for producing real-time simulation results. However, the proposed HIL setup is a joint collaboration between OPAL-RT® and National Instruments (NI). The proposed research laboratory uniquely combines computer simulation and hardware testing, allowing researchers to first perform LabVIEW-Multisim co-simulation at computer facilities. In this research work, LabVIEW-Multisim co-simulation is conducted in a way that the digital controller (modified NLM) is implemented using LabVIEW software and the analog circuitry of MMC is developed using Multisim. By utilizing LabVIEW-Multisim co-simulation, researchers initially investigate the behavior of the modified NLM for MMC through software simulation. After obtaining satisfactory software simulation results, the next step is to load the same modified NLM controller with minor modifications into the CompactRIO (CRIO), and the Multisim MMC circuitry is loaded into the NI PXIe hardware to achieve real-time simulation results. It can be concluded that the proposed HIL setup saves time, improves project quality, and provides flexibility for effectively testing and designing power converters. The transition from software simulation (offline simulation) to real-time simulation (HIL setup) is made easier with the proposed setup, as summarized in Figure 3. The proposed HIL setup is explained in detail in research works [22], [23].

The electrical hardware solver (EHS) software (provided by OPAL RT) enables the automatic simulation of an electrical circuit without requiring expertise in FPGA or VHDL programming. This software is compatible with various simulation programs, including MATLAB, PSIM, Multisim, and LabVIEW. By utilizing these four programs, researchers can design the MMC-MTDC project and load it directly onto the NI PXIe FPGA hardware. EHS generates the electrical circuit model and produces real-time simulation results in nanoseconds, as depicted in Figure 4.

As compared to analog setups, HIL configuration demands lesser maintenance, time, and cost. It provides a suitable framework to verify and validate the electrical system, enabling engineers and researchers

to transform their innovative concepts into reality as it generates results that are highly comparable to experimental outcomes. Figure 5 illustrates the configuration of the HIL laboratory that is currently accessible at our university.

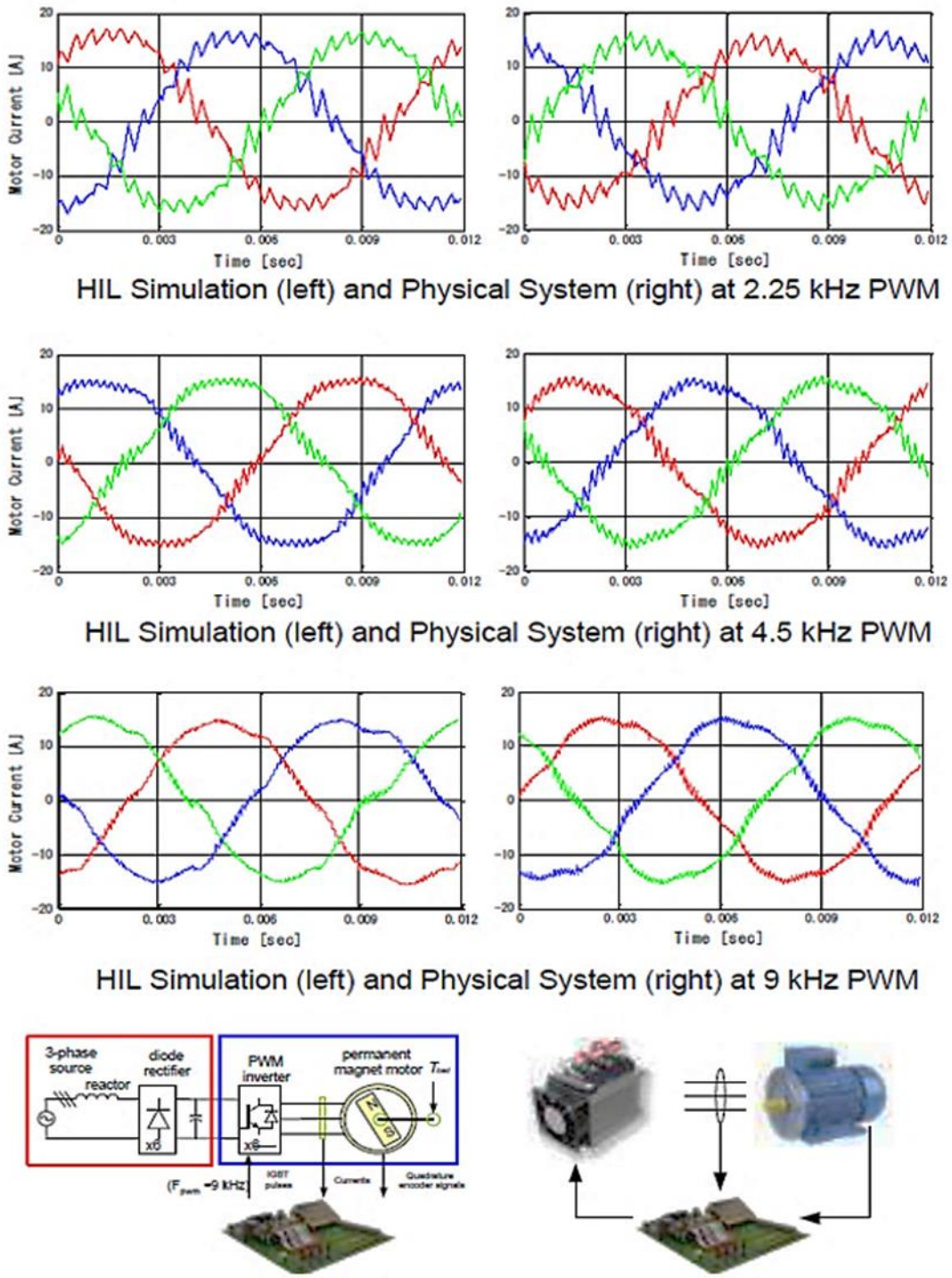


Figure 2. HIL setup vs physical setup

The modified NLM method for half-bridge based MMC is implemented by introducing a small phase shift in the reference waveform for either the upper or lower arm in each phase of the three-phase MMC. The process of adding a small phase shift in the reference waveform to achieve 2N+1 and 4N+1 output levels is depicted in Figure 6. The proposed modified NLM is loaded into National Instruments'

CompactRIO (CRIO) for controller HIL testing. The LabVIEW-developed control algorithm was initially compiled and then burnt into NI CRIO FPGA to observe the controller's real-world performance. The algorithm underwent evaluations at various MMC stages. The configuration of the system is depicted in Figure 7, while the outcomes derived from the CRIO are presented in Figure 8. After the controller exhibited the intended functionality, the CRIO-produced signals were employed to control an actual MMC circuit, which was executed on an NI FPGA-integrated PXIe platform.

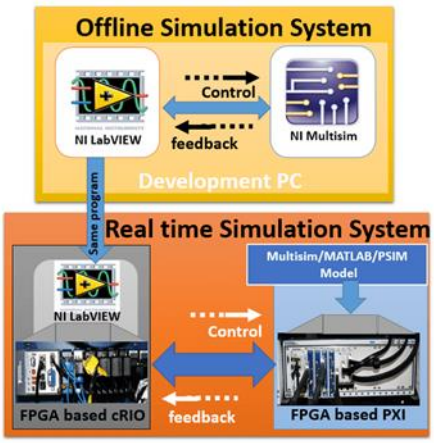


Figure 3. Proposed HIL setup

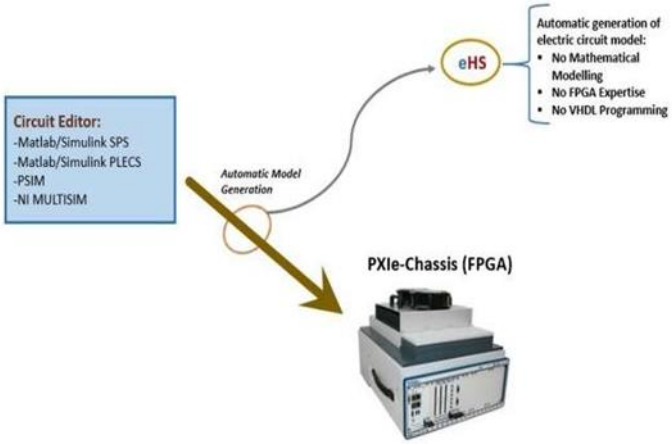


Figure 4. EHS software

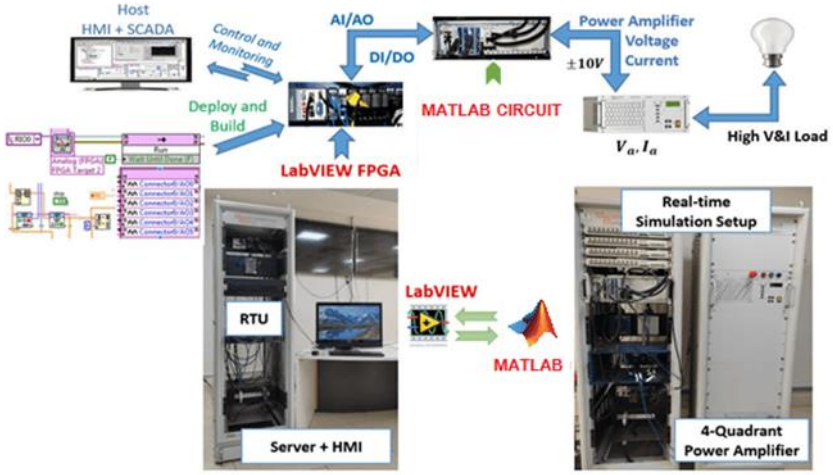


Figure 5. EHS software

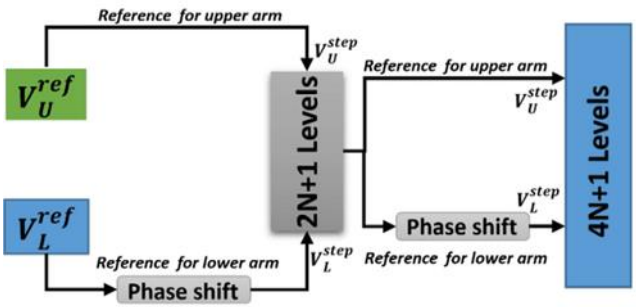


Figure 6. Proposed modified NLM method for MMC

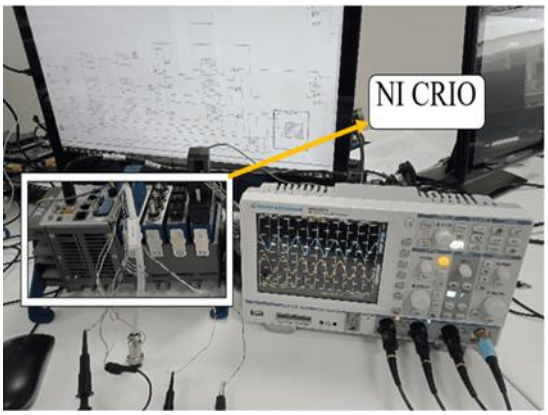


Figure 7. NI CRIO digital controller for implementing proposed modified NLM

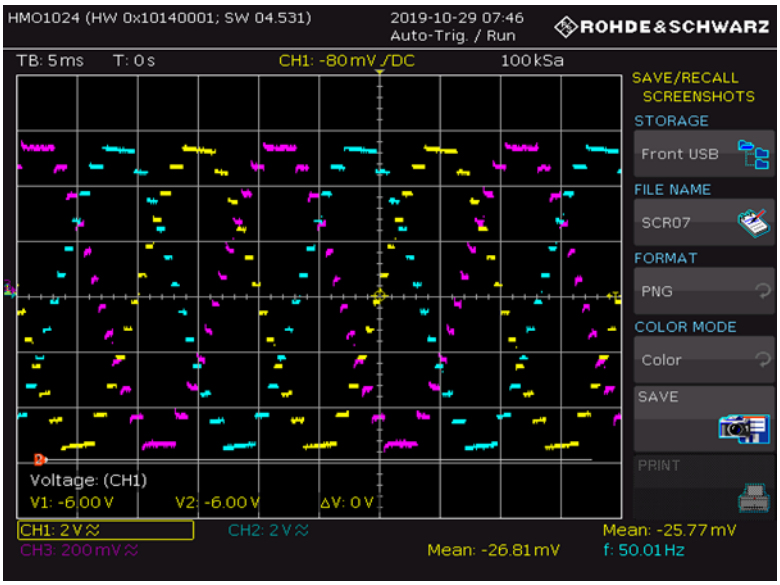


Figure 8. Gate signals for MMC switches from NI CRIO digital controller

4. MMC MATHEMATICAL MODELING

MMC mathematical modeling is applied in Figure 9. Equations (3) and (4) denotes Upper (Vau) and lower (Val) arm voltages. Equation (5) is of phase voltage. Equations (6) and (7) is of upper and lower arm currents. Moreover, equation (8) is for differential current. The differential current is composed of two components such as dc component and ac component. For successful operation of the converter, DC component is required and AC component of circulating must be eliminated. Sub-module upper arm capacitor voltage is represented in (9). It should be noted that CCSC can suppress harmonic components present in phase power and reduce energy variation. Circulating current is shown in Figure 9 with red dotted lines.

$$V_{up} = \frac{1}{2}V_{dc} - V_u - L\frac{di_u}{dt} \quad (3)$$

$$V_{low} = -\frac{1}{2}V_{dc} + V_L + L\frac{di_L}{dt} \quad (4)$$

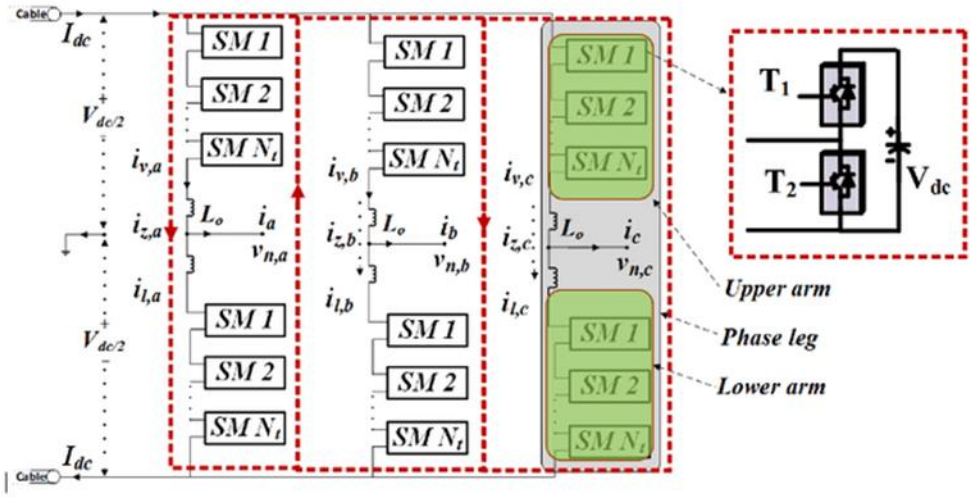
$$V_{phase} = V_{dc} - L_o\frac{d(i_{ua}+i_{la})}{dt} \quad (5)$$

$$i_U = I_{circ} + \frac{i_{dc}}{2} \quad (6)$$

$$i_U = I_{circ} - \frac{i_{dc}}{2} \quad (7)$$

$$iz, = (iu{+}il)2 = Idc/3 + icirc, a \sin(n\omega t + \varphi y) \quad (8)$$

$$V_{cu,i} = \frac{V_{dc}}{N} + \Delta_{V_{ripple,ua}} \quad (9)$$



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5. PROPOSED SYSTEM DESCRIPTION

Figure 9 presents a comprehensive block diagram of the entire control system for the closed-loop enhanced MMC station. The proposed enhancement features a modified NLM control, inner current control, CCSC, and outer control loops including active power control and alternative voltage control, as illustrated in Figure 7. The widely-accepted vector current control scheme is employed for the phase-locked loop (PLL), enabling independent and decoupled active and reactive power control. A thorough presentation of the mathematical equations and implementation processes for the vector current control scheme can be found in references [24]–[26]. The enhanced control system leverages a modified NLM method (4N+1 levels) that requires fewer SMs while also reducing harmonic content. Lastly, the CCSC ensures minimal circulating current, with its block diagram displayed in Figure 10.

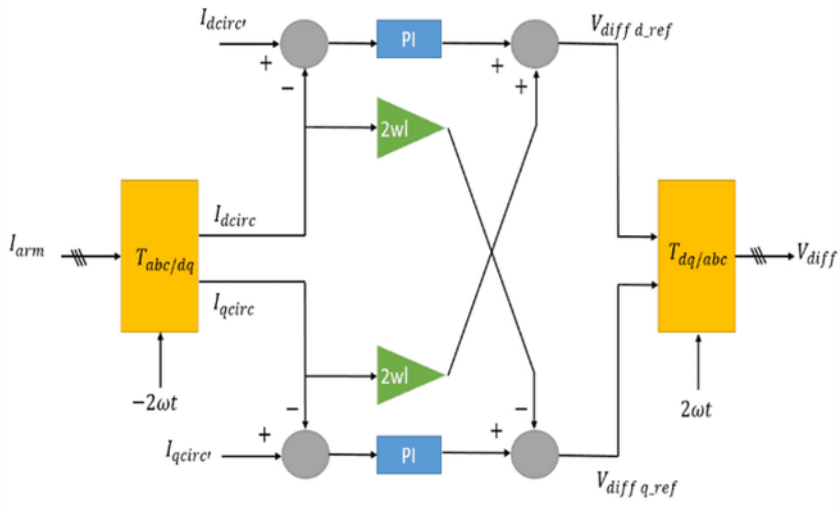

Figure 10. CCSC block diagram

6. REAL TIME SIMULATION RESULTS FOR ENHANCED MMC WITH REDUCING CIRCULATING CURRENTS AND CAPACITOR VOLTAGE RIPPLE

The MMC circuit, developed using Multisim, is loaded into the NI PXI, a floating-point solver based on FPGA technology. This solver generates a bit file for the circuit and executes it within nanoseconds on the FPGA. Subsequently, the previously designed modified NLM is incorporated into an FPGA-powered CRIO controller to manage the circuit operating within the PXI system.

It is important to note that the chosen number of SMs (SMs) is 12 (N=12). The conventional NLM can generate 13 levels of output voltage and current (N+1). However, the proposed modified NLM can produce 25 levels of output voltage and current (2N+1). By making minor adjustments to the phase shift of reference signals, the modified NLM can be further extended to achieve 49 levels of output voltage and current (4N+1).

Before the 0.04-second mark, the 2N+1 levels modified NLM is activated, while the 4N+1 levels proposed modified NLM is activated after 0.04 seconds. Figures 11 and 12 display the output voltages and currents for the proposed modified NLM with 12 SMs, respectively. Consequently, it can be concluded that the proposed modified NLM is capable of achieving superior power quality (reduced THD) without increasing the number of SMs compared to the conventional NLM.

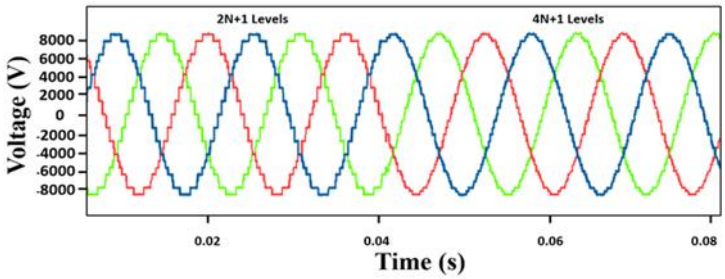

Figure 11. Real-time simulation results for MMC output voltages with 25 and 49 levels

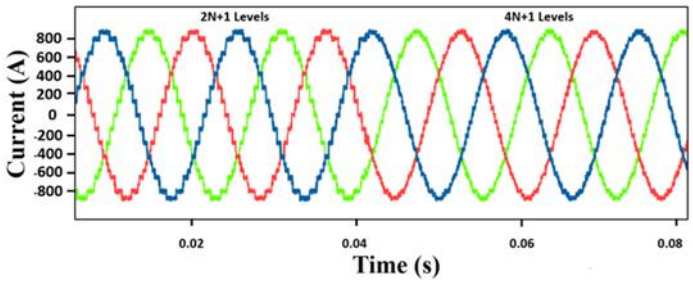

Figure 12. Real-time simulation results for MMC output currents with 25 and 49 levels

The MMC is deemed robust when it exhibits both improved power quality and effective internal dynamics control, such as reduced circulating current and capacitor voltage ripple. The proposed enhanced MMC not only guarantees optimized power quality with 4N+1 output waveform levels but also addresses circulating current and capacitor voltage ripple concerns. The internal dynamics control robustness, such as the CCSC, has been evaluated using a 49-level enhanced MMC. It is evident that the proposed CCSC performs well with the enhanced MMC (4N+1 levels), effectively reducing circulating currents to below 10% of the nominal current, as shown in Figure 13. Moreover, the proposed enhanced MMC ensures not only reduced circulating currents but also well-balanced sub module capacitor voltages, as illustrated in Figure 14.

Figure 14 demonstrates that the MMC's capacitor voltage ripple is minimized, operating within safe limits and preventing the converter from tripping. Furthermore, the capacitor voltages remain balanced and adhere to standard grid codes. As a result of the effective suppression of circulating currents and capacitor voltage ripple, the proposed MMC exhibits smoother arm currents with reduced harmonic content, as displayed in Figure 15. Lastly, Figure 16 shows that the proposed enhanced MMC has a standard modulation index value of 0.8 p.u, ensuring that over-modulation and under-modulation issues are avoided during MMC operation.

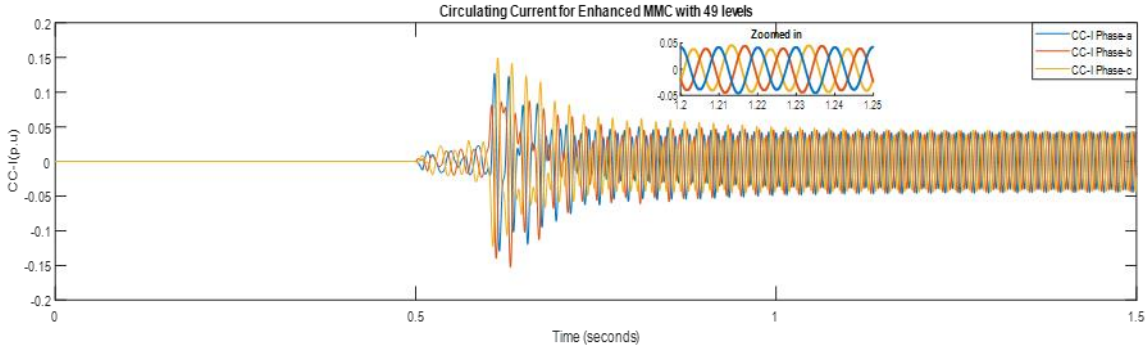

Figure 13. Circulating currents for proposed MMC with 49 levels

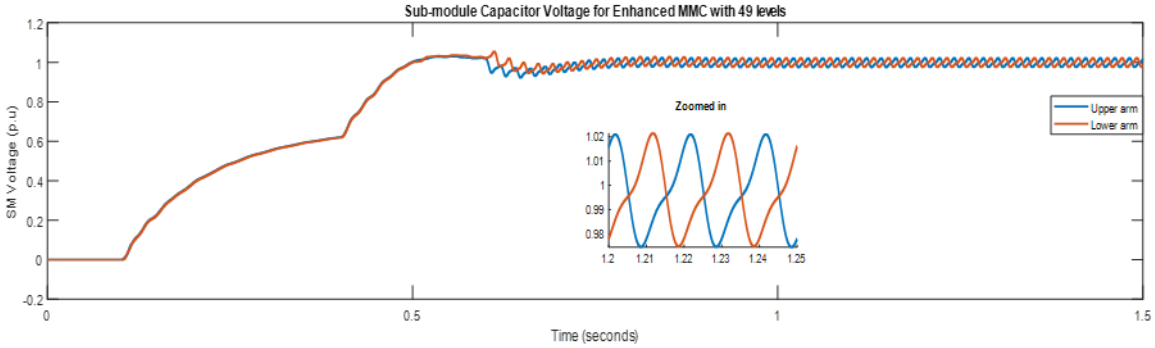

Figure 14. Sub-module capacitor for proposed MMC (Phase A) with 49 levels

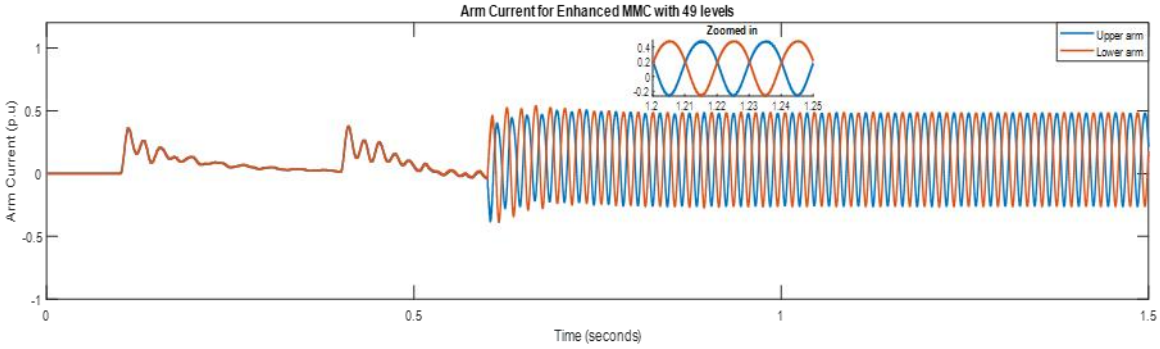

Figure 15. Arm currents for proposed MMC (Phase A) with 49 levels

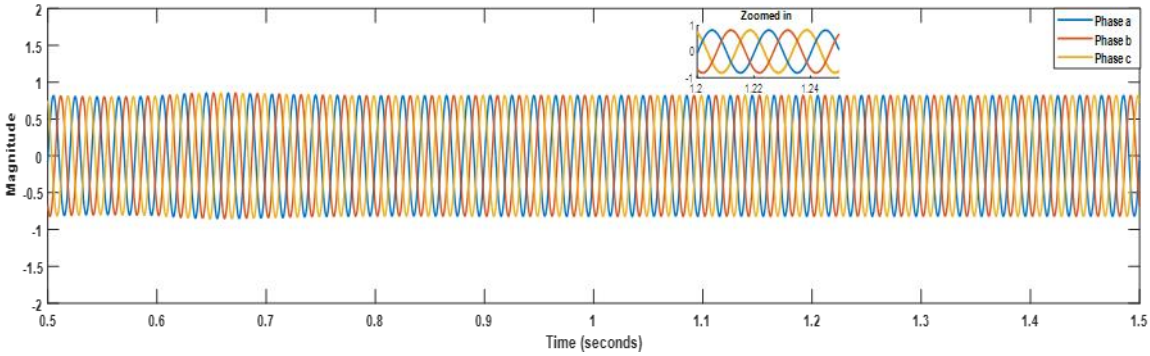

Figure 16. Modulation index value for proposed MMC with 49 levels

7. CONCLUSION

Previous literature focused on the modified nearest level control (NLC) for MMC with 4N+1 levels; however, the studies were limited to examining the output voltage and current waveforms of MMCs. This research broadens the scope by investigating the internal dynamics control of modified NLC for enhanced MMCs. The presented results demonstrate that the proposed CCSC technique successfully addresses the circulating current and capacitor voltage ripple issues, while improving power quality (4N+1). Furthermore, the arm currents exhibit a smoother, sinusoidal profile, and the modulation index adheres to the standard value of 0.8 per unit (PU). This comprehensive analysis highlights the effectiveness of the proposed CCSC technique in managing the internal dynamics of enhanced MMCs, contributing to the advancement of MMC technology and its practical applications.

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