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ISM-Band Energy Harvesting Wireless Sensor Node

FNU Naveed
University of Arkansas-Fayetteville

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ISM-Band Energy Harvesting Wireless Sensor Node

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Naveed
Karachi Institute of Economics and Technology
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Institute of Industrial Electronics Engineering (IIEE, NED)
Bachelor of Engineering in Electronic Engineering, 2014

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University of Arkansas

This dissertation is approved for recommendation to the Graduate Council.

_____
Jeff Dix, Ph.D.
Dissertation Director

_____   _____
Jia Di, Ph.D.   Zhong Chen, Ph.D.
Committee Member   Committee Member

_____
Morgan Ware, Ph.D.
Committee Member

Abstract

In recent years, the interest in remote wireless sensor networks has grown significantly, particularly with the rapid advancements in Internet of Things (IoT) technology. These networks find diverse applications, from inventory tracking to environmental monitoring. In remote areas where grid access is unavailable, wireless sensors are commonly powered by batteries, which imposes a constraint on their lifespan. However, with the emergence of wireless energy harvesting technologies, there is a transformative potential in addressing the power challenges faced by these sensors. By harnessing energy from the surrounding environment, such as solar, thermal, vibrational, or RF sources, these sensors can potentially operate autonomously for extended periods. This innovation not only enhances the sustainability of wireless sensor networks but also paves the way for a more energy-efficient and environmentally conscious approach to data collection and monitoring in various applications. This work explores the development of an RF-powered wireless sensor node in 22nm FDSOI technology working in the ISM band for energy harvesting and wireless data transmission. The sensor node encompasses power-efficient circuits, including an RF energy harvesting module equipped with a multi-stage RF Dickson rectifier, a robust power management unit, a DLL and XOR-based frequency synthesizer for RF carrier generation, and a class E power amplifier. To ensure the reliability of the WSN, a dedicated wireless RF source powers up the WSN. Additionally, the RF signal from this dedicated source serves as the reference frequency input signal for synthesizing the RF carrier for wireless data transmission, eliminating the need for an on-chip local oscillator. This approach achieves high integration and proves to be a cost-effective implementation of efficient wireless sensor nodes.

The receiver and energy harvester operate at 915 MHz Frequency, while the transmitter functions at 2.45 GHz, employing On-Off Keying (OOK) for data modulation. The WSN utilizes an efficient

RF rectifier design featuring a remarkable power conversion efficiency, reaching 55% at an input power of -14 dBm. Thus, the sensor node can operate effectively even with an extremely low RF input power of -25 dBm.

The work demonstrates the integration of the wireless sensor node with an ultra-low-power temperature sensor, designed using 65 nm CMOS technology. This temperature sensor features an ultra-low power consumption of 60 nW and a Figure of Merit (FOM) of 0.022 $[nJ.K^{-2}]$. The WSN demonstrated 55% power efficiency at a TX output power of -3.8 dBm utilizing a class E power amplifier.

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Dedication

I dedicate this work to my beloved parents, my sisters Saba and Yumna who were always there to care for me, my ever-supportive brothers, Shakeel, Waseem, and Nadeem, my nephew Saad and my best mate Muhammad Hassan. Thank you so much. It could not have happened without you all.

Table of Contents

List of Figures

List of Tables

CHAPTER 1 INTRODUCTION

1.1 Overview of Wireless Sensor Nodes and Energy Harvesting

In the ongoing era of a rapidly transforming world and cutting-edge technological advancements, Wireless Sensor Nodes (WSNs) have emerged as a revolutionizing way of monitoring, collecting, and processing data from the physical world [1]. Wireless sensor networks consist of numerous, small, autonomous units called Sensor Nodes. These sensor nodes are typically equipped with multiple sensors, data acquisition (DAQ) units, a power source, and wireless communication circuitry. WSNs are distributed in an area and work within a network to monitor and gather real-time data from the environment such as temperature, humidity, wind speed, and sensor address, and transmit it to a network server. Having wireless capabilities in these sensor nodes facilitates their application in diverse fields of applications such as remote health care, environmental monitoring, smart homes, industrial automation, and smart agriculture. Wireless data transmission also simplifies the deployment of a vast number of sensor nodes by eliminating the need for wiring while cutting the implementation cost. Sensor nodes in a network usually rely on batteries as their power source thus their maintenance cost highly depends on the power utilization efficiency of the node.

Depending upon the type of sensor the power consumption of a single sensor node can range from 100uW to 100mW [2],[3]. Some applications can have a sensor node density as high as 20 nodes/m^2 [4] and with the growth in the WSNs market size, the sensor networks are forecasted to increase in their coverage and density. The limitation of battery-powered sensor become increasingly evident as the node densities in a sensor network continue to increase. Moreover, disposed batteries ending up in landfills pose serious hazards to the environment. The significant challenges in terms of maintenance, environmental impact, and operational efficiency have

sparked research interest in many fields such as programming, networking, software, and circuit designing. Different control algorithms, routing protocols, circuit optimization, and low-power techniques have been developed to increase the life span of the sensor nodes [4]–[7]. These techniques are effective in adding years to the life of the sensor nodes, however, they cannot avoid the natural degradation and self-discharge of the batteries [8], thus batteries may soon become an unreliable source of power in WSNs.

Energy harvesting technique (EHT) is a promising field of research which when coupled with WSNs extends their lifespan and potentially makes them maintenance-free. Not only does it address challenges posed by high node densities, but it also positively impacts the environment by reducing battery waste. The energy harvester converts the energy from ambient sources (like heat, vibration, light, and electromagnetic radiation) into usable electrical energy to power up the node. Energy from ambient sources have a limited window of availability thus power management circuit (PMC) and a storage element (for example super capacitor) is necessary part of an energy-harvesting WSN. The power management circuit keeps the WSN in hibernation until the energy is available to harvest or when the data is needed to be collected from the node. However, prolonged standbys and duty cycling can severely limit the performance of the WSN and make their implementation challenging. Hence, the focus is shifting towards efficient energy harvesting techniques and ultra-low-power designs as important design considerations in the realization of such WSNs.

1.2 Targeted Market Survey and Application

The industrial WSN market have seen significant growth in the last decade and it's estimated to grow from USD 4.97 billion in 2021 to reach USD 8.62 billion in 2030 [9]. This growth is attributed to the robust manufacturing sector, affordable mass production, and their ability to

provide real-time data. Wireless sensors in the medical market will grow from USD 1.57 Billion in 2020 to reach USD 3.56 Billion by 2028 [10]. The growing percentage of the elderly population due to better health care, increased health awareness with wearable medical fitness devices, and adoption of in-home medical devices are some major contributing factors to the growth of wireless sensors in the medical market. This growth in the WSN market will attract a vast number of industries to integrate wireless sensor networks into their applications. Here we highlight the key sectors and applications for our work.

Industrial Automation

Various major industry leaders including General Electric, Siemens, and Boeing, have adopted WSNs solutions to harness the advantages offered by them in industrial automation. WSNs enable the enhancement of the scalability and efficiency of the manufacturing processes in these industries [11]. Small and medium-sized enterprises have also experienced several advantages from adopting WSN, such as decreased maintenance and operational costs, increased productivity, and scalability, boosted revenue, improved flexibility, and enhanced overall performance.

Precision Agriculture and Farming

WSNs have enhanced modern farming techniques by enabling precision agriculture. Sensor nodes in agricultural fields are used to monitor the temperature around the crops, soil acidity, and moisture contents to increase yields, cut costs, and increase productivity [12]. This information allows farmers to take timely steps to protect crops from damage by setting up pest control, optimizing fertilizer use, and irrigation scheduling. Enhancing precision farming positively impacts the environment by limiting the use of pesticides and chemical fertilizers that contaminate underground water sources.

Environmental Monitoring and Smart Cities

According to forecasts by the United Nations, it is anticipated that 70% of the global population will reside in cities and urban regions by the year 2050 [13]. Consequently, this trend suggests a continual increase in emissions and energy consumption with each passing year. This vast urbanization have necessitated the development of smart cities where WSNs enable optimized traffic control, air quality monitoring, emission tracking, enhanced surveillance, and resource management. The Global Smart city market is estimated to grow around 18.1% during the forecast period of 2022 – 2027 [14]. The initiatives in the development of smart cities have fueled the demand for WSN solutions. Leading cities such as New York, Singapore, Barcelona, and Amsterdam have implemented large-scale WSN projects for urban management.

Retail and Inventory Management

Retailers are increasingly adopting WSNs to improve inventory management, supply chain monitoring, and customer behavior analysis. These networks are helping the retail industry to address some key challenges of improving inventory accuracy, automated checkouts, increasing profitability, customer retention, enhanced stocking, and improving overall shopping experience. Retail giants like Walmart and Amazon are implementing WSNs as a standard technology in their stores and warehouses [15].

1.3 Design Objectives

The design objective of this work revolves around researching, designing, and demonstrating a self-contained wireless sensor node capable of harvesting energy as its power source. The design challenges and objectives include:

- Develop energy-efficient circuitry and investigate low-power techniques to optimize the energy consumption of the sensor node.

- Integrate the energy harvester in the sensor node and optimize the interface between them to enhance power efficiency, sensitivity, and range of operation.

- Create a scalable interface with sensors, enabling the acquisition of data from diverse sensor types and ensuring compatibility with standard protocols.

- Develop robust and energy-efficient wireless communication systems for data transmission. Implement strategies to minimize unnecessary transmission thus conserving energy.

- Maintain a balance between the cost, size, and performance, utilizing innovation in both energy harvesting and circuit design techniques.

- Demonstrate the practical application of the developed sensor node by integrating it with a sensor, showing its real-world functionality and usability.

1.4 Brief Introduction to the Components of the WSN Design

Fig. 1.0.1 shows a block design representation of a typical energy-harvesting wireless sensor node. The diagram shows the essential components of the design that enable autonomous operation. The WSN features an energy harvester that captures energy from the environment in the form of light, vibration, thermal, or electromagnetic and converts it into usable electrical energy. This block serves as the power source for the WSN. WSNs are also equipped with specialized sensors along with interface circuitry to acquire data from the environment. A control processing unit processes the received data and makes real-time decisions according to set conditions. A wireless communication module transmits the acquired data to a server of the wireless sensor network. The WSN also integrates an energy storage unit that stores the surplus harvested energy and utilizes it in the events when there is low energy to harvest, thus maintaining the functionality of the WSN.
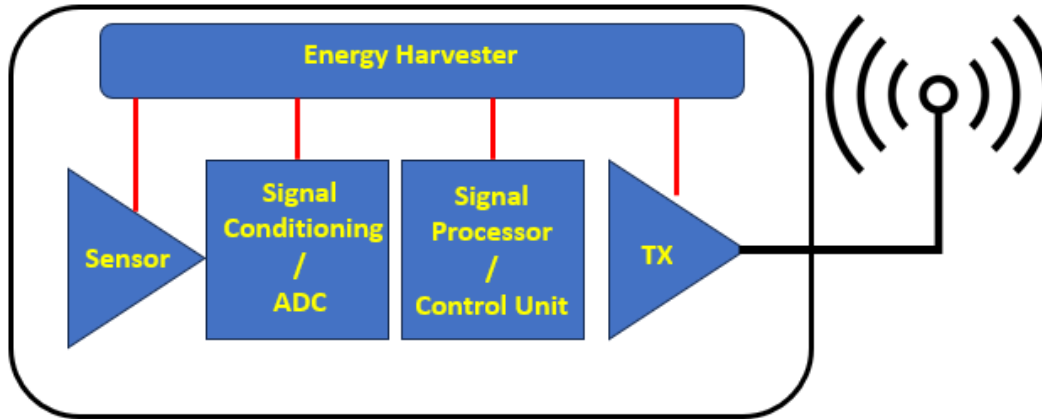
Fig. 1.0.1 Block representation of a typical energy harvesting WSN.

Additionally, efficient power management circuity regulates and distributes the harvested energy to the system ensuring that the network operates optimally under different operating conditions. The Fig. 1.0.1 depicts the integration of different components that form a robust, autonomous, energy-harvesting wireless sensor node. This work will design and demonstrate such an autonomous WSN with efficient energy harvesting capabilities.

1.5 Organization of Dissertation

The organization of the dissertation document is discussed below:

In Chapter 2, a review of various EHT is presented for our application. Each technique is evaluated for its unique opportunities, challenges, and complexities. The significance of utilizing the ISM band for our work is presented.

Chapter 3 presents a description of the proposed system with its design considerations and requirements. A brief discussion of the signal generation scheme, the significance of power management, temperature sensor design, and wireless data transmission circuitry is also covered in this chapter.

Chapter 4 presents the design and simulation of all the necessary components of the RF energy harvester and the PMC .

Chapter 5 presents the design and simulation of all the necessary components of the frequency synthesizer circuit. In this chapter, a frequency multiplier architecture is implemented to generate the 2.4 GHz carrier signal. The choice of Class E switching RF power amplifier to achieve good power amplifier efficiency is presented.

Chapter 6 presents the design of an ultra-low power temperature sensor fabricated on a separate chip in a 65 nm CMOS process. The temperature sensor is designed to be integrated with the proposed WSN in this work. The experimental results of the fabricated temperature sensor are compared with previous reported works.

Chapter 7 presents the design integration of WSN components in the 22nm FDSOI process. The details of the test PCB and equipment are provided. The measurement results are presented and compared with previous implementations.

Finally, chapter 8 concludes the work and provides future research recommendations.

CHAPTER 2 ENERGY HARVESTING MECHANISM AND COMPARATIVE

ANALYSIS

Sustainable energy provision stands as a cornerstone for the prolonged and autonomous operation of wireless sensor networks. With the advancements in CMOS (Complementary Metal Oxide Semiconductor) technologies, their power consumption is going down. This development has opened doors to power WSNs with the harvested energy from the ambient environment mitigating the challenges posed by finite power sources in WSNs. This chapter reviews a range of energy harvesting methods, each approach is evaluated for their unique opportunities, challenges, and complexities. At the end of the chapter, we briefly explore the significance of utilizing the ISM band for RF energy transfer and communication infrastructure within our WSN implementation.

2.1 Comparative Analysis of Various Energy Harvesting Techniques

Microelectronics systems can be powered up with a diverse range of energy harvesting sources. The output power of the energy harvester exhibits significant variability, influenced by factors like the harvester type and its surroundings. This section will provide a brief overview of several energy harvesting technologies, including photovoltaic, vibrational, thermal, and RF energy harvesters. These techniques will be evaluated based on parameters such as output power, limitations, advantages, disadvantages, reliability, and applications.

Solar Energy Harvesting and Photovoltaic Cells

Photovoltaic cells, also known as solar cells, work based on the principle of the photovoltaic effect. When a light source shines on the cell, it excites electrons in the semiconductor material, creating a flow of electric current. This process occurs due to the presence of a p-n junction within the cell, which separates the positive and negative charges and generates a voltage difference. Photovoltaic energy harvesting has been explored to power microelectronics, Several studies have investigated

the integration of photovoltaic cells into microelectronic devices and wearable systems [16],[17],[18]. These studies highlight the potential of photovoltaic cells in providing sustainable and renewable power for various applications. The power density of photovoltaic cells typically ranges from 5 to 20 mW/cm² under standard sunlight conditions. The efficiency of photovoltaic cells in converting solar energy into electrical energy has improved over the years. Advances in materials, such as the use of perovskite materials, have shown great potential in enhancing the efficiency of photovoltaic cells [17]. However, the integration of perovskite materials into photovoltaic cells for microelectronics is still an area of ongoing research. Despite the advantages of photovoltaic energy harvesting, some limitations make it less suitable for wireless sensor networks (WSNs). One major limitation is the reliance on direct sunlight as the primary source of energy. WSNs are often deployed in various environments, including indoor and underground settings, where access to direct sunlight is limited [19]. This restricts the continuous and reliable power supply to the sensor nodes.

Another limitation is the size and weight of photovoltaic cells. Microelectronics and wireless sensor nodes require compact and lightweight power sources for seamless integration. Traditional photovoltaic cells, especially those based on silicon, can be bulky and heavy, making them impractical for small-scale devices [20].

Furthermore, the efficiency of photovoltaic energy conversion is a concern, especially under low-light conditions. While advancements have been made in improving the efficiency of photovoltaic cells, they may not generate sufficient power in environments with limited sunlight [18]. This can result in insufficient power generation for the energy requirements of microelectronics and WSNs.

Vibrational Energy Harvesting

Vibration energy harvesting is a promising technique that is considered a feasible solution for continuous power supply, replacing batteries in microelectronic devices [21]. This technology has gained considerable interest as a means of powering wireless sensor nodes[22]. There are various designs and configurations for vibration energy harvesters among which piezoelectric energy harvesting is a commonly used method. The piezoelectric material when deformed with movements in the environment can convert waste vibrational energy into electrical energy, making it a useful self-powered source for driving microelectronic devices [23]. An application of vibrational energy harvesting using piezoelectric material is a small-scale wind energy harvesting from vortex-induced vibrations (VIV) which has been introduced as a renewable power source for microelectronics and wireless sensors [24]. Magnetoelectric (ME) harvesting is another useful vibrational energy harvesting technique. In ME harvesters, external vibrations induce changes in the magnetic field through the movement of a magnet. Within ME composites, the piezomagnetic phase responds to these vibrations by either elongating or contracting. This action strains the ferroelectric phase in the composites, producing an output voltage through the piezoelectric effect. Magnetoelectric vibration energy harvesters are suitable for capturing energy from low-frequency vibrations such as machinery, vehicles, and even human movements An application of magnetoelectric harvester involves harvesting energy from human motion, such as walking or running [25]. The maximum output power of 14.44 μW has been achieved for the prototype shown in Fig. 2.0.1.
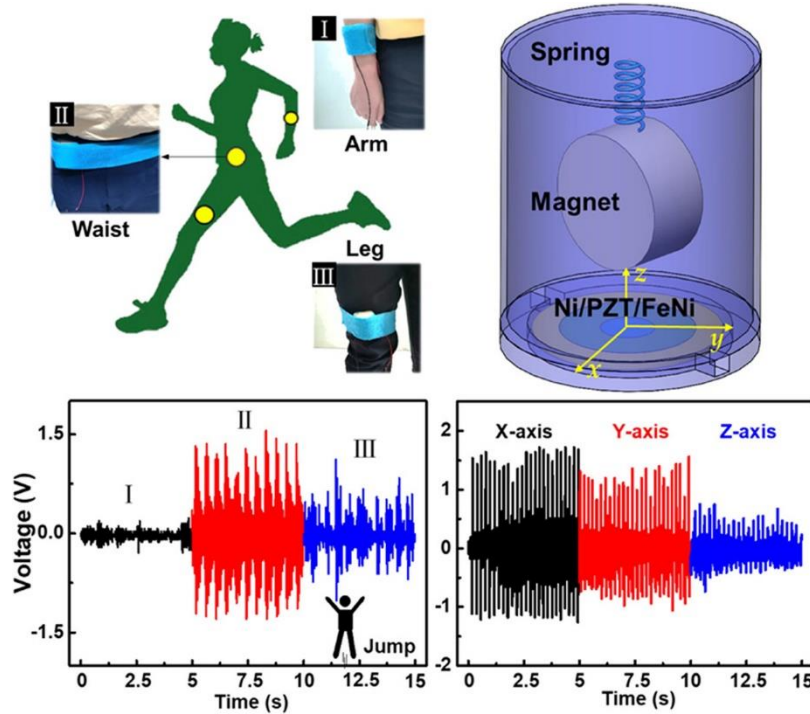
Fig. 2.0.1 The output of the magnetoelectric harvesting from human motions. (a) The prototype is attached to the arm (I), waist (II), and leg (III). The output under jumping conditions is shown [25].

The frequency up-conversion technique is significant in the design of micro-scale energy harvesting devices, where the resonance frequency of the structure can be at the level of 1 kHz, while the ambient vibration frequency is generally below 100 Hz [26]. For example, a hybrid energy harvesting system incorporating frequency up-conversion components is proposed in [27]. The system includes a flexible base and two cantilevers (internal and external). These distinct cantilevers, designed for piezoelectric and electromagnetic transduction, allow the internal piezoelectric cantilever to produce significant power output by harnessing large-displacement vibrations. Another design is a 2 × 2 array piezoelectric-electromagnetic hybrid energy harvester, which can increase the power output by utilizing multiple harvesters [21]. A resonant hybrid vibration energy harvester using a piezoelectric cantilever with electret-based electrostatic coupling has also been developed, offering frequency-tunable resonant characteristics [28].

Vibration energy harvesting has shown great potential as an energy source for microelectronic systems and wireless sensor nodes, providing a long-term power supply to these devices [29]. However, several limitations need to be considered when utilizing this technology. One limitation is the efficiency of energy conversion from mechanical vibrations to electrical energy is often low, resulting in limited power output [30]. Another limitation is the narrow bandwidth of vibration energy harvesters. Most vibration energy harvesters are designed to operate within a specific frequency range, which may not cover the full spectrum of ambient vibrations[31]. This can restrict the harvesting capability and limit the overall energy generation. The size and weight of vibration energy harvesters can also pose limitations. To be integrated into small-scale devices, such as wireless sensor nodes, the harvesters need to be compact and lightweight. However, the design and construction of efficient vibration energy harvesters that meet these size and weight requirements can be challenging [32].

Thermal Energy Harvesting Through Thermoelectric Generators

The working principle of thermal energy harvesting (TEG) is based on the Seebeck effect, which occurs when a temperature gradient is applied across a thermoelectric material. The temperature difference causes a flow of charge carriers (electrons or holes) from the hot side to the cold side of the material, generating an electric potential difference and producing electrical power [33]. Fig. 2.0.2 illustrates the thermoelectric energy harvesting from the Seebeck effect [34].
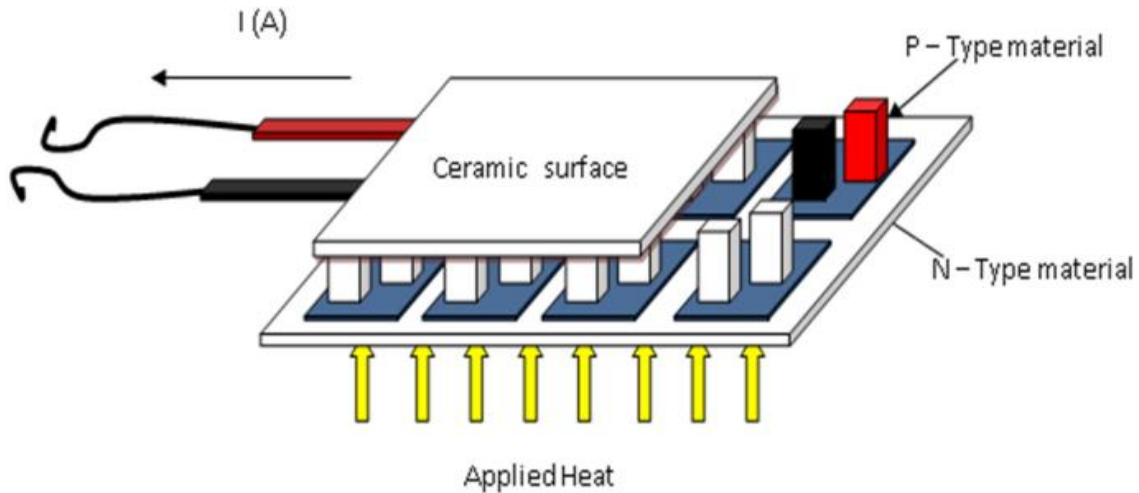
Fig. 2.0.2 The thermoelectric energy harvesting from the Seebeck effect [34].

The efficiency of TEGs depends on the thermoelectric properties of the materials used, such as the Seebeck coefficient, electrical conductivity, and thermal conductivity. A single thermocouple can have a voltage generation coefficient of 0.2 mV/K therefore a large number of such units are required to generate enough voltages to power up a circuit or system. The power output and efficiency of TEGs depend on various factors such as the temperature gradient, material properties, and device design. The power output of TEGs can range from microwatts to several watts, depending on the specific application and operating conditions [35]. The thermoelectric performance of a thermocouple is evaluated using a dimensionless figure of merit (ZT) defined as (1)

$$ZT = \left(\frac{\alpha^2 \sigma}{\kappa}\right)$$

(1)

Where α is the Seebeck coefficient, σ is electrical conductivity, κ is thermal conductivity and T is the temperature. To obtain a high FoM, the Seebeck coefficient and electrical conductivity are desired to be high, while thermal conductivity must be low. Lower thermal conductivity of the material is desired in maintaining the temperature difference for producing a stronger Seebeck effect. The review report by [34] provides an overview of recent developments in thermoelectric

13

energy harvesters for various applications. It highlights the ability of TEGs to utilize waste thermal energy generated by different applications, making them suitable for a wide range of potential applications. [36] discuss the design of thermoelectric clothes that harvest thermal energy from the human chest, highlighting the potential of TEGs in wearable applications. When integrated into a shirt, the device demonstrated a substantial voltage output of 11.5 mV and a power output of 146.9 nW from the chest area, with an ambient temperature of 278 K. [37] investigate the homogeneous incorporation of MXene in $(Bi, Sb)_2Te_3$ matrix to achieve high-efficiency thermoelectric power generation. These studies emphasize the importance of materials and structural design in enhancing the thermoelectric conversion efficiency of TEGs.

The integration of TEGs into microelectronics and wearable devices has also been explored. [38] discuss the materials strategies and device architectures of emerging power supply devices for implantable bioelectronics, including TEGs. They highlight the effectiveness of thermoelectric materials in generating power for implantable devices. [39] presents a micropower thermoelectric generator form using a thin Si membrane in a planar CMOS process. The device shown in Fig. 2.0.3 consists of a Si membrane (100 nm thick) with embedded n,p doped regions. The device uses the temperature difference between the cold membrane and the hot Si frame to achieve a power output of 4.5 $\mu W/cm^2$ for a temperature difference of 5.5 K.
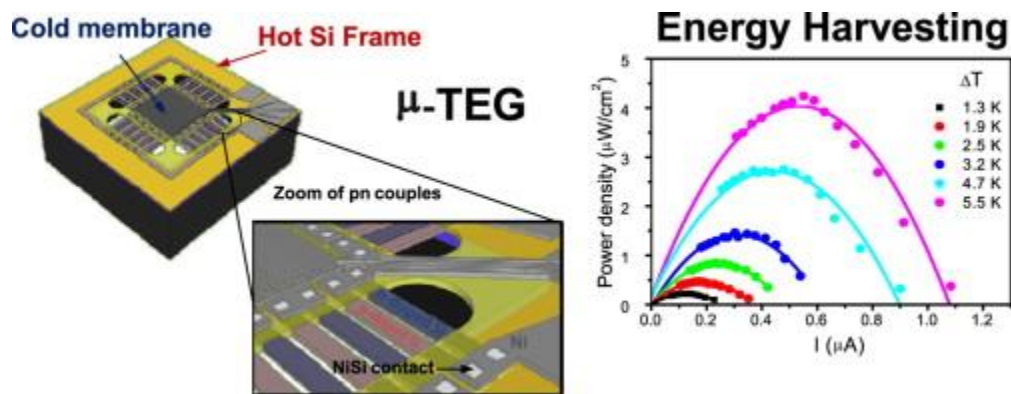
Fig. 2.0.3 Micropower thermoelectric generator fabricated in a planar CMOS process. [39]

While TEGs offer potential benefits for microelectronics, some challenges need to be addressed. [40] discuss unconventional thermoelectric materials for energy harvesting and sensing applications, highlighting the limitations of ionic thermoelectric effects for typical thermoelectric generators under continuous operation.

Despite the potential of TEGs for energy harvesting, some limitations make them less suitable for WSNs. One limitation is the relatively low efficiency of TEGs compared to other energy harvesting techniques. The conversion efficiency of TEGs is typically lower (5 – 8 %) than that of photovoltaic cells or vibration energy harvesters [34]. This limits the amount of electrical power that can be generated from a given temperature gradient. Another limitation is the requirement for a significant temperature difference to generate sufficient power. TEGs operate based on the temperature gradient between the hot and cold sides of the device. In many WSN applications, the available temperature difference may be small, resulting in low power output from the TEGs [41]. The size and weight of TEGs can also be a limitation for microelectronics and WSNs. Traditional TEGs often consist of bulky and heavy materials, which may not be suitable for integration into small-scale devices [42]. However, advancements in flexible and lightweight TEG materials, such as organic conducting polymers, have shown promise in addressing this limitation [43]. Furthermore, the cost of TEG materials can be a barrier to widespread adoption. Some thermoelectric materials, such as bismuth telluride, are expensive and may not be cost-effective for large-scale deployment in WSNs [34]. Research efforts are focused on developing cost-effective and scalable thermoelectric materials for improved energy harvesting performance.

Radio Frequency (RF) Energy Harvesting

Collectively electromagnetic (EM) waves like Gamma rays, X-rays, Infrared waves, and light waves form the electromagnetic spectrum. Radio waves, a component of this spectrum, are

employed in wireless communication to transmit sound messages and information. Electromagnetic radiation falling within the frequency range of approximately 10 kHz to 100 GHz is specifically termed Radio Frequency. The transmission of energy through electromagnetic waves can be categorized into two types: near-field energy transfer and far-field energy transfer. Near-field energy transfer, also known as non-radiative energy transfer, occurs within approximately one wavelength (λ) from the antenna. It relies on the resonance of two magnetically coupled coils. Unlike radiative transfer, this method confines the energy within a short proximity of the transmitter. No power leaves the transmitter if there is no receiving device within their limited range to "couple" to. The range of this transfer is limited, and the transferred energy decreases exponentially with distance, making it unsuitable for WSN application. Far-field energy transfer, also known as RF energy transfer, extends beyond one wavelength (λ) from the antenna. This form of transfer, termed radiative, involves the energy leaving the antenna, with the electric and magnetic fields perpendicular to each other, propagating as an electromagnetic wave. The energy radiates in all directions and is lost if there's no receiver in its trajectory. However, various techniques [44], [45] are utilized to concentrate the transmission, minimizing losses, and expanding the range of energy transfer. Fig. 2.0.4 shows a block diagram of a far-field energy harvesting system [46]. The power received (P_{RX}) at the Rx-Antenna is converted into an electrical signal and transferred to a CMOS RF-DC converter (RF- RF-Rectifier), the rectifier converts the signal into a DC voltage and stores it as energy in a capacitor/battery.
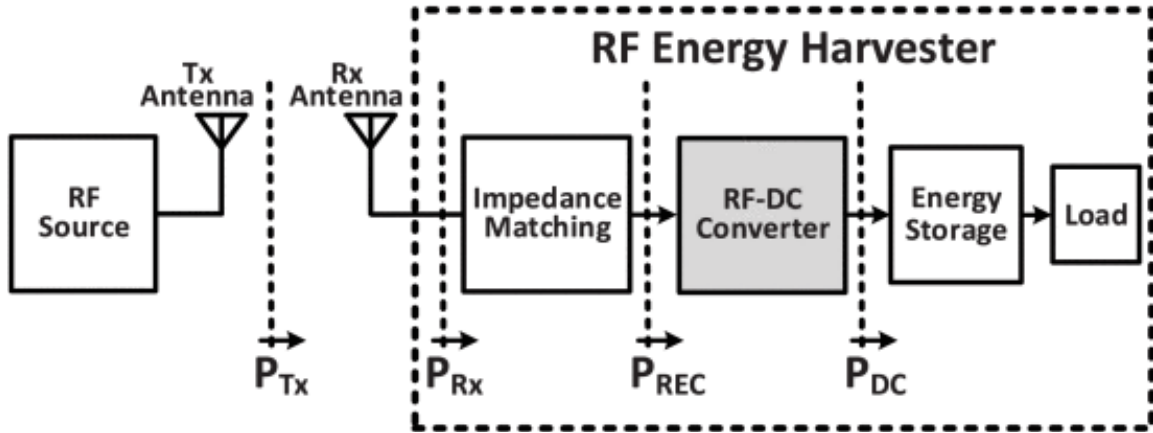
Fig. 2.0.4 Block diagram of a far-field RF energy harvesting system [46].

RF transmitters not designed for the transfer of radiofrequency energy are referred to as ambient RF sources. RF energy harvesting involves capturing and converting these ambient radio frequency (RF) signals into electrical energy. In essence, this radiofrequency energy is free. Ambient radio frequency sources have a wide range of transmit powers which varies based on factors like location and purpose. FM radio towers range from a few hundred watts to 100 kW, digital TV towers use kilowatts to hundreds of kilowatts, and GSM 900 MHz and GSM 1800 MHz towers typically operate at 20-100 watts. Urban areas often have lower power towers due to higher user density, while rural areas might have fewer towers with higher power for wider coverage. While some ambient sources transmit more power than others, their available power density at a given distance varies due to their different transmission frequencies. This decay in available power can be calculated using the Friis transmission equation as (2)

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\,\pi R)^2} \qquad (2)$$

Where, P_r is Power at the receiving antenna, P_t is the output power of the transmitter antenna, G_t is the gain of the transmitter antenna, G_r is the gain of the receiver antenna, λ is wavelength and R is distance between the antennas. Fig. 2.0.5 shows an overview of the RF spectrum of normalized power densities in close vicinity to an antenna site of different ambient sources [47]. It should be

17

noted that because cellular signals are transmitted at higher frequencies, there is a greater available power density. Moreover, their increased power densities caused by the daily growth in cellular subscribers and deployment of more GMS towers to improve their network coverage make them a desirable ambient source for energy harvesting.
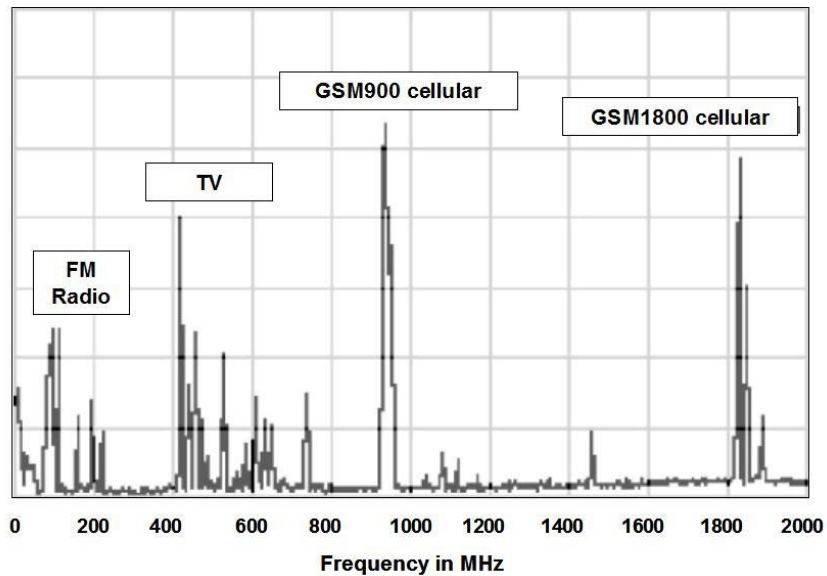
Fig. 2.0.5 An overview of the RF spectrum of normalized power densities in close vicinity to an antenna site of different ambient sources [47].

The available power level (P_{RX}) at the receiving antenna of the RF energy harvesting systems is critical for the functioning of the harvesting system. The RF-DC converter shown in Fig. 2.0.4 generally uses MOSFET (Metal Oxide Semiconductor Fiel Effect Transistor) diodes (MOS diodes) to perform rectification. The MOSFETs require a minimum voltage set-up by their threshold voltage (V_{TH}) before they can conduct current. If the available power is too low to overcome this threshold voltage requirement of the RF-DC converter, the system will fail to start. Generally, to achieve 1 V DC output from a CMOS RF-rectifier, −22 dBm to −14 dBm P_{RX} is required, and to achieve a power conversion efficiency (PCE) of more than 70%, P_{RX} should be above -10 dBm [48]. Several studies have conducted measurements of mobile phone power output in various scenarios, including urban and rural areas. A survey was conducted to determine the expected

18

power density levels at 25-100 meters distance from the GSM base station [49]. RF power density was found to be between 0.01-0.1 $\mu W/cm^2$ (around -30 to -20 dBm). Another survey measured the ambient RF energy at different locations in public/private, indoor/outdoor, rural/urban, and cell phone frequency bands (824-960MHz, 1710-2170MHz) and unlicensed industrial, scientific, and medical (ISM) devices (2.4-2.5GHz, 5.150-5.875GHz). According to the survey, up to 37% and 11% of the locations can reach a minimum peak available power of -30dBm and -20dBm, respectively. It was concluded that the RF energy at the measurement sites in general is either too low or too irregular to be useful for energy harvesting.

Dedicated RF Energy Sources to Improve Reliability

Placing a dedicated powerful RF energy source in the wireless sensor network is a promising and simple solution in providing energy to the WSNs without having any effect on their maintenance requirements. A dedicated RF energy will improve the reliability of the WSN and the increased power density will boost the power conversion efficiency of the energy harvester [48]. The license-free Industrial, Scientific, and Medical (ISM) frequency bands are a preferred choice for dedicated RF harvesting applications since they allow high EIRP Effective Isotropic Radiated Power (EIRP). The Federal Communications Commission (FCC) of the United States has set a maximum 4W (36 dBm) EIRP limit for both the 915 MHz and 2.44 GHz ISM bands [50]. A practical estimate of the transmission distance can be made using (2) choosing a reasonable transmitter gain of 8 dBi, EIRP (36 dBm), and 915MHz transmission frequency. In this case, an energy harvester coupled with a simple patch antenna (with a receiving gain of 2.5 dBi) can achieve 1V DC output at 35 meters from the RF energy source. Placing the RF energy source placed at the center of this network can provide line-of-sight coverage of about 3848 m^2.

2.2 Comparison of the RF Approach with Other Techniques in Terms of Scalability, Efficiency, Suitability, and Production Cost for the Proposed WSN Application

The choice of energy harvesting technique is influenced by the deployment scale, power requirements, application, and particular environmental conditions. As discussed in the previous section, each of the energy harvesting techniques, RF, solar, thermal, and vibrational, offers challenges as well as benefits and drawbacks. Based on the discussion a choice can be made taking the scalability, efficiency, and suitability of Wireless Sensor Network applications into consideration.

Scalability

RF energy harvesting systems can be highly scalable, allowing multiple devices to harvest energy simultaneously from a high-power dedicated RF source. This scalability is beneficial for large-scale WSN deployments. While solar panels are scalable, their suitability for certain environments may be limited to areas with better sunlight. The scalability of thermal energy harvesting highly depends upon the presence of notable temperature differences. For some industrial applications, vibration energy harvesting is a viable solution because it can be scaled up in settings where mechanical vibrations occur continuously.

Efficiency

RF energy harvesting can be highly efficient, especially in environments with a dedicated reliable RF energy source. Efficiency can be optimized with proper antenna design and matching circuits, ensuring a reliable harvesting technique. In well-lit areas, solar energy harvesting is highly efficient. However, the efficiency drops on cloudy days or in partially shaded areas, which reduces its dependability. It is possible to harvest thermal energy from temperature differences effectively, but efficient harvesting requires a greater temperature gradient which is not practically available

in our targeted application. Vibration harvesting is an efficient technique in high-vibration areas like industrial environments, however, outdoor environments are not an efficient source of energy for its implementation.

Suitability

RF energy harvesting is suitable for WSNs in both indoor and outdoor areas with wireless communication infrastructure, providing intermittent bursts of power for sensor nodes. It's ideal for applications requiring periodic data transmission. Solar energy harvesting works well for agricultural and environmental monitoring applications in outdoor WSNs that have access to sunlight. Thermal energy harvesting provides continuous low-power energy and is appropriate for only specific applications with stable temperature differentials, such as HVAC systems or industrial processes. When used in indoor industrial settings where machinery vibrations are regular, vibration energy harvesting provides a dependable power source for sensors.

Production Cost

RF harvesting antennas can be fabricated with low-cost setups and can easily be integrated with electronics systems potentially reducing their production cost much lower than photovoltaic cells. Specific materials and complex designs are frequently used in thermal and vibration energy harvesters respectively, which could raise their production costs, particularly for high-efficiency systems.

Considering the discussion presented in the previous section, it is decided that the most suitable energy harvesting choice for the intended WSN application is RF energy harvesting. A summary of the power density, benefits, and drawbacks of the discussed harvesting methods is given in Table 1.

Table 1 Summar of the available power sources for energy harvesting

Sources	Power density	Harvesting Tech	Advantages	Disadvantages
Solar	~10 mW/cm^2	Photovoltaic	High Power density Mature	Not always available Expensive
Vibration	15 µW	Piezoelectric Magnetoelectric	Implantable High efficiency	Not always available Material limitation
Thermal	Human: 146 nW (chest area) Industrial: 4.5 µW/cm^2	Thermoelectric	High power density Implantable	Not always available Excess heat
RF	GSM: 0.1 µW/cm^2	Antenna	Always available Implantable	Low Power density

2.3 ISM Band for RF-Powered WSN

Implementation of an autonomous, power-efficient, and low-cost RF-powered WSN poses several design challenges. One of the most important design challenges is the availability of stable frequency carrier for wireless communication. On-chip local oscillators (LO) are commonly used for RF carrier generation in various applications [51], [52]. However, they may not be suitable for WSNs because the power requirements of such oscillator (LO) can exceed the total power budget of the system [53]. Additionally, On-chip oscillators, such as ring oscillators, may not be stable enough for accurate and reliable operation of WSNs where power constraints may limit the use of error compensation circuitry [54]. Another low-power choice is RFID (Radio Frequency

Identification) which uses backscattering to reflect the incoming RF signal to encode information without generating an RF carrier signal. However, their reliance on the reflection of ambient RF signals inherently limits the communication range [55]. This limitation makes it challenging to establish reliable and robust communication links over longer distances, which is often required in WSNs deployed in large areas. Another drawback of RFID backscattering is its susceptibility to self-jamming because of transmission in the same frequency range[55], [56]. This can result in reduced communication performance. [57] avoids generating the RF carrier signal by using the incoming 915-MHz RF signal and extracts a 457.5-MHz carrier by frequency division using a true-single-phase-clock divider with low power consumption and a small die area. Another work [58] upconvert an incoming 915Mhz RF signal and synthesize a 2.4 GHz carrier signal for communication, this frequency reuse makes the communication architecture both power and area efficient and can easily be implemented in the ISM band. The frequency reuse is the suitable choice for our application where we can use one frequency band for power transfer from the dedicated RF energy source and use it to generate the other frequency band for the wireless data transmission from the sensor node. Several factors can be used to establish a comparison between the energy transfer performance of both the frequency bands, one of the important performance factors is Free Space Path Loss (FSPL). FSPL refers to the attenuation or reduction in power density (signal strength) of an electromagnetic wave as it travels through free space (air or a vacuum) over a specific distance. This attenuation occurs naturally as the signal spreads in space, therefore it's a crucial factor in determining the effective range of wireless energy transfer performance without the need to consider specific antennas or environmental conditions. The FSPL can be calculated using the following formula:

$$FSPL\ (dB) = \ 20\ log_{10}\ (d) + 20\ log_{10}\ (f) + 20\ log_{10}\ (\frac{4\pi}{c}) - G_t - G_r \qquad (3)$$

Where, d is the distance between the transmitter and the receiver in meters, f is the frequency of the signal in hertz, c is the speed of light in meters per second (3×10^8 m/s), G_t is the gain of the transmitter antenna in decibels (dB) and G_r is the gain of the receiver antenna in decibels (dB).
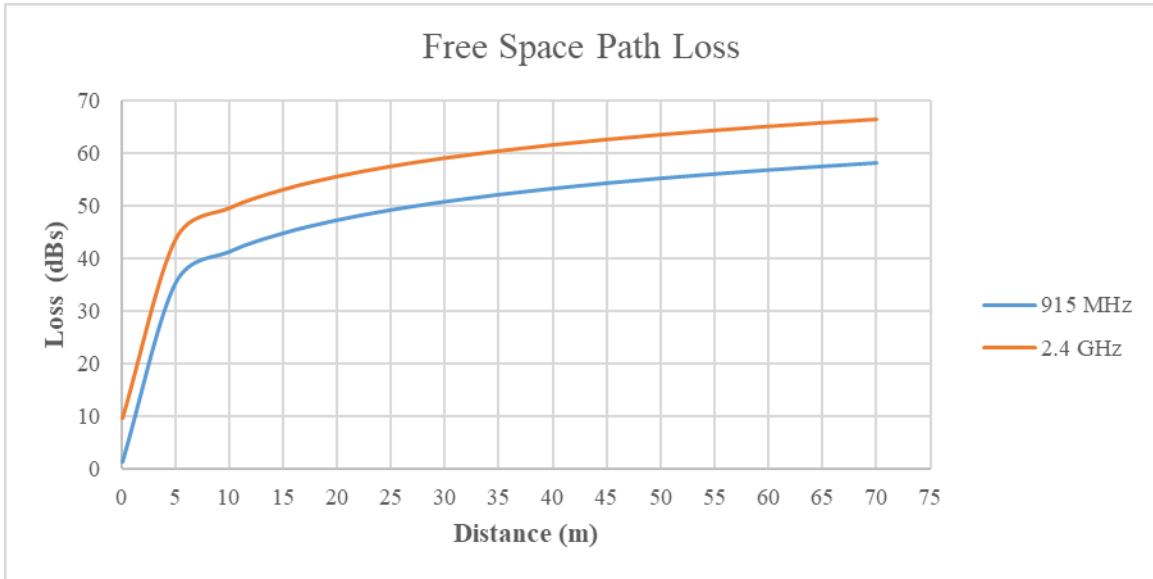
Fig. 2.0.6 Free Space Path Loss at 915 MHz and 2.4 GHz

A practical estimate of signal loss at 30 meters can be calculated by considering a transmitter gain of 8 dB and a receiver gain of 2.5 dB. If the RF energy source operates at 915 MHz, the Free Space Path Loss (FSPL) is 50.7 dB. Conversely, for an operating frequency of 2.4 GHz, the FSPL is 59 dB. Hence, under the same conditions, the free space path loss for 915 MHz is 8.3 dB less than that for 2.4 GHz. This indicates that energy signals experience more significant attenuation at 2.4 GHz, adversely affecting energy transfer performance. Fig. 2.0.6 shows the plot of FSPL vs distance for the two frequency bands. Another important factor to consider is the size of the receiving antenna. A larger antenna possesses a larger capture area, allowing it to intercept more energy from the surrounding electromagnetic field. Therefore, the lower frequency band of 915 MHz having a larger antenna size is more suitable for efficient energy capture. Additionally, lower frequencies generally have a reduced data-carrying capacity hence high frequency band of 2.4 GHz is a more suitable choice for wireless data transfer from the WSN. Furthermore, it is worth

24

noting that the Federal Communications Commission (FCC) sets the allowable RF sources power emissions in the 915 MHz band to be as high as 4 watts, which greatly benefits the range of energy transfer in our specific application.

2.4 Conclusion

Different energy harvesting methods were discussed including photovoltaic, vibrational thermal, and radiofrequency (RF). Photovoltaic and vibrational energy harvesting can provide high power in specific applications indoor and outdoor applications, but they are not suitable for the intended WSN application. In addition, the power available from ambient RF and thermal sources is deemed insufficient, unreliable, and unsuitable for the intended use. However, the RF energy harvesting technique can easily utilize a dedicated high-power RF energy source (working in the ISM band) for a variety of applications and environments. RF energy harvesters can be easily integrated into the electronics making their mass production cost effective. Moreover, circuit design techniques can be studied and applied to improve the overall range, efficiency, and sensitivity of the proposed WSN.

CHAPTER 3 SYSTEM LEVEL DESCRIPTION OF THE DESIGN

3.1 System Level Block Diagram

The system-level block diagram of the proposed WSN is shown in Fig. 3.0.1. It is assumed that a dedicated 915 MHz RF energy source is present in the vicinity of the WSN. The sensor node captures RF energy through an antenna tuned at 915 MHz. The antenna converts the electromagnetic energy into electrical energy and supplies it to an RF rectifier through a matching network. The RF rectifier along with the antenna forms the energy harvesting block of the system and provides DC power in its output. The DC power is stored on an off-chip capacitor. A power management block continuously monitors the DC voltage of the storage capacitor until enough power has been gathered to wake up the sensor and the wireless data transmission block.
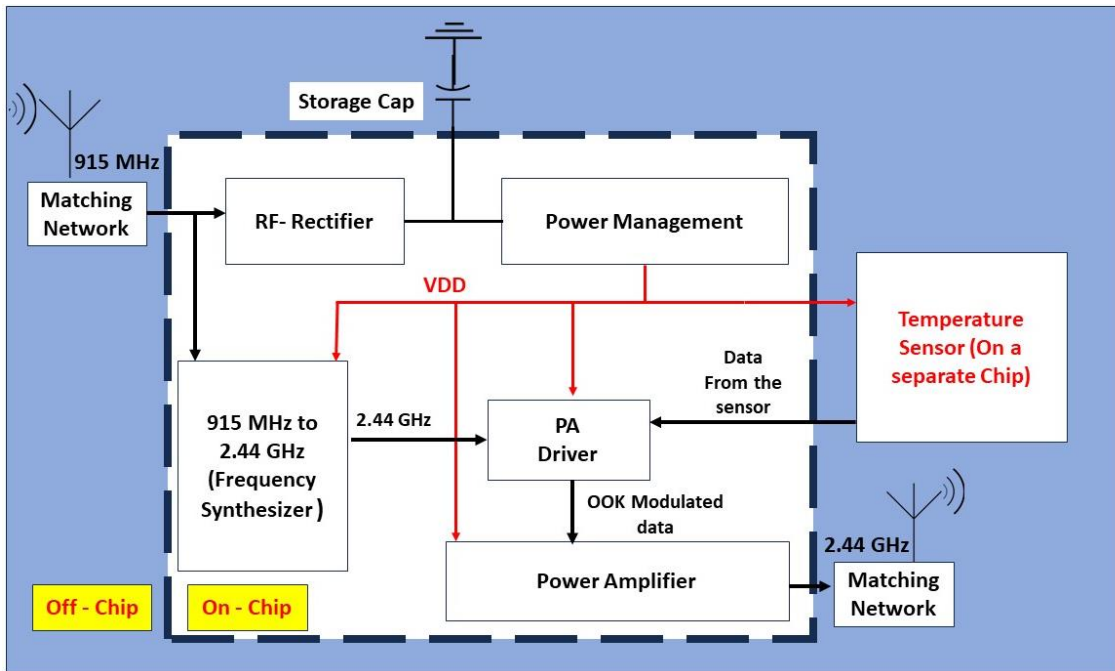
Fig. 3.0.1 System Level Block Diagram of the Proposed WSN

The wireless data transmission block consists of a frequency synthesizer, a Power Amplifier (PA), and the PA driver (OOK modulator). Frequency synthesizer uses the 915 MHz signal from the antenna as a reference input and upconverts it to 2.44 GHz which serves as the carrier for wireless

data transmission. The temperature sensor is designed on a separate chip which produces serial temperature data in its output. The PA-Driver takes the serial data from the temperature sensor and modulates it on the 2.44 GHz carrier using the On-Off keying (OOK) modulation technique. Finally, the modulated signal is transmitted through a PA and a 2.44 GHz antenna (off-chip). The wireless data transmission drains energy from the storage capacitor and when the voltage level on the storage capacitor drops below a threshold level, the power management block forces the transmission circuit to sleep until enough power is available on the storage capacitor.

3.2 RF- Energy Harvester

The performance of the energy harvester block is of great significance for the functionality of the WSN, therefore it is necessary to optimize the building block of the energy harvest to achieve a good performance in terms of efficiency, sensitivity, and size. The block diagram of the energy harvester is shown in Fig. 3.0.2.
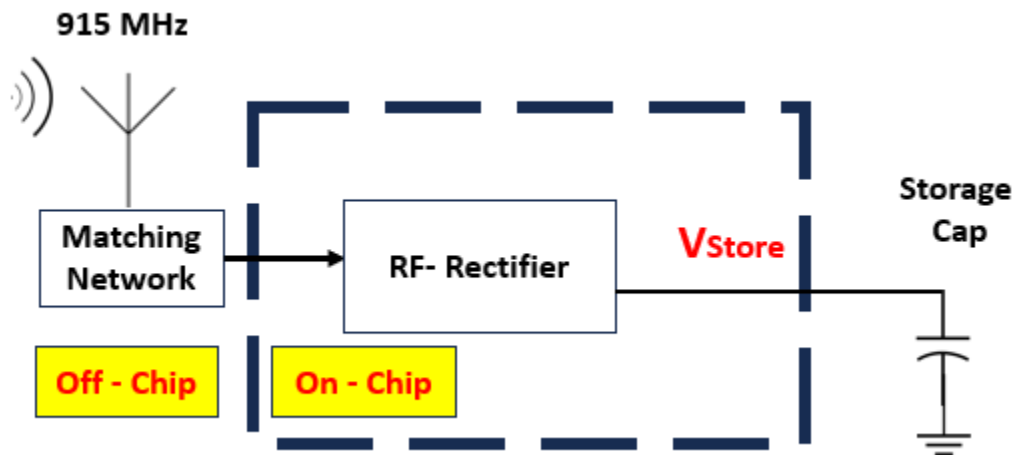
Fig. 3.0.2 RF Energy Harvesting Circuit

The antenna serves as an interface between the electromagnetic radiation in the environment and the electronics of the energy harvester. The choice of the 915 MHz ISM band enables the implementation of a moderate-sized antenna with a planar structure such as a patch antenna. Since

the available power that can be delivered to the load from the antenna is directly proportional to the effective area of the antenna, more energy can be captured from the environment. Additionally, patch antennas can be printed directly onto a substrate, making them easy and cost-effective to manufacture. They can be integrated into the PCB (Printed Circuit Board) without adding significant bulk or complexity to the overall system. Matching the impedance between the antenna and rectifier is crucial for efficient energy harvesting, an impedance-matching network ensures maximum power transfer between the antenna and the RF rectifier. Moreover, the LC combination in the matching network can benefit from the resonance to provide a passive voltage boost to the incoming RF signal [59], the voltage boost can significantly improve the sensitivity and range of the energy harvesting circuit. In our system, we opted to incorporate an external impedance-matching network utilizing off-the-shelf discrete inductors and capacitors. This external network allows for calibration, and the availability of High-Q inductors and capacitors greatly enhances passive voltage boosting, implementing a High-Q resonator.

The RF-rectifier also plays an important role in the efficient implementation of the energy harvester. The rectifier converts the RF signal into a DC voltage using MOS diodes and supplies it to the storage capacitor. In addition to rectification, the rectifier can be used to double the received voltages by strategically placing capacitors between the MOS diodes. These capacitors store the charge generated during the positive half-cycles of the RF signal. During the negative half-cycle, the stored charge is released, effectively doubling the voltage across the capacitors. By connecting multiple stages of these diodes and capacitors in series, the voltage across the storage capacitor can be multiplied to be several times higher than the input voltage. The number of stages can be optimized to attain the maximum voltage multiplication factor with the fewest stages

possible. The design details and simulation of the energy harvesting block are presented in Chapter 4.

3.3 Power Management Block

The power management block plays a significant role in ensuring efficient utilization of harvested energy. It continuously monitors and regulates the voltage of the storage capacitor, which directly impacts the performance and functionality of the entire system. It prevents under-voltage situations that could lead to system malfunctions or data loss. It ensures that wireless communication modules, such as the frequency synthesizer and the power amplifier receive a stable and optimal power supply. This stability is vital for reliable data transmission, minimizing transmission errors, and enhancing the overall efficiency of the wireless communication process. Additionally, the power management circuit also controls the power supply to the temperature sensor of the WSN. By regulating the power supply to the sensor, the power management circuit ensures accurate and consistent temperature readings. This accuracy is essential for making informed decisions based on the environmental conditions monitored by the WSN.
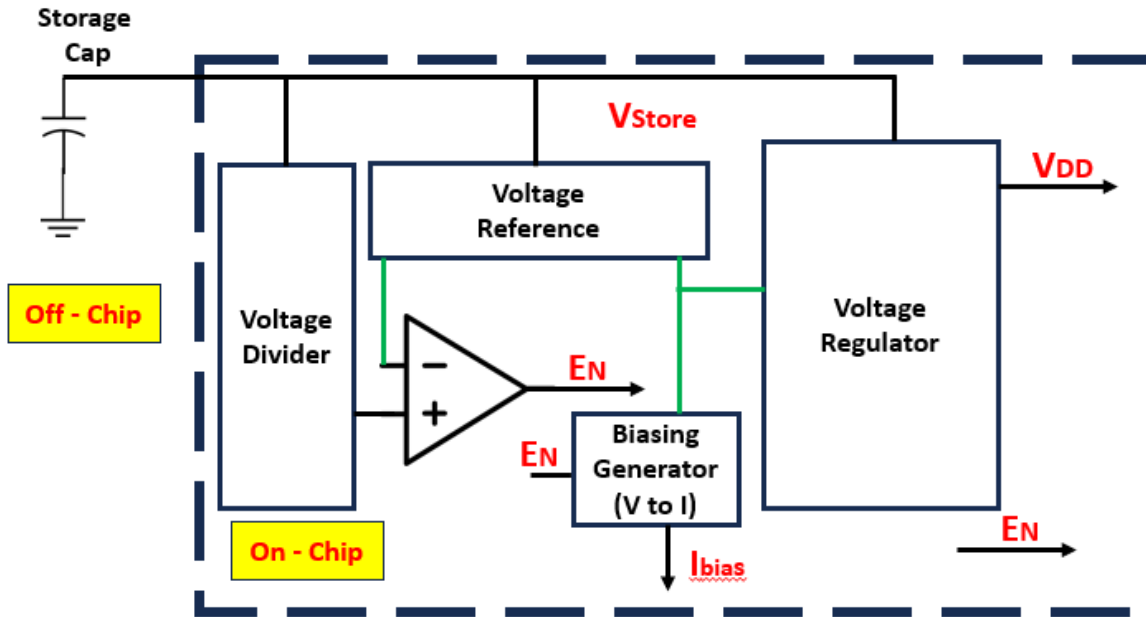
Fig. 3.0.3 The Power Management block.

As shown in Fig. 3.0.3 the power management circuit houses a voltage reference circuit, a bias current generator, and a voltage regulator circuit. Because the power management circuit operates continuously, its internal power efficiency is essential for the overall power efficiency of the WSN implementation. Hence, it's necessary to design each component within the power management circuit with minimal power consumption. The power management circuit monitors the voltage level of the storage capacitor throughout the energy harvesting phase. When sufficient voltage (V_H) is detected on the storage capacitor, the WSN transitions into the data transmission phase. The temperature sensor and wireless communication module wake up during this phase and drain power from the storage capacitor until its voltage drops to voltage (V_L). These cycles, as depicted in Fig. 3.0.4, repeat regularly. The frequency of this cycle depends on several factors like the size of the storage capacitor, the energy available for harvesting in the environment, and the power consumption of the sensor and wireless data transmission block.
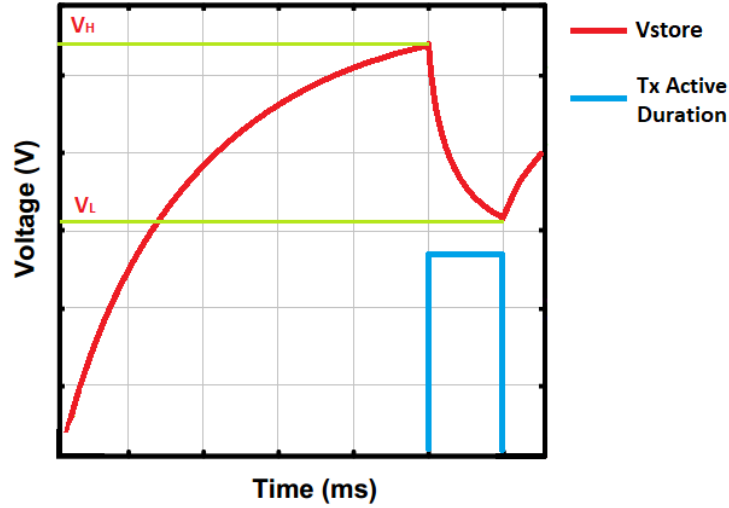
Fig. 3.0.4 Storage capacitor Voltage vs Time during the energy harvesting and data transmission phases of the WSN.

The regulation of the supply voltage V_{DD} and the bias current generation depends on the performance of the voltage reference circuit. The voltage reference circuit must provide a stable output voltage when the storage capacitor discharges from V_H and V_L, therefore these voltage levels are determined during the design of the voltage reference circuit. The design details of the power management circuit are provided in Chapter 4.

The size of the storage capacitor can be calculated using the formula:

$$P_{supplied} = \frac{E_{supplied}}{T_{active}} \tag{4}$$

Where $P_{supplied}$ is the power supplied to WSN, $E_{supplied}$ is the energy supplied by the storage capacitor and T_{active} is the time for which the WSN actively draws current from the storage capacitor. $E_{supplied}$ can also be represented as the stored energy difference that's created by discharging storage capacitor from the voltage level V_H to V_L as shown below.

$$E_{supplied} = E_H - E_L \tag{5}$$
$$E_{supplied} = \frac{1}{2}C_{Store}V_H^2 - \frac{1}{2}C_{Store}V_L^2 \tag{6}$$

31

Substitution (4) in the above equation and solving for Cstore:

$$P_{supplied} = \frac{C_{Store}}{2T_{active}}(V_H^2 - V_L^2) \tag{7}$$

$$C_{Store} = \frac{P_{supplied} \times 2T_{active}}{V_H^2 - V_L^2} \tag{8}$$

Thus, the value of storage capacitor can be estimated after determining the total power consumption of the WSN along with the required active time. The active time will depend on the wireless data transfer size and the speed of transfer in Mbps. (8) will be revisited in the final integration chapter.

3.4 Temperature Sensor

The temperature sensor is fabricated on a separate chip and its power supply is regulated by the WSN. This separate fabrication allows the WSN to be integrated with various sensor types if needed. Therefore, it is essential to create a sensor interface that is simple and compatible with the WSN. Because of the WSN's constrained power resources, it is crucial to optimize the temperature sensor design for minimal power consumption, ensuring prolonged operation of the WSN. Fig. 3.0.5 illustrates a simplified block diagram of the temperature sensor, while comprehensive design details are provided in Chapter 6.
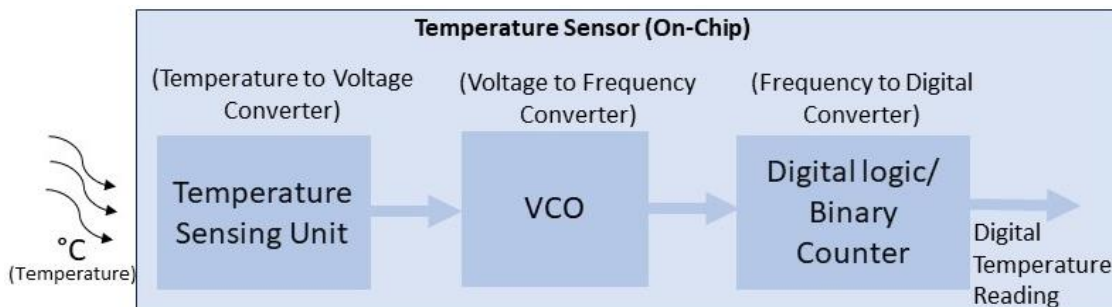
Fig. 3.0.5 Simple Block diagram of the proposed temperature block.

3.5 Wireless Data Transmission Module

As established in the earlier discussion, for a reliable operation, the WSN is powered by the signal from the RF energy source operating in 915 MHz ISM band. The RF signal received by the WSN is reused to generate the transmitter's 2.4 GHz RF carrier. To accomplish this frequency conversion, the 915 MHz signal is initially divided by 3, resulting in 305 MHz. Subsequently, this frequency is multiplied by 8 through three stages of 2x multiplication, yielding an output of 2.44 GHz (305 MHz x 8 = 2.44 GHz). Fig. 3.0.6 depicts the block diagram of the wireless data transmission module. The 915 MHz signal received from the antenna lacks the strength to drive the frequency divider directly. Hence, an RF signal conditioning block is employed to buffer the signal. This signal conditioning block interfaces with the antenna-rectifier interface and needs to be optimized to minimize its impact on the efficiency of the energy harvesting circuit. Following the frequency division, the signal serves as the reference frequency input for the delay-locked loop (DLL) based 8x frequency multiplier.
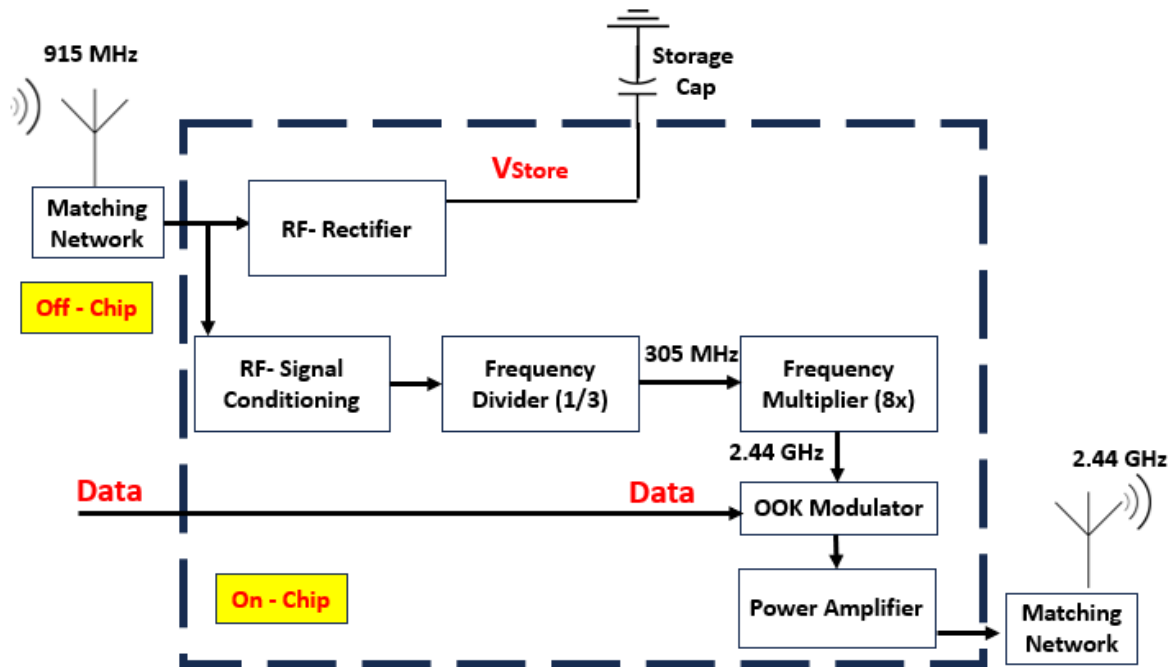
Fig. 3.0.6 Wireless Data Transmission Module

The power amplifier (PA) stands out as the most power-hungry component in the WSN. Due to limited optimization possibilities, designing it for high efficiency presents a significant challenge. The PA driver employs On-Off Keying (OOK) to encode sensor data and activates the PA for transmission only when the temperature sensor signals the temperature data conversion flag. This approach minimizes the PA's active time, conserving power. The design details of the wireless data transmission module are discussed in Chapter 5.

3.6 Conclusion

In this chapter, we presented the description of the overall system along with the challenges and requirements associated with the implementation of various components of the system. It establishes an initial understanding of the correlation between the storage capacitor, WSN power consumption, and the activity cycle of the WSN. The chapter emphasizes the significance of power management in prolonging the operation of WSN and ensuring efficient energy usage. At the end the frequency conversion scheme employing the frequency divider and Delay-Locked Loop to generate the transmission carrier is discussed.

CHAPTER 4 ENERGY HARVESTER AND POWER MANAGEMENT DESIGN

4.1 Energy Harvester Design

As discussed in the previous chapter the energy harvester design comprises a receiving antenna, impedance impedance-matching network, and the RF rectifier. To keep the focus of this chapter on the circuit design aspects of the RF rectifier, the fundamental theory of the antenna parameters, the design details of the antenna, and the choice of the impedance matching network are discussed in Appendix -A. Throughout the work the impedance matching networks are calculated using an online calculator [52]. The physical design of the patch antenna is shown in Fig. 4.0.1. The dimension of the patch is 73 mm x 73 mm. The antenna is designed to have an input impedance of 50 Ω and an operating frequency of 915 MHz. The simulation of the radiation pattern and S11 return loss measurement of the antenna is shown in Fig. 4.0.2. The performance features are summarized in Table 2.
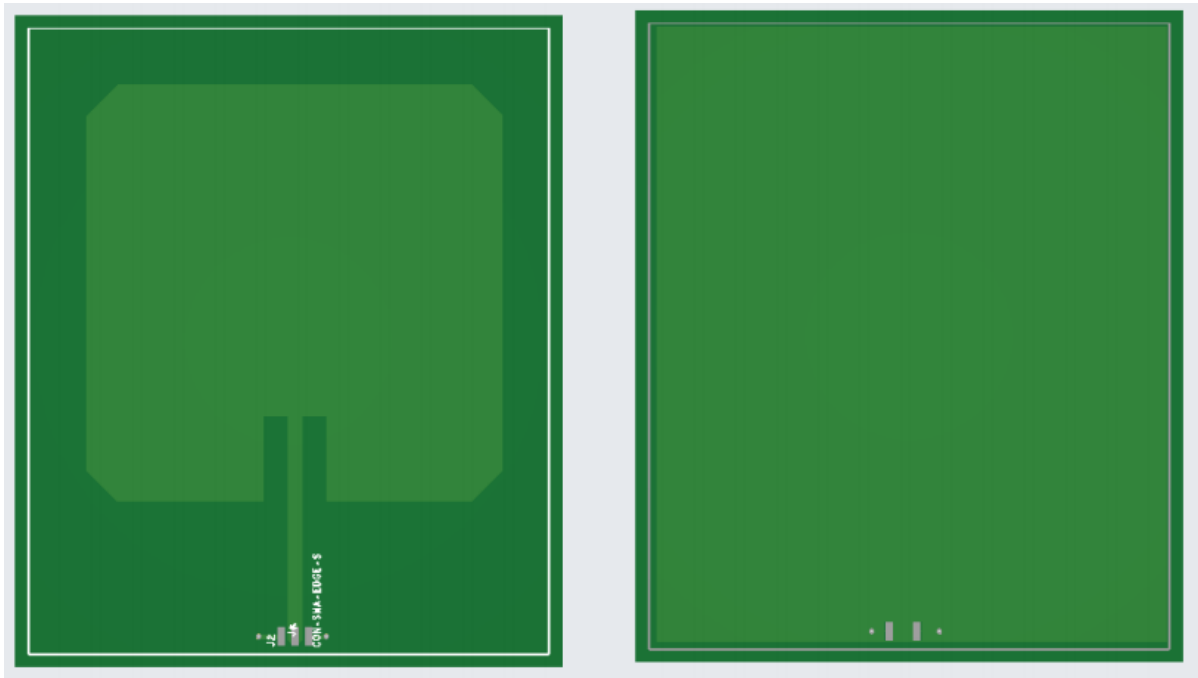
Fig. 4.0.1 Physical Design of the Patch Antenna.
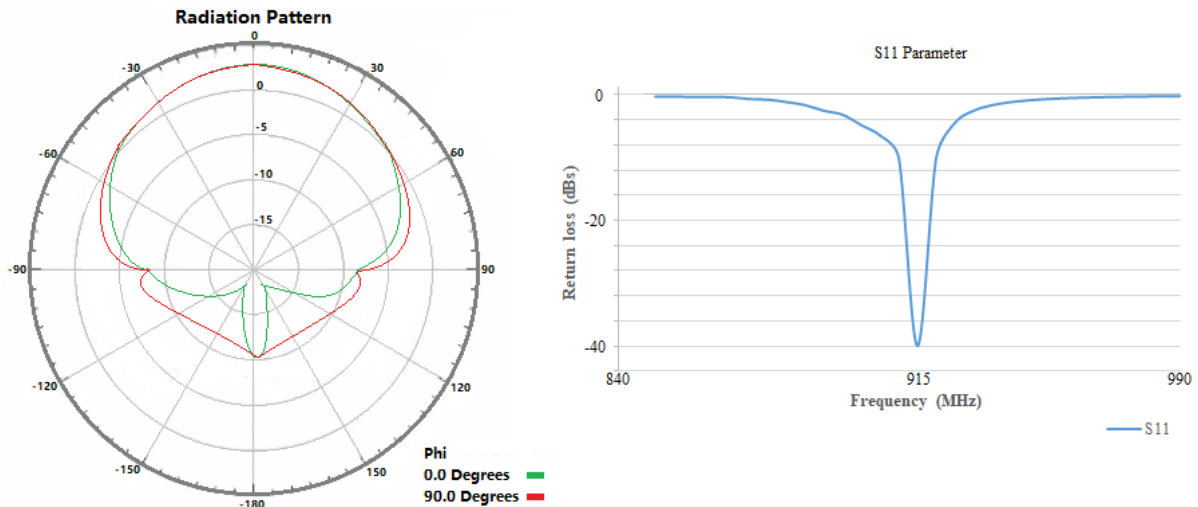
Fig. 4.0.2 Simulated Radiation Pattern of the Patch antenna (Lef). Measured S11 Return loss Parameter of the Antenna in dBs (Right).

Table 2 Simulated Performance features of the 915 Patch Antenna

Center Frequency	915 MHz
Impedance	50 Ω
VSWR	1.03
Return Loss (S11)	-40 dB
Bandwidth	7 MHz
Gain	3.4 dBi
Polarization	Vertical

Rectifier Design

The core component of the RF energy harvester is the RF rectifier, it converts the RF signal from the antenna into a direct current (DC) signal, called rectification. The efficiency of this conversion significantly influences the overall power efficiency of the WSN. Another important factor is the sensitivity of the rectifier, as it directly impacts the power transfer range [58]. To achieve rectification, an RF-DC employs a nonlinear element (diode). In CMOS technology, this nonlinear element can be realized using diode-connected MOS transistors (where the gate is connected to the drain). But the Vth of the utilized MOSFET can severely limit the maximum power transfer.

As we have established earlier the incoming RF signal have low amplitude (-20 to -16 dBm or 0.06 to 0.1 V_p), so boosting the output voltage through a voltage multiplier is necessary to obtain a DC voltage suitable for powering the circuits in the WSN. Various rectifier and voltage multiplier topologies are available, each with its own set of advantages and disadvantages. Our initial approach involves the use of the conventional Dickson voltage multiplier, widely employed in energy harvesting applications due to its good trade-off between simplicity and performance. The Dickson voltage multiplier, introduced in 1976 [60], is a modified version of the Cockcroft–Walton multiplier and is chosen in our work for its suitability in energy harvesting contexts. Using the Dickson voltage multiplier, a sensitivity of -19 dBm at 800 MHz is obtained using the 40nm CMOS process [61]. A conventional single-stage Dickson voltage rectifier using diode-connected MOS is shown in Fig. 4.0.3. The rectifier operates by receiving an AC signal at its input. In the first negative cycle of the input signal, C_1 is charged through the first diode-connected NMOS (D_1), while D_2 remains reverse-biased and turned off. During the subsequent positive cycle, D_1 is turned off, allowing D_2 to charge C_2 using the stored charge in C_1 and the incoming positive cycle. This process effectively amplifies the output voltage.
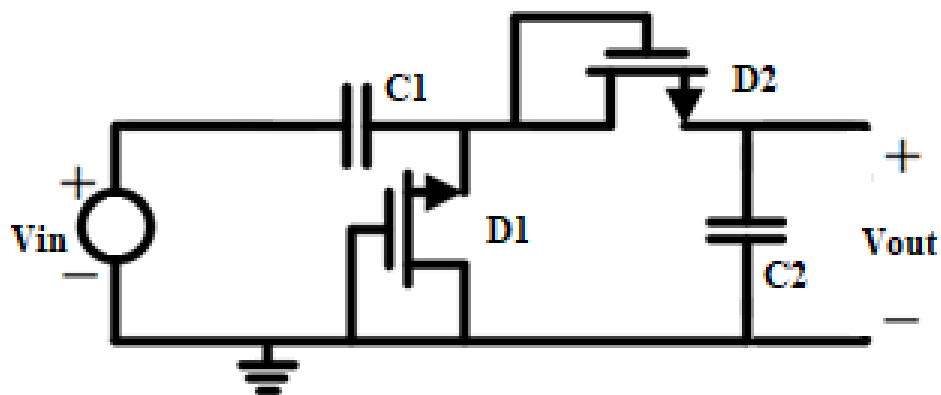
Fig. 4.0.3 A conventional single-stage Dickson voltage rectifier

The WSN circuits including the RF-rectifier are implemented in 22-nm FD-SOI (Fully-Depleted Silicon-On-Insulator) process technology. FD-SOI transistor technology delivers energy

efficiency, low parasitic capacitances, and low power operation as compared to the transistor fabricated over bulk silicon [62]. In conventional bulk silicon technology, a large portion of the current in an OFF-transistor results from the leakage from junction areas, such as the bottom of source-drain areas, which are non-critical to device function. As seen in Fig. 4.0.4, in the SOI technology the leakage current in an OFF transistor is due only to the vertical area at the drain/channel junction [63]. This is only a fraction of the total source-drain area that could cause leakage current in a bulk transistor of corresponding geometry. All these characteristics are desirable for the power-efficient implementation of RF rectifiers.
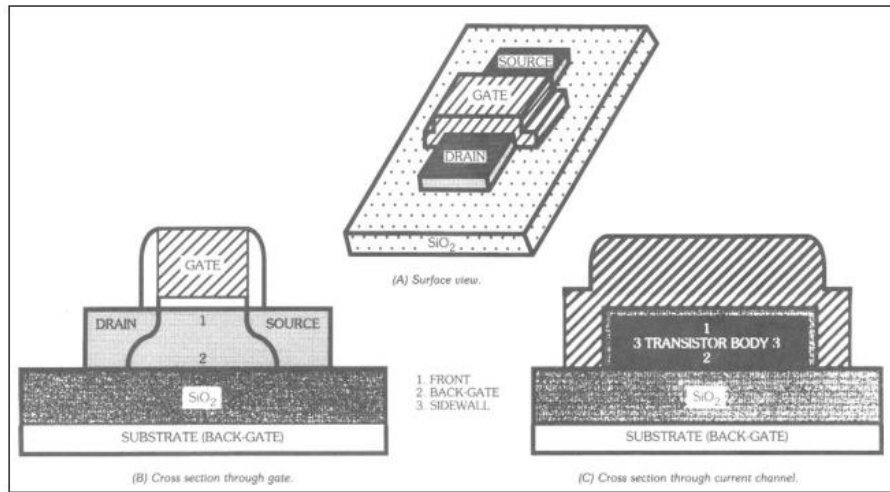
Fig. 4.0.4 Transistor view in SOI Technology [63]

The performance of a rectifier is mainly evaluated using the two performance parameters: DC output voltage and RF-DC power conversion efficiency (PCE). Maximum output voltage of an unloaded n stages Dickson multiplier is estimated by (9)

$$V_{out} = 2n\,(V_{RF,peak} - V_{th}) \tag{9}$$

Where $V_{RF,\text{the peak}}$ is the peak input RF voltage, while Vth is the threshold voltage of the transistor used. The power conversion efficiency (PCE) of an RF rectifier is a measure of how effectively the rectifier converts the received radio frequency (RF) signal into usable direct current (DC)

38

power. It quantifies the ratio of the DC power output to the RF power input, expressed as a percentage. The power conversion efficiency can be calculated using the following formula (10):

$$PCE(\%) = \frac{P_{DC,out}}{P_{RF,in}} = \frac{V_{out}^2}{R_{Load} \cdot P_{RF,in}} \qquad (10)$$

Where, $P_{DC,out,}$ and $P_{RF\ in}$ represent the DC output power and the absolute RF input power respectively. A higher efficiency means that a larger percentage of the received RF power is successfully converted into usable electrical power, leading to more effective energy harvesting systems. It can be noted from (9) and (10) that PCE can be improved by decreasing threshold voltage V_{th}, an important feature of SOI technology is the back gate biasing that provides control over the threshold voltage of the transistor. As reported in [64], when a positive bias is applied on the back gate of an SOI transistor, the V_{th} decreases. As seen in (9) a small V_{th} will result in higher DC output voltage. The decrease in V_{th} will also result in a smaller voltage drop across diodes, improving the sensitivity of the rectifier. However, it is observed [65] that forward biasing the back gate results in increased leakage current that will compromise the efficiency of the rectifier. Dynamic back gate polarization [64] controls this increase in leakage currents when the transistors are OFF and ensures a low V_{th} when they are turned ON. The modified Dickson voltage multiplier with dynamic back gate polarization is shown in Fig. 4.0.5 [64].
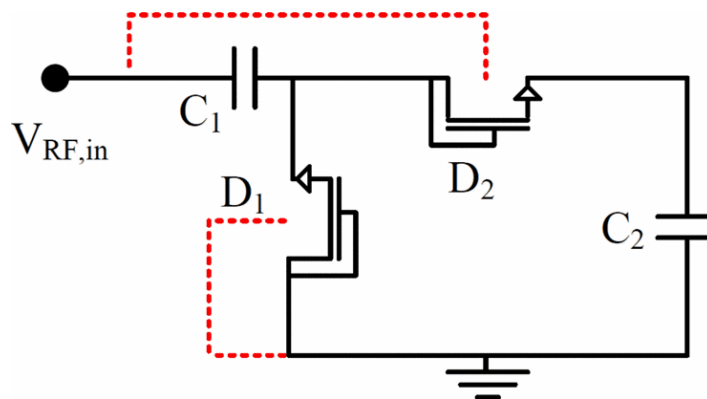
Fig. 4.0.5 Modified Dickson voltage multiplier with dynamic back gate polarization[64].

When a MOS diode is in the off state due to reverse biasing, a slight current flow through it because of reverse leakage, this leakage current increases as V_{DS} (drain-to-source voltage) rises in the off state. This current can discharge capacitor C_1 through D_1, reducing the charge transfer from C_1 to C_2. Consequently, this reduces the output voltage and decreases the power conversion efficiency. In our work, we propose the use of the ultra-low-power diode (ULPD) architecture, which was initially introduced in [66] using SOI CMOS technology. The aim is to enhance the Power Conversion Efficiency (PCE) of the RF rectifier by substituting the MOS diode with the ULPD. The circuit topology of this ULPD is depicted in Fig. 4.0.6. Originally designed for memory cell applications, this ULPD architecture can also be effectively applied in RF rectifiers.
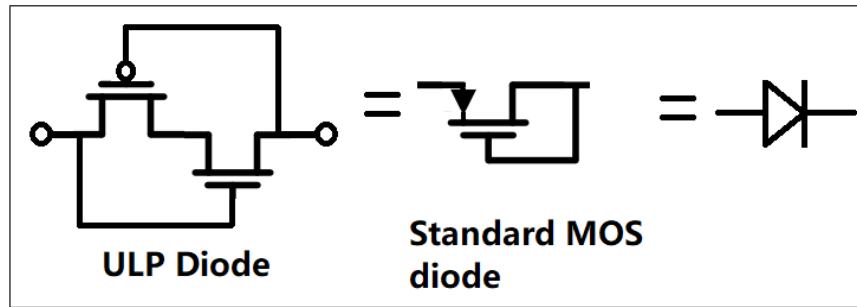
Fig. 4.0.6 Ultra-low power diode architecture

The current flow in the ULPD, both under reverse and forward bias conditions, can be approximated as equal by setting the ideality factor n to 1. This current can be mathematically expressed as:

$$I_{diode} = I_o \left(e^{\frac{V_{diode}}{V_t}} - e^{\frac{V_{diode}}{2V_t}} \right) \tag{11}$$

Where I_0 is the technology-related characteristic current and V_t is the thermal voltage. It can be analyzed from (11) that its forward characteristic is identical to conventional diode at room temperature for $V_{diode} > 4V_t$ (~100 mV). Whereas, during reverse biasing, the current rapidly decreases as $V_{GS,p}$ increases. To further analyze the improved performance, we simulated and compared the reverse leakage current of conventional MOS diode and ULPD in the Cadence

Virtuoso design suit. Fig. 4.0.7 shows the simulated I-V characteristics. The threshold voltage and the forward bias current of both the diodes are the same as discussed earlier. The leakage current at the reverse bias voltage 0f 0.5 V is approximately 1000 times smaller for the ULPD as compared to the conventional MOS diode.
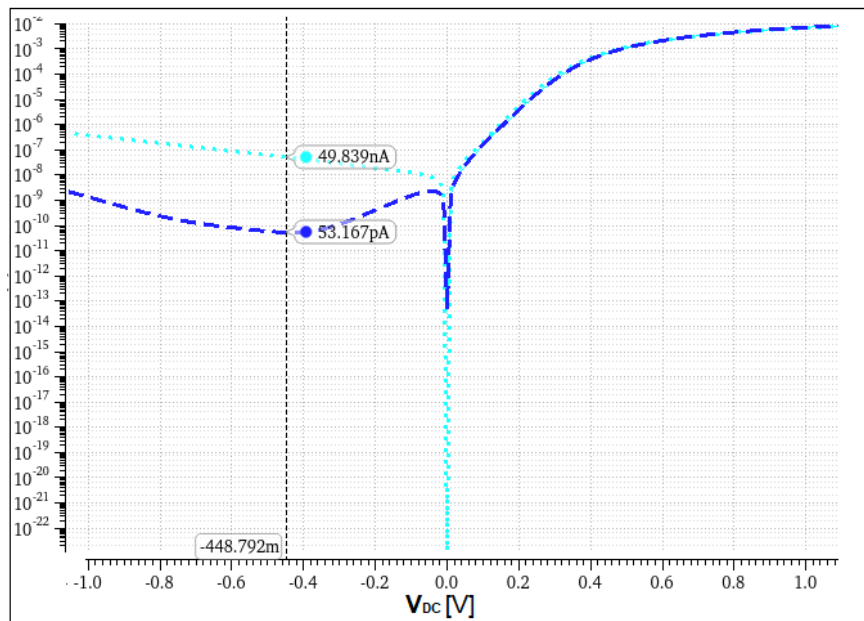
Fig. 4.0.7 Simulated I-V characteristics of conventional MOS diode vs ULPD.

For performance comparison two single-stage Dickson rectifiers were designed using conventional MOS and ULPD shown in Fig. 4.0.8. Dynamic back gate polarization was employed in both implementations to reduce V_{th}. Small coupling capacitors (C = 0.4 pF) are used to ensure a smaller chip area and faster charging time. Minimum transistor length is used while the width of the transistor is determined by analyzing the charging time for different widths. It was observed that increasing the width decreases the charging time, However, widths exceeding 10 μm provide minimal advantages due to the rise in internal parasitic capacitance, leading to slower charging. Therefore, an optimal width of 10 μm was selected for both circuits. After setting the capacitor and transistor size, the input impedance is analyzed and matched with the source to benefit from the resonance voltage boost effect as discussed earlier.
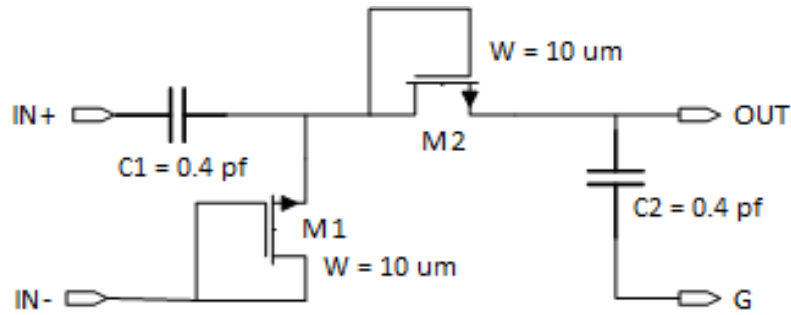
Fig. 4.0.8 Implemented Single-stage Dickson Voltage Multiplier (back game connection not shown)

Fig. 4.0.9 shows simulation of the two rectifiers showing a comparison of PCE and output voltage.

The ULPD achieves a maximum PCE of 90 % at -4 dBm while the conventional MOS diode implementation achieves a maximum PCE of 84 %. The PCE appears to degrade at higher input power levels because the higher reverse voltage will cause the diodes to leak more current during their OFF state. The output voltage is also shown for both rectifiers on the left axis. It is observed that ULPD achieves a higher output voltage due to its better PCE.
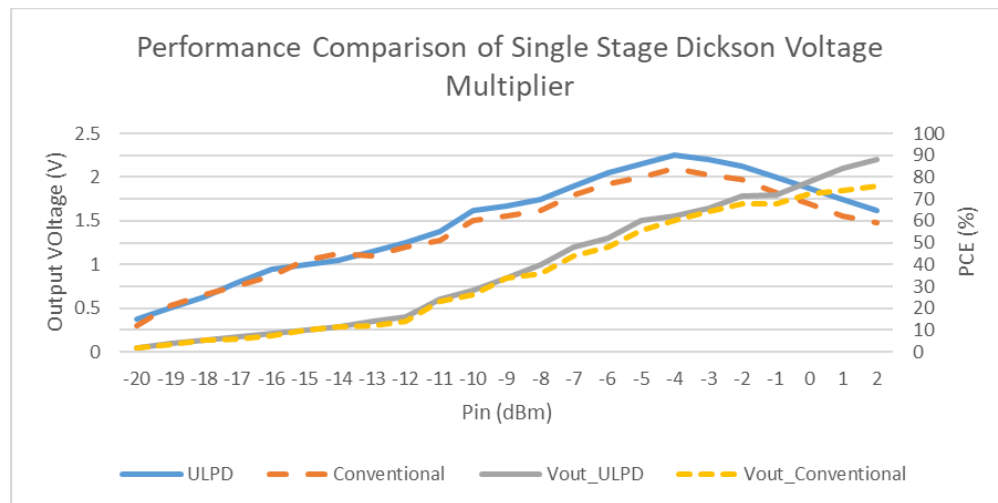
Fig. 4.0.9 Simulation of the two rectifiers showing a comparison of PCE and output voltage.

Note that V_{out} is only about 50 mV @ Pin = -20 dBm, which is not sufficient to power up the WSN.

A higher output voltage can be achieved by cascading several rectifying stages in series. For clarity only a 2-stage cascaded rectifier is shown in Fig. 4.0.10. It can be seen that the RF signal appears simultaneously at the input of all the cascaded stages, while the DC voltages add up in series to

42

yield a higher DC output. Cascading several stages increases the output voltage linearly at the expense of increasing the charging time of the output due to the increasing parasitic capacitance burden. We determined an optimal stage count (N) by simulating the rectifier with an increasing number of stages and analyzed the normalized charging time vs the output voltages @ Pin = -25 dBm. The targeted input power is decreased from -20 dBm to -25 dBm to account for antenna losses and decreased PCE (due to cascading effect).
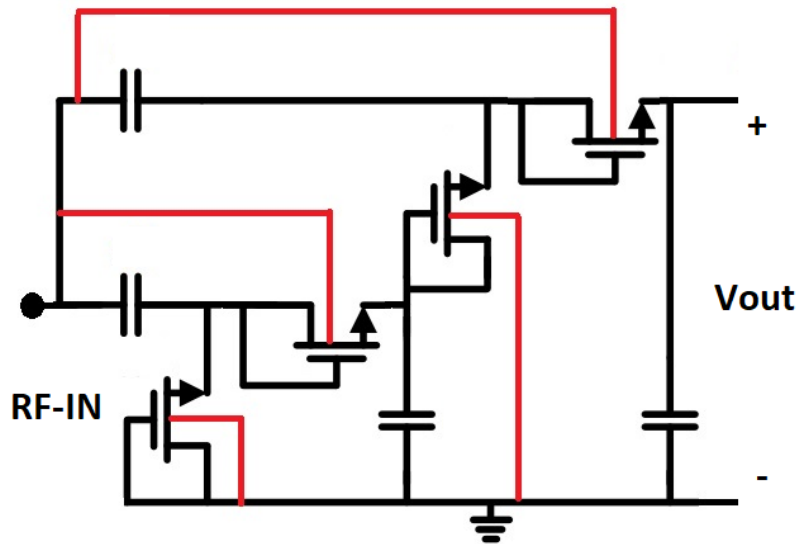
Fig. 4.0.10 A two-stage cascaded RF rectifier (backplate connections are shown in red).

Fig. 4.0.11 shows the normalized charge time and output voltages for N number of rectifier stages. A 500 nF storage capacitor is used for simulation purposes, and the final selection of the storage capacitor is addressed in the final integration chapter 7. With a rectifier having stages N=1, the charging time is approximately 10 ms, whereas N=15 stages result in about 8 seconds of charging time. In our work, a rectifier structure consisting of 10 stages is opted for generating 1.6 V with a charging time of 1.5 seconds at low power levels of -25 dBm. The parameters of the designed rectifier are summarized in Table 3.
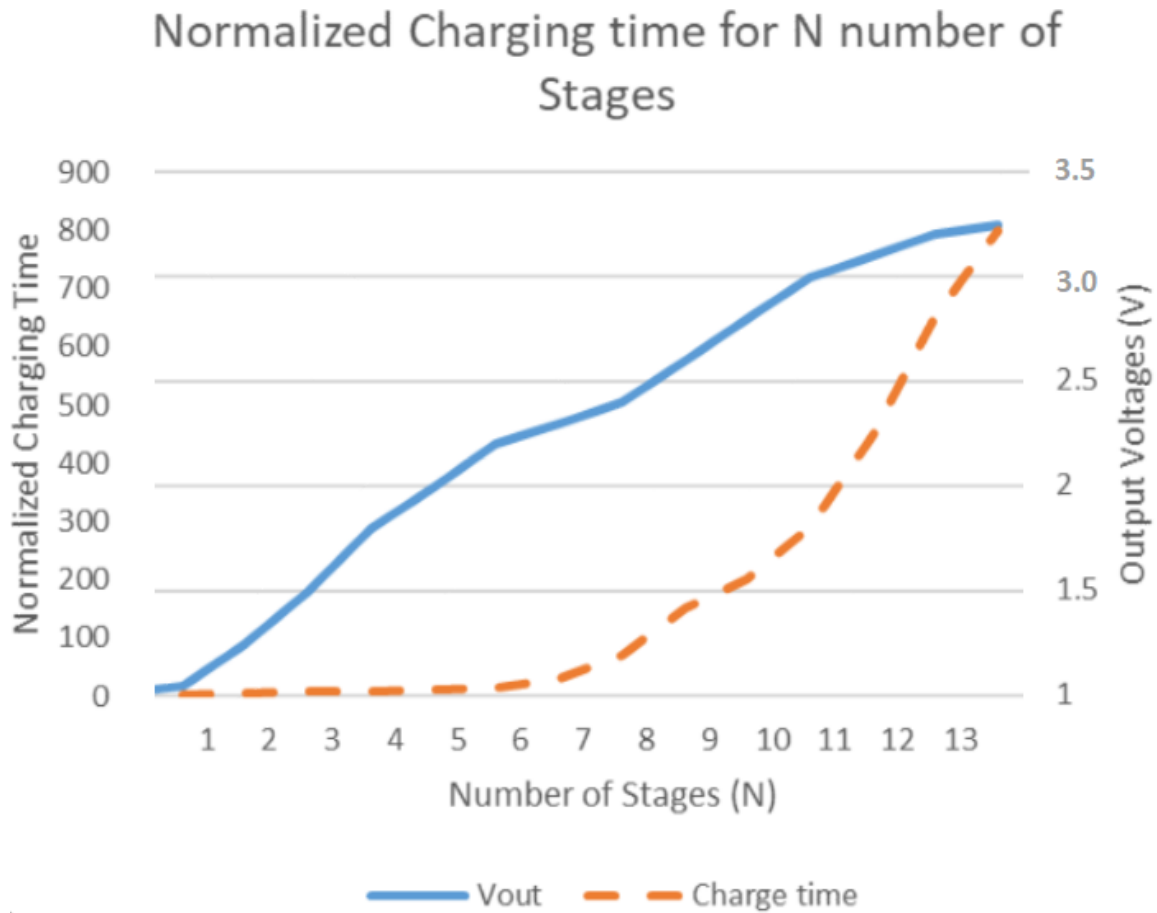
Fig. 4.0.11 Normalized charge time and output voltages for N number of rectifier stages.

Table 3 Performance summary of the rectifier design

Input Power	-25 dBm
Coupling Capacitor (C)	0.4 pF
Device Width (W)	10μm
Number of Stages (N)	10
Charging time	1.5 s
Output Voltage	1.6 V

4.2 Components of Power Management Block

The design of all the necessary components of the power management block is presented in this section. Fig. 4.0.12 shows all the components of the block and their interconnection. The design is

composed of a voltage reference, a current-to-voltage converter, a voltage detector, and a voltage regulator.
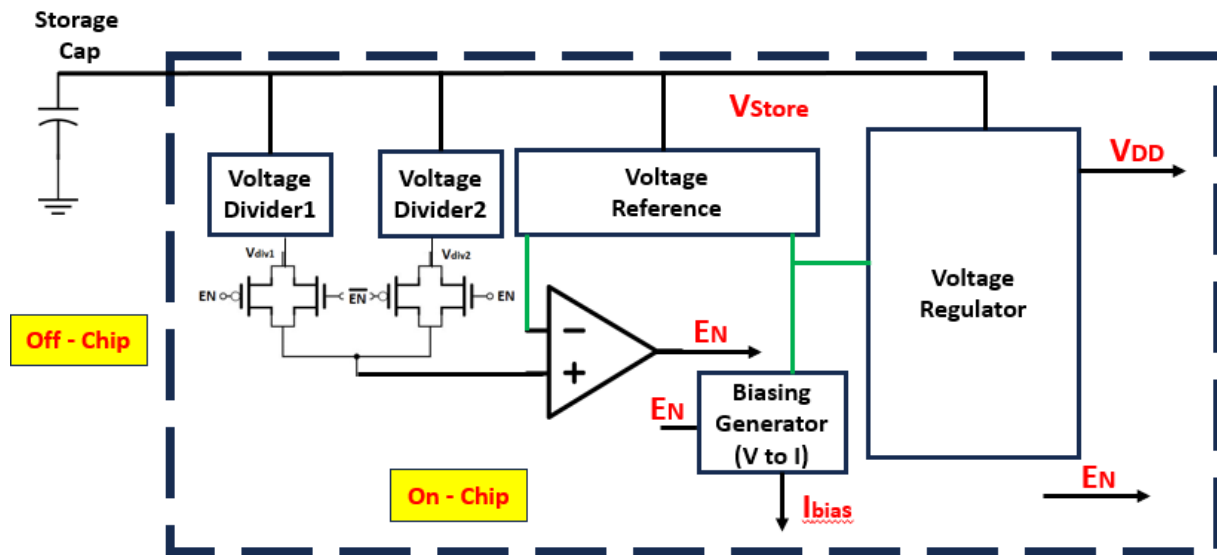
Fig. 4.0.12 Components of power management block

Voltage Reference Design

The voltage reference circuit sits at the core of the power management circuit and generates voltage reference for all the other necessary circuits. The voltage reference is enabled all the time of WSN operation therefore it must be designed for minimum power consumption with minimal compromise on its temperature and supply voltage performance. In this work, we proposed a subthreshold MOSFET-based voltage reference circuit. The circuit implements a proportional to the square of absolute temperature $(PTAT)^2$ current source to generate temperature stable voltage reference through non-linear compensation of the subthreshold temperature dependency of diode-connected MOSFET. The bias current is generated using an Oguey current source [67], but the current source is modified to improve the PSRR (power supply rejection ratio) of the bias current generator. Fig. 4.0.13 shows the topology of the voltage reference circuit. It consists of a reference

voltage generating branch, a (PTAT) [2-bias] current generator, and a start-up circuit. All the MOSFETs in the circuit except M_{12} and those of the start-up circuit operate in strong inversion.
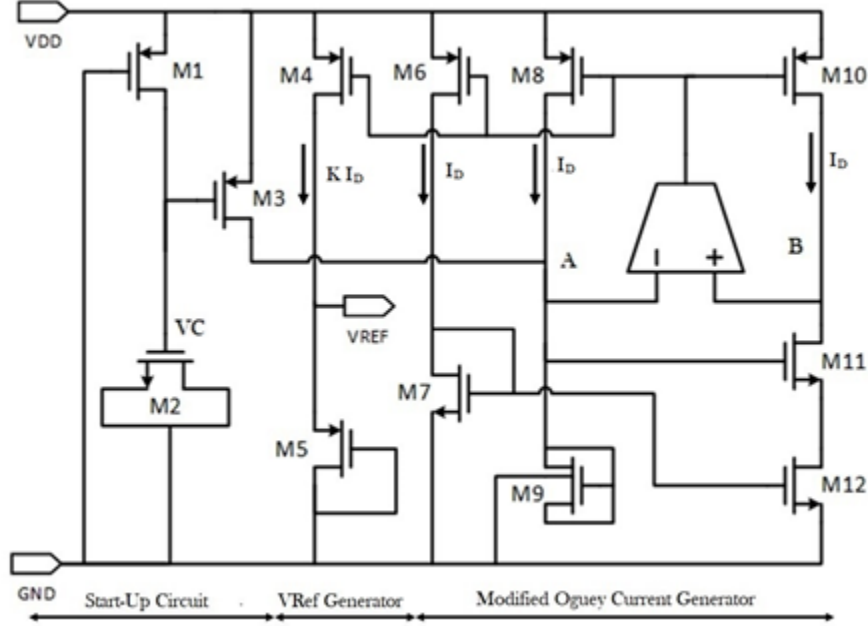
Fig. 4.0.13 The voltage Reference circuit design

As shown in Fig. 1, the voltage reference is obtained by passing a bias current (I_D) through a diode-connected MOSFET (M_5) operating in the subthreshold region. In this region, the drain current of the MOSFET is expressed as [68]:

$$I_D = \frac{W}{L} \mu\, C_{ox}\, V_T^2 e^{\left(\frac{V_{GS} - V_{TH}}{n\, V_T} \right)} \left[1 - e^{\left(-\frac{V_{DS}}{V_T} \right)} \right] \tag{12}$$

where W & L are the width and length of the MOSFET respectively, μ is the electron mobility, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area, t_{ox} is the oxide thickness and ε_{ox} is the oxide permittivity. V_T is the thermal voltage, which is denoted by $V_T = KT/q$, where K is the Boltzmann Constant, T temperature, and q charge of an electron. V_{GS} denotes the gate-source voltage, V_{TH} is the threshold voltage of the MOSFET, and n is the subthreshold slope parameter. V_{DS} is the drain to source voltage drop of the MOSFET. The sizing of the MOSFET is kept such

46

that V_{DS} satisfies the condition for the subthreshold region of operation i.e., $V_{DS} \geq 4V_T$. In the subthreshold saturation region, (12) can be expressed in terms of V_{GS} as:

$$V_{GS} = nV_T \ln\left[\frac{I_D}{\frac{W}{L}\mu \, C_{ox} \, V_T^2}\right] + V_{TH} \tag{13}$$

Note that there are three temperature-dependent terms V_{TH}, V_T, and μ in (13) that are being summed to generate V_{Ref}. V_T has a positive temperature (TC) while it is a well-established fact that μ and V_{TH} have a negative TC. Thus, to perform temperature compensation of the V_{Ref}, I_D should be of the form:

$$I_D = \alpha \, \mu \, C_{ox} \, V_T^2 \tag{14}$$

where α is a temperature-independent term. Note that the current ID in (14) should have a square dependency on the temperature to effectively cancel out the nonlinear term in (13). The current should also have a direct relation with μ. Substituting (14) in (13) gives:

$$V_{Ref} = V_{GS} = nV_T \ln[\alpha] + V_{TH} \tag{15}$$

With the proper setting of the remaining parameters in (15), a temperature-insensitive reference voltage is obtained.

The bias current of the form in (14) can be generated using the Oguey current reference source [67]. The Oguey current reference source is a supply-insensitive, self-biasing circuit that can produce a $(PTAT)^2$ current. As shown in Fig. 4.0.13, a modified form of the Oguey current reference source is used to generate the bias current. The modifications are discussed in the next section. The bias current I_D of the circuit is determined by M_{12}, which is operating in a deep-triode region (i.e., the V_{DS} of M_{12} is much less than its overdrive voltage $[V_{GS}-V_{TH}]$). The current flowing in M_{12} can be expressed as:

$$I_{D12} = \mu\, C_{ox}\, K_{12}[(V_{GS12} - V_{TH12})V_{DS12}\frac{1}{2}V_T^2] \tag{16}$$

and the voltage $V_{DS12} = V_{GS9} - V_{GS11}$ can be expressed as [67]:

$$V_{DS12} = nV_T \ln[\frac{K_{11}}{k_9}] \tag{17}$$

The MOSFET M_7 is diode-connected and operates in saturation. Its current can be expressed as:

$$I_D = \frac{\mu\, C_{ox}}{2}\, K_7(V_{GS7} - V_{TH7})^2 \tag{18}$$

Equations (16), (17), and (18) can be solved to give the current I_D as:

$$I_D = \frac{\mu\, C_{ox}}{2}\, K_7 V_T^2 K_{eff} \tag{19}$$

With

$$K_{eff} = \left[S_2 - 0.5 + \sqrt{S_2(S_2 - 1)}\right]\ln S_1{}^2 \tag{20}$$

Where:

$$S_1 = \frac{K_{11}}{K_9}\ , S_2 = \frac{K_{12}}{K_7} \tag{21}$$

The current I_D is proportional to the square of absolute temperature and μ, which meets all the requirements of I_D shown in (14). The factor K_{eff} is a function of device sizes and, therefore, can easily be adjusted.

As mentioned previously, some modifications are made to the traditional Oguey current source. To achieve a high PSRR and improved line sensitivity, the modified Oguey current generator block uses a subthreshold operational transconductance amplifier (OTA) and PMOS-based N-Well

diodes. Rather than using a diode-connected MOSFET, a PMOS-based diode is implemented by connecting the drain, source, and gate terminal of M_9 thus utilizing the P-N junctions formed between the N-well (body connection) and the source/drain terminals of the PMOS. The diodes in M_9 exhibit a constant voltage drop with respect to the supply voltages thus improving the overall line sensitivity of the generated current.

The bias current of the OTA is only 2 nA and comes from the same current generator block. The OTA keeps the voltages of nodes A and B in Fig. 4.0.13 equal so that the change in supply voltage can be directed to the drain-source voltages of M_8 and M_{10}. When the supply variation causes the voltage of node B to increase, the input to the non-inverting terminal of OTA increases, which increases the output of the OTA. This increase in the output of the OTA in turn decreases the V_{GS10} and thus effectively increases V_{DS10}, and the voltage of node B would fall again and vice versa. To further enhance the supply rejection, the channel length of the PMOS current mirrors (M_4, M_6, M_8, and M_{10}) are kept long to have a high output impedance, which also prevents the channel length modulation effect.

During the time of start-up, the circuit can settle in two possible stable states. One of the states corresponds to (19), and the other stable state is when the bias current is zero. To prevent the zero bias current state, a start-up circuit is employed as shown in Fig. 4.0.13. The start-up circuit comprises of M_1, M_2, and M_3. M_2 is connected as a MOS-CAP, which is required to produce a necessary delay in the turning-off of M_1 and M_3. When the circuit starts, the node voltage V_C is zero. Thus, both the transistors M1 and M3 are ON in strong inversion. The MOS-CAP now charges through M_3 up to the supply voltage V_{DD}, causing M_1 and M_3 to eventually turn OFF. The start-up circuit consumes power only during the start-up time.
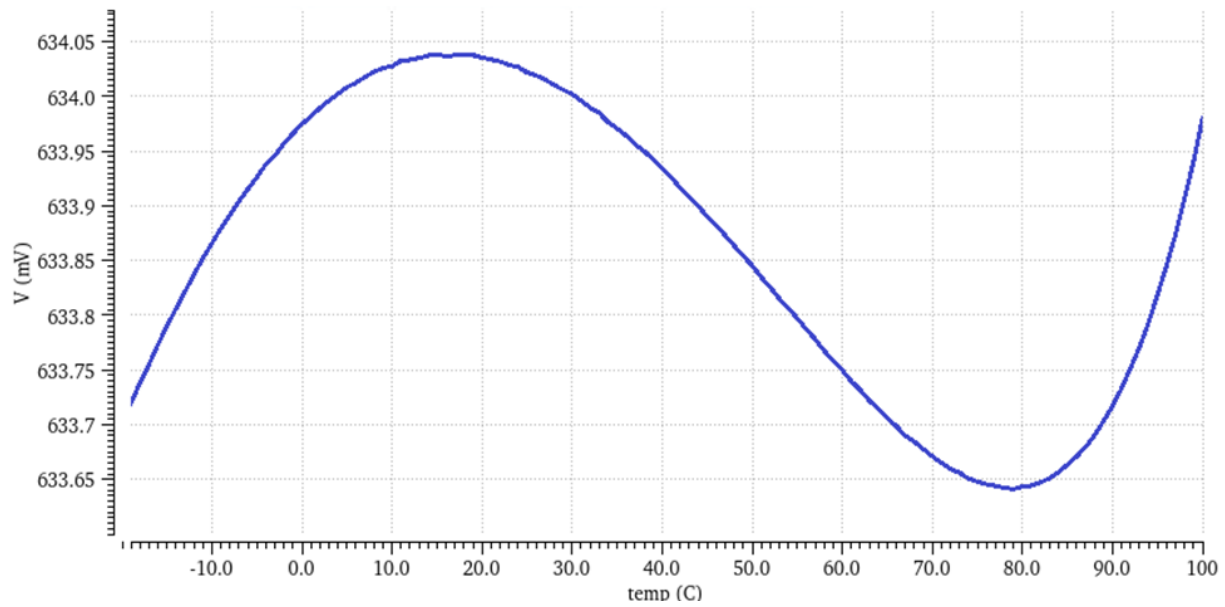
Fig. 4.0.14 Temperature dependence of voltage reference circuit

The power consumption of the circuit at room temperature is around 32 nW, which is constant over the 0.65 to 2.5 V supply range. Fig. 4.0.14 shows the temperature sensitivity of V_{Ref} at 1.5 V supply. The TC of V_{Ref} is 5.2 ppm/°C for the temperature range of -20 to 100 °C. The line sensitivity of the V_{Ref} at 27 °C for the supply voltage range of 0.65 to 2.5 V, is 0.0015 %/V. PSRR of the circuit at room temperature is shown in Fig. 4.0.15, at a supply voltage of 1.5 V. The circuit achieves a PSRR of −80 dBs @ 100 Hz and less than -30 dBs at higher frequencies without the use of any capacitor at the output. The simulated performance of the voltage reference circuit is summarized in Table 4
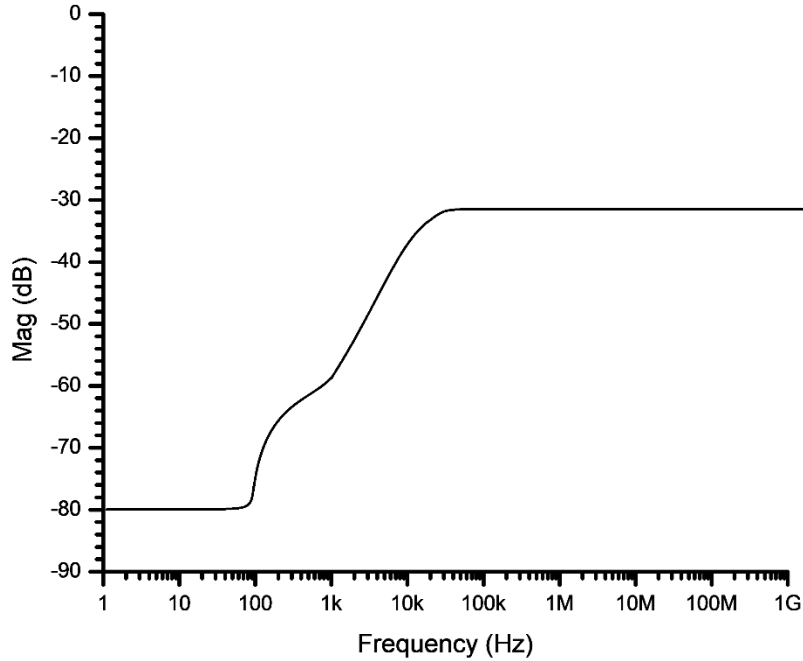
Fig. 4.0.15 PSRR of the voltage reference circuit

Table 4 Performance summary of the voltage reference

V_{dd} (V)	0.65 to 2.5
Temperature Range (°C)	-20 to 100
V_{Ref}	27
Temperature Coefficient (ppm/°C)	5.2
Power Consumption (nW)	32
PSRR (dBs)	−80 @ 100 Hz
Line Sensitivity (%/V)	0.0015

Sub-Threshold OTA Design

For node tracking in voltage reference circuit, voltage detection, and voltage regulation in the power management design, a two-stage Miller-Compensated OTA. The amplifier operates in a sub-threshold region to achieve Nano-Watt power consumption. The OTA schematic is shown in Fig. 4.0.16.

51
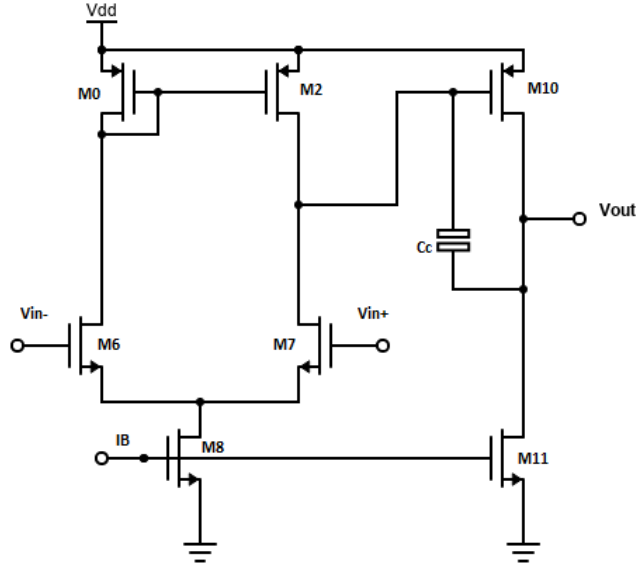
Fig. 4.0.16 The designed two-stage Miller-Compensated OTA

The capacitance C_C is used as compensation for closed-loop stability. The overall DC Gain of the OTA is given by the following equation.

$$A_{VDC} = g_{m1}\, g_{m7}(r_{d1}||r_{d3})(r_{d6}||r_{d7}) \tag{22}$$

Where g_m is the transconductance, r_d is the drain-source resistance.

$$g_m = \frac{I_D}{m\, V_T} \tag{23}$$

And

$$r_d = \frac{m\, V_T}{I_D \lambda_D} \tag{24}$$

Where λ_D is the DIBL effect coefficient. Thus,

$$A_{VDC} \cong \frac{1}{(\lambda_{D1} + \lambda_{D3})(\lambda_{D7} + \lambda_{D6})} \tag{25}$$

Since transistor length is inversely proportional to DIBL coefficient λ_D length of NMOS and PMOS transistors is modified to adjust the gain Av of the two-stage op-amp as shown in the equation:

$$A_{VDC} \cong \frac{1}{\frac{1}{L_P} + \frac{1}{L_n}} \qquad (26)$$

The relation between compensation capacitance C_c and gain–bandwidth product (GBW) is given by the equation:

$$\omega_{GBW} = \frac{g_{m1}}{C_c} = \frac{I}{nV_T C_C} \qquad (27)$$

With proper sizing using the above equation and a bias current on 2n Amp, the amplifier shows greater than 63 dBs open-loop gain. The dimensions and values of different components of OTA are listed in Table 5.

Table 5 Parameters of the designed OTA

M_0, M_2	20 µm/500nm
M_6, M_7	5µm/500nm
M_8	1µm/500 nm
M_{11}	20 µm/500nm
M_{10}	10 µm/500nm
C_c	2 pF
I_{Bias}	2 nA
V_{dd}	0.65 to 2.5 V

The simulated performance of the OTA on different process corners is summarized in Table 6.

Table 6 Simulated performance of the designed OTA.

Corner	UGBW (MHz)	PM (Degree)	DC gain (dBs)
TT	30	52	63
SS	27	52.2	62.5
FF	33	52	63.8
FS	29	52.1	63.5
SF	32	51	61.5

Voltage Reference to Current Reference Conversion

The circuit illustrated in Fig. 4.0.17 is employed to generate necessary current references for the proposed system. The circuit is constructed OTA in negative feedback configuration. The output current passing through R_1 (433K) is set at 1.5 μA by the reference voltage applied to the input of the differential pair. This current remains constant due to the feedback and is not influenced by variations in the supply voltage. N+ polysilicon resistor is employed for R_1 to ensure reliable temperature performance. The circuit self-biased using a current mirror in the resistance-carrying branch to make it independent of any external reference. The reference current is supplied to the system through M_{P8} and M_{P6}. To conserve power this block is enabled only during the wireless data transmission phase and disabled during energy harvesting, through the transistors M_{N8} and M_{N10}.
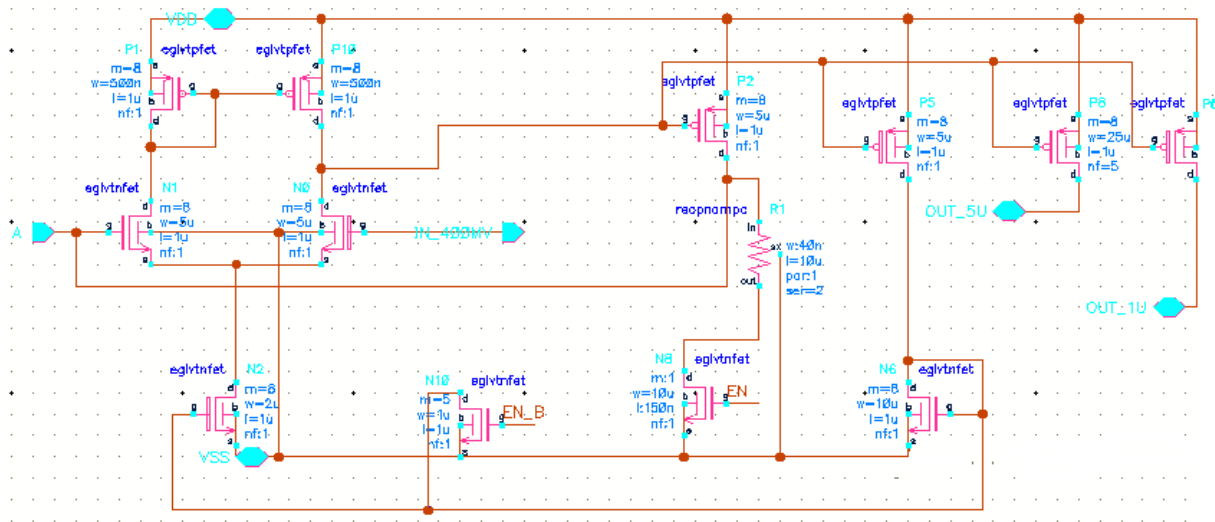
Fig. 4.0.17 The implemented architecture for current generation from voltage reference.
In Fig. 4.0.18, the simulated I_{ref} vs. temperature is shown for three different process corners. The TC of the current in the typical process corner is simulated to be 25 ppm/°C within the range of -20 °C to 100 °C. The most significant TC occurs in the fast corner, reaching 100.8 ppm/°C. The variation seen across process corners is unavoidable due to the tolerance of the resistors. All the

circuits using the bias currents coming from this block are simulated for the variation in the bias current to ensure their performance in all possible process and temperature corners.
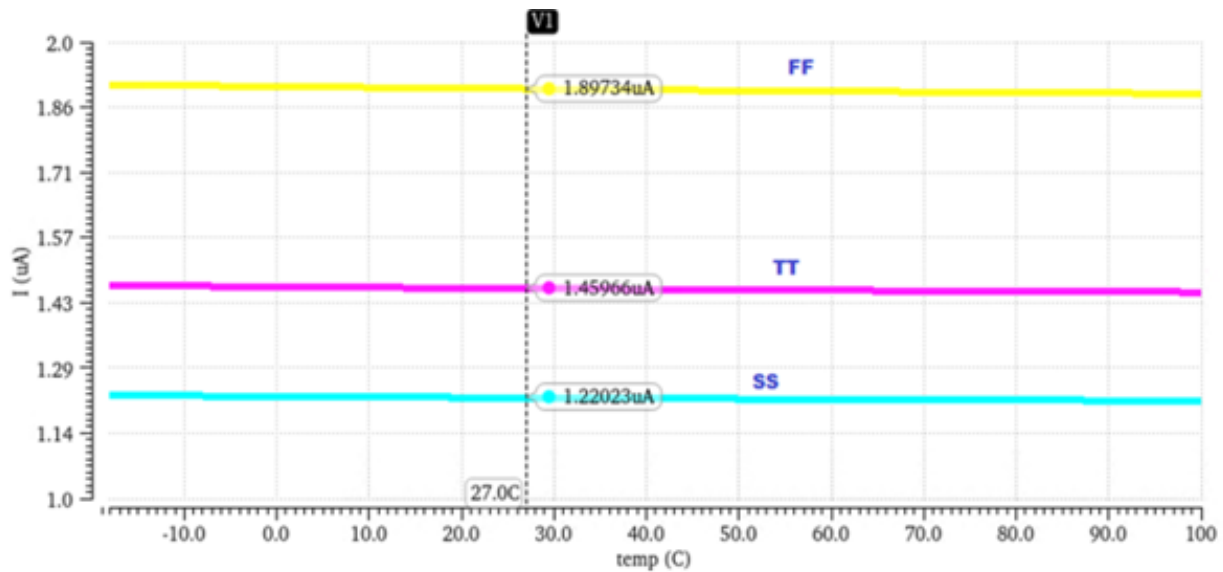
Fig. 4.0.18 Simulated current reference I$_{ref}$

Voltage Regulator Design

The voltage regulator ensures a stable V$_{dd}$ (0.8 supply voltage) for the operational block of the WSN. It is enabled only during the wireless data transmission phase; therefore, it must have a fast-settling time, effective load regulation, low dropout voltage (V$_{drop}$ = V$_{in}$ - V$_{out}$), and minimal quiescent current (consumption during no load). The dropout voltage establishes V$_L$ (the lower trigger level of the power management block that disables data transmission). If the input voltage (V$_{store}$) falls below 0.8+V$_{drop}$, the voltage regulator cannot sustain the WSN circuit's V$_{dd}$, impairing their functionality. Fig. 4.0.19 shows the configuration of the voltage regulator. As previously mentioned, the same Operational Transconductance Amplifier (OTA) designed in the previous section serves as the core of the voltage regulator, with a PMOS as pass device.
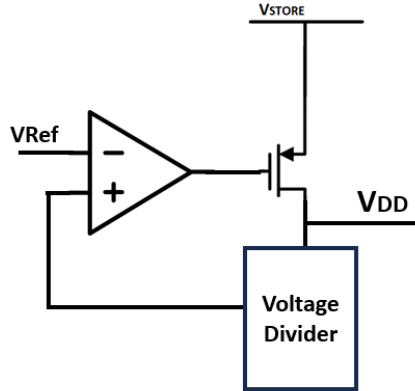
Fig. 4.0.19 Voltage regulator configuration

The reference input and bias current for the voltage regulator are provided by the designed voltage reference and V-I converter circuit, respectively. To conserve chip area, the voltage divider network, which sets the output voltage of the voltage regulator, is implemented using stacked PMOS diodes. This voltage divider network can generate the required feedback voltage with minimal power consumption, effectively reducing the quiescent current of the voltage regulator.. The simulated performance of the voltage regulator is summarized in

Table 7. The simulated max V_{drop} is found to be 150 mv at max load condition (I_L = 10mA) across all process corners. Therefore, it's safe to set V_L = 0.8+0.15 = 0.95 V.

Table 7 Simulated Performance summary of the designed Voltage regulator.

V_{out} (V)	0.8
I_Q	10 nA
Max Load (mA)	10
C_L(pF)/R_L(ohms)	10/80
PSRR(dB)	-30/100 MHz
DC Load Regulation (mV/mA)	1.2
Settling time (us)	0.25
Dropout Voltage (at max load)	0.15

Storage Voltage Detector

The storage voltage detector operates directly from V_{store}, necessitating its ability to function at a supply voltage as low as 0.65 V. It employs a modified version of the OTA designed in the previous section. The configuration of the voltage detector is illustrated in Fig. 4.0.20. This detector continuously monitors the storage capacitor's voltage level using the voltage supplied by two voltage dividers connected to the V_{Store}. One voltage divider (V_{div1}) corresponds to V_H, and the other (V_{div2}) corresponds to V_L. A 2:1 multiplexer (MUX) is implemented using transmission gates, selecting the appropriate voltage division applied to the non-inverting input of the voltage comparator. The reference voltage (V_{ref}, 0.63 V) is applied to the inverting input of the voltage comparator. The voltage comparator controls the activation or deactivation of wireless data transmission and switches the states of the WSN based on the storage capacitor voltage (V_{store}).
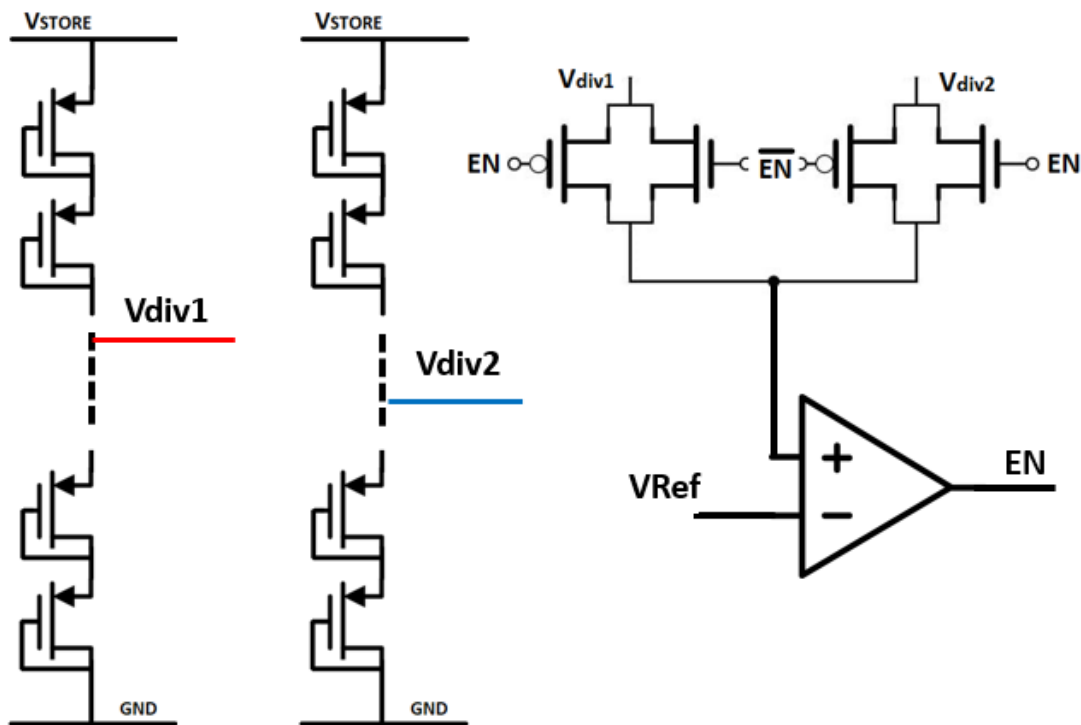
Fig. 4.0.20 Storage Voltage Detector

57

During the cold start (EN = 0, $\overline{\text{EN}}$ = 1) Vdiv1 is applied to the input of the comparator through the MUX, which keeps the WSN in energy harvesting mode until the storage voltage level reaches V_H (V_{div1}> 0.63 V). When the WSN enters wireless data transmission mode (EN = 1, $\overline{\text{EN}}$ = 0) the Mux switches the input of voltage comparator to Vdiv2. Since V_{store} is still greater than V_L (V_{div2}> 0.63) the output of the voltage comparator remains enabled but the transmission circuits start drawing current from the storage capacitor and keep discharging it until V_{store} drops to voltage level VL (V_{div2}< 0.63 V). The voltage comparator again switches the WSN into energy harvesting mode (EN = 1, $\overline{\text{EN}}$ = 0) and this cycle keeps repeating. The transient simulations are shown in Fig. 4.0.21. The total simulated power consumption of the power management circuit during energy harvesting is about 40 nW.
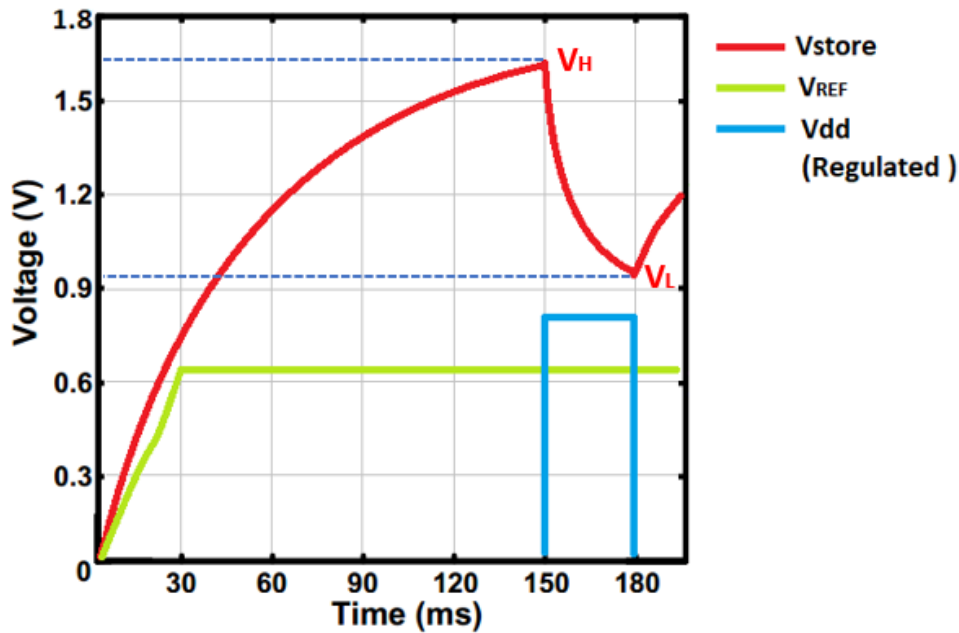
Fig. 4.0.21 Integrated functionality simulation of the storage voltage detector, voltage reference, and voltage regulator.

4.3 Conclusion

In this chapter, we presented the design and simulation of all the necessary components of the Energy harvester. The received signal is used for RF energy harvesting and the harvested energy is used to charge a storage capacitor. A power management circuit is combined with the energy harvester for efficient utilization of the stored charge. During the energy harvesting phase, the power consumed by the PMC is 40 nW. Simulation shows an initial charging time of 150 ms with Pin = -25dBm, after that the frequency of the charge/discharge cycle of the storage capacitor depends upon the power consumption of the wireless data transmission circuit and temperature sensor.

CHAPTER 5 WIRELESS DATA TRANSFER CIRCUIT DESIGN

5.1 Frequency Synthesizer

The frequency synthesizer's block diagram is presented in Fig. 5.0.1 This synthesizer takes its reference frequency input from the antenna and initially divides the frequency by 3 to produce a 305 MHz reference frequency for the DLL circuit. The DLL then multiplies this frequency by a factor of 8 to generate the 2.44 GHz carrier signal for wireless data transmission. The design details of each component within the frequency synthesizer are discussed in subsequent sections.
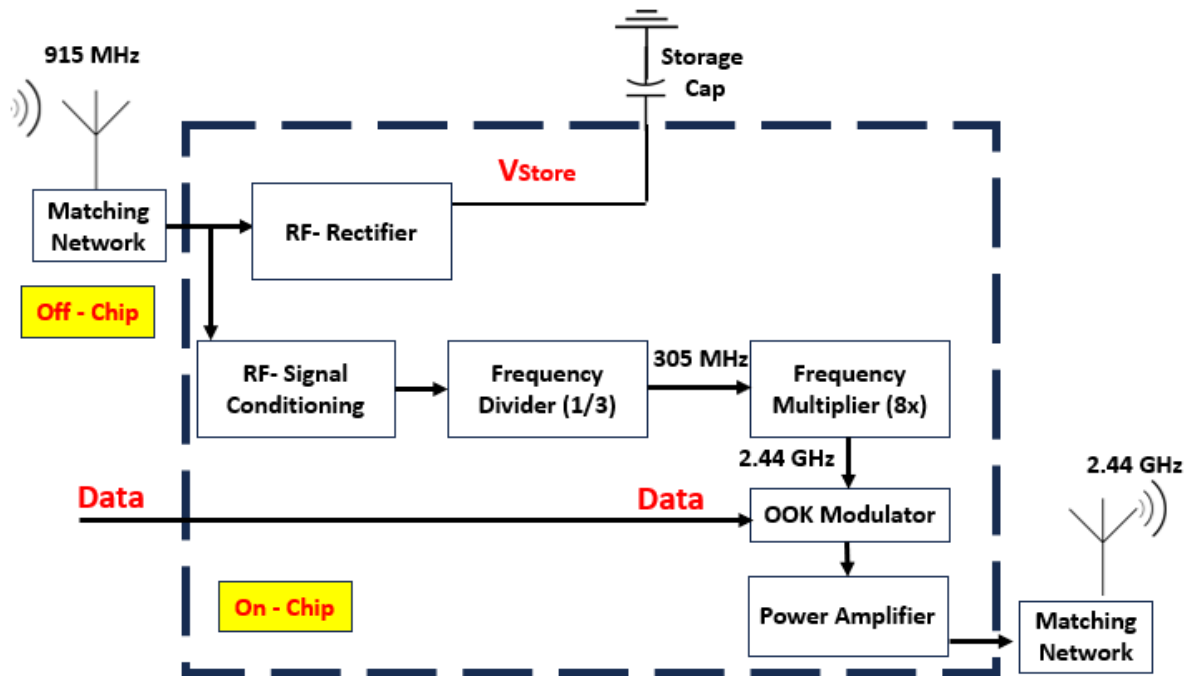
Fig. 5.0.1 Frequency synthesizer for generating 2.44 GHz carrier signal.

RF signal Conditioning and Frequency Divider

The RF signal conditioning circuit converts the incoming RF signal received by the antenna into a square wave signal. This conversion is essential to drive the input of the frequency divider circuit. The incoming RF signal undergoes AC coupling using C2, and a DC offset, equal to half of the supply voltage, is applied to the signal through a voltage divider formed between M1 and M2. The value of C2 is optimized to ensure that the input impedance of this stage does not impair the energy

harvester and antenna interface. Subsequently, the signal is amplified by the inverter chain, consisting of transistors M5, M6, M7, and M8, as illustrated in Fig. 5.0.2. Simulations indicate that a minimum Vin of 120 mV is sufficient for the signal conditioning to operate effectively at an input RF power of -25 dBm. This feasibility is attributed to the resonant voltage spiking effect obtained due to the matching network.
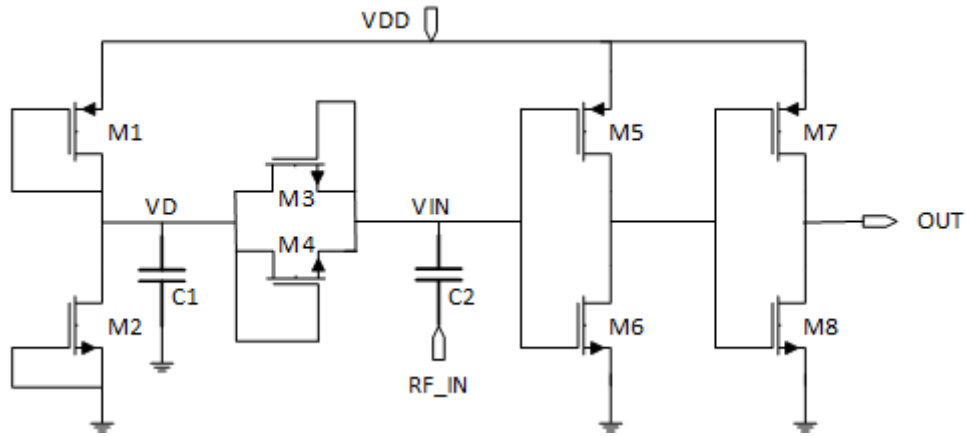
Fig. 5.0.2 RF signal Conditioning Circuit
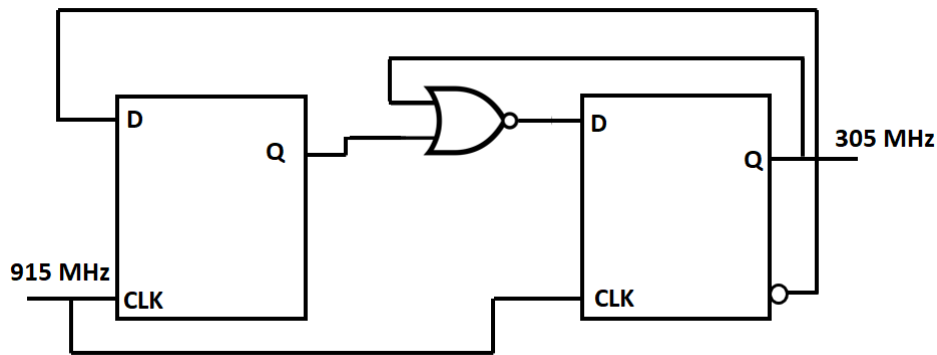
Fig. 5.0.3 Frequency divider 1/3

The circuit shown in Fig. 5.0.3 down converts the input signal into a low frequency signal of 1/3 frequency. The frequency divider uses high-speed TSPC D flip-flops (DFF) and logic circuits to determine the division ratio. The circuit is optimized for power consumption and frequency. The

simulated waveforms of the RF signal conditioning circuit coupled with the frequency divider are

shown in Fig. 5.0.4. Process spread of the duty cycle is simulated and summarized in Table 8. The

frequency divider along with the signal conditioning circuit consumes 35 µW power.
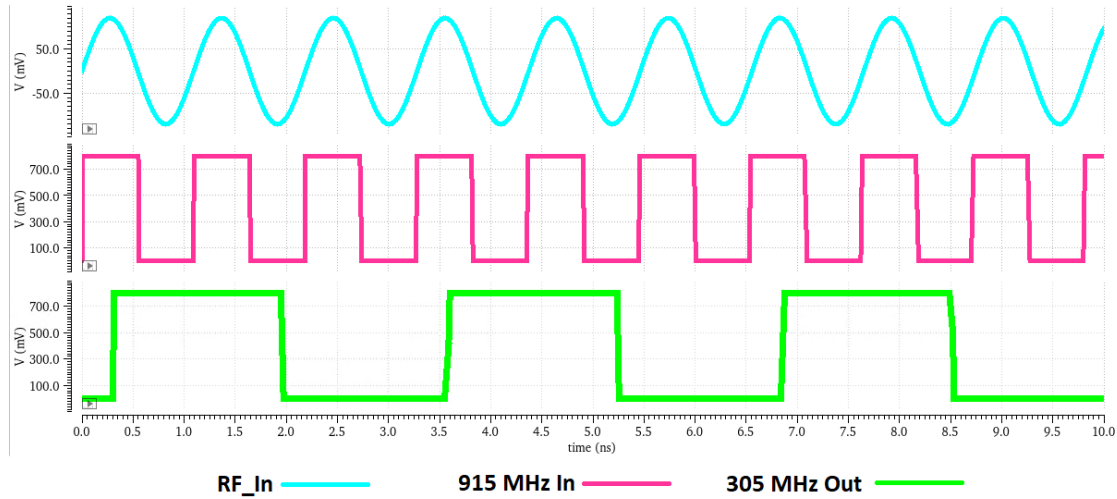
Fig. 5.0.4 Waveform simulation of RF signal conditioning circuit with frequency divider.

Table 8 Simulated Process spread of the frequency divider duty cycle.

Corner	Duty Cycle (%)
TT	49.8
SS	49.95
FF	50.2
FS	50.5
SF	49.9

Design of the Low-Power Delay Locked Loop

The 305 MHz signal is provided to a Delay Locked Loop (DLL) which multiplies this frequency

by a factor of 8x to generate the 2.44 GHz signal. A series of three 2x multipliers is used to achieve

8X frequency multiplication. A single 2x multiplication DLL is configured as shown in Fig. 5.0.5.

Each 2x multiplication comprises a voltage-controlled delay cell (VCDL), an XOR gate, and a

duty-cycle control loop (DCCL). Given that frequency locking is not an issue, an XOR gate is preferred as the phase detector in our approach.
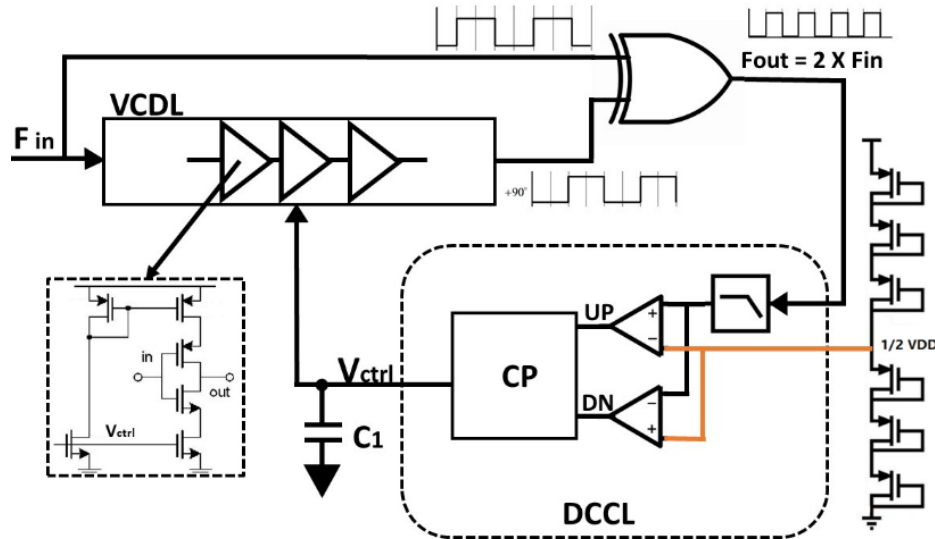
Fig. 5.0.5 DLL configuration showing the full operation of 2X multiplication.

The XOR gate takes in both the original signal and the delayed signal to output a 2X frequency, as shown in Fig. 5.0.6.
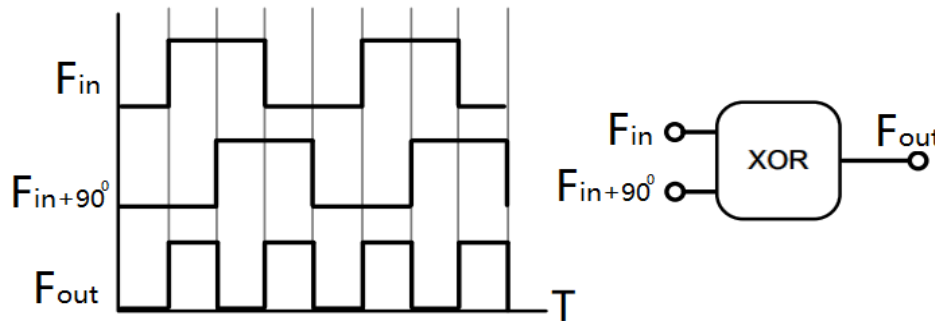
Fig. 5.0.6 XOR logic-based frequency multiplication technique.

Initially, the delay introduced by the VCDL may not be exactly 90°. The duty cycle may be less than or greater than 50%. The duty cycle correction circuit uses a passive integrator to generate an average DC voltage proportional to the duty cycle. The output of the integrator is compared with a voltage level equal to half of the supply voltage (V_{DD}) using comparators. After comparison, the DCCL circuit signals the charge pump (CP) circuit to generate feedback control voltages. The feedback coming from CP then varies V_{ctrl} to correct the delay to 90°, achieving a 50 % duty cycle.

Current Starved Delay Cell

Current-starved full-swing inverter cells are used in the VCDL to generate the 90° delay. The implemented delay cell is optimized for low power consumption and is shown in Fig. 5.0.7. The current in the delay cell is controlled by the gate voltage of MN2 and MP2. The inverter is sized to produce only a fraction of the total delay. Too many or too few delay cells in VCDL can impact the process corner variation. Therefore, the number of delay cells in each VCDL is optimized to achieve better performance across process corners. Careful consideration in layout design is taken to minimize mismatches.

Fig. 5.0.7 Implemented Current Starved Delay Cell

XOR Logic

Conventional XOR gates are used for frequency multiplication. The use of an edge combiner is avoided in this implementation to reduce the number of XOR gates. The current implementation

uses only three XOR gates in total to achieve 8X frequency multiplication. Comparatively, an edge combiner will require seven XOR gates for 8X multiplication. The schematic of the implemented XOR gate topology is shown in Fig. 5.0.8. Since each multiplication stage has a different input frequency, each of the XOR gates is optimized for power consumption and frequency.
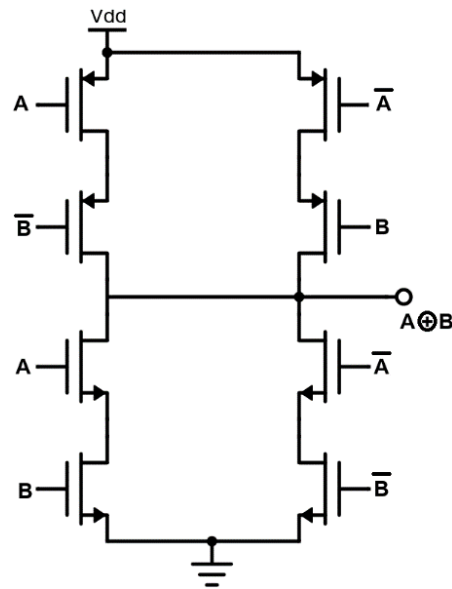
Fig. 5.0.8 Implemented XOR gate.

Duty Cycle Correction Loop

The DCCL ensures a 50% duty cycle of the output on all PVT corners. It controls the delay of VCDL using the signal Vctrl. The feedback forces the average (i.e., DC component) of the 2X signal to be equal to half of the VDD to achieve a 50% duty cycle. To save power and area, diode-connected stacked PMOS devices are used. The stacked MOS diodes generate a V_{REF} equal to half of V_{DD}. A passive RC-integrator extracts the DC of the 2X signal and compares it with V_{REF} using OTAs, as shown in Fig. 5.0.9. The OTAs are biased in the subthreshold region to achieve ultra-low-power operation. The UP and DN signals coming from the OTAs are fed into the charge pump circuit to generate V_{ctrl}.

65
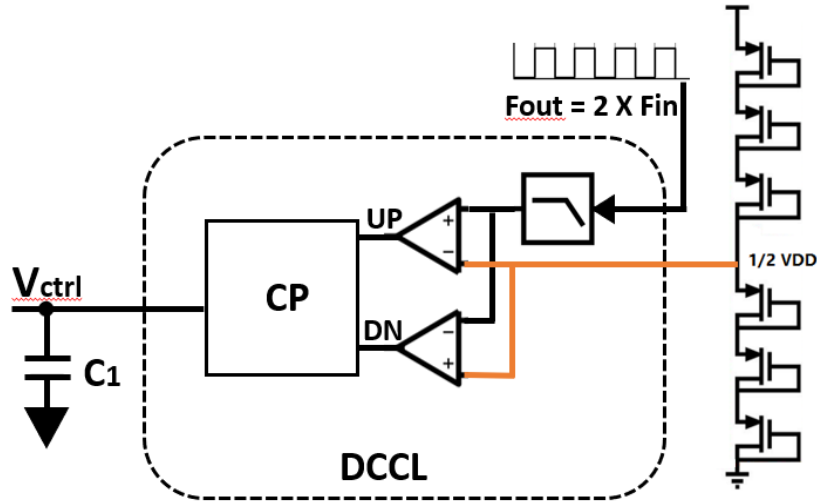
Fig. 5.0.9 Duty Cycle Correction Loop

The implemented charge pump (CP) circuit is shown in Fig. 5.0.10. The CP is biased in the subthreshold region for low current consumption. When the duty cycle is > 50%, the UP signal is High, and the DN signal is Low so that C1 charges and V_{ctrl} increases. This increase in V_{ctrl} decreases the delay in the VCDL until the duty cycle becomes 50%. When the duty cycle is < 50%, the UP signal is Low, and the DN signal is High. Thus, correcting the duty cycle by decreasing V_{ctrl}. This feedback loop ensures a 50% duty cycle across all PVT corners.
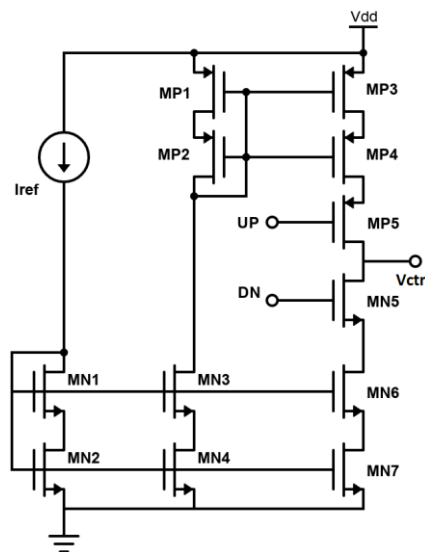
Fig. 5.0.10 Charge pump circuit implementation.

Fig. 5.0.11 shows the performance of the 8X frequency multiplier. 305 MHz is given as input frequency to the multiplier, which generates an output frequency of 2.44 GHz. Fig. 5.0.12 shows the action of the control loop to correct the duty cycle of the output signal. It takes about 40 us to achieve a 50% duty cycle. The experimental result of the multiplier shows a power consumption of about 130 uW at 0.8 V supply.
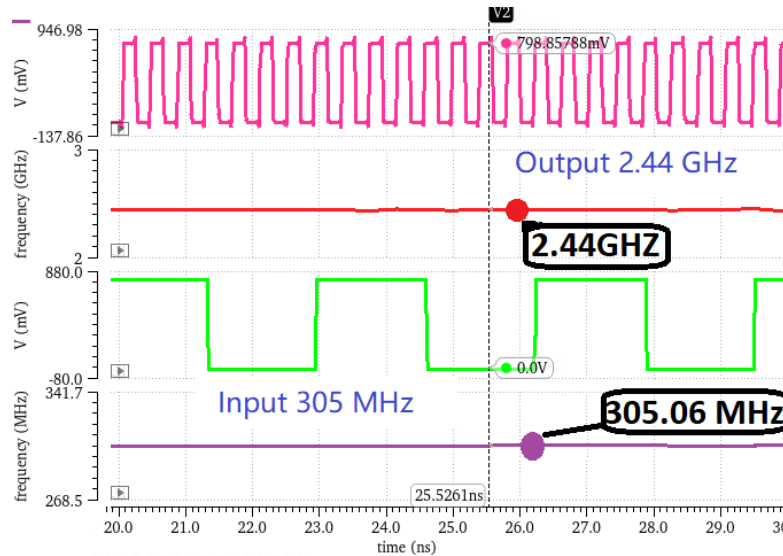
Fig. 5.0.11 Input Vs output Frequency of the proposed circuit showing 8X multiplication.
The circuit passed all the post-layout process corner simulations for a temperature range of -20 to

100 °C while the supply voltage was kept constant at 0.8V.
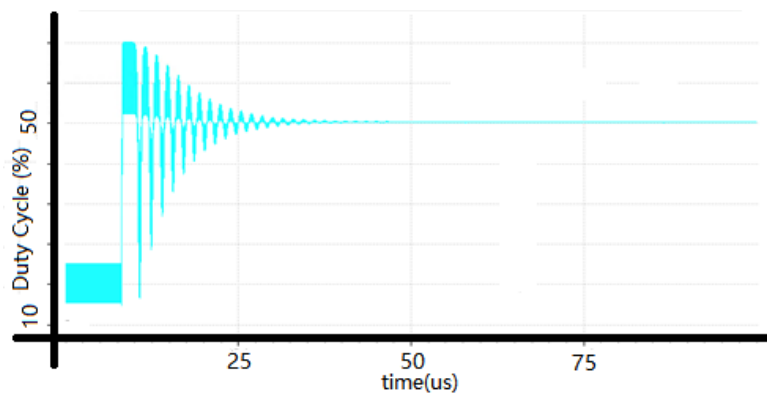
Fig. 5.0.12 The response of the duty cycle correction loop. The circuit takes 40 us to achieve a 50% duty cycle.

67

Fig. 5.0.13 shows the measured Frequency spectrum of the output, with an output buffer. The sideband harmonics power level is seen to be at least 25 dB lower than the carrier. The simulation shows a timing jitter of 24ps (pk-pk).
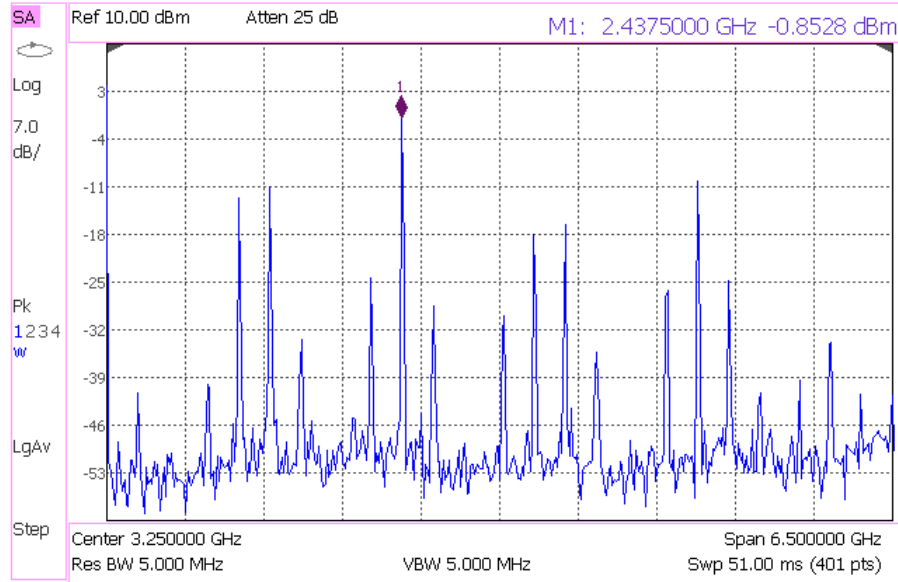
Fig. 5.0.13 Frequency spectrum of the output.

An FOM (figure of merit) is derived from [69] to make a performance comparison with the state-of-the-art (28) calculates the FOM using multiplication factor (N), Power Consumption (Pdc), Process minimum length (L_{min}), operating bandwidth (BW in %), and Area(A). The comparison of performance is summarized in Table 9. The proposed multiplier achieves the best FOM due to lower power consumption, wider operating bandwidth, and better multiplication-factor/area ratio. Note that a lower FOM is an indication of better performance.

$$FOM = 10 \; log\frac{Pdc}{N} + 10 \; log\frac{A}{L_{min}} - 10 \; log(BW) \tag{28}$$

Table 9 Summary of Performance Comparison.

	This Work	[70]	[71]	[72]
Supply Voltage(V)	0.8	0.6 – 1.2	1	N/A
Multiplication Factor	8x	32x	3x	3x
Input/Output Frequency (GHz)	0.305/2.44	0.017/0.574	20/60	3.5/10.5
Timing jitter (Simulated)(ps)	24 ps @ 2.44 GHz (pk-pk)	97 ps @ 574 GHz (pk-pk)	N/A	N/A
Power consumption (mW)	0.13	2.71	50	5.5
Active area (mm^2)	0.09	0.014	0.4	0.075
Technology	22-nm FD-SOI	28-nm FD-SOI	45-nm SOI CMOS	22-nm FD-SOI
FOM	74.01	91.76	111.85	114.53

5.2 Power Amplifier Design

Power Amplifier (PA) is the most significant power consuming block within a WSN. The power consumption of a PA is influenced by various factors including data rate, modulation scheme, output power, and efficiency. The efficiency of a power amplifier can be determined using the formula:

$$Efficiency(\%) = \frac{P_{RF-OUT}}{P_{DC-IN}} \, x100 \tag{29}$$

Where P_{RF-OUT} is the radio frequency power delivered to the load (in watts or dBm). P_{DC-IN} is the direct current power consumed by the amplifier from the power supply (in watts). Various types of PAs have been developed and studied in literature, each with its own advantages and drawbacks. Class A power amplifiers are known for their simplicity and linearity. However, they suffer from

low efficiency, typically around 25%, as they operate in a highly linear but inefficient region of the transistor's characteristics. This low efficiency leads to significant power dissipation and limits their use in battery-powered applications. Class B power amplifiers offer improved efficiency compared to Class A amplifiers by operating in a push-pull configuration. However, they suffer from distortion due to the non-linear behavior of the transistors when transitioning between the on and off states. This distortion results in poor linearity and introduces harmonic components in the output signal. Class C power amplifiers are highly efficient but sacrifice linearity. They operate in a highly non-linear region of the transistor's characteristics, resulting in significant distortion and the generation of harmonic components in the output signal. This limits their use in applications that require high linearity, such as wireless communications. Class D power amplifiers, also known as switching amplifiers, offer high efficiency by operating the transistor as a switch. They achieve this by rapidly switching the transistor between on and off states, resulting in minimal power dissipation. However, they suffer from high levels of harmonic distortion and require complex filtering to remove the harmonic components from the output signal. Class E power amplifiers are a variation of Class D amplifiers that aim to further improve efficiency by optimizing the transistor's switching characteristics. They achieve this by using resonant circuits to shape the voltage and current waveforms, resulting in reduced power dissipation. The modulated data in our application is an OOK signal; thus, a Class-E switching power amplifier is a preferred choice in our work which outperforms typical Class-B or –C in its switching performance. The transistor in the Class-E amplifier (Shown in Fig. 5.0.14) . The power to the amplifier is supplied through a L_{DC} and the DC component of the output is filtered with C_{DC}. The network configuration ensures minimal power dissipation during switching, the output LC filter filters out the transmission signal.

Because of the resonance, the drain voltage can exceed four times of V_{DD} and can be stressful for the switch. Therefore, M2 serves as a cascade to protect the PA from high voltage damage.
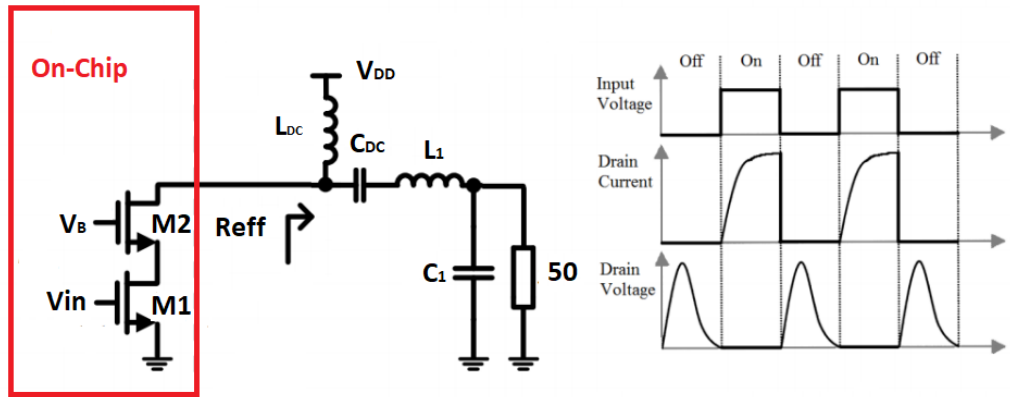
Fig. 5.0.14 Class-E Power Amplifier shown with Voltage and current waveform of the Switch. Power Added Efficiency (PAE) is another crucial parameter in the analysis of power amplifiers.

Power Added Efficiency is a measure of how efficiently a power amplifier converts the DC power it consumes into RF power. In other words, it represents the efficiency of the power amplifier in adding power to the RF signal.

The Power Added Efficiency (PAE) of a power amplifier is defined as the ratio of the RF output power added by the amplifier to the DC input power consumed by the amplifier. Mathematically, it is expressed as:

$$PAE(\%) = \frac{P_{OUT} - P_{IN}}{P_{DC-}P_{IN}} \, x100 \tag{30}$$

Where P_{OUT} is the RF output power, P_{IN} is the RF input power, and P_{DC} is the DC input power. The design is simulated to determine the required dimensions of the transistors for the different design parameters like, maximum PAE, and desired output power for a 0.8 V V_{DD}.

The transient simulation of PA is shown in Fig. 5.0.15. It shows the voltage across the switch and the current through it plotted against time. Marker V1 points at the condition of max V and min I, whereas Marker V2 shows max I and min V condition. In both conditions, the power product is

71

minimal, which is necessary for low switching losses. Fig. 5.0.16 shows the output power to be -4.3 dBm and dc power consumption of 500µW which yields a good power-added efficiency (PAE) of 60.4%. The simulated power gain is good at 11.7 dBs.
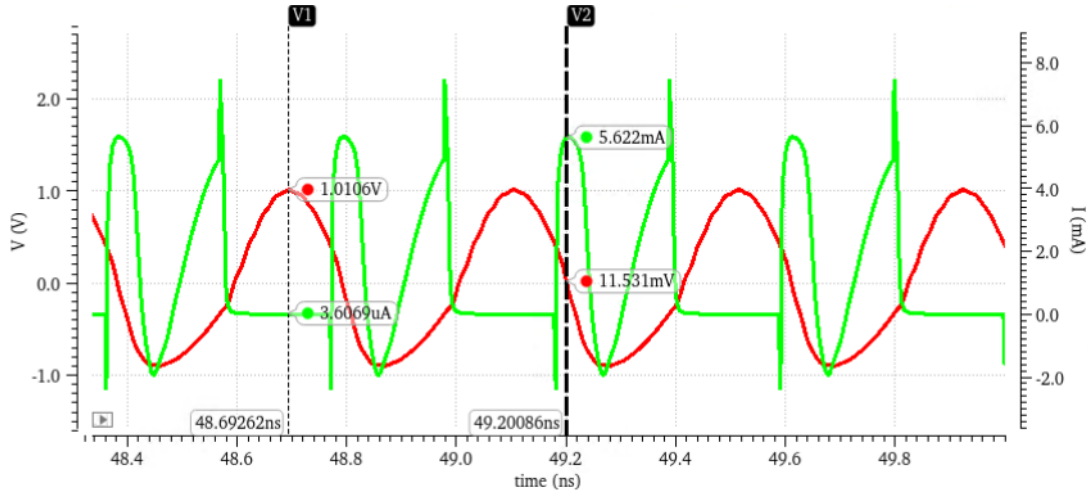
Fig. 5.0.15 Transient simulation of Class-E PA
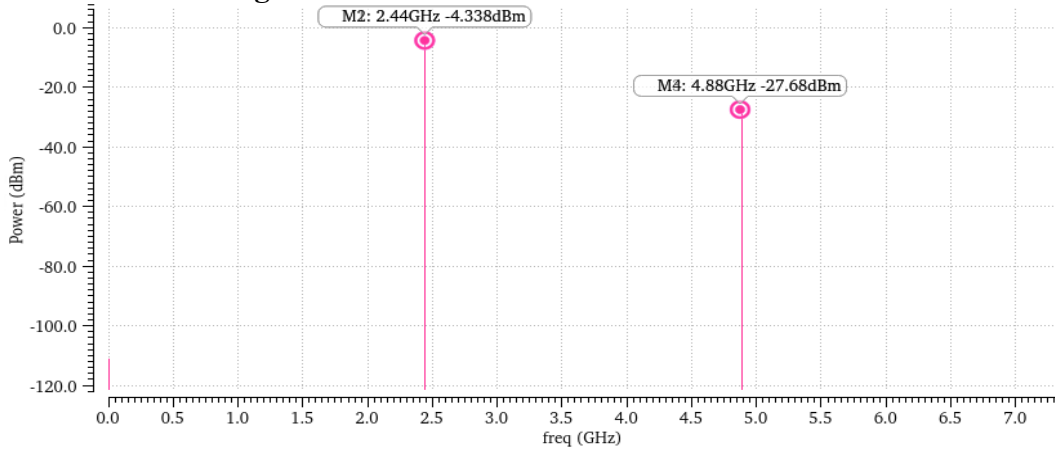
Fig. 5.0.16 Simulated output Power at -16dBm Pin.

OOK Modulation

The OOK Modulation of the carrier signal is achieved by employing a simple three-input AND gate at the input of the PA as shown in Fig. 5.0.17. For the simulation shown a clock of 0.5 Mbps (500 KHz) is applied to the DATA input. The power consumption is observed at 448 µW at -3.1 dBm output power.

72
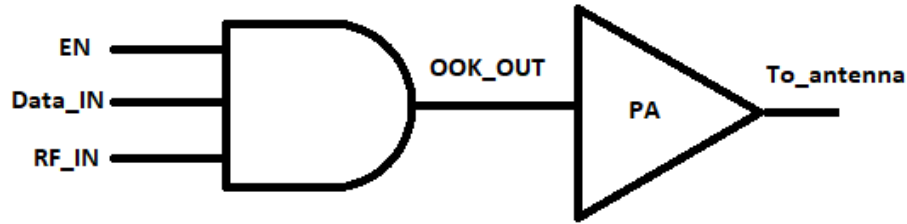
Fig. 5.0.17 OOK modulation using AND gate.
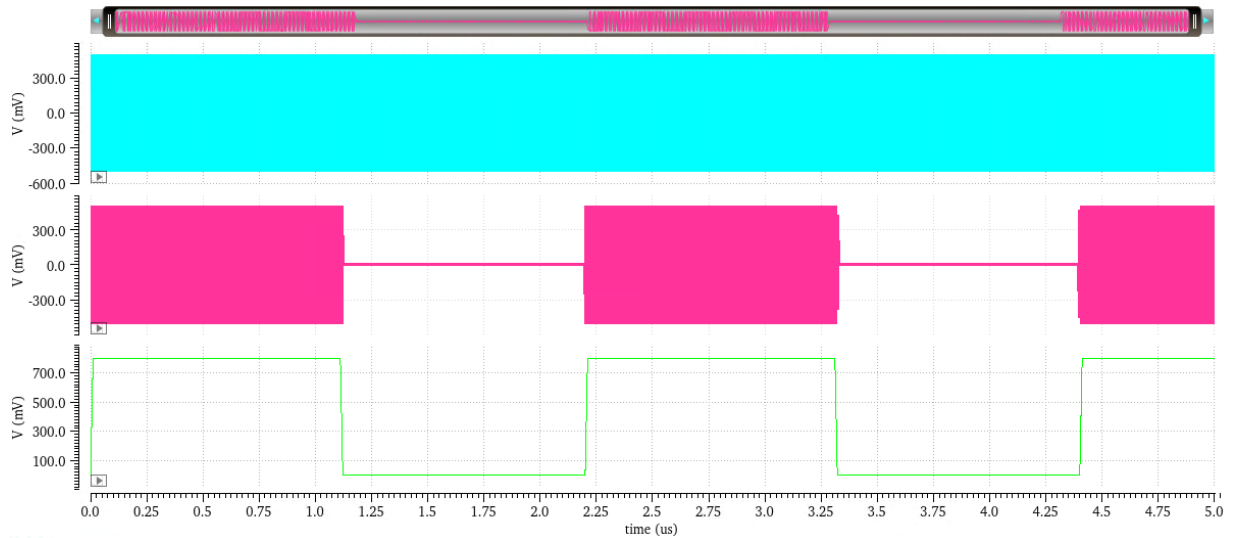
Fig. 0.18 Simulated Transient Response with OOK Modulation.

5.3 Conclusion

In this chapter, we presented the design and simulation of all the necessary components of the frequency synthesizer circuit. A DLL-based and XOR-based frequency multiplier architecture is implemented to generate the 2.4 GHz carrier signal. A Class E switching RF power amplifier is utilized to achieve good power amplifier efficiency. With OOK modulation at 0.5 Mbps, the power amplifier achieves 448 µW at -3.1 dBm output power.

CHAPTER 6 TEMPERATURE SENSOR DESIGN

An ultra-low power temperature sensor is designed in this chapter. The design is fabricated on a separate chip in a 60nm CMOS process. The temperature sensor is designed to be integrated with the proposed WSN in this work.

6.1 The Proposed Temperature Sensor Block Diagram

A temperature sensor detects the temperature around it and generates a digital code as a representation of the detected temperature. Fig. 6.0.1 shows the proposed architecture of our temperature sensor as a block diagram. The design has three major functional blocks: 1) a temperature sensing unit, 2) a voltage-to-frequency converter, and 3) a frequency-to-digital converter logic.
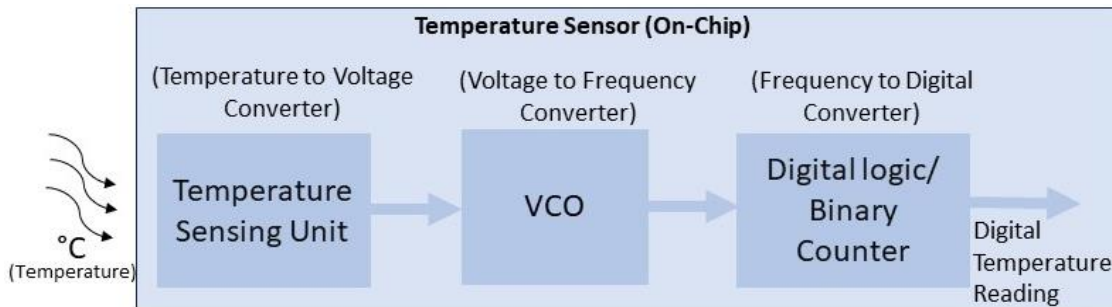
Fig. 6.0.1 Block diagram of the proposed temperature sensor.

The temperature sensing unit generates a PVT-tolerant Reference Voltage (V_{REF}) and a temperature-sensitive voltage (V_{PTAT}). The V_{PTAT} then controls a VCO to convert the temperature change into a temperature-dependent frequency (F_{PTAT}). Another identical VCO converts the V_{REF} into a reference frequency (F_{REF}). In the end, a digital logic circuit compares the frequencies F_{REF} and F_{PTAT} to generate a binary temperature code.

Special design considerations have to be taken to ensure the low power consumption (nano-Watt) of each block. The power consumption of the proposed temperature sensor is mainly influenced

by the temperature sensing unit. The range of the generated voltages V_{PTAT} and V_{REF} defines the range of oscillation frequency that directly affects the dynamic power consumption of the digital logic. Therefore, it's critical to have a strictly defined range for the generated voltages in all the process, temperature, and supply corners.

6.2 Temperature Sensing Unit

The temperature sensing unit outputs V_{PTAT} and V_{REF} voltages. Fig. 6.0.2 shows a conventional way to generate such voltages using a couple of current sources and resistors. In this scheme, the current is copied from a current generator to a resistor to generate corresponding voltages. The approach is simple but has drawbacks associated with it. To achieve a low-power operation, a low frequency of VCO is desired. For this, the control voltage of the VCO is required to be low (~ 200 mv). If the current source is producing < 10 nA range of current leading the resistor to be very large (> 5 MΩ), minimizing the resistor size will require a high current from the current source. Thus, the implementation poses a challenge in eliminating constraints on either power or area.
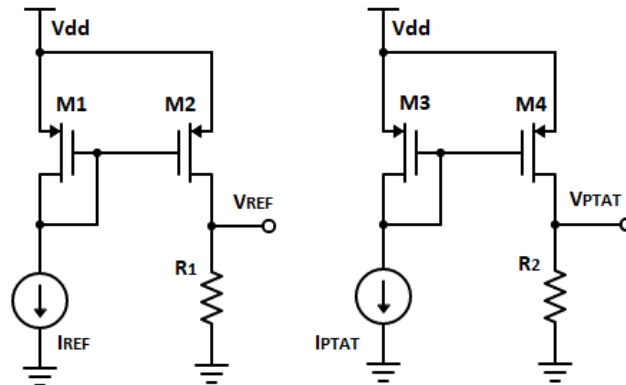
Fig. 6.0.2 Conventional method to generate voltages from a current source.

Another challenge in this approach is that the linear nature of the resistor will require the current source to have well-defined PVT dependencies. We will need two different current sources having different temperature dependencies to generate V_{PTAT} and V_{REF}, therefore, increasing the design

complexity and putting further strain on area and power. To minimize the design complexity, power consumption, and area requirement, we propose a resistorless design as shown in Fig. 6.0.3. The design uses only one current source having a square dependency on temperature $(PTAT)^2$. The voltage is generated by copying the current to a branch having a diode-connected MOSFET. The square nature of the current to the absolute temperature is used to compensate for second-order non-linear temperature dependencies of diode voltage drops. Using the nonlinear compensation and tweaking of the parameters of the MOS diode operating in the subthreshold region, a linear V_{PTAT}, and a stable V_{REF} can be synthesized. The proposed design can potentially decrease power consumption by 25% (eliminating one of the four current carrying branches) and eliminate the need for bulky resistors (saving chip area). The diode-connected MOSFET used to generate control voltages will enhance their supply sensitivity. Because the design uses the same current source to generate V_{PTAT} and V_{REF}, both control voltages will have identical process variations that can easily be canceled out later in the frequency-to-digital converter logic.
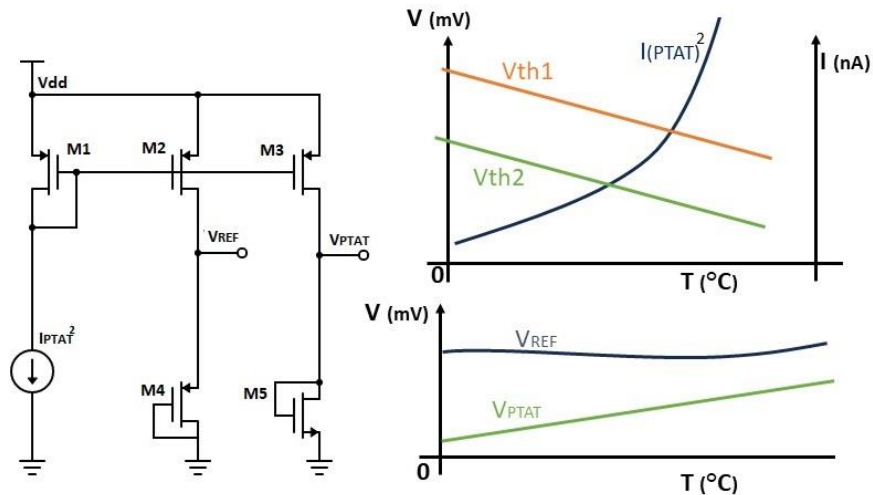
Fig. 6.0.3 Proposed resistor-less structure to generate PTAT and reference voltages from a $PTAT^2$ current source.

PTAT and Reference Voltage Generation

As mentioned in the previous section, the voltages V_{PTAT} and V_{REF} are generated by passing a bias current (I_D) through a diode-connected MOSFET operating in the subthreshold region. The drain current of a diode-connected MOSFET in subthreshold is expressed as [68]:

$$I_D = \frac{W}{L} \mu C_{ox} V_T^2 \, exp \left(\frac{V_{GS}-V_{TH}}{\eta V_T} \right) [1 - exp \left(\frac{V_{DS}}{V_T} \right)] \tag{31}$$

where W/L is the width-to-length ratio of the MOSFET, μ is the electron mobility, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area, t_{ox} is the oxide thickness and ε_{ox} is the oxide permittivity. V_T is the thermal voltage, which is denoted by $V_T = KT/q$, where K is the Boltzmann Constant, T temperature, and q charge of an electron. V_{GS} denotes the gate-source voltage of the MOSFET, V_{TH} is the threshold voltage of the MOSFET, and η is the subthreshold slope factor. V_{DS} is the drain-to-source voltage drop.

The size of the MOSFET is kept such that $V_{DS} \geq 4V_T$, which is necessary to keep a subthreshold MOSFET in saturation. Setting $V_{DS} \geq 4V_T$, (31) can be solved and expressed in terms of V_{GS} (MOS diode drop) as:

$$V_{GS} = \eta \, V_T \, ln \left[\frac{I_D}{\left(\frac{W}{L} \right) \mu C_{ox} V_T^2} \right] + V_{TH} \tag{32}$$

In (32) V_T has a positive temperature coefficient (TC) while μ and V_{TH} have a negative TC. These temperature-dependent coefficients can set the temperature behavior of the diode drop if the I_D is of the form:

$$I_D = \beta \mu C_{ox} V_T^2 \tag{33}$$

where β is an arbitrary variable. It can be seen that the mobility is canceled out, that is a process/temperature term and as a result, better process tolerance is achieved. Note that the current

I_D in (33) should have a square dependency on the temperature to effectively cancel out the nonlinear term in (32). Substituting (33) in (32) gives:

$$V_{DS} = V_{GS} = \eta V_T \ln\left(\frac{\beta}{W/_L}\right) + V_{TH} \tag{34}$$

The value of the β variable, the sizing, and the choice of the MOS diode with a suitable temperature dependence can be used to generate V_{PTAT} and V_{REF} as illustrated in Fig. 6.0.3. The value of the subthreshold slope factor (η) is about 1.3, and the thermal voltage V_T has a well-defined temperature coefficient (TC) of 0.086 mV/K. The threshold voltages (V_{TH}) have a negative TC of −4 to −2 mV/K, which varies from device to device. The temperature coefficient of V_T is significantly weaker than that of V_{TH} thus to compensate for the negative TC of V_{TH} a high value of the β/(W/L) >> 1 is needed. After determining the MOSFET size and value of β of the current source, an appropriate choice of MOS diodes will be used to generate V_{PTAT} and V_{REF}. A PMOS diode tends to have a more significant temperature dependence in terms of V_{TH} compared to the NMOS diode; hence a PMOS diode will be used to generate V_{REF}, and an NMOS diode will be used to generate V_{PTAT}. V_{TH} is the only process-dependent term remaining in (34), but since both the V_{PTAT} and V_{REF} will be simultaneously influenced by this variation it can easily be nullified in the digital logic when comparing the frequencies of their VCOs.

Current Source Design

As we established by the mathematical representation in (33), we require a current source that has a square dependency on the absolute temperature. The current source must be self-biased, low voltage, and immune to supply variation. To meet all those requirements, we present the design of a current source based on Oguey's topology. The design has been optimized to improve the power

supply rejection ratio (PSRR). The Oguey current reference [67] is based on a PTAT current source shown in Fig. 6.0.4.
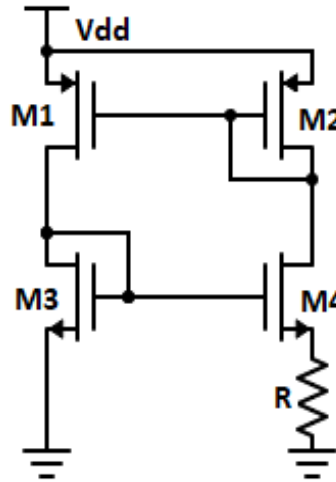
Fig. 6.0.4 A simple self-biased PTAT current source circuit.

 The design achieves low-power operation by keeping M_3 and M_4 in the subthreshold region. M_1 and M_2 act as current mirrors. The voltage drop across the resistor determines the magnitude of the current which is given by:

$$V_{S4} = V_T \ln\left(\frac{k_4 k_1}{k_3 k_2}\right) \tag{35}$$

where V_T is the thermal voltage and k_1, k_2, k_3 and k_4 are dimensions (W/L) of the MOSFETs respectively. It shows that the voltage drop across the resistor is PTAT because of its dependence on thermal voltages. The voltage remains insensitive to supply variation as long as the voltage drop across M_3 remains greater than $4V_T$, keeping M_3 and M_4 in saturation. Oguey eliminates a major drawback from the design by replacing the resistor with a MOSFET (M_5) working in the triode region (linear region). A branch is introduced in the circuit to supply bias M_5, as shown in Fig. 6.0.5.
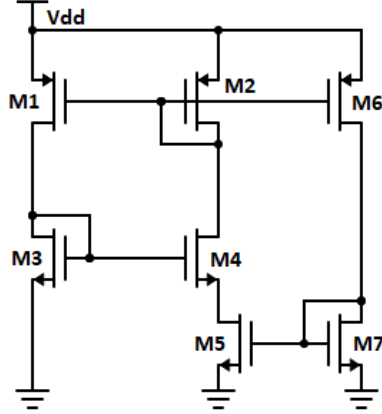
Fig. 6.0.5 Oguey Current reference circuit to generate low power PTAT current.

M_5 determines the bias current I_D, which is kept in the deep-triode region (i.e., the V_{DS} of M_5 is much less than its overdrive voltage ($V_{GS}-V_{TH}$). The current flowing in M_5 can be expressed as:

$$I_D = \mu C_{ox} k_5 \left[(V_{G5} - V_{TH5}) V_{DS5} - \frac{1}{2} - V_{DS}^2 \right] \tag{36}$$

and the voltage $V_{DS5} = V_{GS3} - V_{GS4}$ can be expressed as:

$$V_{DS5} = \eta V_T \, ln \left(\frac{k_4}{k_3} \right) \tag{37}$$

Where K_n is the W/L ratio of the nth MOSFET. The MOSFET M_7 is diode-connected and operates in saturation. Its current can be expressed as:

$$I_{D7} = \frac{1}{2} \mu C_{ox} k_7 (V_{TH} - V_{TH})^2 \tag{38}$$

Equations (36), (37), and (38) can be solved to give the current I_D as:

$$I_D = \frac{1}{2} \mu C_{ox} k_7 V_T^2 K_{eff} \tag{39}$$

80

With:

$$K_{eff} = \left[S_2 - \frac{1}{2} + \sqrt{S_2(S_2 - 1)} \right] ln^2(S_1) \tag{40}$$

Where:

$$S_1 = \frac{k_4}{k_3} \quad , \quad S_1 = Q\frac{k_5}{k_7} \tag{41}$$

The current ID in (39) is proportional to the square of absolute temperature and the electron mobility (μ), which meets all the requirements of I_D shown in (33). The factor Keff is a function of device sizes and, therefore, can easily be adjusted. The complete design of the proposed temperature sensing unit is shown in Fig. 6.0.6
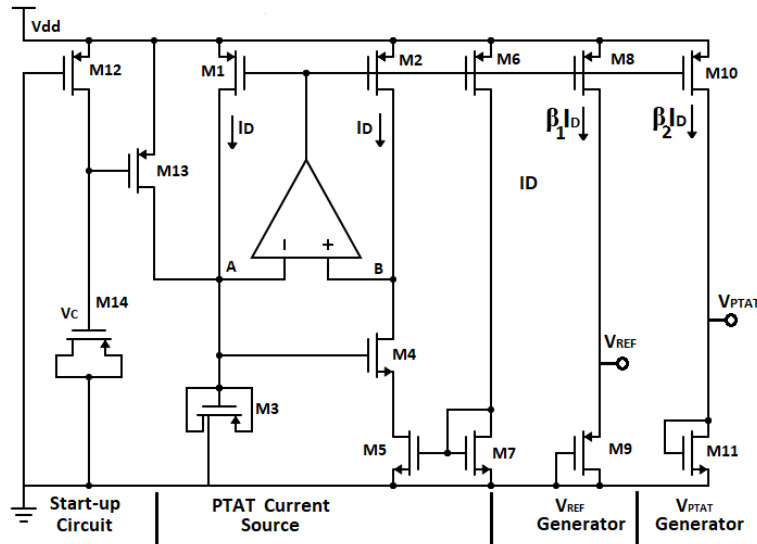
Fig. 6.0.6 . Complete design of the proposed temperature sensing unit.

Keeping the NMOS pair (M3 and M4) in the subthreshold region is crucial to ensure insensitivity to supply variation. We propose modifying the Oguey current source to improve the supply rejection by actively controlling the voltage of nodes A and B as shown in Fig. 6.0.6. An operational transconductance amplifier (OTA) is used to form a closed loop around nodes A and

B with V_{DD}[73]. The OTA gets its bias current from the same current generator block. The OTA is biased at only 2.5 nA to keep the power consumption low. The OTA controls the voltages of nodes A and B so that the change in supply voltage can be directed to the drain-source voltages of M_1 and M_2 keeping a constant drop across the M_3 and M_4. When the V_{DD} variation causes the voltage of node B to increase, the input to the non-inverting terminal of the OTA increases, which causes the output of the OTA to rise. This increase in the output of the OTA decreases V_{GS2} and causes an increase in V_{DS2}, and the voltage of node B would fall again and vice versa. It can also be seen in Fig. 6.0.6 that the OTA creates a virtual short between nodes A and B. These nodes define V_{DS2}, and thus, virtual shorting together the drain and source terminal of M_4 makes it diode-connected keeping it in saturation. Node A, however, is connected to the inverting terminal of the OTA and doesn't benefit from the closed loop. To improve the line sensitivity of node A, another modification is done by replacing the diode-connected MOS (M_3) with PMOS-based N-Well diodes. The N-Well diodes are formed by connecting the drain, source, and gate terminal of M_3 and utilizing the P-N junctions formed between the N-well (body connection) and the source/drain terminals of the PMOS, as shown in Fig. 6.0.7 . As compared to the original diode-connected MOS in the Oguey current source, the N-Well diodes formed in M_3 exhibit a superior voltage regulation across it [28]. By keeping a constant voltage drop at node A, the overall line sensitivity of the generated current is improved. The channel length of the PMOS current mirrors (M_1, M_2, M_6, M_8, and M_{10}) are kept long to have a high output impedance that provides passive immunity to supply variation, and using long channel length prevents second-order effects like channel length modulation.
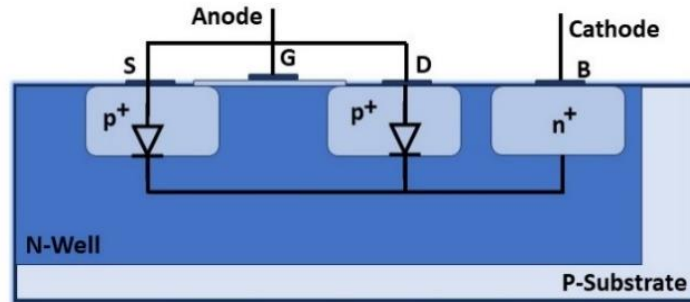
Fig. 6.0.7 N-well diodes formation.

The current source is self-biased, so during the power-up, the circuit can settle in two possible stable states. One of the stable states is when the bias current I_D is zero while the other possible state is when I_D is of the form in (**39**. A start-up circuit is introduced in the modified source to prevent the zero-bias current state, as shown in Fig. 6.0.6 . The start-up circuit is simple and comprises M_{12}, M_{13}, and M_{14}. M_{14} is connected in a MOS-CAP configuration and serves as a delay element keeping M_{12} and M_{13} from turning off during the startup. At startup (t = 0), the node voltage VC is zero and transistors M_{12} and M_{13} are ON in strong inversion. The MOS-CAP M_{14} starts charging through M_{12} until its voltage reaches up to the supply voltage V_{DD}, causing M_{12} and M_{13} to eventually turn OFF. During startup, M_{13} ensures that the current source is in a stable state with a finite current flowing in its branches. The start-up circuit consumes power only during a short duration of start-up time. Fig. 6.0.8 and Fig. 6.0.9 show the simulation results of V_{REF} and V_{PTAT} across the process corners. The sensing unit consumes 15 nW at 25°C and achieves a low variability across process corners. A Monte Carlo simulation of 1000 samples reveals a mean V_{REF} of 585.5 mV with a standard deviation of 2.63 mV in Fig. 6.0.10.
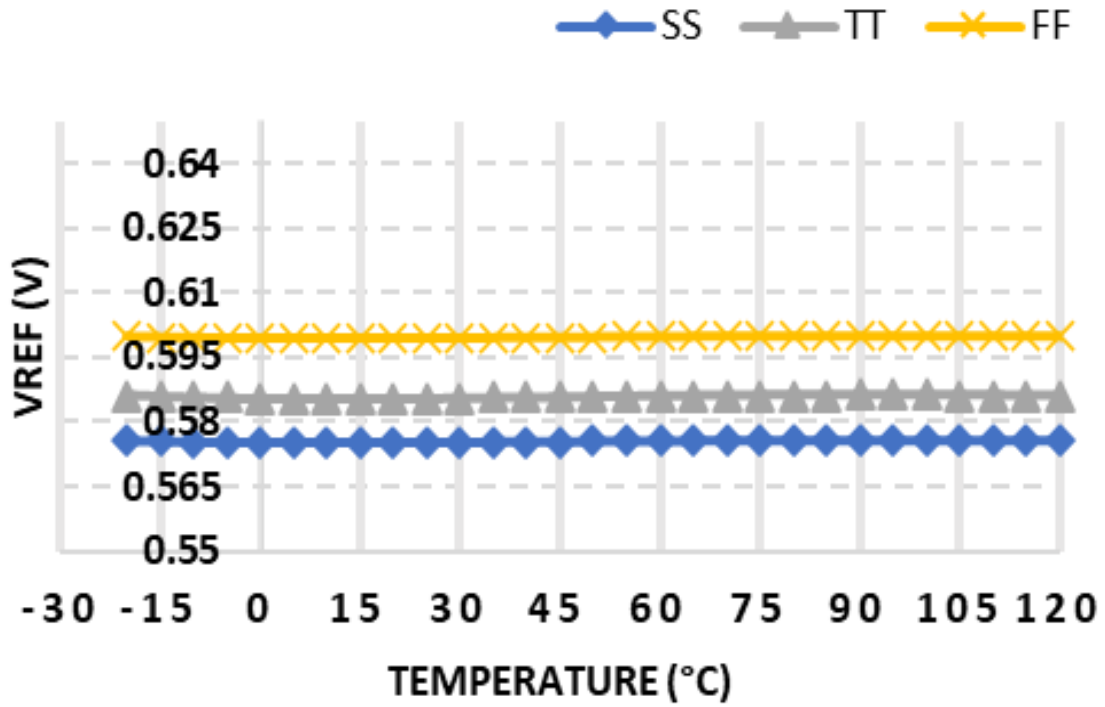
Fig. 6.0.8 Simulation results of V_{REF} across the process corners.
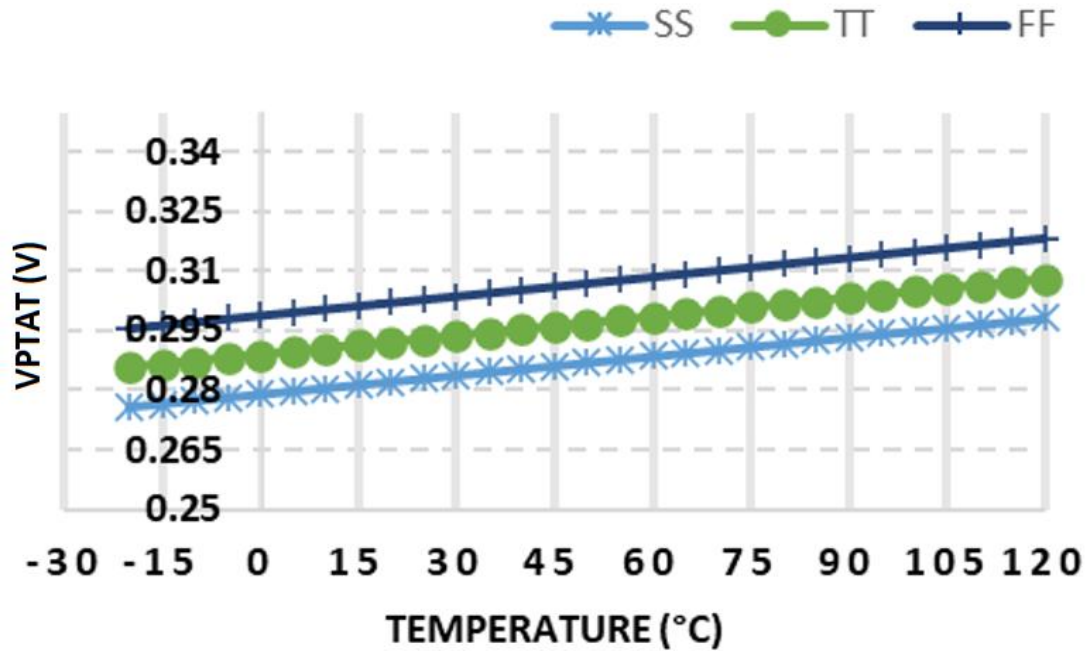
Fig. 6.0.9 Simulation results of VPTAT across the process corners.
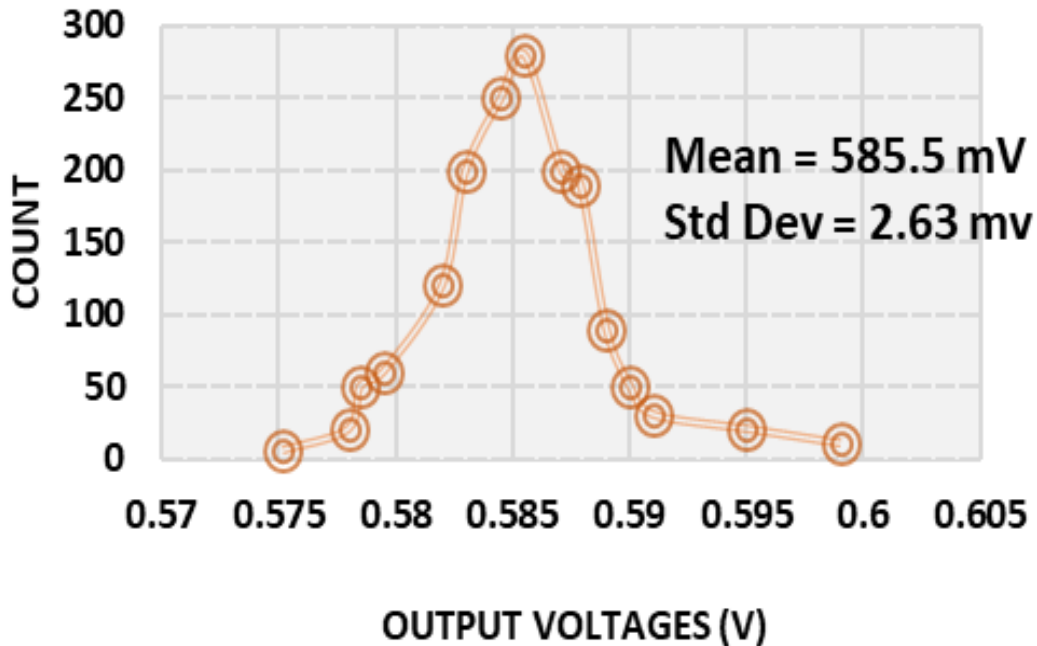
Fig. 6.0.10 Monte Carlo simulation of 1000 samples for the V_{REF} generator.

6.3 Voltage-To-Frequency Converter

The voltages from the temperature sensing unit are translated into frequency using a voltage-controlled ring oscillator (VCO). The design of the differential delay element for the proposed VCO is shown in Fig. 6.0.11. Instead of relying on a conventional approach of using an inverter as a delay element, our work proposes a new differential pair to control the frequency of the ring oscillator. In our approach, the tail current and an extra active load are varied using the control voltage. This variation provides better control and a wide frequency variation with a small change in control voltages. Differential circuits provide good rejection of common-mode supply and substrate noise. Noise sensitivity is a crucial aspect of the design of our temperature sensor; hence, the differential structure of the delay element is a preferable choice to improve noise immunity. In addition to being noise-tolerant, differential ring oscillators also let us employ an even number of stages in the oscillator's loop. If we want oscillations using single-ended inverters, the stages have

85

to be in odd numbers. However, in the differential structure, we can obtain the extra inversion by simply crossing the outputs of a single stage.
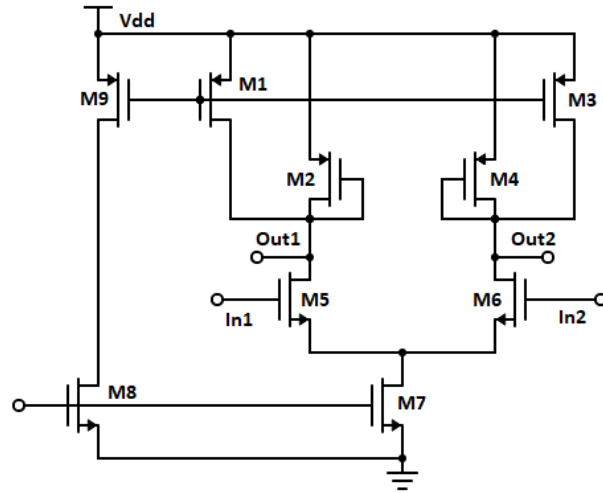
Fig. 6.0.11 Design of the differential delay element for proposed VCO.
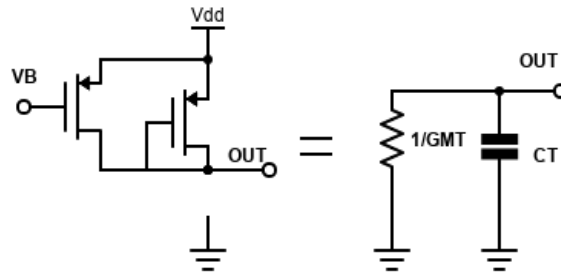
Fig. 6.0.12 Simplified RC model approximation of the differential delay cell.

As shown in Fig. 6.0.12, the propagation delay (t_d) of a single differential stage can be estimated using a simple RC model. The simple RC model is driven from the half-circuit small-signal model during the Low-to-High transition, and it can be mathematically expressed as:

$$t_d = C_T R_T \tag{42}$$

With,

$$R_T = \frac{1}{G_m} = \frac{1}{g_{m1} + g_{m2}} \tag{43}$$

$$t_d = \frac{C_T}{G_m} \tag{44}$$

Where C_T is the total load capacitance seen by the output of a stage (including parasitic capacitances), gm_1 and gm_2 are the transconductance of M_1 and M_2, respectively. It can be noted that variation of the active load M1 using the control voltages changes the delay of each stage. The time it takes for a single transition to propagate twice around the ring of the oscillator determines its oscillation frequency. From [74] the frequency of oscillation F_{OSC} can be expressed as:

$$F_{OSC} = \frac{1}{2Nt_d} = \frac{G_m}{2NC_T} \tag{45}$$

The outputs V_{PTAT} and V_{REF} from the sensing unit will control the frequency of their respective ring oscillators, giving us F_{PTAT} and F_{REF}. It can be noted that the delay of the differential stage depends on transconductance (G_m), and G_m is sensitive to both temperature and supply voltage. The ring oscillator shows a simulated supply sensitivity of $+1.7$ to $-2.8\ °C$ across a supply variation of 1 to 1.4 V. However, since both VCOs have identical structures, their supply and temperature sensitivity are minimized by comparing their frequencies in the digital section. The temperature sensing accuracy may also suffer due to process variation; therefore, careful layout considerations are adopted to minimize this variation. Long-channel devices are used along with common centroid layouts to improve mismatches.

6.4 Frequency-to-Digital Conversion Logic

A digital logic circuit is designed to convert the frequencies F_{PTAT} and F_{REF} into digital outputs using two asynchronous counters configured as 12-bit binary counters. F_{PTAT} and F_{REF} serve as the clock sources Clk_{PTAT} and Clk_{REF} for the PTAT- counter, and reference counter, respectively. The

frequencies are chosen such that the reference frequency is always greater than the PTAT frequency at all temperature, supply, and process corners. As shown in Fig. 6.0.13, the 'Setup' signal triggers the oscillation in both oscillators making the counters increment with each clock pulse. Since the reference frequency is higher, its counter overflows first and raises its 'overflow' signal. This overflow signal triggers the transfer of count from the PTAT counter to the parallel-to-serial converter. The 'Setup' signal again clears and start both the counters for a new set of temperature reading. At high temperatures, more counts are accumulated in the PTAT counter, and at low temperatures, the accumulated count is low. Hence, the PTAT count serves as the binary representation of the measured temperature. Conversion can be set to continuous mode using the internal 'Setup' signal, or to conserve power the conversion can be triggered from an external signal when needed. Circuit level optimization is done by carefully considering the device sizing in each switching stage of the counters to minimize short circuit currents and leakages. Capacitive loading of the counter is also minimized at the layout level to reduce the charging and discharging currents leading to efficient power consumption.
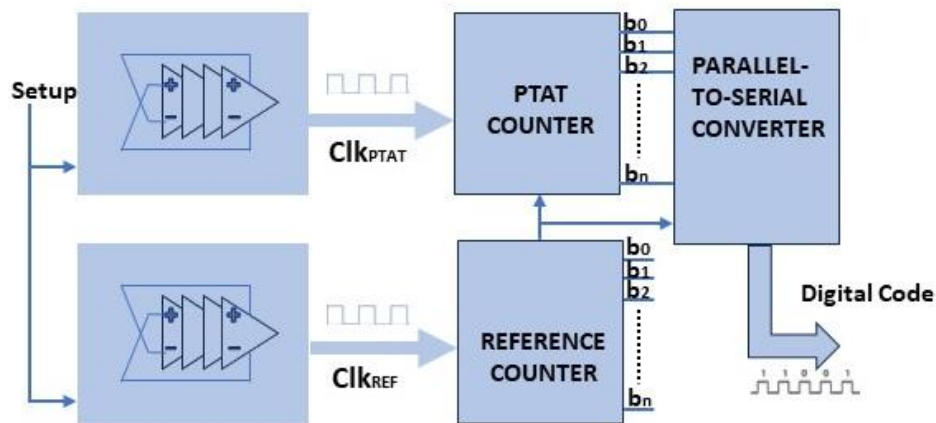
Fig. 6.0.13 Block Diagram of the counters and the proposed digital logic for data conversion.

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6.5 Experimental Results

The micrograph of the temperature sensor chip is shown in Fig. 6.0.14 . The design is fabricated

in a 65 nm CMOS process and occupies an area of 0.02 mm^2.
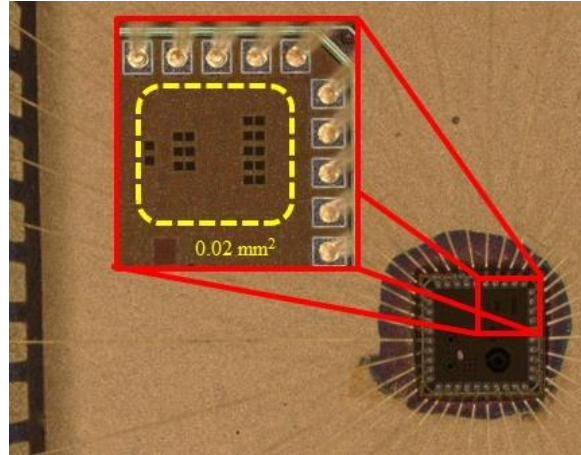
Fig. 6.0.14 Micrograph of the proposed temperature sensor.

The measurement setup is shown in Fig. 6.0.15. Twelve dies were selected and packaged in the

QFP package for testing the temperature sensor.
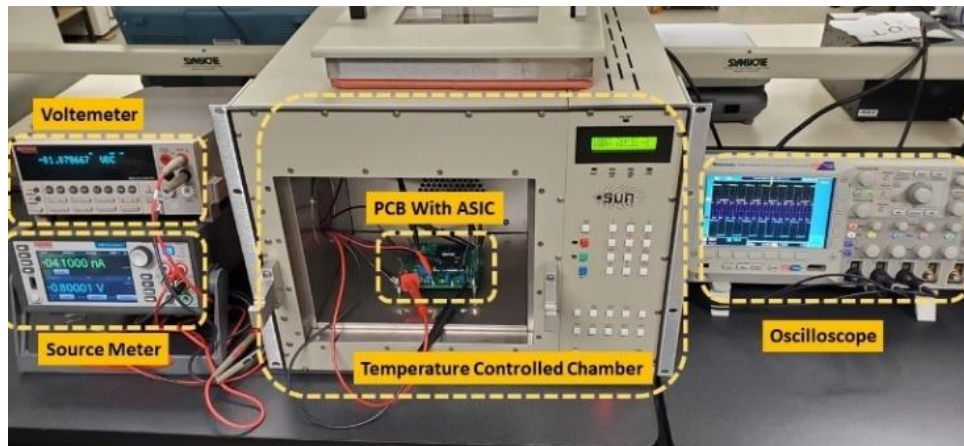
Fig. 6.0.15 Testing setup showing all the equipment used for testing and measurement.

Fig. 6.0.16 shows the output voltage V_{PTAT} over the range of −20 to 120 °C. The V_{PTAT} output

shows a linear output with minimal dependence on process variation. The average temperature

sensitivity of V_{PTAT} is measured to be 0.19 mV/°C. A mean value of 266.4 mV is observed at a

supply voltage of 0.8 V @ 25 °C with a standard deviation of 13.19 mV across samples. The output voltage V_{REF} is shown in Fig. 6.0.16. V_{REF} shows an average temperature sensitivity of 0.95 µV/°C, and a mean value of 601.5 mV is observed at 0.8 V supply @ 25 °C. V_{REF} shows a standard deviation of 25 mV across samples.
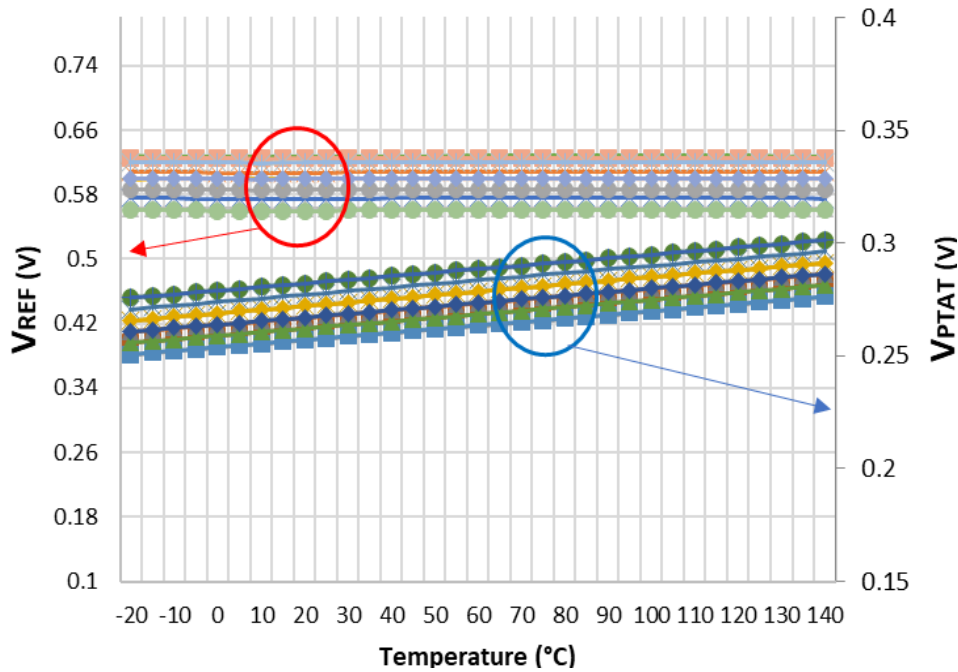
Fig. 6.0.16 Measured V_{REF} and V_{PTAT} across the temperature range.
The average power consumption of the sensing unit is measured to be 18 nW. The measured average F_{PTAT} varies from 168 KHz to 308 KHz across the temperature range, and the measured average F_{REF} is 442 KHz @ 25 °C as shown in Fig. 6.0.17. The average RMS resolution of the temperature sensor across samples was measured to be 0.2 °C$_{rms}$. A supply voltage change of 0.8-1.2 V produced an error of +1.5/−2.1 °C in the temperature measurement. Fig. 6.0.18 shows the measured error of 1.5 °C/−1.6 °C across the temperature range after 2-point calibration at 25 °C and 105 °C.

The average power consumption of the complete sensor over the 12 dies at ambient temperature and 0.8 V supply is 59 nW as shown in Fig. 6.0.19. The overall power breakdown is shown in Fig.

6.0.20, which shows that the ring oscillator accounts for about 50% of the power consumption while generating V_{REF} and V_{PTAT} consumes about 30% of the total power budget. Table 10 shows the comparison of the design with other low-power temperature sensors reported in the literature. The comparison is based on a figure of merit (FoM) derived from [75]. The proposed design shows a significantly better performance in terms of area, power consumption, and measurement error. A lower FoM means better performance and is calculated as follows:

$$FoM \left[\frac{nJ}{K^2}\right] = Energy/\ Conversion\ \times\ (Resolution)^2 \qquad (46)$$
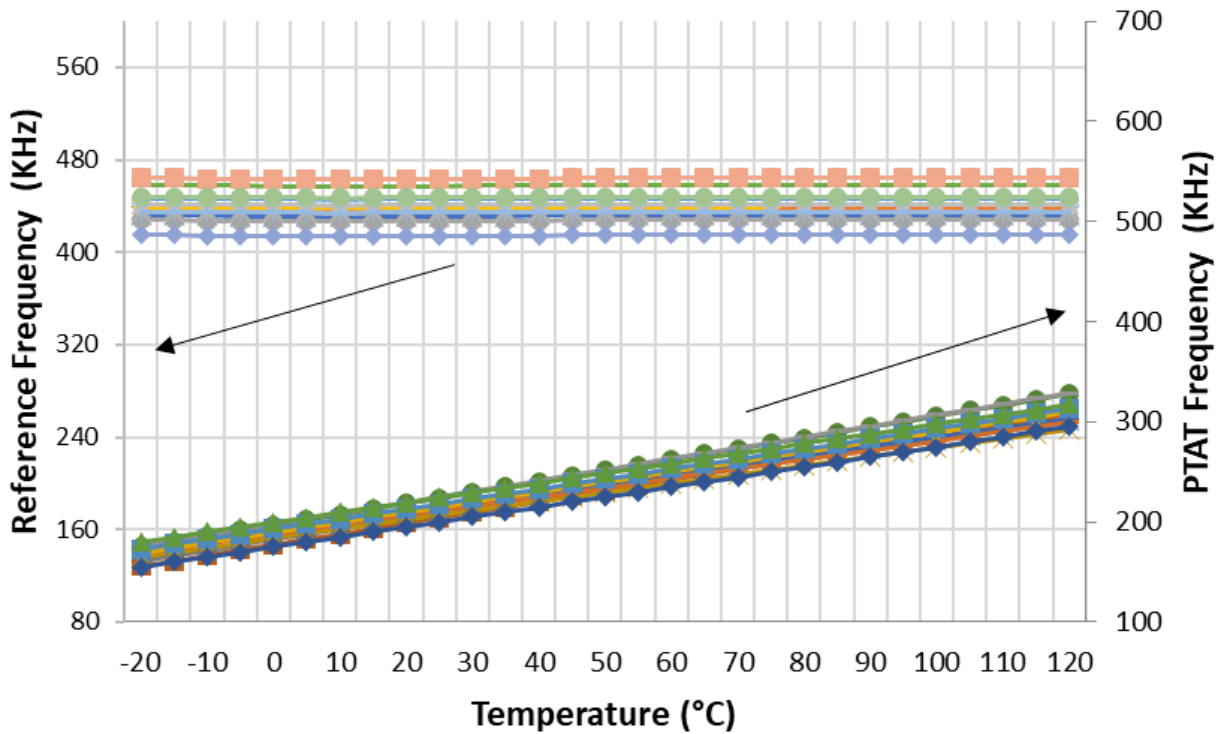
Fig. 6.0.17 Measured F$_{REF}$ and F$_{PTAT}$ across the temperature range.
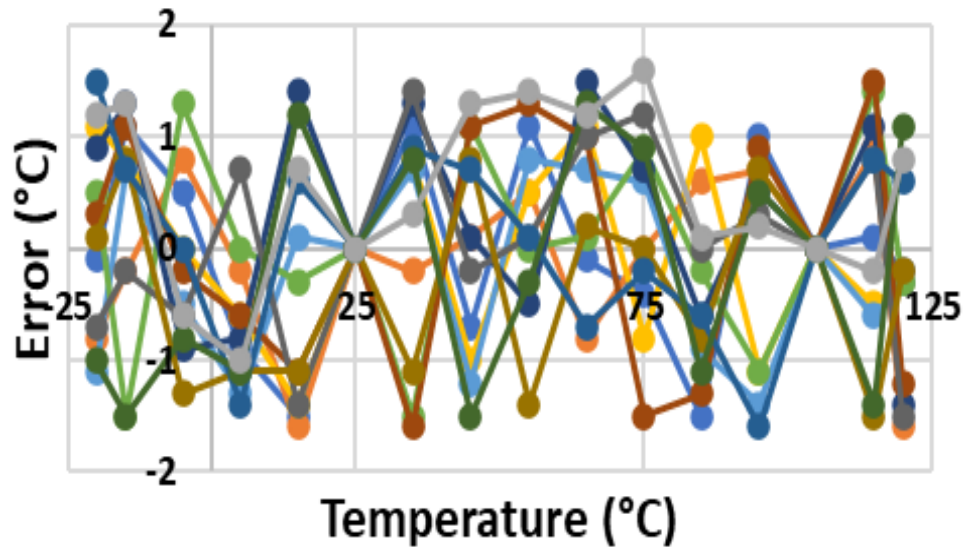
Fig. 6.0.18 Measured errors across all the tested samples with 2-point calibration.
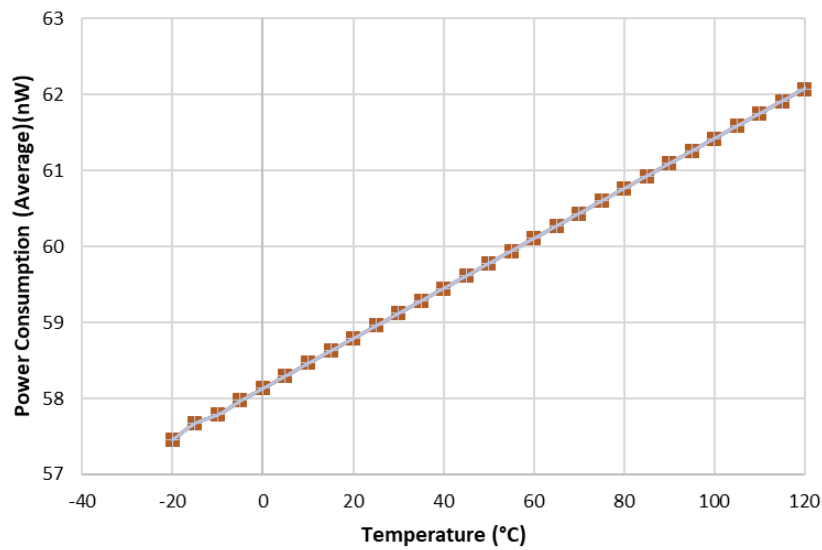
Fig. 6.0.19 The average measured power consumption of the proposed temperature sensor.
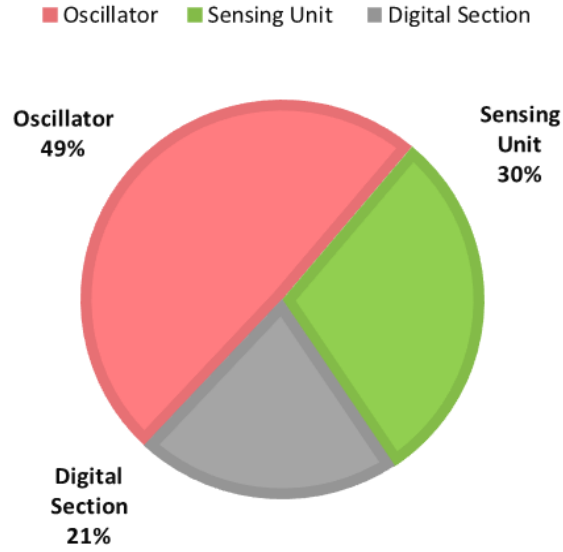
Fig. 6.0.20 Breakdown of the total power consumption among the main functional blocks.

Table 10 Comparison with The State-Of-The-Art

	This work	TCAS -I' 21 [76]	TCAS -II' 22 [77]	TCAS -II' 19 [78]	JSSC' 19 [79]	JSSC'16 [80]
Process	65nm	130nm	180nm	180nm	180nm	65nm
Type	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET
Area	$0.02\ mm^2$	$0.07\ mm^2$	$0.049\ mm^2$	$0.007\ mm^2$	$0.074\ mm^2$	$0.008\ mm^2$
Supply Range	0.8V	0.95V	0.35V	0.6- 1.2V	0.8V	1V
Temperature Range	−20-120 ºC	0-80 ºC	0-100 ºC	0-100ºC	−20-80 ºC	0-100 ºC
Resolution	$0.2\ ºC^{-1}$	$0.1\ ºC^{-1}$	$0.27\ ºC^{-1}$	$0.55ºC^{-1}$	$0.14ºC^{-1}$	$0.3ºC^{-1}$
Conversion time	9.2ms	59ms	33ms	300ms	839ms	0.022ms
Calibration points	2	2	2	2	2	2
Error	+1.5/−1.6 ºC	+0.44/−0.4 ºC	+3/−3 ºC	+0.67/−1.64 ºC	+1.2/−0.9 ºC	+0.9/−0.9 ºC
Fully Integrated	yes	yes	yes	yes	yes	yes
Power	60nW	196nW	14nW	3.92nW	11nW	154uW
Energy per Conversion	0.55nJ	11.56nJ	0.46nJ	1.2nJ	8.9nJ	3.4nJ
FOM [nJ.K^{-2}]	0.022	0.12	0.034	0.36	0.19	0.3

6.6 Conclusion

In this chapter, we demonstrated an ultra-low power temperature sensor that can be integrated into our battery-less wireless sensor node. The sensor achieves ultra-low power and area-efficient design by using a resistorless approach. Moreover, both the reference voltage and the temperature-sensitive voltages are derived from the same current source to improve process sensitivity. As a result, the sensor consumes only 60 nW at room temperature. The sensor operates on a temperature range of −20 to 120 °C and achieves an inaccuracy of +1.5/−1.6°C after 2- 2-point calibration. The design achieves a conversion rate of 108 samples/second and consumes 0.55 nJ/conversion. The proposed sensor will be integrated into a wireless sensor node to demonstrate its suitability.

CHAPTER 7 WSN INTEGRATION AND TESTING

7.1 Experimental Results of Full Integration

The WSN has been fabricated in Global Foundries 22nm FD-SOI technology. The complete die size is 5 mm^2 while the WSN circuits occupy an active area of only 0.107 mm^2 as shown in Fig. 7.0.1. Each major block is highlighted for clarity. The test PCB shown in Fig. 7.0.2 is designed on an FR-4 substrate, with a 0.8 mm thickness of PCB. The chip is wire-bonded directly on the PCB for testing. Measurements are done using Tektronix MD04104C mixed domain 0scilloscope, Tektronix AFG1062 arbitrary functions generator, Keysight FieldFox N9914B RF Analyzer 6.5 GHz, Sun Systems Temperature controlled chamber signal, 86471 RF Signal Generator, and a Keithley 2470 source meter.
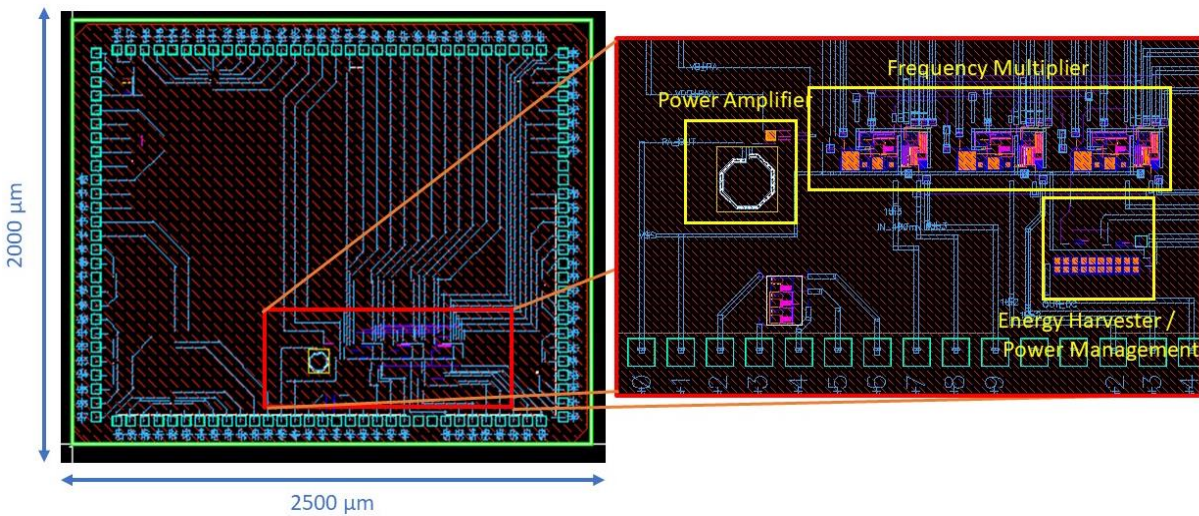
Fig. 7.0.1 Chip layout details
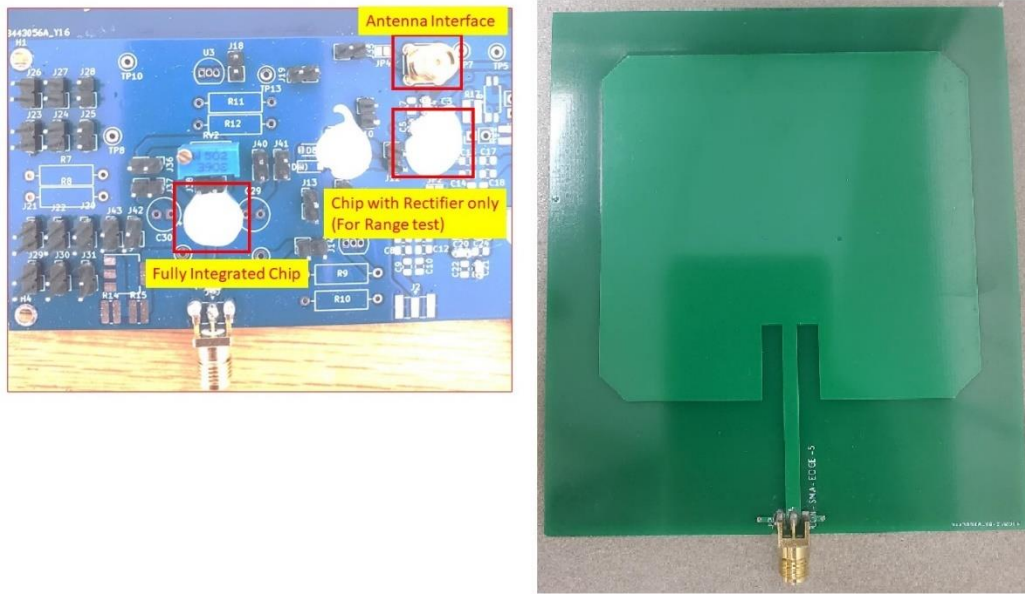
Fig. 7.0.2 Test PCB and the fabricated Patch Antenna

7.2 Calculating the Value of Storage Capacitor.

We measured the power consumption of each block of the sensing node in the lab setup before testing the WSN, to calculate the value of the Cstore, the total power consumption of the sensing node (during wireless data) can be estimated with some reasonable tolerances to be 700 µW. The measured breakdown of the total power consumption of the sensing node (including temperature sensors) is summarized in Table 11.

Table 11 Total estimated Power Consumption of the sensing node

Power Management	50 nW
Frequency synthesizer	160 µW
Power Amplifier	500 µW
Temperature Sensor	60 nW
Power consumption Total	~700 µW

The size of the storage capacitor can be calculated by revisiting equation (8) established in section 3.3, shown below.

$$C_{Store} = \frac{P_{supplied} \, x \, 2 \, T_{active}}{V_H^2 - V_L^2} \tag{47}$$

96

Since most of the power is consumed during the wireless data transmission the duration of this transmission is taken as T_{active} in our calculation. The 12-bit temperature sensor data modulates the 2.4 GHz carrier with a data rate of 0.5 Megabits per second, which requires an active transmission time of 24 µs. The value of $V_H = 1.6$ V, $V_L = 0.95$ V, total power consumption $= 700$ µW, and $T_{active} = 24$ µs is substituted in (47) to yield a storage Capacitor value of 84 nf. The experimental results in the next section are based on the choice of this capacitor value.

7.3 Energy Harvesting Testing

The energy harvesting performance is evaluated in free space by connecting the patch antenna (Shown in Fig. 7.0.2) with the RF Rectifier and placing it at an increasing distance from a dedicated wireless energy source. For the wireless source, we used TX91503 transmitter with 3W Effective Isotropic Radiated Power (EIRP). The output of the rectifier is connected to the storage capacitor (Cstore = 80 nf) without power management for this experiment. Fig. 7.0.3 illustrates the measured data points with respect to the distance from the source. The transmitter is attached to the tripod and placed in the lab corridor for a line of site measurement.
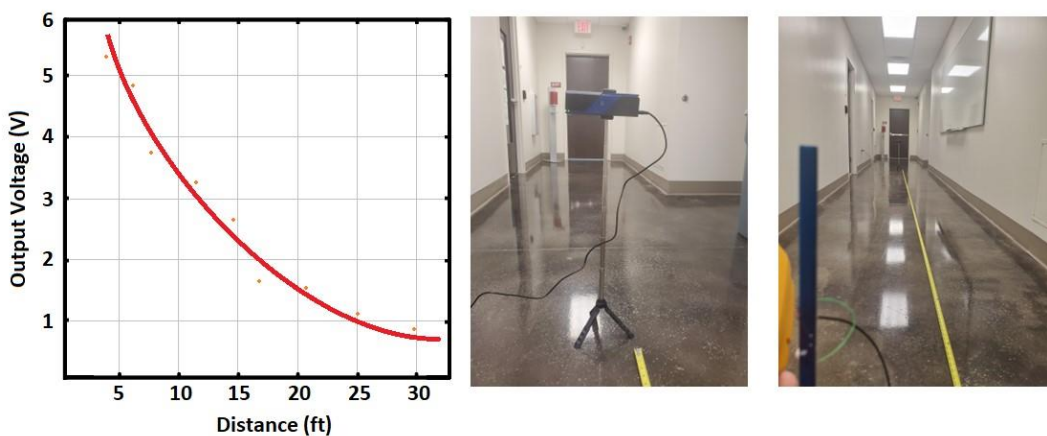
Fig. 7.0.3 Output Voltage (fitted curve) vs distance measurement in free space when power with a dedicated wireless source.

The energy harvester achieved 1 V in the output at about 25 ft from the source. Since the transmitted waves can get absorbed in the walls and roof of the corridor it's difficult to establish the range and sensitivity of the energy harvester in open space without the use of an RF power detector in the close vicinity of the energy harvester. Therefore, we decided to measure the performance of the rectifier with a 50Ω signal generator. The output and the power conversion efficiency under different load conditions are measured as shown in Fig. 7.0.4.
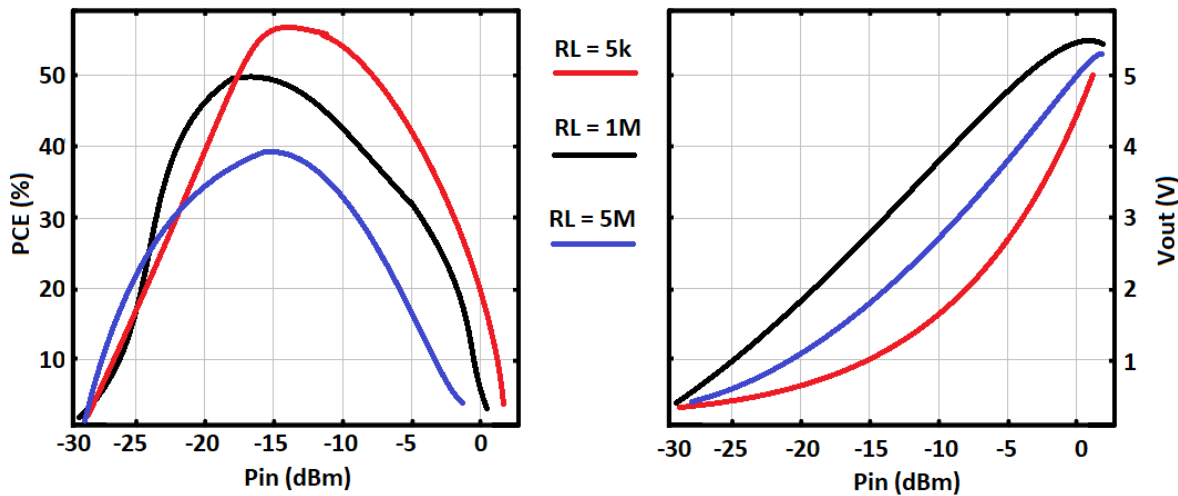
Fig. 7.0.4 Measured output and PCE for different resistors at output vs Pin

The power conversion efficiency shows an inverse correlation with the output voltage. The rectifier achieves 57 % PCE at 5KΩ load at -14 dBm input power, while maximum voltages are achieved in low load conditions.

7.4 Full Integration Testing

The full integration of the WSN was tested in the lab setup. For reliability and stability of the testing results a -15 dBm 915 MHz RF input is given to the WSN through an RF signal generator. In the first test, to ensure a 50% probability of '0' and '1' in the data, a 50% clock signal of 500 KHz (0.5 MBps) is given as the input to the OOK modulator of the wireless data transmission circuit. Another signal generator along with some digital logic gates is used to emulate the 9 ms

conversion time of the temperature sensor. The output of the WSN transmitter with and without OOK modulation is observed on a spectrum analyzer as shown in Fig. 7.0.5. The output power is observed at -3.8 dBm and -3.56 dBm for modulated and unmodulated TX respectively. The degradation of output power in the modulated output is due to the spread of the power in the sidebands. The total power consumed by the sensing node during active phase (@ -3.8 dBm) is 750 µW, resulting in a power efficiency of 55 %.
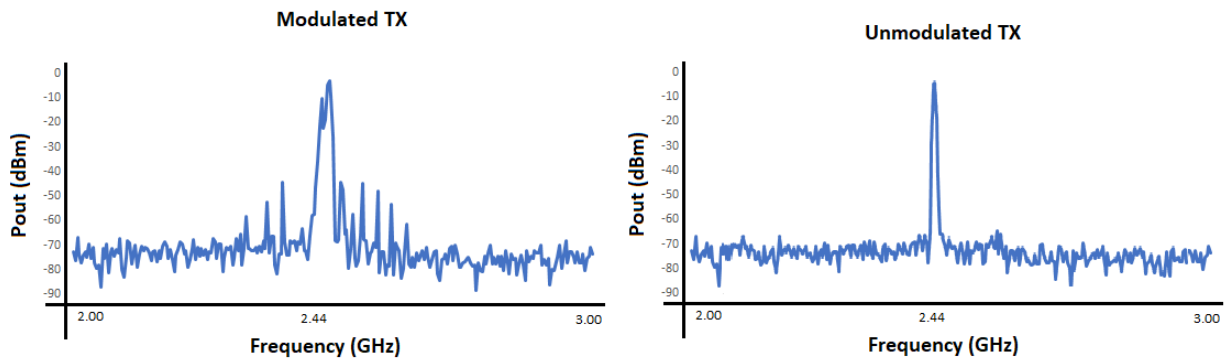
Fig. 7.0.5 Measured output spectrum of the RF transmitter in WSN in modulated and unmodulated conditions.

Fig. 7.0.6 shows the discharging voltage of V_{store} from V_H to V_L during the active transmission phase of about 28 µs.
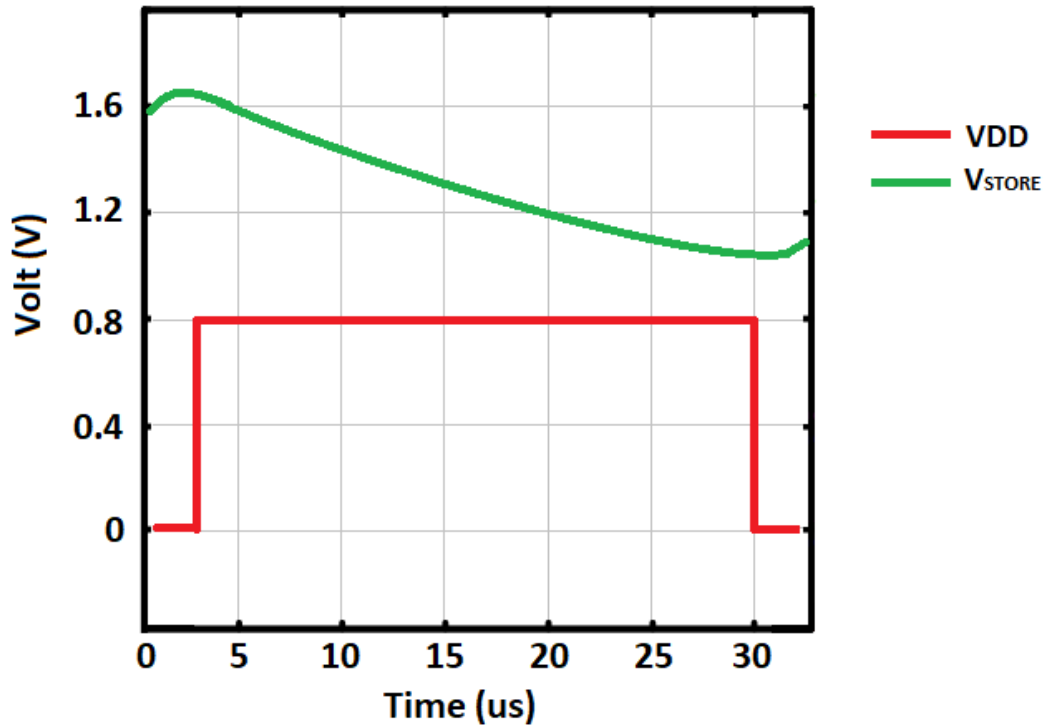
Fig. 7.0.6 Waveforms of Vstore and VDD during the active time

The temperature sensor was tested after integration in the WSN. The measurement results show a temperature measurement inaccuracy of 0.9 °C at room temperature.

7.5 Performance Comparison with Previous Work

The performance of the proposed WSN is compared with previous works and is summarized in Table 12. Our work demonstrates an extremely area-efficient design with an on-chip area of 0.107 mm². Among the prior works, only the design in [83] features a smaller die area. However, that work relies on resonant cavity-based wireless power transfer (WPT) and achieves a low efficiency of 11.5% @-11 dBm. In contrast, our design achieves an excellent power conversion efficiency of 57% @ -14 dBm with a sensitivity of -25 dB due to efficient rectifier design minimizing the leakages, which is comparable to -23 dB in [81] but exceptionally lower than [82], [83]and [84]. Moreover, if necessary, the sensitivity can be further enhanced by incorporating more rectifying

stages but at the cost of charging time. The proposed transmitter WSN exhibits a relatively low data rate which is limited only due to the low data rate of the implemented temperature sensor, the data rate can be optimized for different applications. Our work demonstrates an exceptional TX output power (-3.8 dBm) and a power efficiency of 55 % because of the ultra-low power design of the DLL and power management system. To compare our work with previous implementations of WSNs we have established a figure of merit (FoM) formulated as:

$$\boldsymbol{FoM} = \boldsymbol{10\ log\frac{A}{L_{min}^2} + 10\log(\frac{E_{bit}}{E_{bit,max}}) + 100\ x\ 10\ log\frac{100 + Ps}{100 + P_{TX}} - PE} \tag{48}$$

$$\boldsymbol{FoM = FoM_1 + FoM_2 + 100\ x\ FoM_3 - FoM_4} \tag{49}$$

Where A is the active on-chip area of the WSN, L_{min} is the minimum device length, E_{bit} is the energy consumed per bit transmission, $E_{bit,max}$ is the reference value for normalization, P_S is the sensitivity, P_{TX} is the transmitted power and P_E is the power efficiency of the WSN. The overall Figure of Merit (FoM) comprises four distinct FoMs, each addressing specific design aspects. It is important to note that a lower FoM indicates a better performance. FoM_1 primarily considers technology-dependent parameters, where a larger active area contributes to a higher FoM, and a shorter channel length also weakens the FoM. This approach ensures a fair comparison among different processes by accounting for these influential factors. FoM_2 is the normalized Energy consumed per bit and focuses on the energy consumption and data rate aspects of the WSN. The normalization process involves dividing the energy per bit by the maximum reported energy per bit from prior works. This normalization allows for a comparative analysis that accounts for varying data rates observed across different works. FoM_3 holds major significance as it determines the operational range of the WSN concerning the energy harvesting distance and data transmission range. Sensitivity sets the maximum distance achievable between the WSN and the RF energy source. Meanwhile, the transmission power sets the data transmission range of the WSN. The

magnitude of FoM$_3$ is relatively small; therefore, it's multiplied by 100 to amplify its influence on the overall FoM since other factors typically fall within a similar range of magnitude. FoM$_4$ is the power efficiency of the WSN expressed in percentage.

Table 12 Performance Comparison with Previous Work

	This work	JIOT '22 [81]	TCAS -I' 20 [82]	TCAS -II' 21 [83]	TMTT' 21 [84]
Process Technology	22 nm FDSOI	130 nm CMOS	180 nm CMOS	180 nm CMOS	180 nm CMOS
Area	0.107 mm^2	0.45 mm^2	0.249 mm^2	0.078 mm^2	11.5 mm^2
Frequency	915 MHz/2.44 GHz	915 MHz/2.45 GHz	868 MHz/6-8.8 GHz	434 MHz/2.4 GHz	2.4 GHz /2.4 GHz
Sensitivity	-25 dBm	-23 dBm	-18.8 dBm	-11.56 dBm	-10 dBm
TX Data rate	0.5 Mbps (00K)	20 Mbps (00K)	0.00512 Mbps (UWB)	10 Mbps (OOK/FSK)	NA
TX output power	-3.8 dBm	-11 dBm	-42 dBm	-33 dBm	-10 dBm
Power Efficiency	55%	51%	7.5%	0.7%	25%
Rectifier PCE	57% (@-14 dBm)	NA	NA	11.5% (-11 dBm)	53.8% (@-14 dBm)
Power Active(μW)	700	1368	164	70	7200
FoM$_1$	83.4	74.3	68.9	63.8	85.5
FoM$_2$	-13.59	-16.7	0	-36.6	NA
100 x FoM$_3$	-108.1	-62.89	146.12	120.57	0
FoM$_4$	55	51	7.5	0.7	25
FoM	-93.29	-56.29	-84.72	147	60.5

7.6 Conclusion

This work presented an RF-powered wireless temperature sensor nod using 22nm FDSOI technology working in the ISM band. The circuit consists of an RF energy harvesting module,

implemented with a multi-stage RF Dickson rectifier, a PMC unit, and a DLL-based frequency synthesizer for RF carrier generation. The frequency multiplier synthesizes the RF carrier for transmission by utilizing the RF input signal as a reference frequency, eliminating the need for a local oscillator. This approach results in a highly integrated and cost-effective wireless sensor node. The receiver supports a 915-MHz Frequency, and the transmitter works at 2.45-GHz utilizing On-Off Keying (OOK) for data modulation, achieving data rates of up to 0.5 Mbps. It achieves a remarkable power conversion efficiency of 55% at -14 dBm input power and it operates effectively with an extremely low RF input power of -25 dBm. The WSN demonstrated 55% power efficiency at a TX output power of -3.8 dBm utilizing a class E power amplifier.

CHAPTER 8 CONCLUSION AND FUTURE RECOMMENDATION

In this dissertation, an in-depth exploration of energy-efficient circuitry and low-power techniques was conducted, leading to the design and implementation of an autonomous RF-powered wireless sensor node. In this work, the interface between the energy harvester and the components of the sensor node is optimized to enhance power efficiency, sensitivity, and range of operation. A scalable interface with the sensor is implemented to enable the acquisition of data from diverse sensor types and ensure compatibility with standard protocols. The practical application showing real-world functionality and usability of the proposed wireless sensor node was demonstrated through the integration of an ultralow power temperature sensor. A comprehensive evaluation was undertaken to assess the advantages of employing RF as the primary power source in various indoor and outdoor settings. Moreover, the use of a dedicated RF source significantly enhanced the reliability, compactness, and overall power efficiency of the WSN design. The core focus of this work revolved around the optimization of circuit and system designs, specifically considering the requirements of RF-powered WSNs. Power management strategies are adopted in the design to minimize unnecessary transmission and efficiently utilize the available power.

8.1 Future Recommendations

Some suggestions for improved performance and efficiency of the WSN are listed in this section.

Antenna Design

Exploring advanced antenna designs customized for optimal energy harvesting, focusing on efficient radiation patterns and impedance matching, could further enhance the performance of RF-powered wireless sensor nodes. Investigating miniaturized and high-gain antenna configurations specifically suited for the ISM band can contribute to improved energy harvesting.

Power Efficiency

For increasing the global power efficiency of the WSN system, the energy efficiency design of WSN components such as the rectifier and power amplifier is crucial. Exploring novel circuit topologies, advanced semiconductor materials, and optimized layouts can potentially elevate efficiency levels, leading to better overall energy utilization and prolonged device operation.

Maximum Power Point Tracking (MPPT) in Rectifier Design

Integrating Maximum PowerPoint Tracking algorithms into the rectifier design can enhance energy extraction from varying RF input conditions. Investigating adaptive rectification techniques, possibly incorporating MPPT algorithms, can optimize power extraction, ensuring the system operates efficiently under changing environmental RF conditions.

Power Amplifier (PA) Design Optimization

Focus on refining the Power Amplifier design, potentially exploring class-E amplifier improvements, and exploring techniques to reduce power dissipation is needed. Investigating advanced PA architectures and switching techniques could lead to higher efficiency, reduced losses, and improved overall energy utilization.

On-chip Power-Efficient Oscillator Design

Developing on-chip power-efficient oscillators optimized for RF frequency carrier generation can improve performance, minimize power consumption, and enhance the stability of existing WSNs. Investigating low-power oscillator circuits, possibly leveraging innovative technologies like MEMS-based oscillators or digitally controlled oscillators, can contribute to innovative WSN design. By focusing on these areas, future research works can further enhance the efficiency,

reliability, and applicability of RF-powered sensor nodes, ensuring sustainable and robust wireless

sensing capabilities.

References

[1] M. Kocakulak and I. Butun, "An overview of Wireless Sensor Networks towards Internet of things," in *2017 IEEE 7th Annual Computing and Communication Workshop and Conference (CCWC)*, Jan. 2017, pp. 1–6. doi: 10.1109/CCWC.2017.7868374.

[2] A. A. Valenzuela, M. Schwab, A. A. Silnik, A. F. Debattista, and R. A. Kiessling, "Low Power Wireless Sensor Node Platform for Agriculture Monitoring in Argentina," in *2018 International Conference on Cyber-Enabled Distributed Computing and Knowledge Discovery (CyberC)*, Oct. 2018, pp. 101–1014. doi: 10.1109/CyberC.2018.00029.

[3] Y. Hu *et al.*, "Event-driven wireless temperature sensor networks powered by air-flow based nanogenerator," in *2017 IEEE 12th International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*, Apr. 2017, pp. 410–413. doi: 10.1109/NEMS.2017.8017053.

[4] D. Bhattacharyya, T. Kim, and S. Pal, "A Comparative Study of Wireless Sensor Networks and Their Routing Protocols," *Sensors*, vol. 10, no. 12, Art. no. 12, Dec. 2010, doi: 10.3390/s101210506.

[5] S. You, J. K. Eshraghian, H. C. Iu, and K. Cho, "Low-Power Wireless Sensor Network Using Fine-Grain Control of Sensor Module Power Mode," *Sensors*, vol. 21, no. 9, Art. no. 9, Jan. 2021, doi: 10.3390/s21093198.

[6] D. Sharma, K. Kavitha, and R. Gururaj, "Estimating Node Density for Redundant Sensors in Wireless Sensor Network," *Sensor Netw Data Commun*, vol. 04, no. 02, 2015, doi: 10.4172/2090-4886.1000127.

[7] D. Hemanand, C. Senthilkumar, O. S. Saleh, B. Muthuraj, A. Anand, and V. Velmurugan, "Analysis of power optimization and enhanced routing protocols for wireless sensor networks," *Measurement: Sensors*, vol. 25, p. 100610, Feb. 2023, doi: 10.1016/j.measen.2022.100610.

[8] V. M. Dileepan and J. Jayakumar, "Performance analysis of lithium batteries," in *2017 International Conference on Innovations in Electrical, Electronics, Instrumentation and Media Technology (ICEEIMT)*, Feb. 2017, pp. 330–333. doi: 10.1109/ICIEEIMT.2017.8116860.

[9] S. Research, "Industrial Wireless Sensor Network Market Size is projected to reach USD 8.62 billion by 2030, growing at a CAGR of 7.13%: Straits Research," GlobeNewswire News Room. Accessed: Oct. 21, 2023. [Online]. Available: https://www.globenewswire.com/en/news-release/2023/07/06/2700575/0/en/Industrial-Wireless-Sensor-Network-Market-Size-is-projected-to-reach-USD-8-62-billion-by-2030-growing-at-a-CAGR-of-7-13-Straits-Research.html

[10] "Wireless Sensor For Medical Market Size, Opportunities & Forecast," Verified Market Research. Accessed: Oct. 22, 2023. [Online]. Available: https://www.verifiedmarketresearch.com/product/wireless-sensor-for-medical-market/

[11] Z. Sheng, C. Mahapatra, C. Zhu, and V. C. M. Leung, "Recent Advances in Industrial Wireless Sensor Networks Toward Efficient Management in IoT," *IEEE Access*, vol. 3, pp. 622–637, 2015, doi: 10.1109/ACCESS.2015.2435000.

[12] P. Saha, V. Kumar, S. Kathuria, A. Gehlot, V. Pachouri, and A. S. Duggal, "Precision Agriculture Using Internet of Things and Wireless Sensor Networks," in *2023 International Conference on Disruptive Technologies (ICDT)*, May 2023, pp. 519–522. doi: 10.1109/ICDT57929.2023.10150678.

[13] O. Lai, "Top 7 Smart Cities in the World in 2023," Earth.Org. Accessed: Oct. 22, 2023. [Online]. Available: https://earth.org/top-7-smart-cities-in-the-world/

[14] "Global Smart City Market Research Report to 2028 - Featuring AT&T, Cisco Systems, Hitachi and IBM Among Others - ResearchAndMarkets.com." Accessed: Oct. 22, 2023. [Online]. Available: https://www.businesswire.com/news/home/20220926005685/en/Global-Smart-City-Market-Research-Report-to-2028---Featuring-ATT-Cisco-Systems-Hitachi-and-IBM-Among-Others---ResearchAndMarkets.com

[15] "cr-qcom-181_v16.pdf." Accessed: Oct. 22, 2023. [Online]. Available: https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/cr-qcom-181_v16.pdf

[16] P. Jokic and M. Magno, "Powering smart wearable systems with flexible solar energy harvesting," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2017, pp. 1–4. doi: 10.1109/ISCAS.2017.8050615.

[17] J. Zhao *et al.*, "Self-Powered Implantable Medical Devices: Photovoltaic Energy Harvesting Review," *Advanced Healthcare Materials*, vol. 9, no. 17, p. 2000779, 2020, doi: 10.1002/adhm.202000779.

[18] C. Xu, Y. Song, M. Han, and H. Zhang, "Portable and wearable self-powered systems based on emerging energy harvesting technology," *Microsyst Nanoeng*, vol. 7, no. 1, Art. no. 1, Mar. 2021, doi: 10.1038/s41378-021-00248-z.

[19] J. Yick, B. Mukherjee, and D. Ghosal, "Wireless sensor network survey," *Computer Networks*, vol. 52, no. 12, pp. 2292–2330, Aug. 2008, doi: 10.1016/j.comnet.2008.04.002.

[20] M. Hatamvand *et al.*, "Recent advances in fiber-shaped and planar-shaped textile solar cells," *Nano Energy*, vol. 71, p. 104609, May 2020, doi: 10.1016/j.nanoen.2020.104609.

[21] B. Han, S. Zhang, J. Liu, and Y. Jiang, "Design and Development of a 2 × 2 Array Piezoelectric–Electromagnetic Hybrid Energy Harvester," *Micromachines*, vol. 13, no. 5, Art. no. 5, May 2022, doi: 10.3390/mi13050752.

[22] B. Jiang, F. Zhu, Y. Yang, J. Zhu, Y. Yang, and M. Yuan, "A Hybrid Piezoelectric and Electromagnetic Broadband Harvester with Double Cantilever Beams," *Micromachines*, vol. 14, no. 2, Art. no. 2, Feb. 2023, doi: 10.3390/mi14020240.

[23] "Submicron crystalline buildup and size-dependent energy harvesting characteristic in PZN–PZT ternary ferroelectrics - Yue - 2017 - Journal of the American Ceramic Society - Wiley Online Library." Accessed: Oct. 24, 2023. [Online]. Available: https://ceramics.onlinelibrary.wiley.com/doi/10.1111/jace.15054

[24] J. Wang, L. Tang, L. Zhao, G. Hu, R. Song, and K. Xu, "Equivalent circuit representation of a vortex-induced vibration-based energy harvester using a semi-empirical lumped parameter approach," *International Journal of Energy Research*, vol. 44, no. 6, pp. 4516–4528, 2020, doi: 10.1002/er.5228.

[25] K. Y. Fang, W. Q. Jing, Y. F. He, Y. C. Zhao, and F. Fang, "A low-frequency vibration energy harvester employing self-biased magnetoelectric composite," *Sensors and Actuators A: Physical*, vol. 332, p. 113066, Dec. 2021, doi: 10.1016/j.sna.2021.113066.

[26]   "Toward Broadband Vibration-based Energy Harvesting - Lihua Tang, Yaowen Yang, Chee Kiong Soh, 2010." Accessed: Oct. 24, 2023. [Online]. Available: https://journals.sagepub.com/doi/10.1177/1045389X10390249

[27]   I. Izadgoshasb, Y. Y. Lim, L. Tang, R. V. Padilla, Z. S. Tang, and M. Sedighi, "Improving efficiency of piezoelectric based energy harvesting from human motions using double pendulum system," *Energy Conversion and Management*, vol. 184, pp. 559–570, Mar. 2019, doi: 10.1016/j.enconman.2019.02.001.

[28]   "Frequency-tunable resonant hybrid vibration energy harvester using a piezoelectric cantilever with electret-based electrostatic coupling - Feng - 2023 - IET Nanodielectrics - Wiley Online Library." Accessed: Oct. 24, 2023. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/10.1049/nde2.12043

[29]   S. P. Beeby *et al.*, "A micro electromagnetic generator for vibration energy harvesting," *J. Micromech. Microeng.*, vol. 17, no. 7, pp. 1257–1265, Jul. 2007, doi: 10.1088/0960-1317/17/7/007.

[30]   J. Jiang, S. Liu, L. Feng, and D. Zhao, "A Review of Piezoelectric Vibration Energy Harvesting with Magnetic Coupling Based on Different Structural Characteristics," *Micromachines*, vol. 12, no. 4, Art. no. 4, Apr. 2021, doi: 10.3390/mi12040436.

[31]   D. Cao, J. Wang, X. Guo, S. K. Lai, and Y. Shen, "Recent advancement of flow-induced piezoelectric vibration energy harvesting techniques: principles, structures, and nonlinear designs," *Appl. Math. Mech.-Engl. Ed.*, vol. 43, no. 7, pp. 959–978, Jul. 2022, doi: 10.1007/s10483-022-2867-7.

[32]   "Improving functionality of vibration energy harvesters using magnets - Lihua Tang, Yaowen Yang, Chee-Kiong Soh, 2012." Accessed: Oct. 24, 2023. [Online]. Available: https://journals.sagepub.com/doi/10.1177/1045389X12443016

[33]   X. Zhang and L.-D. Zhao, "Thermoelectric materials: Energy conversion between heat and electricity," *Journal of Materiomics*, vol. 1, no. 2, pp. 92–105, Jun. 2015, doi: 10.1016/j.jmat.2015.01.001.

[34]   M. F. Sanad, A. E. Shalan, S. O. Abdellatif, E. S. A. Serea, M. S. Adly, and Md. A. Ahsan, "Thermoelectric Energy Harvesters: A Review of Recent Developments in Materials and

Devices for Different Potential Applications," *Top Curr Chem (Z)*, vol. 378, no. 6, p. 48, Oct. 2020, doi: 10.1007/s41061-020-00310-w.

[35]   "Thermoelectric Cooling and Power Generation | Science." Accessed: Oct. 29, 2023. [Online]. Available: https://www.science.org/doi/10.1126/science.285.5428.703

[36]   X.-L. Shi, J. Zou, and Z.-G. Chen, "Advanced Thermoelectric Design: From Materials and Structures to Devices," *Chem. Rev.*, vol. 120, no. 15, pp. 7399–7515, Aug. 2020, doi: 10.1021/acs.chemrev.0c00026.

[37]   X. Lu *et al.*, "High-Efficiency Thermoelectric Power Generation Enabled by Homogeneous Incorporation of MXene in (Bi,Sb)2Te3 Matrix," *Advanced Energy Materials*, vol. 10, no. 2, p. 1902986, 2020, doi: 10.1002/aenm.201902986.

[38]   X. Huang *et al.*, "Materials Strategies and Device Architectures of Emerging Power Supply Devices for Implantable Bioelectronics," *Small*, vol. 16, no. 15, p. 1902827, 2020, doi: 10.1002/smll.201902827.

[39]   A. P. Perez-Marín *et al.*, "Micropower thermoelectric generator from thin Si membranes," *Nano Energy*, vol. 4, pp. 73–80, Mar. 2014, doi: 10.1016/j.nanoen.2013.12.007.

[40]   M. Massetti *et al.*, "Unconventional Thermoelectric Materials for Energy Harvesting and Sensing Applications," *Chem. Rev.*, vol. 121, no. 20, pp. 12465–12547, Oct. 2021, doi: 10.1021/acs.chemrev.1c00218.

[41]   J. Katic, S. Rodriguez, and A. Rusu, "A Dual-Output Thermoelectric Energy Harvesting Interface With 86.6% Peak Efficiency at 30 \mu \text W and Total Control Power of 160 nW," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 8, pp. 1928–1937, Aug. 2016, doi: 10.1109/JSSC.2016.2561959.

[42]   B. T. McGrail, A. Sehirlioglu, and E. Pentzer, "Polymer Composites for Thermoelectric Applications," *Angewandte Chemie International Edition*, vol. 54, no. 6, pp. 1710–1723, 2015, doi: 10.1002/anie.201408431.

[43]   O. Bubnova and X. Crispin, "Towards polymer-based organic thermoelectric generators," *Energy Environ. Sci.*, vol. 5, no. 11, pp. 9345–9362, Oct. 2012, doi: 10.1039/C2EE22777K.

[44] A. Karalis, J. D. Joannopoulos, and M. Soljačić, "Efficient wireless non-radiative mid-range energy transfer," *Annals of Physics*, vol. 323, no. 1, pp. 34–48, Jan. 2008, doi: 10.1016/j.aop.2007.04.017.

[45] A. M. Aibinu *et al.*, "A Systematic Review of Wireless Transmission System," *Current Journal of Applied Science and Technology*, pp. 66–79, Mar. 2021, doi: 10.9734/cjast/2021/v40i231260.

[46] D. Khan *et al.*, "An Efficient Reconfigurable RF-DC Converter With Wide Input Power Range for RF Energy Harvesting," *IEEE Access*, vol. 8, pp. 79310–79318, 2020, doi: 10.1109/ACCESS.2020.2990662.

[47] "Scientific Study: RF Radiation Levels From Cellular Towers | EMF & RF Testing | Mitigation | Shielding Experts." Accessed: Oct. 30, 2023. [Online]. Available: http://www.emfrf.com/rf-radiation-levels-from-cellular-towers/

[48] X. Lu, P. Wang, D. Niyato, D. I. Kim, and Z. Han, "Wireless Networks With RF Energy Harvesting: A Contemporary Survey," *IEEE Communications Surveys & Tutorials*, vol. 17, no. 2, pp. 757–789, 2015, doi: 10.1109/COMST.2014.2368999.

[49] H. J. Visser, A. C. F. Reniers, and J. A. C. Theeuwes, "Ambient RF Energy Scavenging: GSM and WLAN Power Density Measurements," in *2008 38th European Microwave Conference*, Oct. 2008, pp. 721–724. doi: 10.1109/EUMC.2008.4751554.

[50] "FCC Rules -." Accessed: Oct. 30, 2023. [Online]. Available: https://afar.net/tutorials/fcc-rules/

[51] G. P. Cabrera *et al.*, "A 2.4 GHz Energy-efficient Short-range Receiver with Wake-up and Multiple Gain Settings for Wireless Sensor Networks," in *TENCON 2018 - 2018 IEEE Region 10 Conference*, Oct. 2018, pp. 0026–0031. doi: 10.1109/TENCON.2018.8650538.

[52] C.-T. Tsai, C.-C. Li, C.-H. Lin, C.-T. Lin, S. Chi, and G.-R. Lin, "Long-reach 60-GHz MMWoF link with free-running laser diodes beating," *Sci Rep*, vol. 8, no. 1, Art. no. 1, Sep. 2018, doi: 10.1038/s41598-018-32058-1.

[53] N. M. Pletcher, S. Gambini, and J. M. Rabaey, "A 2GHz 52 μW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture," in *2008 IEEE International Solid-State*

Circuits Conference - Digest of Technical Papers, Feb. 2008, pp. 524–633. doi: 10.1109/ISSCC.2008.4523288.

[54]   J. Carlsson, K. Palmkvist, and L. Wanhammar, "A Clock Gating Circuit for Globally Asynchronous Locally Synchronous Systems," in *2006 NORCHIP*, Nov. 2006, pp. 15–18. doi: 10.1109/NORCHP.2006.329234.

[55]   N. Van Huynh, D. T. Hoang, X. Lu, D. Niyato, P. Wang, and D. I. Kim, "Ambient Backscatter Communications: A Contemporary Survey," *IEEE Communications Surveys & Tutorials*, vol. 20, no. 4, pp. 2889–2922, 2018, doi: 10.1109/COMST.2018.2841964.

[56]   Y. Zhang *et al.*, "Design of an RFID-Based Self-Jamming Identification and Sensing Platform," *IEEE Transactions on Mobile Computing*, pp. 1–15, 2023, doi: 10.1109/TMC.2023.3280942.

[57]   Y.-J. Kim, H. S. Bhamra, J. Joseph, and P. P. Irazoqui, "An Ultra-Low-Power RF Energy-Harvesting Transceiver for Multiple-Node Sensor Application," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 11, pp. 1028–1032, Nov. 2015, doi: 10.1109/TCSII.2015.2456511.

[58]   G. Papotto, F. Carrara, A. Finocchiaro, and G. Palmisano, "A 90-nm CMOS 5-Mbps Crystal-Less RF-Powered Transceiver for Wireless Sensor Network Nodes," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 335–346, Feb. 2014, doi: 10.1109/JSSC.2013.2285371.

[59]   Y. Shinki, K. Shibata, M. Mansour, and H. Kanaya, "Impedance Matching Antenna-Integrated High-Efficiency Energy Harvesting Circuit," *Sensors*, vol. 17, no. 8, Art. no. 8, Aug. 2017, doi: 10.3390/s17081763.

[60]   J. F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, Jun. 1976, doi: 10.1109/JSSC.1976.1050739.

[61]   H. Ito *et al.*, "A 2.3 pJ/bit frequency-stable impulse OOK transmitter powered directly by an RF energy harvesting circuit with −19.5 dBm sensitivity," in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2014, pp. 13–16. doi: 10.1109/RFIC.2014.6851645.

[62]   J.-P. Celis and B. Prakash, "Chapter 4 - Surface Modification of Materials by Plasma Immersion Ion Implantation," in *Materials Surface Processing by Directed Energy Techniques*, Y. Pauleau, Ed., in European Materials Research Society Series. , Oxford: Elsevier, 2006, pp. 111–149. doi: 10.1016/B978-008044496-3/50005-8.

[63]   P. K. Chatterjee *et al.*, "Integrated Circuits," in *Reference Data for Engineers*, Elsevier, 2002, pp. 20-1-20–113. doi: 10.1016/B978-075067291-7/50022-4.

[64]   M. Awad, P. Benech, J.-M. Duchamp, and N. Corrao, "Performance Comparison of Two Stage of Dickson Voltage Rectifier Realized in FD-SOI 28 nm and BiCMOS 55 nm for RF Energy Harvesting," in *2018 IEEE/MTT-S International Microwave Symposium - IMS*, Jun. 2018, pp. 980–983. doi: 10.1109/MWSYM.2018.8439412.

[65]   M. Awad, P. Benech, and J. M. Duchamp, "Electronic circuit design for RF energy harvesting using 28 nm FD-SOI technology," *Microwave and Optical Technology Letters*, vol. 60, no. 6, pp. 1349–1353, 2018, doi: 10.1002/mop.31157.

[66]   D. Levacq, C. Liber, V. Dessard, and D. Flandre, "Composite ULP diode fabrication, modelling and applications in multi-Vth FD SOI CMOS technology," *Solid-State Electronics*, vol. 48, no. 6, pp. 1017–1025, Jun. 2004, doi: 10.1016/j.sse.2003.12.016.

[67]   H. J. Oguey and D. Aebischer, "CMOS current reference without resistance," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, pp. 1132–1135, Jul. 1997, doi: 10.1109/4.597305.

[68]   "A 0.9-V supply, 16.2 nW, fully MOSFET resistorless bandgap reference using sub-threshold operation | Analog Integrated Circuits and Signal Processing." Accessed: Nov. 05, 2023. [Online]. Available: https://link.springer.com/article/10.1007/s10470-019-01521-y

[69]   K.-H. Nam, N.-P. Hong, and J.-S. Park, "A 16-Times Frequency Multiplier for 5G Synthesizer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 11, pp. 4961–4976, Nov. 2021, doi: 10.1109/TMTT.2021.3103203.

[70]   M. Cochet *et al.*, "A 28nm FD-SOI standard cell 0.6–1.2V open-loop frequency multiplier for low power SoC clocking," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2016, pp. 1206–1209. doi: 10.1109/ISCAS.2016.7527463.

[71]   W. Lee, T. Dinc, and A. Valdes-Garcia, "Reconfigurable 60-GHz Radar Transmitter SoC with Broadband Frequency Tripler in 45nm SOI CMOS," in *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2019, pp. 43–46. doi: 10.1109/RFIC.2019.8701736.

[72]   A. Balasubramaniyan and A. Bellaouar, "Digital Frequency Multiplier for LO Generation using 22nm FDSOI," in *2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct. 2018, pp. 1–2. doi: 10.1109/S3S.2018.8640194.

[73]   Naveed and J. Dix, "A Resistor-less, Nano-Watt CMOS Voltage Reference with High PSRR," in *2021 22nd International Symposium on Quality Electronic Design (ISQED)*, Apr. 2021, pp. 19–23. doi: 10.1109/ISQED51717.2021.9424289.

[74]   S. Docking and M. Sachdev, "A method to derive an equation for the oscillation frequency of a ring oscillator," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 2, pp. 259–264, Feb. 2003, doi: 10.1109/TCSI.2002.808235.

[75]   "Organisatie," TU Delft. Accessed: Nov. 06, 2023. [Online]. Available: https://ei.et.tudelft.nl/smart_temperature/

[76]   J. Li, Y. Lin, N. Ning, and Q. Yu, "A +0.44°C/−0.4°C Inaccuracy Temperature Sensor with Multi-Threshold MOSFET-Based Sensing Element and CMOS Thyristor-Based VCO," IEEE Trans. Circuits Syst. I, vol. 68, no. 3, pp. 1102-1113, March 2021.

[77]   B. Zambrano, E. Garzón, S. Strangio, F. Crupi and M. Lanuzza, "A 0.05 mm², 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS," IEEE Trans. Circuits Syst II: Exp. Briefs, vol. 69, no. 3, pp. 749-753, March 2022.

[78]   C.-Y. Ku and T.-T. Liu, "A voltage-scalable low-power all-digital temperature sensor for on-chip thermal monitoring," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 66, no. 10, pp. 1658–1662, Oct. 2019.

[79]   T. Someya, A. K. M. Islam, T. Sakurai, and M. Takamiya, "An 11-nW CMOS temperature-to-digital converter utilizing sub-threshold current at sub-thermal drain voltage," IEEE J. Solid-State Circuits, vol. 54, no. 3, pp. 613–622, Mar. 2019.

[80]   T. Anand, K. A. A. Makinwa, and P. K. Hanumolu, "A VCO based highly digital temperature sensor with 0.034 ∘C/mV supply sensitivity," IEEE J. Solid-State Circuits, vol. 51, no. 11, pp. 2651–2663, Nov. 2016

[81]   M. A. Karami and K. Moez, "An Integrated RF-Powered Wake-Up Wireless Transceiver With –26 dBm Sensitivity," *IEEE Internet of Things Journal*, vol. 9, no. 11, pp. 8693–8706, Jun. 2022, doi: 10.1109/JIOT.2021.3116208.

[82]   S. Schmickl, T. Faseth, and H. Pretl, "An RF-Energy Harvester and IR-UWB Transmitter for Ultra-Low-Power Battery-Less Biosensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 5, pp. 1459–1468, May 2020, doi: 10.1109/TCSI.2020.2970765.

[83]   H. Bhamra, Y.-W. Huang, Q. Yuan, and P. Irazoqui, "An Ultra-Low Power 2.4 GHz Transmitter for Energy Harvested Wireless Sensor Nodes and Biomedical Devices," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 206–210, Jan. 2021, doi: 10.1109/TCSII.2020.3005332.

[84]   A. Hejazi *et al.*, "A 2.4 GHz Power Receiver Embedded With a Low-Power Transmitter and PCE of 53.8%, for Wireless Charging of IoT/Wearable Devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 9, pp. 4315–4325, Sep. 2021, doi: 10.1109/TMTT.2021.3088503.

Appendix A

The calculation for designing a patch antenna operating at 915 MHz on an FR-4 substrate:

Patch Antenna Design Parameters

- Frequency of Operation (f_r): 915 MHz

- Substrate Material: FR-4

- Substrate Dielectric Constant (ε_r): 4.4 (typical for FR-4)

- Substrate Loss Tangent (δ): 0.02 (approximate for FR-4)

- Desired Impedance: 50 ohms

Patch Antenna Calculations

Patch width Calculation: The width of the patch is calculated using the frequency of operation as

$$W = \frac{C_o}{2\,f_r}\sqrt{\frac{2}{\varepsilon_r + 1}} \tag{50}$$

Where h is the height or thickness of substrate while W is the width of the patch. Due to the fringing effect, the effective length (L_{eff}) of the patch becomes larger than the physical length of the patch and it is calculated as :

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\sqrt{1 + 12\frac{h}{W}} \tag{51}$$

Where h is the height or thickness of substrate while W is the width of the patch. Due to the fringing effect, the effective length (L_{eff}) of the patch becomes larger than the physical length (L) of the patch and it's calculated as :

$$\mathbf{L}_{eff} = L + \Delta L \tag{52}$$

$$\Delta L = 0.412 \frac{\varepsilon_{eff} + 0.3}{\varepsilon_{eff} - 0.258} \frac{\frac{w}{h} + 0.264}{\frac{w}{h} + 0.8} \tag{53}$$

$$L = \frac{C_o}{2 f_r \sqrt{\varepsilon_{eff}}} - 2\Delta L \tag{54}$$

The length (L_G) and width(W_G) of the ground plane of the patch antenna are calculated as :

$$\mathbf{L_G} = 6h + L \tag{55}$$

and

$$W_{\mathbf{G}} = 6h + W \tag{56}$$

The patch antenna is fed with a microstrip feed line and sets the input impedance of the patch. The impedance (Z) of the feedline is calculated as:

$$Z = \frac{120\pi\, C_o}{\sqrt{\varepsilon_{eff}}} \left[\frac{W_f}{h} + 1.398 + 0.667\, ln\left(\frac{W_f}{h} + 1.444 \right) \right] \tag{57}$$

Where Z is kept 50Ω and W_f is the width of the feed line. The length of the feed (L_f) inside the patch area is calculated as :

$$L_f = 10^{-4} \big(0.001699 * \varepsilon_r{}^7 + 0.13761 * \varepsilon_r{}^6 - 6.1783 * \varepsilon_r{}^5 + 93.187 * \varepsilon_r{}^4 \tag{58}$$

$$- 682.69 * \varepsilon_r{}^3 + 2561.9 * \varepsilon_r{}^2 - 4043 * \varepsilon_r + 6697 \big) \frac{L}{2}$$

The simulation and result details are discussed in section 3.3.