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High-Rate Acquisition System for an Infrared LPS

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Abstract—In the last years, the demand for positioning systems based on visible light, infrared light or, in general, optical signals has increased considerably due to their high accuracy and low cost compared to positioning systems based on other technologies, as well as their ease of integration due to their wide presence in domestic and industrial environments. The main constraint of these solutions is that the high speed of light makes the acquisition process complex. This work proposes a complete acquisition architecture for the twelve signals coming from four QADA (Quadrature Angular Diversity Aperture) photoreceptors, based on an analog front-end for signal conditioning at the input, an analog-to-digital converter, and a final digital stage using an FPGA for the acquisition of the data coming from the converter with high data rates up to 16.25 Msps. To verify the system performance, LS (Loosely Synchronized) sequences, often used in positioning systems, are emitted by a LED, and, later, they are acquired and digitally processed successfully by the proposed architecture in some preliminary experimental tests.

Index Terms—optical positioning system, infrared, FPGA

I. INTRODUCTION

Location-based services (LBS) and tasks have become a key aspect in recent decades for a large number of devices and applications, not only for mobile robots and drones, but also for people in different situations [1]. A person's position may allow to provide them with a more oriented information in a museum or cultural centre, or may support a longer independent living of elderly in their own homes. Whereas Global Navigation Satellite Systems (GNSS) are already capable of achieving accurate enough positioning outdoors, the conditions and performance of GNSS change dramatically indoors and in some particular outdoor placements, such as natural or urban canyons, where local positioning is still a challenging issue.

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Many technologies have already been applied to local positioning systems (LPS) [2]. Radio-frequency solutions are likely the most common, such as WiFi routers [3], UWB (Ultra Wide Band) nodes [4], or Bluetooth ones [5]. They are often easy to deploy and implement, but achieve a limited accuracy, according to the methods and algorithms implemented. Ultrasonic positioning systems have also shown a suitable performance in positioning [6], with accuracies in the range of centimeters. Infrared and visible light are a feasible option in this context as well [7] [8], particularly since the massive installation of LED lamps in most indoor environments. They are characterized by the constraint derived from the speed of light, which makes complex the measurements and the associated computation. For that purpose, different positioning algorithms can be found in previous works, such as triangulation based on measuring the Angles-of-Arrival (AoA) [9], or fingerprinting based on Received Signal Strength (RSS) [10] [11].

With regard to the type of receiver involved in Infrared LPSs (IRLPS), imaging sensors can be integrated [12], although this often implies the application of computer vision methods that require a high computational load. On the other hand, photodetectors can also be employed without requiring complex algorithms [13], sometimes even forming arrays with particular geometrical distributions [14]. In this group, it is possible to find the quadrant photodiodes [15] [16], together with an aperture dedicated to improve the estimation of AoAs.

Another relevant aspect in IRLPSs with multiple emitters is the medium access technique for supporting simultaneous transmission [6]. When it is necessary to emit simultaneously from some LEDs, encoding techniques are a typical approach to allow the receiver to distinguish the signals coming from each emitter [16], while providing a longer range and accuracy, as well as robustness against noise and interference. Nevertheless, these encoding techniques usually imply more complex processing algorithms, including modulation schemes to adapt the transmission to the bandwidth available, as well as correlations and matched filtering to efficiently detect the sequences transmitted by LEDs.

Although the computational requirements may vary according to the number of emitters and receivers existing in the proposal, the treatment of the acquired incoming signals at the receivers in order to search for the different simultaneous transmissions often becomes a challenge, since it requires a massive parallel processing of samples, that it is difficult to handle in real time by general-purpose processors. In this context, Field-Programmable Gate Arrays (FPGA) have become a feasible solution thanks to their internal parallelism, capable of dealing with several dataflows at high rates [17]. These devices have already been tested successfully with encoding techniques for other sensory technologies in positioning [6].

This work presents an efficient architecture based on a FPGA device that is able to process the acquired signals coming from the QADA receivers in a IRLPS. The IRLPS consists of four QADA, where each one provides three incoming signals. An analog front-end (AFE) has been proposed and designed for a suitable conditioning and amplification of the signals coming from the QADA sensors before the acquisition stage, based on a automatic gain control (AGC). The resulting twelve signals are sampled by a AD9249 converter at rates up to 16.25 Msps. A controller has been designed in the FPGA to suitably handle the twelve channels at those rates, by implementing the corresponding memory banks that can be addressed afterwards for further processing.

The main novelty of this work is then the definition and design of an specific FPGA-based architecture, capable of managing in real time the incoming signals from a QADA receiver, which is part of IRLPS. The architecture is designed in such a way that makes possible to achieve high acquisition rates, compared with previous works, while assuring a suitable conditioning of the input signals. The rest of the manuscript is organized as follows: Section II describes the general overview of the IRLPS involved, as well as the design of the analog front-end dedicated to the proper conditioning of the signals coming from the QADA sensors and the FPGA-based architecture proposed for the acquisition of those signals; Section III presents some preliminary experimental signals; and, finally, conclusions are discussed in Section IV.

II. SYSTEM ARCHITECTURE OF THE PROPOSED IRLPS

The proposed IRLPS is based on a set of LEDs located at unknown 3D coordinates denoted as $\mathbf{b}_i (x_{t,i}, y_{t,i}, z_{t,i})$ within the coverage area, and a receiver module located at a known position on a specific plane. A general overview of the implemented IRLPS is presented in Fig. 1, where the LEDs i are located on board the mobile to be positioned (i.e. a person), whereas the receivers j are located in a certain plane (i.e. the ceiling).

A block diagram of the proposed system architecture is presented in Fig. 2, where the light emitted by the LEDs illuminates each QADA receiver, then goes through an analog conditioning stage before being digitized by the acquisition stage. Each stage will be explained in detail in the following Subsections.

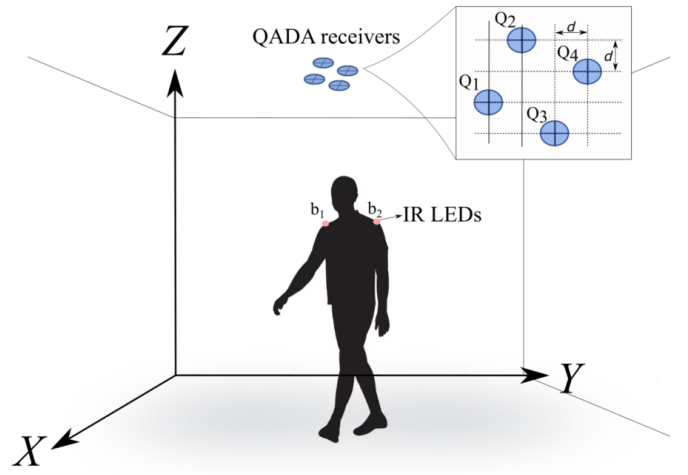


Fig. 1. General overview of the proposed system.

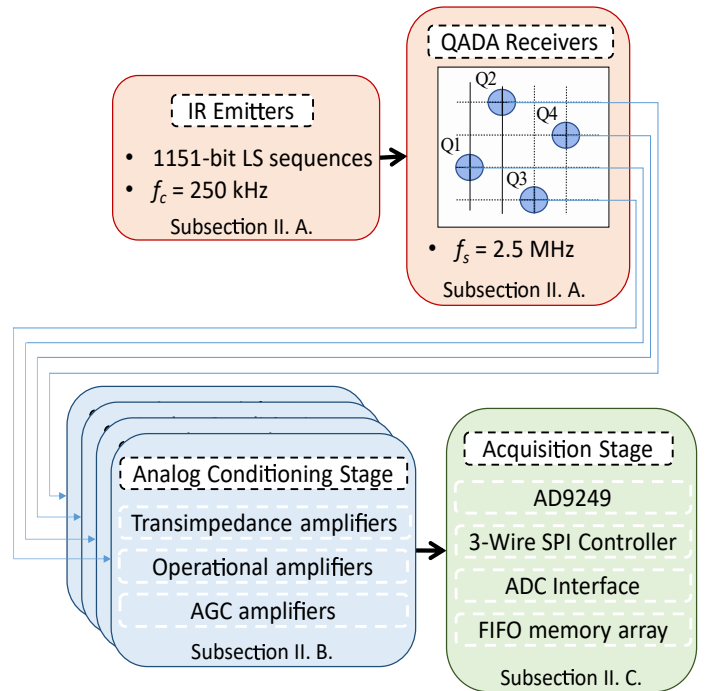


Fig. 2. Block diagram of the proposed system architecture.

A. Emitter and Receiver Description

The IR beacons transmit a 1151-bit LS sequence using a BPSK modulation at a high carrier frequency ($f_c = 250$ kHz). The transmission is defined by an oversampling of $M = f_s/f_c = 10$ samples for a carrier cycle (sampling frequency $f_s = 2.5$ MHz) and sequence shifting of 10 samples [18]. Each LED has a unique code.

The receiver module is based on four Quadrant photodiode Angular Diversity Aperture (QADA). Each QADA is a circular photoreceptor QP50-6-18u-TO8 [19] with a square aperture placed on top of it at a height of $h_{ap} = 2.6$ mm. The geometrical distribution of the receiver module is shown in

Fig. 1, where it can be observed that the QADAs are not aligned, thus avoiding potential singularities. The distance d between QADAs has been set at 15 cm [20].

The operating principle of the proposed IRLPS is that the light emitted by the LEDs passes through the centre of each aperture and illuminates each QADA receiver. This results in four currents (one for each quadrant) per QADA that are proportional to the illuminated area on the photodiode. These four output signals are processed in the analog conditioning stage.

B. Analog Conditioning Stage

When using QADA receivers with aperture as described in [9], [21], the conditioning block of the signals coming from the sensor is of paramount importance, considering that it must operate in a linear zone with large dynamic signal margins and provide the sum output (all the radiation received from an emitter) and the differential outputs (indicative of the beam deviations in horizontal and vertical directions) of the QADA. The differential signals are after normalized with respect to the sum signal to allow the use of the positioning algorithms independently of the received radiation level [18], [22].

The analog conditioning system can be provided by the QADA manufacturer itself in evaluation boards [23] or, as in this work, developed to fit particular features (a view of the block diagram and final board are shown in Fig. 3.a) and 3.b), respectively. This conditioning stage of the QADA outputs employs transconductance amplifiers with continuous and low frequency (backlighting) signal cancellation [24] and a high dynamic range automatic gain control (AGC) applied to the three channels, with one of them performing as a master: the gain G of this channel is forwarded to the other two.

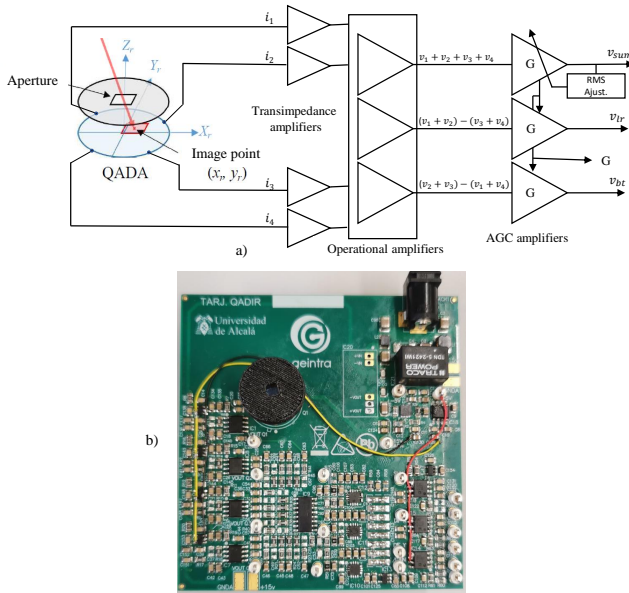


Fig. 3. a) Block diagram of the analog conditioning system developed; and b) view of the PCB board.

The system is intended to operate under usual conditions of natural or artificial illumination. Therefore, taking advantage of the fact that the useful emissions are coded and modulated at relatively high frequencies (hundreds of kHz), the system should be provided with a filtering that eliminates the low-frequency components of the radiation received by the QADA, which corresponds to the background radiation caused by the natural light or dimming frequencies from artificial systems.

As the relative positions between the transmitter and the receiver change, which is inherent to any positioning system, the range of signal levels to be handled is large (differences of up to 100 dB between different situations). This can be caused by the distance between the emitter and the receiver or by the angles at which the rays pass through the sensor aperture. This considerably limits the relative emitter-receiver distances and orientations that can be handled: a very high gain can lead to amplifier saturations, whereas a small gain limits the reception of low-amplitude signals. The solution is to include an AGC that adapts the received levels according to each circumstance. As shown in Fig. 3, three output signals must be obtained from the four photocurrents supplied by the QADA: the sum radiation (v_{sum}), the differential radiation in the X -axis (v_{lr}) and the differential radiation in the Y -axis (v_{bt}). The amplification of these three signals must be identical in the three output channels to allow the subsequent normalization of the differential channels with respect to the sum radiation. This is essential to make the calculation of the central point of incidence from the beam passing through the aperture, i.e. (x_r, y_r) in Fig. 3, independently of the received signal level.

The AGC is based on the Analog Devices AD8338 IC [25]. As for the channel of the sum current (signal v_{sum} in Fig. 3), a configuration has been arranged where the gain is self-adjusted according to the RMS value of the received signal. The sum signal has been chosen since it always presents the highest signal level. The gain is self-adjusted to ensure that the output v_{sum} has a fixed RMS value of 10 mV. The gain G obtained in this stage is also used for the other amplifiers of the two channels v_{lr} and v_{bt} , which behave as programmable gain amplifiers. The gain G can also be digitized, so the following modules can know its value at every time.

C. Acquisition Stage

The acquisition stage is composed by a 16-channel analog-to-digital converter (ADC) connected to the FPGA board through the FMC HPC port. An AD9249-65EBZ board is used, which is based on the 14-bit AD9249 chip that allows conversion rates up to 65 Msps. This evaluation board includes an on-board 65 MHz crystal oscillator that can be used as the clock source of the system and a SPI interface to setup the parameters of the device. In this design, the ADC is set up to operate with the on-board oscillator to avoid using an external clock source that would increase the system size. Furthermore, the ADC resolution is set to a 12-bit serial stream.

The FPGA design in charge of addressing this ADC consists of three modules: a 3-Wire SPI controller to interact with the

SPI circuitry of the AD9249; an interface block to acquire and condition the input data; and an array of FIFO memories used to store the acquired data and subsequently send them to the following signal processing stage via the AXI4-Stream communication. The block diagram of the proposed architecture is depicted in Fig. 4.

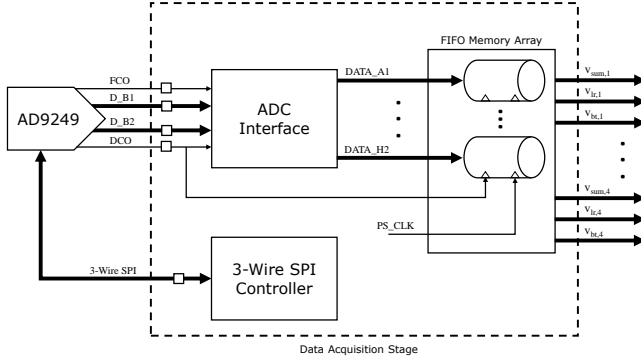


Fig. 4. Block diagram of the acquisition stage. Note that the data provided by the AD9249 are split into two 8-channel data banks: D_B1 and D_B2.

First of all, the 3-Wire SPI controller is made up of a Hierarchical State Machine (HSM) that manages the three signals of the bus before, during and after a SPI transaction occurs. In addition, a busy port is used to report to external devices whether it is busy in a transaction or, on the contrary, is available to start a new one. This peripheral is encapsulated into an AXI4-Lite wrapper to allow the designer to set up the bus features, as well as the serial clock frequency, by means of the Zynq Processing System.

On the other hand, the core element of the design is the ADC interface. The purpose of this block is to carry out the serial data acquisition of the 16 available channels. The AD9249 provides the LVDS serial data D_B1 and D_B2, the bit clock DCO and the frame clock FCO, as labeled in Fig. 4. Firstly, these signals are introduced into a differential input buffer to output single-ended signals. Subsequently, a Double Data Rate (DDR) flip-flops stage is used to capture the data in both bit clock edges. The data are fed into the block output, synchronized with the frame clock rising edges, which signals the start of a new data frame. Furthermore, a prescaler is added for downsampling purposes if necessary. This configuration allows high-speed acquisition with data rates up to 16.25 Mps.

Finally, an array of FIFO memories is added with two main purposes. On the one hand, it is necessary to tackle a clock domain crossing issue, because the ADC interface module exports data synchronously with the bit clock input of the board, and the rest of the general design operates with the clock provided by the processing system in the FPGA. On the other hand, the later signal processing stage may operate slower than the data acquisition. These problems are solved by using asynchronous FIFO memories, which allow independent write and read operations with different clock domains and store a certain depth of samples, avoiding data losses when

the signal processing modules are slower than the acquisition one.

III. EXPERIMENTAL RESULTS

For the validation of the results, the incoming signals have been acquired from a single QADA, where a temporal window containing a complete period of the transmitted signal has been digitized. The sequences used during the tests are 1151-bit LS codes, modulated in BPSK, with a carrier frequency of 250 kHz and a sampling rate of 2.5 MHz. An example of the transmitted LS codes is plotted in Fig. 5. The sum signal v_{sum} , and the difference ones v_{lr} and v_{bt} , are depicted in Fig. 5 as well.

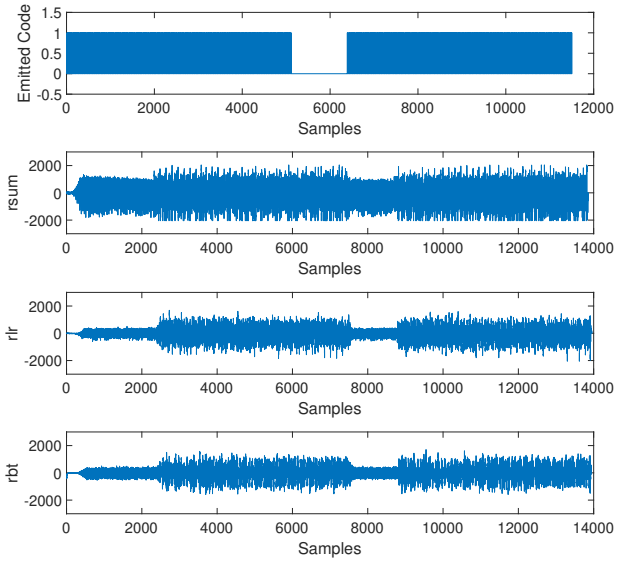


Fig. 5. Example of the transmitted 1151-bit LS codes (top), and the acquired signals v_{sum} , v_{lr} , and v_{bt} .

To carry out the experimental tests, the configuration shown in Fig. 6 is set. On the one hand, the receiving part consists of a receiver module composed mainly by a QADA photoreceptor and the analog front-end shown in Subsection II-B connected to the AD9249-65EBZ acquisition board, which, in turn, communicates with the FPGA-based architecture implemented in the ZC706 board by means of an FMC HPC connector. On the other hand, the emitter part is based on a custom design consisting of an IR LED emitting the LS sequences. A STM32 microcontroller is in charge of controlling the emission, which allows the sequences to be emitted and the frequency of the carrier to be varied.

The signals v_{sum} , v_{lr} , and v_{bt} acquired in the FPGA are uploaded to a computer, where they are processed offline in MATLAB© for validation's sake. A matched filtering with the emitted LS codes is applied, in order to obtain the final correlation signals c_{sum} , c_{lr} and c_{bt} , as shown in Fig. 7 for the corresponding acquired signals shown before in Fig. 5. It is possible to observe the correlation peaks for the three

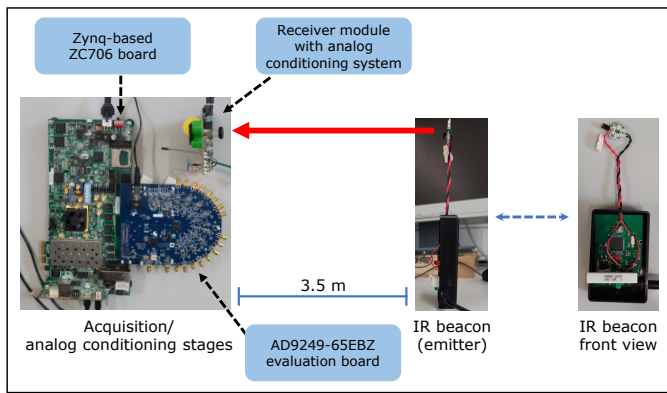


Fig. 6. Global overview of the experimental setup used for the validation of the proposal.

QADA channels, that can be used to estimate the final emitter's position.

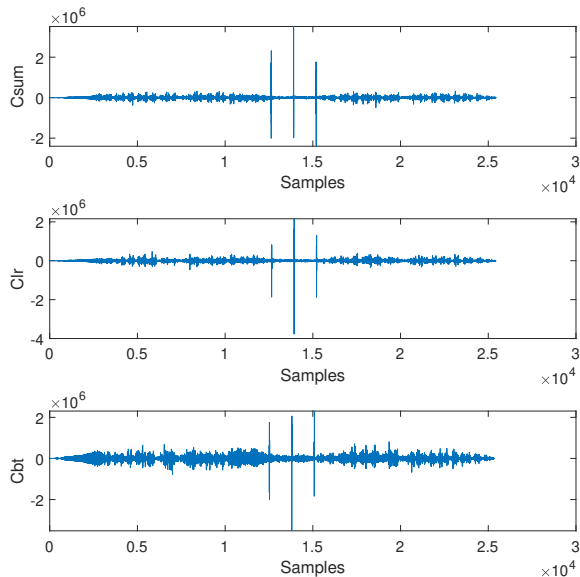


Fig. 7. Correlation signals, c_{sum} , c_{lr} , and c_{bt} , after processing the acquired signals shown in Fig. 5.

IV. CONCLUSIONS

A high-speed data acquisition system targeting the design of an infrared LPS has been proposed, developed and tested in this work. On the one hand, an analog front-end has been designed in order to correctly adapt and filter the signals coming from four QADA photoreceptors, as well as to provide an automatic gain control with high dynamic range to properly adjust the signals' voltages at the inputs of the analog-to-digital converter. On the other hand, an FPGA-based architecture has been developed to acquire the conditioned signals into the digital domain at sampling rates up to 16.25

Msp, with downsampling capabilities if necessary. Finally, an experimental setup with a LPS consisting of a LED emitter and a QADA receiver has been implemented, based on transmissions encoded with LS codes. The experimental signals have been processed offline, proving the successful operation of the proposal at the maximum sampling frequency of 16.25 Msp.

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