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# High Step-Up Reverse Coupled-Inductor Dual-Switch DC-DC Converter with Low Turn Ratio

Yuliang Ji, Lina Geng, Hongchen Liu, *Senior Member, IEEE* and Pat wheeler, *Fellow, IEEE*

***Abstract*-In this paper, a high step-up reverse coupled-inductor dual-switch (HS-RCLDS) DC-DC converter is presented. Through one reverse coupled-inductor cell, one capacitor and one diode to form voltage-double circuit when two switches are on at the same time, the proposed converter can produce the higher voltage gain, and turn ratio range varies only between 1 and 2, which is beneficial to coupled-inductor design with low leakage inductance. This voltage gain has the proportional relations with turn ratios and switch duty ratios. Also, the proposed converter owns continuous input current. Operation principles, derivation of voltage gain, component voltage stresses, parameter design, efficiency analysis and performance comparison of the proposed converter are described in detail. Finally, the experimental results are given out to verify the feasibility of the theoretical analysis.**

***Index Terms*—DC-DC converters, reverse coupled-inductor, dual-switch, high gain, continuous input current.**

## I. INTRODUCTION

WITH the widespread application of low-voltage dc power such as fuel cell supply system and PV micro converter system, DC-DC converters obtains great attention to boost low input voltage to high output voltage [1, 2].

When isolated DC-DC converters output high voltage gain, higher turn ratio will be needed. This will increase the leakage inductance and design difficulty of transformer, and then influence the system performance. Therefore, nonisolated DC-DC converters can become a more attractive solution for high voltage gain [3-5].

Traditional boost converter has low boost ability, the higher voltage gain will accompany extreme switch duty ratio [6]. In 2002, Z-source network was reported to achieve the single-stage voltage-boost inverter, subsequently used to DC-DC converters [7]. But its discontinuous input current and large startup impulse current constrict its application [8]. Through embedding the input source into Z-source network, embedded Z-source converter realizes continuous input current and lowers two capacitor stresses by introducing two input sources [9]. Quasi-Z-source converters [10] can lower voltage stresses across two capacitors when only using one input source. Based on impedance networks above, some improved structures are presented through introducing switched-inductor [11, 12], cascading structure [13], switched-capacitor [14-18], and coupled-inductor technology [19-26]. But DC-DC converters based on Z-source/Quasi-Z-source networks have higher variation relations between voltage gain and switch duty ratio, namely smaller range of switch duty ratio will result in higher range of voltage gain. This leads the larger current of circuit components in the high voltage gain, which will increase the losses and rating values of circuit components.

Switched-inductor, cascading structure and switched-capacitor technology largely improves the converter performance such as boost ability, input current state and lower voltage stresses of components, but introducing massive components. And yet coupled-inductor technology can form high-performance topology with lower component counts, which can be considered to achieve high boost ability. So, integrating coupled-inductor technology, some high-gain DC-DC converters [27, 28] are reported by moving the switches forward to make low-resistance MOSFET available and produce the higher boost ability. To further optimize the conversion performance, some dual-switch DC-DC converters with single inductors are presented in [29-31], but without higher voltage gain.

In this paper, a reverse coupled-inductor dual-switch DC-DC converter is presented. Through introducing coupled-inductor cell, proposed topology produces high boost ability in using smaller switch duty ratio, and own continuous input current. Turn ratio range of proposed converter varies only between 1 and 2, which is beneficial to coupled-inductor design with low leakage inductance. Theoretical analysis and experimental verification for proposed HS-RCLDS DC-DC converter is operated in detail as follows.

## II. PROPOSED HS-RCLDS CONVERTER

Fig.1 gives out topology structure of proposed HS-RCLDS DC-DC converter, which is constituted by two switches, two capacitors, one coupled-inductor cell and three diodes. Through simultaneously controlling two switches on or off to form voltage-double circuit, proposed HS-RCLDS obtains high boost ability and continuous input current. Because of the reverse coupled-inductor connection, this coupled-inductor turn ratio range is between 1 and 2, which is beneficial to coupled-inductor design with low leakage inductance. The following parts will give out operation principle, derivation of voltage gain, component stresses of voltage and current, parameter design, efficiency, design process and experimental verification.

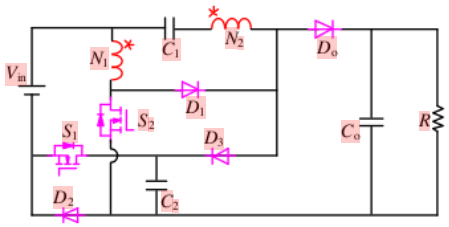


Fig.1 Proposed HS-RCLDS converter.

## III. THEORETICAL ANALYSIS

### A. Operation principles

In this part, we assume that coupled-inductor cell can be replaced for one magnetizing inductance $L_M$, one leakage inductance $L_k$ and one ideal transformer.

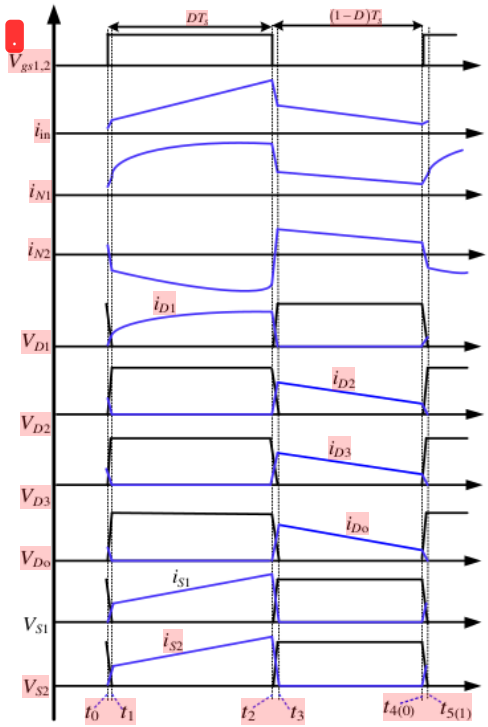


Fig.2 Theoretical waveforms.

In CCM, four operation stages of proposed converter can be described. Theoretical waveforms such as coupled-inductor cell, diodes and capacitors are plotted in Fig.2. Fig.3 gives out equivalent circuits of operation states above.

Stage I [$t_1$-$t_2$], equivalent circuit with conductive two switches is described in Fig.3 (a). It can be seen that power $V_{in}$, capacitor $C_2$ and coupled-inductor cell form the conduction path by two switches. Based on magnetic coupled theory, the windings ($N_1$ and $N_2$), and the leakage inductance $L_k$ charge capacitor $C_1$ by diode $D_1$. Diodes ($D_2$, $D_3$ and $D_o$) with reverse voltage are not conductive, and capacitor $C_o$ independently supplies the power for the load $R$.

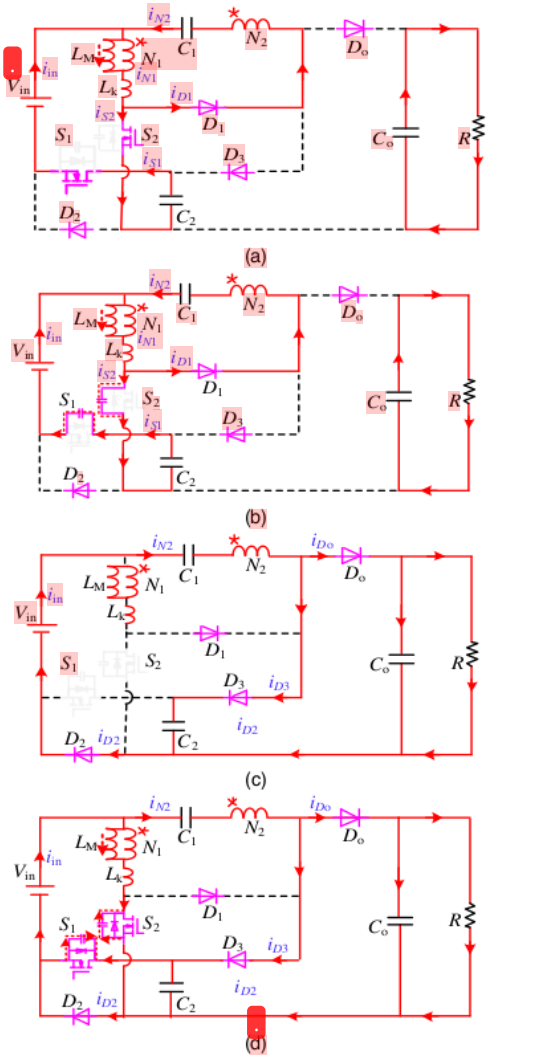


Fig.3 Equivalent circuits of operation stages (a) Stage I (b) Stage II (c) Stage III (d) Stage IV.

Stage II [$t_2$-$t_3$], at time $t_2$, two switches are turned off. Fig.3 gives out equivalent circuit in this stage. power $V_{in}$, leakage inductor $L_k$, magnetizing inductance $L_M$ and capacitor $C_2$ charge the parasitic capacitors of two switches. At time $t_3$, operation states of two switches are not ungated, and then diodes ($D_2$, $D_3$ and $D_o$) are conductive. This interval is finished.

Stage III [$t_3$-$t_4$], two switches are off. Equivalent circuit is described in Fig.3 (c). Based on the volt-second balance principle, the voltage polarity of windings when two switches are off is contrary to that when switches are on. So, the input source $V_{in}$, winding $N_2$, and capacitor $C_1$ charge the capacitors ($C_1$ and $C_o$) and load $R$ through didoes ($D_2$, $D_3$ and $D_o$), and then the diode $D_1$ is reversed. The current of winding $N_1$ drops to zero. Since current balance principle of coupled-inductor cell, current of winding $N_2$ produces a sudden drop.

Stage IV [$t_{4(0)}$-$t_{5(1)}$], at time $t_{4(0)}$, two switches are turned on. Fig.3 (d) gives out equivalent circuit in this operation state. The energy of the parasitic capacitor discharges by two switches. From Fig.3 (d), it can be seen that power $V_{in}$ and coupled-inductor cell form conduction path by two switches. Till to time $t_{5(1)}$, the energy of the parasitic capacitor is run out. This interval is finished.

### B. Derivation of voltage gain and voltage stresses

The operation states (stage II and stage IV) are very transient to be ignored. According to equivalent circuit of stage I, we have

$$V_{in}+V_{C2}-V_{LkI}-V_{N1I}=0 \quad (1)$$

$$V_{C1}=(N-1)V_{N1I}-V_{LkI} \quad (2)$$

$$V_{Do}=V_{D2}=V_{D3}=V_{C2}=V_{Co} \quad (3)$$

Where $V_{in}$ is input voltage. $V_{N1I}$ is voltage of coupled-inductor winding $N_1$ in stage I. $V_{C1}$, $V_{C2}$, $V_{Co}$ express the voltages of capacitors ($C_1$, $C_2$, $C_o$). $V_{LkI}$ expresses voltage of leakage inductance in stage I. $V_{D2}$, $V_{D3}$, $V_{Do}$ express the voltages of diodes ($D_2$, $D_3$, $D_o$). $N$ is turn ratio expressed by $N=N_2/N_1$.

For convenience of analysis, the relation between the leakage inductance $L_k$ and magnetizing inductance $L_M$ are defined by the equation (4):

$$k=\frac{L_M}{L_M+L_k} \quad (4)$$

Where $k$ expresses coupling coefficient of coupled-inductor cell. Therefore, the following equations can be obtained.

$$V_{N1I}=kV_{in}+kV_{C2} \quad (5)$$

$$V_{C1}=(N-1-\frac{1-k}{k})V_{N1I} \quad (6)$$

According to equivalent circuit of stage III, the following equations can be obtained.

$$V_{in}+V_{C1}-NV_{N1III}=V_{Co} \quad (7)$$

$$V_{C1}+(1+\frac{1-k}{k}-N)V_{N1III}=V_{D1} \quad (8)$$

Where $V_{N1III}$, $V_{N2III}$ express voltages of windings ($N_1$ and $N_2$) in stage III. $V_{D1}$ expresses the voltage of diode $D_1$.

In charging and discharging stages, inductor has the same volt second value, as follows.

$$\int_0^{DT_s} V_{N1I}dt+\int_{DT_s}^{T_s} V_{N1III}dt=0 \quad (9)$$

By submitting the equations (5-8) to the equation (9), output voltage and voltage gain are obtained.

$$V_{Co}=GV_{in}=\frac{kNV_{in}}{2-kN-2D} \quad (10)$$

As listed in the equation (10), turn ratio of proposed converter can range from 1 to 2, this lower turn ratio is beneficial to coupled-inductor design with low leakage inductances.

In $k$=1, voltage gain and device voltage stresses can be obtained by the equation (11).

$$\begin{cases} G=\dfrac{N}{2-N-2D} \\ V_{C1}=\dfrac{2(N-1)(1-D)V_{in}}{2-N-2D},\quad V_{C2}=\dfrac{NV_{in}}{2-N-2D} \\ V_{D1}=\dfrac{2(N-1)V_{in}}{2-N-2D},\quad V_{D2}=V_{D3}=\dfrac{NV_{in}}{2-N-2D} \\ V_{S1}=\dfrac{NV_{in}}{2-N-2D},\quad V_{S2}=\dfrac{(2-N)V_{in}}{2-N-2D} \end{cases} \quad (11)$$

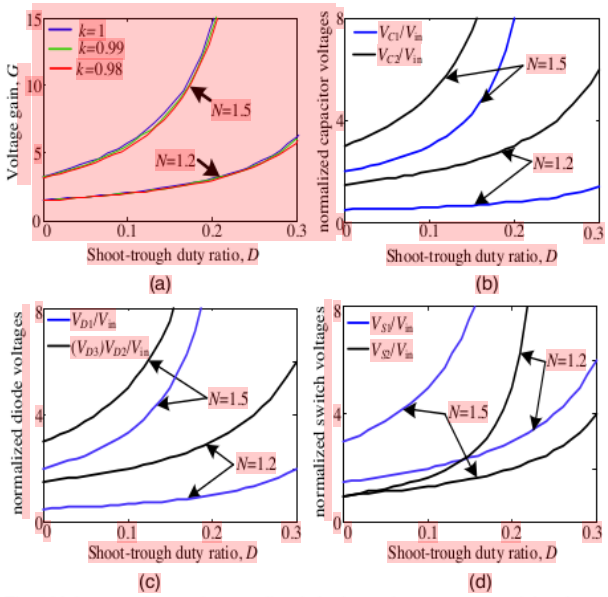


Fig.4 Voltage gains and normalized device voltage stresses (a) voltage gain with various coupling coefficient (b) capacitor stresses (c) diode stresses (d) switch stresses.

Fig. 4 (a) gives out voltage gains under the various coupling coefficients and switch duty ratios. As shown in Fig.4 (a), voltage gain increases as coupling coefficient increases. Also, it can be known that voltage gain has the positive relation with switch duty ratio and turn ratio. Normalized device voltage stresses under various turn ratios and switch duty ratios are described in Fig. 4 (b, c, d). From Fig.4 (b, c), it can be seen that voltage stresses of capacitors and diodes increases as switch duty ratio and turn ratio increase. As shown in Fig.4 (d), the voltage of switch $S_2$ has inversely proportional relation with turn ratios, and then the voltage of switch $S_1$ has proportional relation with turn ratios.

### C. Derivation of current stresses

According to power balance principle of capacitors, average currents through diodes ($D_o$, $D_1$, $D_2$ and $D_3$) are obtained in one cycle.

$$I_{Do\,[t_2,t_5]}=\frac{V_{in}N}{(2-N-2D)R} \quad (12)$$

$$I_{D1[t_0,t_1]}=\frac{\int_0^{T_s} i_{D1}dt}{T_s}=\frac{V_{in}(2-2D)(N+1)D^2T_s}{2NL_{N1}(2-N-2D)} \quad (13)$$

$$I_{D2[t_2,t_5]}=\frac{\int_0^{T_s} i_{D2}dt}{T_s}=\frac{V_{in}(N-ND)D^2T_s}{L_{N2}(2-N-2D)} \quad (14)$$

$$I_{D3[t_0,t_3]}=\frac{V_{in}(1-D)D^2T_s}{NL_{N1}(2-N-2D)} \quad (15)$$

Where $R$ is the load, $L_{N1}$ and $L_{N2}$ are the inductor values of windings ($N_1$ and $N_2$), and then $i_{D1}$, $i_{D2}$, $i_{D3}$, $i_{Do}$ express the transient current of diodes ($D_o$, $D_1$, $D_2$, $D_3$).

According to operation states when two switches are on and off, average currents of switches ($S_1$ and $S_2$) can be calculated as follows.

$$I_{S1[t_0,t_3]}=\frac{V_{in}(1-D)D^2T_s}{L_{N1}(2-N-2D)} \quad (16)$$

$$I_{S2[t_0,t_3]}=\frac{V_{in}(2-2D)D^2T_s}{2L_{N1}(2-N-2D)} \quad (17)$$

So, according to the current equations above, the average currents of windings ($N_1$ and $N_2$) are expressed by the following equations.

$$I_{N1[t_0,t_3]}=\frac{V_{in}(1-D)(N+1)D^2T_s}{NL_{N1}(2-N-2D)} \quad (18)$$

$$\left|I_{N2[t_0,t_3]}\right|=\frac{V_{in}(2-2D)(N+1)D^2T_s}{NL_{N1}(2-N-2D)} \quad (19)$$

## IV. Parameter Design and Performance Comparison

### A. Design of capacitors and inductors

Design of coupled-inductor cell and capacitors at the boundary between CCM and DCM will be given out as follows. Transient process is neglected, and Fig.5 gives out relevant theoretical waveforms.

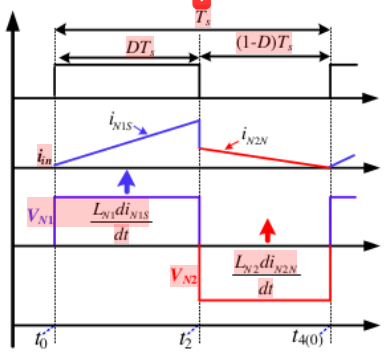


Fig.5 Theoretical waveforms in one cycle.

When two switches are conductive, the current and voltage of windings ($N_1$ and $N_2$) has the following relations.

$$V_{N1S}=\frac{L_{N1}di_{N1S}}{dt}=V_{in}+V_{C2} \quad (20)$$

So, the current and voltage of windings ($N_1$ and $N_2$) are obtained by the equation (21).

$$\left|V_{N2N}\right|=N\left|V_{N1N}\right|=\frac{ND(2-D)}{(2-N-2D)(1-D)}=\frac{N^2L_{N1}di_{N2N}}{dt} \quad (21)$$

Since input currents are formed by current of winding $N_1$ under conductive switches and current of winding $N_2$ under off switches, therefore average input current is obtained through combing equations (20-21).

$$\bar{i}_{in}=\frac{V_{in}(1-D)(N+1)D^2T_s}{NL_{N1}(2-N-2D)} \quad (22)$$

The output current is calculated by the following equation.

$$i_o=\frac{V_{in}N}{(2-N-2D)R} \quad (23)$$

In theory, input power is equal to output power. Therefore, the inductor values of windings ($N_1$ and $N_2$) at the boundary between CCM and DCM are obtained as follows.

$$L_{N1}=\frac{(1-D)(N+1)(2-N-2D)RD^2T_s}{N^3} \quad (24)$$

$$L_{N2}=\frac{(1-D)(N+1)(2-N-2D)RD^2T_s}{N} \quad (25)$$

If the designed inductor values of windings ($N_1$ and $N_2$) are higher than those calculated by the equations (24) and (25), the inductor current will be continuous, otherwise be discontinuous.

According to equation (26), it can be kwon that the voltage fluctuation of capacitors mainly is produced by the charging or discharging currents of capacitors.

$$i=CdV/dt \quad (26)$$

Where $C$ expresses capacitor value, and $i$ expresses capacitor current. Therefore, maximum voltage fluctuation of capacitors origins from the maximum value between charging current and discharging currents of capacitors. So, capacitors ($C_1$, $C_2$, $C_o$) can be selected through following equations (27-29), respectively.

$$\frac{V_{in}(2-2D)D^2T_s^2}{NL_{N1}(2-N-2D)\Delta V_{C1}}\le C_1 \quad (27)$$

$$\frac{V_{in}(2-2D)D^2T_s^2}{L_{N1}(2-N-2D)\Delta V_{C2}}\le C_2 \quad (28)$$

$$\frac{V_{in}RDT_s(2-2D)-V_{in}L_{N2}}{L_{N1}(2-N-2D)\Delta V_{Co}}\le C_o \quad (29)$$

Where $\Delta V_{C1}$, $\Delta V_{C2}$ and $\Delta V_{Co}$ express voltage fluctuation of corresponding capacitors.

### B. Feature comparisons

To prove feature advantages of proposed converter, two converters [21, 29] are made the comparison with proposed converter. The voltage gains $G$, capacitor voltages except output capacitor ($V_{C1}$ and $V_{C2}$), diode voltages ($V_{D1}$, $V_{D2}$, $V_{S2}$) except output diode, switch voltages ($V_{S1}$ and $V_{S2}$), and component counts $C$ of three converters above are given in

Table I.

Table I Parameter comparisons

| Topology | Converter [21] | Converter [29] | Proposed converter |
|---|---|---|---|
| $G$ | $\frac{1}{1-KD}$ | $\frac{1+(2N+1)D}{1-D}$ | $\frac{N}{2-N-2D}$ |
| $V_{S1}$ | $\frac{V_{in}}{1-KD}$ | $\frac{V_{in}}{1-D}$ | $\frac{NV_{in}}{2-N-2D}$ |
| $V_{S2}$ | No | $\frac{V_{in}}{1-D}$ | $\frac{(2-N)V_{in}}{2-N-2D}$ |
| $V_{C1}$ | $\frac{(1-D)V_{in}}{1-KD}$ | $\frac{V_{in}}{1-D}$ | $\frac{2(N-1)(1-D)V_{in}}{2-N-2D}$ |
| $V_{C2}$ | $\frac{(K-1)DV_{in}}{1-KD}$ | $\frac{V_{in}}{1-D}$ | $\frac{NV_{in}}{2-N-2D}$ |
| $V_{D1}$ | $\frac{(K-1)V_{in}}{1-KD}$ | $\frac{2NV_{in}}{1-D}$ | $\frac{2(N-1)V_{in}}{2-N-2D}$ |
| $V_{D2}$ | No | $\frac{2NV_{in}}{1-D}$ | $V_{D2}=V_{D3}=\frac{NV_{in}}{2-N-2D}$ |
| $C$ | 7 | 10 | 10 |

From Table I, it can be seen that proposed converter uses same component count with converter [29], and is higher than the other converter [27].

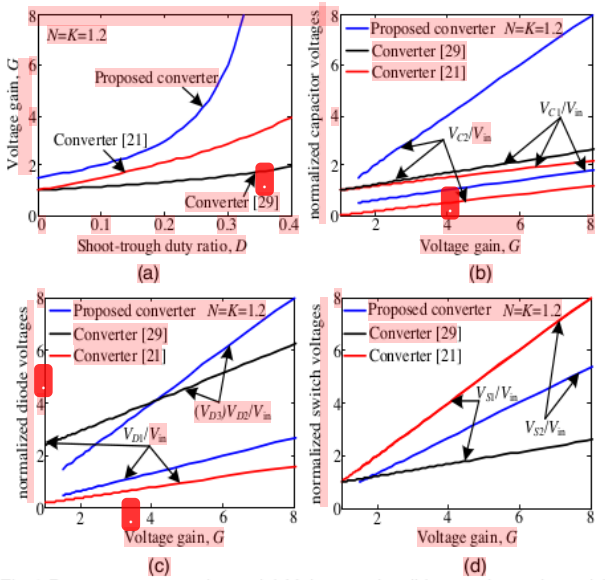


Fig.6 Parameter comparisons (a) Voltage gains (b) capacitor voltage (c) diode voltage (d) switch voltage.

The parameter comparisons among converters [21, 29] and proposed converter have been made and given in Fig.6. Voltage gain comparison is given in Fig.6 (a). The proposed converter owns the highest voltage gain, compared with converters [21, 29].

Fig.6 (b) gives out comparison of normalized capacitor voltage stresses. As shown in Fig.6 (b), proposed converter produces the highest voltage stress across capacitor $C_2$, and owns the lowest voltage stress across capacitor $C_1$, compared with converters [21, 29].

The comparison of normalized diode voltage stresses is made. A shown in Fig.6 (c), the voltage stress on diode $D_1$ of proposed converter is lower than that of converter [29], and then higher than that of converter [21]. Also, it can be found that the voltage stresses on diode $D_{2,3}$ of proposed converter are lower than that of converter [29], when voltage gain is lower than 4. And then the voltage stresses on diode $D_{2,3}$ of proposed converter are highest in other voltage gain range.

The comparison of normalized switch voltage stresses is shown in Fig.6 (d). It can be found that The voltage stress on switch $S_1$ of proposed converter is equal to that of converter [21], and higher than that of converter [29]. The voltage stress on switch $S_2$ of proposed converter is lowest compared to converters [21, 29].

According to the parameter comparisons above, it can be found that proposed converter owns high boost ability, and realizes lower voltage stress on partial circuit components.

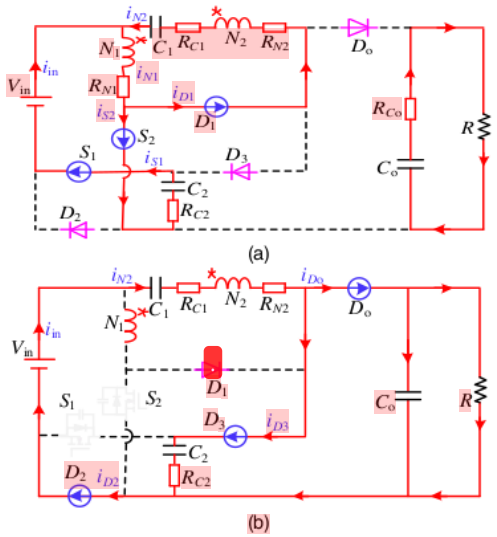


Fig.7 Equivalent circuits of efficiency analysis (a) when switch is on (b) when switch is off.

## V. EFFICIENCY ANALYSIS

In this efficiency analysis, the equivalent resistances of windings ($N_1$ and $N_2$) and capacitors ($C_1$, $C_2$ and $C_o$) are expressed by $R_{N1}$, $R_{N2}$, $R_{C1}$, $R_{C2}$, $R_{Co}$. The equivalent voltage drop of diodes ($D_1$, $D_2$, $D_3$ and $D_o$) and switches ($S_1$ and $S_2$) is uniformly expressed by $V_{SD}$. Neglecting the transient operation states (stage II and stage IV) and leakage inductance influence, equivalent circuits of stage I and stage III are shown in Fig.7.

According to the aforementioned current stress calculation of circuit components, the losses of capacitors, switches, diodes, and coupled-inductor cell are expressed by the equation (30-33).

$$P_{C\text{-}loss}=\frac{4V_{in}^2(1-D)^2D^4T_s^2[R^2(N+1)^2R_{C1}+R^2R_{C2}]+4V_{in}^2N^4L_{N1}^2R_{Co}}{N^2L_{N1}^2(2-N-2D)^2R^2} \quad (30)$$

$$P_{S\text{-}loss}=\frac{2V_{in}(1-D)D^2T_sV_{SD}}{L_{N1}(2-N-2D)} \quad (31)$$

$$P_{D\text{-}loss}=\frac{V_{in}[(1-D)(N+2)RD^2T_s+N^2L_{N1}]V_{SD}}{NL_{N1}(2-N-2D)R} \quad (32)$$

$$P_{CL\text{-}loss}=\frac{V_{in}^2(1-D)^2(N+1)^2D^2T_s(R_{N1}+4R_{N2})}{N^2L_{N1}^2(2-N-2D)^2} \quad (33)$$

The input power is calculated as follows.

$$P_{in}=\frac{V_{in}^2(2-2D)(N+1)D^2T_s}{2NL_{N1}(2-N-2D)} \quad (34)$$

So, the efficiency can be expressed as follows.

$$\eta=\frac{P_{in}-P_{C\text{-}loss}-P_{S\text{-}loss}-P_{D\text{-}loss}-P_{CL\text{-}loss}}{P_{in}} \quad (35)$$

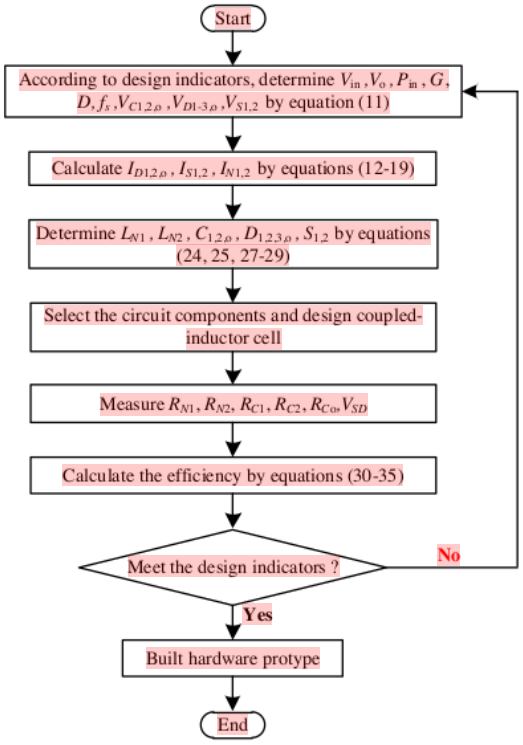


Fig.8 Design process of proposed converter

## VI. Design Process of Converter

Aiming to the specific application circumstance, through the known parameters and performance indicators, design process of proposed converter has been given in Fig.8.

## VII. Experiment Results

To prove performances and operation feasibility of proposed converter, the experimental protype is built according to the parameters in Table II. This hardware picture is shown in Fig.9.

Fig.10 gives out experimental results when $V_{in}$=40V and $N$=1.2. Fig.10 (a) gives out experimental waveforms of input voltage and output voltage, whose values are about 40V and 228V. Fig.10 (b) gives out experimental waveforms of capacitors ($C_1$ and $C_2$). The corresponding experimental values are about 51V and 227V. Fig.10 (c) gives out experimental waveforms of diodes ($D_1$ and $D_2$), whose peak values are about 73V and 227V. Fig.10 (d) gives out experimental waveforms of diodes ($D_3$ and $D_o$), whose peak values are close about 226V and 228V. Fig.10 (e) gives out experimental waveforms of coupled-inductor windings ($N_1$ and $N_2$), the current ranges of windings ($N_1$ and $N_2$) respectively vary from 0 to 16A and -9A to 6A to 1.5A. Fig.10 (f) gives out the experimental waveforms of switch voltages, and the experimental peak values are about 153V and 227V.

Table II Experiment device specifications

| Parameter/Description | Parameter/Value |
|---|---|
| Input Voltage $V_{in}$ | 40V and 50V |
| Output Voltage $V_o$ | 240V and 300V |
| Switch frequency $f_s$ | 50kHz |
| Output power | 200W |
| Capacitor $C_1$ | 220uF |
| Capacitor $C_2$ | 470uF |
| Capacitor $C_o$ | 470uF |
| Magetic core material | PC40 |
| Turn ratio ($N$) | $N$=1.2 |
| Diode ($D_1$, $D_2$, $D_3$, $D_o$) | 60EPU06 |
| Switch ($S_1$, $S_2$) | IPW65R019C7 |

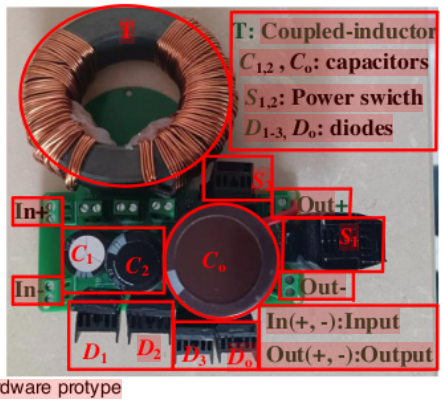


Fig.9 Hardware protype

The experimental results of proposed converter when input voltage $V_{in}$=50V and turn ratio $N$=1.2 are shown in Fig.11. Fig.11 (a) gives out the experimental waveforms of input voltage and output voltage, whose values are about 50V and 289V, respectively. Fig.11 (b) gives out the experimental waveforms of capacitors ($C_1$ and $C_2$). The corresponding experimental values are about 65V and 288V. Fig.11 (c) shows the experimental waveforms of diodes ($D_1$ and $D_2$), whose peak values are about 93V and 287V, respectively. Fig.11 (d) shows the experimental waveforms of diodes ($D_3$ and $D_o$), whose peak values are close about 288V and 229V. The experimental waveforms of coupled-inductor windings ($N_1$ and $N_2$) are shown in Fig.11 (e), it can be seen that the current ranges of windings ($N_1$ and $N_2$) respectively varies from 0 to 15A and -8.5A to 5A to 1A. Fig.11 (f) gives out the experimental waveforms of switch voltages. As shown in Fig.11 (f), the experimental peak values are about 195V and 288V, respectively.

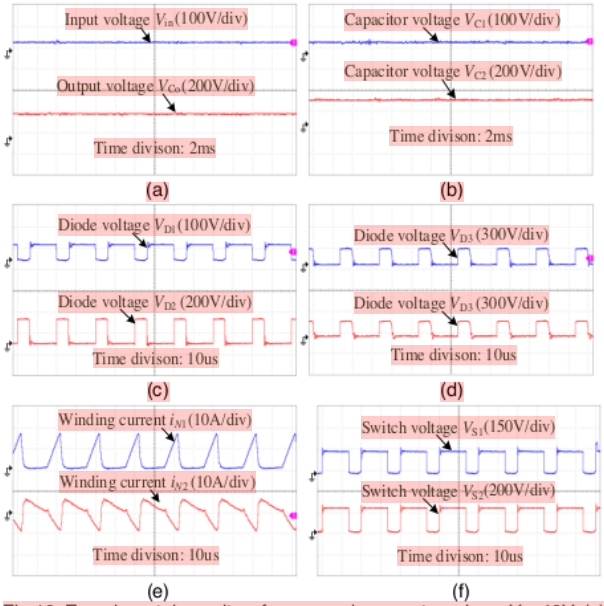


Fig.10 Experimental results of proposed converter when $V_{in}$=40V (a) input voltage and output voltage (b) voltages of capacitors ($C_1$ and $C_2$) (c) voltages of diodes ($D_1$ and $D_2$) (d) voltages of diodes ($D_3$ and $D_o$) (e) currents of windings ($N_1$ and $N_2$) (f) voltages of switches ($S_1$ and $S_2$).

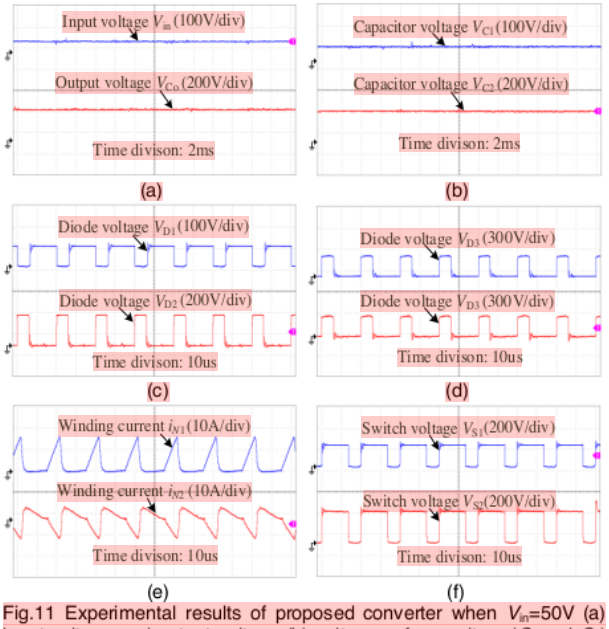


Fig.11 Experimental results of proposed converter when $V_{in}$=50V (a) input voltage and output voltage (b) voltages of capacitors ($C_1$ and $C_2$) (c) voltages of diodes ($D_1$ and $D_2$) (d) voltages of diodes ($D_3$ and $D_o$) (e) currents of windings ($N_1$ and $N_2$) (f) voltages of switches ($S_1$ and $S_2$).

The experiment results above are very close to theoretical values, and can verify the high boost ability of proposed converter when using the low turn ratio $N$=1.2. Also, according to currents of windings, it can be obtained that the proposed converter realizes the continuous input current.

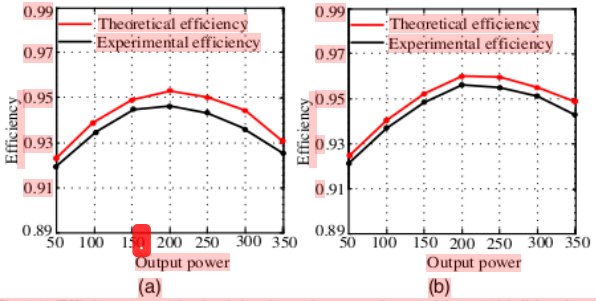


Fig.12 Efficiency analysis (a) when input voltage $V_{in}$ = 40V (b) when input voltage $V_{in}$ = 50V.

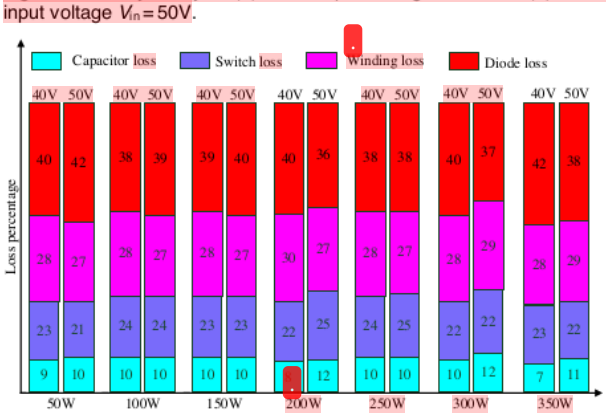


Fig.13 Loss distribution when input voltage $V_{in}$ = 40V and $V_{in}$=50V.

The efficiency analysis of proposed converter is operated when turn ratio $n$=1.2, input voltage $V_{in}$=40V and $V_{in}$=50V. The efficiency is tested by each 50W when the output range of converter power varies from 50W to 350W. Fig.12 gives out the corresponding theoretical efficiency and experimental efficiency. As shown in Fig.12, experimental efficiency value is higher to 94.6% in $V_{in}$=40V and higher to 95.3% in $V_{in}$=50V when output power is 200W, and very close to theoretical efficiency value. Also, the efficiency when $V_{in}$=50V is higher than that when $V_{in}$=40V, especially when output power is greater than 100W. The loss distribution for experiment results above is analyzed and shown in Fig.13.

## CONCLUSION

This paper proposes a high step-up reverse coupled-inductor dual-switch DC-DC converter. The high voltage gain can be produced by using the coupled-inductor cell with low turn ratio, which is beneficial to design of coupled-inductor cell. Through analyzing the operation states, voltage gain, voltage stresses of components, design of capacitors and inductors, efficiency analysis and making the comparisons with other converters, the following conclusion can be obtained. The proposed converter can realize the continuous input current, and produce the higher voltage gain when turn ratio $N$=1.2. The partial diode voltage and switch voltage are lower, and then other diode voltage and switch voltage is same with output voltage. The experimental protype is built by given design process, and the corresponding experimental results verify the feasibility of the theoretical analysis. Finally, the

efficiency analysis is operated, it can be seen that the efficiency in different input voltages is different. This efficiency can be increased by increasing the input voltage in the same output power.

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Yuliang Ji received the B.S. degree in electrical engineering from Harbin University of Science and Technology (HUST), Harbin, China, in 2012, and the M.S. degree in electrical engineering from HUST, Harbin, in 2015. He received the Ph.D. degree in electrical engineering from Harbin Institute of Technology (HIT). He worked in school of electrical engineering in Northeast Electric Power University. His current research interests include converter topologies and motor drives.

Lina Geng, received the B.S. degree in electrical engineering from Harbin University of Science And Technology (HUST), Harbin, China, in 2013, and the M.S. degree and Ph.D. degree in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2015 and 2019. She worked in school of electrical and electronic engineering in Changchun University of Technology. Her current research interest is permanent magnet synchronous machines.

Hongchen Liu (Senior Member, IEEE) received the B.S. in electrical engineering from Northeast Agricultural University, Master and Ph.D degrees in electrical engineering from Harbin Institute of Technology (HIT), Harbin, China, in 2001, 2003, and 2007, respectively. In 2009, he joined the Department of Electrical Engineering, where he has been an Professor since 2019. His current major research interests include DC/DC converter and inverter in photovoltaic system and Matrix converter.

PAT WHEELER (Fellow, IEEE) received the B.Eng. degree (Hons.) from the University of Bristol, U.K., in 1990, and the Ph.D. degree in electrical engineering for his work on Matrix Converters from the University of Bristol, U.K., in 1994. In 1993, he moved to the University of Nottingham and worked as a Research Assistant in the Department of Electrical and Electronic Engineering. In 1996, he became a Lecturer at the Power Electronics, Machines and Control Group, University of Nottingham, U.K. Since January 2008, he has been a Full Professor with the Power Electronics, Machines and Control Group. He was the Head of the Department of Electrical and Electronic Engineering, University of Nottingham, from 2015 to 2018. He is currently the Head of the Power Electronics, Machines and Control Research Group, and the Global Director of the University of Nottingham's Institute of Aerosapce Technology. He has published 500 academic publications in leading international conferences and journals. He was an IEEE PELs Distinguished Lecturer, from 2013 to 2017. He is a member of the IEEE PELs AdCom.

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