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SiC MOSFET vs SiC/Si Cascode short circuit robustness benchmark

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A B S T R A C T

Nowadays, MOSFET SiC semiconductors short circuit capability is a key issue. SiC/Si Cascodes are compound semiconductors that, in some aspects, show a similar MOSFET behaviour. No interlayer dielectric insulation suggests, in theory, Cascode JFETs as more robust devices. The purpose of this paper is to compare the drift and degradation of two commercial devices static parameters by exposing them to different levels of repetitive 1.5 μs short-circuit campaigns at 85% of its breakdown voltage. Short-circuit time has been set experimentally, and longer times result in catastrophic failure of MOSFET devices due to over self-heating. For this purpose, pre- and post-test short circuit characterizations are presented.

1. Introduction

Design of solid state high voltage DC (HVDC) protections requires high voltage devices with fast switch-off times and, in case of current limiting capabilities, high temperature working conditions capability. The electrical properties of SiC devices make these power transistors interesting for this application. Due to the criticality of the application, it is essential to study such devices from the reliability point of view.

Normally-off are the most common devices in solid state protections. In SiC technology, normally-off MOSFET and normally-off SiC/Si Cascode are the most used devices. MOSFETs are much more employed than Cascodes, although they have a similar DC and switching performance.

From the electronic reliability point of view, it is well known that SiC MOSFET degradation differs from its Si counterpart [1]. Some reliability key points under study are the gate oxide degradation [2] and the threshold voltage instabilities and drifts [3–5]. These effects have been already studied for SiC MOSFET devices, however, there is lack of reliability data reported on commercial SiC/Si Cascode devices.

Standard normally-off SiC/Si Cascode structure consists on a normally-on SiC JFET, and a low voltage Si MOSFET. In Fig. 1 it is shown the Cascode symbol and its simplified internal structure. The SiC JFET blocks the high voltage, while Si MOSFET provides turn-on and turn-off control. The absence of gate oxide in JFET transistors seems, a priori, an advantage in terms of device reliability, however, any potential degradation effect in the JFET transistor must be measured indirectly [6].

The aim of this paper is to compare the aging of SiC MOSFET and SiC/Si Cascode devices under high voltage stress short circuit (SC) conditions, similar to what can be expected in fast-response solid-state HVDC protection systems [7].

For this purpose, pre- and post-test characterization has been performed using a Keysight B1505A Power Device Analyser.

Three different number of short-circuit repetitions have been established (100SC, 140SC and 200SC). During the short circuit, the power device stands at 85% of its maximum blocking voltage capability. V_{GS} has been set accordingly to manufacturer's recommendations; however, a lower V_{GS} condition (8.5 V) has been also tested, since it is typical value for some MOSFET photovoltaic drivers used in DC protections [7]. The total population of SiC MOSFET and SiC/Si Cascode tested are 20 for each device.

To end this section, the work is structured as follows: Section 2 details the experimental setup. Test results and discussion are presented in Section 3. The work ends with the conclusions in Section 4.

2. Experimental setup

2.1. Device under test (DUT)

For this study, MOSFET C2M0080120D from CREE [8] and SiC/Si Cascode UJC1206K from United Silicon Carbide Inc. [9], have been chosen. As shown in Table 1, they have similar electrical characteristics and both are TO-247-3L packaged.

2.2. Short circuit setup

Short circuit tests were performed at the Aalborg University in Center of Reliable Power Electronics (CORPE) using the Non Destructive Testing (NDT) Setup. The NDT setup allows repetitive and

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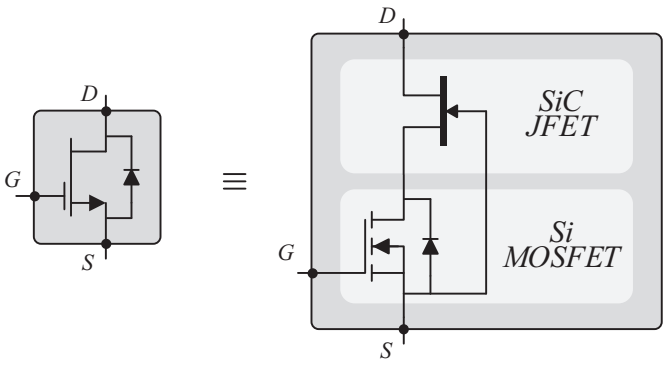

Fig. 1. Symbol and SiC/Si Internal Cascode structure.

Table 1
C2M0080120D & UJC1206K characteristics.

Device	$V_{DS\ max}$ [V]	$I_{D\ max}$ [A]	R_{on} [mΩ]
C2M0080120D	1200	36	80
UJC1206K	1200	38	60

controlled short circuits tests. It consists of a bank of ten high voltage (2400 V) and high capacity (500 μF) capacitors (ES50.S34-504NTO – Electronicon) supplied by a high voltage power source (TS 6U – Magna Power Electronics). The capacitors are connected to the *DUT* through a *SERIES* protection consisting of 4 IGBT modules (DIM1500ESM33 – DYNEX), in order to prevent the capacitors discharge in case of *DUT* short circuit failure. A PCB with the *DUT* and a driver is connected to the *SERIES* protection. CPWR-AN10 from CREE was used as the *DUT* driver. This driver allows V_{GS} adjustment in a simple way. The setup is controlled by a personal computer connected to a *FPGA* (DE2-115 – Altera) and an oscilloscope (HOD 6104-MS – LeCroy) which acquires V_{GS}, I_S and V_{DS}. The *FPGA* controls the *SERIES* protection and the *DUT* driver. The setup is optimized in terms of parasitic inductance (< 50 μH). The complete setup diagram is shown in Fig. 2.

2.3. Aging parameters

Threshold gate voltage ($V_{GS(TH)}$), drain-source leakage current (I_{DSS}), and R_{on} have been used as aging indicators. These indicators are common parameters to identify the semiconductor aging level [2,3].

In order not to interfere with the short circuit campaign process, the characterization was performed before and after test. Degradation process has been analysed for three different number of short circuits repetitions, as a percentage of a maximum (100%, 75% and 50%). For each condition, 5 samples were tested in order to get representative results. However, variations between devices are very low. For this reason and for the sake simplicity only one trace, the closest to the mean, is shown in Figs. 3,4,5,6.

3. Experimental results and discussion

3.1. Test definition

Test voltage has been set to 1000 V, which represents the 85% of breakdown *DUTs* voltage, please refer to Table 1. In our knowledge there are no previous studies in similar conditions, so this test results can be useful to optimize derating values in some applications. V_{GS} was the recommended by manufacturers; V_{GS} = 0 V for off state in both *DUTs* and V_{GS} = 20 V for C2M0080120D and V_{GS} = 12 V for UJC1206K for on state.

The maximum short circuit time both DUT_S can handle under these test conditions was checked experimentally. Experimental results show that C2M0080120D is the weakest device, the maximum short circuit time it can handle, in these conditions, is 1.5 μs, for higher short circuit time, the device is destroyed by overheating. As 1.5 μs is enough for fast-response HVDC protections [7], short circuit time has been set

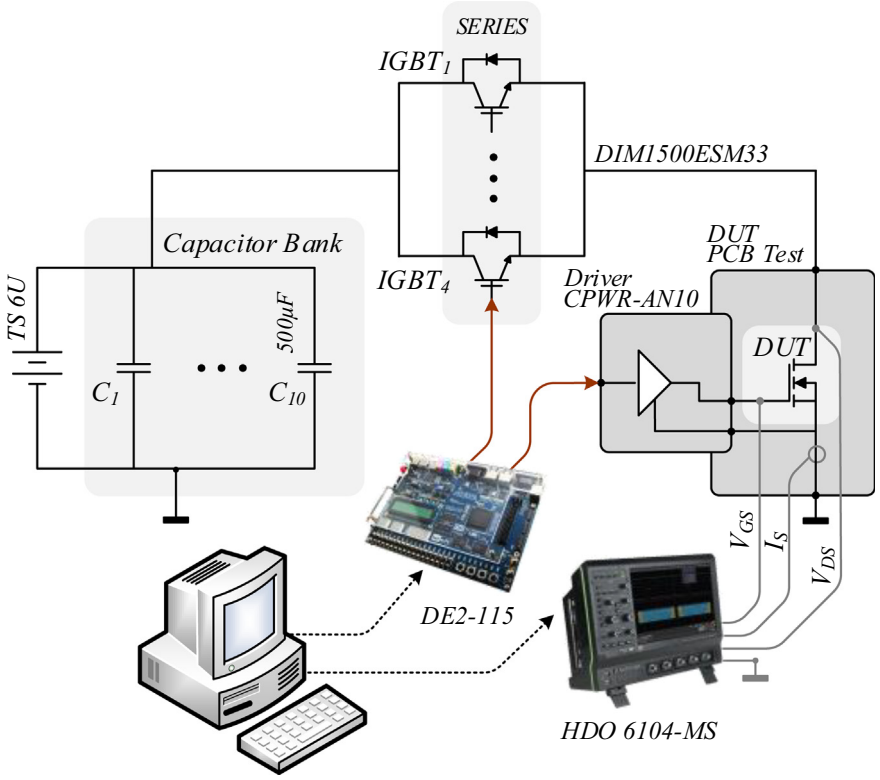

Fig. 2. *NDT* setup. MOSFET device symbol as *DUT* example.

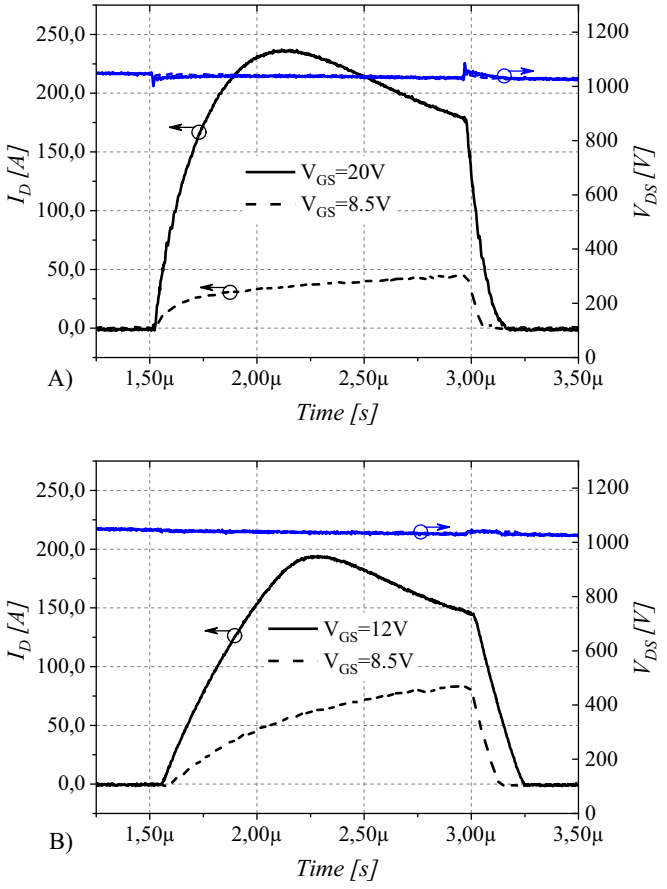

Fig. 3. Short circuit test waveforms at VDS = 1000 V.
A) C2M0080120D waveforms. In left Axis ID (Black) in right Axis VDS (Blue) B) UJC1206K waveforms. In left Axis ID (Black) in right Axis VDS (Blue). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

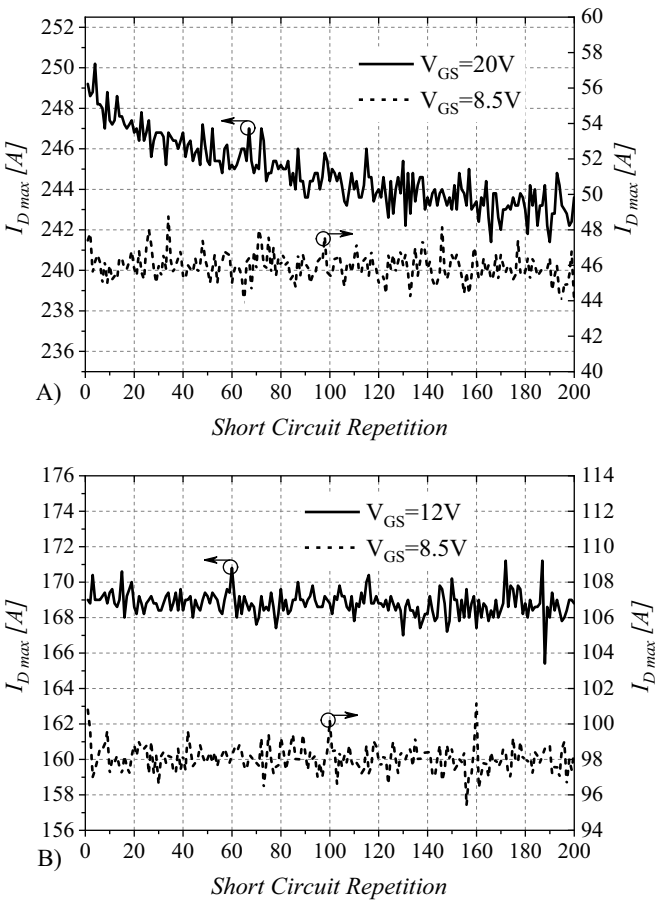

Fig. 4. Peak currents during 200SC test at V_{DS} = 1000 V.
A) C2M0080120D peak current evolution.
B) UJC1206K peak current evolution.

1.5 µs for all tests.

The number of short circuits performed was: 200, 140 and 100 using the recommended manufacturer V_{GS}, and 200 using V_{GS} = 8.5 V. A thermal relaxation interval of 20 s was left between short circuits, and all tests were performed at a room temperature of 19 °C. The handled short circuit energy in these tests is 0.3 J and 0.25 J for the C2M0080120D and UJC1206K respectively. When V_{GS} = 8.5 V the handled energy is 0.54 J and 0.087 J for the C2M0080120D and UJC1206K respectively.

In Fig. 3 it is shown the short circuit test waveforms for both *DUTs*. As can be seen, the UJC1206K peak current is 193 A, while the C2M0080120D peak current reaches 236 A using the recommended V_{GS}. This is due to the lower UJC1206K JFET saturation current. When V_{GS} = 8.5 V, the C2M0080120D peak current reaches 48 A while the UJC1206K peak current reaches 98 A. In this case, Cascode peak current is higher than MOSFET one, this is due to the lower Si MOSFET Cascode threshold voltage ($V_{GS(TH)}$).

3.2. Waveforms analysis

From the oscilloscope waveforms acquired, it can be concluded that over all the short circuit performed, V_{DS} value remains constant because is fixed by the NDT setup and V_{GS} has no appreciable variation, showing no gate oxide relevant degradation. However, the *DUT* peak current (I_{Dmax}) presents a decreasing evolution over the tests.

In Fig. 4 it is shown the peak current value evolution over 200 short circuit tests. This decreasing trend is more remarkable in the C2M0080120D, showing a 2.5% peak current drop. The UJC1206K does not show a significant peak current decrease, this could be due to the short circuit energy dissipated in UJC1206K is 16% lower than C2M0080120D in the worst condition (V_{GS} = 12 V) and also because in its internal structure, the voltage blocking and consequently the power dissipation is handled by the JFET that shows a better behaviour in short circuit conditions since it is a simpler device.

Results at V_{GS} = 8.5 V do not show any apparent drop in the *DUT* peak current over the tests in any device.

3.3. B1505A devices characterization

All *DUTs* have been characterized before and after the repetitive short circuit campaign, the results are shown in Figs. 5 and 6. The characterization parameters used (V_{DS} *and* V_{GS}) are the established by manufacturers datasheets and are listed in Table 2.

- I_D vs V_{GS}

As illustrated in Fig. 5, high voltage repetitive short circuit tests have a significant effect on C2M0080120D threshold voltage ($V_{GS(TH)}$). This phenomenon has been already described in the literature [10] and could be due to the appearance of trapping effects at the Si/SiO2 interface. This drift increases in a linear way with the number of short circuits, reaching a maximum of 4.12% at 200 short circuits.

As expected, and described in other studies [11], *DUTs* devices tested with V_{GS} = 8.5 V do not present appreciable $V_{GS(TH)}$ drift.

As shown in Fig. 6, there is no $V_{GS(TH)}$ drift in UJC1206K, and it is worth noting that the threshold voltage in this case is considerably

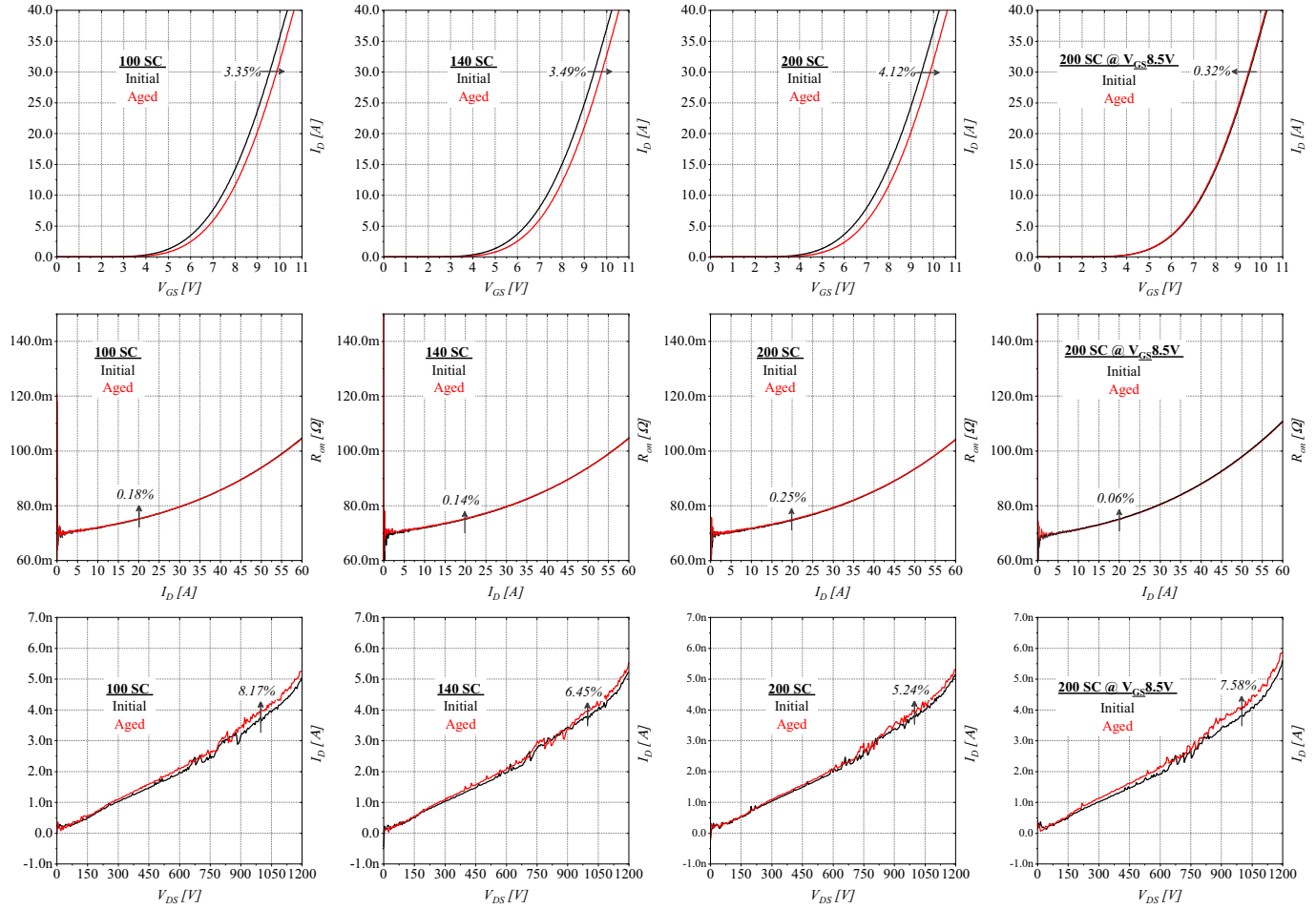

Fig. 5. C2M0080120D – B1505A characterization. Black: Fresh device trace. Red: Aged device trace.
First row: I_D vs V_{GS}. Second row: R_{on} vs I_D. Third row: I_D vs V_{DS} at V_{GS} = 0 V. First column: 100SC aging. Second column: 140SC aging. Third column: 200SC aging. Fourth column: 200SC aging at V_{GS} = 8.5 V. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

lower than in C2M0080120D. In this case, the UJC1206K Si MOSFET avoids the appearance of the trapping effect.

- R_{on} vs I_D

As shown in Fig. 5, the increase of the on resistance (R_{on}) in C2M0080120D is proportional to number of short circuits and it is between 0.18% and 0.25% at 20A I_D. For devices tested with V_{GS} = 8.5 V, R_{on} increase is 0.06% at same current value. These increases, in general, are due to two different issues, the increase of the bond wires resistance due to aging and microfracturing as described in [11] and the equivalent increase of R_{on} due to the $V_{GS(TH)}$ drift.

In the UJC1206K, a significant increase of the equivalent R_{on} between 1.41% and 1.84% is appreciated. The measured resistance is the addition of the equivalent resistance of SiC JFET Cascode and Si MOSFET, please refer to Fig. 1, and again, this phenomenon could be justified from two different perspectives: The first is the increase of the bond wire resistance between both devices as well as the increase of the bond wire resistance to pinout. The second is the JFET threshold voltage drift. This phenomenon has been described in the literature in [6]. A decrease of the JFET threshold (normally-on) would affect the current saturation levels, and therefore from the point of view of the device, in an equivalent increase of R_{on}. Equivalents results have been obtained for the devices tested at V_{GS} = 8.5 V.

- I_D vs V_{DS}

In Fig. 5 it can be seen a C2M0080120D drain-source leakage current (I_{DSS}) increase, especially for $V_{DS} \geq 700$ V, the increase is between 5.24% and 8.17%. According to [12], an increase in I_{DSS} after a short circuit test suggests lower robustness.

On the other hand, the UJC1206K drain-source leakage current presents an unexpected behaviour not previously described in the literature. Drain-source leakage currents are reduced by a percentage between 3% and 25%, being higher this reduction in devices with a higher number of short circuits. This phenomenon could be due to the JFET threshold voltage drift. In a fresh device, the low SiC JFET leakage current causes the Si MOSFET is not blocking voltage. After test, the increase of the negative biasing voltage would lead a higher leakage in JFET. This increase could lead a new equilibrium condition in which MOSFET blocks higher voltage resulting in a lower overall drain-source leakage current. When V_{GS} = 8.5 V is applied, the opposite behaviour is shown.

4. Conclusions

This work compares the degradation of SiC MOSFET and SiC/Si Cascode devices under high voltage stress short circuit repetitive conditions. The degradation has been characterized using a B1505A curve tracer before and after short circuit test.

Results reveal lower peak current degradation in the Cascode, influenced by a lower JFET saturation current. The on resistance increase is higher in the Cascode, however, even considering it, it has a lower

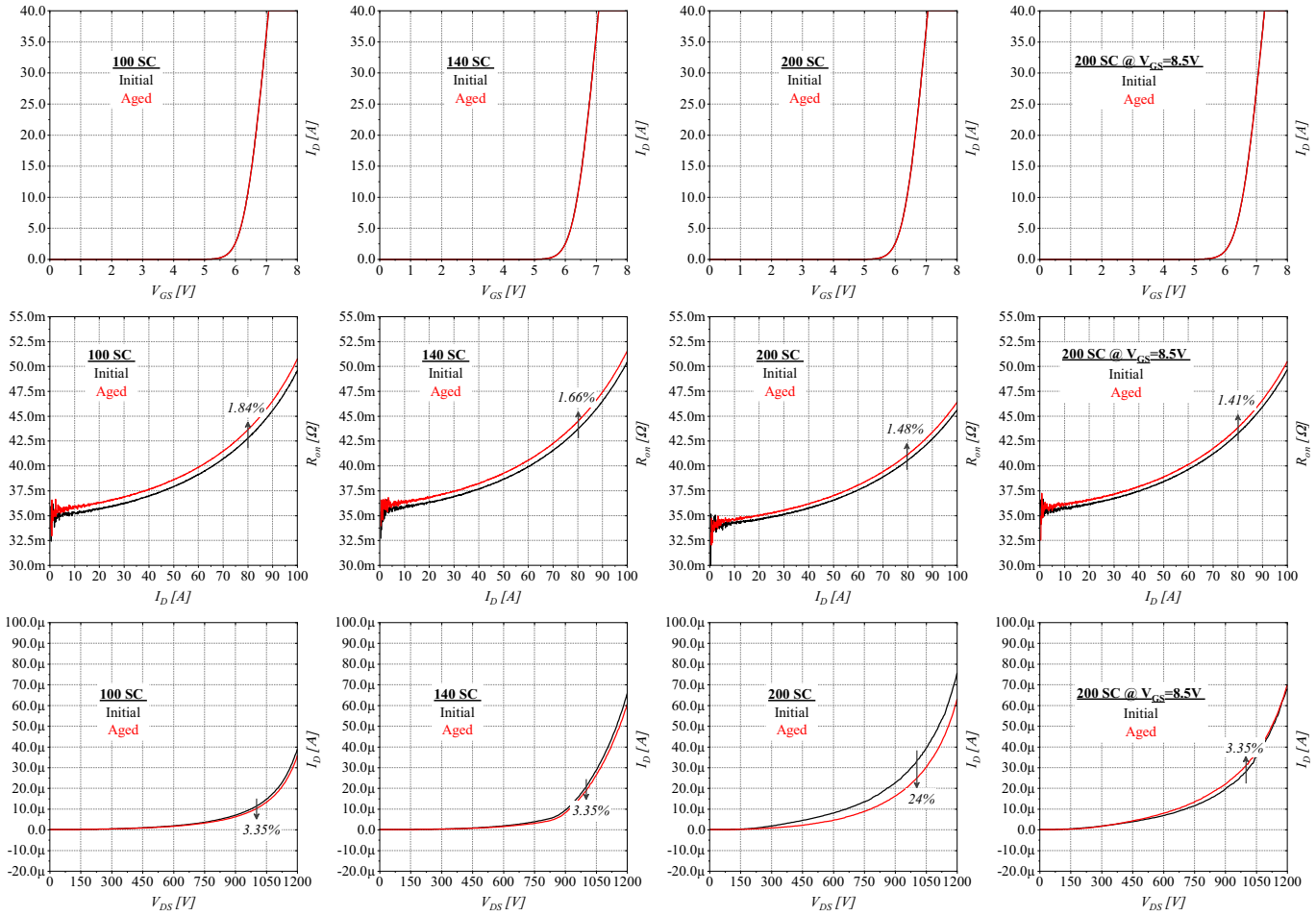

Fig. 6. UJC1206K – B1505A characterization. Black: Fresh device trace. Red: Aged device trace.
First row: I_D vs V_{GS}. Second row: R_{on} vs I_D. Third row: I_D vs V_{DS} at V_{GS} = 0 V. First column: 100SC aging. Second column: 140SC aging. Third column: 200SC aging. Fourth column: 200SC aging at V_{GS} = 8.5 V. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 2
C2M0080120D & UJC1206K B1505A test parameters.

Test	V_{DS} [V]	V_{GS} [V]
C2M0080120D		
I_D vs V_{GS}	20	–
R_{on} vs I_D	–	20
I_D vs V_{DS}	–	0
UJC1206K		
I_D vs V_{GS}	5	–
R_{on} vs I_D	–	12
I_D vs V_{DS}	–	0

resistance than the equivalent SiC MOSFET. In the case of the drain-source leakage current, the Cascode shows an improvement after the SC tests, however, the Cascode Si MOSFET could be internally blocking higher voltages, reducing its useful life time.

Based on the results, SiC/Si Cascode are very promising devices for solid state HVDC protection where small R_{on} is required.

In a foreseeable future, the Cascode leakage current reduction causes should be confirmed by a finite element simulation or by the implementation of a discrete Cascode, in this last option however, the effects of cross heating between JFET and MOSFET would be difficult to analyse.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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