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Endless and hitless phase shifter

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ABSTRACT

The present disclosure relates to a phase shifter (PS) designed to be endless and hitless, i.e., able to continuously phase shift without discontinuities over an infinite range. A fast PS unwraps the phase of a slower PS which has reached the limit of its range. After this unwrapping is done, the fast PS may quickly reset and return to its neutral state. With repeated resets, the slow PS effectively has endless and hitless operation over infinite range. This approach enable operation without temperature stabilization, e.g., use of a thermoelectric cooler (TEC).

DETAILED DESCRIPTION

A phase shifter is an optical device configured to manipulate the phase of light, such as for photonic components, including optical modulators. The present disclosure relates to a phase shifter designed to be endless and hitless, i.e., able to continuously phase shift without discontinuities over an infinite range.

An example of the need for such a PS is in the compensation of thermal drifts. Unbalanced interferometric structures such as resonant structures taken on their own, or Mach-Zehnder interferometers (MZI) with a delay path, are subject to temperature drifts of their optical transfer functions. In silicon platforms, this drift of the transfer function along a frequency axis is approximately 10 GHz/°C. This effect arises from the thermo-optic coefficient of the underlying waveguiding material. As a free spectral range (FSR) corresponds to 2π rads of phase shift, a corresponding rate in rads/°C for a specific structure.

This drift may be compensated by one or more PS within the structure. As the FSR becomes small, the required phase shift for hitless control over a significant temperature range (e.g., 100°C) may become excessively large. Another requirement of many applications is for hitless operation – i.e., the device may not reset to another multiple of 2π, as phase locking would be lost momentarily, especially if the PS is relatively slow.

Certain classes of PS may be operated fast, but offers several drawbacks: requirement of correspondingly fast electronics, poor efficiency, high optical losses, large footprint, etc.

This disclosure describes the combination of a slow but efficient PS, which is the main PS, which a faster but less efficient high-speed PS (HSPS) used intermittently for reset of the main PS. An example of a slow PS may be a thermal phase shifter (TPS). An example of a HSPS may be a current-injection (CI) Si PIN diode.

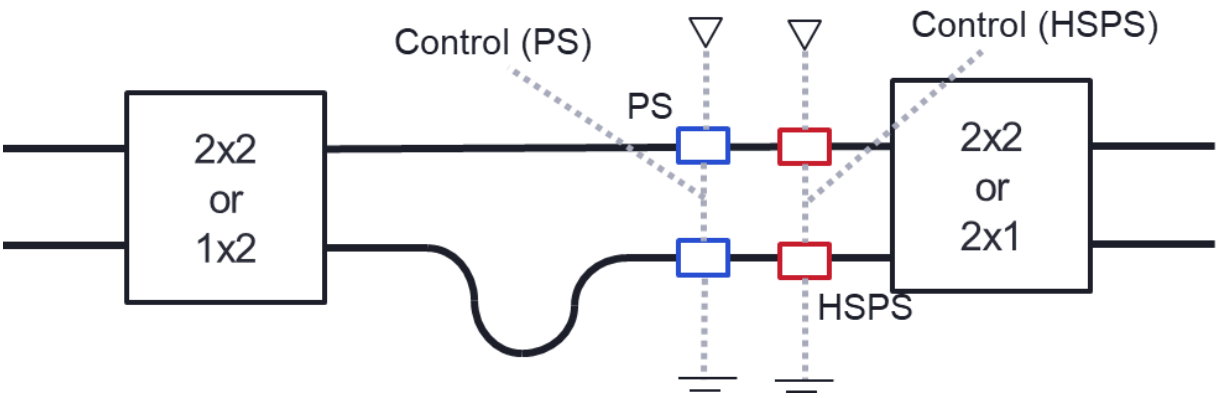

FIG. 1: Example with differential control of the PS and HSPS in an MZI.

For a MZI, the PS and HSPS may be controlled differentially, with a device in each arm, for better control of the optical losses and delay in each arm. The other ports are connected to ground and a constant voltage supply (e.g., VCC), respectively. The PS and HSPS have a finite range which is some multiple of 2π, i.e., k x 2π, where k > 1. Their range need not be equal but must be greater than 2π.

In operation, the PS may track a phase continuously until it approaches its phase limit. To unroll the PS, the HSPS may be controlled to apply a phase shift in the same direction as the approaching limit of the PS. Correspondingly, the PS may reduce the amount of phase shift in that direction, until it has unwrapped by a full multiple of 2π rads. When this is achieved, the HSPS may be turned off or reverted to its initial neutral value. A Si CI PS, for example, may have a transient in the range of nanoseconds or less, compared to milliseconds or microseconds for typical thermal phase shifters.

This is represented below visually and as a flow chart:

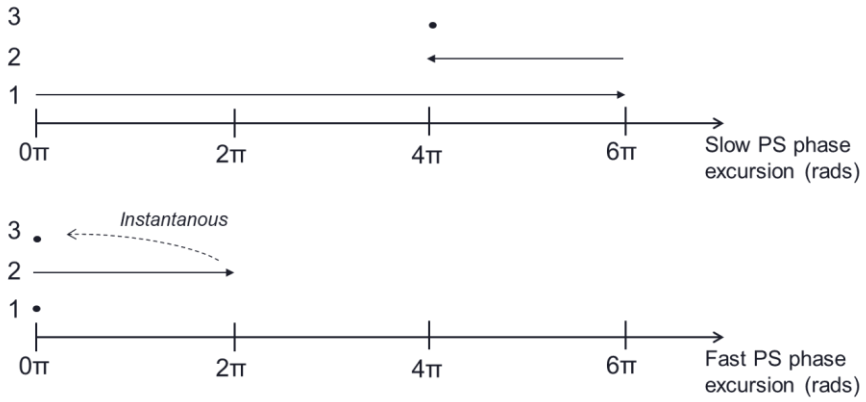

FIG. 2: Visual representation of the operation of both PS for a 2π phase unwrapping of the slow PS.

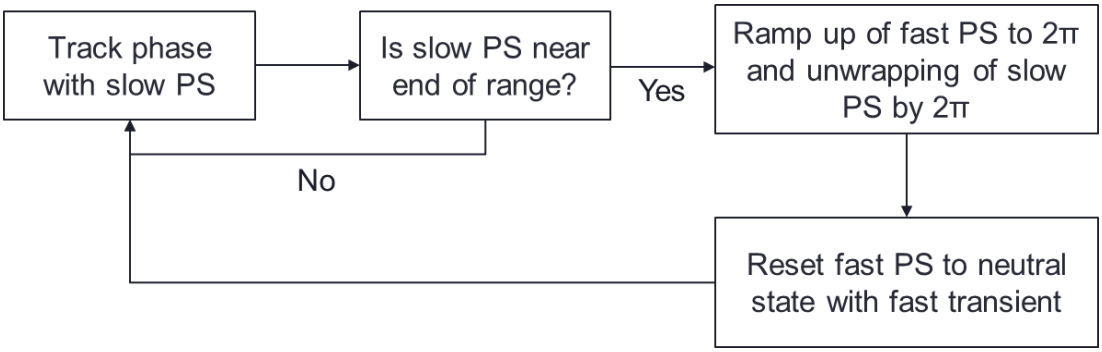

FIG. 3: Flowchart.

Benefits of a differential control for the HSPS is that at a middle point equal to VCC/2, the optical losses are balanced in each arm, leading to no impairment of the common-mode rejection ration (CMRR) or extinction ratio of the interferometer, and it is equally suitable for a reset in both positive and negative phase directions.

As the reset TPS is used intermittently, a single control may be used for several HSPS through a switch.

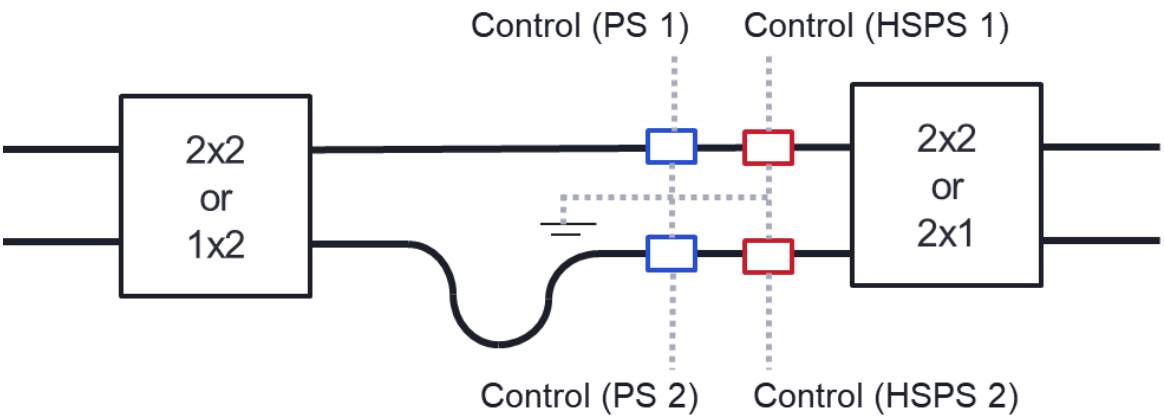

FIG. 4: Example with dual single-ended control of the PS and HSPS in an MZI.

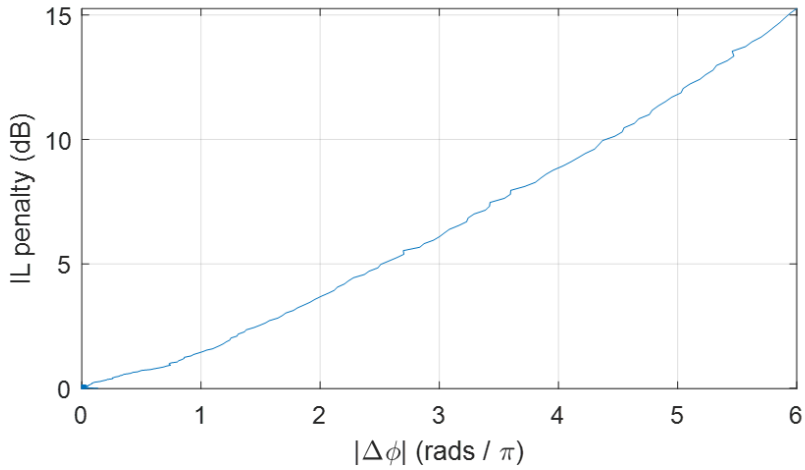

FIG. 5. Fast phase shifter – Silicon PIN with current injection, Raw attenuation–phase shift, typical length

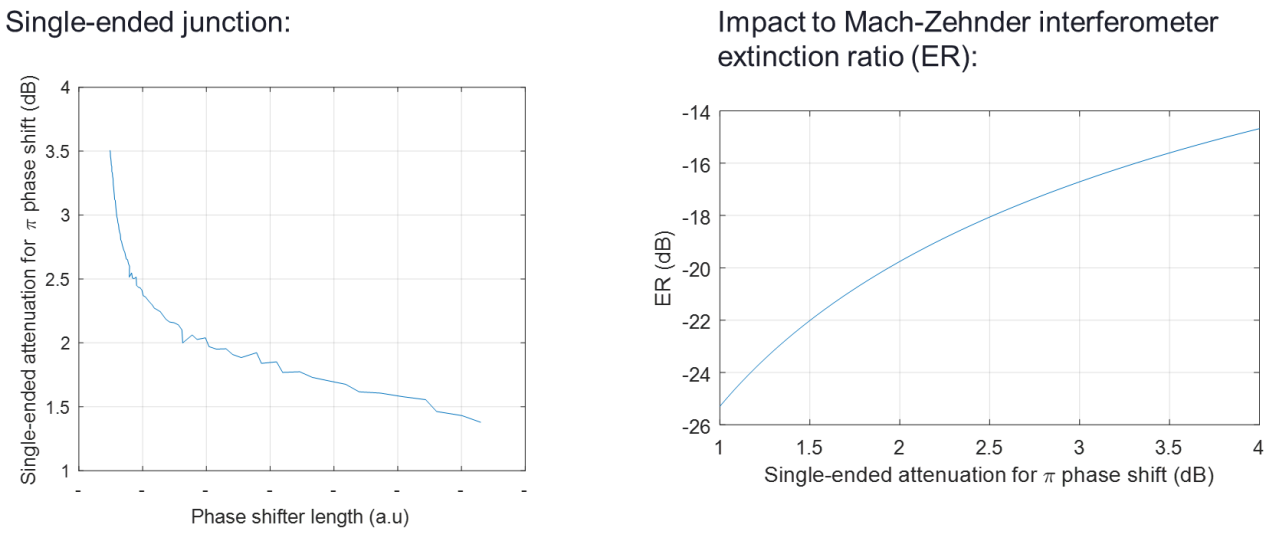

FIG. 6. Fast phase shifter – Silicon PIN with current injection, Normalized to π.

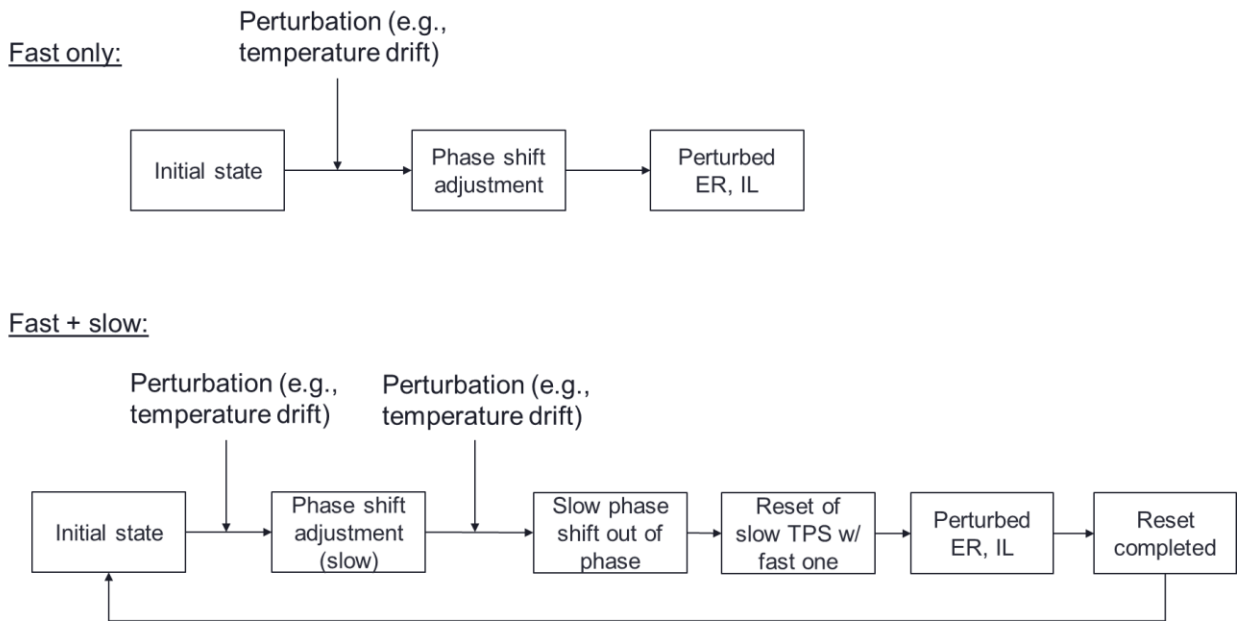

FIG. 7. Flowchart

It will be appreciated that some embodiments described herein may include one or more generic or specialized processors ("one or more processors") such as microprocessors, digital signal processors, customized processors, and Field-Programmable Gate Arrays (FPGAs) and unique stored program instructions (including both software and firmware) that control the one or more processors to implement, in conjunction with certain non-processor circuits, some, most, or all of the functions of the methods and/or systems described herein. Alternatively, some or all functions may be implemented by a state machine that has no stored program instructions, or in one or more Application-Specific Integrated Circuits (ASICs), in which each function or some combinations of certain of the functions are implemented as custom logic. Of course, a combination of the aforementioned approaches may be used. Moreover, some embodiments may be implemented as a non-transitory computer-readable storage medium having computer-readable code stored thereon for programming a computer, server, appliance, device, etc. each of which may include a processor to perform methods as described and claimed herein. Examples of such computer-readable storage mediums include, but are not limited to, a hard disk, an optical storage device, a magnetic storage device, a ROM (Read Only Memory), a PROM (Programmable Read-Only Memory), an EPROM (Erasable Programmable Read-Only Memory), an EEPROM (Electrically Erasable Programmable Read-Only Memory), Flash memory, and the like. When stored in the non-transitory computer-readable medium, the software can include instructions executable by a processor that, in response to such execution, cause a processor or any other circuitry to perform a set of operations, steps, methods, processes, algorithms, etc.

Although the present disclosure has been illustrated and described herein with reference to preferred embodiments and specific examples thereof, it will be readily apparent to those of ordinary skill in the art that other embodiments and examples may perform similar

functions and/or achieve like results. All such equivalent embodiments and examples are within the spirit and scope of the present disclosure.