Dynamic Modeling and Analysis of the Bidirectional DC-DC Boost-Buck Converter for Renewable Energy Applications

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Abstract

This paper focuses on the modeling, dynamic analysis, and simulation of the bidirectional DC-DC boost-buck power converter. The switching sequence applies different duty cycles in the input and output stages, resulting in full regulation of the system variables. By using this strategy, the input stage can be regulated disregarding perturbations in the output leg, as well as the output stage can be controlled independently of the effects of disturbances in the input part; which gives significant robustness to the converter. Based on the switching actions, the state-space average equations are derived, accomplishing the base to obtain the small-signal equations and equivalent small-signal circuits. The open-loop transfer functions are developed, besides the input and output impedance, and the audio susceptibility. Simulation results indicate that the proposed model can predict the dynamic behavior of the system in a wide range of the frequency spectrum, and the results in the time domain are in perfect agreement with the model predictions under disturbances of the control variables, variations of the value of the supply voltage and load changes.

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1. Introduction

In recent years, renewable energy sources are becoming more attractive and a sustainable solution for the growing electrical demand, in which photovoltaic (PV) energy receives more attention due to its reliability, pollution-free characteristics, and capability to be used in stand-alone or large-scale grid applications [1]-[4]. In order to reduce the amount of PV panels in the array, to decrease the installation costs, and to improve the interface between the solar panels and the grid, DC-DC converters can be employed to ensure adequate voltage and current regulation between the input and output stages [5].

In most PV applications, a maximum power point tracking (MPPT) algorithm should be included for full extraction of the power provided by the PV panels, regardless the solar irradiation condition. It can be implemented using a DC-DC converter as the interface between the photovoltaic modules and the load. Basic Buck or Boost converters are not proper for this purpose since they cannot ensure that the operating point will match the maximum power point for every irradiation and temperature conditions. The following conclusion can be obtained from the literature review. The Buck converter may not track the MPP under high temperature (low voltage) and high irradiation (high current) since these environmental conditions establishes the MPP on the non-operational region. The Boost Converter cannot track the MPP under low temperature (high voltage) and low irradiation (low current). The Buck-Boost, or any converter with similar static characteristic, is able to find the MPP independently on the environmental conditions. The aforementioned converters are more appropriate to be employed in PV applications, mainly in situations in which the environmental conditions vary widely.

In this context, several articles analyze different DC-DC converters that can be utilized for renewable energy applications, in which the majority of the topologies presents voltage source characteristics in their outputs [6]-[8]. Al-

though this feature can reduce the output voltage ripple in operations whereby the converter feeds linear loads, it requires the addition of an extra inductor in applications where the converter injects current into the utility grid. Besides, the injected current cannot be pre-regulated by the DC-DC converter, leading the DC-AC stage, which connects the converter to the grid, to be switched with high frequencies and, consequently, increasing the overall losses of the system.

Therefore, a robust power converter that can be employed in those applications is the DC-DC boost-buck converter. This topology is the combination of the boost and buck structures, as shown in Fig. 1. It is a non-isolated, bidirectional, step-up/step-down DC-DC converter that presents high power density and, at the same time, the feature that the input and output currents are continuous. Furthermore, it is a versatile converter that can be used in several applications such as PV systems [9]-[13], AC power generation [14], high-efficiency wirelesses power transfer [15], power factor correction [16] and, thermoelectric generators [17]-[19]. Moreover, it can also be adapted for multilevel and three-phase applications [20], [21].

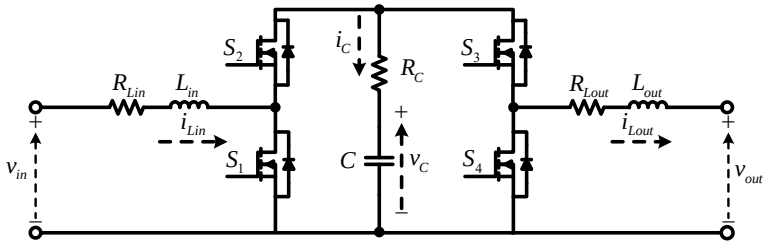


Figure 1: Bidirectional DC-DC boost-buck converter including the parasitic elements in the passive components.

To properly design the controllers for any power converter, a comprehensive dynamic analysis must be carried out first. Therefore, it is important to select the switching actions carefully and examine the behavior of the system variables during the different switching states. In cascaded converters, such as the boost-buck, a modulation strategy which enables the input and output stages to be decoupled is desired, because it permits the input variables to neglect the effects

of perturbations in the output variants and vice-versa.

The first modulation strategy for the boost-buck converter was proposed in [22], which uses the same duty cycle for both legs of the converter. Although this strategy is the most straightforward one to be implemented, the use of same duty cycles cannot provide enough degrees of freedom to the converter, leading the capacitor voltage amplitude to be higher than the actual value required for the proper operation of the topology. In the works presented in [9] and [10], a strategy that allows the converter to be operated either in buck or boost mode was given. It results in a two states model that is used to derive the dynamics of the input and output currents, but it disregards the effect of the DC-link capacitor voltage; hence, it can present unpredictable behavior under transients, decreasing the stability of the system. Another approach was proposed by [18], whereby different phase shifted duty cycles were used. However, the number of control variables increases and leads to a complex model which cannot decouple the input from the output stages.

Therefore, a modulation strategy that enables controlling all system variables and, simultaneously, avoiding the input and output dependency is preferable. The modulation strategy proposed in this paper consists of applying different duty cycles for each leg of the converter showed in Fig. 1, in which the input ratio is higher than the output. So, the state whereby the input and output are connected can be eliminated and, consequently, the variables can be unrelated to each other. Moreover, a step-by-step study of the boost-buck converter is presented, which allows the complete dynamic behavior of the topology to be understood.

Firstly, an in-depth steady-state analysis of the converter is conducted, which enables understanding the role of each variable of the structure. Based on this analysis, the state-space average technique is employed considering parasitic elements to obtain a more accurate dynamic model. However, the mathematical model presents non-linear characteristics making the dynamic analysis of the topology highly complex. The model of the converter can be linearized by applying the well-known small-signal technique [23], [24]. This technique linearizes

the model of the topology for a specific operating point by adding small perturbations in their average equations. By manipulating the perturbed equations, an equivalent linear circuit model can be synthesized and solved using simple circuit analysis to find the TFs for the input and output currents as well for the capacitor voltage. Moreover, it also enables the output and input impedance and the TF relating the input voltage to the output voltage to be derived, also known as audio susceptibility [25].

Another contribution of this paper relies on an extensive study through simulations to analyze the different behaviors of the converter for distinct working conditions. Therefore, to validate the small-signal model for the proposed modulation strategy, simulation results comparing the time domain response of the small-signal equations with the boost-buck converter show that both responses have similar behavior for different input voltage, duty ratio and load conditions. Furthermore, simulation results in the frequency domain confirm that the dynamic response obtained using the TFs is in close agreement with the simulated converter.

This paper is organized as follows: In section 1, the introduction is given. Section 2 the boost-buck converter is described when it is regulated using the proposed modulation strategy. In Section 3, the mathematical model for the boost-buck is derived. Section 4 presents simulation results in order to validate the theoretical analyzes through time and frequency domains. Finally, the conclusions are presented in Section 5.

2. System Description

By cascading the boost power converter with a buck power stage, it is possible to obtain the two-stage boost-buck converter. It consists of a four active switches topology, S_1, S_2 for the input leg, and S_3, S_4 for the output one, that presents three energy storage elements: the inductors L_{in} and L_{out}, and a DC-link capacitor C. In this section, the operating principle of the converter using the proposed modulation strategy is detailed, and the general expressions

of the topology are derived considering the power transfer from the input to the output, in which an ideal voltage source feeds the converter and the load is modeled as a resistance. Finally, guidelines to size all the passive elements of the structure are presented.

2.1. Modulation Strategies and Working Principle

Let us consider that the capacitor voltage is constant and the conduction intervals are established as functions of the duty cycles $t_1 = d_1 T_s$, for $\left\{S_1, \overline{S_2}\right\}$, and $t_2 = d_2 T_s$, for $\left\{S_3, \overline{S_4}\right\}$, whereby d_1 is the pulse width generated by the input leg, d_2 is the pulse width generated by the output leg, and T_s is the switching period. For the modulation strategies considered in previous works, the input and output currents are the variables of interest [9],[10], [16] and [22]. However, some applications might require capacitor voltage regulation, making the topology robust against sudden variations in the load or input voltage.

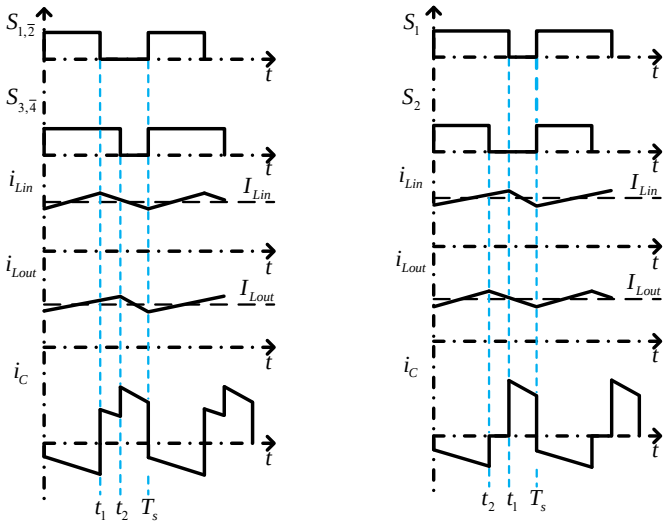
Therefore, two modulation strategies are proposed to add the capacitor voltage as an extra system variable, whose main waveforms are shown in Fig. 2(a) and (b). These strategies consist of driving the topology with the conditions $d_1 < d_2$ or $d_1 > d_2$, depending on the voltage conversion ratio. The modulation strategy shown Fig. 2(a) (Case I) can be employed when the output voltage is lower than the input one. On the other hand, when the output voltage is higher than the input source, Case II is adopted. Although the proposed modulation strategies add one more switching state, they allow all state variables to be manipulated, as it will be shown later.

Based on the in-built converter characteristics and the modulation strategy used, the capacitor voltage determines the duty cycles of both legs and they can be calculated similarly to the boost and buck converters.

$$d_1 = 1 - \frac{v_{in}}{v_C}; \tag{1}$$

and

$$d_2 = \frac{v_{out}}{v_C}. \tag{2}$$



(a) (b)

Figure 2: Proposed switching strategies for the boost-buck converter: a) Case I: $d_1 < d_2$, b) Case II: $d_1 > d_2$.

Through the proposed modulation strategies, it is possible to describe the topology working principle, design the passive elements and to derive the equation for the voltage gain. Therefore, when the boost-buck converter is modulated with the strategy in Case II, it presents the following behavior in steady-state:

Interval I - $(0 \leq t < d_2 T_s)$: S_1 and S_3 are in on-state and the input inductor L_{in} is connected to the input voltage source v_{in}; consequently, its current i_{Lin} increases linearly in time. Meanwhile, the stored energy in capacitor C is discharged to the load through switch S_3, charging the output inductor L_{out}.

Interval II - $(d_2 T_s \leq t < d_1 T_s)$: S_1 is in on-state and S_3 is in off-state, thus the input inductor L_{in} keeps connected to v_{in}. Since S_2 and S_3 are in off-state, there is no current flowing through C. Thus, the magnetic energy stored in L_{out} circulates through the switch S_4 feeding the load.

Interval III - $(d_1 T_s \leq t < T_s)$: S_1 and S_3 are in off-state and the capacitor C

is charged through the energy stored in L_{in} and from the input voltage source. The energy from L_{out} keeps circulating through S_4 supplying the load.

2.2. Converter Design

The working principle acknowledges the behavior of the variables for each state and to establish the time intervals that are necessary to design the passive elements. During interval I, the voltage across the input inductor L_{in} is equal to the input voltage v_{in}; thus, the input inductance can be calculated as follows:

$$L_{in} = \frac{v_{in} d_1}{F_s \Delta i_{Lin}} \tag{3}$$

where, $\Delta_{i_{Lin}}$ is the specified input inductor current ripple.

Similarly, the output inductor is designed following the same procedures. During interval I, the voltage across L_{out} is the difference between the capacitor and the output voltages. Therefore, by considering the capacitor as a constant voltage source, the output inductance can be calculated as:

$$L_{out} = \frac{(V_C - V_{out}) d_2}{F_s \Delta i_{Lout}} \tag{4}$$

where $\Delta_{i_{Lout}}$ is the desired current ripple for the output inductor, while V_C and V_{out} are the average values for the capacitor and output voltages, respectively.

The last passive element to be sized is the DC-link capacitor. Knowing that during the time interval I its current is equal to the output inductors current $i_C = i_{Lout}$, the capacitance can be calculated as follows:

$$C = \frac{I_{Lout} d_2}{\Delta v_C F_s} \tag{5}$$

where, I_{Lout} is the average value for the output current and Δ_{v_C} is the stated capacitor voltage ripple.

Another important information that is required when power converters are used is the voltage gain of the structure (M). It can be calculated as the ratio between the output and input voltages in function of the duty cycles values. By manipulating (1) and (2), the expression can be found as yields:

$$M = \frac{v_{out}}{v_{in}} = \frac{d_2}{1 - d_1} \tag{6}$$

3. Derivation of the Small-Signal Linear Model and Frequency Response

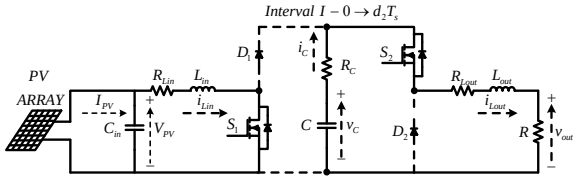
In this section, the small-signal model for the DC-DC boost-buck converter is derived when the proposed modulation strategy is applied. Moreover, the small-signal terms can be used to obtain the equivalent circuits, giving the bases to achieve the frequency response of the topology. Finally, the open-loop TFs, the input and output impedance and the audio susceptibility TFs can be derived, providing the complete understanding of the dynamic behavior of the converter.

3.1. Deduction of the Equivalent Small-Signal Circuit

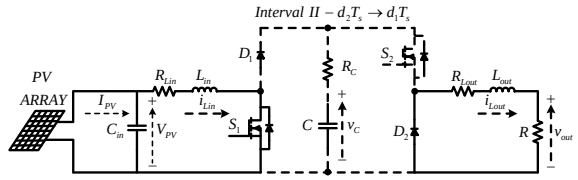
According to [26], to obtain the linear small-signal model of a converter, it is necessary to choose a specific operating point. As mentioned in Section II, this paper considers a modulation strategy in which $d_1 > d_2$, whose main waveforms are shown in Fig. 2(b).

To better perform the analysis of the dynamic behavior of the power converter the parasitic resistances, (R_{Lin}), (R_{Lout}) and (R_C), which represent the series resistances of the input and output inductors and the capacitor resistance, respectively, have been added. Moreover, the converter is fed by a PV array, considered in this paper as a constant DC voltage source for the mathematical analysis. By applying the proposed switching strategy, three different circuits can be obtained to aid the average model derivation process, as it is shown in Fig. 3. In Fig. 3(a), the circuit representing the interval I is drawn. At the interval II, the corresponding circuit is displayed in Fig. 3(b). The circuit presented in Fig. 3(c) represents the last switching action.

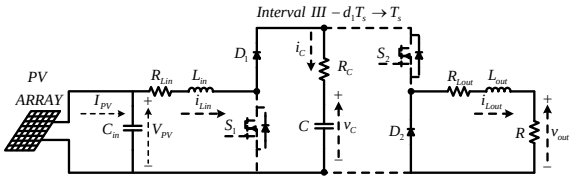
The average model can be obtained by analyzing the circuits for each time interval and adding the duty cycles as a weighting factor for each set of equations. By including them, the average dynamic model of the converter can be derived and it is expressed as follows:



(a) Interval I: $d_2T_s - 0$.



(b) Interval II: $d_1T_s - d_2T_s$.



(c) Interval III: $T_s - d_1T_s$.

Figure 3: Active circuits for the boost-buck converter during each interval: a) Interval I, b) Interval II, and c) Interval III.

$$L_{in}\frac{d\langle i_{Lin}\rangle}{dt} = \langle v_{in}\rangle - R_{Lin}\langle i_{Lin}\rangle - \left[\left(\langle v_C\rangle + R_C\langle i_{Lin}\rangle\right)(1-d_1)\right]; \tag{7}$$

$$L_{out}\frac{d\langle i_{Lout}\rangle}{dt} = \left[\left(\langle v_C\rangle - R_C\langle i_{Lout}\rangle\right)d_2\right] - \langle v_{out}\rangle - R_{Lout}\langle i_{Lout}\rangle; \tag{8}$$

$$C\frac{d\langle v_c\rangle}{dt} = \langle i_{Lin}\rangle(1-d_1) - \langle i_{Lout}\rangle d_2; \tag{9}$$

$$\langle v_{out}\rangle = \langle i_{Lout}\rangle R; \tag{10}$$

$$\langle i_{in}\rangle = \langle i_{Lin}\rangle. \tag{11}$$

where, the terms $\langle i_{Lin} \rangle$, $\langle i_{Lout} \rangle$, $\langle v_C \rangle$ and $\langle v_{out} \rangle$ are the low-frequency averaged input current, output current, capacitor voltage, and output voltage, respectively.

By observing the average equations using the new modulation strategy, it can be noted that the input and output stages are decoupled. This fact can be explained because (7) does not present any terms related to the output current and (8) is not affected by variations in the input current.

Owing to the difficulty of manipulating non-linear variables such as the ones in the average model, is desired to linearize the system through the small-signal technique. So, each low-frequency averaged variant is replaced by a DC term plus an AC one. These AC terms are superimposed and much smaller than the DC values at the operating point. They can be described as the following general expression:

$$\langle x \rangle = X + \widehat{x} \tag{12}$$

where X represents the DC values for the circuit while $\widehat{x}$ is the perturbed AC value.

After replacing the obtained terms from (12) in the average model and ignoring the non-linear terms, two set of equations can be obtained: the DC terms representing the circuit in steady-state condition and the AC terms corresponding to the linearized dynamic behavior:

DC terms:

$$0 = V_{in} - R_{Lin} I_{Lin} - V_C(1 - D_1) - R_C I_{Lin}(1 - D_1); \tag{13}$$

$$0 = (V_C - R_C I_{Lout})\, D_2 - V_{out} - R_{Lout} I_{Lout}; \tag{14}$$

$$0 = I_{Lin}(1 - D_1) - I_{Lout} D_2; \tag{15}$$

$$V_{out} = I_{Lout} R; \tag{16}$$

$$I_{in} = I_{Lin}. \tag{17}$$

AC small-signal terms:

$$L_{in}\frac{d\widehat{i}_{Lin}}{dt} = \widehat{v}_{in} - (R_{Lin} + R_C(1-D_1))\widehat{i}_{Lin} - (1-D_1)\widehat{v}_C + (V_C + R_C I_{Lin})\widehat{d}_1; \tag{18}$$

$$L_{out}\frac{d\widehat{i}_{Lout}}{dt} = D_2\widehat{v}_C + (V_C - R_C I_{Lout})\widehat{d}_2 - \widehat{v}_{out} - (R_{Lout} + R_C D_2)\widehat{i}_{Lout}; \tag{19}$$

$$C\frac{d\widehat{v}_C}{dt} = (1-D_1)\widehat{i}_{Lin} - I_{Lin}\widehat{d}_1 - D_2\widehat{i}_{Lout} - I_{Lout}\widehat{d}_2; \tag{20}$$

$$\widehat{v}_{out} = R\widehat{i}_{Lout}; \tag{21}$$

$$\widehat{i}_{in} = \widehat{i}_{Lin}. \tag{22}$$

By manipulating equations (13)-(17), it is possible to obtain the voltage gain of the boost-buck converter in steady-state when the effects of the parasitic resistances are considered, yielding:

$$M = \frac{D_2}{(1-D_1)}.\left(\frac{R}{R_{Lin}\left(\frac{D_2}{1-D_1}\right)^2 + \frac{R_C {D_2}^2}{1-D_1} + R_C D_2 + R_{Lout} + R}\right) \tag{23}$$

Once the AC terms were obtained, a linear time-invariant (LTI) equivalent small-signal circuit can be drawn. Fig. 4(a) shows the small-signal circuit related to the voltage across the input inductor expressed by (18). The small-signal model is characterized by two independent voltage sources $\widehat{v}_{in}$ and $V_C\widehat{d}_1$, one dependent voltage source $(1-D_1)\widehat{v}_C$, the energy storage element itself L_{in} and two parasitic resistances, the input inductor series resistance R_{Lin} and the capacitor series resistance. Furthermore, it can be observed that the capacitor

resistance presents a term that is reflected to the input side, in which it can be expressed as:

$$R_{Cin} = R_C(1 - D_1) \tag{24}$$

Following the same principle, (19) can also be represented as a small-signal circuit. The expression $D_2\widehat{v}_C$ is drawn as a dependent voltage source while $V_C\widehat{d}_2$ is described as an independent voltage source. The term $\widehat{v}_o$ is the output voltage across the load. The output inductor keeps defined as L_{out} and the circuit also has two parasitic elements, R_{Lout} and the capacitor series resistance. Similarly as the input current small-signal equation, the capacitor resistor presents another term that is reflected to the output stage, and it can be defined as:

$$R_{Cout} = R_C D_2 \tag{25}$$

The current flowing through the capacitor C is described by (20). The expression has two dependent current sources, represented by $(1 - D_1)\widehat{i}_{Lin}$ and $D_2\widehat{i}_{Lout}$, and two independent current sources, defined by the terms $I_{Lin}\widehat{d}_1$ and $I_{Lout}\widehat{d}_2$. The small-signal circuit for the capacitor current is presented in Fig. 4(c).

By combining the small-signal circuits for the input inductor voltage, DC-link capacitor current and output inductor voltage, the complete equivalent small-signal circuit for the boost-buck converter can be obtained as it is presented in Fig. 4(d). It is noticed that the dependent sources can be combined as ideal transformers, T_{in} and T_{out}, which are part of the averaged small-signal model and the transformers ratio is related to the duty cycles.

Finally, an interesting insight can be drawn by observing the small-signal circuits, which is the effect of the capacitor parasitic resistance R_C in the circuit. As it is possible to see in the equivalent small-signal circuit, the capacitor resistance is reflected to both input and output stages and does not affect the capacitor small-signal voltage directly. If this effect is not observed and the

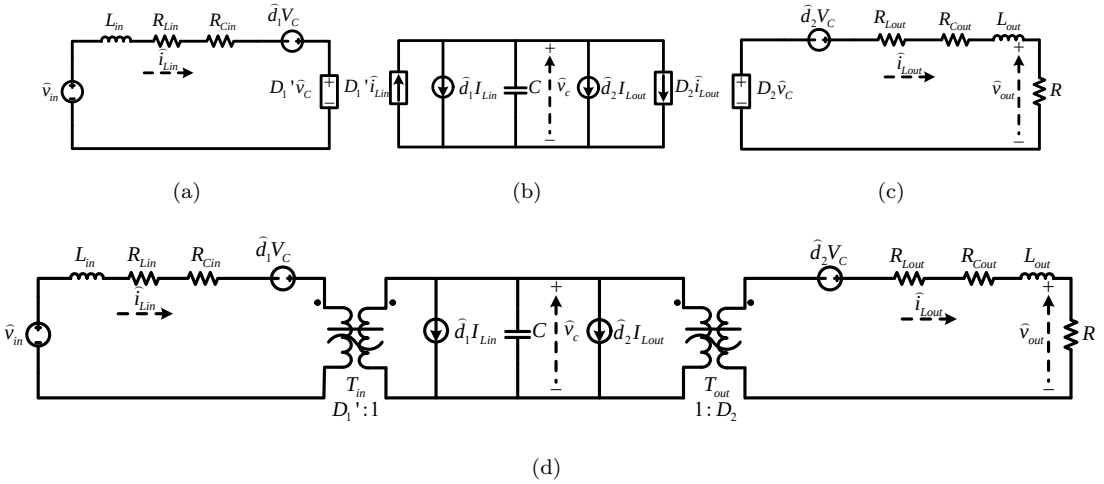


Figure 4: Equivalent small-signal circuit for the boost-buck converter. a) Input inductor voltage, b) Capacitor current, c) Output inductor voltage, and d) Full model.

capacitor parasitic resistance is added after the equivalent small-signal circuit is derived, as it can be done for other converters, such as the boost and buck, the dynamic response of the circuit will present a different behavior than the actual topology. Therefore, it is most important to understand that the capacitor parasitic reflection is a natural dynamic behavior of the converter when it is operated using the new modulation strategy.

3.2. Control Transfer Functions

As mentioned, the boost-buck converter presents three variables to be controlled, the input current i_{Lin}, the DC-link capacitor voltage v_C and the output current i_{Lout}, in which can be manipulated by two variables d_1 and d_2. So, it is necessary to derive the open-loop TFs for understanding the dynamic behavior of the system.

Through the equivalent small-signal circuit, it is possible to derive all TFs. Firstly, the ones regarding the impact of the input duty cycle $\widehat{d}_1$ over the input current $\widehat{i}_{Lin}$ and the capacitor voltage $\widehat{v}_C$ are obtained. In order to do so, the input voltage $\widehat{v}_{in}$ and the output duty cycle $\widehat{d}_2$ are set to zero. Thus, by

applying the mentioned conditions and reflecting all the terms to the secondary of T_{out}, the equivalent small-signal circuit can be redrawn as shown in Fig. 5. The reflected parameters are given in the Appendix A.

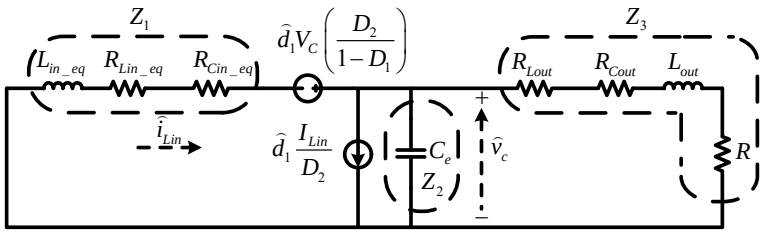


Figure 5: Manipulated circuit to find the input control transfer functions.

In order to derive the input control-to-input current TF, the superposition principle can be used to express the effect of each source in Fig. 5. Therefore, the independent current source is opened and the input current is calculated according to the impact of the voltage source. Then, the input current is derived when the voltage supply is short-circuited and only the current source is considered. By summing the results of the two analysis, it is possible to obtain the input control-to-input current TF given by (26).

$$\left.\frac{\widehat{i}_{Lin}}{\widehat{d}_1}\right|_{\widehat{v}_{in},\widehat{d}_2=0} = \frac{(1-D_1)}{D_2}\cdot\frac{1}{Z_4}\cdot\left\{V_{C\_eq}\left[\frac{Z_1}{Z_1+(Z_2||Z_3)}\right] + I_{Lin\_eq}\left[Z_1||\left(Z_2||Z_3\right)\right]\right\} \tag{26}$$

By observing (26), it can be noticed the presence of two terms, a DC gain ($(1-D_1)/D2$) and an impedance part ($1/Z_4$). These terms are necessary because the sources and equivalent impedance presented in Fig. 5 are placed in the secondary of the output transformer, while the input control-to-input current transfer function consists of variables that are located in the primary of the input transformer. Therefore, by multiplying the DC gain and the impedance ($1/Z_4$) with the superposition terms, it is possible to reflect the transfer function to the primary of T_{in}. Finally, manipulating the terms in (26), the open loop input

control-to-input current can be obtained and it can be expressed as follows:

$$G_{iLin} = \left.\frac{\widehat{i}_{Lin}}{\widehat{d}_1}\right|_{\widehat{v}_{in},\widehat{d}_2=0} = \frac{a_1 s^2 + a_2 s + a_3}{b_1 s^3 + b_2 s^2 + b_3 s + b_4} \tag{27}$$

where the terms of all transfer functions derived in this paper are expressed in Appendix B.

As expected, (27) is a third order system due to the presence of the three energy storage components and it can be observed that the transfer function has no terms regarding the output current. As a result, the input stage is not affected by variations in the output control variable, allowing to conclude that the input and output stages are decoupled when the new modulation strategy is applied.

Through the same process, the input control-to-capacitor voltage TF can be derived. Moreover, the capacitor is also reflected to the secondary of T_{out}; thus, it is necessary to readjust the DC gain, represented by the term $1/D_2$.

$$\left.\frac{\widehat{v}_C}{\widehat{d}_1}\right|_{\widehat{v}_{in},\widehat{d}_2=0} = \frac{1}{D_2}\cdot\left\{V_{C\_eq}\left[\frac{Z_2||Z_3}{Z_1+(Z_2||Z_3)}\right] - I_{Lin\_eq}\left[Z_1||\left(Z_2||Z_3\right)\right]\right\} \tag{28}$$

$$G_{vC_{d_1}} = \left.\frac{\widehat{v}_C}{\widehat{d}_1}\right|_{\widehat{v}_{in},\widehat{d}_2=0} = -\frac{a_4 s^2 + a_5 s + a_6}{b_1 s^3 + b_2 s^2 + b_3 s + b_4} \tag{29}$$

When $\widehat{d}_1$ is set to zero, the equivalent small-signal circuit can be rearranged, as it is displayed in Fig. 6. So, the TFs for the output current and capacitor voltage regarding the effects of the output duty cycle can be derived.

By solving the reflected circuit shown in Fig. 6, it is possible to obtain the terms which arise from the two independent sources, expressed as follows:

$$\left.\frac{\widehat{i}_{Lout}}{\widehat{d}_2}\right|_{\widehat{v}_{in},\widehat{d}_1=0} = \frac{1}{R}\cdot\left\{V_C\left[\frac{R}{Z_3+(Z_1||Z_2)}\right] - I_{Lout\_eq}\left[\frac{R\left(Z_1||Z_2\right)}{Z_3+(Z_1||Z_2)}\right]\right\} \tag{30}$$

Solving (30), the output control-to-output current can be defined as follows:

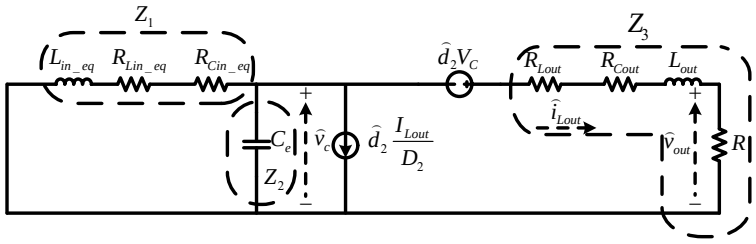


Figure 6: Manipulated circuit to find the output control transfer functions.

$$G_{iLout} = \left.\frac{\widehat{i}_{Lout}}{\widehat{d}_2}\right|_{\widehat{v}_{in},\widehat{d}_1=0} = \frac{a_7 s^2 + a_8 s + a_9}{b_1 s^3 + b_2 s^2 + b_3 s + b_4} \tag{31}$$

The same process can be used for the output control-to-capacitor voltage TF. Furthermore, the same DC gain as the input control-to-capacitor voltage is added because of the reflection to the secondary of T_{out}:

$$\left.\frac{\widehat{v}_C}{\widehat{d}_2}\right|_{\widehat{v}_{in},\widehat{d}_1=0} = -\frac{1}{D_2}\cdot\left\{V_C\left[\frac{Z_1||Z_2}{Z_3+(Z_1||Z_2)}\right] + I_{Lout\_eq}\left[Z_1||\left(Z_2||Z_3\right)\right]\right\} \tag{32}$$

By manipulating these terms, the output control-to-capacitor voltage can be derived as:

$$G_{vC_{d_2}} = \left.\frac{\widehat{v}_C}{\widehat{d}_2}\right|_{\widehat{v}_{in},\widehat{d}_1=0} = -\frac{a_{10} s^2 + a_{11} s + a_{12}}{b_1 s^3 + b_2 s^2 + b_3 s + b_4} \tag{33}$$

Finally, it can be observed that the numerator of the input control-to-input current (27) presents no terms regarding the output duty cycle. The same can be noted from the numerator of the output control-to-output current (31) which disregards the effects of the input duty ratio, being a consequence of the averaged model previously expressed.

3.3. Derivation of the Input and Output Impedance

In addition to the previously derived control TFs, the dynamic analysis of the impedance in a DC-DC converter gives relevant information related to the stability of the system [27]. Once again, the small-signal circuit of Fig. 4(d) is

used to derive the input impedance and output impedance TFs. By setting to zero the input variables $\widehat{d}_1$ and $\widehat{d}_2$, the equivalent small-signal circuit can be rearranged as shown in Fig. 7. Furthermore, all the output passive elements and the capacitor have to be reflected to the primary side of T_{in} given in the Appendix A.

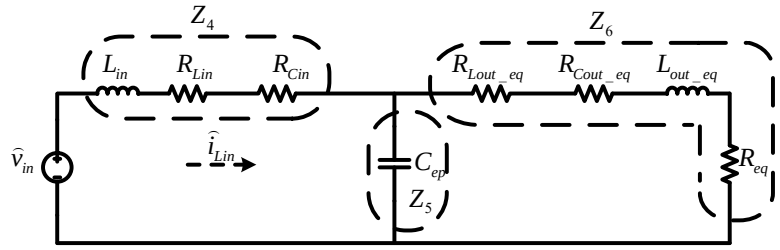


Figure 7: Manipulated circuit to derive $Z_{in}(s)$.

Therefore, through circuit analyzes of Fig. 7, it is possible to obtain the input impedance TF given as:

$$\left.\frac{\widehat{v}_{in}}{\widehat{i}_{Lin}}\right|_{\widehat{d}_1,\widehat{d}_2=0} = Z_{in}(s) = (Z_5||Z_6) + Z_4 \tag{34}$$

$$\left.\frac{\widehat{v}_{in}}{\widehat{i}_{Lin}}\right|_{\widehat{d}_1,\widehat{d}_2=0} = Z_{in}(s) = \frac{a_{13}s^3 + a_{14}s^2 + a_{15}s + a_{16}}{b_5 s^2 + b_6 s + b_7} \tag{35}$$

To obtain the output impedance TF ($Z_o(s)$) the passive elements are reflected to the secondary of T_{out}, following the same procedure for the open-loop control TFs along with $\widehat{d}_1$ and $\widehat{d}_2$ being set to zero; consequently, there is no current circulation in the circuit, as it is observed in Fig. 8. Therefore, an external current source ($\widehat{i}_g$) is connected in parallel with the load creating a small-signal voltage drop across the resistance R, which is equal to the small-signal output voltage in the equivalent small-signal circuit [26].

Therefore, similarly to the input impedance, $Z_o(s)$ is obtained by solving the circuit of Fig. 8 as follows:

$$\left.\frac{\widehat{v}_{out}}{\widehat{i}_g}\right|_{\widehat{v}_{in},\widehat{d}_1,\widehat{d}_2=0} = Z_{out}(s) = \{[(Z_1||Z_2) + Z_7]\,||R\} \tag{36}$$

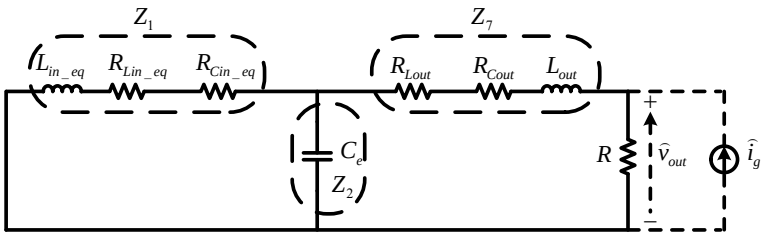


Figure 8: Manipulated circuit to derive $Z_o(s)$.

Manipulating (36), the output impedance TF can be derived and it is expressed as:

$$\left.\frac{\widehat{v}_{out}}{\widehat{i}_g}\right|_{\widehat{v}_{in},\widehat{d}_1,\widehat{d}_2=0} = Z_{out}(s) = R.\left[\frac{a_{17}s^3 + a_{18}s^2 + a_{19}s + a_{20}}{b_1 s^3 + b_2 s^2 + b_3 s + b_4}\right] \tag{37}$$

3.4. Derivation of the Open-Loop Audio Susceptibility

Setting the input control variables, $\widehat{d}_1 = 0$ and $\widehat{d}_2 = 0$ and disregarding the effects of variations in the circulating currents, the circuit shown in Fig. 9 is obtained, which allows the audio susceptibility or input-to-output voltage TF ($M_v(s)$) to be derived. By solving the equivalent circuit, the following expression can be obtained:

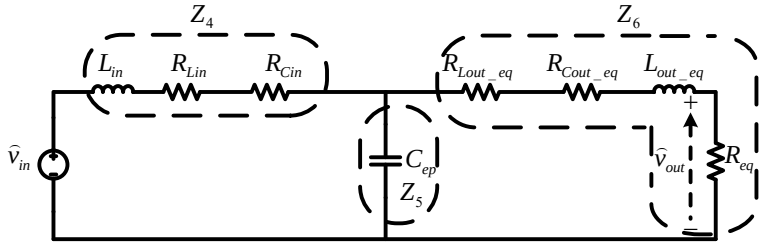


Figure 9: Manipulated circuit to find the audio susceptibility transfer function.

$$\left.\frac{\widehat{v}_{out}}{\widehat{v}_{in}}\right|_{\widehat{d}_1,\widehat{d}_2=0} = M_v(s) = \frac{D_2}{1-D_1}.\frac{R_{eq}}{Z_6}.\left[\frac{(Z_5||Z_6)}{(Z_5||Z_6)+Z_4}\right] \tag{38}$$

Through analytical simplification, the audio susceptibility can be expressed as:

$$\left.\frac{\widehat{v}_{out}}{\widehat{v}_{in}}\right|_{\widehat{d}_1,\widehat{d}_2=0} = M_v(s) = R.D_2.(1-D_1)\left[\frac{1}{b_1 s^3 + b_2 s^2 + b_3 s + b_4}\right] \tag{39}$$

4. Stability Analysis

In this section, the frequency responses of the input control-to-input current and the output control-to-output current transfer functions using the proposed modulation strategy are analyzed considering the condition $d_1 > d_2$. The bode plots shown in Figs. 10 and 11 are obtained considering the parameters presented in Table 1.

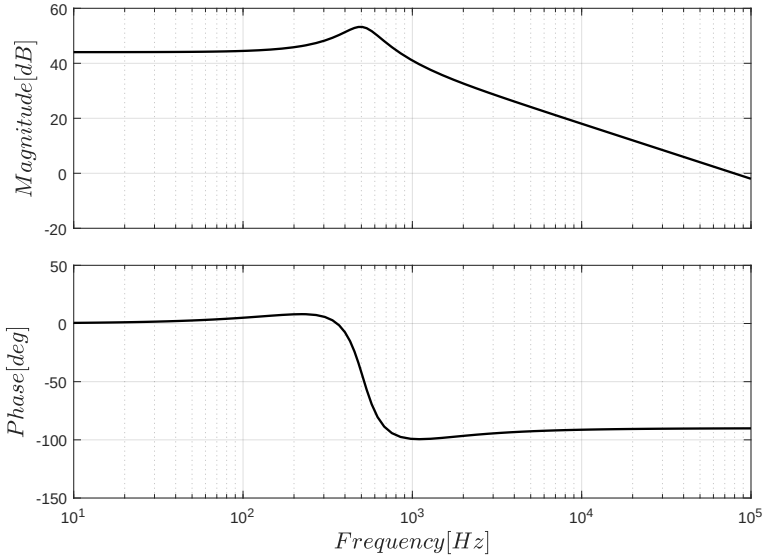


Figure 10: Frequency response for $\hat{i}_{Lin}/\hat{d}_1$.

By analyzing the frequency responses shown in Fig. 10, it can be observed that the proposed modulation strategy demonstrates a stable behavior. It presents an infinite gain margin, since throughout frequency range the open-loop phase is kept higher than -180^o, whereas the phase margin is close to 90^o when the frequency is equal to 79.4 kHz.

Fig. 11 shows that the frequency response for the output stage present a gain margin equals to $-25.9dB$ at 478Hz, whereas the phase margin is equal to 93.2^o

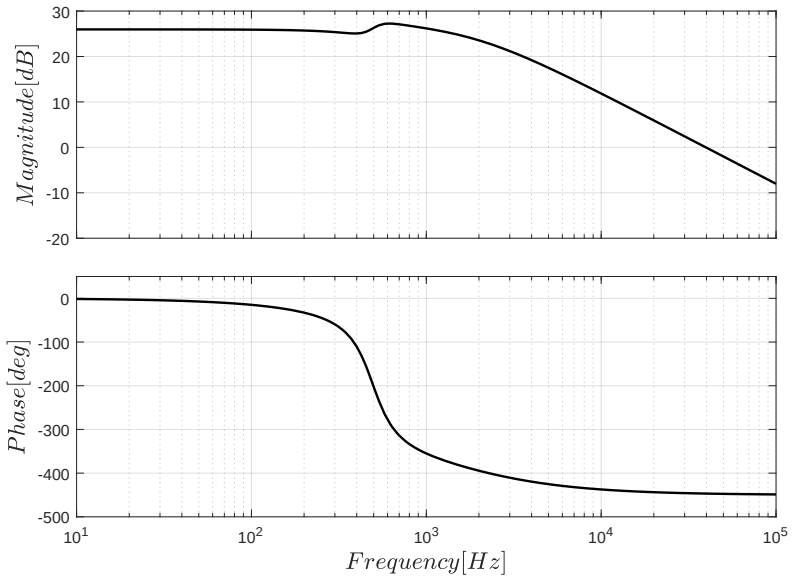


Figure 11: Frequency response for $\hat{i}_{Lout}/\hat{d}_2$.

at 39kHz. Nevertheless, the transfer function did not present a high overshoot, easing the tuning process when designing regulators such as a proportional-integral (PI) controller.

Therefore, it can be stated that for different parameter values of the converter, the conclusion about stability is maintained.

5. Results

After modeling the bidirectional DC-DC boost-buck converter, the equivalent small-signal equations, equivalent small-signal circuit, control transfer functions, input and output impedance, and the audio susceptibility were obtained. Therefore, to validate the analysis for the novel modulation strategy, simulation results in time and frequency domains are presented. In time, the small-signal equations given in (18) to (22), and the boost-buck converter with parasitic elements Fig. 3, are compared to validate that the model can predict the transient responses of the circuit under perturbations in the input voltage and in the in-

put and output duty cycles. The results obtained in frequency domain correlate the behavior of the TFs with the simulated boost-buck topology to ascertain that the model is capable of performing the same characteristics. The circuit was simulated in PSIM® while the transfer functions and the mathematical model were derived using Matlab-Simulink®. The energy storage elements can be obtained using equations (3) to (5) and Table 1 presents the parameters used in the simulations.

Table 1: Simulation Parameters

Input Power	$P_{in} = 3500W$
Input voltage	$V_{in} = 150V$
Output voltage	$V_{out} = 300V$
Input inductor	$L_{in} = 1mH$
Input inductor resistance	$R_{Lin} = 10m\Omega$
Output inductor	$L_{out} = 2mH$
Output inductor resistance	$R_{Lout} = 10m\Omega$
Capacitor	$C = 10\mu F$
Capacitor resistance	$R_C = 10m\Omega$
Load	$R = 25\Omega$
Input leg duty cycle	$D_1 = 0.7$
Output leg duty cycle	$D_2 = 0.6$
Switching frequency	$F_s = 40kHz$

The simulation comparing the AC and DC terms with the boost-buck converter was done by perturbing the input and output duty ratios, the input voltage and the load, as follows:

a) The small-signal input voltage $\widehat{v}_g$ starts with value equals to 0V.

b) At t = 0.025s: negative step in $\widehat{d}_1$ equals to 0.02.

c) At t = 0.05s: positive step in $\widehat{d}_1$ equals to 0.01.

d) At t = 0.075s: a positive step in $\widehat{v}_g$ equals to 80V.

e) At t = 0.1s: negative step in $\widehat{v}_g$ equals to 50V.

f) At t = 0.125s: positive step in $\widehat{d}_2$ equals to 0.05.

g) At t = 0.15s: negative step in $\widehat{d}_2$ equals to 0.03.

h) At t = 0.175s: negative step in the load equals to -50% of the nominal value.

i) At t = 0.2s: positive step in the load equals to +50% of the nominal value.

Figs. 12 to 15 show the temporal comparison of the input and output currents and the capacitor and output voltages under different perturbations in the input voltage, duty cycles and load. The results corresponding to the mathematical model are represented as a black line, and the converter responses are shown in a orange trace. The model duty cycles, $\hat{d}_1$ and $\hat{d}_2$, are displayed in dashed blue and orange lines while the converter duty ratios are shown in continuous red and black lines, respectively. The model and the topology input voltages are given in dashed blue and continuous red lines.

As expected, the input current is most influenced by perturbations in the input duty cycle in contrast to the output duty ratio, because it changes the charging time of the input inductor and, consequently, the capacitor voltage level also varies. Furthermore, when the output duty cycle suffers perturbations, the input current also changes. Similar behavior can be concluded for the output current.

Observing Fig. 14, it is noticed independence of the capacitor voltage from the output duty cycle, misleading to the conclusion that the input switch can only control the capacitor voltage. This fact requires to be explained because the simulations presented in this paper consider the system operating in open loop conditions. If a control strategy is applied in the input current, it makes possible to control the capacitor voltage once the input duty cycle is not fixed. Therefore, both duty cycles would change to keep the power balance between the input and the output. Besides, it is noted that during all perturbations, the model was able to predict the behavior of the circuit, which validates the analysis.

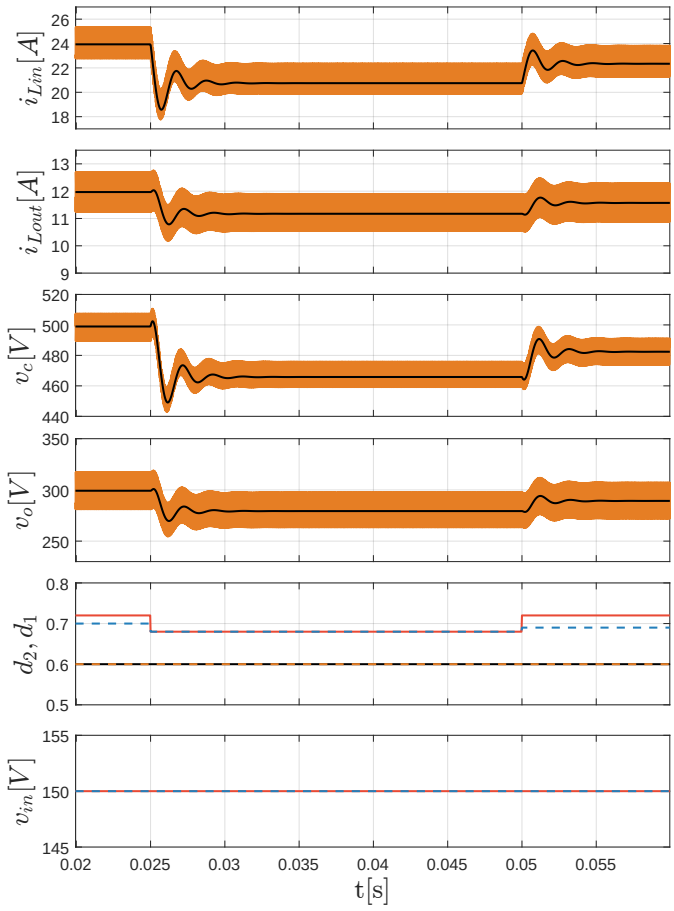


Figure 12: Time domain responses of the mathematical model and the boost-buck converter during perturbations in the input duty ration, where $[0.02 < t \leq 0.06]$. In the voltage and current waveforms, the orange line represents the simulated circuit response and the black trace is the behavior of the DC and AC terms from the small-signal model. For the duty cycles, the red and black lines are the circuit's input and output duty ratios, respectively, while the blue and orange dashed lines are the model's input and output duty cycles.

According to [26], mathematical analysis of the dynamic response during load variations can be performed by perturbing the AC small-signal terms whereas the DC small-signal ones are set to zero. Fig. 15 shows that in t = 0.175s, the load changes to 50% of its initial value. On the other hand, at t

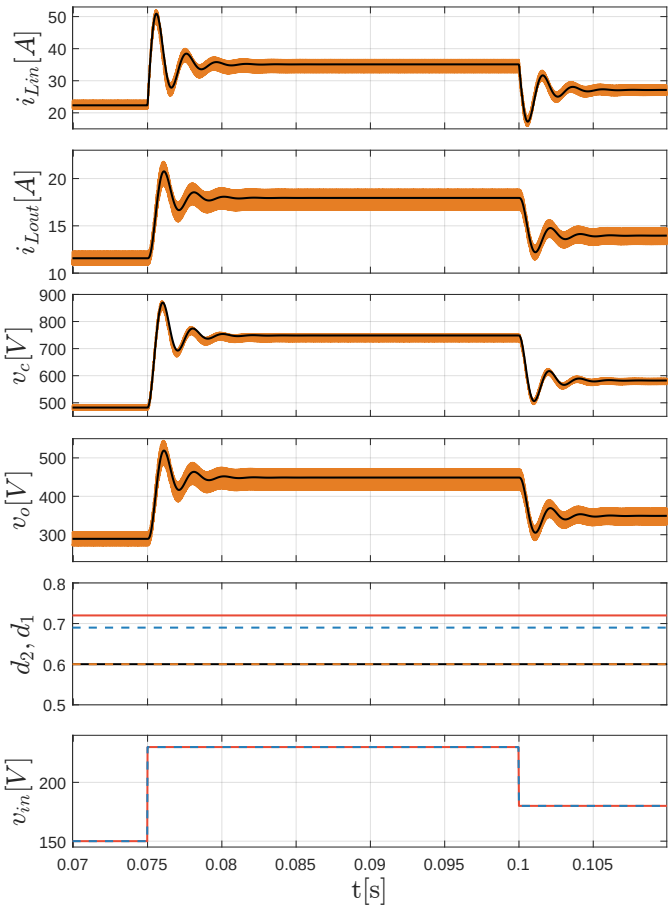


Figure 13: Time domain responses of the mathematical model and the boost-buck converter when the input voltage is perturbed, in which $[0.07 < t \leq 0.11]$.

= 0.2s, the load step represents 1.5 time the nominal value.

By observing the results given in Fig. 15, it can be noted that the output voltage presents two spikes during the transients which are caused by the sudden change in the load. Even though the circuit response present such high perturbations, the mathematical model can predict this behavior showing the same dynamical response.

In Fig. 16, the RMS currents in switches S_1 and S_3, which determine the

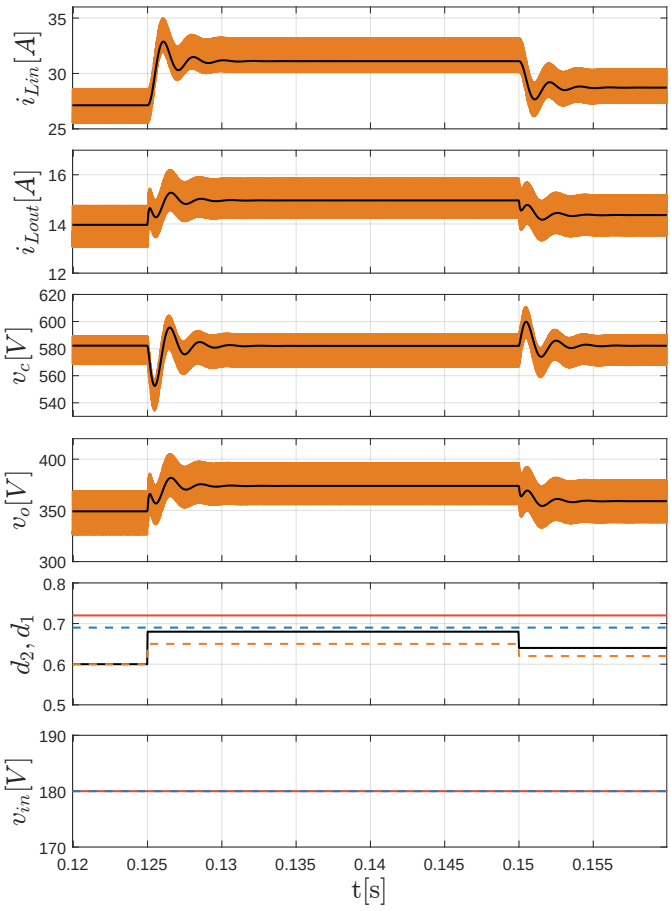


Figure 14: Time domain responses of the mathematical model and the boost-buck converter when the output duty ratio varies, where $[0.12 < t \leq 0.16]$.

conduction losses, are compared for different voltage ratios when different modulation strategies are employed. The comparison is done when the topology is operated in step-up mode since the proposed application requires the converter to extract the maximum power from the PV array to feed the load. By observing this figure, it can be noted that the strategy proposed in [9] presents lower RMS current flowing through the input switch S_1, whereas the Case I presents a slightly higher current level, having a difference smaller 2% for the highest

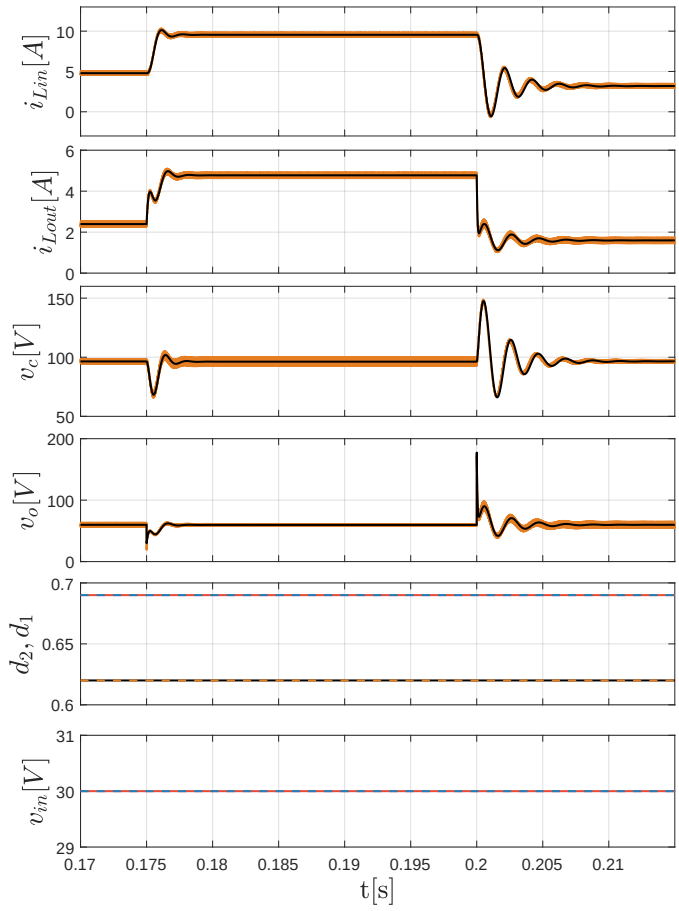
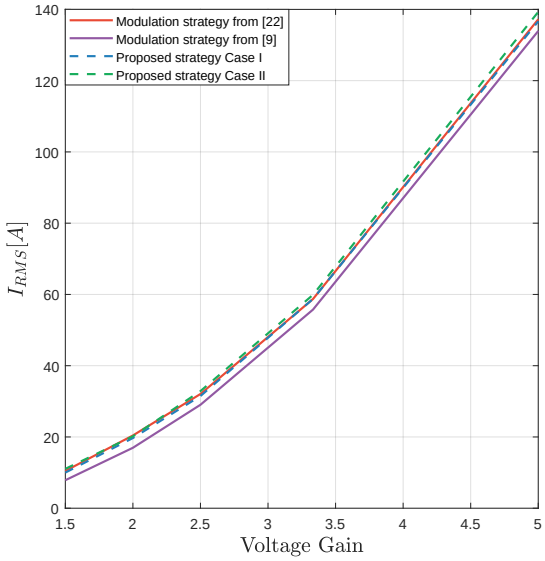


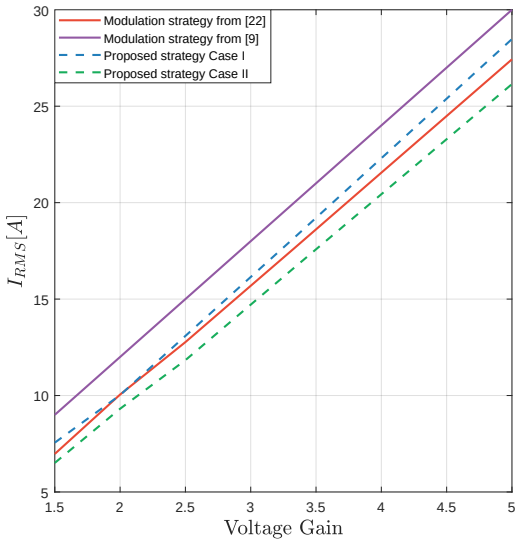
Figure 15: Time domain responses of the mathematical model and the boost-buck converter during different load conditions, where $[0.17 < t \leq 0.22]$.

voltage ratio. However, for the RMS current in the switch S_3, the proposed modulation strategy Case II has the best performance. The results indicate that the current level is 5% smaller than that proposed in [22] and 13% lower than the one proposed in [9] when the voltage gain is equal to 5.

As a conclusion, the modulation strategy proposed in this paper presents the lowest RMS current in the switches considering the evaluation in both legs, which results in the best operating condition of the converter from the point of



(a) RMS current for switch S_1.



(b) RMS current for switch S_3.

Figure 16: RMS current comparison for different modulation strategies: a) RMS current flowing through S_1, and b) RMS current flowing through S_3.

view of the total conduction losses.

For the open-loop control TFs and audio susceptibility, three distinctive scenarios were simulated:

(a) An ideal topology, in which the solid red line represents the TF, while the simulated circuit response is presented in blue dots.

(b) Converter with all parasitic resistances equal to $10m\Omega$, whereby the TF is drawn as a solid black trace, and the circuit is given in a green "+" line.

(c) The parasitic capacitor resistances is increased to 1Ω, where the solid magenta line represents the transfer function and a cyan dashed line for the circuit response.

According to the results shown in Figs. 17 to 20, it can be observed that the frequency responses of the circuit are in close agreement with the TFs, validating the proposed model. Furthermore, the transfer functions $\hat{v}_C/\hat{d}_2$ and $\hat{i}_{Lout}/\hat{d}_2$ are more affected by the capacitor parasitic resistance. This fact can be explained because the capacitor resistance is reflected to the input and output sides of the converter, and for the second stage it is increased by the output duty cycle D_2 directly, while in the input it is multiplied by $1 - D_1$. Moreover, for Fig. 20, it is noted a small gain in low frequencies, meaning that the output duty cycle has no effect over the capacitor voltage in open-loop strategies, respecting the results obtained in the time domain analysis.

For audio susceptibility TF, the frequency response simulation was done for the three conditions above. From Fig. 21, it can be observed that the parasitic elements have a minimum effect over the audio susceptibility, even when the capacitor internal resistance is increased; thus, the location of the poles and zeros are fixed for different parasitic levels. Furthermore, it can be concluded that the transfer functions can predict the circuit response.

The frequency response for the input impedance $Z_{in}(s)$ is given in Fig. 22. The solid red line is the result obtained from the TF, while the dotted blue line is the values obtained from the circuit. As it can be observed, the magnitude plot behaves similarly to the inverted input control-to-input current, whereby the DC gain is smaller due to the rejection of the capacitor voltage value. Moreover, the input impedance presents characteristics of a series resonant circuit,

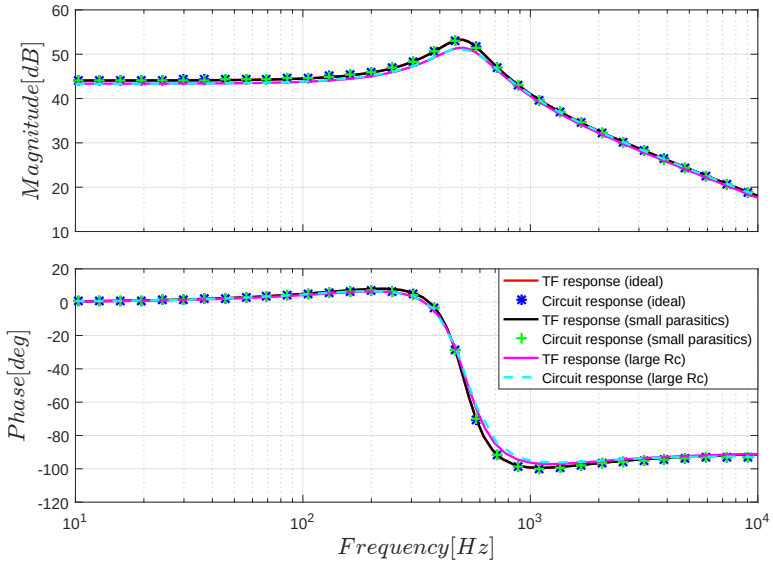


Figure 17: Frequency responses for $\hat{i}_{Lin}/\hat{d}_1$.

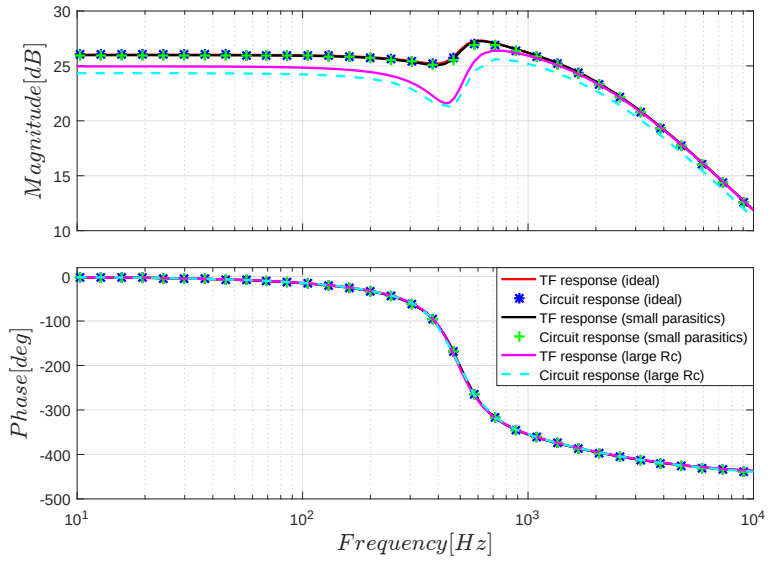


Figure 18: Frequency responses for $\hat{i}_{Lout}/\hat{d}_2$.

in which there is a small DC gain for low frequencies and for the values above the resonance frequency, which in this case is approximately 500Hz, the gain

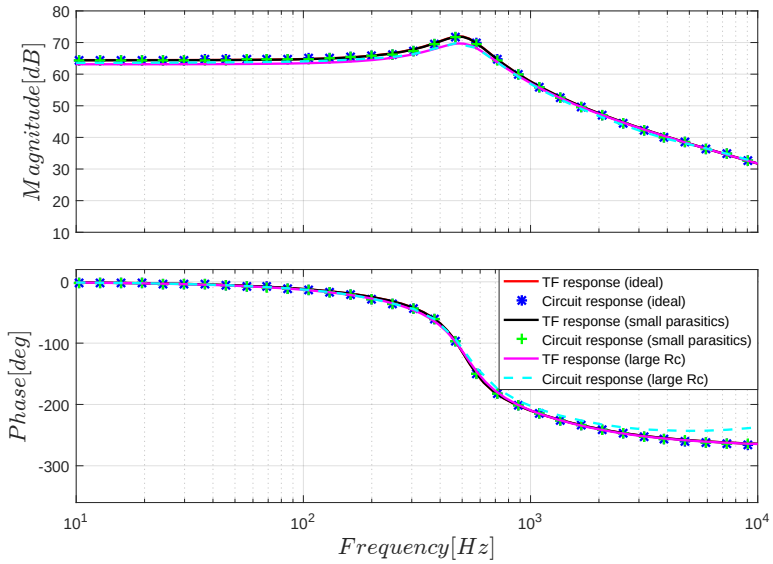


Figure 19: Frequency responses for $\hat{v}_C/\hat{d}_1$.

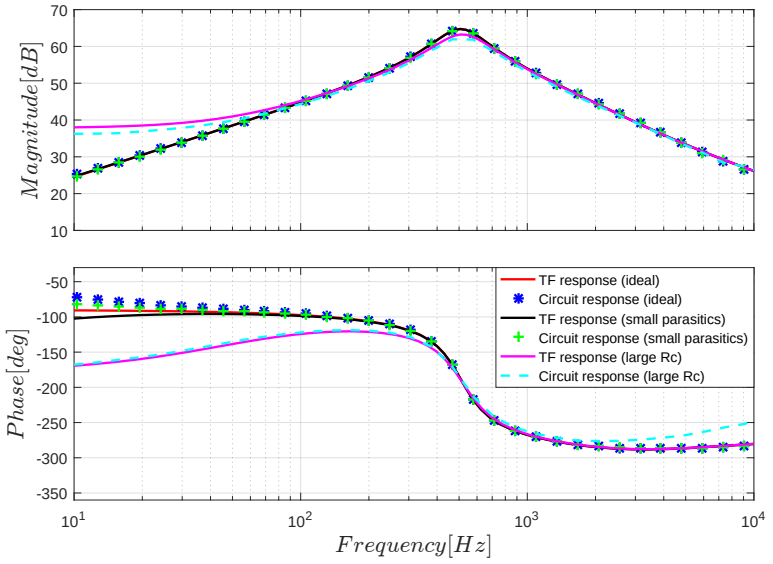


Figure 20: Frequency responses for $\hat{v}_C/\hat{d}_2$.

increases rapidly. This can be explained due to the fact that the numerator of the transfer function given in $Z_{in}(s)$ presents higher order than the denomina-

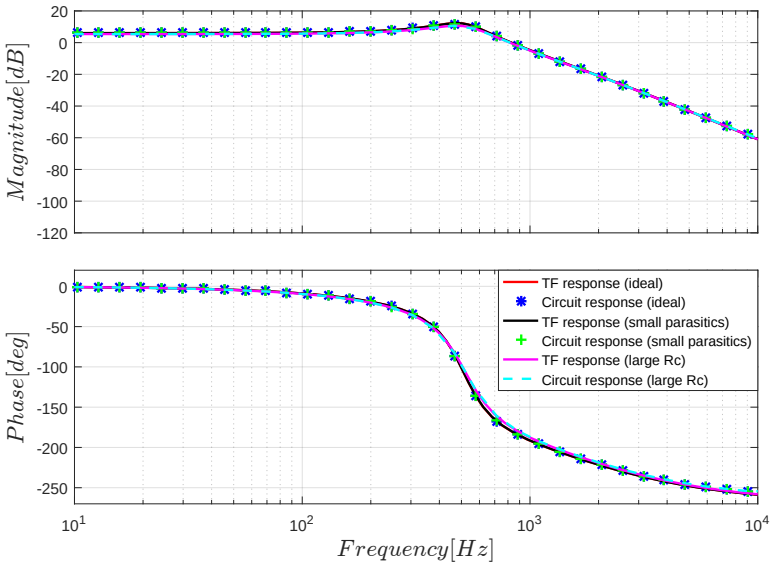


Figure 21: Frequency responses for M_v.

tor. Besides, the high frequency behavior is dominated by the presence of a high-frequency zero.

The bode plots for the output impedance $Z_{out}(s)$ are presented in Fig. 23. Similarly to the transfer function $\hat{v}_C/\hat{d}_2$, it is noted a small DC gain in low frequencies, because the output voltage, which is used to derive $Z_{out}(s)$, is directly affected by the capacitor voltage. Furthermore, the frequency response is also similar to those of a parallel resonant circuits.

6. Conclusion

The dynamic model of the bidirectional DC-DC boost-buck converter was presented. The modulation strategy consists in applying different duty cycles for each leg, increasing the converter robustness because the input stage can be controlled neglecting the impact of perturbations in the output, and, at the same time, the output stage can be regulated disregarding disturbances in the input part.

Firstly, the working principle of the ideal topology was described when it is

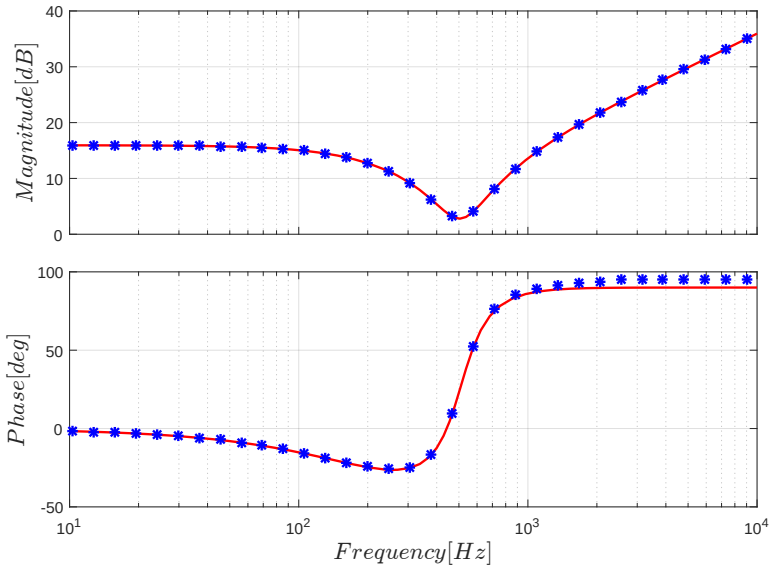


Figure 22: Frequency response for Z_{in}. The red line represents the frequency response obtained from $Z_{in}(s)$, while the dotted blue trace is the response of the simulated circuit.

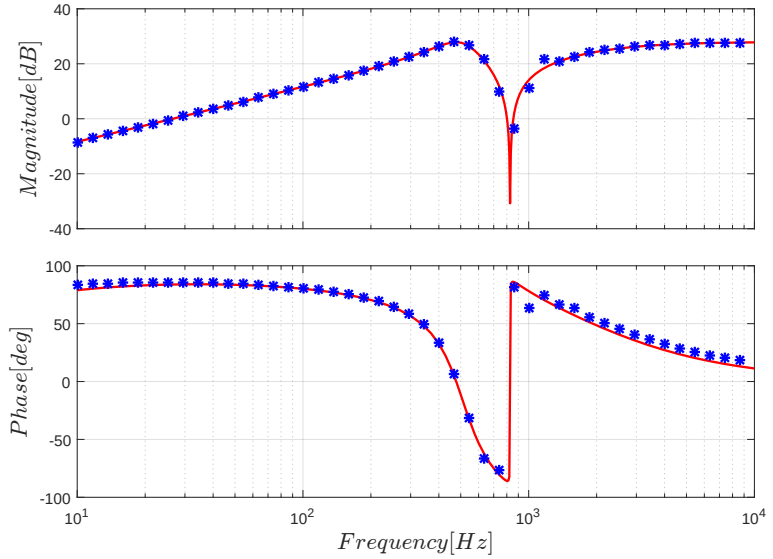


Figure 23: Frequency response Z_{out}. The red line represents the frequency response obtained from $Z_{out}(s)$, while the dotted blue trace is the response of the simulated circuit.

regulated by the proposed modulation strategy, giving the bases to design the passive elements. In addition, the parasitic elements were added in the inductors and the capacitor, to provide a closer dynamic representation of the topology. Moreover, the non-linear average model was obtained and by using the small-signal model technique, the DC and AC small-signal terms were derived and used to gather the equivalent small-signal circuit. In this circuit, it was observed that the capacitor parasitic resistance is reflected to the input and output stages; thus, the capacitor series resistance has no direct effect on the small-signal capacitor voltage. Furthermore, employing the superposition principle in the equivalent circuit, the control transfer functions were obtained along with the input and output impedance and the audio susceptibility.

Simulation results in time domain confirmed that the mathematical model could predict the behavior of the boost-buck converter during perturbations in the input and output duty cycles as well as for input voltage disturbances. Also, it was stated that when the system has no current control in its input current, the output switch is unable to control the capacitor voltage. The same phenomena were observed when the control transfer functions and the circuit were compared in the frequency domain. Moreover, the frequency responses of the control transfer functions for an ideal case and with small parasitic elements presented insignificant gain and phase differences. On the other hand, when the capacitor series resistance was increased, the output control transfer functions were more affected than the input control ones, due to the reflection of the term to the output of the converter. Finally, the obtained frequency response for the input and output impedance and the audio susceptibility are also in close agreement, even during high gain and phase transitions.

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Appendix A. Reflected Parameters

$L_{in\_eq} = L_{in}\left(\frac{D_2}{1-D_1}\right)^2$;
$R_{Lin\_eq} = R_{Lin}\left(\frac{D_2}{1-D_1}\right)^2$;
$R_{Cin\_eq} = R_C\frac{D_2^2}{1-D_1}$;
$C_e = \frac{C}{(D_2)^2}$;
$V_{C\_eq} = V_C\left(\frac{D_2}{1-D_1}\right)$;
$I_{Lin\_eq} = \frac{I_{Lin}}{D_2}$;
$I_{Lout\_eq} = \frac{I_{Lout}}{D_2}$;
$L_{out\_eq} = L_{out}\left(\frac{1-D_1}{D_2}\right)^2$;
$R_{Lout\_eq} = R_{Lout}\left(\frac{1-D_1}{D_2}\right)^2$;
$R_{Cout\_eq} = R_{Cout}\left(\frac{1-D_1}{D_2}\right)^2$;
$R_{eq} = R\left(\frac{1-D_1}{D_2}\right)^2$;
$C_{ep} = \frac{C}{(1-D_1)^2}$.

Appendix B. Coefficients of the Transfer Functions

$Z_1 = L_{in\_eq}s + R_{Lin\_eq} + R_{Cin\_eq}$;
$Z_2 = \frac{1}{C_e s}$;
$Z_3 = L_{out}s + R_{Lout} + R_{Cout} + R$;
$Z_4 = L_{in}s + R_{Lin} + R_{Cin}$;
$Z_5 = \frac{1}{C_{ep}s}$;
$Z_6 = L_{out\_eq}s + R_{Lout\_eq} + R_{Cout\_eq} + R_{eq}$;
$Z_7 = L_{out}s + R_{Lout} + R_{Cout}$;
$a_1 = CL_{out}V_C$;
$a_2 = L_{out}I_{Lin}\,(1 - D_1) + CV_C(R + R_{Lout} + R_{Cout})$;
$a_3 = V_C D_2^2 + I_{Lin}(1 - D_1)(R_{Lout} + R + R_{Cout})$;
$a_4 = L_{in}L_{out}I_{Lin}$;
$a_5 = L_{out}\,(D_1 - 1) + L_{in}I_{Lin}\,(R + R_{Lout} + R_{Cout}) + L_{out}I_{Lin}(R_{Lin} + R_{Cin})$;
$a_6 = I_{Lin}R_{Lin}R_{Lout} + V_C R_{Lout}(D_1 - 1) + V_C R(D_1 - 1) + I_{Lin}R_{Lout}R_{Cin} +$
$I_{Lin}RR_{Lin} + V_C R_{Cout}(D_1 - 1) + I_{Lin}RR_{Cin} + I_{Lin}R_{Cin}R_{Cout} + I_{Lin}R_{Lin}R_{Cout}$;

$a_7 = L_{in}CV_C;$

$a_8 = CV_CR_{Lin} + CV_CC_{in} - L_{in}I_{Lout}D_2;$

$a_9 = V_C(1 - D_1)^2 + I_{Lout}R_{Cout}(D_1 - 1) - I_{Lout}R_{Lin}D_2;$

$a_{10} = L_{in}L_{out}I_{Lout};$

$a_{11} = L_{in}I_{Lout}R_{Lout}+L_{out}I_{Lout}R_{Lin}+L_{in}I_{Lout}R+L_{out}I_{Lout}R_{Cin}+L_{in}I_{Lout}R_{Cin}+$
$L_{in}V_CD_2 + L_{in}I_{Lout}R;$

$a_{12} = I_{Lout}R_{Lin}R_{Lout}+I_{Lout}R_{Lout}R_{Cin}+V_CR_{Lin}D_2+I_{Lout}RR_{Lin}+V_CR_{Cout}(1-$
$D_1) + I_{Lout}RR_{Cin} + I_{Lout}R_{Cin}R_{Cout}D_2 + I_{Lout}R_{Lin}R_{Cout};$

$a_{13} = L_{in}L_{out}C;$

$a_{14} = L_{in}CR_{Lout} + L_{out}CR_{Lin} + L_{out}CR_{Cin} + L_{in}CR + L_{in}CR_{out};$

$a_{15} = L_{out}(1-D_1)^2+L_{in}D_2^2+CR_{Lin}R_{Lout}+CR_{Lout}R_{Cin}+CRR_{Lin}+CRR_{Cin}+$
$CR_{Cin}R_{Cout} + CR_{Lin}R_{Cout};$

$a_{16} = R_{Lout}(1 - D_1)^2 + R(1 - D_1)^2 + R_{Cout}(1 - D_1)^2 + R_{Cout}D_2 + R_{Lin}D_2^2;$

$a_{17} = L_{in}L_{out}C;$

$a_{18} = L_{out}CR_{Cin} + L_{in}CR_{Cout} + L_{out}CR_{Lin} + L_{in}CR_{Lout};$

$a_{19} = L_{out}(1-D_1)^2+CR_{Cin}R_{Cout}+CR_{Lout}R_{Cin}+CR_{Lin}R_{Cout}+L_{out}CR_{Lin}+$
$L_{in}D_2^2;$

$a_{20} = R_{Lout}(1 - D_1)^2 + R_{Lin}D_2^2 + R_{Cin}R_{Cout}D_2 + R_{Cout}(1 - D_1)^2;$

$b_1 = CL_{in}L_{out};$

$b_2 = CL_{in}R_{Lout} + CL_{out}R_{Lin} + CL_{in}R + CL_{in}R_{Cout} + CL_{out}R_{Cin};$

$b_3 = L_{out}(1 - D_1)^2+L_{in}D_2+CR_{Lin}R_{Lout}+CR_{Lout}R_{Cin}+CRR_{Cin}+CR_{Cin}R_{Cout}+$
$CR_{Lin}R_{Cin} + CRR_{Lin};$

$b_4 = R_{Lout}(1 - D_1)^2 + R(1 - D_1)^2 + R_{Lin}D_2^2 + R_{Cin}D_2^2 + R_{Cout}(1 - D_1)^2;$

$b_5 = CL_{out};$

$b_5 = C(R + R_{Lout} + R_{Cout});$

$b_6 = D_2^2.$

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