A Reprogrammable Graphene Nanoribbon-Based Logic Gate

***Abstract*—In this article, taking into consideration the exceptional technological properties of a unique 2-D material, namely Graphene, we are envisioning its usage as the structure material of a non-back-gated re-programmable switching device. The proposed topology is analyzed in depth, not only by verifying its operation and re-programmability as a 2-input XOR, 3-input XOR and 3-input Majority gate, but also by examining its computing performance in terms of area, delay and power dissipation. More specifically, we are utilizing L-shaped Graphene Nanoribbons (GNRs) to develop comb-shaped Graphene based switching devices. These devices are in position with effective programming through biasing to design any combinatorial circuit as resulting from the aforementioned universal set of Boolean gates. The resulting figures of merit regarding the area with a universal footprint of 2.53 nm^2 for every gate independently of the number of inputs, the propagation delay with 2.05 10^{-2} ps and, last but not least, the power dissipation with only 10.204 nW for the gates with greater number of inputs, are quite encouraging and promising. Moreover, the ability of the proposed topology to pave the way towards the implementation of basic circuits has been further investigated, by demonstrating an example of a 1-bit full adder cell and its sufficient operation arriving from the corresponding successful SPICE simulation results.**

***Index Terms*—Graphene, nanoribbon transistors, nanoelectronic circuits.**

INTRODUCTION

Graphene pioneered the field of 2D materials when it was introduced for the first time. In fact, it was theoretically described many years before; however, researchers managed to isolate it only back in 2004. It was the first 2D material to be thermodynamically stable and one of the most recent nano- materials [1], [2]. After its invention and successful isolation, it sparked high interest throughout the research community, in many different fields. The main reason forthis ever-increasing research interest is the very compelling properties ofthe mate- rial, which promise to provide new ground-breaking properties in applications spanning from electronics to biotechnology, con- struction, and many more, or even bringing together different scientific fields.

One of the areas in which Graphene is considered to be able to play a significant role and push its future development, is the area of electronic circuits. The material entails properties that are very appealing in the field of electronics, and more specifically for the realization of electronic devices, that will comprise computing and sensing systems. Very high thermal conductivity [3], as well as electrical conductivity many times higher than that of Silicon, are named as the two most significant properties for the field of electronics, as well as the field of energy and power-related applications. Apart from that, Graphene's optical and some mechanical properties are very attractive, especially in combination with previously mentioned electronic properties, for realizing electronic devices with enhanced features, that will empower electronics for special applications. The transparency of Single-Layer Graphene (SLG), absorbing only 2.3% of light in the visible spectrum, is ideal for light sensing applications, as well as for transparent electronics. The high Young's modulus of Graphene can also be exploited not only for sensors, but in general, for flexible electronics, electronics applied on flexible substrates fabrics and other special materials [4]. Another key characteristic of Graphene that is very appealing to the research community and can possibly enable bringing together biology with electronics, is its biocompatibility [5], [6]. Graphene, albeit the existence of some contradictory results considering its cyto- toxicity, in general, is considered to be a biocompatible material, in specific forms and with a high correlation to its fabrication method. This biocompatibility feature can really come in handy for the realization of biosensors, bioimaging applications as well as tissue engineering [7].

Apart from all those possible uses in future electronics and electronics for special applications, Graphene, is considered to be one of the main candidates for the post-silicon era. Many different forms of Graphene have been tested for the implemen- tation of switching devices, such as Carbon Nanotubes (CNTs), Graphene Oxide (GO), Fullerene and Graphene Nanoribbons (GNRs). The latter is considered to be one of the most promising forms of Graphene for realizing ultra-fast switches with en- hanced properties. Graphene Field-Effect Transistors (GFETs) and similar to them devices have been already presented both in theoretical and experimental forms [8]. Also, GNR-based devices have been proposed for the implementation of devices with hysteresis, that can be used in Neural Network (NN) accelerators, in the form of synapses [9], [10], [11].

However, Graphene in its pristine form is a zero bandgap material, meaning that it has a metallic behavior and cannot effectively operate as a switch. In order for this problem to be surpassed and induce bandgap to Graphene, many different methods have been proposed. Among those methods is the application of external electric bias [12] or magnetic bias [13], the stacking and twisting of Graphene [14], as well the Graphene shape modulation [15], [16]. This last method specifically, can be noted as the topology awareness of Graphene and has been exploited in many different ways. While each approach has its advantages and disadvantages, the question remains: what is the most effective way to modulate the conductance of a GNR device, induce a bandgap, and preserve its properties for usage in different applications?

In this work, we are leveraging the topology awareness of Graphene in order to create a device that is able to operate as a switch, without the demand of a back-gate terminal. We then use that switch in order to create a single topology that owns the property of re-programmability, in an attempt to expand the use of Graphene, especially GNRs, in the field of re-configurable computing, in a different way compared to what has been previ- ously proposed [17], [18], [19]. More specifically, we are using the

L-shaped GNRs, which have been proven to be able to oper- ate satisfactorily enough as switches [20]. In Section II, we con- duct for the first time a design space exploration on the devices and investigate the effects of their geometrical and structural characteristics on their electrical characteristics. The simulation method for the investigated devices is analytically exposed in Section III. Sections IV-A and IV-B present a re-programmable comb-shaped device that with effective programming through biasing, can operate as 2-input XOR and 3-input XOR gate respectively. In Section IV-C the operation of this topology is extended for the first time, showcasing its ability to operate also as a 3-input Majority gate through simple reprogramming. In Section IV-D, we also present the first circuit consisted purely by comb-shaped topologies, a full adder unit, which is comprised of a XOR gate and a Majority gate and whose operation is verified through SPICE simulations, for the first time for that type of devices. In addition to the presentation of the topologies, we extend our investigations by including some significant metrics considering computing devices, which are the area, delay, and power, in comparison with state-of-the-art CMOS circuits, as well as another state-of-the-art low-power complementary GFET-based architecture [12] in Section V. The resulting figures of merit regarding the area with a universal

footprint of $2.53\ 10^{2}$ nm^2 for every gate independently of the number of inputs, the propagation delay with $2.05\ 10^{-2}$ ps and, last but not least, the power dissipation with only 10.204 nW
for the gates with greater number of inputs, are quite encouraging and promising. Finally, in Section VI, the conclusions of the manuscript are drawn.

I. L-Shaped Graphene Nanoribbons

Graphene nanoribbons, amongst all the allomorphs of Graphene, are considered to be one of the most promising for the realization of electronic devices. In their pristine form, they are very short-width Graphene lattices of a few nanometers, with a high length to width ratio. They can be boldly clustered into two main categories based on the orientation of their edges, the zig-zag edged GNRs (zGNRs) and the armchair GNRs (aGNRs) [21] which plays a very significant role in their electronic behavior. In their simplest zig-zag-edged form, they reportedly present no bandgap, which is a prohibitive feature for nano switches. In our approach, we expand Graphene nanoribbons from their simplest straight form to an L-shaped form. As previewed in Fig. 1(a), an L-shaped GNR is in fact a combination of the two aforementioned different types of GNRs, the zGNR, and the aGNR. This combination seems to be capable of creating a small bandgap in the GNRs' band structure, which is clearly visible in the energy dispersion to conductance diagram of Fig. 1(b), calculated using the state of the art atomistic level modeling tool, that is described analytically in Section III. This gap realization has been attributed to the scattering phenomena that are introduced through this edge direction change from zGNR to aGNR [20]. In addition, L-shaped GNRs allow for easy conductance tuning through the application of external electric bias in the form of top gates. In contrast to common GFETs, additional electric biasing through any form of back gate terminal is not required. This feature provides another level of freedom, as it does not require Graphene to be placed on top of a thick insulating layer. The proposed devices can thus be placed on top of every compatible substrate, elastic, fabric, organic etc.

A. L-Shaped GNR Sizing

The sizing of the proposed topology is crucial not only in order to compete with the state-of-the-art scaling trends, bubecause it proves to affect its operation and performance. A very significant parameter is the ratio between the width of the zGNR and the aGNR part of the device. As presented in Fig. 2, this ratio significantly affects both the high conductance value (OFF-state) and low conductance value (ON-state) of the branches. With the red line, we mark the lowest conductance value (Fig. 2(b)) and the highest conductance value (Fig. 2(c)) for a set of different width aGNR-zGNR combinations. Choosing a set of bigger sized branches, more to the right top corner of the graphs, will provide a switch with a higher high-conductance value as seen in Fig. 2(c), but also with a poor low conductance value as seen in Fig. 2(b). On the other hand, choosing very low GNR widths for both the horizontal and vertical part of the branch, will lead to a device with a very small low-conductance value but a very poor high-conductance value. Thus, the dimensions of the device have to be chosen carefully keeping in mind to maintain as good as possible both high and low conductance values. Fig. 2 also presents a phenomenon of periodicity that connects the dimension ratio of the device with its conductance. The aGNR size is dominant, as for specific values of aGNR width, the device generally has higher conductance and is not strongly affected by the zGNR. This phenomenon of dependency of the conductance on the dimensions is probably due to the overlapping of the energy bands of zGNRs and aGNRs with specific dimensions.

For our simulations, we have selected the dimensions of the branches with the strategy to maintain an ON/OFF ratio of around

10^{4}. Thus the selected dimensions are 3.266 nm for the width of the horizontal part and 5.78 nm for the width of the vertical part, as shown in Fig. 2(a), keeping in mind that such small- sized branches are not so easy to be fabricated with the current fabrication technology. However, several experimental reports have proposed fabrication techniques that can provide GNRs of dimensions similar to the ones that we propose [22]. In any case, the designer can make his own decision depending on his needs, based on Fig. 2. This decision will also be finally reflected in the performance of the device.

B. Top Gate Sizing

The gate size is also a significant aspect that must be care- fully examined during the design of the device, as it affects its

performance. The total gate area is the determinant factor of the device's parasitic capacitance as described in Section III-A, which will then affect the total delay of the device. Apart from that, as it has been proven both theoretically and experimentally, the length of the Graphene nanosheet does not significantly affect the total resistance of the device, mainly due to the ballistic transport, making the impact of the size (the length, as depicted in Fig. 2(a)) of the top gates as the main variable, which will determine the total length of the L-shaped GNR. As depicted in Fig. 3, the size of the top gates indeed has a significant effect on the conductance of the GNR. Fig. 3(a) presents the effect of different gate sizes on the conductance of a switched-off L-shaped GNR, while Fig. 3(b) presents the same effect on a switched-on L-shaped GNR. As those figures indicate, the effect on the OFF-state of the GNR is far more intense compared to the effect on the ON-state. In Fig. 3(a), the maximum value is $6 \quad 10^3$ bigger than the minimum, while in Fig. 3(b), the maximum value is only 2 bigger than the minimum. The maximum value of normalized conductance in both cases is encountered for a device with very small gates, which is reasonable, as applied electrical potential influences only a very small amount of carbon atoms. The increase of gate size, leads to a decrease on conductance. Also, both Fig. 3(a) and (b) show an antisymmetric relation, implying that the location of the different-sized gates is not significant. For the design of the presented topology, due to the severity of the effect described above, we have selected the size (length) of the gates to be both at 4.8 nm, as marked with the red square in the figures. This is the only operation point from those explored, that can provide the desirable ON/OFF ratio of the device, which is equal to 10^4. Top gates of bigger length, may, probably, lead to even better results, leading however to a device with a bigger active area footprint. However, the results of our simulations indicate that gate-to-gate distance primarily impacts the device's area footprint, rather than its functional performance.

C. *Top Gate Biasing*

In Fig. 3(c), we have investigated the operation of an L-shaped GNR with 2 top-gates, under the influence of different potential values, in order to reasonably select the operating voltage of the proposed topology. It is clear that we can separate the operation of the device in 3 different generalized categories. The 1st category refers to the case where both top gates are connected to the ground, in which the device is tuned to the highest possible conductance, depending on its dimensions. The 2nd category refers to the case where the top gates are biased with voltage of different polarity. This is practically depicted by the two blue regions of Fig. 3(c), where the device is tuned towards very low conductance values. The 3rd category refers to the case where the top gates are biased with a voltage of the same polarity. For this case, the values of the normalized conductance span in a very small range from 0.4 up to 0.7 regardless of the absolute value or the sign of the applied voltages. Having said that, it is obvious that the operation of each top gate is similar to the operation of a mechanical valve in a pipe line (i.e., graphene branch). As Fig. 3(c) implies, when all the applied biases have the same polarity, the flow of electrons and thus current, is allowed, setting the GNR to the ON-state, while when there are different polarity biases, the corresponding branch is not conductive, tuned to the OFF-state. A GNR that utilizes 3 top gates, like those we will be using in Section IV, operates based on the same principle: When all the top gates are biased with same polarity potentials, then the GNR is tuned to the ON-state. On the contrary, when one of the top gates is biased with opposite polarity potential compared to the others, then the GNR is tuned to the OFF-state.

From Fig. 3(c) becomes obvious that the device needs po- tentials with different polarity on its inputs and top-gates in order to operate and provide an acceptable ON/OFF ratio. Thus, we do need to use a negative value for the logic level 0 that will provide easier device cascadability and a positive value for the logic level 1. Also, Fig. 3(c) clearly shows that the minimum conductance value is encountered when the top gate biases have the value pair of 0.5 Volts and 0.5 Volts. This is practically the top-gate bias combination that sets the L-shaped GNR to the OFF-state. In summary, for the effective switching operation of the L-shaped GNRs, we used 0.5 Volts for the logic 1, and 0.5 Volts for logic 0. The high conductance operating point (ON-state) at $(V_{TG1}, V_{TG2}) = (0.5 \text{ Volts}, 0.5 \text{ Volts})$ or $(+0.5 \text{ Volts}, +0.5 \text{ Volts})$, provides a device with a conductance only 2.3 smaller than the highest possible conductance at $(V_{TG1}, V_{TG2}) = (0 \text{ Volts}, 0 \text{ Volts})$, which is depicted with yellow color in Fig. 3(c). We have also used ground (0 Volts) for the programming of the topology, as we present in the following Sec- tions IV-B and IV-C. Grounding a top-gate practically eliminates its participation in the tuning of the conductance of the GNR, which is now determined by the rest of the top-gate potentials.

II. Computational Method

The investigation of the use of Graphene as a material that comprises computing devices requires a simulation method that is able to take under consideration all the phenomena that play a decisive role in determining its electronic behavior. There have already been proposed a couple of different compact models for GNR-based Field-Effect Transistors (GNRFETs), that practically lead to parametrized equivalent circuits, allowing for easy and fast SPICE simulations, in an attempt to ease the GNRFET-based circuit design process [23], [24], [25]. However, the most accurate GNR device simulation is achieved through atomistic simulations. The state-of-the-art numerical tool that is used for computing the energy band structure of Graphene and thus its conduction consists of the combination of the Tight-Binding Hamiltonian (TBH) model [26], [27], with the Non-Equilibrium

Green's Function method (NEGF) [28], [29]. This powerful atomistic level modeling technique describes effectively the quantum transport phenomena, such as the ballistic transport of carriers that governs the operations of Graphene-based devices. First the TBH is used for the description of the total energy of the system based on the geometry of the device, which is then passed to the NEGF method for further calculations. TBH provides a great amount of freedom in terms of the shape and the lattice condition of the simulated device. Apart from shape variations, it allows for easy inclusion of grid defects, and bonds with other interstitial atoms as well as the investigation of any other possible grid anomaly [30]. It also embeds the effects of any applied external potential such as top-gate and back-gate biases. After that, the NEGF is responsible for calculating the conductance and current of the device with proven accuracy in comparison to experimental results. In this work, we are leveraging the topology awareness of Graphene through the use of L-shaped devices, which will be included in the simulation through the TBH; a square matrix given by (1):

$$H = -\tau \quad \hat{c}_i \hat{c}^{\dagger}_j, \qquad (1)$$

It practically resembles the eagerness of an electron to hop from one legal lattice site to another. The extreme case of $\tau = 0$ leads to an electron being unable to hop to another atom, practically an isolated system. Equation (1) in its extensive form can model any range of atom interconnec- tion; however, in this implementation we are only taking under consideration nearest neighbor interactions, in an attempt not to increase the required computational power and time while not

requires the G^R and G^A from (2) and can be produced as follows:

$$A = i \left[G^R - G^A \right]. \qquad (6)$$

The DoS is the number of legal energy states in a system of a specific volume, in a specific energy range.

Finally, the 4th step of this method leads to the calculation of the conductance of the investigated nanodevice, in a range of energies. This calculation directly leads to the realization of the energy dispersion diagrams.

losing almost any of the method's accuracy.

Then, the investigated geometry is passed as a square Hamiltonian matrix, calculated through TBH, to the NEGF method. The NEGF method describes the response of the nanodevice when carriers pass through it as well as the interactions between the carriers themselves. The method can be separated into 4 discrete steps, that lead to the calculations of all the needed quantities. Each step is described by an equation. The 1st step computes the retarded Green's function in the following way, as described by (2):

This complex simulation method provides very accurate results for the electronic properties and in this case for the conductance (and thus the resistance) of the GNR, based on its shape, dimen- sions and grid condition, and applied potentials. However, the calculation of further parameters is necessary for a better inves- tigation of GNR-based devices, including their performance as circuit components.

$$G^R = [EI - H - \Sigma_1 - \Sigma_2 - \cdots - \Sigma_N]^{-1}, \qquad (2)$$

In that generalized form of (2), the retarded Green's function (G^R) is calculated for any given number of contacts of the device [20]. Those contacts are introduced into the system by the self-energy factors, $\Sigma_{1\ldots N}$. Also E, represents the energy level of the carriers passing through the GNR and I is the square Identity matrix. The calculation of the advanced Green's equation is also required as an intermediate step before the use of (3) and can
easily derive G^R as follows: $G^A = (G^R)^{\dagger}$.

The 2nd step of the NEGF method is the calculation of G^n:

A. Parasitic Capacitance

Parasitic capacitances play a significant role in determining operating dynamic characteristics of gated computing devices, mainly the propagation delay t_{pd} and the dynamic power dissipa- tion. Especially carbon-based gated devices like CNT FETs and GFETS, constitute a special case. Apart from the ordinary par- allel plate capacitance of the top-gates (C_{ox}), they also display another form of capacitance, the quantum capacitance (C_q). The C_{ox} is based on the geometrical characteristics of the top-gate and is calculated by the following well-known formula

$$G^n = G^R \Sigma^{in} G^A, \qquad (3)$$

$$C = kE$$

$$A, \qquad (8)$$

G^n is practically a quantity that represents the density of carriers at a specific energy level, E. G^A is the previously reported advanced Green's function while the Σ^{in} factor describes the effects of all the externally applied power sources to the in- vestigated system. This can be computed through the following equation:

$$\Sigma^{in} = f_1\Gamma_1 + f_2\Gamma_2 + \cdots + f_N\Gamma_N. \quad (4)$$

In this generalized form, f_N is the Fermi energy of every contact that comprises the investigated device. In the same manner, Γ_N is the broadening factor of every available contact in the system. Those broadening factors quantify the interaction of the metallic

$$C_{ox} = \frac{k\varepsilon_0 A}{d}$$

where k, and d are the dielectric constant and the thickness of the gate dielectric respectively, E_0 is the permittivity of empty space, A is the area of the top-gate.

Plenty of research has been conducted considering the de- termination of the quantum capacitance of Graphene. For our calculations, we have leveraged the analytical formula presented in [32], the results of which have been in also in accordance with experimental results [33], [34], [35]. The formula is:

$$C_q = \frac{2q^2 k_B T}{\pi(\hbar v_F)^2} \ln 2 \left(1 + \cosh\frac{qV_g}{k_B T}\right), \quad (9)$$

contacts of the device with the main body of the nanoconductor, GNR and can be calculated with the help of the aforementioned self-energies through the (5) below:

$$\Gamma_{1,2,\ldots,N} = i\left[\Sigma_{1,2,\ldots,N} - \Sigma_{1,2,\ldots,N}\right], \quad (5)$$

where N is again equal to the number of contacts. The addition of every individual product in (4) calculates the total self-energy of the system Σ^{in}.

The 3^{rd} step of the NEGF method is to calculate the density of states (DoS) of the carriers in the nanodevice. This calculation where $\hbar$ is the Planck constant, q is the electron charge, k_B is the Boltzmann constant, v_F $c/300$ is the Fermi velocity of the Dirac electron, c is the speed of light in vacuum and V_g is the voltage of the Graphene channel. Cq shows a clear dependence on the voltage applied on Graphene and thus the DOS. The two capacitances are practically connected in series, meaning that the total capacitance of a gate can be calculated as in (10):

$$C_{tot} = \frac{C_q \times C_{ox}}{C_q + C_{ox}} \quad (10)$$

Fig. 4. (a) Top and side view of the proposed comb-shaped GNR-based 2-input XOR gate. The substrate is presented with green color, the Graphene sheet with black, insulator layers with orange, ohmic metallic contacts in direct contact with Graphene are presented with red color, and metallic contacts of the top gates with purple. (b) Top view of the proposed comb shaped GNR-based 3-input XOR gate. (c) Top view of the proposed comb shaped GNR-based 3-input MAJ gate.

B. Delay Estimation

The delay induced by the proposed topology is estimated through the Elmore delay model. In this estimation, apart from the resistance of the Graphene channel, the resistances of the contacts are taken into consideration. The Elmore delay model for the proposed topology can be previewed in (11):

by the formula:

$$P_{dynamic} = C_{tot} V_{dd} f, \quad (12)$$

where C_{tot}, is the total capacitance of the capacitors being charged and discharged during the operation of the topology, V_{dd} is the operating voltage and f is the operating frequency. Thus, the total power dissipated by the topology during its operation

(11)
is calculated as $P_{tot} = P_{static} + P_{dynamic}$.

III. GNR Comb-Shaped Topology

I. where R_{GNR} is the resistance of the Graphene nanoribbon, $R_{C,L}$ and $R_{C,R}$ are the resistances of the left and right contacts of the device, respectively and C_{tot} is the total parasitic capacitance as calculated in (10). $C_{\min}$ is the conductance between the input and output contacts, which is equal to quantum capacitance C_q. Due to its very low value, (11) can be approximately rewritten as $t_{pd} = (R_{GNR} + R_{C,L} + R_{C,R})\ C_{tot}$. The values of the contact resistances are considered to be the same and were based on various experimental results. Common values for contact resistances on GNR-based devices have been reported in the bibliography to span at a range from as low as $30\,\Omega\ \mu$m, up to almost $1\,\text{K}\Omega\ \mu$m, for contacts of various different met- als [36], [37], [38]. For the provided calculations, a value of $R_{C,L} = R_{C,R} = 200\,\Omega\ \mu$m was selected, as it is very common for the vast majority of the contact materials, and also used as the contact resistance value in [39].

C. Power Dissipation

For the estimations of the power dissipation of the proposed topology, we have included both the static power (P_{static}) and the dynamic power ($P_{dynamic}$). For our calculations, we have designed a simple DC-equivalent and conducted SPICE simulations in order to calculate the total static power dissi- pation of comb-shaped topology. For the SPICE simulations, we have exploited the NEGF method for the calculation of the conductance at various operating points in the operation voltage range. Every different steady state of the circuit was examined separately (the 4 different states of the 2-input XOR gate and 8 different states of the 3-input XOR gate and the Majority gate, each one representing 1 row of the corresponding truth table), and only the worst case for each gate was included in Table V. The portion of the dynamic power was also included, calculated

Through the combination of multiple L-shaped GNRs, we have proposed a comb-shaped topology presented in Fig. 4(a), taking inspiration from the one proposed in [40]. Apart from the substrate, the topology consists of 4 ohmic contacts, 3 input and 1 output, and 5 top-gates for external electric bias application. The top-gates comprise metallic electrodes that are separated from the Graphene channel through an insulator (i.e. Al_2O_3). The two out of five top-gates are shared by two branches, while the remaining three top-gates belong solely to one branch each. Through that count of top gates, we can have a re-programmable topology, which operates accordingly under the influence of different top-gate and input voltage combinations.

A. GNR 2 Input XOR Gate

The proposed re-programmable comb-shaped topology can be tuned to operate as a 2-input XOR gate, by setting its top- gate biases and inputs to the appropriate signals, as shown by Fig. 4(a). The way that the device operates is inspired by the architecture of the universal set of logic gates that have already been presented [41]. However, there is a major difference, in this approach that is presented here, input signals are applied not only on the top gates, but also in the input terminals, passing through the device itself, and thus operating in a way that reminds the operation of pass transistor logic circuits (PTL).

Fig. 4(a) shows the proper biasing of the comb-shaped topol- ogy for the operation of the 2-input XOR gate. The single-branch top gates have fixed biases, logic 0 for the top and bottom branches, and logic 1 for the middle branch. Logic level 1 is equal to 0.5 Volts and the logic level 0 is equal to 0.5 Volts. Also in the input terminals, the proper values must be applied in order the topology to produce the output of $A\ B$. In the top branch, the value of signal B is applied, in the bottom branch the value of signal A, while the middle branch value is constant and equal to the value of logic 0.

The valid operation of the proposed topology with the appro- priate programming can be verified through the validation of a 2-input XOR gate truth table, such as Table I. The validation of this operation will be conducted through the examination of the state of each different branch of the device (namely the top middle and bottom branches), under all four different input combinations.

For the case of both inputs A and B being at the logic 0, from Fig. 5 occurs that the top and bottom branches which are both described by Fig. 5(a) are switched ON, while the middle branch is switched OFF, as described in Fig. 5(b). Thus, both the logic values of A and B, which are equal to logic 0, are delivered to the output. Similar is the operation of the device with an input of A and B being equal to logic 1. Now the top and bottom branches' conductance is described by Fig. 5(b), while only the middle branch is switched ON (Fig. 5(a)), passing the value of logic 0 to the output.

There are also two cases where the two inputs, A and B, do not have the same logic value. In both those cases the middle branch is switched OFF, as described by Fig. 5. When A is equal to logic 1 and B to 0, the value of A passes to the output from the bottom branch, which is switched ON. Similarly, when A is equal to logic 0 and B is equal to logic 1, the value of B passes through the top branch to the output.

B. GNR 3-Input XOR Gate

As an extension to the aforementioned 2-input XOR gate, we have proposed a topology that implements a 3-input XOR gate. The topology presented in Fig. 4(b), is practically the same

re-programmable topology of Fig. 4(a), with different applied signals. The extension from a 2-input to a 3-input XOR gate demands an increase of the input signals maintaining, however, the same occupied area.

The proposed topology of Fig. 4(b), has the top-gates of the top and bottom branch biased with the value of input C and the value of the top-gate of the middle branch grounded (0 Volts). The only difference in the input signals is that now in the middle branch, the value of input C is applied.

As proof of the valid operation of the proposed topology, we will analytically investigate the accordance with the truth table of the 3-input XOR gate as proposed in the 4th column of Table II. The operation of this topology can be examined in 3 separate categories.

The first category refers to the cases where only A and B inputs have the same logic value. In those cases, only the middle branch is switched ON, with a conductance tuned as in Fig. 5(a), when both the top-gate biases are positive, or tuned as in Fig. 5(a) when both the top gate biases are negative. In those cases, the value of input C passes to the output, verifying the 2nd and 7th rows of the truth table.

The second category is the one where A and B have different logic values. In all those cases, the middle branch is switched OFF. The switched ON branch is every time one, either the top or the bottom, and more specifically each time the one that has top-gate biases of the same value. All those cases cover from the 3^{rd} up to the 6th row of the truth table.

Finally, the third category covers the extreme cases where all the input signals have the same value. In those cases all three branches are switched ON, passing the same value to the output, either logic 0, covering the 1st row of the truth table, or logic 1, covering the 8th row of the truth table.

C. GNR Majority Gate

The technology of re-programmable comb-shaped devices allows for the realization of a Majority gate, which in com- bination with the XOR gates presented in Sections IV-A and IV-B, enables the creation of a half adder and a 1-bit full adder cell. Therefore, it is crucial to achieve the realization of the Majority gate. A first approach of a comb-shaped GNR-based Majority gate has already been presented [42], however, our proposed topology operates differently, by passing the input signals through the devices, more similar to the PTL circuits operation, allowing for the realization of a re-programmable topology and performance optimizations.

The operation of the majority gate can thus be replicated by the aforementioned 3 branch comb shaped topology. In fact, the only differences now, in comparison to the previously described 2-input and 3-input XOR logic gates, are the different locations of the externally applied signals (inputs A, B, C that pass through the device).

The proposed device utilizes shared input gates that retain the initial signal values of inputs A and B. Additionally, the 3 single-branch top-gates also retain their values during the 3-input XOR gate operation. The only alteration occurs at the inputs of the device, where the applied signals from top to bottom branch are A, B, and C, respectively. This topology can be observed as being appropriately biased in Fig. 4(c).

Similar to Section IV-B, we will analytically examine the operation of the proposed device to confirm its effectiveness as a majority gate through the MAJ column of Table II. The operation of this majority gate topology can be divided into three distinct categories.

The first category represents the cases where only A and B have matching logic values. In these cases, the middle branch is the only one switched ON and is described by the energy dispersion diagram of Fig. 5(a) when A and B are equal to logic level 0 and Fig. 5(d) when A and B are equal to logic level 1. As a result, only the logic value of B is passed to the output, being either 0 for the 2nd or 1 for the 7th row of the truth Table(II).

The second category encompasses cases where A and B pos- sess different logic values. Those where A and C have the same value, set the top branch to a switch ON state, and pass the value of input A to the output, as outlined in rows 3 and 6 of Table II. Similarly, those where B and C have the same value, set the bottom branch to a switch ON state and pass the value of C to the output, successfully verifying rows 4 and 5 of Table II.

The third category entails extreme cases where all three inputs have the same value. In both those cases, all three branches are set to a switch ON state, visible in Fig. 5(a), when the input value is equal to logic 0 and in Fig. 5(d) when the input value is equal to logic 1. Those cases cover also the 1st and 8th row of Table II.

D. GNR Based Full-Adder

As a first proof of the usefulness of the aforementioned presented topology, we have utilized it as building block of a basic 1-bit Full Adder (FA) cell. The realization of a full adder is a natural outcome of the presented XOR and MAJ gates. In fact, the direct equivalent of a Full Adder cell is a combination of a 3-input XOR gate for the calculation of the SUM part and a 3-input

Majority gate for the calculation of the CARRY part, as presented in Fig. 6, along with its truth table (Table II). In the latter, it becomes obvious that the truth table of SUM, indeed matches that of a 3-input XOR gate and the truth table of the CARRY, matches that of a 3-input Majority gate.

Thus, for the implementation of an 1-bit Full-Adder cell, we have used two appropriately programmed comb-shaped topologies, as in Fig. 6(b). The top with the red background is programmed to operate as a 3-input XOR gate, and the bottom is programmed to operate as a 3-input Majority gate. Our proposed cell demands only two comb-shaped GNR devices, maintaining a very low device count, in comparison with the conventional 28 T CMOS FA cell. The interconnects of such devices can be implemented through either metal or Graphene wires [43], [44] and this is going to be part of future research upon devices fabrication.

For the verification of its valid operation, the results of SPICE simulations are presented in Fig. 7. The operation of the circuits was examined with an operating period of 400 ps, in order to provide a fair comparison with the other presented architectures, as described in [12]. The results show an accurate operation that perfectly validates both the truth tables of SUM and Carry. Some spikes appear at both the output signals, at around 0.4 ps and 1.2 ps. Those spikes coincide with the simultaneous tran- sition of two different inputs (inputs B and C for both cases), which momentarily tunes two different branches of a single comb-shaped topology to similar resistance values, affecting the output voltage. However, this change in the output voltage, does not have an amplitude big enough to affect the operation of the device (it is not bigger than the 50% of total voltage range). Also, the circuit manages to overcome this instability in a very small amount of time and as it will operate always between two clocked flip-flops, those small intermediate signal variations, will not affect the final output.

For the case of the area, as a first observation comes that all three implemented logic gates have the same area footprint. This is a straight outcome to the fact that the initial topology is re-configurable and does not require any shape or dimension changes, just a re-arrangement of the applied signals. In terms of absolute numbers, the area covered by the implemented gates is $2.532\ 10^2$ nm^2. Compared to its CMOS counterparts it is 9.5 , 19 and 86 better for the cases of 2-input XOR gate, 3-input XOR gate and 3-input Majority gate, respec- tively. In comparison with its state-of-the-art complementary GFET counterparts, it is very close, being only 6 bigger for the case of 2 input XOR gate and 5 bigger for the cases of 3-input XOR and Majority gates. Also in the case of the Majority gate, it is 50% smaller than the previous approach on comb-shaped majority gate [42], considering that it uses the exact same dimensions at its Graphene branches. In this case and in the search for optimization, in a manner more similar to the PTL circuits, we have implemented a Majority gate using
programmable topologies.

IV. Results and Discussion

Apart from the operation evaluation that we have carried out, we have also tested our topology in terms of performance. As mentioned in Section III, and is presented in Tables III, IV, and V, we have examined the performance of our topologies, measuring their area, delay and power and compared it with state-of-the-art complementary GFET [12] and 7 nm FinFET CMOS architectures [12], [45].
with the 2-input and 3-input XOR gates. The examined circuit, the FA cell, consists of 2 GNR comb-shaped re-configurable topologies, thus its size is calculated to be a bit higher than 2 times the area of a single comb-shaped topology. In absolute numbers, as shown in Table V, the total area of the FA is calculated to be $5.265\ \ 10^2$ nm^2, which is 57 smaller, and 3 bigger than its CMOS and complementary GFET counterparts, respectively.

For the estimations of the transition delay, we have leveraged the Elmore delay model, as described in Section III-B. The computed delay here is again the same for all-three investigated cases. This result is also based on the fact that the device is the same for each implemented gate, with the only difference being the different signal locations. In other words, it does not de- pend neither on the transistor count changes, as in conventional CMOS, nor the gate size, as happens in complementary GFET. We have calculated a fixed delay of 0.02054 ps, which is
446 , 668 and 535 better than its CMOS counterparts for the cases of 2-input XOR, 3-input XOR and 3-input Major- ity gates, respectively. The proposed comb-shaped topology has also similar and slightly better performance in comparison with the complementary GFET architecture. It is 364 , 77 and 5 faster for the cases of 2-input XOR, 3-input XOR and 3-input Majority gates, respectively. For those calculations, we have examined all possible input combinations that can lead to an output transition. From all those input to output transitions, we kept only the worst-case scenario. Due to the symmetry of the device, where all top-gates have the exact same size, and all branches have the same dimensions, the worst case produces always the same delay. Our 1-bit FA implementation consists of a single 3-input XOR gate for the SUM part, and a single 3-input Majority gate for the Carry part of the circuits. Thus, the total delay of the circuit is equal to the delay of the worst part of the circuit. In this case, as the two gates are practically designed with the exact same GNR comb-shaped topology but with different programming, the total delay is equal to the delay of the 3-input XOR and Majority gate, calculated to be equal to
$2.052\ 10^{-2}$ ps. This is 578 and 93 smaller than its CMOS and complementary GFET counterparts, respectively.

Finally, for the power dissipated, we present again the worst case for each one of the examined logic gates. The static part of the

total power dissipation was calculated with the help of a simple dc-equivalent circuit of the topology, simulated through SPICE, as mentioned in Section III-C. For the dynamic part, we leveraged the (12). For the sake of comparison, the selected device clock period was 400 ps equal to the period of the GFET and CMOS gates implementations [12]. The power dissipated is slightly lower in the case of the 2-input XOR gate, than in the cases of the 3-input XOR and Majority gates. This is an outcome of the fact that the 3 single-branch top-gates in the case of 2-XOR, have fixed potential (Fig. 4(a)), while for the 3-XOR and MAJ, 2 out of 3 single-branch top-gates are biased by the C-input signal, which is not constant (Fig. 4(b) and (c)). Thus, even though the static power is equal for the three cases as the topology remains the same, the dynamic power dissipation is higher at the 3-input gates causing this small difference. In absolute numbers, the total power dissipated by the 2-XOR gate is as low as 9.536 nW and by both the 3-input gates, it is
10.204 nW. This makes the proposed topologies 62 , 173 and 341 more power efficient than its CMOS counterparts for the cases of 2-input XOR gate, 3-input XOR and Majority gates respectively. Its performance in terms of power is a lot closer to that of the complementary GFET architecture. By comparing them, our proposed comb-shaped topology is only
6 , 6 and 3 worst in terms of power dissipation for the cases of 2-input XOR,3-input XOR and Majority gates respectively. As estimated, the total power dissipated by the 1-bit FA cell, is calculated to be equal to the power of its components, which is 20.408 nW. This is 388 more power efficient than its CMOS alternative and 3 more power con- suming than its complementary GFET counterparts. The figure of merit of this work, goes beyond the re-programmability of the proposed topology, which introduces Graphene in the field of re-configurable computing, and the ability to functionally operate without the use of a back gate contact which allows for easier combination with alternative substrate materials. In terms of performance, the proposed comb-shaped topology manages to provide favorable results. It is implied through Tables IV and V, as well as stated in Table VI, that our topology per- forms ideally, also when other approaches are considered, in terms of the Power-Delay factor, which describes the efficiency of the device, and practically represents the energy that each logic gate consumes in order to complete an operation. The

results compared to the CMOS architecture are anticipated, as comb-shaped GNRs are performing better in terms of power and delay. The comparison with the complementary GFET results for a slightly superior power-delay product for the pro- posed topology, mainly owing to the lower delay of the comb shaped topology that manages to overcome the worst power performance when compared with complementary GFET. More specifically, for the cases of the 2-input XOR, 3-input XOR, the Majority gate, and also the proposed FA cell, the comb- shaped topology manages to provide a power delay product 66 ,
12.5 , 1.5 and 28 lower compared to its complementary GFET topologies.

V. Conclusion

In this article, we have leveraged the special electronic proper- ties of Graphene, in order to present a re-configurable computing topology. In this manner, we have proposed a re-programmable comb-shaped GNR-based topology, which is able to operate as a 2-input XOR gate, a 3-input XOR gate, and a 3-input Majority gate, with appropriate biasing. As a proof of concept, we have also presented a 1-bit full adder cell, based on the aforemen- tioned topology. This topology works in a way similar to that of PTL circuits and, moreover, does not require back gate biasing in order to operate, allowing for a wider variety of applications. We have investigated the effect of different dimensions of the topol- ogy on its electric properties and specified its dimensions and geometry based on the results. We have enriched the simulation method with capacitance calculations, that enable the analysis of the parasitics of the proposed device. Then, we have analytically exposed the operation of the topology as a re-programmable logic gate and explained the 3 different operation modes, pre- senting as well a basic circuit element as a proof of concept. We have evaluated the operation of the three different gates using the energy dispersion to conductance diagrams in order to verify the conductance of each branch in every possible input combination and, thus, verifying the truth table of every different gate. Finally, through the added features in the simulation, we have estimated some key characteristics of the topology, the area footprint with
a universal value of $2.532\ 10^{2}$ nm^2, the propagation delay with a value of $2.054\ \ 10^{-}2$ ps and the power dissipation at
10.204 nW. We have compared the corresponding results with
metrics for complementary CMOS and state-of-the-art comple- mentary GFET counterparts and showcased very competitive outcome and quite encouraging perspectives. This work clearly indicates that GNR devices can be used as computing blocks with favorable characteristics and find application in PTL and re-configurable computing.

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