IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 19 October 2023, accepted 19 November 2023, date of publication 21 November 2023,
date of current version 30 November 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3335387

RESEARCH ARTICLE

High-Performance and Energy-Efficient Leaky Integrate-and-Fire Neuron and Spike Timing-Dependent Plasticity Circuits in 7nm FinFET Technology

MOHAMMAD KHALEQI QALEH JOOQ[1], MOSTAFA RAHIMI AZGHADI[2], (Senior Member, IEEE), FERESHTEH BEHBAHANI[3], ALAADDIN AL-SHIDAIFAT[1], AND HANJUNG SONG[1]

[1]Department of Nanoscience and Engineering, Centre for Nano Manufacturing, Inje University, Gimhae 50834, South Korea
[2]College of Science and Engineering, James Cook University, Townsville, QLD 4811, Australia
[3]Department of Electrical and Electronic Engineering, Shahed University, Tehran 33191-18651, Iran

Corresponding author: Hanjung Song (hjsong@inje.ac.kr)

This research was supported by the Brain Pool program funded by the Ministry of Science and ICT through the National Research Foundation of Korea (2022H1D3A2A02081529). This work was also supported by the National Research Foundation of Korea (NRF) grant funded by the Korea Government ((MSIT) NRF-2022R1F1A1063656).

ABSTRACT In designing neuromorphic circuits and systems, developing compact and energy-efficient neuron and synapse circuits is essential for high-performance on-chip neural architectures. Toward that end, this work utilizes the advanced low-power and compact 7nm FinFET technology to design leaky integrate-and-fire (LIF) neuron and spike-timing-dependent plasticity (STDP) circuits. In the proposed STDP circuit, only six FinFETs and three small capacitors (two 10fF and 20fF) have been utilized to realize STDP learning. Moreover, 12 transistors and two capacitors (20fF) have been employed for designing the LIF neuron circuit. The evaluation results demonstrate that besides 60% area saving, the proposed STDP circuit achieves 68% improvement in total average power consumption and 43% lower energy dissipation compared to previous works. The proposed LIF neuron circuit demonstrates 34% area saving, 46% power, and 40% energy saving compared to its counterparts. The neuron can also tune the firing frequency within 5MHz-330MHz using an external control voltage. These results emphasize the potential of the proposed neuron and STDP learning circuits for compact and energy-efficient neuromorphic computing systems.

INDEX TERMS Neuromorphic, LIF neuron, synapse, STDP, FinFET.

I. INTRODUCTION

Undoubtedly, computers are among the most important inventions in modern human life, influencing everything from industry, military, and agriculture to even human daily activities. Computers utilize the von Neumann architecture for data processing. In the von Neumann architecture, processing and storage are performed separately using the processor and memory units [1]. Von Neumann computers have successfully addressed data processing needs over the past decades. However, the continuous demand for miniaturizing computing systems with fast, or even real-time operation, has led to the establishment of neuromorphic computing systems [2]. In neuromorphic computing systems, processing and storage occur simultaneously, providing much faster operation with lower power consumption. Moreover, by moving the control from data centers to edge devices, neuromorphic systems are the most promising pathways to the future of high-performance computers [3].

As a brain-inspired computer, neuromorphic computing systems are comprised of two cardinal units: neuron and synapse circuits. The flexibility and extension of

The associate editor coordinating the review of this manuscript and approving it for publication was Yiming Huo.

neuromorphic systems are highly dependent on the performance functionality of the designed neuron and synapse circuits [4]. Therefore, representing compact and energy-efficient neurons and synapses is crucial for developing high-performance on-chip neural systems. Over the past decade, numerous synapse and neuron circuits have been demonstrated in the literature using different platforms and design scenarios [5], [6], [7], [8]. One method to realize neurons and synapses is to develop emerging neural and synaptic devices, such as ferroelectric field-effect transistors, memristive devices, or magnetic tunnel junctions [9], [10], [11]. Scientists have demonstrated that using these emerging devices can remarkably improve the functionality and performance of neuromorphic systems. However, since the fabrication technology for these unique devices is still premature and cannot be used as a commercial technology, their usage as an industrial platform might be limited. Another way is to employ the standard manufacturing process of complementary metal-oxide-semiconductor (CMOS) technology. Due to the large-scale integration of CMOS technology, demonstrating neuromorphic circuits and systems based on this technology is a more efficient way to mass production [12].

As the device dimension of integrated circuits and systems shrinks down to sub-50nm feature size, conventional planar CMOS transistors cannot preserve their unbeatable functionality, and replacement or supplement solutions are required to remove this scaling barrier [13], [14]. One of the potential solutions is to employ non-silicon emerging nanomaterials such as carbon nanotubes, graphene, or other contemporary materials [15]. Material scientists have demonstrated that these non-silicon-based transistors, such as carbon nanotubes, black phosphorus, and transition metal dichalcogenides (TMD), can present better electrical functionality, such as power consumption compared to the silicon-based counterparts [16], [17], [18]. However, the application of non-silicon alternatives has totally faded for real-life applications such as neuromorphic systems and neural networks due to the inability to fabricate these transistors at the industrial level. In this regard, despite providing better energy efficiency (at the simulation level), non-silicon solutions such as CNTFETs cannot be employed for real-life practical applications, and therefore, FinFET technology remains the sole solution for demonstrating realistic neuromorphic systems [19].

The main aim of this work is to demonstrate a novel high-performance and energy-efficient leaky integrate-and-fire (LIF) neuron and spike timing difference plasticity (STDP) circuit as the two fundamental blocks for neuromorphic systems using 7nm FinFET technology. The proposed LIF neuron circuit utilizes a Schmitt-trigger-based configuration for firing the output and has an external control voltage to tune the firing frequency rate. Consequently, the proposed neuron has been designed using 12 FinFETs and two capacitors. In designing the STDP circuit, a cardinal block for weight updating of synapses, both weight potentiation and depression, is provided in a multi-valued fashion. The proposed STDP circuit employs 6 FinFETs and 3 capacitors. The main contributions of this work are highlighted as follows:

- The proposed LIF neuron and STDP circuits are designed using the 7nm FinFET technology as a currently available commercial manufacturing process
- The proposed LIF neuron circuit employed 12 FinFETs, which provides 34% area saving compared to the state-of-the-art works.
- The proposed STDP circuit indicates 60% area saving using 6 FinFETs compared to its counterparts
- The proposed LIF Neuron and STDP circuits demonstrate 57% power and 41% energy savings compared to their counterparts
- The proposed LIF neuron has a tunable firing rate (5MHz-330MHz) using an external control voltage providing a wide frequency range
- The proposed circuits demonstrate robust and durable designs against process variations

Following this introductory section, Section II provides the research preliminaries, including the 7nm FinFET technology and previous related works. The proposed LIF neuron and STDP circuit design details are provided in Section III. Comprehensive simulations are carried out in Section IV, and the main results are concluded in Section V.

II. RESEARCH BACKGROUND

A. 7NM FINFET TECHNOLOGY

CMOS transistors were the only commercially applicable technology for many decades. As the technology footprint shrinks to below 22-nm feature size, several harmful silicon short channel effects such as leakage current increment, mobility degradation, reduced drain-to-source on-resistance, and drain-induced barrier lowering emerged that hinders further device scaling [20]. In the past years, FinFET technology is the spotlight of IC designers owing to their higher I_{ON}/I_{OFF} current ratio, improved subthreshold swing, and ease of batch fabrication using standard manufacturing processes [21].

A 3D schematic view of a tri-gate FinFET is illustrated in Fig. 1. In FinFETs, a thick insulator such as SiO_2 is used as the substrate. Then, the fabrication process follows by developing silicon fins over the substrate through the lithography and etching process. After the formation of fins, a high-k dielectric layer such as HfO_2 surrounds the fins to provide a good gate electrostatic controllability. Finally, the gate metal is deposited over the gate dielectric. More details regarding the fabrication process of FinFETs can be found in [22] and [23].

The drain current of a FinFET device can be given by [23]:

$$I_D = \beta N_{FIN} \frac{2H_{FIN} + T_{FIN}}{L_g} (V_{GS} - V_{TH})^{\alpha} \quad (1)$$

where V_{GS} is the external gate-source bias voltage, V_{TH} is the device threshold voltage, T_{FIN} and H_{FIN} are the fins'

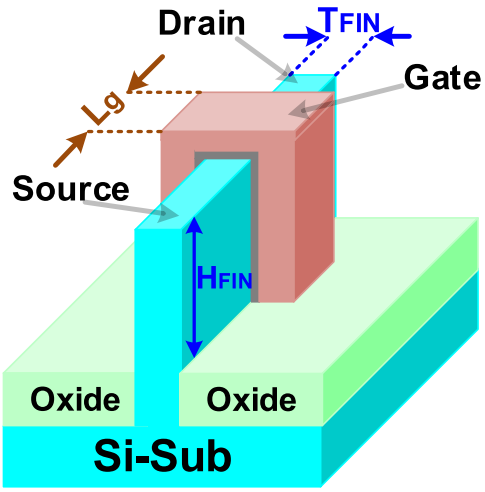


FIGURE 1. The 3D view of a tri-gate FinFET device.

TABLE 1. Some of the fundamental parameters of 7nm FinFET technology [24], [25].

Device Parameter	Value
Fin thickness (T_{FIN})	6.5nm
Fin height (H_{FIN})	32nm
Physical gate length (L_g)	21nm
Equivalent oxide thickness (EoT)	1.5nm
Fin pitch (P_{FIN})	27nm
Body doping (N_{body})	10^{16}cm^{-3}
Doping of source and drain region (N_{SD})	2×10^{20}cm^{-3}
Mobility of n-type device	250cm^2/V.s
Mobility of p-type device	210cm^2/V.s

thickness and height respectively, L_g is the gate length, N_{FIN} is the number of fins, α is the velocity saturation index, and β is a fitting constant parameter.

Table 1 shows the fundamental parameters of the utilized FinFET technology. In this work, 7nm FinFET technology is used for circuit simulations in the Synopsys HSPICE environment [24]. More details about the utilized model can be found in [25].

B. PREVIOUS RELATED WORKS

Based on the design and hardware requirements, various STDP and LIF neuron circuits have been proposed in the literature during the past decades [26], [27], [28], [29]. Most of these works suffer from two cardinal issues: (1) complicated firing and learning behavior of the designed circuits, and (2) high power, energy dissipation, and area budget that hampers the practical implementation of neuromorphic chips. Utilizing nonvolatile emerging materials such as memristors or ferroelectric FETs can remarkably alleviate the circuit design complexity and provide more energy savings [30], [31]. However, fabricating these devices using commercial fabrication methods is demanding and not efficient for batch fabrication.

In 2012, Albrecht et al. demonstrated energy-efficient neuron and synapse circuits using the 90nm standard CMOS process. To realize the designed neuron and synapse, they employed a transconductance amplifier. The designed neuron and STDP circuits used 20 and 105 transistors with 5 capacitors for a correct operation which leads to 0.4pJ energy per spike consumption [32].

By using a resistive synapse configuration, Wu et al. proposed a spiking neuron for brain-inspired neural networks in 180nm CMOS technology. These designs, which employed more than 100 transistors, represent 9.3pJ/spike energy consumption and occupy 0.01mm^2 die area [33]. Aamir et al. used a switched-capacitor structure and demonstrated an LIF neuron for large-scale neuromorphic systems in 2016. The designed circuit was implemented in 65nm CMOS technology and used 20T transconductance amplifier and large capacitors for operation. This structure consumes 138μW power at a 3pF load capacitor [34].

By leveraging memristor devices and eliminating the need for transconductance amplifiers, in 2018 Shamsi et al. designed a CMOS neuron and memristor crossbar arrays in 90 CMOS technology [35]. This work utilizes a winner-take-all structure for realizing the LIF neuron circuit and consumes 4.3pJ/spike energy with 182pW static power consumption. In 2017, Sahoo et al. employed a sub-1V ring oscillator as a leaky integrator to design LIF neuron circuit [36]. This structure operates at a 1MHz firing rate with more than 50 transistors in the 65nm standard CMOS process.

In 2021, by offering a spike frequency adaptation mechanism, Zare et al. proposed an energy-efficient LIF neuron model using TSMC 130nm CMOS technology [37]. The firing frequency of the designed LIF neuron circuit could be calibrated from 0.15MHz up to 0.5MHz with a 22μm^2 layout area.

Akabari et al. designed a 0.3V conductance-based silicon neuron in 180nm CMOS process. This structure consumes 135fJ/spike energy with an area of 993μm^2 [38]. Joo et al. employ a novel design technique to propose an energy-efficient synapse and LIF neuron circuit using STDP on-chip learning in 2022 [39]. The proposed STDP and LIF neuron circuits consume 4.6fJ/spike and 9.5fJ/spike energy in the 28nm CMOS process. Despite providing 94% and 43% improvements in energy and area compared to the previous design, these designs require bias circuits and comparators.

In 2023, Chen et al. demonstrated a power-efficient synapse and neuron circuit for analog spiking neural network applications [40]. The designed neural structure was fabricated in TSMC 65nm CMOS technology with 127μm^2 and 231μm^2 chip area. With a firing rate of 230MHz, the neuron circuit consumes 4pJ/spike energy.

Some of the previous works employed nonvolatile resistive memories such as memristors to establish high-performance neuromorphic systems. Dong, et al. demonstrated a compact machine learning architecture with a spintronic memristor-based synapse circuit [41]. The proposed synapse circuit showed a bimodal behavior because of the threshold characteristic of the memristor device. By fabricating a meta-oxide-based memristor, Dong et al. proposed a flexible

neuromorphic computing system with a hardware-friendly training approach [42]. The proposed hardware demonstrated a good trade-off between accuracy and time dissipation. In 2023, Ji et al. proposed an interactive in-memory computing system for video sentiment application [43]. The circuit-level implementation of the proposed system had been done using budget-efficient carbon-based memristors. More memristor-based related neuromorphic designs can be found in [44], [45], [46], and [47].

More synapse and LIF neuron circuits using different design scenarios can be found in [48], [49], and [50]. In this work, by proposing a novel design method, we propose a compact and energy-efficient STDP and LIF neuron circuit using 7nm FinFET technology. In the following, the design procedure of the proposed STDP and LIF neuron circuits is provided in detail.

III. PROPOSED DESIGNS

In realizing neuromorphic systems, two cardinal blocks should be designed for efficient hardware: neurons and synapses. The performance of spiking neural networks and their on-chip neuromorphic implementation is highly dependent on the performance of these two blocks. LIF neurons and STDP-based synapses are the most frequently used structures for hardware implementation of neuromorphic systems [27], [28], [29]. During the past decades, numerous synapse and LIF neuron circuits have been proposed in the literature using different platforms and design techniques and employing emerging neural and synaptic devices, like ferroelectric field-effect transistors, memristive devices, graphene, or magnetic tunnel junctions [5], [6], [7], [8], [9], [10], [11], [15]. These devices can improve the functionality and performance of neuromorphic systems. However, the main research gap is the inability to fabricate using these particular devices, because of the fact that they are still premature and cannot be used as an industrial solution. Due to the large-scale integration of FinFET technology as the current manufacturing platform, demonstrating neuromorphic synapses and neurons based on this technology is of high interest and can lead to efficient implementations of real-world neuromorphic applications [12]. Hence, the main motivation of this work is to design and demonstrate STDP and LIF neuron circuits using FinFET technology.

A. THE PROPOSED STDP CIRCUIT

There are numerous methods for updating the weight of synapses between neurons. Among various candidates, STDP, a type of Hebbian learning with temporal asymmetry, is a highly compatible learning method with SNNs [51]. Moreover, it has been demonstrated in the literature that the human brain utilizes this method for synaptic plasticity [52]. The general illustration of STDP learning is shown in Fig. 2. According to Fig. 2, the STDP learning is based on the timing difference between the pre (V_{PRE}) and post (V_{POST}) synaptic spikes. When V_{PRE} arrives sooner than the V_{POST} the synaptic weight would be increased (potentiation).

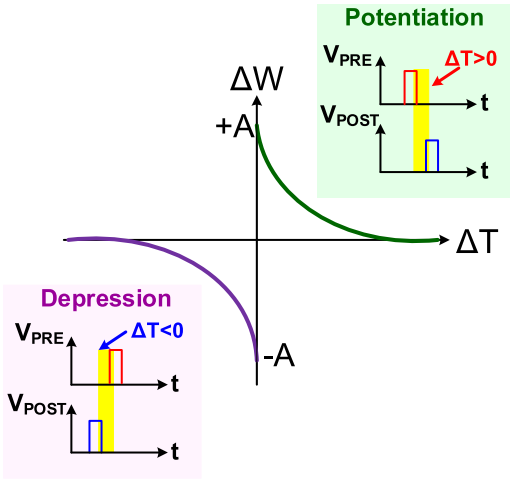


FIGURE 2. The weight potentiation and depression illustration of STDP learning [53], [54].

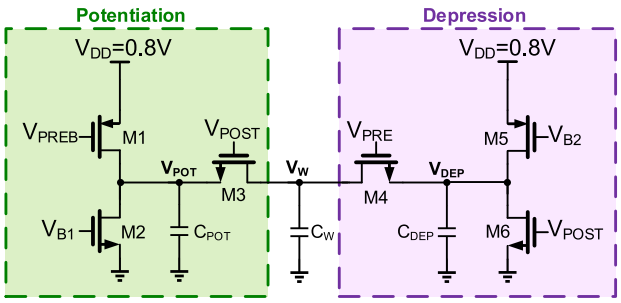


FIGURE 3. The proposed STDP circuit using FinFET technology.

Otherwise, the V_{POST} activates before V_{PRE} and reduces the synaptic weight (depression process). The strength of the potentiation and depression processes depends on the timing difference. More details regarding the STDP learning of SNNs can be found in [53] and [54].

Fig. 3 illustrates the proposed STDP circuit using FinFET technology. As can be seen in this figure, when V_{PRE} is activated, the inverted signal (V_{PREB}) turns on the M1 and starts to charge the C_{POT} capacitor. After the V_{PRE} becomes 0V, the C_{POT} capacitors start to gradually discharge to the ground through the M2 transistor (which acts as a resistor). Consequently, if V_{POST} becomes activated during the discharging period, the remaining voltage will charge the out-node capacitor (C_W). This potentiation process depends on the timing of the activation of V_{POST}. If V_{POST} activates sooner, the more charging voltage is delivered to the C_W.

The depression process is similar to the potentiation. When the V_{POST} turns on before V_{PRE}, the M6 transistor starts to conduct and reduce the voltage of V_{DEP} node to the ground. Meanwhile, if V_{PRE} is activated after V_{POST}, the voltage of the out-node capacitor (C_W) decays to the V_{DEP} voltage. The depression process also depends on the timing difference (ΔT) between the V_{POST} and V_{PRE}. Lower ΔT leads to more discharging of the V_W voltage.

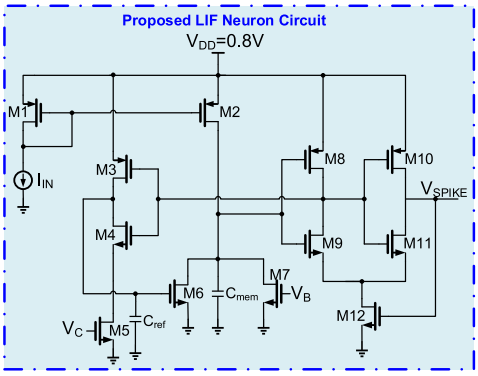


FIGURE 4. The proposed LIF neuron circuit in FinFET technology.

B. THE PROPOSED LIF NEURON CIRCUIT

In designing SNNs, LIF neurons are the most highly applicable models for implementing compact and energy-efficient neuromorphic hardware. During the past years, various LIF neuron circuits using different design methods have been proposed in the literature. Most of these works suffer from high design complexity, a significant number of transistors (due to using transconductance amplifiers), and high energy and area budget [33], [34], [35], [36]. In this section, we demonstrate a compact structure LIF neuron circuit in FinFET technology.

Fig. 4 portrays the proposed LIF neuron circuit. Based on Fig. 4, the input synaptic current (I_{IN}) delivers to the membrane capacitor through the current mirror (M1 and M2). The C_{mem} and M7 act as a leaky integrator. The M8-M10 constructs a Schmitt trigger to fire the output spike. When the C_{mem} rises beyond the upper threshold point of the Schmitt trigger, the out node (V_{SPIKE}) fires. Afterward, the M12 transistors become activated and increase the gate voltage of M3 and M4. Consequently, by charging the C_{ref} capacitor, the M6 transistor turns on the discharge the C_{mem} capacitor. Therefore, the output voltage becomes zero again, and this process will continue to generate the next spike. It is worth poting out that by changing the V_C voltage, the refractory time can be harnessed, and therefore tunable firing rate is achievable. It can be concluded that the LIF neuron has been implemented by using 12 FinFETs and two capacitors without using any transconductance amplifier.

It is worth noting that the proposed LIF neuron and STDP circuit are based on FinFET technology, and no nonvolatile emerging components have been used (such as memristors and ferroelectric capacitors). Moreover, since the utilized capacitors have sub-50fF values, they can be easily scaled using MOS-CAP structures in different technologies. Therefore, the proposed structure can be scaled with large-scale multi-layer neural networks without facing any performance failure. In neuromorphic circuits, long-term stability is a pivotal concern that needs to be investigated at the weight storage synapses. This issue becomes critical when nonvolatile components such as memristors and ferroelectric transistors (FeFETs) are employed for weight backup and restore operation (where the set-reset resistance

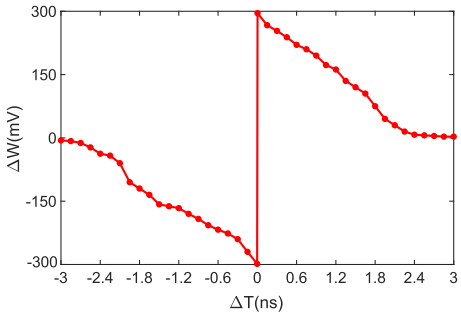


FIGURE 5. The variation of the weight voltage (ΔW) using the proposed STDP circuit.

in memristors and FeFETs should be considered for long-term stability) [18]. However, in silicon-based neuromorphic circuits, the weight storage is performed statically without using any nonvolatile elements and no stability concerns would raise at weight storage and retention stages [39]. In this regard, FinFET-based neural networks and neuromorphic systems are stable structures during the operation over period of use.

IV. PERFORMANCE EVALUATION OF THE PROPOSED DESIGNS

The weight-updating simulation results of the proposed STDP circuit are shown in Fig. 5. In the obtained results, the timing difference between the post- and pre-synaptic spikes is considered as $\Delta t=t_{POST}-t_{PRE}$ and ΔW is the variation of the synaptic weight. After interpreting the results, it can be inferred that the proposed STDP circuit can update the synaptic weight in an applicable wide range (37.5% maximum weight variations for V_{DD}=800mV). It is worth pointing out that the slope of the potentiation and depression in the obtained STDP curve can be calibrated by changing the V_{B1} and V_{B2} bias voltages.

The transient response of the proposed STDP circuit for weight potentiation and depression is shown in Fig. 6a. When V_{PRE} comes sooner than V_{POST} the out node capacitor starts to charge based on the V_{POT} voltage (Fig. 6). If V_{POST} activates before V_{PRE} (Fig. 6b), the C_W capacitor discharge to the related V_{DEP} voltage. As indicated, the proposed STDP circuit provides a wide range of weight potentiation and depression using only 6 FinFETs and 3 capacitors. Therefore, it can be leveraged for on-chip learning of SNNs.

Fig. 7 illustrates the transient response of the proposed LIF neuron circuit. It can be seen that the out-node voltage starts to leaky charge through the membrane capacitor. After the input voltage of the membrane capacitor transcends the upper threshold point, the LIF neuron starts firing and produces the related output spike. It is noteworthy that the firing rate and refractory period can be controlled by the V_C and C_{ref} capacitor.

To obtain the firing frequency range of the proposed LIF neuron circuit, both V_C and V_B (Fig. 4) have changed and represents the simulation results in a 3D plot. Fig. 8 shows the 3D plot of the firing frequency of the proposed LIF neuron

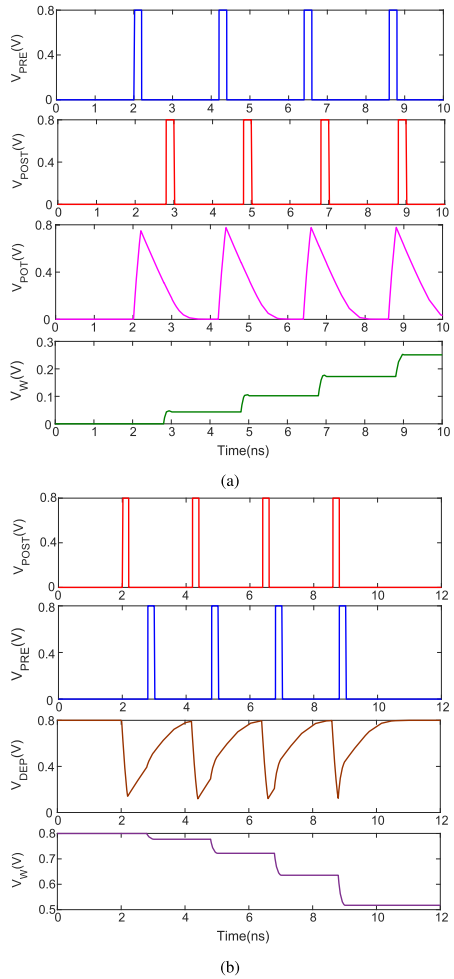


FIGURE 6. The transient response of the proposed STDP circuit. (a) the weight potentiation and (b) depression process.

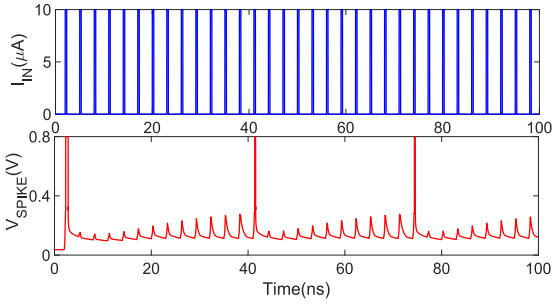


FIGURE 7. The transient response of the proposed LIF neuron circuit.

circuit. It can be seen that V_C voltage has a major impact on the firing rate of the LIF neuron circuit. By changing the control voltage within $0.2V<V_C<0.4V$, the firing frequency can be calibrated from 5MHz to 330MHz.

In designing nanoscale integrated circuits and systems, physical parameters variation of the utilized technology might have a major impact on the performance functionality. In FinFET-based circuits and systems, variations in fin thickness (t_{FIN}), height (H_{FIN}), oxide thickness (t_{ox}) are the main source of variations that can degrade the performance

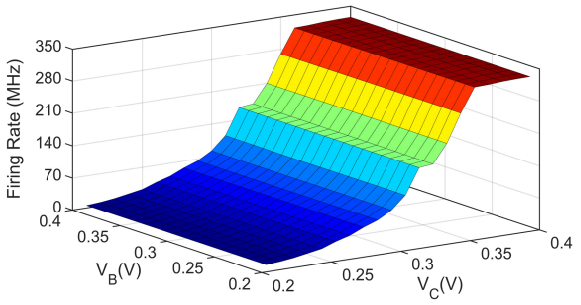


FIGURE 8. The firing rate variations of the proposed LIF neuron circuit.

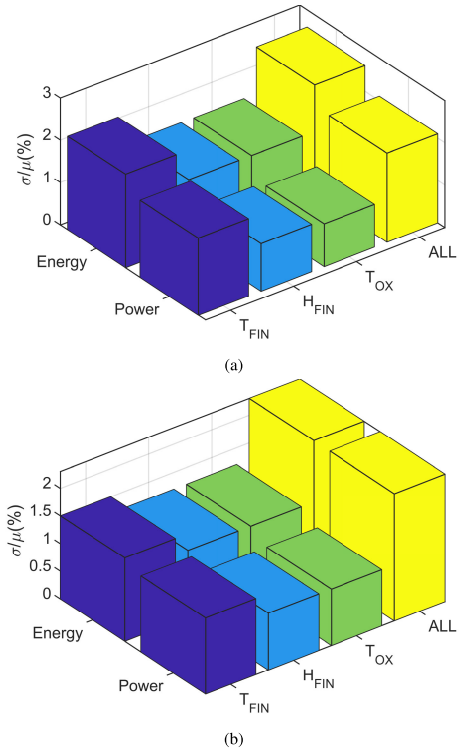


FIGURE 9. The impact of process variations on the energy and power consumption of the proposed (a) STDP and (b) LIF neuron circuit.

of the designed circuits and systems after fabrication [55]. In this regard, 5000 runs of Monte Carlo simulations have been conducted to assess the impact of process variations. Moreover, ±10% variations in the FinFET parameters with a Gaussian distribution have been considered at the 3 sigma level.

The Monte Carlo simulation results of the proposed STDP and LIF neuron circuits are presented in Fig. 9. As depicted, despite experiencing significant physical parameter variations, the proposed STDP and LIF neuron circuits are robust and have not shown more than 3% variations.

A performance comparison between the electrical metrics of the proposed STDP and LIF neuron circuits is shown in Table. 2 and Table. 3. All the compared works have been redesigned based on the utilized 7nm FinFET technology to provide a meaningful comparison. Based on the comparison results between different STDP circuits (Table. 2), it can be

TABLE 2. A performance comparison between the electrical metrics of the proposed STDP circuit and some of the previous related designs.

	Proposed	[39]	[56]	[57]	[58]
Supply Voltage (mV)	800	800	800	800	800
Transistor count	6	16	13	15	12
Capacitor count	3	1	5	4	3
power (μW)	1.2	3.9	1.8	1.9	3.3
Energy (fJ)	15.8	34.1	21.5	29.5	27.8
Area (μm^2)	51.9	55.3	265.4	248.3	197.3
Technology	7nm FinFET	7nm FinFET	7nm FinFET	7nm FinFET	7nm FinFET

TABLE 3. A performance comparison between the proposed LIF neuron circuit and previous related designs.

	Proposed	[35]	[37]	[39]	[40]	[48]	[49]
Supply Voltage (mV)	800	800	800	800	800	800	800
Transistor count	12	9	14	16	13	11	9
Capacitor count	2	1	2	1	1	1	3
power (μW)	4.8	5.1	8.9	5.6	13.1	12.8	33
Energy per spike (fJ)	27	29.3	70.1	35.1	48.7	31.3	202
Firing frequency (MHz)	5-330	10-85	160	117-860	350	950	333
Area (μm^2)	42.4	43.3	100.5	55	85	48.9	153.5
Technology	7nm FinFET	7nm FinFET	7nm FinFET	7nm FinFET	7nm FinFET	7nm FinFET	7nm FinFET

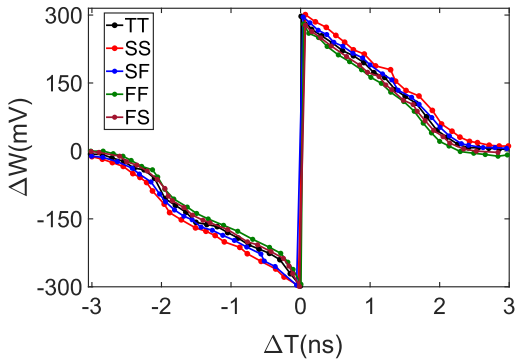


FIGURE 10. The impact of corner variations on the STDP of the proposed FinFET-based weight updating circuit.

observed that using a more compact structure provides 68%, 43%, and 60% total average improvements in power, energy, and area compared to the previous related designs. In Table. 3, the proposed LIF neuron circuit shows 46% improvements in power, 40% improvements in energy, and 34% improvements in the area compared to the other counterparts. Moreover, the proposed design can harness the firing frequency within a wide applicable range.

In designing neuromorphic circuits and systems, noise can usually affect the threshold voltage of the transistors and change the stored weight and weight updating (STDP) circuit [59], [60]. In order to assess the impact of noise on the obtained STDP curve, corner analysis is performed, considering five corner processes: (1) typical n-type typical p-type (TT), (2) fast n-type fast p-type (FF), (3) slow n-type slow p-type (SS), (4) slow n-type fast p-type (SF), and (5) fast n-type slow p-type (FS). Fig. 10 illustrates the corner simulation results for the proposed STDP curve. Based on the results, it can be seen that no failure has occurred under the five corner processes. Therefore, the proposed FinFET-based circuit is completely immune to unwanted noises and variations.

Based on the results, it can be emphasized that the proposed STDP and LIF neuron circuits are high-potential candidates to realize compact and energy-efficient on-chip neuromorphic computing systems.

V. CONCLUSION

In this work, a compact and energy-efficient LIF neuron and STDP circuit have been proposed based on 7nm FinFET technology. The proposed LIF neuron has been designed in a particular way that can calibrate the firing frequency using an external control voltage. Moreover, by offering a simple and compact structure, the multi-valued weight potentiation and depression have been performed in a wide applicable range. The simulation results demonstrate that the proposed STDP and LIF neuron circuits have shown 60% and 34% improvement in the area, respectively. Under similar conditions, the proposed STDP circuit indicates a 68% improvement in total average power consumption and a 43% improvement in energy saving compared to the other counterpart. For the proposed LIF neuron circuit, these values change to 46% for power and 40% for energy dissipation. By changing the external control voltage, the proposed LIF neuron circuit is able to tune the firing frequency in a wide range (5MHz-330MHz).

The proposed results accentuate the promising applications of the proposed STDP and LIF neuron circuit for commercialized on-chip neuromorphic computing circuits and systems without using any non-silicon emerging technology, which is not cost-effective for batch fabrication.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), South Korea.

REFERENCES

[1] S. Dutta, H. Jeong, Y. Yang, V. Cadambe, T. M. Low, and P. Grover, "Addressing unreliability in emerging devices and non-von Neumann architectures using coded computing," *Proc. IEEE*, vol. 108, no. 8, pp. 1219–1234, Aug. 2020.

[2] D. Marković, A. Mizrahi, D. Querlioz, and J. Grollier, "Physics for neuromorphic computing," *Nature Rev. Phys.*, vol. 2, no. 9, pp. 499–510, Jul. 2020.

[3] O. Krestinskaya, A. P. James, and L. O. Chua, "Neuromemristive circuits for edge computing: A review," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 31, no. 1, pp. 4–23, Jan. 2020.

[4] A. Tavanaei, M. Ghodrati, S. R. Kheradpisheh, T. Masquelier, and A. Maida, "Deep learning in spiking neural networks," *Neural Netw.*, vol. 111, pp. 47–63, Mar. 2019.

[5] M. Heidarpur, A. Ahmadi, M. Ahmadi, and M. Rahimi Azghadi, "CORDIC-SNN: On-FPGA STDP learning with Izhikevich neurons," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 7, pp. 2651–2661, Jul. 2019.

[6] S. Chakrabartty, S. Acharjee, A. Al-Shidaifat, M. Biswas, and H. Song, "Gd-doped HfO_2 memristor device, evaluation robustness by image noise cancellation and edge detection filter for neuromorphic computing," *IEEE Access*, vol. 7, pp. 157922–157932, 2019.

[7] F.-X. Liang, I.-T. Wang, and T.-H. Hou, "Progress and benchmark of spiking neuron devices and circuits," *Adv. Intell. Syst.*, vol. 3, no. 8, Aug. 2021, Art. no. 2100007.

[8] X. Yang, B. Taylor, A. Wu, Y. Chen, and L. O. Chua, "Research progress on memristor: From synapses to computing systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 5, pp. 1845–1857, May 2022.

[9] K. Tamersit, M. K. Q. Jooq, and M. H. Moaiyeri, "Computational investigation of negative capacitance coaxially gated carbon nanotube field-effect transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 1, pp. 376–384, Jan. 2021.

[10] M. R. Azghadi, C. Lammie, J. K. Eshraghian, M. Payvand, E. Donati, B. Linares-Barranco, and G. Indiveri, "Hardware implementation of deep network accelerators towards healthcare and biomedical applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1138–1159, Dec. 2020.

[11] S. N. Pagliarini, S. Bhuin, M. M. Isgenc, A. K. Biswas, and L. Pileggi, "A probabilistic synapse with strained MTJs for spiking neural networks," *IEEE Trans. Neural Netw. Learn. Syst.*, vol. 31, no. 4, pp. 1113–1123, Apr. 2020.

[12] D. Chatterjee and A. Kottantharayil, "A CMOS compatible bulk FinFET-based ultra low energy leaky integrate and fire neuron for spiking neural networks," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1301–1304, Aug. 2019.

[13] A. Franceschin, P. Andreani, F. Padovan, M. Bassi, and A. Bevilacqua, "A 19.5-GHz 28-nm class-C CMOS VCO, with a reasonably rigorous result on 1/f noise upconversion caused by short-channel effects," *IEEE J. Solid-State Circuits*, vol. 55, no. 7, pp. 1842–1853, Jul. 2020.

[14] M. K. Q. Jooq, F. Behbahani, A. Al-Shidaifat, S. R. Khan, and H. Song, "A high-performance and ultra-efficient fully programmable fuzzy membership function generator using FinFET technology for image enhancement," *AEU Int. J. Electron. Commun.*, vol. 163, May 2023, Art. no. 154598.

[15] B. Walters, M. V. Jacob, A. Amirsoleimani, and M. R. Azghadi, "A review of graphene-based memristive neuromorphic devices and circuits," *Adv. Intell. Syst.*, vol. 5, no. 10, 2023, Art. no. 2300136.

[16] M. K. Q. Jooq, M. H. Moaiyeri, and K. Tamersit, "Ultra-compact ternary logic gates based on negative capacitance carbon nanotube FETs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 6, pp. 2162–2166, Jun. 2021.

[17] N. K. Singh, M. Kumari, and M. Sahoo, "A compact short-channel analytical drain current model of asymmetric dual-gate TMD FET in subthreshold region including fringing field effects," *IEEE Access*, vol. 8, pp. 207982–207990, 2020.

[18] M. H. Moaiyeri, M. K. Q. Jooq, A. Al-Shidaifat, and H. Song, "Breaking the limits in ternary logic: An ultra-efficient auto-backup/restore non-volatile ternary flip-flop using negative capacitance CNTFET technology," *IEEE Access*, vol. 9, pp. 132641–132651, 2021.

[19] F. Sabetzadeh, M. H. Moaiyeri, and M. Ahmadinejad, "A majority-based imprecise multiplier for ultra-efficient approximate image multiplication," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 11, pp. 4200–4208, Nov. 2019.

[20] H. Ilatikhameneh, T. Ameen, B. Novakovic, Y. Tan, G. Klimeck, and R. Rahman, "Saving Moore's law down to 1 nm channels with anisotropic effective mass," *Sci. Rep.*, vol. 6, no. 1, p. 31501, Aug. 2016.

[21] M. K. Q. Jooq, F. Behbahani, and M. H. Moaiyeri, "Ultra-efficient fully programmable membership function generator based on independent double-gate FinFET technology," *Int. J. Circuit Theory Appl.*, vol. 51, no. 10, pp. 4485–4502, Oct. 2023, doi: 10.1002/cta.3663.

[22] M.-L. Chen, X. Sun, H. Liu, H. Wang, Q. Zhu, S. Wang, H. Du, B. Dong, J. Zhang, Y. Sun, S. Qiu, T. Alava, S. Liu, D.-M. Sun, and Z. Han, "A FinFET with one atomic layer channel," *Nature Commun.*, vol. 11, no. 1, p. 1205, Mar. 2020.

[23] M. K. Q. Jooq, M. Ahmadinejad, and M. H. Moaiyeri, "Ultraefficient imprecise multipliers based on innovative 4:2 approximate compressors," *Int. J. Circuit Theory Appl.*, vol. 49, no. 1, pp. 169–184, Jan. 2021.

[24] (2016). *7-nm FinFET Predictive Process Design Kit*. [Online]. Available: http://asap.asu.edu/asap

[25] L. T. Clark, V. Vashishtha, L. Shifren, A. Gujja, S. Sinha, B. Cline, C. Ramamurthy, and G. Yeric, "ASAP7: A 7-nm finFET predictive process design kit," *Microelectron. J.*, vol. 53, pp. 105–115, Jul. 2016.

[26] W. Zhou, S. Wen, Y. Liu, L. Liu, X. Liu, and L. Chen, "Forgetting memristor based STDP learning circuit for neural networks," *Neural Netw.*, vol. 158, pp. 293–304, Jan. 2023.

[27] M. Rahimi Azghadi, N. Iannella, S. F. Al-Sarawi, G. Indiveri, and D. Abbott, "Spike-based synaptic plasticity in silicon: Design, implementation, application, and challenges," *Proc. IEEE*, vol. 102, no. 5, pp. 717–737, May 2014.

[28] G. Indiveri, E. Chicca, and R. Douglas, "A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity," *IEEE Trans. Neural Netw.*, vol. 17, no. 1, pp. 211–221, Jan. 2006.

[29] J.-Q. Yang, R. Wang, Z.-P. Wang, Q.-Y. Ma, J.-Y. Mao, Y. Ren, X. Yang, Y. Zhou, and S.-T. Han, "Leaky integrate-and-fire neurons based on perovskite memristor for spiking neural networks," *Nano Energy*, vol. 74, Aug. 2020, Art. no. 104828.

[30] M. K. Q. Jooq, M. H. Moaiyeri, and K. Tamersit, "A new design paradigm for auto-nonvolatile ternary SRAMs using ferroelectric CNTFETs: From device to array architecture," *IEEE Trans. Electron Devices*, vol. 69, no. 11, pp. 6113–6120, Nov. 2022.

[31] F. Behbahani, M. K. Q. Jooq, M. H. Moaiyeri, and K. Tamersit, "Leveraging negative capacitance CNTFETs for image processing: An ultra-efficient ternary image edge detection hardware," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 12, pp. 5108–5119, Dec. 2021.

[32] J. M. Cruz-Albrecht, M. W. Yung, and N. Srinivasa, "Energy-efficient neuron, synapse and STDP integrated circuits," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 3, pp. 246–256, Jun. 2012.

[33] X. Wu, V. Saxena, K. Zhu, and S. Balagopal, "A CMOS spiking neuron for brain-inspired neural networks with resistive synapses and in situ learning," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 11, pp. 1088–1092, Nov. 2015.

[34] S. A. Aamir, P. Müller, A. Hartel, J. Schemmel, and K. Meier, "A highly tunable 65-nm CMOS LIF neuron for a large scale neuromorphic system," in *Proc. ESSCIRC Conf. 42nd Eur. Solid-State Circuits Conf.*, Sep. 2016, pp. 71–74.

[35] J. Shamsi, K. Mohammadi, and S. B. Shokouhi, "A hardware architecture for columnar-organized memory based on CMOS neuron and memristor crossbar arrays," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 12, pp. 2795–2805, Dec. 2018.

[36] B. D. Sahoo, "Ring oscillator based sub-1 V leaky integrate-and-fire neuron circuit," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.

[37] M. Zare, E. Zafarkhah, and N. S. Anzabi-Nezhad, "An area and energy efficient LIF neuron model with spike frequency adaptation mechanism," *Neurocomputing*, vol. 465, pp. 350–358, Nov. 2021.

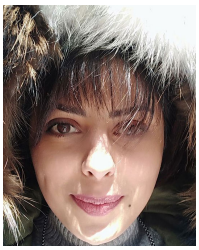
[38] M. Akbari, S. M. Hussein, T.-I. Chou, and K.-T. Tang, "A 0.3-V conductance-based silicon neuron in 0.18 μm CMOS process," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 10, pp. 3209–3213, Oct. 2021.

[39] B. Joo, J.-W. Han, and B.-S. Kong, "Energy- and area-efficient CMOS synapse and neuron for spiking neural networks with STDP learning," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 9, pp. 3632–3642, Sep. 2022.

[40] X. Chen, Z. Byambadorj, T. Yajima, H. Inoue, I. H. Inoue, and T. Iizuka, "CMOS-based area-and-power-efficient neuron and synapse circuits for time-domain analog spiking neural networks," *Appl. Phys. Lett.*, vol. 122, no. 7, Feb. 2023, Art. no. 074102.
[41] Z. Dong, C. S. Lai, Z. Zhang, D. Qi, M. Gao, and S. Duan, "Neuromorphic extreme learning machines with bimodal memristive synapses," *Neurocomputing*, vol. 453, pp. 38–49, Sep. 2021.
[42] Z. Dong, X. Ji, C. S. Lai, and D. Qi, "Design and implementation of a flexible neuromorphic computing system for affective communication via memristive circuits," *IEEE Commun. Mag.*, vol. 61, no. 1, pp. 74–80, Jan. 2023.
[43] X. Ji, Z. Dong, Y. Han, C. S. Lai, and D. Qi, "A brain-inspired hierarchical interactive in-memory computing system and its application in video sentiment analysis," *IEEE Trans. Circuits Syst. Video Technol.*, early access, May 12, 2023, doi: 10.1109/TCSVT.2023.3275708.
[44] Z. Dong, X. Ji, G. Zhou, M. Gao, and D. Qi, "Multimodal neuromorphic sensory-processing system with memristor circuits for smart home applications," *IEEE Trans. Ind. Appl.*, vol. 59, no. 1, pp. 47–58, Jan. 2023.
[45] Z. Dong, X. Ji, C. S. Lai, D. Qi, G. Zhou, and L. L. Lai, "Memristor-based hierarchical attention network for multimodal affective computing in mental health monitoring," *IEEE Consum. Electron. Mag.*, vol. 12, no. 4, pp. 94–106, Jul. 2022.
[46] X. Ji, C. S. Lai, G. Zhou, Z. Dong, D. Qi, and L. L. Lai, "A flexible memristor model with electronic resistive switching memory behavior and its application in spiking neural network," *IEEE Trans. Nanobiosci.*, vol. 22, no. 1, pp. 52–62, Jan. 2023.
[47] X. Ji, D. Qi, Z. Dong, C. S. Lai, G. Zhou, and X. Hu, "TSSM: Three-state switchable memristor model based on Ag/TiOx nanobelt/Ti configuration," *Int. J. Bifurcation Chaos*, vol. 31, no. 7, Jun. 2021, Art. no. 2130020.
[48] H. Zheng, K. J. Bai, and Y. Yi, "Enabling a new methodology of neural coding: Multiplexing temporal encoding in neuromorphic computing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 31, no. 3, pp. 331–342, Mar. 2023.
[49] H. Eslahi, T. J. Hamilton, and S. Khandelwal, "Compact and energy efficient neuron with tunable spiking frequency in 22-nm FDSOI," *IEEE Trans. Nanotechnol.*, vol. 21, pp. 189–195, 2022.
[50] G. Srinivasan, A. Sengupta, and K. Roy, "Magnetic tunnel junction based long-term short-term stochastic synapse for a spiking neural network with on-chip STDP learning," *Sci. Rep.*, vol. 6, no. 1, Jul. 2016, Art. no. 29545.
[51] N. Rathi, P. Panda, and K. Roy, "STDP-based pruning of connections and weight quantization in spiking neural networks for energy-efficient recognition," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 38, no. 4, pp. 668–677, Apr. 2019.
[52] H. Fang, Y. Zeng, and F. Zhao, "Brain inspired sequences production by spiking neural networks with reward-modulated STDP," *Frontiers Comput. Neurosci.*, vol. 15, Feb. 2021, Art. no. 612041.
[53] N. Caporale and Y. Dan, "Spike timing-dependent plasticity: A Hebbian learning rule," *Annu. Rev. Neurosci.*, vol. 31, pp. 25–46, Jul. 2008.
[54] C. Sun, H. Sun, J. Xu, J. Han, X. Wang, X. Wang, Q. Chen, Y. Fu, and L. Li, "An energy efficient STDP-based SNN architecture with on-chip learning," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 69, no. 12, pp. 5147–5158, Dec. 2022.
[55] Z. Zhang, X. Jiang, R. Wang, S. Guo, Y. Wang, and R. Huang, "Extraction of process variation parameters in FinFET technology based on compact modeling and characterization," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 847–854, Mar. 2018.
[56] S. A. Bamford, A. F. Murray, and D. J. Willshaw, "Spike-timing-dependent plasticity with weight dependence evoked from physical constraints," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 385–398, Aug. 2012.
[57] A. W. Smith, L. J. McDaid, and S. Hall, "A compact spike-timing-dependent-plasticity circuit for floating gate weight implementation," *Neurocomputing*, vol. 124, pp. 210–217, Jan. 2014.
[58] S. Moriya, T. Kato, D. Oguchi, H. Yamamoto, S. Sato, Y. Yuminaka, Y. Horio, and J. Madrenas, "Analog-circuit implementation of multiplicative spike-timing-dependent plasticity with linear decay," *Nonlinear Theory Appl. IEICE*, vol. 12, no. 4, pp. 685–694, 2021.
[59] M. Rahimi Azghadi, S. Al-Sarawi, D. Abbott, and N. Iannella, "A neuromorphic VLSI design for spike timing and rate based synaptic plasticity," *Neural Netw.*, vol. 45, pp. 70–82, Sep. 2013.
[60] M. R. Azghadi, N. Iannella, S. Al-Sarawi, and D. Abbott, "Tunable low energy, compact and high performance neuromorphic circuit for spike-based synaptic plasticity," *PLoS ONE*, vol. 9, no. 2, Feb. 2014, Art. no. e88326.

MOHAMMAD KHALEQI QALEH JOOQ received the Ph.D. degree in electrical engineering from Lorestan University, Khorramabad, Iran. He is currently a Postdoctoral Research Fellow with the Nano Circuit Design Laboratory, Inje University, South Korea. His current research interests include neuromorphic circuits, carbon nanotube electronics, VLSI design, nanoscale device modeling, ferroelectric devices, emerging device beyond CMOS technology, approximate computing, and fuzzy logic.

MOSTAFA RAHIMI AZGHADI (Senior Member, IEEE) received the Ph.D. degree in electronics from Adelaide University, Australia. He is currently an Associate Professor with the College of Science and Engineering, James Cook University, Australia, where he researches low-power and high-performance neuromorphic accelerators for neural-inspired and deep-learning networks. He has co-raised over U.S. $11 M in research funding from national and international resources. He received the Doctoral Research Medal and the University Alumni Medal from Adelaide University. He is a recognized international scientist and a leader. Since 2020, he has been in the top 2% of worldwide highly-cited EEE researchers. He is the Chair of the IEEE Northern Australia Section and a TC Member of the Neural Systems and Applications of the Circuit and System Society. He is an Associate Editor of *Frontiers in Neuromorphic Engineering* and IEEE Access.



FERESHTEH BEHBAHANI received the M.Sc. degree in electrical engineering from Lorestan University, Khorramabad, Iran. She is currently pursuing the Ph.D. degree in electrical engineering with Shahed University, Tehran, Iran. Her current research interests include image processing, neuromorphic computing, VLSI circuit design, neural networks, and neuromorphic computing.

ALAADDIN AL-SHIDAIFAT received the B.S. degree in software engineering from Al-Hussein Bin Talal University, Jordan, in 2011, the M.Eng. degree in computer engineering from Inje University, South Korea, in 2015, and the Ph.D. degree from the Department of Nanoscience and Engineering, Inje University. Currently, he is a Research Professor with the Nanoscience and Engineering Department, Inje University. He is also with the Nano Circuit Design Laboratory (NCDL). His current research interests include medical image processing, computer vision, integrated circuits, computational sensors, smart structures, and neuromorphic applications.

HANJUNG SONG was born in South Korea. He received the B.S., M.S., and Ph.D. degrees in electronics engineering from Hanyang University, South Korea, in 1986, 1988, and 2000, respectively. He joined the Nano Design Circuit Laboratory, Inje University, South Korea, in 2004, where he is currently the Head and a Professor with the Department of Nanoscience Engineering. He has published several research articles in refereed international journals. He is carrying out three sponsored research projects as the Principal Investigator. His current research interests include power IC circuit design, the analog VLSI design of silicon neuron systems and chaotic circuits, semiconductor device modeling, and reliability.