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Modeling Integrated Antennas and Unisolated High-Power Amplifiers in Infinite Scanning Arrays

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***Abstract* — This paper presents a model of active-integrated power amplifiers and antennas in a scanning array environment. The model links together load-pull data and unit-cell antenna simulations through a synthesized power combining and matching network to determine the active load reflection seen by the individual transistors. From this an estimate of the overall power-added efficiency, interconnect losses and radiated output power is calculated for a complete scan range at a given operating frequency. The model is intended to provide a fast, first-order indication of the most suitable technology choice and design strategy for a given operating frequency and transmit power requirement.**

***Keywords* — Antennas, power amplifiers, power combining, direct matching, phased arrays.**

I. Introduction

The limited bandwidth availability in the radio frequency (RF) spectrum pushes developments in wireless communication and sensing applications towards the millimeter-wave (mm-wave) band between 30 and 300 GHz. For example, the fifth generation of mobile communication (5G) uses sections of the Ka-band, and automotive radar has moved from 24 GHz to W-band operating frequencies. A trend can be seen towards developments in the D-band beyond 100 GHz, where even wider bandwidths and smaller device sizes can be achieved [1].

Active beamforming arrays show promise for a wide range of mm-wave applications, enabling efficient use of radiated power using a steerable beam to track individual mobile users, satellites, or radar targets to name a few examples. However, the half-wavelength element spacing for wide-scanning arrays leads to tight area budgets for the electronics. Moreover, material losses increase with frequency and the achievable performance of power amplifiers (PAs) degrades [2]. These factors combined could result in high levels of thermal dissipation, a major challenge that can also be recognised in high-power applications at lower frequencies, leading to a demand for efficient PAs, antennas and interconnects.

The pursuit of low losses and limited area budget can lead to highly integrated designs, with electronics and radiating elements closely combined in the same package or even on the same chip. At the cost of modularity, removing lossy interconnects and isolating networks can improve efficiency. Since in this case a conventional 50 Ω interface is no longer needed, a single matching network or a direct match between PA and antenna as illustrated in Fig. 1 could reduce size and losses even further as demonstrated in earlier works [3].

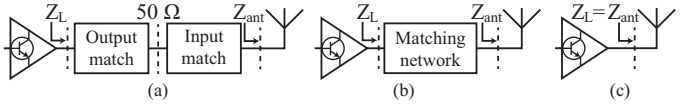

Fig. 1. Schematics of (a) conventional matching with a 50 Ω interface, (b) single matching network and (c) direct matching between PA and antenna [3].

An overview of co-designed low-noise amplifiers (LNAs) and antennas in [4] shows the potential for gain increase and noise reduction compared to 50 Ω-matched references. In [3] an overview is presented of several co-design strategies to integrate active transmitting antennas with PAs. The presented strategies and implementations vary widely, and examples of co-designed scanning array elements, particularly at mm-wave, are limited in open literature [5]. Hence, the aim of this research is to derive generalized co-design strategies for active integrated array antennas (AIAAs).

A first step towards this goal is to explore the design parameter space, including semiconductor technology choice, transistor design, number of transistors, antenna type and matching strategy, and their respective impacts on performance. For this purpose, a computational model has been constructed that combines antenna and transistor simulation data for fast assessment of power output and efficiency in an infinite scanning array as a function of such parameters.

II. HPA-Integrated Array Antennas

Transistor output power and efficiency are dependent on the load impedance Z_L as presented by the network at the transistor drain interface, shown in Fig. 1. The optimum $Z_{L,opt}$ tends to decrease for increasing power requirements, as the output voltage is limited by the semiconductor material breakdown and peak output current must be increased. In the ideal scenario of Fig. 1c this optimum load should equal the antenna impedance Z_{ant}, although practically an interconnect will exist between the antenna and drain.

The definition of high-power amplifier (HPA), as used in the title of this paper, can vary greatly between applications and operating frequencies. At millimeter-wave, a single watt of transmit power can be considered high-power, whereas hundreds of watts per element is not unheard of in sub-10 GHz

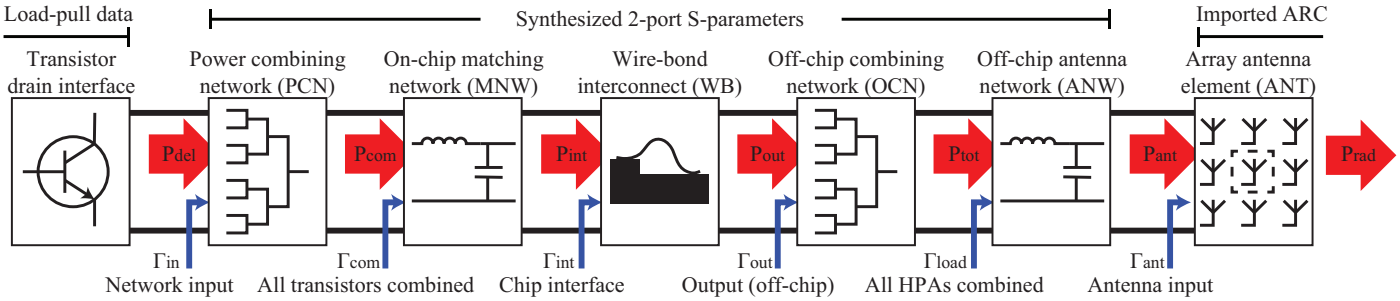

Fig. 2. Schematic overview of the model, with power flows and input reflections depicted at each interface.

radar arrays. In this work the term HPA is used when a single transistor pushed into compression is insufficient and the power of multiple transistors is combined [6]. This combiner will also contribute to an impedance transformation, increasing the antenna impedance Z_{ant} as seen from the drain.

Both Z_{ant} and Z_L vary with frequency, generally with opposing rotations on the Smith chart making direct broadband matching a challenge. Moreover, as the active antenna impedance in a scanning array changes with scan angle, a directly connected PA may lead to significant variations in delivered power and efficiency within a given scan range. A single-impedance port-termination in a circuit simulator may not provide sufficient insight on expected performance across frequency and scan range. For this reason a model was constructed that can provide fast first-order assessments of transistor performance over the full antenna scan range.

III. Model Overview

The HPA-AIAA model, illustrated in Fig. 2, is implemented in MATLAB and can be divided into three functional parts: the transistor model consisting of load-pull data, the antenna model providing the active reflection coefficient (ARC), and cascaded scattering (S)-parameters of the combiner, matching and interconnect networks. This section describes these model parts separately, and the combination of their results.

A. Transistor Load-Pull Data

The most accurate method to obtain load-pull data without performing measurements on transistor samples is through the process design kit (PDK) provided by the manufacturer [6]. The power-added efficiency (PAE) and delivered power P_{del} data at a single frequency can be generated using circuit simulator software, such as Keysight PathWays Advanced Design System (ADS), by performing a parametric sweep over a series of load reflections. This data is then imported into MATLAB, where a look-up table is generated and interpolated. All examples in this paper are based on the 0.15 μm Gallium Nitride (GaN) process from United Monolithic Semiconductors (UMS), and four 75 μm-wide gate fingers [7].

When a PDK is inaccessible, for example during an exploratory design phase where the technology is yet unspecified, an analytical transistor model based on [8] could be employed. With estimates of current-voltage (IV)-characteristics and parasitics based on published designs, the PAE and P_{del} load-pull can be calculated for a range of frequencies at once. This would also allow transistor design variations, such as gate finger count and width, to be explored without exporting a new result set from ADS each time.

B. Array Antenna Element

The large variety of antenna types and high degree of design freedom limits the usefulness of simple analytical expressions to obtain the ARC data of an element in a scanning array. Instead, the element is modeled in an infinite array environment using a full-wave solver such as Dassault Systèmes CST Microwave Studio (CST MWS). A parameter sweep of a range of scan angles θ_0 and ϕ_0 results in complex ARC data $\Gamma_{ant}(\theta_0, \phi_0)$ that is exported to MATLAB.

As an example, a wide-scanning 50 Ω-matched probe-fed stacked-patch array antenna based on [9] was simulated at 30 GHz. As shown in Fig. 3, interpolation of the sampled data allows the model to calculate results for any scan angle within the scan range swept in the full-wave solver.

The assumption of an infinite array, where identical operating conditions are considered for all elements and HPAs, holds only for elements in large-scale arrays. An expansion of the model to support finite arrays is planned.

C. Network Models

Fig. 2, shows a series of components including power combining networks (PCNs), matching networks (MNWs) and a wire-bond (WB). Each component is modeled separately, and

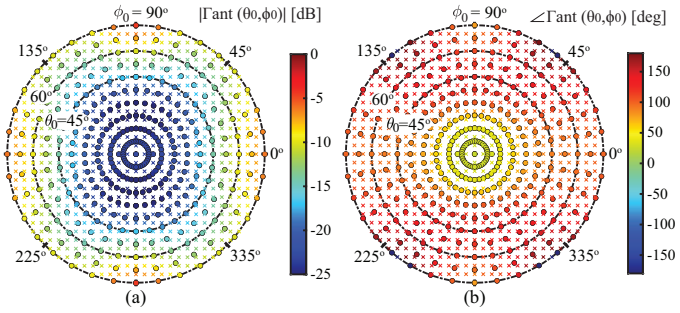

Fig. 3. Simulated (o) and interpolated (x) active reflection coefficient magnitude (a) and phase (b) of a 50 Ω-matched stacked-patch antenna in an infinite array for sampled scan angles within 75° from broadside.

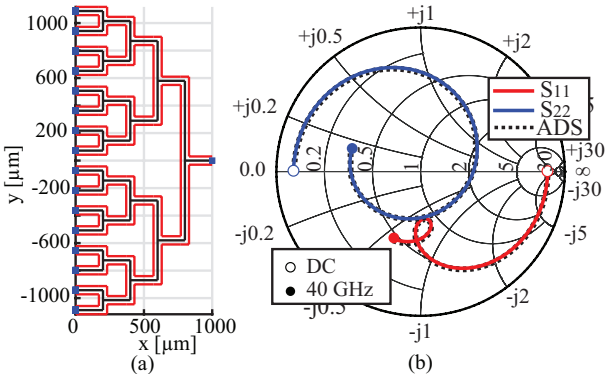

Fig. 4. (a): Schematic of a synthesized 16:1 combiner network. (b): Calculated active S_{11} and S_{22} results, compared against ADS simulations. Port 1 denotes an individual transistor drain interface, port 2 the common output of the PCN.

expressed as two-port S-parameters. Using analysis methods from [10], the Γ at any interface can be transformed to Γ_{in} at the transistor drain reference and the power at each interface can be determined.

1) *Power Combining Network Synthesis*

Given a transistor spacing d_t, widths per line section W, and displacement between combiner stages L_x, a microstrip-based PCN is synthesized entirely within MATLAB. The number of transistors N_T is limited to 2^n ($n \in \mathbb{N}$), to assume ideal symmetry. The $16:1$ combiner network shown in Fig. 4 was synthesized with the following inputs: $W = 60$ μm, $d_t = 145$ μm and $L_x = 200$ μm. These values have been applied for all examples in this paper. The limited number of parameters still allows for tuning of length and impedance of individual line segments, whilst enabling faster set-up and adjustment than conventional circuit simulators.

Each PCN line section is modeled as a transmission (ABCD)-matrix, with characteristic impedance Z_0 and propagation constant $\gamma = \alpha + j\beta$ calculated using static impedance, dispersion and loss models from [11]. The T-junctions are modeled as described in [12]. Ideal symmetry within the combining network was assumed, neglecting line-coupling and transistor variations, to transform each T-junction to an equivalent two-port network. The impedance scaling is modeled with a $1{:}\sqrt{2}$ transformer between the input and output legs. As shown in Fig. 4, the calculated S-parameters results follow the active input and output reflections simulated in ADS closely from 0 through 40 GHz.

Fig. 5 shows the one-way PCN dissipation losses between a single transistor and the common output port, for various transistor counts N_T. The total PCN line length and losses increase with N_T, leading to a trade-off between output power and efficiency. A comparison with reference simulations in ADS shows accuracies better than hundredths of a dB for practical line lengths and frequencies up to 40 GHz.

2) *Matching Strategies*

The optimal Γ_{in} is based on the load-pull data and a requirement for optimum P_{del}, PAE or a trade-off between the

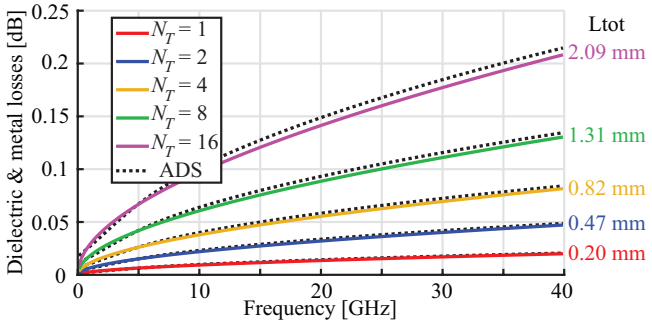

Fig. 5. Calculated losses for synthesized $N_T : 1$ GaN-based power combining networks consisting of 50 Ω microstrip lines, with ADS-simulated reference values. L_{tot} denotes the line length between each transistor and the output.

Table 1. Required antenna impedance in [Ω] for optimum PAE without MNW, for N_T GaN transitors with synthesized on-chip PCN.

N_T	1 GHz	10 GHz	30 GHz
1	331+j126	27.9+j76.2	9.0+j13.8
2	157+j70.7	10.7+j28.2	4.3-j11.6
4	75.8+j37.2	4.7+j6.4	3.2-j31.2
8	36.7+j18.6	2.3-j6.0	8.8-j81.4
16	17.8+j8.3	1.3-j17.6	3.8+j30.7

two. With the synthesized PCN-parameters and Γ_{ant} known, a matching network can be synthesized to achieve this optimum load impedance.

As the examples in this work follow common GaN-HPA design practices, series and shunt capacitances are modeled as low-loss lumped elements whilst series inductances are achieved by adjusting line lengths. An expansion of the model is planned to perform incremental matching steps throughout the combiner network instead of in between the PCN and WB, as is conventional in HPA design for bandwidth improvement.

Alternatively, the optimum Γ_{in} can be translated to an optimum impedance $Z_{ant,opt}$ at the antenna interface, which can then be considered as design goal for a direct-matched antenna. As seen from the example results listed in Table 1, an impedance scaling trend of $1{:}N_T$ is seen at 1 GHz where the PCN is electrically small. At 10 and 30 GHz the effects of drain parasitics and line lengths become more pronounced.

3) *Wire-Bond Interconnect*

A series resistive-inductive (RL)-network can be included to model the influence of a wire-bond. For brevity of this paper,

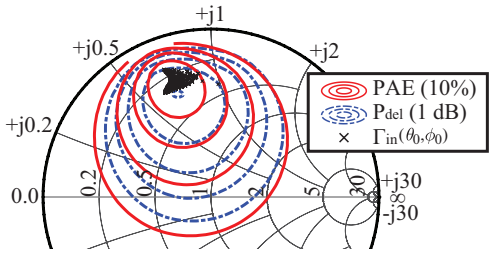

Fig. 6. Varying values of Γ_{in} due to scanning to angle (θ_0, ϕ_0) within 75° from broadside, projected onto interpolated load-pull contours.

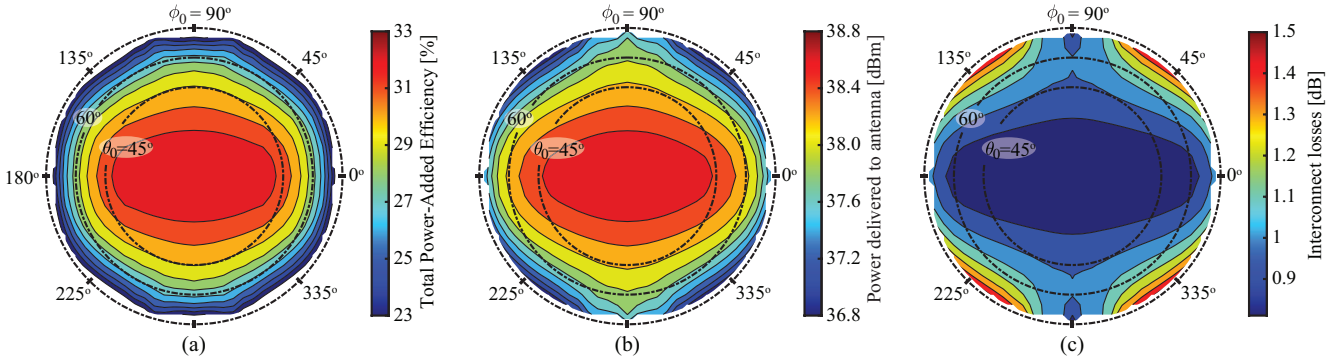

Fig. 7. Model results for a 30 GHz 50 Ω stacked-patch element in an infinite array, connected to an eight-transistor GaN HPA with a synthesized PCN, a single on-chip L-shaped MNW, and a 500 μm bondwire. In (a) and (b), the total PAE and P_{ant} values are mapped to their respective scan angles (θ_0, ϕ_0) within 75° from broadside. The total mismatch and network losses between the Γ_{in} and Γ_{ant} interfaces are plotted for each scan angle in (c).

it is assumed the antenna is connected directly to the chip output interface after the WB. The off-chip networks between WB and antenna are considered inactive, although their implementation is similar to the PCN and MNW components.

IV. Combined Results

The load-pull data, synthesized PCN S-parameters and the antenna ARC are combined in MATLAB to achieve a fast estimate of the effect of scanning on transistor output power and efficiency. The results of this procedure are illustrated with a stacked-patch element at 30 GHz, a single L-type MNW and a HPA consisting of eight 4-finger GaN transistors.

The scan-angle dependent $\Gamma_{ant}(\theta_0, \phi_0)$ is mapped to the load-pull data as depicted in Fig. 6. The interpolated PAE and delivered power results are mapped back to each scan angle. The modeled L-shaped MNW was designed for an optimum transistor-level PAE at a scan angle of $(15°, 45°)$. It should be noted that this matching network was designed for a single frequency and does not provide a wide-band match.

The power and mismatch losses are calculated with Z_{ant} and the network S-parameters, which can be combined with the delivered power and element pattern to achieve the resulting total PAE and P_{ant} per antenna element for any given scan angle (θ_0, ϕ_0). The total PAE, P_{ant}, and losses are depicted for scan angles within $\theta_0 \leq 75°$ in Fig. 7a-c.

V. Conclusion

This contribution has presented a fast model for prediction of direct-connected HPA-antenna performance in scanning arrays, with a focus on the impedance-scaling and power-dissipation effects in the PCN. The model can assist in preliminary design choices as technology and transistor count.

An expansion of the model is planned to provide results for given frequency spans and for finite arrays. The next step is to derive generalized co-design strategies and first-order technology choices for HPA and AIAA-elements to meet given operating frequency and transmit power requirements.

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