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Original scientific article

Performance Improvement for Reconfigurable Processor System Design in IoT Health Care Monitoring Applications

K. GANAPRIYA*, A. POOBALAN, K. KALAIVANI, S. GOPINATH

Abstract: This research focuses on critical hardware components of an Internet of Things (IoT) system for reconfigurable processing systems. Single-Instruction Multiple-Data (SIMD) processors have recently been utilized to preprocess data at energy-constrained sensor nodes or IoT gateways, saving significant energy and bandwidth for transmission. Using traditional CPU-based systems to implement machine learning algorithms is inefficient in terms of energy consumption. In the proposed method Single-Instruction Multiple-Data (SIMD) processors are assembled by scaling the largest possible operand value subunits into direct access to the internal memory, where the carry output of each unit is conditionally fed into the next unit based on the implementation of the SIMD Processor design for Internet of Things applications. Each method has evaluated sub-operations that contribute considerably to the overall potential of the design. If the single register file can complete the intended action, a zero (one)-signal is applied to each unit's carry input. Multiplexers combine two or more adders, sending the carry signal from one unit into another if additional units are necessary to compute the sum. The outcome results compare high-speed end device techniques in terms of area and power consumption. The proposed SIMD processor-based IoT healthcare monitoring system with a MIMD processor's performance analysis of comparison clearly demonstrates that the system produces decent outcomes. The suggested system has an area overhead of 85 m^2, a power usage of 4.10 W, and a time delay of 20 ns.

Keywords: area and power consumption; health care; Internet of things (IoT); reconfigurable processor; single-instruction multiple-data (SIMD)

1 INTRODUCTION

Due to the ability of Reconfigurable computing to hand speed up a huge variety of applications, it has invited many researchers to this domain. The prominent feature of Reconfigurable computing lies in the fact that it deals with both hardware and software solutions in terms of speed and performance. Reconfigurable computing also involves the power of coupling i.e. if there is some programming logic that cannot be mapped onto the Reconfigurable architectures, then they can be executed to some host microprocessors [1]. Numerous coupling techniques can couple devices with the Reconfigurable logic and they are as follows: First, the Reconfigurable architectures can be used as a standalone functional unit with a host coprocessor. Second, the Reconfigurable architectures can act as a-processor and third, the Reconfigurable architectures can be interfaced with some processors for implementing only some functions and four, the microcontrollers and microprocessors can use Reconfigurable architectures if they require extra memory or want to implement some complex logic functions. The Reconfigurable architectures are flexible and can be integrated with other devices, however, this integration would be application-specific. The Reconfigurable architecture is extensively used in developing different applications of Image processing and Micro strip patch antennas for wireless applications [2]. IoT is certainly one of the most energizing topics for society, research, and industry network whereas the conventional Web encourages correspondence between several devices as well as individuals, IoT integrates a wide range of "things" through an entire system of interrelated information without human intervention. The need for IoT and the progression of remote correspondence innovations enable patients' well-being to designate concentrated parental figures progressively [3]. In addition, multiple accessible sensors or flexible instruments can calculate human biological measurements directly by simple contact, including the Heartbeat (HR), The Breath Rate (RR), and Circulatory Strain (BP). Even though it is always in the preliminary stage, the IoT intensity has been immediately understood by organizations and enterprises and updates have been produced along with client encounters. However, the coordination of IoT innovation in medicinal services brings a few difficulties including information storing, information management, information sharing between devices, safety and protection; combined and daunting exposure. Cloud Computing Technology is a potential solution to these problems [4]. IoT-based sensitive devices generate a great deal of information. Such information will use measurements and applications for processing algorithms. Vital productivity is needed to accomplish increased performance, accuracy, and to incur the least cost for IoT-based smart devices. Such massive data can be stored, created and imaged from IoT. There are extremely helpful details and various possible properties in the sensor material.

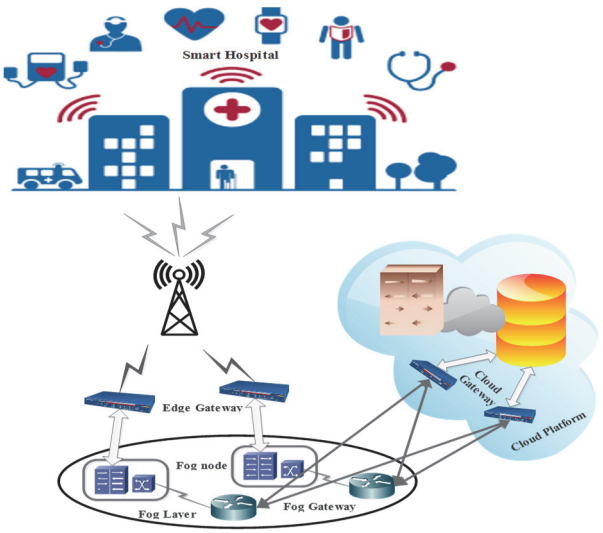

Figure 1 Overview of a modern healthcare network relying on IoT and cloud storage

The system will be associated with around 30 billion smart devices. However, the microcontroller or processor

requires device computing capacity to upgrade the most essential device. This promotes better economic battery reinforcing tools to use FPGA. The sensor hubs rely on microcontrollers as the preparation capacity is limited. The FPGAs provide optimized phases and target to chip away with economic power and vitality use [5-7]. Fig. 1 demonstrates a standard medical services platform that integrates IoT as well as cloud networking which includes general and clear information and routine basis, existing on-demand resources across the network and the execution of tasks that are in problems.

2 LITERATURE SURVEY

The focus of this work is the design and analysis of low power strategies' for signal processing and communication blocks for IoT applications using reconfigurable arithmetic unit-based SIMD processors. The hierarchical design of a signal processing block consists of sub-systems such as multipliers and adders that form the fundamental building block for any signal processing unit. In this chapter, a literature review on the design and analysis of various multipliers and adders is presented [8-10]. The adder function is used in the majority of applications. These are accomplished through the use of multiple CMOS logic types. It serves as a fundamental functional unit in the majority of complicated computational circuits and Arithmetic Logic Units (ALU). Adder was a significant source in applications such as laptops, personal computers (PC), microprocessors, microcontrollers, filters, etc. As a result, the creation of low-power and area-efficient adders plays a critical role in modern technologies [10-13]. The pull-up network employs two PMOS transistors, whereas the pull-down network employs two NMOS transistors. Similarly, an XNOR gate and a NOT gate are used to construct another adder. It differs from the original design in that it makes use of an XNOR gate [14]. The proposed new Full Adder cell surpasses current techniques in terms of power delay product, such as Gate Diffused Input (GDI) Full Adder cell and Static Energy Recovery Full Adder (SERF) low power consumption. It also solves the output voltage swing SERF and GDI cell issues [16]. Full Adder design with 8 transistors uses a three transistor XOR gate to lower the device's power consumption by decreasing the transistor count. It has a 2:1 multiplexer to calculate the carry. The bias voltage in this innovative design is 450 mV, which is applied to an NMOS transistor linked across the output. Because of its modest space and energy efficiency, this design is appropriate for high processors. The aspect ratio is changed to downsize the transistors and get a powerful '0' and '1' output [17]. The three modules are used to create the Hybrid Full Adder. Two modules are used to conduct the XNOR logic function, and one is used to compute the carry. Modules 1 and 2 are linked together to calculate the sum output. To decrease power usage, the XNOR circuit employs weak inverters. When MOS transistors have a narrow channel width, they are weak inverters. To produce a total swing output, the reaction from the inefficient inverters is used to construct a controlled inverter that functions as a level restorer. The suggested XNOR circuit is built using six transistors, which reduces size and power consumption [18]. In this work two 16-bit Ripple Carry Adders (RCA) performed better in performance characterized by low PDP, full-swing operation, and outstanding driving talents compared to ordinary complete adders. A cadence layout editor is used to evaluate circuits, which are then extracted utilizing 0.13 mm and 90 nm PD SOI CMOS technology [19]. The author analyzed Pass Transistor Logic (PTL). The first kind of issue is a decline in the threshold voltage across the channel of transistors, which affects the driving current and the speed of operation at low voltage levels. This is relevant to low power design since running at the lowest voltage level is required. The following issue is that V is not the high input voltage level of the regenerative inverters, and the PMOS (P-type Metal-Oxide-Semiconductor) transistor in the inverter is not turned off, resulting in sizeable static power dissipation [20]. In this technique wireless capsule endoscopy is a popular method of doing endoscopic procedures to obtain gastrointestinal tract photos for medical diagnosis because its DCT has a vital energy compaction feature for associated image pixels. For this real-time application, image compression is preferable. To suit the wireless capsule endoscopy applications strict power budget and compact size constraint, an energy-efficient DCT based on CMOS implementation [21]. A full adder was shown, which was created using three modules. Two modules are selected to conduct the XNOR logic function, and one is used to compute the carry. Modules 1 and 2 are linked together to calculate the sum output. To decrease power usage, the XNOR circuit employs weak inverters. When MOS transistors have a narrow channel width, it is referred to as a weak inverter. The reaction from the inefficient inverters is used to create a controlled inverter that functions as a level restorer to achieve a total swing output. The suggested XNOR circuit is built using six transistors, which reduces size and power usage [22]. A low-voltage, low-power CMOS full adder was proposed, including rigorous design methodologies integrating k-maps and the pass network theorem. When the power supply voltage is lowered, this design can function reliably within certain limitations. The designed circuit tries to reduce power consumption and transistor count while running at low supply voltages. When all control signals are high, an NMOS (PMOS) transistor series connection sends the input to the output (common). In this situation, pass logic implementations are used. The key difference between pass and gate networks is that the reduction technique must include both 0 s and 1 s from the function. Initially, the pass network selects all necessary pass primes [23]. The power-gating technique: outcome benefits and drawbacks of the power-gating approach in terms of power, area, and performance are examined in this article. This experiment demonstrates that 4% of the overall site and 5% of the dynamic Power are sacrificed, saving 47% of leakage power while retaining the same performance. Several factors, including sleep transistor size and latency, are closely connected to power gating, supply voltage level and area. The gated region experimentally demonstrates that the circuit and power mesh grain impact the gating approach's system-level power budget. As a result, power gating is a low-power optimization strategy for the coming generation of Technology [24]. ECRL gates are powered by a timed power source, allowing energy recovery and repurposing. By employing the ECRL technology, the adder's power dissipation is decreased. Additionally, the

ECRL adder has fewer transistors. This work proposes a unique gate-level approach based on the pencil and paper approach for the optimum Parallel Carry-Select Adders design. This method is straightforward and organized, which explains why the multiplexer delay depends on its fan-out. More than 1000 adders have validated the suggested technique. According to analysis, the method results in a hold that is often modest and always within 5.7%. CSL provides a reasonable performance-area-power trade-off that falls between the low power consumption [25]. A better power-performance trade-off is produced via a revolutionary power gating method. Saving the multiple mode capability enables a CPU to enter power-saving modes more frequently due to more significant leakage. The many sleep phases provide an additional 17% decrease of total leakage over typical single-mode gating. Leakage in a retentive manner can occur in a single state. Lowered by up to 19% of data route splitting method leads to a reduction of 3.2. A 9% decrease in standby mode leakage and an improvement in intermediate mode leaking methods for fine-grained power-gating are also beneficial in lowering ground bounce and minimizing the impact on surrounding logic [26]. This section discusses the literature survey for many of the complex designs that have adopted power reduction techniques at different hierarchies. Very little literature addresses the reduction of power at all levels of abstraction. Hence, it is required to demonstrate that power reduction can not only be achieved at one level of abstraction but all levels of abstraction.

3 PROPOSED SYSTEM

SIMD computing accelerates the development of linear system of equations methods such as LU decomposition and iterative matrix inversion techniques. On top of current SIMD computer techniques, the capacity of SIMD architectures to operate massive vectors in a short period of time has been established. However, g code executed code programmer into hardware logic will result in an inefficient solution. Because power system applications comprise a combination of seldom executed code and code to manipulate large matrices in real time, we chose a SIMD architecture in which an array of processing components that perform the most critical calculations is connected to a host. A significant amount of IoT devices is remote because the devices cannot be wired over and over. A number of IoT devices are remote because the devices cannot be wired repeatedly, the battery space is restricted. Strengthening this device is a challenging task. Now, the significant components of the IoT systems are defined because it is necessary to consider the elevated sensor location under hazards concerning IoT devices and applications. For each, an IoT system can be described as a network of equipment, scheduling, availability arrangements, and sensors in the grid of deviating things. Therefore, IoT Hardware Design comprises four essential segments: detecting, networking, information handling, and application phase. These Phases are shown in important form below.

3.1 Detecting Phase

The primary motivation behind the detection phase would be to discern some mystery at the edge of the devices and obtain data from the actual truth. There are a few sensors in this row. One of the main aspects of IoT devices is the usage of different sensors for applications.

3.2 Network Phase

This phase of the process goes like a correspondence channel for collecting information to other from vices in the detection process phases. The network layer is updated with numerous (wired and wireless) communications technologies to enable data to stream among devices throughout a specific network.

3.3 Information Handling Phase

The information handling layer comprises the primary information preparation unit of IoT devices. The data preparing phase takes information gathered in the detecting phase and investigates the data to resolve choices dependent on the outcome. This level may share the consequence of information preparation with other associated devices through the system layer.

3.4 Application Phase

The application layer executes and presents the consequences of the information preparing layer to achieve the unique utilization of IoT devices. The application layer is a client-driven layer that executes different errands for the clients.

3.5 Reconfigurable Processor Computing in IoT

This research focuses on critical hardware components of an IoT system for reconfigurable processing systems. SIMD processors have recently been utilized to preprocess data at energy-constrained sensor nodes or IoT gateways, saving significant energy and bandwidth for transmission. Using traditional CPU-based systems to implement machine learning algorithms is inefficient in terms of energy consumption. As a result, a hardware accelerator is presented, and an optimization approach increases throughput while lowering power consumption. Because of their parallelism, traditional SIMD computers are extremely effective for early visual processing. However, they have several issues when it comes to conducting more complex processing, such as low performance in global operations and a tradeoff between processing flexibility and pixels. This paper presents a novel vision chip design with example algorithms that can dynamically rearrange its hardware by chaining processing components. To overcome the aforementioned concerns and create a capability for performing more advanced processing, a new architecture has been devised. In terms of functionality, it varies from typical vision chips and SIMD processors. It can, for example: 1) calculate scalar feature values like summations at high rates; 2) carry out fast communication between distant PEs; and 3) dynamically change the PE grain size and network architecture. These qualities are attained by making very minimal changes to a normal SIMD image processor, yet the total performance is much improved. Fig. 2 depicts the structure of the PE. It functions similarly to a traditional SIMD image processor, with a 1-bit ALU and local memory, but it only performs

one-bit actions at a time. However, the inter-PE communication partner output port is a latch rather than a flip-flop. Each PE is equipped with a Photodetector (PD), which is arranged in a two-dimensional array. Each PE is linked to the up, down, left, and right PEs in its area and communicates with them. Data from outside the array is always 0 since the grid is open-ended. Every row and column has its own global bus, and data is fed into them from the outside through shift registers. With the development of the Internet the Internet of Things (IoT) development devices need to be more skilled than previous embedded systems, which follow strict power constraints. The power consumption planning must be changed to integrate new capabilities such as learning. Approximate calculations are promising examples for reducing power consumption while introducing errors into calculations. In this work, a Single Instruction Multiple Data (SIMD) processor array for migrating machine learning applications into IoT edge devices are presented for medical application and the Multiplier-Accumulator (MAC) unit of SIMD is designed.

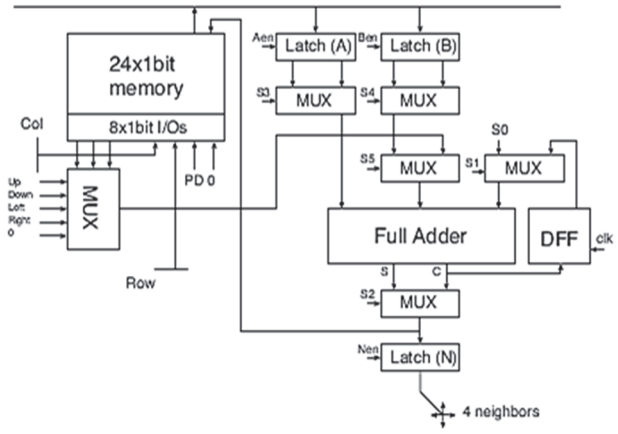

Figure 2 Structure of SIMD-PE

Fig. 3 depicts the SIMD processor's architecture, which demonstrates that up to 32 processor components can work in parallel and execute the same instruction. A daisy chain is used to send data from the FFT/IFFT to each processor element. Each processing element has its own local memory unit, where data streams and intermediate results are stored as they are calculated. Each cycle requires three read and one write requests to service the arithmetical unit. For the real and imaginary parts of complex numbers, the arithmetic unit uses an 18 bit 32 bits.

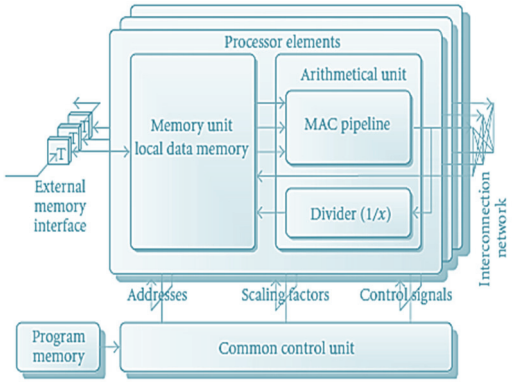

Figure 3 SIMD processor

The vector-optimized arithmetic unit consists of a MAC (multiply and accumulate) unit and a divider unit. The division unit can be used to calculate the proportion of true worth. This work, for example, is required to standard transitional findings. The number of divisions in the algorithms under examination is fairly little in comparison to the MAC operations. One division unit is shared by eight processor elements in this investigation. In this, a designed SIMD processor is used to monitor patient details through IoT.

4 SIMULATION RESULTS AND DISCUSSION

This section compares the simulation outcomes and the performance analyses of the proposed reconfigurable IoT system with various other current approaches. The suggested device's simulation is built on Xilinx 14.7 software and Spartan 6 xc6slx-3csg32.

Table 1 Device Utilization of different Reversible hybrid Adders (16 and 32 bit Inputs)

Devices	32 bit inputs			
	Rev-KS-RCA	Rev-KS-CSlA	Rev-KS-CSkA	Rev-KS-CLA
No. of LUTs	81	94	87	84
No. of FFs	82	94	85	82
No. of Ios	102	102	102	103
Delay (ns)	10.63	9.569	9.61	8.67

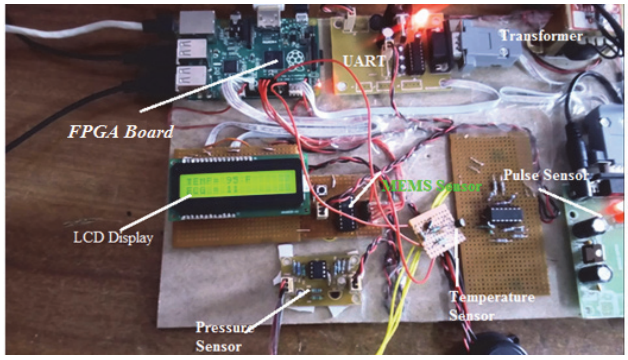

Figure 4 Prototype model of IoT applications

Fig. 4 shows the real-time hardware implementation model of the proposed SIMD processor-based wireless patient healthcare monitoring system using IoT. Fig. 5 shows the IoT web page screenshot of the proposed SIMD processor-based patient monitoring system. This IoT webpage continuously obtains the data from the local server every 5secs. If any abnormal status occurs, the IoT server sends the alert to doctors and family members.

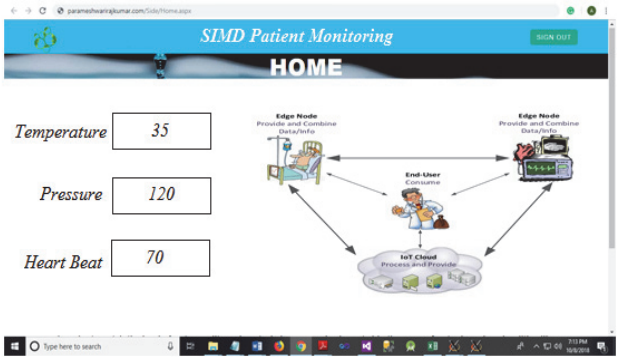

Figure 5 Screenshot of IoT web page

Tab. 2 explains the proposed SIMD processor-based IoT healthcare monitoring system with a MIMD processor's performance analysis of comparison clearly demonstrates that the system produces decent outcomes. The suggested system has an area overhead of 85 m^2, a power usage of 4.10 W, and a time delay of 20 ns.

Table 2 Performance analysis of SIMD and MIMD based Healthcare monitoring

Processors	Area overhead / μm^2	Power consumption / μW	Time delay / ns
MIMD	176	10.27	51
SIMD	85	4.10	20

5 CONCLUSION

This work presents the efficient design of reconfigurable SIMD processors for IoT medical applications for patient monitoring . The impact of SIMD size and varied instruction sets on possible performance is discussed in this work. Several challenges affecting IoT applications regarding SIMD optimization are explored, and solutions for all architectures are offered. For IoT applications, most designs contain particular SIMD instructions. While the recommended method can result in considerable performance improvements, it may be unsuccessful for other application families. We found a set of generic SIMD instructions in this research that significantly improve the performance of IoT-based health monitoring apps. The suggested SIMD processor architecture has modified the modifiers for framing multiplier structure, notably with the reconfigurable ALU. With clever inventiveness, the potential for reducing delays and power have been proved. This illustrates that reconfigurable processor technologies are effective in enabling IoT-based health monitoring applications to be implemented. Smart innovation has proved the ability to reduce delays and improve power. This illustrates that reconfigurable processor technologies are effective in enabling IoT-based healthcare monitoring applications to be implemented.

6 REFERENCES

[1] Akbar, M. A., Wang, B., & Bermak, A. A. (2020). Self repairing hybrid adder with hot-standby topology using fault localization. *IEEE Access*, *8*, 150051-150058. https://doi.org/10.1109/ACCESS.2020.3016427

[2] Awaludin, A., Harashta, L., & Kim, H. (2021). High-Speed and Unified ECC Processor for Generic Weierstrass Curves over GF (*p*) on FPGA. *Sensors*, *21*(4), 1451. https://doi.org/10.3390/s21041451

[3] Bartík, M. (2020). External Power Gating Technique An Inappropriate Solution for Low Power Devices. *11th IEEE Annual Information Technology, Electronics and Mobile Communication Conference (IEMCON)*, 0241-0245. https://doi.org/10.1109/IEMCON51383.2020.9284855

[4] Chu, Y. Y., Shieh, S. H., Feng, H., Deng, H., Shiau, M. S.,& Huang, D. C. (2021). A high-speed carry-select adder with optimized block sizes. *IEEE 15th International Conference on Anti-counterfeiting, Security, and Identification (ASID)*, 182-186. https://doi.org/10.1109/ASID52932.2021.9651488

[5] Daphni, S. & Vijula Grace, K. S. (2021). Design an Area Efficient Kogge Stone Adder using Pass Transistor Logic. *Third International Conference on Intelligent Communication Technologies and Virtual Mobile Networks (ICICV)*. https://doi.org/10.1109/ICICV50876.2021.9388489

[6] Devnath, B. C., Biswas, S. N., & Datta, M. R. (2020). 4-bit wallace and dadda multiplier design using novel hybrid 3-2 counter. *2nd International Conference on Advanced Information and Communication Technology (ICAICT)*, 189-194. https://doi.org/10.1109/ICAICT51780.2020.9333511

[7] Dra, S. K. R., Deb, S., Vrms, V., & S. S.(2021). Design and analysis of high-performance carry skip adder using various full adders.*Smart Technologies, Communication and Robotics (STCR)*,1-5. https://doi.org/10.1109/STCR51658.2021.9588863

[8] Dubey, S. & Verma, G. (2020). Analysis of Basic Adder with Parallel Prefix Adder.*First IEEE International Conference on Measurement, Instrumentation, Control and Automation (ICMICA)*, 1-6. https://doi.org/10.1109/ICMICA48462.2020.9242842

[9] Xingzhi, F., Qingjiang, L., Weihe, W., Hui, X., Yinan, W., Wei, W., Hongqi, Y., & Zhiwei. L. (2022). High-Speed Memristor-Based Ripple Carry Adders in 1T1R Array Structure. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *69*(9), 3889-3893. https://doi.org/10.1109/TCSII.2022.3174219

[10] Garg, N., Pratap, Y., Gupta, M., & Kabra, S. (2021). Dielectric Separated Independent Gates Junctionless Transistor (DSIG-JLT) For Highly Scaled Digital Logic Implementation. *IEEE Transactions on Nanotechnology*, *20*, 262-269. https://doi.org/10.1109/TNANO.2021.3066814

[11] Giustolisi, G. & Palumbo, G. (2022). Analysis and comparison in the energy-delay space of nanometer CMOS one-bit full-adders. *IEEE Access*, *10*, 75482-75494. https://doi.org/10.1109/ACCESS.2022.3192016

[12] Gorgin, S., Nejad, H. Z., & Lee, J. A. (2022). A practical energy/power reduction approach for parallel decimal multiplier. *IEEE Access*, *10*, 11372-11381. https://doi.org/10.1109/ACCESS.2022.3145001

[13] Gulafshan, M. A. & Khan Hasan, M. (2022). Design of high speed, energy, and area efficient spin-based hybrid MTJ/CMOS and CMOS Only Approximate Adders. *IEEE Transactions on Magnetics*, *58*(5), 1-8. https://doi.org/10.1109/TMAG.2022.3155968

[15] Hu, X., Abraham, A. S., Incorvia, J. A. C., & Friedman, J. S. (2021). Hybrid pass transistor logic with Ambipolar transistors. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *68*(1), 301-310. https://doi.org/10.1109/TCSI.2020.3034042

[16] Li, Y., Cui, X., & Zhang, Y. (2022). An Efficient CRT-Based Bit-Parallel Multiplier for Special Pentanomials. *IEEE Transactions on Computers*, *71*(3),736-742. https://doi.org/10.1109/TC.2021.3058346

[17] Lu, Z., Mou, H., Pu, Y., Wen, Y., Zhang, X., & Zhang, X. (2022). Magnetic full adder based on negative differential resistance-enhanced anomalous hall effect. *IEEE Magnetics Letters*, *13*, 1-5. https://doi.org/10.1109/LMAG.2022.3146132

[18] Nirmaladevi, R. & Seshasayanan, R. (2019). Energy efficient parallel hybrid adder architecture for 3X generation in radix 8 booth encoding.*Cluster Computing*, *22*(5), 10709-10716.

[19] Panda, A. K., Palisetty, R., & Ray, K. C. (2020). High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder. *IEEE Transactions on Circuits and Systems*, *67*(11), 3944-3953. https://doi.org/10.1109/TCSI.2020.3016275

[20] Pinto, R. & Shama, K. (2019). Low-power modified shift-add multiplier design using parallel prefix adder. *Journal of Circuits, Systems and Computers*, *28*(02), 1950019. https://doi.org/10.1142/S0218126619500191

[21] Ranasinghe, A. C. & Gerez, S. H. (2020). Glitch-optimized circuit blocks for low-power high-performance booth Multipliers. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *28*(9),2028-2041. https://doi.org/10.1109/TVLSI.2020.3009239

[22] Shukla, P., Kumar, P., & Misra, P. K. (2022). A highly reliable, dynamic logic-based hybrid MTJ/CMOS magnetic

full adder for high-performance and low-power. *IEEE Transactions on Magnetics, 58*(5),1-8. https://doi.org/10.1109/TMAG.2022.3159823

[23] Tsai, K. L., Chang, Y. J., Wang, C. H., & Chiang, C. T. (2021). Accuracy-configurable Radix-4 adder with a dynamic output modification scheme. *IEEE Transactions on Circuits and Systems*, *68*(8), 3328-3336. https://doi.org/10.1109/TCSI.2021.3085572

[24] Yang, T., Sato, T., & Ukezono, T. (2020). An Accuracy-Configurable Adder for Low-Power Applications. *IEICE Transactions on Electronics*, *103*(3), 68-76. http://dx.doi.org/10.1587/transele.2019LHP0002

[25] Zhi, Y., Kuiqing, H., Zeqing, Z., Yao, L., Zheng, L., Yijiao, W., Zhaohao, W., & Weisheng, Z. (2022). A novel computing-in-memory platform based on hybrid spintronic/CMOS memory. *IEEE Transactions on Electron Devices*, *69*(4), 1698-1705. https://doi.org/10.1109/TED.2021.3137761

[26] Vinoth Kumar, K., Karthikeyan, S., Bhavani, S., & Vennila, C. (2022). Performance Improvement of SIMD Processor for High-Speed end Devices in IoT Operation Based on Reversible Logic with Hybrid Adder Configuration. *Technical Gazette*, *29*(1), 252-258. https://doi.org/10.17559/TV-20210719025814

Contact information:

K. GANAPRIYA, Assistant Professor
(Corresponding Author)
Department of Electronics and Communication Engineering,
SSM Institute of Engineering and Technology, Dindigul, India
E-mail: ganapriyag@gmail.com

A. POOBALAN, Assistant Professor
Department of Computer Science and Engineering,
University College of Engineering, Dindigul, India
E-mail: apoobal@gmail.com

K. KALAIVANI, Associate Professor
Department of Information Technology,
Vignana Bharathi Institute of Technology,
Hyderabad, Telangana, India
E-mail: kalaivani.sai21@gmail.com

S. GOPINATH, Professor
Department of Electronics and Communication Engineering,
Karpagam Institute of Technology, Coimbatore, India
E-mail: gopi.vasudev@gmail.com