Sensors & Transducers, Vol. 263, Issue 4, December 2023, pp. 29-35

www.sensorsportal.com

Sensors Transducers

Published by IFSA Publishing, S. L., 2023
http://www.sensorsportal.com

Setting Point and Operation Range of a BiCMOS On-Chip BiCMOS Thermometer

*** B. TON, S. CHEN, D. PRÊLE, and M. GONZALEZ**
Université Paris Cité, CNRS, Astroparticule et Cosmologie, F-75013 Paris, France
Tel: +33 757421933
E-mail: ton@apc.in2p3.fr

Received: 9 October 2023 / Accepted: 8 December 2023 / Published: 21 December 2023

Abstract: Thermometer circuit can be designed in BiCMOS technology to measure directly the on-chip temperature right close to other functions of an Application Specific Integrated Circuit (ASIC). This paper discusses on-chip thermometry with high temperature sensitivity. The setting of an operating point around 50 °C with no-offset is discussed allowing a multiplication of the output current times ten for a better sensitivity. An analytical model based on a proportional to temperature cell and a complementary to absolute temperature cell is discussed. Linear response in the [-150 °C: +150 °C] is illustrated. However, out from this range, deviations between analytical models and simulations based on foundry models are discussed pointing the importance of the setting point depending on the temperature range.

Keywords: On-chip thermometer, BiCMOS, ASIC, CTAT, PTAT.

1. Introduction

Temperature management in electronic devices is highly recommended in the design and development of technology. Each device has its specific temperature range, and operating outside this range may lead to performance degradation (e.g., the battery's effectiveness may change due to cooling or heating [1]), or sometimes increase the rate of failure. Temperature measurement is also crucial in meeting the high reliability requirements of electric systems because elevated temperatures can cause aging [2], decreasing the lifespan of these devices [3]. In the context of space missions, managing temperature variations is sometimes required to ensure the lifetime of the mission. Moreover, controlling the device's temperature within the operational range can prevent thermal runaway of certain devices, thereby enhancing mission safety. To align with the rapid pace of technological advancement, integrated circuits are increasingly incorporating a greater number of transistors, reaching figures greater than one hundred thousand, a scale commonly referred to as Very Large Scale Design (VLSI) [4]. Decreasing the transistor size increases parasitic resistance and transistor density, leading to an increase of Joule dissipation [5] (self-heating) caused by the flow of current passing through the conductors (i.e.: interconnection [6]). Whether improving dissipation systems, optimizing the layout or selecting low resistance conducting materials could help, it is still important to monitor and control the temperature of the chips.

This paper represents an extended version of the work presented in [7], focusing on the design of an application-specific integrated circuit (ASIC) incorporating a thermometer using IHP 130 nm BiCMOS SiGe technology and discussing the operating range/ setting point. We delve into the topology considerations for sizing this novel thermometer by expressing the analytical model and

simulate it with Cadence software, showing a simulated linear sensitivity of approximately 10 µA/ °C within a 300 °C temperature range centered around room temperature (higher sensitivity is achievable in a smaller temperature range or with a higher voltage supply). The output signal propagates differentially, allowing for readout in current or voltage in a load without common-mode coupling. This off-chip differential signal propagation preserves the remaining functions of the ASIC (which are not discussed here) from common-mode noise contamination.

2. Design Methodology

The methodology for developing a thermometer using electronic devices commonly relies on reading the temperature coefficient of resistances (thermistors [8], RTDs, etc.) or it is based on the threshold voltage of diodes or transistors.

The temperature sensitivity is typically constrained by the direct temperature dependance of resistances or threshold voltages. This paper explores the use of two opposing semiconductor temperature-sensitive thresholds to cancel out the signal within the desired temperature range. This approach facilitates DC amplification, leading to a substantial enhancement in temperature sensitivity.

In more detail, the concept is rooted in two opposing temperature-dependent parameters inherent in a semiconductor junction: thermal voltage $V_T(T)$ and saturation current $I_S(T)$. On one hand, the thermal voltage $V_T(T)$ is proportional to absolute temperature; on the other hand, the saturation current increases exponentially with absolute temperature. Incorporating these two parameters, we introduce the junction voltage $V_J(T)$:

$$V_J(T) = V_T \ln\left[\frac{I_J}{I_S} + 1\right], \quad (1)$$

which is a function of thermal voltage $V_T(T)$ and the ratio between junction current and saturation current $I_J/I_S(T)$, which decreases with temperature.

In equation (1), $V_T(T)$ is defined as k_BT/q, where k_B represents the Boltzmann constant, T denotes the temperature in Kelvin, and q is the absolute value of the electric charge of electrons. Despite the linear increase of $V_T(T)$ with T, the thermal dependencies are predominantly influenced by the saturation current I_S. Notably, I_S exhibits an exponential growth with T, resulting in a decline of $V_J(T)$, as depicted in Fig. 1.

The natural logarithm in equation (1) transforms $V_J(T)$ into a parameter that linearly decreases with T, at least in a first approximation.

In addition to the direct use of these thermal dependencies, this paper discusses how to subtract DC/offset and combine (in absolute value) two thermal dependencies, to increase the sensitivity. The thermal dependencies can be efficiently amplified and the offset is canceled around a chosen operating temperature.

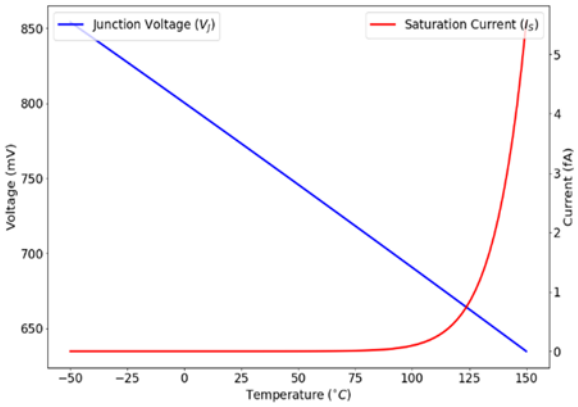

Fig. 1. The junction voltage $V_J(T)$ (in blue) decreases with temperature even though the contribution of thermal voltage $V_T(T)$ in the equation (1), owing to the exponential increase of the saturation current (in red).

3. Thermometer Circuit Design and Analysis

The idea of bandgap reference [9] is widely used in electronics. It provides a stable voltage with negligible variation in a large range of temperature by summing up signals with two opposite temperature dependencies. The voltage summation circuit adds together a complementary to absolute temperature (CTAT), and a proportional to absolute temperature (PTAT) voltage sources.

In this design, we propose a "subtraction" instead of "summation" to double the temperature sensitivity of the signal instead of canceling it. In addition, we use current sources instead of voltage sources.

The thermometer circuit consists of three components: a CTAT current source shown in Fig. 2, a PTAT current source illustrated in Fig. 3, and a crossing bridge for current subtraction. In ASICs design, where transistors are predominantly used instead of single junctions, we opt for the collector current I_C instead of the junction current I_J and the base-emitter voltage V_{BE} instead of the junction voltage V_J, employing an NPN bipolar transistor instead of a diode. In this section we will explain the working principles of the CTAT and PTAT current sources, using these fundamental parameters.

3.1. CTAT Current Source

The CTAT current source is based on the base-emitter voltage (V_{BE}) temperature sensitivity. Its schematic circuit is shown in Fig. 2. The two transistors B_7 and B_8 are mounted as a Darlington transistor [10], allowing to double the temperature

dependence. Indeed, the base-emitter voltage can be expressed and simplified as[1]:

$$V_{BE} \approx 2V_T(ln\frac{I_C/\beta}{I_S} + ln\frac{I_C}{I_S}) \approx 2V_T\, ln\frac{I_C}{I_S}, \quad (2)$$

where β is the ratio of collector and base current of the NPN bipolar transistors.

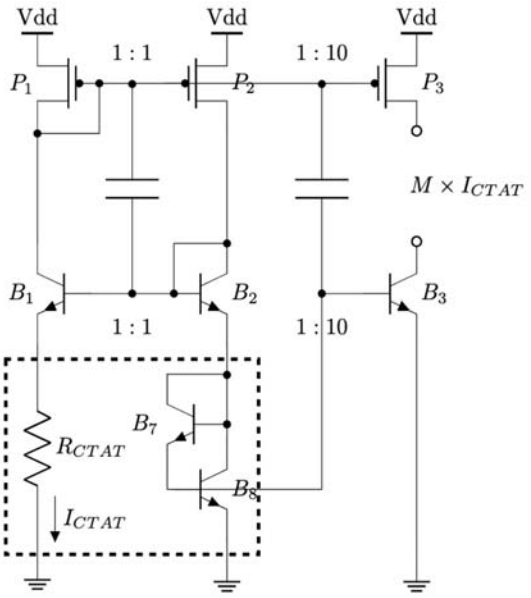

Fig. 2. CTAT current source applying the Darlington structure by combining transistors B_7 and B_8, where the resistor R_{CTAT} plays the role of converting base emitter voltage V_{BE} into the current through current mirror B_1: B_2. On the other hand, the PMOS P_3 and transistor B_3 amplify the current by the factor of 10.

The voltage across the resistor R_{CTAT} is equivalent to the base-emitter Darlington voltage, as referenced in equation (2). The overall expression for the current flowing through R_{CTAT} can be determined using equation (3):

$$I_{CTAT} = \frac{2V_{BE}}{R_{CTAT}} \approx \frac{2\,k_BT}{qR_{CTAT}}\, ln\frac{I_C}{I_S} \quad (3)$$

The saturation current I_S in equation (3) can be calculated as [11]:

$$I_S = \frac{q\,A_E D_n n_i^2}{W_B N_A}, \quad (4)$$

where A_E denotes the junction area, D_n is the diffusion coefficient of electrons and n_i is the intrinsic number of carriers. Otherwise W_B is the junction thickness[2], and N_A is the doping density.

To assess the thermal sensitivity of I_S, the temperature dependencies of parameters, D_n and n_i, are examined. D_n can be computed as:

$$D_n = V_T\mu_n = \frac{k_BT}{q}\mu_n = \frac{k_BT}{q}\, CT^a, \quad (5)$$

with $\mu_n = C\,T^a$ the electron mobility considering the case where lattice scattering is dominant [11]. The electron mobility is significant when lattice scattering dominates, a condition applicable for non-cryogenic temperature operations. The constants C and a are inherent to the material and the manufacturing process [12]. The carrier concentration n_i can be calculated with the following the equation [13]:

$$n_i = \sqrt{N_cN_v}T^{3/2}e^{\frac{-E_g}{2k_BT}}, \quad (6)$$

By substituting equations (5) and (6) into equation (4), we obtain the expression for the saturation current:

$$I_S = AT^{4+a}e^{\frac{-E_g}{k_BT}}, \quad (7)$$

where $A = \frac{k_BCA_EN_CN_v}{W_BN_A}$ is a coefficient independent of temperature. By substituting equation (7) into equation (3), we ultimately derive the expression for the CTAT current:

$$I_{CTAT} \approx \frac{2\,k_BT}{qR_{CTAT}} ln\left[\frac{I_C}{I_S}\right] = \\ = \frac{2\,k_BT}{qR_{CTAT}} ln\left[\frac{I_C}{AT^{4+a}e^{\frac{-E_g}{k_BT}}}\right] = \\ = \frac{2}{q\,R_{CTAT}}[\,E_g + k_BT\, ln\frac{I_C}{A} - (4+a)k_BT\, ln\, T\,] \quad (8)$$

We can explore the temperature dependence of I_{CTAT} by taking its derivative, obtaining:

$$\frac{\partial}{\partial T}(I_{CTAT}) = \frac{k_B}{qR_{CTAT}}[ln\frac{I_C}{A} - (4+a)\,(1+ln\,T)],$$

where a is an empirical parameter, ranging from -2 to -4 [15], so that $(4-a) > 0$ and $-(4+a)\,(1+ln\,T) < 0$. On the other hand, the term $ln\frac{I_C}{A}$ can be simply estimated refering to equation (7) in the case of silicon at 300K.

It turns out that $I_C \ll A$, so that $ln\frac{I_C}{A} < 0$. From these two approximations, we can conclude that $\frac{\partial I_{CTAT}}{\partial T} < 0$. This relationship illustrates the inverse correlation of CTAT current with absolute temperature.

[1] +1 doesn't appear in the junction equation for the remainder of the paper. This is because I_c/I_J is significantly greater than 1.

[2] Base width in the case of employing a bipolar transistor as opposed to a standard diode.

3.2. PTAT Current Source

The proportional to absolute temperature (PTAT) current source relies on the temperature sensitivity of a junction's thermal voltage (V_T). Illustrated in Fig. 3, a resistor R_{PTAT} is positioned beneath the emitter of transistor B_5. The voltage across the resistor can be determined as the base-emitter voltage difference between transistors B_5 and B_6 [14], as given by:

$$V_{PTAT} = V_{BE_6} - V_{BE_5} = V_T \, ln\frac{N_5}{N_6}, \quad (9)$$

with $N_5/\,N_6$ denoting the size ratio[1] between the two transistors B_5 and B_6. The term $ln\frac{N_5}{N_6}$ defines the thermal sensitivity of the PTAT current source.

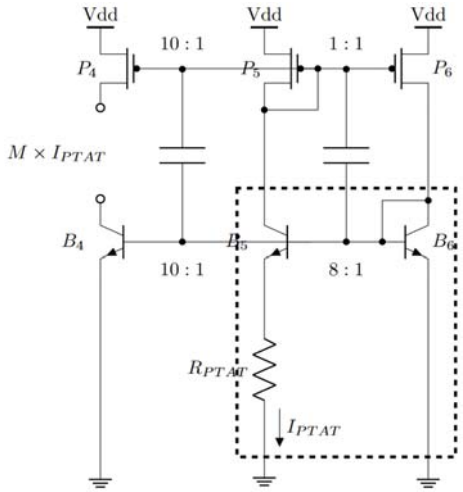

Fig. 3. PTAT current source schematic circuit. The transistor B_5 is eight times larger than the transistor B_6. The R_{PTAT} resistor plays the role of converting the V_{PTAT} into current through the current mirror $B_5{:}B_6$. On the other hand, the PMOS P_4 and the transistor B_4 are used to amplify the current by a factor of 10.

The current through R_{PTAT} can then be derived as:

$$I_{PTAT} = \frac{k_B\,T}{q\,R_{PTAT}}\,ln\frac{N_5}{N_6} \quad (10)$$

Equation (10) distinctly emphasizes the direct proportionality of I_{PTAT} with temperature. Due to the logarithmic nature, excessively increasing the ratio $N_5/\,N_6$ is not beneficial. A ratio of 8 is employed in our design to obtain the $ln\,8 = 2$ factor.

3.3. CTAT and PTAT Current Subtraction

The currents supplied by the CTAT and PTAT current sources exhibit slopes with opposite signs (Fig. 4) they can be combined to be subtracted in a load resistor. The resistances R_{PTAT} and R_{CTAT} can be tuned to optimize temperature sensitivity while nullifying the current offset at a specified temperature. This can be represented by the equation:

$$\Delta I = M \times (I_{PTAT} - I_{CTAT}) \quad (11)$$

The comprehensive circuit is depicted in Fig. 6, where R_{L+} and R_{L-} denote the readout load. P_3 and P_4 amplify the two currents by M = 10 before subtraction. This multiplication is feasible because the readout occurs after offset subtraction. Otherwise, the offset would considerably diminish the dynamic range. The M multiplying factor directly enhances temperature sensitivity, as demonstrated in Fig. 4 and Fig. 5.

3.4. Circuit Simulation with Cadence Virtuoso

In addition to formulating the analytical model based on the background outlined in the CTAT and PTAT sections, it is imperative to conduct simulations to validate our circuit design. The simulation employs device models from the IHP130 nm library, closely resembling the practical devices used in fabricating the ASIC. DC analysis is performed with temperature variations. This simulation serves the dual purpose of validating the developed model and delineating a suitable "range" for unknown parameters/operations, referred to as "empirical parameters."

4. Results

The circuit depicted in Fig. 6 has been simulated utilizing IC CAD tools (Cadence Virtuoso), demonstrating the anticipated linear progression of I_{PTAT} and I_{CTAT} with temperature across an extensive temperature range from -150 °C to 150 °C.

Fig. 4. shows the comparison between the temperature dependencies of ICTAT and IPTAT as analytically predicted, employing IHP130 BiCMOS ASIC technology. Setting $R_{PTAT} = 280\,\Omega$ and $R_{CTAT} = 6.25\,k\Omega$ these currents intersect at approximately 50 °C and demonstrate comparable slopes (in absolute value) of about 0.5 µA/ °C.

Finally, the configuration in Fig. 6 illustrates the method to subtract (equation (11)) the two currents, magnified by 10, resulting in a differential current flowing out from the ASIC into two resistor loads, R_{L+} and R_{L+}. A central-tap connected to the common mode voltage reference $V_{CM} = V_{DD}/2$ enables the receiver to set the common mode voltage of the differential signal. This technique decouples the common mode of the thermometer readout from the ASIC common

[1] In practice, different sizes of transistors are obtained by putting elementary transistors in parallel. Thus, N_5 and N_6 are the number of transistors connected in parallel.

mode, preventing noise contamination during the transmission process.

Minor deviations from the simulated output signal (depicted in black in Fig. 5) to analytical or simulated signals multiplied by 10 reveal non-idealities of the output current mirror. These non-idealities originate from both higher common-mode operation and extreme-temperature environments.

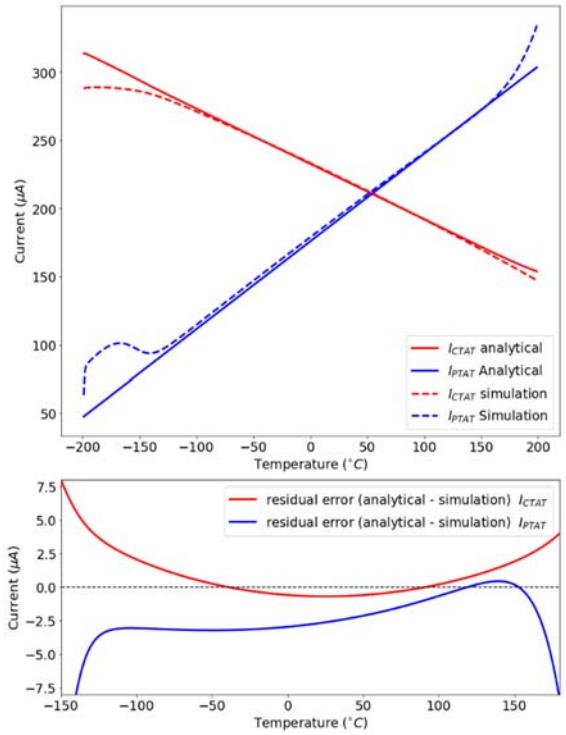

Fig. 4. I_{PTAT} and I_{CTAT} vs. temperature from $-200\,°C$ to $200\,°C$. Residuals between analytical results and simulations show non-linearity at temperature below -150 °C and above 150 °C.

5. Discussion

The linear relationship between output current and temperature within the range from approximately -150 °C to nearly 150 °C is illustrated in Fig. 5 and Fig. 6. A strong agreement between model and simulation is found in this temperature range. A significant deviation appears outside this temperature range.

The analytical model is based on the fundamental temperature dependencies of SiGe material (simplified for clarity). However, the model tends to overlook practical effects arising from the design, such as parasitic resistances, which are included in the simulations. These resistances can impact the temperature of ASICs, and their influence becomes more pronounced with increased design density, particularly under high voltage or current conditions. This section will focus on discussing factors that could cause the discrepancy of the analytical model compared to the simulation results.

Three reasons can be the cause of this:

1. Simulations made out of specified temperature range (linear model, extrapolation);
2. Analytical model does not consider high order thermal dependencies and neglect dependencies only significant far from room temperatures;
3. The thermometer schematic is optimized around room temperature (setting point: crossing 0 at 50 °C) leading to non-optimal operating point far from this temperature. Moreover, such thermometers with differential output provide a larger output current far from the setting point. Larger output current than 1 mA can lead to enhanced nonlinearities.

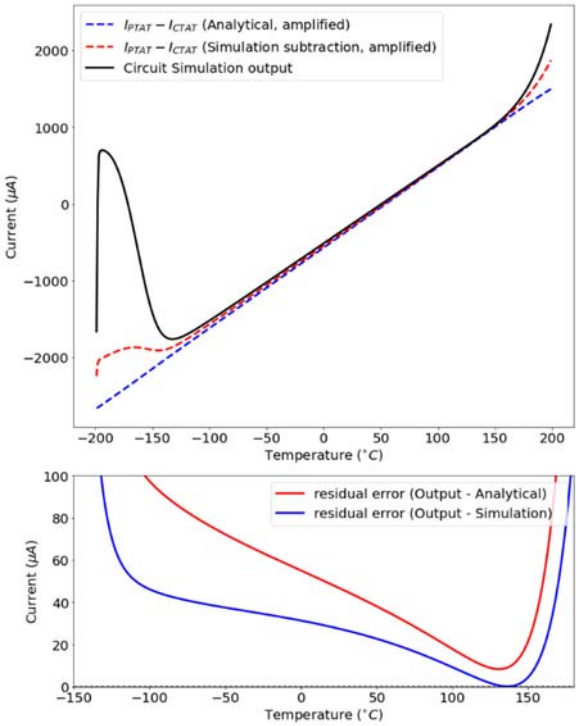

Fig. 5. Top: Differential output current of the thermometer flowing through the R_{L+} and R_{L-} loads (depicted in black) showing the 10 μA/ °C temperature sensitivity of this on-chip thermometer; the subtraction of the current I_{CTAT} and I_{PTAT} multiply by factor of 10 for comparison with the output signal: analytical result (red) and simulations (blue). Bottom: The discrepancy between the output and the analytical expression (red), and between the output and the simulation (blue), both have been multiplied by 10.

5.1. Transistor Model Specified Temperature

Simulations exhibited in Fig. 5 and Fig. 6. are done using the IHP design KIT which procures transistors model. These models NPN 13v2 are made for a typical use around room temperature. However, even if -200 °C and 200 °C are far from the usual temperature operation of an ASIC, the observed deviations are probably not only due to the transistor model.

5.2. Simplified Analytical Expression

Deviations between the analytical model and simulation can be due to non-representative simulation or analytical models. Indeed, we describe in this paper the ingredients of our analytical model, which could be improved by including parasitic resistances, non-ideality factors, self-heating, etc.

5.3. Nonlinearities Far from Setting Point

For a given R_{PTAT} and R_{CTAT}, the thermometer is set to provide zero differential current at a given temperature; here, 50 °C as illustrated in Fig. 5. Far from this setting point, the current in the circuit starts to be unbalanced, until even becoming zero on one branch. This seems the most credible reason of the saturations at output current > |2mA| of the thermometer.

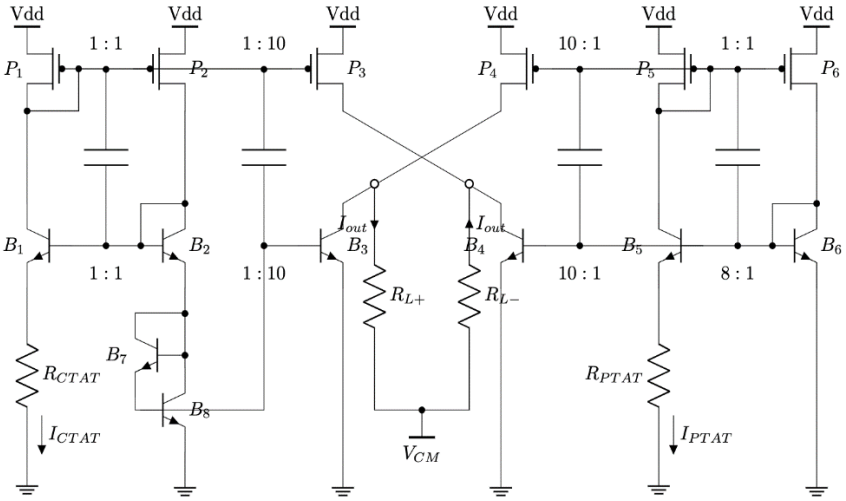

Fig. 6. Thermometer schematic including the PTAT (right), CTAT (left) and crossing bridge subtracting the currents (middle).

6. Conclusion

The suggested on-chip thermometer exhibits a linear response across an extensive temperature range from -150 °C to 150 °C. The sensitivity of this thermometer is adaptable through modifications in the M factor, R_{PTAT}, and R_{CTAT} values. Additionally, the zero offset temperature is adjustable by varying the ratio R_{PTAT}/R_{CTAT}. This enables the optimization of the temperature range centered around a specific temperature. This paper introduces a set of parameters enabling coverage of up to a 300 °C range around 50 °C.

Acknowledgment

This work is supported by the Institut National de Physique Nucléaire et de Physique des Particules (IN2P3) of the Centre National de la Recherche Scientifique (CNRS), the Centre National d'Etudes Spatiales (CNES), and the BiCMOS R&T.

References

[1]. S. Ma, M. Jiang, P. Tao, C. Song, J. Wu, J. Wang, T. Deng, W. Shang, Temperature effect and thermal impact in lithium-ion batteries: A review, *Progress in Natural Science: Materials International*, Vol. 28, Issue 6, 2018, pp. 653-666.

[2]. S. I. Kim, M. Im, E. Cho, H. Jang, S. Y. Jang, D. W. Kim, K. W. Kim, I. Heo, Y. J. Kim, J. H. Lee, Effects of thermal aging on the electronic and structural properties of Pt-Pd and toluene oxidation activity, *Science of the Total Environment*, Vol. 847, 2022, 157482.

[3]. S. Arar, High-temperature Aging Method to Evaluate Electronic Component Aging and Stability. Technical Articles, https://www.allaboutcircuits.com/technical-articles/introduction-to-high-temperature-accelerated-aging-for-evaluating-the-electronic-component-stability-and-aging/

[4]. Y. Li, J. He, Z. Xie, D. Jiang, Y. Li, Frontier development of chips design and production, *Procedia Computer Science*, Vol. 139, 2018, pp. 554-560.

[5]. S. Im, K. Banerjee, Full chip thermal analysis of planar (2-D) and vertically integrated (3-D) high performance ICs, *Tech. Dig. IEDM*, 2000, pp. 727-730.

[6]. B. Ton, S. Chen, D. Prêle, M. Gonzalez, High Sensitivity On-chip BiCMOS Thermometer with Differential Output and Offset Nulling, in *Proceedings of the 5th International Conference on Microelectronic Devices and Technologies (MicDAT'23)*, Funchal, Portugal, 20-22 September 2023, pp. 47-51.

[7]. VLSI Interconnects – Course, https://onlinecourses.nptel.ac.in/noc22_ee125/preview#:~:text = Interconnects%20are%20the%20wired%20connections,connection%20cannot%20be%20ignored%20anymore

[8]. R. K. Kamat, G. M. Naik, Thermistors – in search of new applications, manufacturers cultivate advanced NTC techniques, *Sensor Review*, Vol. 22, Issue 4, 2002, pp. 334-340.
[9]. G. Prasad, Band-Gap Reference, 2018. https://www.researchgate.net/publication/328364212_Band-Gap_Reference
[10]. R. Singh, R. Mehra, Qualitative Analysis of Darlington Feedback Amplifier at 45nm Technology, *Bulletin of Electrical Engineering and Informatics*, Vol. 7, 2018, pp. 21-27.
[11]. P. R. Gray, R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Ed., *John Wiley Sons, Inc*., 1990
[12]. S. M. Sze, Physics of Semiconductor Devices, *Wiley*, New York, 1981.
[13]. C. Kittel, Introduction to Solid State Physics, 8th Ed, *Wiley*, New York, 2005.
[14]. S Chen, Radiation-hardened mixed-signal ASICs design for space observatories, PhD Thesis, *Université Paris Cité*, 2019.
[15]. B. Van Zeghbroeck, Principles of Semiconductor Devices, *University of Colorado*, 2023.