Electronics and Electrical Engineering

AIMS Electronics and Electrical Engineering, 7(4): 322–336.
DOI: 10.3934/electreng.2023017
Received: 24 August 2023
Revised: 05 October 2023
Accepted: 12 October 2023
Published: 19 October 2023

http://www.aimspress.com/journal/ElectrEng

Research article

Analytical model of subthreshold swing in junctionless gate-all-around (GAA) FET with ferroelectric

Hakkee Jung*

Department of Electronic Eng., Kunsan National University, Gunsan-si, Jeollabuk-do, 54150, Republic of Korea

* **Correspondence:** Email: hkjung@kunsan.ac.kr; Tel: +82-63-469-4684; Fax: +82-63-469-7431.

Abstract: An analytical SS model is presented to observe the subthreshold swing (SS) of a junctionless gate-all-around (GAA) FET with ferroelectric in this paper. For the gate structure, a multilayer structure of metal-ferroelectric-metal-insulator-semiconductor (MFMIS) was used, and the SS was calculated in $15 \le P_r \le 30\,\mu C/cm^2$ and $0.8 \le E_c \le 1.5\,MV/cm$, which are the ranges of remanent polarization and coercive field suggested in various experiments in the case of HZO as the ferroelectric material. It was found that the SSs from the presented analytical SS model agree well with those derived from the relationship between drain current and gate voltage using a 2D potential distribution in the range of device parameters used for simulation. As a result of analyzing the SS of the junctionless GAA FET with ferroelectric using the analytical SS model presented in this paper, the SS decreased because the voltage across the inner gate decreased when the ferroelectric thickness increased. It was observed that the condition of SS < 60 mV/dec was sufficiently obtained according to changes in device parameters such as channel length, channel radius and ferroelectric thickness, and that the SS maintained a constant value according to the ratio of remanent polarization and coercive field P_r/E_c. As P_r/E_c increases, the SS increases as the ferroelectric capacitance increases. As the channel length becomes smaller, the change in SS according to P_r/E_c is more severe.

Keywords: subthreshold swing; junctionless; gate-all-around (GAA); ferroelectric; remanent polarization; coercive field

1. Introduction

The planar-type MOSFETs are no longer available due to Short Channel Effects (SCEs), such as

an increase in subthreshold swing, off-current, threshold voltage roll-off and Drain Induced Barrier Lowering (DIBL) as the transistor size decreases [1–3]. The FinFET structure, which is a tri-gate structure used to solve this problem, also has limitations in scaling, so a transistor with a new structure has been developed [4–6]. In particular, FinFET using ferroelectric was developed to solve the increase in power consumption, which is the most problematic due to the reduction in transistor size, which is indispensable for high-speed operation [7,8]. Also, a Gate-All-Around (GAA) FET is being developed as a next-generation transistor structure to overcome the limitations of FinFETs [9,10]. The GAA FET has a structure that maximizes the ability of the gate to control the channel carrier, and numerous studies are currently being conducted on these devices [11,12]. In particular, the junctionless structure [13,14], which makes the doping concentration of the channel and the source/drain region almost the same, is applied to the GAA FET structure as a structure that can solve the difficulty of manufacturing due to the reduction in transistor size [15–17].

In addition, to achieve low power consumption, it is also necessary to reduce the subthreshold swing (SS). To overcome the limit of 60 mV/dec for the SS, ferroelectric materials are used, for which Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structures and Metal-Ferroelectric-Metal-Insulator-Semiconductors (MFMIS) are mainly used [18,19]. Compared to the MFMIS structure, the stability of the ferroelectric material in the MFIS structure is independent of the gate leakage current, but gate leakage is ignored in this paper, so an analytical model of subthreshold swing is presented for the junctionless GAA FET of the MFMIS structure with high on-current. Research has been conducted extensively on junction-based MFIS-structured GAA FETs [20,21], but little has been done on junctionless MFMIS-structured GAA FETs.

Rassekh et al. analyzed SCEs such as the SS and DIBL for a channel length of 100 nm for the MFMIS-structured double-gate junctionless FET with ferroelectric [22]. It was found that the change of SS for the ferroelectric thickness could not be observed in the deep subthreshold region when the channel length was about 100 nm. Pahwa et al. analyzed the threshold voltage roll-off, SS, DIBL, etc. up to 10 nm channel length for undoped channel double gate FETs with MFIS and MFMIS structures, but they only used numerical simulation [23]. Sakib et al. analyzed SCEs for ferroelectric GAA FETs, but only numerically simulated junction-based MFIS and MFMIS structures [24]. Choi et al. and Raut et al. analyzed SCEs for junctionless GAA FET using ferroelectric, but only used TCAD [25,26]. Mehta et al., Gaidhane et al. and Kim et al. analyzed the current-voltage characteristics of the ferroelectric MFIS structure, but analyzed only one-dimensionally for the channel radial direction of the long-channel, so the change of SS occurring in the short channel could not be interpreted [27–29]. It is necessary, however, to analyze not only the potential distribution along the radial direction of the channel but also along the channel length direction as the size of the transistor decreases. To this end, it is necessary to solve the two-dimensional Poisson equation in the GAA structure. In addition, in the junctionless GAA structure using ferroelectric, it is necessary to know how the charge in the ferroelectric changes according to the gate voltage to interpret the SS in the junctionless GAA FET with ferroelectric. Therefore, in this paper, we will find the solution of Poisson's equation two-dimensionally for the junctionless GAA FET of cylindrical structure with ferroelectric, and derive the drain current-gate voltage relationship using it. From the current-voltage relationship obtained in this way, we will find SS according to the definition of SS and compare it with the value of the analytical SS model presented. Ferroelectric will use the properties of HZO and will use the MFMIS structure, which has been proven in many experiments [30,31]. In addition, we will use the relationship between ferroelectric voltage, inner voltage and outer voltage by the LK (Landau-Khalatnikov) equation.

2. MFMIS junctionless GAA FET with ferroelectric

2.1. Structure of junctionless GAA FET with ferroelectric and ferroelectric charge

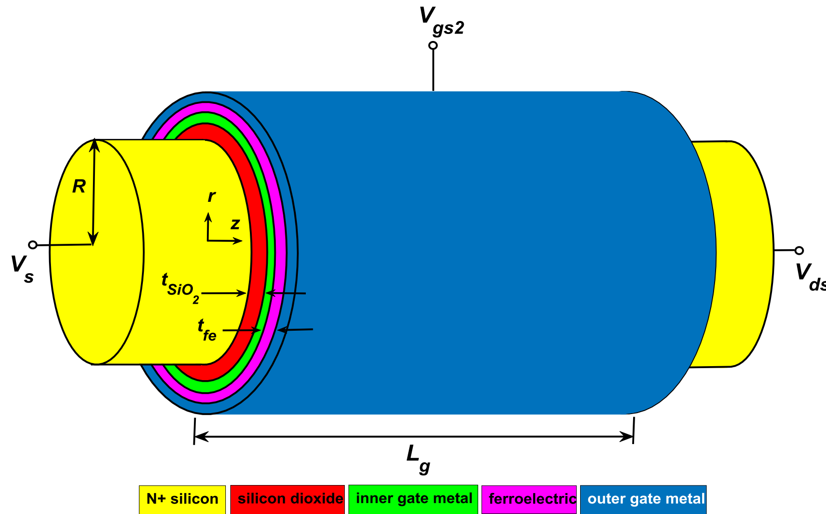

Figure 1. Schematic view of junctionless GAA FET with ferroelectric.

Figure 1 is the structure of the ferroelectric junctionless GAA FET used in this paper. As shown in Figure 1, the MFMIS structure was used and device parameters are shown in Table 1. Although not shown in Figure 1, V_{gs1} is the voltage induced to the inner gate metal, and V_{gs2} is the voltage applied to the outer gate metal.

Table 1. Device parameters for this analytical SS model.

Device parameter	Symbol	Value
Channel length	L_g	20~60 nm
Channel radius	R	5~10 nm
SiO_2 thickness	t_{ox}	1~2 nm
Doping concentration	N_d	10^{18} /cm^3
Ferroelectric thickness	t_{fe}	0~10 nm
Remanent polarization	P_r	15~30 μC/cm^2
Coercive field	E_c	0.8~1.5 MV/cm

To obtain the potential distribution within the channel of a MOSFET with a GAA structure, Li's two-dimensional potential model for the r and z directions was used [32]. In other words, the potential in the channel can be obtained as the sum of the one-dimensional solution $\phi_1(r)$ of Poisson's equation and the two-dimensional solution $\phi_2(r,z)$ of the homogeneous Laplace equation, as follows.

$$\phi(r,z) = \phi_1(r) + \phi_2(r,z)$$

$$\phi_1(r) = -\frac{qN_d}{4\varepsilon_{si}} r^2 + V_{gs} - \phi_{ms} + \frac{qN_d R}{2C_{ox}} + \frac{qN_d R^2}{4\varepsilon_{si}} \tag{2.1}$$

$$\phi_2(r,z) = \sum_{n=1}^{\infty}\left[C_n \exp\left(\frac{\alpha_n z}{R}\right) + D_n \exp\left(-\frac{\alpha_n z}{R}\right)\right] J_0\left(\frac{\alpha_n r}{R}\right) \tag{2.2}$$

where α_n is an eigenvalue that satisfies (2.3). Refer to the C_n and D_n in [32]

$$RJ_0(\alpha_n) - \frac{\varepsilon_{si}}{C_{ox}} \alpha_n J_1(\alpha_n) = 0 \tag{2.3}$$

To find the charge in the ferroelectric, the charge in the channel must first be obtained from the relational expression of (2.4).

$$Q_{sc} = -C_{ox}(V_{gs1} - \phi_{ms} - \phi_s) \tag{2.4}$$

At this time, the surface potential ϕ_s can be obtained as the following (2.5) by substituting $r = R$ into (2.1) and (2.2).

$$\varphi_s(z) = \varphi_1(R) + \varphi_2(R,z) \tag{2.5}$$

$$\phi_1(R) = -\frac{qN_d}{4\varepsilon_{si}} R^2 + V_{gs1} - \phi_{ms} + \frac{qN_d R}{2C_{ox}} + \frac{qN_d R^2}{4\varepsilon_{si}} = V_{gs1} - \phi_{ms} + \frac{qN_d R}{2C_{ox}}$$

$$\begin{aligned}\phi_2(R,z) &= \sum_{n=1}^{\infty}\left[C_n \exp\left(\frac{\alpha_n z}{R}\right) + D_n \exp\left(-\frac{\alpha_n z}{R}\right)\right] J_0\left(\frac{\alpha_n R}{R}\right) \\ &= \sum_{n=1}^{\infty}\left[C_n \exp\left(\frac{\alpha_n z}{R}\right) + D_n \exp\left(-\frac{\alpha_n z}{R}\right)\right] J_0(\alpha_n)\end{aligned}$$

where ϕ_{ms} is the work function difference between the gate metal and semiconductor. Substituting (2.5) into (2.4), the charge in the channel Q_{sc} can be obtained as shown in (2.6) below.

$$Q_{sc} = C_{ox}\left\{\frac{qN_d R}{2C_{ox}} + \sum_{n=1}^{\infty}\left[C_n \exp\left(\frac{\alpha_n z}{R}\right) + D_n \exp\left(-\frac{\alpha_n z}{R}\right)\right] J_0(\alpha_n)\right\} \tag{2.6}$$

Using (2.6), the ferroelectric charge Q can be obtained from (2.7).

$$2\pi R L_g \times Q = -\int_0^{L_g} \pi R Q_{sc}\, dz \tag{2.7}$$

Here, the ferroelectric charge can be derived as in (2.8).

$$Q = -\frac{1}{2L_g}\int_0^{L_g} Q_{sc} dz$$
$$= -\frac{qN_d R}{4} - \frac{C_{ox}}{2L_g}\left[\sum_{n=1}^{\infty}\left[C_n \exp\left(\frac{\alpha_n L_g}{R}\right) - D_n \exp\left(-\frac{\alpha_n L_g}{R}\right) - C_n + D_n\right]\left(\frac{R}{\alpha_n}\right) J_0\left(\alpha_n\right)\right] \quad (2.8)$$

Using the ferroelectric charge Q, the ferroelectric voltage V_f can be obtained from the following (2.9) by Landau theory.

$$V_f = 2\alpha t_f Q + 4\beta t_f Q^3 + 6\gamma t_f Q^5 \quad (2.9)$$

$$\alpha = -\frac{3\sqrt{3}}{4}\frac{E_c}{P_r}\ (m/F)$$
$$\beta = \frac{3\sqrt{3}}{8}\frac{E_c}{P_r^3}\ (m^5/F/C^2)$$
$$\gamma = 0$$

where P_r is the remanent polarization of the ferroelectric material and E_c is the coercive field. As shown in Table 1, the values of P_r and E_c were within the range derived from various papers in the case of HZO [33−36]. Using the ferroelectric voltage V_f derived in this way, the relationship between inner gate voltage V_{gs1} and outer gate voltage V_{gs2} can be expressed as in (2.10) below.

$$V_{gs2} = V_{gs1} + V_f \quad (2.10)$$

Using (2.1) and (2.2), the relationship between drain current and gate voltage can be derived by the following (2.11).

$$I_d = \frac{2\pi N_d \mu_n kT\left\{1 - \exp\left(\frac{-qV_{ds}}{kT}\right)\right\}}{\int_0^{L_g}\frac{1}{\int_0^R r\exp\left\{\frac{q\phi(r,z)}{kT}\right\}dr}} \quad (2.11)$$

The relationship between drain current and gate voltage obtained using (2.11) is shown in Figure 2(a). As can be seen in Figure 2(a), it was found to be in good agreement with the ISE-TCAD result at t_{fe} = 0, and in Figure 2(b), it was observed that the SS decreased as the ferroelectric thickness increased. In this paper, we propose an analytical SS model consistent with the two-dimensional SS derived in Figure 2.

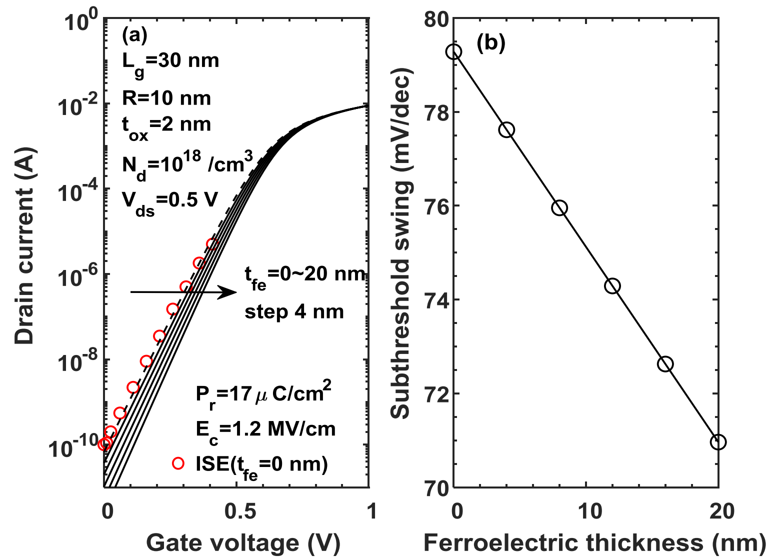

Figure 2. (a) Drain current vs. gate voltage curves with the ferroelectric thickness as a parameter and (b) subthreshold swing derived from the slope of drain current vs. gate voltage curves under the given conditions in the figure.

2.2. Analytical subthreshold swing of junctionless GAA FET with ferroelectric

To obtain the analytical SS model, the SS can be expressed in the following (2.12) by the definition of SS.

$$SS = \frac{\partial V_{gs2}}{\partial(\log I_{ds})} = \ln(10)\left(\frac{kT}{q}\right)\left(\frac{\partial \phi_{\min}}{\partial V_{gs2}}\right)^{-1} = \ln(10)\left(\frac{kT}{q}\right)\left[\frac{\partial \phi(0, z_{\min})}{\partial V_{gs2}}\right]^{-1} \tag{2.12}$$

Here, $r = 0$ is substituted since most carriers move along the central axis of the channel in the junctionless structure, and $z = z_{\min}$, which has the minimum potential value, is substituted [37]. In (2.12), the parenthesis of the last term is as follows.

$$\begin{aligned}
\frac{\partial \phi(0, z_{\min})}{\partial V_{gs2}} &= \frac{\partial}{\partial V_{gs2}}\left\{\sum\left[C_n \exp\left(\alpha_n z_{\min}/R\right) + D_n \exp\left(-\alpha_n z_{\min}/R\right)\right] J_0(0) + \phi_1(0)\right\} \\
&= \frac{\partial}{\partial V_{gs2}}\left\{\sum\left[C_n \exp\left(\alpha_n z_{\min}/R\right) + D_n \exp\left(-\alpha_n z_{\min}/R\right)\right]\right\} + \frac{\partial \phi_1(0)}{\partial V_{gs2}} \qquad \left\{\because J_0(0) = 1\right\} \\
&= \frac{\partial \phi_1(0)}{\partial V_{gs1}} \frac{\partial V_{gs1}}{\partial Q} \frac{\partial Q}{\partial V_{gs2}} + \sum\left[\begin{array}{l} \exp\left(\alpha_n z_{\min}/R\right)\dfrac{\partial C_n}{\partial V_{gs2}} + C_n \dfrac{\partial}{\partial V_{gs2}}\left\{\exp\left(\alpha_n z_{\min}/R\right)\right\} \\ + \exp\left(-\alpha_n z_{\min}/R\right)\dfrac{\partial D_n}{\partial V_{gs2}} + D_n \dfrac{\partial}{\partial V_{gs2}}\left\{\exp\left(-\alpha_n z_{\min}/R\right)\right\} \end{array}\right] \\
&= \frac{\partial V_{gs1}}{\partial Q} \frac{\partial Q}{\partial V_{gs2}} + \sum\left[\begin{array}{l} \exp\left(\alpha_n z_{\min}/R\right)\dfrac{\partial C_n}{\partial V_{gs2}} + C_n \dfrac{\partial}{\partial V_{gs2}}\left\{\exp\left(\alpha_n z_{\min}/R\right)\right\} \\ + \exp\left(-\alpha_n z_{\min}/R\right)\dfrac{\partial D_n}{\partial V_{gs2}} + D_n \dfrac{\partial}{\partial V_{gs2}}\left\{\exp\left(-\alpha_n z_{\min}/R\right)\right\} \end{array}\right] \left\{\because \frac{\partial \phi_1(0)}{\partial V_{gs1}} = 1\right\}
\end{aligned} \tag{2.13}$$

The derivative of each term for V_{gs2} in (2.13) can be obtained using the parametric differentiation method indicated in the Appendix. Using the formula in the Appendix, the SS can be obtained analytically.

To obtain the analytical SS model, the value of n=1 had to be used when calculating the z_{min} value in the Appendix. To prove its validity, the deviation of SSs calculated for $n = 1$ and $n = 32$ (the number of n that satisfies (2.3) when the maximum of α is 100) is shown in Figure 3 according to the ratio of the channel length and radius, L_g/R. As shown in Figure 3, the deviation increased as the ratio of channel length and radius decreased, and the deviation was less than 1% regardless of the ferroelectric thickness for $L_g/R > 3$. In particular, it was found that it is sufficient to calculate only the case of $n = 1$ when calculating this analytical SS model as the ferroelectric thickness decreases. In general, it will be sufficient to calculate only the case of $n = 1$ since $L_g/R > 2$.

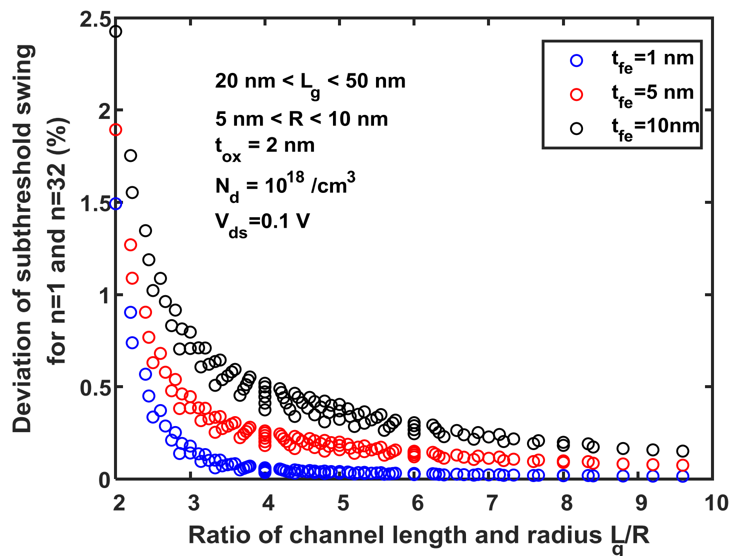

Figure 3. Deviation of SS for $n = 1$ and $n = 32$ for the ratio of channel length and radius with the ferroelectric thickness as a parameter under the given conditions in the figure.

3. Results and discussions

3.1. Verification of the analytical SS model

In Figure 4, the results of the analytical SS model in the case of $n = 1$ presented in this paper, the SS derived from the relationship between drain current and gate voltage in (2.11) and the 3D ISE-TCAD simulation value [32] calculated at $t_{fe} = 0$ nm were compared. As shown in Figure 4, it can be seen that the SS proposed in this paper is reasonable.

To compare the change of SS according to the ferroelectric thickness with the case of using the analytical SS model of this paper and the SS derived from the slope in the subthreshold region of the drain current and gate voltage curve of (2.11), the SSs are shown with the channel length as a parameter in Figure 5. At this time, to maintain the deviation of less than 1%, it was calculated for the case of $L_g/R > 4$. As can be seen in Figure 5, the SSs from the analytical SS model of this paper agree very well with the SSs derived from the curve of drain current and gate voltage using a 2D potential distribution. As can be observed in Figure 5, it can be seen that the difference between the

two values increases as L_g/R decreases. As mentioned in Figure 2(b), the SS decreased as the ferroelectric thickness increased and the change in SS due to the change in ferroelectric thickness decreased as the channel length increased. In particular, SS $<$ 60 mV/dec was exhibited when the channel length was 40 nm or more under the given conditions.

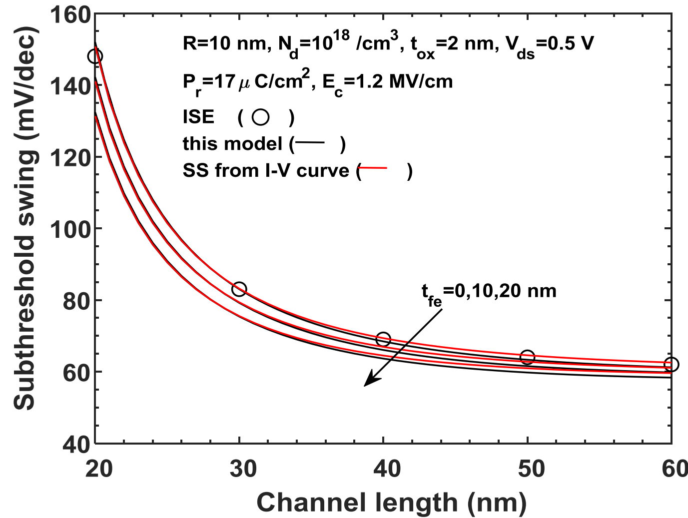

Figure 4. Comparison of SSs from this model and drain current vs. gate voltage curveand ISE-TCAD with the ferroelectric thickness as a parameter under the given conditions in the figure.

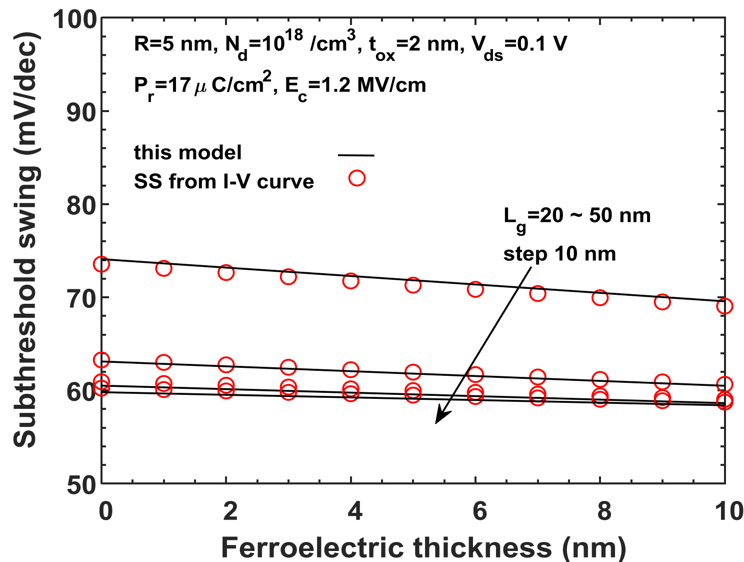

Figure 5. Comparison of SSs from this model and drain current vs. gate voltage curve with the channel length as a parameter under the given conditions in the figure.

To compare the change of SS with the change of channel radius, Figure 6 shows the change of SS while changing the channel radius R from 5 nm to 10 nm when the channel length is 30 nm under the given conditions. Based on Figure 6, it can be observed that the results of the 2D calculation and the analytical SS model are in good agreement. Since it is in the range of 3 $< L_g/R <$ 6, even if n = 1 was used, the value could be obtained within the deviation range of less than 1%. As the channel radius R increases, SS increases, and it can be observed that the increasing rate ($\Delta SS / \Delta R$)

increases as R increases. In particular, it was found that the case of R = 5 nm, that is, the case of L_g/R = 6, matches very well. Therefore, the analytical SS model of this paper will be very useful.

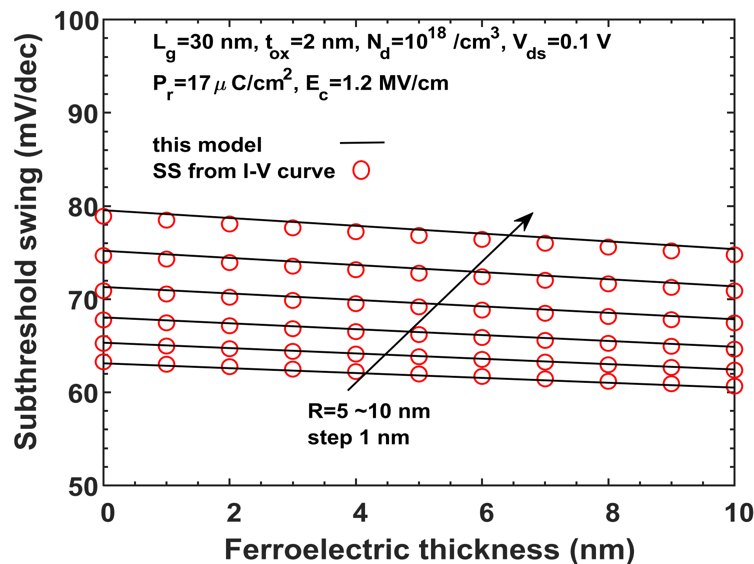

Figure 6. Comparison of SSs from this model and drain current vs. gate voltage curve with the channel radius as a parameter under the given conditions in the figure.

3.2. SS for remanent polarization and coercive field

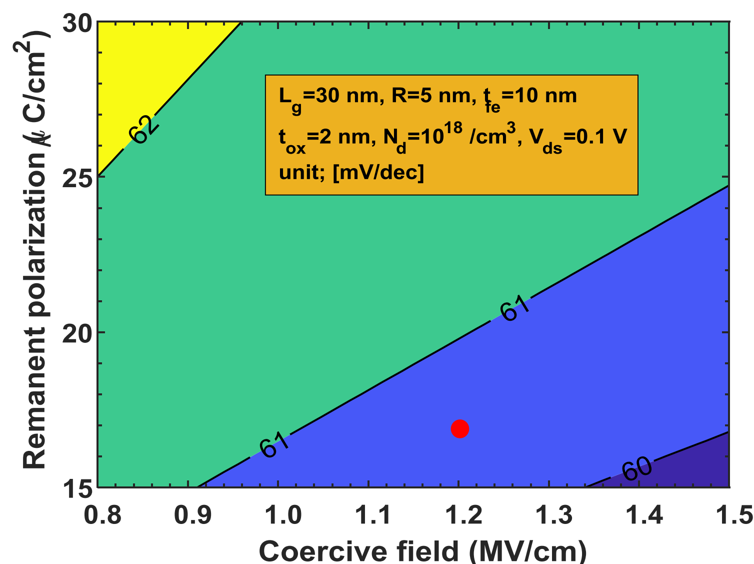

Figure 7. Contours of SSs for remanent polarization and coercive field at L_g = 30 nm under the given conditions in the figure.

As shown in Figure 5, it can be seen that SS > 60 mV/dec if L_g < 30 nm under the given conditions. This is the case of remanent polarization $P_r = 17\,\mu C/cm^2$ and coercive field E_c = 1.2 *MV/cm*, as shown in Figure 5. The remanent polarization and coercive field values are important factors that determine the hysteresis characteristics of ferroelectric materials, and it is known that the SS value is proportional to the absolute value $|C_{fe}|$ of the capacitance of ferroelectric materials [38].

Figure 7 shows the contours of SS for the change of P_r and E_c when the channel length is 30 nm while keeping the device parameters the same as in Figure 5. The red dot in Figure 7 shows the SS value calculated under the conditions of Figure 5. As can be seen in Figure 7, the SS decreases as the remanent polarization decreases and the coercive field increases, and it can be observed that a region of SS < 60 mV/dec appears in the range of $15 \le P_r \le 16.8\,\mu C/cm^2$ and $1.34 \le E_c \le 1.5\,MV/cm$. It can be seen that there is a relationship of $|C_{fe}| \propto P_r/E_c$. Therefore, if P_r and E_c satisfying the condition of SS < 60 mV/dec are used, SS < 60 mV/dec can be obtained even if the channel length is shortened.

As shown in Figure 5, the SS shows a relatively large value of SS > 70 mV/dec when the channel length is 20 nm. To obtain the condition of SS < 60 mV/dec, after reducing R = 3 nm and t_{ox} = 1 nm, the contour plot for P_r and E_c is shown in Figure 8. As can be seen in Figure 8, it can be observed that the SS < 60 mV/dec appears in the range of $15 \le P_r \le 23\,\mu C/cm^2$ and $0.95 \le E_c \le 1.5\,MV/cm$. As such, it can be observed that if the channel radius R and the oxide thickness t_{ox} are reduced, device parameters satisfying the value of SS < 60 mV/dec can be obtained even when the channel length is about 20 nm. However, the models for the quantum and tunneling effect are required when the channel length is less than 10 nm or the channel diameter is reduced to 7 nm [39–43], but further research on this should be conducted.

Observing Figures 7 and 8, it can be seen that the contours have a relationship of P_r = aE_c (a is a proportionality constant) to maintain a constant SS value. That is, it can be seen that the SS according to a certain P_r/E_c value is constant. To observe this, Figure 9 shows the change of SS for the change of P_r/E_c value with the channel length as a parameter. As can be seen in Figure 9, it can be seen that the SS is plotted as a single value when P_r/E_c is determined in a given channel length. As mentioned in this section, the SS increases as the value of $|C_{fe}|$ increases if P_r/E_c increases. It can be seen that the change of SS is relatively large according to P_r/E_c when the channel length is relatively short, 20 nm. As the channel length increased, the changing rate of SS for P_r/E_c decreased, and as P_r/E_c increased, the changing rate of SS for the channel length increased. Note that the SS is almost identical at P_r/E_c = 10 pF/cm for channel lengths of 30 nm and 40 nm.

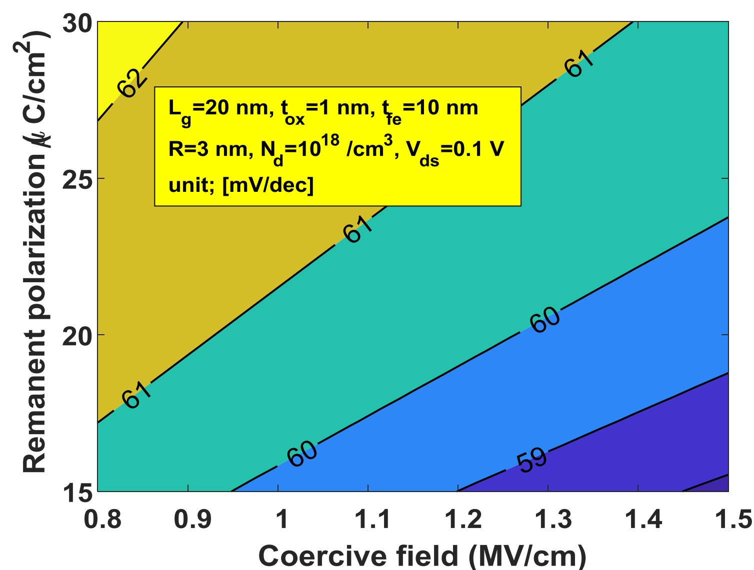

Figure 8. Contours of SSs for remanent polarization and coercive field at L_g=20 nm under the given conditions in the figure.

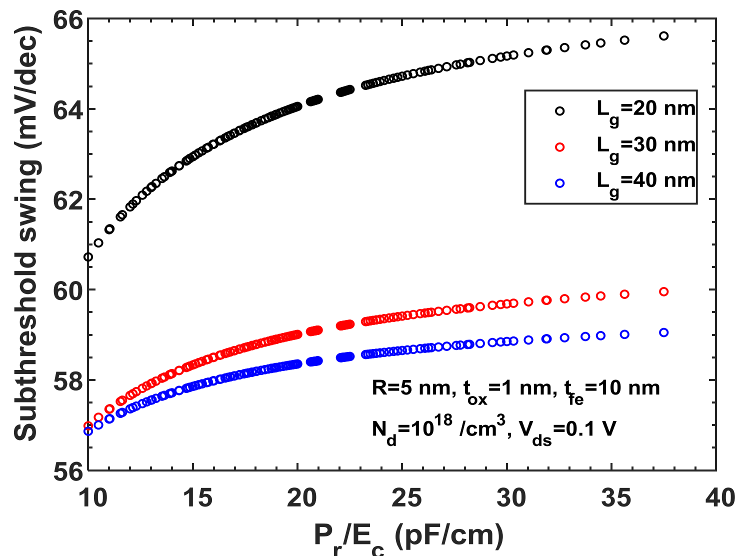

Figure 9. SSs for the ratio of the remanent polarization and coercive field P_r/E_c with the channel length as a parameter under the given conditions in the figure.

4. Conclusions

In this paper, an analytical SS model was presented to analyze the SS for junctionless GAA FET with ferroelectric. It has been found that the analytical SS model is valid since the SS value derived from the relation between drain current and gate voltage using a 2D potential distribution agrees well with the analytical SS model proposed here. In the case of the potential distribution represented by the Fourier-Bessel series in this paper, the case of $n = 1$ is dominant, so compared to the case of using $n = 32$, $n = 1$ could be used with a deviation of less than 1% according to the given conditions. As a result of SS analysis of junctionless GAA FET with ferroelectric using this analytical SS model, when the ferroelectric thickness increases at the same outer gate voltage, the voltage applied to the inner gate decreases as the voltage applied to the ferroelectric increases, and the flowing drain current decreases and SS also decreases. As the channel length increased, the change of SS according to the change of ferroelectric thickness relatively decreased. The decrease in channel radius results in a relatively greater ferroelectric thickness, resulting in a decrease in SS. As such, it can be seen that the SS value changes according to the relationship between the channel dimension and the ferroelectric thickness, and a result of SS < 60 mV/dec could be derived according to the device parameters when the ratio P_r/E_c between the remanent polarization P_r and the coercive field E_c decreases even in case of the channel length of 20 nm. In addition, it was found that the SS value was also constant at the given P_r/E_c. From the above results, it is judged that the analytical SS model presented in this paper can be used to analyze the SS of junctionless GAA FET with ferroelectric, and if the device parameters used in this paper are smaller, research on the quantum mechanical model should be conducted.

Supplementary: The derivative of each term

$$\frac{\partial C_n}{\partial V_{gs2}} = \frac{\partial C_n}{\partial V_{gs1}} \frac{\partial V_{gs1}}{\partial Q} \frac{\partial Q}{\partial V_{gs2}}$$

$$\frac{\partial D_n}{\partial V_{gs2}} = \frac{\partial D_n}{\partial V_{gs1}} \frac{\partial V_{gs1}}{\partial Q} \frac{\partial Q}{\partial V_{gs2}}$$

$$\frac{\partial C_n}{\partial V_{gs1}} = -\frac{2J_1(\alpha_n)}{\alpha_n[J_1^2(\alpha_n)+J_0^2(\alpha_n)]} \frac{\left[\exp\left(-\alpha_n L/R\right)-1\right]}{2\sinh\left(-\alpha_n L/R\right)}$$

$$\frac{\partial D_n}{\partial V_{gs1}} = -\frac{2J_1(\alpha_n)}{\alpha_n[J_1^2(\alpha_n)+J_0^2(\alpha_n)]} \frac{\left[1-\exp\left(\alpha_n L/R\right)\right]}{2\sinh\left(-\alpha_n L/R\right)}$$

$$\frac{\partial V_{gs1}}{\partial Q} = \left(\frac{\partial Q}{\partial V_{gs1}}\right)^{-1} = \left[-\frac{C_{ox}}{2L_g}\left[\sum_{n=1}^{\infty}\left[\frac{\partial C_n}{\partial V_{gs1}}\exp\left(\frac{\alpha_n L_g}{R}\right)-\frac{\partial D_n}{\partial V_{gs1}}\exp\left(-\frac{\alpha_n L_g}{R}\right)-\frac{\partial C_n}{\partial V_{gs1}}+\frac{\partial D_n}{\partial V_{gs1}}\right]\left(\frac{R}{\alpha_n}\right)J_0\left(\alpha_n\right)\right]\right]^{-1}$$

$$\frac{\partial Q}{\partial V_{gs2}} = \frac{1}{2\alpha t_{fe} + 12\beta t_{fe} Q^2 + 30\gamma t_{fe} Q^4 + \dfrac{\partial V_{gs1}}{\partial Q}}$$

$$\frac{\partial}{\partial V_{gs2}}\left[\exp\left(\alpha_n z_{\min}/R\right)\right] = \frac{\alpha_n}{R}\exp\left(\alpha_n z_{\min}/R\right)\frac{\partial z_{\min}}{\partial V_{gs2}}$$

$$\frac{\partial}{\partial V_{gs2}}\left[\exp\left(-\alpha_n z_{\min}/R\right)\right] = -\frac{\alpha_n}{R}\exp\left(-\alpha_n z_{\min}/R\right)\frac{\partial z_{\min}}{\partial V_{gs2}}$$

Here, the $z_{\min}$ and derivative of $z_{\min}$ for V_{gs2} can be obtained as the following.

$$z_{\min} = \left(\frac{R}{2\alpha_1}\right)\ln\left(\frac{D_1}{C_1}\right)$$

$$\frac{\partial z_{\min}}{\partial V_{gs2}} = \left(\frac{R}{2\alpha_1}\right)\frac{\partial}{\partial V_{gs2}}\left(\ln D_1 - \ln C_1\right)$$

$$= \left(\frac{R}{2\alpha_1}\right)\left(\frac{\partial \ln D_1}{\partial V_{gs1}}\frac{\partial V_{gs1}}{\partial Q}\frac{\partial Q}{\partial V_{gs2}} - \frac{\partial \ln C_1}{\partial V_{gs1}}\frac{\partial V_{gs1}}{\partial Q}\frac{\partial Q}{\partial V_{gs2}}\right) = \left(\frac{R}{2\alpha_1}\right)\left(\frac{\partial \ln D_1}{\partial V_{gs1}} - -\frac{\partial \ln C_1}{\partial V_{gs1}}\right)\left(\frac{\partial V_{gs1}}{\partial Q}\frac{\partial Q}{\partial V_{gs2}}\right)$$

$$\left(\frac{R}{2\alpha_1}\right)\left(\frac{\partial \ln D_1}{\partial V_{gs1}} - \frac{\partial \ln C_1}{\partial V_{gs1}}\right) = \left(\frac{R}{2\alpha_1}\right)\left(\frac{2J_1(\alpha_1)}{\alpha_1[J_1^2(\alpha_1)+J_0^2(\alpha_1)]}\right)\left[\frac{-\left[1-\exp\left(\alpha_1 L/R\right)\right]}{2D_1\sinh\left(-\alpha_1 L/R\right)} - \frac{-\left[\exp\left(-\alpha_1 L/R\right)-1\right]}{2C_1\sinh\left(-\alpha_1 L/R\right)}\right]$$

$$= \left(\frac{R}{4\alpha_1\sinh\left(-\alpha_1 L/R\right)}\right)\left(\frac{2J_1(\alpha_1)}{\alpha_1[J_1^2(\alpha_1)+J_0^2(\alpha_1)]}\right)\left[\frac{\left[\exp\left(\alpha_1 L/R\right)-1\right]}{D_1} + \frac{\left[\exp\left(-\alpha_1 L/R\right)-1\right]}{C_1}\right]$$

Use of AI tools declaration

The authors have not used Artificial Intelligence (AI) tools in the creation of this article.

Conflict of interest

The author declares that there is no conflicts of interest in this paper.

References

1. Ratnesh RK, Goel A, Kaushik G, Garg H, Singh M, Prasad B (2021) Advancement and challenges in MOSFET scaling. *Mat Sci Semicon Proc* 134: 106002. https://doi.org/10.1016/

j.mssp.2021.106002
2. Khanna VK (2016) Short-Channel Effects in MOSFETs. *Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies*, 73–93. https://doi.org/10.1007/978-81-322-3625-2_5
3. Zhang S (2020) Review of Modern Field Effect Transistor Technologies for Scaling. *Journal of Physics: Conference Series* 1617: 012054. https://doi.org/10.1088/1742-6596/1617/1/012054
4. Razavieh A, Zeitzoff P, Nowak EJ (2019) Challenges and Limitations of CMOS Scaling for FinFET and Beyond Architectures. *IEEE T Nanotechnol* 18: 999–1004. https://doi.org/10.1109/TNANO.2019.2942456
5. Saini G, Rana AK (2011) Physical Scaling Limits of FinFET Structure: A Simulation Study. *International Journal of VLSI & Communication Systems* 2: 26–35. https://doi.org/10.5121/vlsic.2011.2103
6. Hu VP, Chiu P, Sachid AB, Hu C (2017) Negative Capacitance Enables FinFET and FDSOI Scaling to 2 nm Node. *Electron Devices Meeting (IEDM)* 23.1.1–23.1.4. https://doi.org/10.1109/IEDM.2017.8268443
7. Chauhan V, Samajdar DP (2021) Recent Advances in Negative Capacitance FinFETs for Low-Power Applications: A Review. *IEEE T Ultrason Ferr* 68: 3056–3068. https://doi.org/10.1109/TUFFC.2021.3095616
8. Yan S, Wu C, Sun C, Lin YW, Yao YJ, Wu YC. (2022) Trench FinFET Nanostructure with Advanced Ferroelectric Nanomaterial HfZrO2 for Sub-60-mV/Decade Subthreshold Slope for Low Power Application. *Nanomaterials* 12: 2165. https://doi.org/10.3390/nano12132165
9. Mukesh S, Zhang J (2022) A Review of the Gate-All-Around Nanosheet FET Process Opportunities. *Electronics* 11: 3589. https://doi.org/10.3390/electronics11213589
10. Qin L, Li C, Wei Y, Hu G, Chen J, Li Y, et al. (2023) Recent Developments in Negative Capacitance Gate-All-Around Field Effect Transistors: A Review. *IEEE Access* 11: 14028–14042. https://doi.org/10.1109/ACCESS.2023.3243697
11. Shilov A (2022) Samsung Begins 3 nm Production: World's First Gate-All-Around Transistors. Available from: https://www.tomshardware.com/news/samsung-kicks-off-3nm-production-gate-all-around-fets-make-an-entrance
12. Batakala J, Dhar RS (2022) Effect of Channel Material on Performance Parameters of GAA MOSFET. *Journal of Nano- and Electronic Physics* 14: 02003. https://doi.org/10.21272/jnep.14(2).02003
13. Jazaeri F, Sallese JM (2018) *Modeling nanowire and double-gate junctionless field-effect transistors*, Cambridge University Press. https://doi.org/10.1017/9781316676899
14. Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, et al. (2010) Nanowire transistors without junctions. *Nature Nanotech* 5: 225–229. https://doi.org/10.1038/nnano.2010.15
15. Chaujar R, Yirak MG (2023) Sensitivity Investigation of Junctionless Gate-all-around Silicon Nanowire Field-Effect Transistor-Based Hydrogen Gas Sensor. *Silicon* 15: 609–621. https://doi.org/10.1007/ s12633-022-02242-0
16. Priyadarshani KN, Singh S, Mohammed MKA (2022) Gate-all-around junctionless FET based label-free dielectric/charge modulation detection of SARS-CoV-2 virus. *RSC Advances* 12: 9202–9209. https://doi.org/10.1039/d1ra08587e
17. Merad F, Guen-Bouazza A (2020) DC performance analysis of a 20 nm gate length n-type Silicon GAA junctionless (Si JL-GAA) transistor. *International Journal of Electrical and Computer Engineering* 10: 4043–4052. https://doi.org/10.11591/ijece.v10i4.pp4043-4052
18. Lee S, Chen H, Shen C, Kuo PY, Chung CC, Huang YE, et al. (2020) Effect of Seed Layer on Gate-All-Around Poly-Si Nanowire Negative-Capacitance FETs With MFMIS and MFIS

Structures: Planar Capacitors to 3-D FETs. *IEEE T Electron Dev* 67: 711−716. https://doi.org/10.1109/TED.2019.2958350
19. Lee S, Chen H, Shen C, Kuo PY, Chung CC, Huang YE, et al. (2019) Experimental Demonstration of Performance Enhancement of MFMIS and MFIS for 5-nmx12.5-nm Poly-Si Nanowire Gate-All-Around Negative Capacitance FETs Featuring Seed-Layer and PMA-Free Process. *2019 Silicon Nanoelectronics Workshop (SNW),* 1−2. https://doi.org/23919/SNW.2019.8782939
20. Sakib FI, Mullick FE, Shahnewaz S, Islam S, Hossain M (2020) Influence of device architecture on the performance of negative capacitance MFMIS transistors. *Semicond Sci Technol* 35: 025005. https://doi.org/10.1088/1361-6641/ab5b76
21. Thoti N, Li Y (2022) Design of GAA Nanosheet Ferroelectric Area Tunneling FET and Its Significance with DC/RF Characteristics Including Linearity Analyses. *Nanoscale Res Lett* 17: 53. https://doi.org/10.1186/s11671-022-03690-8
22. Rassekh A, Sallese J, Jazaeri F, Fathipour M, Ionescu AM (2020) Negative Capacitance Double-Gate Junctionless FETs: A Charge-Based Modeling Investigation of Swing, Overdrive and Short Channel Effect. *IEEE J Electron Devi* 8: 939−947. https://doi.org/10.1109/JEDS.2020.3020976
23. Pahwa G, Agarwal A, Chauhan YS (2018) Numerical Investigation of Short-Channel Effects in Negative Capacitance MFIS and MFMIS Transistors: Subthreshold Behavior. *IEEE T Electron Dev* 65: 5130−5136. https://doi.org/109/TED.2018.2870519
24. Sakib FI, Hasan MA, Hossain M (2020) Exploration of Negative Capacitance in Gate-All-Around Si Nanosheet Transistors. *IEEE T Electron Dev* 67: 5236−5242. https://doi.org/ 10.1109/TED.2020.3025524
25. Raut P, Nanda U, Panda DK (2022) RF with linearity and non-linearity parameter analysis of gate all around negative capacitance junction less FET (GAA-NC-JLFET) for different ferroelectric thickness. *Phys Scripta* 97: 105809. https://doi.org/10.1088/1402-4896/ac90fa
26. Choi Y, Hong Y, Shin C (2020) Device design guideline for junctionless gate-all-around nanowire negative-capacitance FET with HfO2-based ferroelectric gate stack. *Semicond Sci Technol* 35: 015011. https://doi.org/10.1088/1361-6641/ab5775
27. Mehta H, Kaur H (2017) Impact of interface layer and metal workfunction on device performance of ferroelectric junctionless cylindrical surrounding gate transistors. *Superlattices and Microstructures* 111: 194−205. https://doi.org/10.1016/j.spmi.2017.06.032
28. Gaidhane AD, Pahwa G, Verma A, Chauhan YS (2018) Compact Modeling of Drain Current, Charges and Capacitances in Long-Channel Gate-All-Around Negative Capacitance MFIS Transistor. *IEEE T Electron Dev* 65: 2024−2032. https://doi.org/10.1109/ TED.2018.2813059
29. Kim Y, Seon Y, Kim S, Kim J, Bae S, Yang I, et al. (2021) Analytical Current-Voltage Modeling and Analysis of the MFIS Gate-All-Around Transistor Featuring Negative-Capacitance. *Electronics* 10: 1177. https://doi.org/10.3390/electronics10101177
30. Lee S, Lee C, Kuo Y, Li S, Chao T (2021) Ultra Sub-5-nm Hf1-xZrxO2 for a Stacked Gate-All-Around Ferroelectric FET With Internal Metal Gate. *Journal of the Electron Devices Society* 9: 236−241. https://doi.org/10.1109/JEDS.2021.3056438
31. Zhao G, Wang X, Yip WH, Huy NTV, Coquet P, Haung M, et al. (2022) Ternary logics based on 2D ferroelectric-incorporated 2D semiconductor field effect transistors. *Front Mater* 9: 872909. https://doi.org/10.3389/fmats.2022.872909
32. Li C, Zhaung Y, Di S, Han R (2013) Subthreshold Behavior Models for Nanoscale Short-Channel Junctionless Cylindrical Surrounding-Gate MOSFETs. *IEEE T Electron Dev* 60: 3655−3662. https://doi.org/10.1109/TED.2013.2281395
33. Das D, Gaddam V, Jeon S (2020) Demonstration of High Ferroelectricity (Pr~29μC/cm2) in Zr Rich HfxZr1-O2 Films. *IEEE Electron Device Letters* 41: 34−37. https://doi.org/10.1109/

LED.2019.2955198

34. Das D, Buyantogtokh B, Gaddam V, Jeon S (2021) Influence of High-Pressure Annealing Conditions on Ferroelectric and Interfacial Properties of Zr-rich HfxZr1-xO2 Capacitors. *IEEE T Electron Dev* 68: 1996–2002. https://doi.org/10.1109/TED.2021.3061963
35. Chen K, Chen P, Wu Y (2017) Excellent reliability of ferroelectric HfZrOx free from wake-up and fatigue effects by NH3 plasma treatment. *2017 Symposium on VLSI Circuits,* T84−T85. https://doi.org/10.23919/VLSIC.2017.8008572
36. Dang Z, Lv S, Gao Z, Chen M, Xu Y, Jiang P, et al. (2022) Improved Endurance of $Hf_{0.5}Zr_{0.5}O_2$-based Ferroelectric Capacitor Through Optimizing the Ti-N Ratio in TiN Electrode. *Electron Device Letters* 43: 561−564. https://doi.org/10.1109/LED.2022.3153063
37. Jung H (2022) Analysis of subthreshold swing in junctionless cylindrical surrounding gate MOSFET using Gaussian doping profile. *International Journal of Advanced Technology and Engineering Exploration* 9: 1073−1082. https://doi.org/10.19101/IJATEE.2021.874994
38. Tu L, Wang X, Wang J, Meng X, Chu J (2018) Ferroelectric Negative Capacitance Field Effect Transistor. *Adv Electron Mater* 4: 1800231. https://doi.org/10.1002/aelm.201800231
39. Shafizade D, Shalchian M, Jazaeri F (2019) Ultrathin Junctionless Nanowire FET Model, Including 2-D Quantum Confinements. *IEEE T Electron Dev* 66: 4101−4106. https://doi.org/10.1109/TED.2019.2930533
40. Tamersit K, Jooq MKQ, Moaiyeri MH (2021) Analog/RF performance assessment of ferroelectric junctionless carbon nanotube FETs: A quantum simulation study. *Physica E: Low-dimensional Systems and Nanostructures* 134: 114915. https://doi.org/10.1016/j.physe.2021.114915
41. Pandey N, Pahwa G, Chauhan YS (2021) Addressing source to drain tunneling in extremely scaled Si-transistors using negative capacitance. *Solid State Electron* 186: 108189. https://doi.org/10.1016/j.sse.2021.108189
42. Kumar N, Purwar V, Awasthi H, Gupta R, Singh K, Dubey S (2021) Modeling the threshold voltage of core-and-outer gates of ultra-thin nanotube Junctionless-double gate-all-around (NJL-DGAA) MOSFETs. *Microelectron J* 113: 105104. https://doi.org/10.1016/j.mejo.2021.105104
43. Kumar A, Tiwari PK, Roy JN (2022) Subthreshold model of asymmetric GAA junctionless FETs with scaled equivalent oxide thickness. *Microelectron J* 126: 105490. https://doi.org/10.1016/j.mejo.2022.105490

AIMS Press

© 2023 the Author(s), licensee AIMS Press. This is an open access article distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/4.0)