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BASIC LOGIC ELEMENT OF A FIELD PROGRAMMABLE GATE ARRAY

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Annotation. The article deals with the basic architecture of programmable logic integrated circuits and basic logic element, part of its main component - configurable logic block. Electrical functional circuit of the basic logic element with the ability to perform the sum operation was designed. On the basis of the functional diagram the RTL-representation of the basic logic element was obtained and the results of its modeling are presented.

Keywords: FPGA, basic logic element, computer-aided design, register transfer level.

Logic blocks. Field programmable gate arrays (FPGAs) are devices that can be electrically programmed to implement any type of digital circuit or system. The simplest structure of an FPGA consists of multiple configurable logic blocks (CLBs), an interconnection network, and input/output blocks as shown in Figure 1. The CLBs are used to perform combinational and sequential operations. Combinational logic uses a set of lookup tables (LUTs) as generators of arbitrary logic functions, and sequential logic uses a set of D flip-flops. Some advanced forms of CLBs support additional functions such as local data storage (distributed memory), multiplexer, and adder [1].

The flexibility of an FPGA stems from its core component, the CLB, which enables logical operations and data storage. Each CLB is formed by a set of *N* basic logic elements (BLEs). A BLE is a *K*-input LUT whose output can be routed to any other LUT input with or without a stored value in the storage element. Each BLE has *I* inputs coming from the outputs of other BLEs or from external signals. All parameters *N*, *K* and *I* can be set by the FPGA designer. The FPGA performance is determined by these parameters [2].

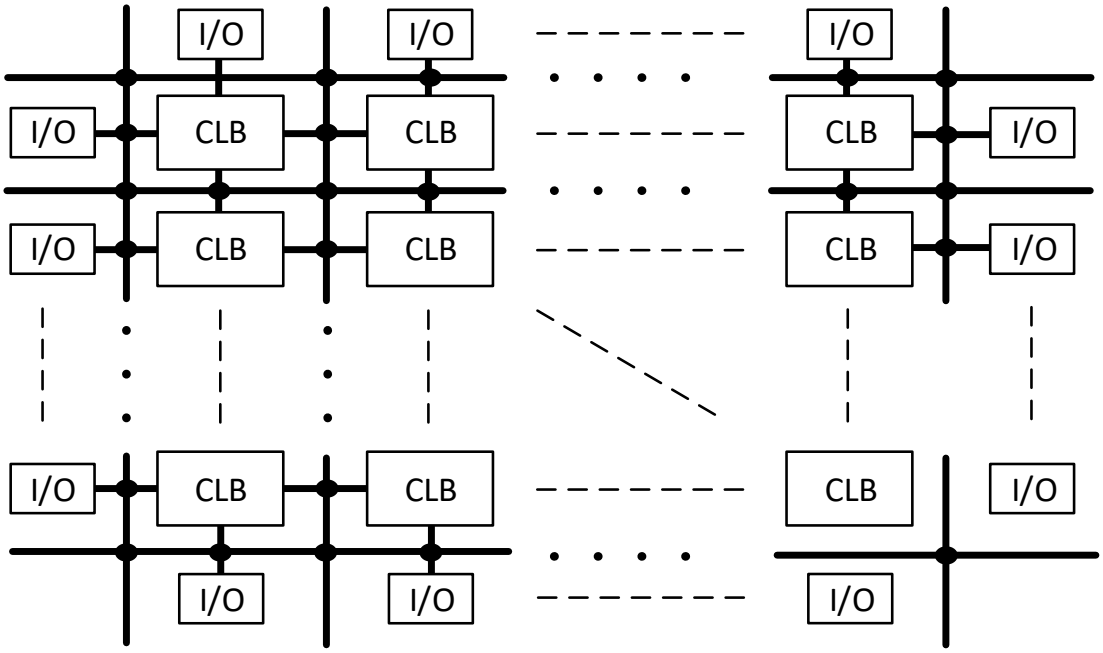

Figure 1 – Simplest FPGA structure

The designed BLE has $K = 4$. The number of inputs is determined by the additional devices built into the FPGA, the most common of which is the adder [3]. The functional scheme on the basis of which the representation of the designed BLE on the register transfer level (RTL) is formed is shown in Figure 2. The result of modeling RTL-representation of BLE is shown in Figure 3. The timing diagram shows two operations alternating on the positive edge of the clock signal: the reset of LUTs, flip-flops, programmable bits (PBs) and the result of the addition operation with the input carry set.

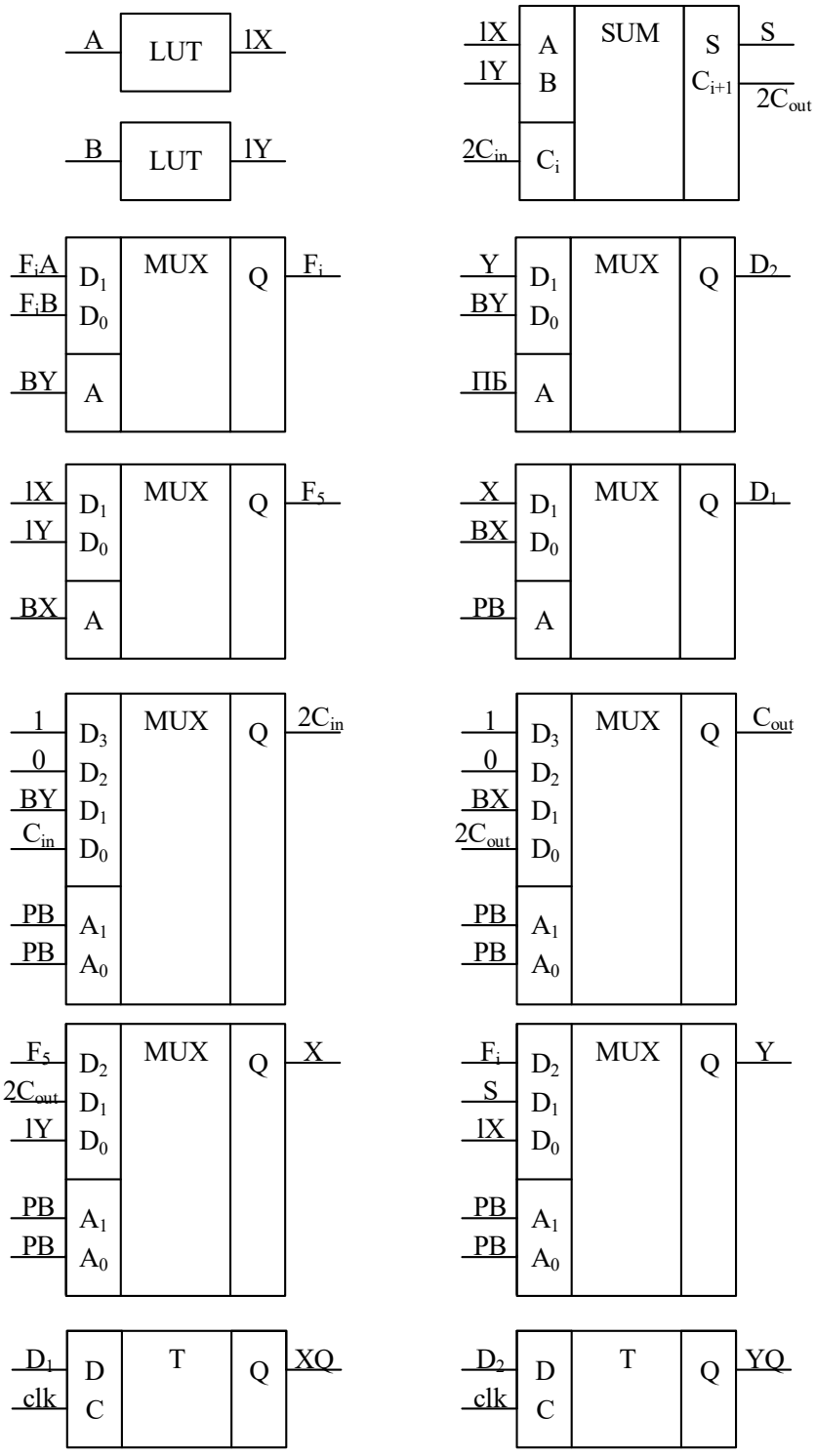

Figure 2 – Functional scheme of BLE

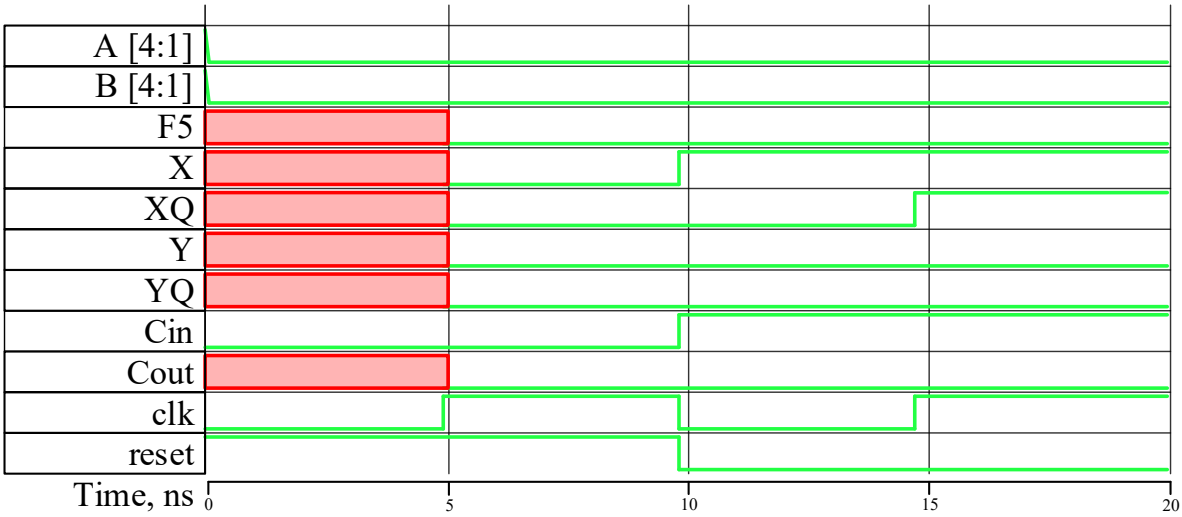

Figure 3 – Timing diagram of BLE

4 BLEs are connected to each other through the C_{in} (C_{out}) inputs (outputs), forming a CLB with a serial carry chain as shown in Figure 4. Within the CLB, all BLEs operate in parallel.

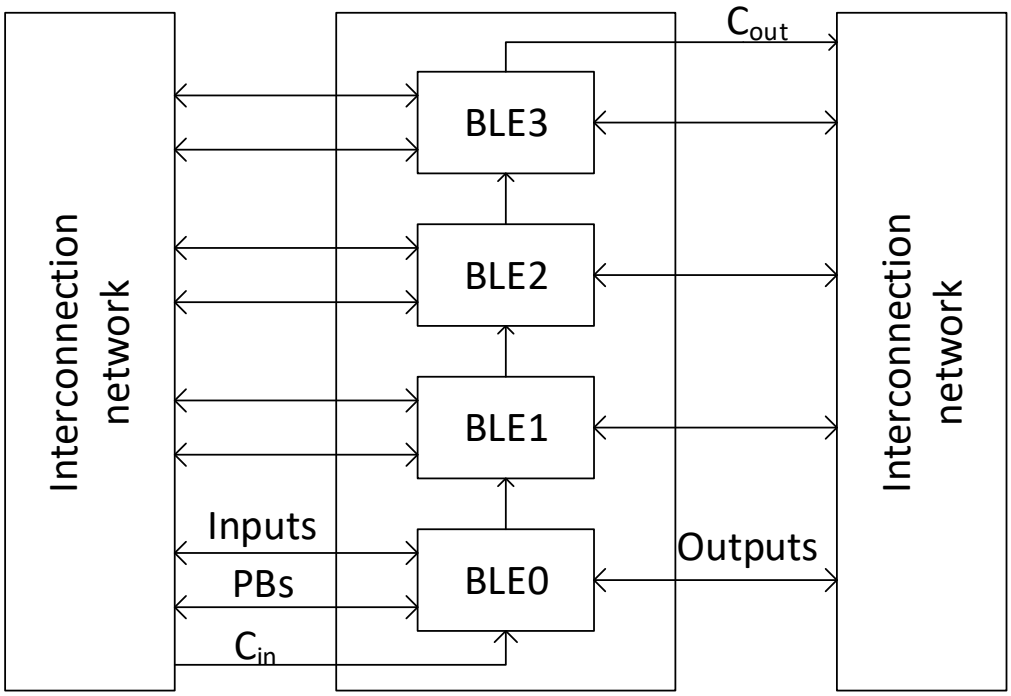

Figure 4 – Structure of CLB

Conclusion. Based on the analysis of architectures of programmable logic integrated circuits, a functional scheme and RTL representation of the basic logic element, suitable for use in the construction of configurable logic blocks, were designed.

References

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