Design optimization of the gallium nitride high electron mobility transistor with graphene and boron nitride heat-spreading elements

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The self-heating effect has long been a persistent issue for high electron mobility transistors based on gallium nitride due to their inherently poor heat dissipation capability. Although a wide variety of thermal management solutions has to date been proposed, the problem of the extremely non-uniform heat dissipation at the micrometer scale is still challenging. It has recently been demonstrated, however, that the performance of gallium nitride high electron mobility transistors can be substantially improved by the introduction of various heat-spreading elements based on graphene, boron nitride or diamond. In this paper, using numerical simulation, we carried out a design optimization procedure for a normally-off gallium nitride high electron mobility transistor containing both graphene and cubic boron nitride layers. First, a screening experiment based on a very economical Plackett−Burman design was performed in order to find the most critical geometric parameters that influence the dc characteristics. After that, a full two-level factorial experiment consisting of three factors was implemented and an optimized parameter set was yielded. By applying this set, the output power was increased by 11.35%. The combination of the most significant parameters does not include any factors related to the heat-spreading layers.

Keywords: gallium nitride, high electron mobility transistor, optimization, Plackett−Burman design, screening experiment, self-heating.

1. Introduction

The advent of power semiconductor devices in the middle of the 20th century laid a strong foundation for modern power electronics. This is the branch of electrical engineering that deals with the control and conversion of electric power. It is used in a wide spectrum of applications, varying in size from a switch-mode power supply in ac adapters, through a variable-frequency drive used in pumping plants, up to a high-voltage dc electric power transmission line. As a power conversion system can be found in virtually all electronic components, advancements in power electronics are essential to insuring efficient generation, distribution and consumption of electrical energy. A major breakthrough that would markedly improve the efficiency by reducing switching and conduction losses is expected from the development of novel materials and devices.

Since the beginning of solid-state electronics, silicon has continued to be the basic semiconductor material for manufacturing power devices. However, traditional silicon technology is now struggling to keep pace with the requirements of up-to-date industrial applications and, to common opinion, is about to reach its both theoretical and physical limits [1]. As a consequence, there is a continuous trend towards the adoption of next-generation power devices based on wide band gap semiconductors. One of these attractive materials is GaN, which represents unique group-III nitrides. Among the benefits offered

by GaN transistors are a low on-state resistance, a high breakdown voltage, a high operational switching frequency as well as exceptional thermal and radiation stability. Moreover, a definite advantage of GaN is the ability to form different top-quality heterostructures with other group-III nitrides using band-gap engineering.

One of the most appealing devices for power electronics is a high electron mobility transistor (HEMT), or a heterostructure field-effect transistor, based on group-III nitrides [2]. It exploits the high in-plane mobility of the two-dimensional electron gas that is generated in the quantum well near the heterojunction [3]. Although GaN HEMTs have recently made remarkable progress [4,5], there are still several fundamental challenges that must be resolved to reveal them as reliable and economically viable devices. One such crucial problem is the self-heating phenomenon. When a GaN HEMT is powered at a high level, ohmic heating leads to the degradation of its electrical behavior and results in some long-term reliability issues [6]. For suppressing the self-heating effect, a wide variety of approaches has to date been proposed. Unfortunately, most of them act at the package level and fail to adequately remove the excess heat from the active area of the transistor. In the last years, it has been demonstrated, however, that the performance of GaN HEMTs can be substantially improved by the local deposition of graphene [7,8], boron nitride [9] or diamond layers [10]. In this communication, using numerical simulation, we further elaborated on this concept and completed
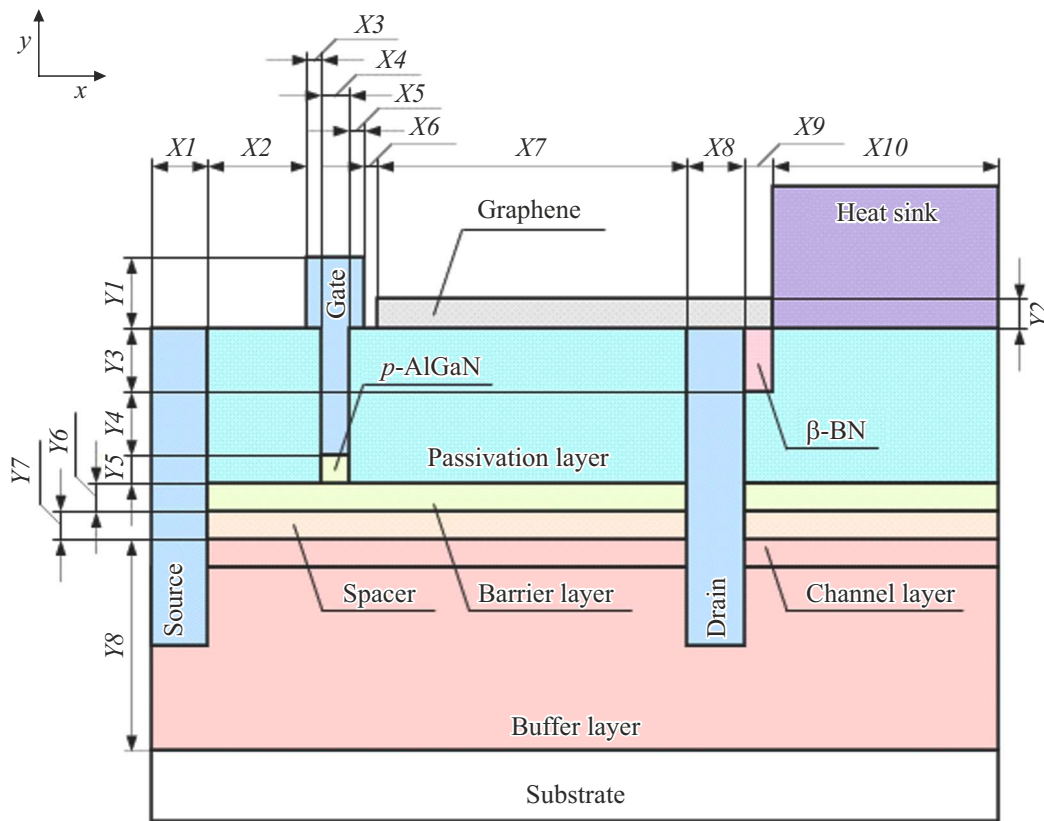
Figure 1. GaN HEMT with graphene and β-BN heat-spreading elements.

a design optimization procedure for a normally-off gallium nitride high electron mobility transistor containing graphene and cubic boron nitride (β-BN) heat-spreading elements.

2. Device structure

The main object of our research is a normally-off GaN HEMT augmented with a heat-removing system comprised of graphene and β-BN heat-spreading elements and a pyrolytic graphite heat sink. A two-dimensional representation of the device structure is shown in Fig. 1, where $X1 \ldots X10$ and $Y1 \ldots Y8$ are the geometric parameters to be considered. The default values of these parameters are given in Table 1.

Table 1. Default values of the geometric parameters $X1 \ldots X10$ and $Y1 \ldots Y8$

Parameter/Value (μm)								
$X1$	$X2$	$X3$	$X4$	$X5$	$X6$	$X7$	$X8$	$X9$
1	1.9	0.1	0.5	0.1	0.1	5.7	1	0.5
$X10$	$Y1$	$Y2$	$Y3$	$Y4$	$Y5$	$Y6$	$Y7$	$Y8$
4	0.1	0.0035	0.08	0.1	0.02	0.015	0.002	1.5

We specifically used AlGaN/AlN/GaN HEMTs with the layered structure that is composed of a 15 nm-thick $Al_{0.14}Ga_{0.86}N$ barrier layer, a 2 nm AlN spacer, a 50 nm GaN channel layer and a 1.45 μm GaN buffer layer deposited on a sapphire substrate. The barrier, spacer and channel layers are all undoped. Iron-induced deep-level acceptor trap states with an associated energy of 0.7 eV below the conduction band minimum and a uniform concentration of $1 \cdot 10^{18}$ cm^{-3} are introduced into the buffer layer to control the drain current in the subthreshold region. Additionally, a 20 nm p-type $Al_{0.14}Ga_{0.86}N$ layer with an acceptor concentration of $5.3 \cdot 10^{18}$ cm^{-3} is formed beneath the gate to produce a normally-off device [11]. The source, drain and T-shaped gate electrodes are nominally made of gold and set to be ohmic contacts. At last, an 0.2 μm SiO$_2$ layer is applied for surface passivation.

The substrate thickness equals to 100 μm, while the thickness of the heat sink is 20 μm. The device structure is 1 mm wide.

With the purpose of accurately simulating the temperature distribution, two thermal boundary conditions are imposed, one on the bottom surface of the substrate and another on the top surface of the heat sink. Both of these regions are sufficiently thick to assume that the temperature at the thermal contacts remains rigid. The thermal boundary resistance at the interfaces between the ambient and both the substrate and the heat sink is not taken into account.

With reference to this, the heat transfer coefficient goes to infinity.

3. Equations and models

The electrical behavior of semiconductor devices is operated by a mathematical model consisting of a coupled set of fundamental partial differential equations that bind together the electrostatic potential and the carrier concentration. The framework of this model is provided by the Poisson and carrier continuity equations.

The Poisson equation governs the interaction between the potential and the space charge density:

$$\nabla(\varepsilon\varepsilon_0\nabla\varphi) = q(n - p - N_d^+ + N_a^-) - Q, \qquad (1)$$

where ε is the relative permittivity, ε_0 is the electric constant, φ is the electrostatic potential, q is the elementary charge, n and p are the electron and hole concentrations, N_d^+ and N_a^- are the ionized donor and acceptor impurity concentrations, Q is the charge density induced by traps and other defects.

The continuity equations describe the way the electron and hole concentrations evolve as a result of transport, generation and recombination processes:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla\mathbf{J}_n + G_n - R_n, \qquad (2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla\mathbf{J}_p + G_p - R_p, \qquad (3)$$

where $\mathbf{J}_n$ and $\mathbf{J}_p$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes.

The current density equations, or charge transport models, are generally derived by applying various approximations to the Boltzmann transport equation. The simplest charge transport model is the drift-diffusion model, which has the advantage of avoiding any independent variables, with the exception of the potential and the carrier concentration:

$$\mathbf{J}_n = qD_n\nabla n + q\mu_n n\mathbf{E}, \qquad (4)$$

$$\mathbf{J}_p = qD_p\nabla p - q\mu_p p\mathbf{E}, \qquad (5)$$

where D_n and D_p are the diffusion coefficients for electrons and holes, μ_n and μ_p are the electron and hole mobilities, $\mathbf{E}$ is the electric field.

For electrons and holes, we employed low- and high-field temperature-dependent mobility models developed specifically for the (Al,Ga)N material system [12].

Simulation of the self-heating effect suggests the addition of a lattice heat flow equation to the coupled system consisting of the Poisson and carrier continuity equations. In the framework of the thermodynamically rigorous model of lattice heating [13], the heat flow equation, which describes the evolution of the local lattice temperature, is given by

$$C_V\frac{\partial T_L}{\partial t} = \nabla(\kappa\nabla T_L) + H, \qquad (6)$$

where C_V is the volumetric heat capacity, T_L is the lattice temperature, κ is the thermal conductivity, H is the heat generation rate.

As ohmic heating is the dominant heat generation process in GaN HEMTs, the other mechanisms are often neglected [14] and the heat generation rate is consequently reduced to the form of

$$H = (\mathbf{J}_n + \mathbf{J}_p)\mathbf{E}. \qquad (7)$$

It is well established that thermal conductivity is strongly dependent on temperature. This fact should be taken into consideration, as the operating temperature is very sensitive to the thermal conductivity in certain regions of the device structure. Otherwise, a noticeable error may occur. In many scientific papers, reports and material databases, the thermal conductivity for a given material is often presented as a function of temperature in graphic or tabular form. In order to incorporate these data into a device simulation software package through a C language interpreter, we transformed the temperature dependence of the thermal conductivity into a mathematical model by constructing an approximating curve that has the best fit to a series of data points. The standard expression for thermal conductivity above room temperature is

$$\kappa(T) = \kappa(300\,\text{K})\left(\frac{T}{300}\right)^\tau, \qquad (8)$$

where T is the temperature, τ is the temperature dependence coefficient.

For AlGaN, the dependence of the thermal conductivity on composition fraction and temperature is defined by [15]

$$\kappa(\text{Al}_x\text{Ga}_{1-x}\text{N})(T)$$

$$= \left[\frac{x}{\kappa(\text{AlN})(T)} + \frac{1-x}{\kappa(\text{GaN})(T)} + Cx(1-x)\right]^{-1}, \quad (9)$$

where C is the bowing parameter:

$$C = 3.649 \cdot 10^{-3}T - 0.221. \qquad (10)$$

We employed Eq. (8) for all the unary and binary materials except for gold and graphene. For the former, a simple linear regression is used [16]:

$$\kappa(\text{Au})(T) = 3.365 - 6.5 \cdot 10^{-4}T. \qquad (11)$$

The thermal conductivity of graphene is assumed to be $20\,\text{W/(cm}\cdot\text{K)}$, which corresponds to a film composed of ten or more atomic layers [17].

The material-dependent parameters from Eq. (8) are given in Table 2.

Table 2. Parameters for the thermal conductivity model [15,16,18-22]

Parameter	Material							
	AlN	GaN	Al_2O_3	Si	6H-SiC	SiO_2	β-BN	Graphite
$\kappa(300\,K)$ (W/cm $\cdot$ K)	3.893	2.583	0.387	1.48	3.736	0.014	8.368	19.342
τ	-1.277	-1.031	-1.195	-1.65	-1.49	0.33	-0.972	-1.125
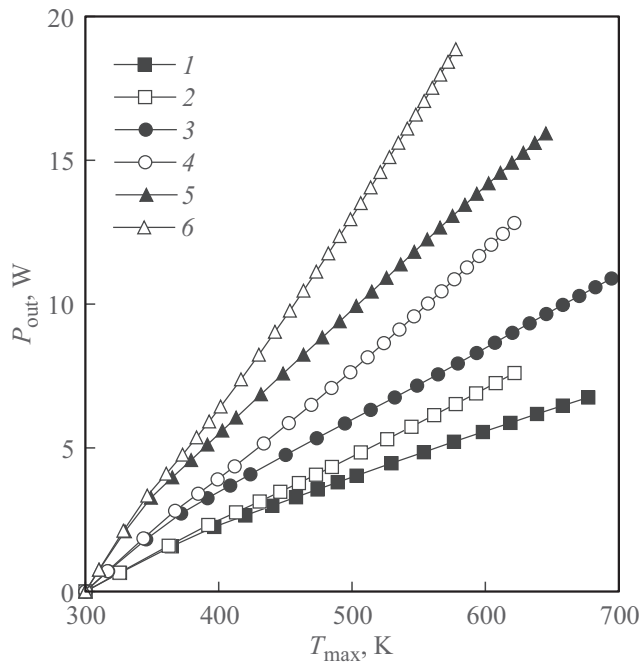
Figure 2. Output power as a function of the maximum temperature in the active area of the GaN HEMTs on sapphire (curves *1* and *2*), silicon (*3* and *4*) and 6H-SiC (*5* and *6*) substrates: *1, 3* and *5* — temperature-dependent thermal conductivity models; *2, 4* and *6* — constant thermal conductivity models.

When a lattice heat flow equation is solved, at least one thermal boundary condition must be specified. If a thermal contact is implemented as a Robin boundary condition, or a third-type boundary condition, the following expression holds:

$$\alpha(T_L - T_0) = -\kappa\nabla T_L, \qquad (12)$$

where α is the heat transfer coefficient, T_0 is the ambient temperature, which is assumed to be equal to 300 K.

To weigh the effect of the temperature-dependent thermal conductivity models on simulation results, a device structure identical to that previously described but without the heat-spreading elements was simulated using the thermal conductivity models that either account for or ignore the temperature dependence of this thermoelectric parameter. In addition to sapphire substrate, the transistors fabricated on silicon and 6H-SiC substrates were also considered. The thermal boundary resistance at the sapphire-GaN interface was neglected owing to the low thermal conductivity of the former. To imitate the thermal boundary resistance at the silicon-GaN and 6H-SiC-GaN contacts, a 10 nm-thick heat isolation layer with a thermal conductivity of 0.003 W/(cm $\cdot$ K) [23] was inserted between the substrate and the buffer layer. The relationship between the output power (P_{out}) and the maximum temperature in the active area (T_{max}) is plotted in Fig. 2. The gate-source voltage is 6 V.

As seen in Fig. 2, the discrepancy of the output power caused by the application of thermal conductivity models of two fundamentally different classes is quite striking. At a maximum temperature of 550 K, the output power of the device structure on sapphire substate is reduced by 18.26%, from a value of 5.86 to 4.79 W, as a consequence of the thermal conductivity degradation. If silicon and 6H-SiC substrates are used, the output power is decreased by 26.00%, from a value of 9.73 to 7.20 W, and by 28.60%, from a value of 16.75 to 11.96 W, respectively. These results directly stress the importance of the temperature-dependent thermal conductivity models for accurate simulation of high-power devices.

4. Optimization procedure

Contemporary industry-standard technology computer-aided design software solutions enable engineers to easily simulate and optimize semiconductor processes and devices. Numerical simulation helps to build qualitative and quantitative understanding of the final product without the need to conduct expensive and time-consuming experiments in manufacturing. Optimization is carried out with the aim to determine the absolute best set of admissible conditions so that to obtain the optimal device characteristics.

The electrical behavior of advanced semiconductor devices is dependent on a tremendous number of parameters, or factors. However, only few of them have a noticeable impact on the device performance. When there is a large list of potential factors, a screening experiment intended to find the most significant factors should first be performed. One of the most popular screening designs is the family of Plackett−Burman designs based on Hadamard matrices and developed for examining the dependence of some response variable on a large number of independent variables using a relatively small quantity of trials. For the case of two levels, the Paley construction is used to generate an orthogonal matrix with all entries being either $+1$ or -1 corresponding to the maximum and minimum values of the independent
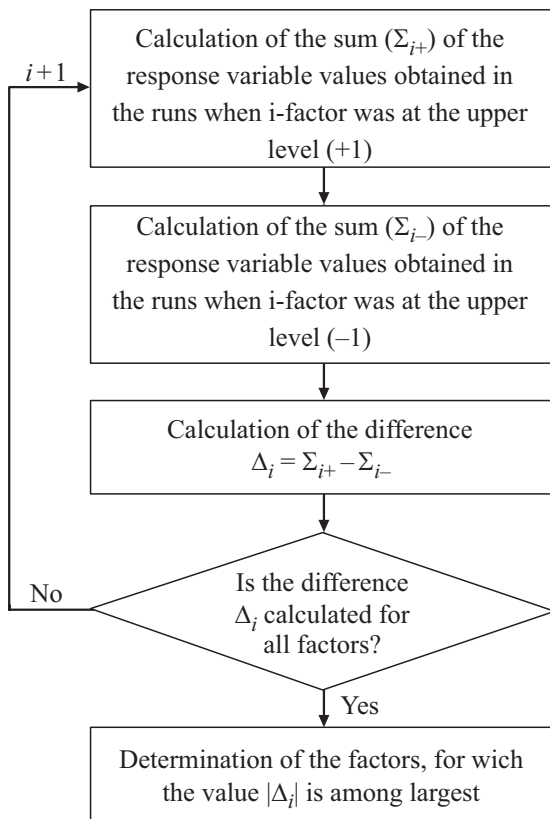
Figure 3. Screening experiment output data processing.

variables, respectively. The design is fully preset by the pattern for the first column or row. Each of the subsequent columns (rows) is simply the previous one shifted one step down (to the right), with the final entry from the previous column (row) being placed at the start of the subsequent one. The last column is entirely set to -1. The output data obtained after a series of simulation runs is completed are analyzed following the procedure given in Fig. 3.

With a limited set of the most important factors secured, the design optimization continues with a full two-level factorial experiment that is implemented for providing an optimized parameter set. When this set is included in the device simulation overwriting the default values of the geometric parameters, the optimization procedure ends.

5. Results

The screening experiment based on a Plackett−Burman design that was carried out to select the most critical parameters from the list of $X1\ldots X10, Y1\ldots Y8$ is presented in Table 3. The levels are denoted by „+" and „−" to save the space in the cells. The maximum and minimum values of each of the factors equal to $+10\%$ and -10% of its initial value, respectively. The output power at the drain-source voltage of 15 V serves as the response variable.

According to the screening experiment, the most significant geometric parameters of the GaN HEMT enhanced by the graphene and β-BN heat-spreading elements are the distance from the source to the head of the gate ($X2$), the thickness of the p-AlGaN layer underneath the gate ($Y5$) and the thickness of the spacer ($Y7$). The effect of each of these parameters on the output power is shown in Fig. 4, where σ denotes the deviation of the factors from their initial values in percentage terms.

It is apparent from Fig. 4 that the output power is linearly dependent on each of the parameters $X2, Y5$ and $Y7$ on condition that the deviation of these factors from their initial values does not exceed $\pm10\%$. The relationships obtained are consistent with previous studies. A decrease in the source-gate distance enhances the electric field component along the conducting channel, leading to a higher electron concentration beneath the gate and, consequently, to a higher output power [24]. In its turn, a decrease in the thickness of the p-AlGaN layer results in a negative shift of the threshold voltage (V_{th}), providing a higher output power at the same gate-source voltage [25]. The electron concentration can also be enlarged by an increase in the thickness of the spacer. In this case, however, the effect of a reduction in the electron mobility is observed [26], but it is neglected in our work.

The full two-level factorial experiment that was performed to find the optimal values for the most critical geometric parameters is presented in Table 4. The threshold voltage values are also included.

According to the full factorial experiment, the highest output power is achieved with a combination of
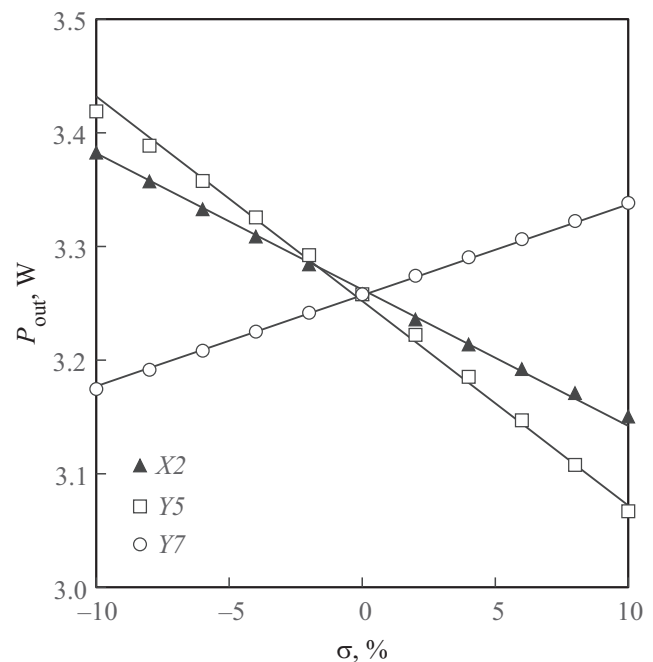
Figure 4. Effect of the factors $X2, Y5$ and $Y7$ on the output power.

Table 3. Screening experiment

Factor	Simulation run											
	1	2	3	4	5	6	7	8	9	10	11	12
$X1$	+	+	−	−	+	+	+	+	−	+	−	+
$X2$	−	+	+	−	−	+	+	+	+	−	+	−
$X3$	+	−	+	+	−	−	+	+	+	+	−	+
$X4$	+	+	−	+	+	−	−	+	+	+	+	−
$X5$	−	+	+	−	+	+	−	−	+	+	+	+
$X6$	−	−	+	+	−	+	+	−	−	+	+	+
$X7$	−	−	−	+	+	−	+	+	−	−	+	+
$X8$	−	−	−	−	+	+	−	+	+	−	−	+
$X9$	+	−	−	−	−	+	+	−	+	+	−	−
$X10$	−	+	−	−	−	−	+	+	−	+	+	−
$Y1$	+	−	+	−	−	−	−	+	+	−	+	+
$Y2$	−	+	−	+	−	−	−	−	+	+	−	+
$Y3$	+	−	+	−	+	−	−	−	−	+	+	−
$Y4$	+	+	−	+	−	+	−	−	−	−	+	+
$Y5$	+	+	+	−	+	−	+	−	−	−	−	+
$Y6$	+	+	+	+	−	+	−	+	−	−	−	−
$Y7$	−	+	+	+	+	−	+	−	+	−	−	−
$Y8$	−	−	+	+	+	+	−	+	−	+	−	−
P_{out}	3.06	3.05	3.17	3.59	3.25	3.29	3.00	3.23	3.28	3.52	3.15	3.03

Factor	Simulation run								Σ_{i+}	Σ_{i-}	Δ_i	$|\Delta_i|$
	13	14	15	16	17	18	19	20				
$X1$	−	−	−	−	+	+	−	−	32.57	32.42	0.14	0.14
$X2$	+	−	−	−	−	+	+	−	31.34	33.65	−2.31	**2.31**
$X3$	−	+	−	−	−	−	+	−	32.44	32.55	−0.10	0.10
$X4$	+	−	+	−	−	−	−	−	32.18	32.81	−0.62	0.62
$X5$	−	+	−	+	−	−	−	−	32.49	32.50	−0.01	0.01
$X6$	+	−	+	−	+	−	−	−	32.53	32.46	0.08	0.08
$X7$	+	+	−	+	−	+	−	−	32.20	32.79	−0.59	0.59
$X8$	+	+	+	−	+	−	+	−	32.41	32.58	−0.17	0.17
$X9$	+	+	+	+	−	+	−	−	32.33	32.66	−0.32	0.32
$X10$	−	+	+	+	+	−	+	−	32.65	32.34	0.31	0.31
$Y1$	−	−	+	+	+	+	−	−	32.47	32.52	−0.06	0.06
$Y2$	+	−	−	+	+	+	+	−	32.54	32.45	0.08	0.08
$Y3$	+	+	−	−	+	+	+	−	32.63	32.36	0.27	0.27
$Y4$	−	+	+	−	−	+	+	−	32.37	32.62	−0.25	0.25
$Y5$	+	−	+	+	−	−	+	−	30.74	34.25	−3.51	**3.51**
$Y6$	+	+	−	+	+	−	−	−	32.67	32.33	0.34	0.34
$Y7$	−	+	+	−	+	+	−	−	33.31	31.68	1.63	**1.63**
$Y8$	−	−	+	+	−	+	+	−	32.83	32.16	0.68	0.68
P_{out}	2.80	3.58	3.25	3.16	3.73	3.40	2.97	3.47	−	−	−	−

Table 4. Full factorial experiment

Factor	Simulation run								
	0	1	2	3	4	5	6	7	8
$X2$	1.9	2.09	2.09	2.09	2.09	1.71	1.71	1.71	1.71
$Y5$	0.02	0.022	0.022	0.018	0.018	0.022	0.022	0.018	0.018
$Y7$	0.002	0.0022	0.0018	0.0022	0.0018	0.0022	0.0018	0.0022	0.0018
V_{th}	1.99	2.15	2.49	1.53	1.88	2.15	2.50	1.53	1.88
P_{out}	3.26	3.05	2.88	3.38	3.23	3.27	3.09	3.63	3.47
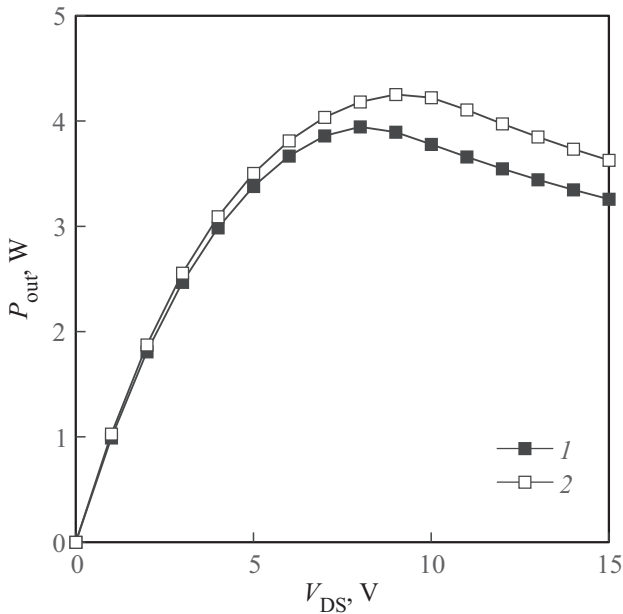
Figure 5. Output power vs. drain-source voltage characteristics: *1* — geometric parameters with the initial values, *2* — geometric parameters with the optimal values.

$X2 = 1.71\,\mu$m, $Y5 = 0.018\,\mu$m and $Y7 = 0.0022\,\mu$m. The improvement of the dc characteristics due to the design optimization is demonstrated in Fig. 5. The gate-source voltage equals to 6 V.

As a result of the optimization, the output power of the GaN HEMT with the graphene and β-BN heat-spreading elements at a drain-source voltage of 15 V is increased by 11.35%, from a value of 3.26 W to 3.63 W.

It is noteworthy that the combination of the most significant parameters does not include any factors related to the heat-spreading layers. Anyhow, the dimensions of the graphene and β-BN elements have a considerable influence on their heat dissipation efficiency (η). The effect of the graphene heat-spreading element length on the dc, small-signal ac and breakdown characteristics of a GaN HEMT has recently been investigated [8]. The efficiency of the β-BN heat-spreading element as a function of its thickness (parameter $Y3$) is shown in Fig. 6 for a device structure identical to the current version but without the graphene element. The corresponding curve for the maximum temperature in the active area is also given. The distance from the heat sink to the barrier layer remains constant. The gate-source voltage is 6 V and the drain-source voltage is 30 V.

It follows from Fig. 6 that an increase in the thickness of the β-BN layer from a value of $0.02\,\mu$m to $0.18\,\mu$m leads to an enhancement of the efficiency by 22.95%, from a value of 18.67% to 41.62%. At the same time, the maximum temperature is decreased by 28.8 K, from a value of 449.6 K to 420.8 K. It is obvious that the higher $Y3$, the larger the contacting area between the drain and the β-BN layer, which

partially substitutes the SiO_2 passivation layer with a very low thermal conductivity.

The efficiency of the β-BN heat-spreading element as a function of its length (parameter $X9$) is shown in Fig. 7. The corresponding curve for the maximum temperature in the active area is also presented.

As follows from Fig. 7, an extension of the length of the β-BN from a value of $0.5\,\mu$m to $10\,\mu$m leads to a reduction
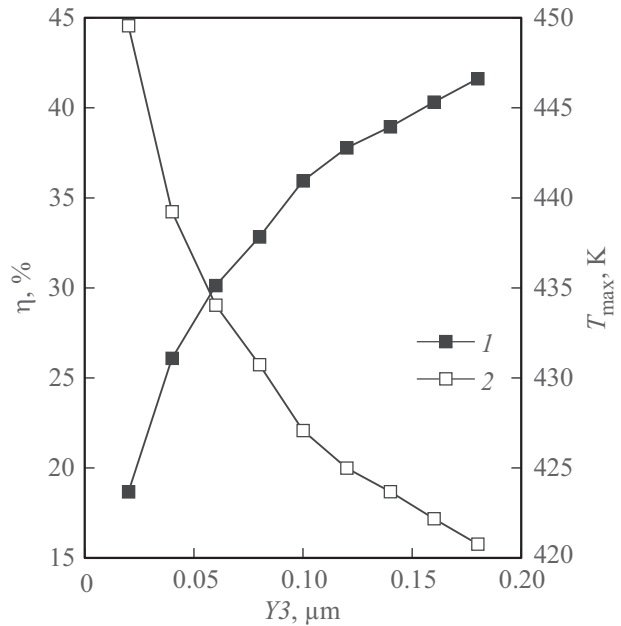
Figure 6. Effect of the thickness of the β-BN heat-spreading element on the efficiency (*1*) and the maximum temperature in the active area (*2*).
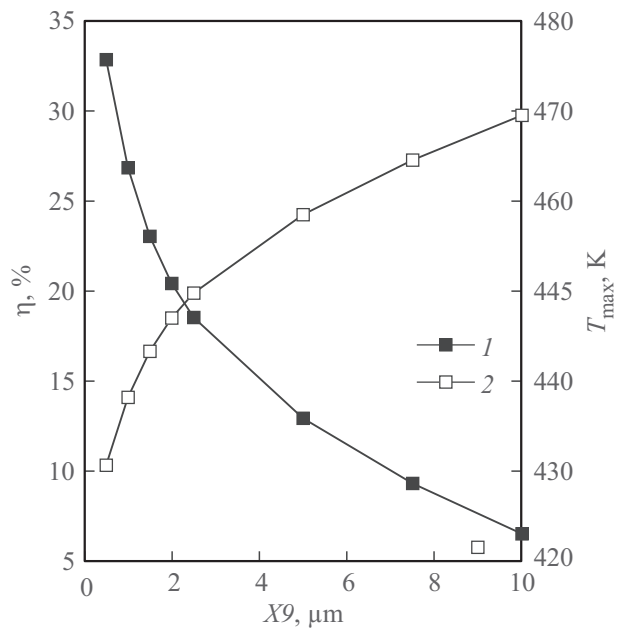
Figure 7. Effect of the length of the β-BN heat-spreading element on the efficiency (*1*) and the maximum temperature in the active area (*2*).

in the efficiency by 26.27%, from a value of 32.83% to 6.56%, and to a rise in the maximum temperature by 38.8 K, from a value of 430.7 K to 469.5 K. This can be explained by the increasing distance between the active area and the heat sink.

6. Conclusions

In this work, a design optimization procedure for a normally-off GaN HEMT augmented with a heat-removing system comprised of graphene and β-BN heat-spreading elements and a pyrolytic graphite heat sink was carried out. A screening experiment based on a very economical Plackett−Burman design showed that the most critical geometric parameters are the distance from the source to the head of the gate, the thickness of the p-AlGaN layer underneath the gate and the thickness of the spacer. The combination of the most significant parameters does not include any factors related to the heat-spreading layers. As a result of the design optimization, the output power at a drain-source voltage of 15 V was increased by 11.35%.

Acknowledgements

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