Sensor signal processing

A Time-Encoded Capacitance-to-Digital Converter Based on a Switched-Capacitor Feedback

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Manuscript received 23 August 2023; revised 18 September 2023; accepted 21 September 2023. Date of publication 27 September 2023; date of current version 10 October 2023.

Abstract—An innovative method to perform capacitance-to-digital conversion without requiring sensor biasing circuitry is proposed. This letter is intended for the readout of MEMS capacitive microphones used in human-to-machine interface applications, where the main constraints are low power consumption and small chip area. The time-encoded sigma-delta ADC described here employs a switched-capacitor-based feedback to linearize the voltage-controlled oscillator and to couple the capacitive sensor to the readout. A prototype was fabricated to test the concept with a CMOS 130-nm process. The achieved relative capacitance resolution is 14.7 b with a rest capacitance value of 2.575 pF and a total power consumption of 343 μW. Linearity measurements ($SNDR_{peak} = 51.5$ dB in the bandwidth from 300 Hz to 6.8 kHz) are limited by the test fixture due to the nonlinearity of the varactor introduced in lieu of a testing input sensor.

Index Terms—Sensor signal processing, capacitance, converter, digital, MEMS, microphone, sensor, sigma-delta, time-encoding, VCO-ADC.

I. INTRODUCTION

Many MEMS sensors, such as pressure and acoustic sensors, require a capacitance-to-digital interface. In the state of the art, there are different architectures performing this task. Successive approximation register (SAR)-based capacitance-to-digital converters are well known for their excellent energy efficiency, but linearity and resolution are limited by mismatch [1]. Continuous-time (CT) sigma-delta (ΣΔ) analog-to-digital converters (ADCs), instead, provide a remarkable dynamic range (DR) at the cost of large area requirements and power-hungry analog subsystems; this class of ADCs can achieve high resolution thanks to oversampling and noise shaping [2], [3]. The zoom architecture combines the advantages of SAR and ΣΔ ADCs (a good tradeoff between resolution and energy dissipated per conversion step), but common drawbacks are the area occupation and linearity issues in the case of multibit digital-to-analog converters (DACs) [4]. In recent years, extensive research has focused on voltage-controlled oscillator (VCO)-based ADCs [5], [6]. Their mostly digital nature allows them to cope with the increasingly challenging power and area constraints in ADC design. The main disadvantages are the oscillator nonlinearity and its gain dependency on process–voltage–temperature (PVT) variations. In conventional VCO-based ADCs, the electrical input (voltage or current) modulates the instantaneous oscillation frequency of an oscillator, and this time-encoded signal is then processed by digital electronics. Therefore, it is required an intermediate conversion from a capacitive signal to a voltage (or current) one, which is the ADC input. In particular, capacitive microphones are sensitive to variations in the gap between the plates; their most popular readout is based on a constant-charge configuration, shown in Fig. 1(a), which generates a voltage signal linear to the inverse of capacitance. This requires biasing circuitry (a charge pump and a high-ohmic resistance), which is less scalable than the subsequent VCO-based ADC. An innovative approach for capacitance-to-digital converters (CDCs) is to remove the intermediate voltage conversion and to directly encode the capacitive signal into the oscillation frequency of a ring oscillator (RO) [7]. In this way, the charge pump and the high-ohmic resistor can be removed, and this is particularly advantageous in light of easier scalability and smaller area. Unfortunately, unbiased MEMS sensors usually provide less sensitivity, limiting the attainable resolution. Therefore, this innovative approach is suitable for human-to-machine interface applications, which require small and low-power digital microphones rather than high resolution. The CDC shown in Fig. 1(b) provides a possible solution to the aforementioned VCO-based ADC issues. The usage of a switched-capacitor (SC) feedback for ROs has already

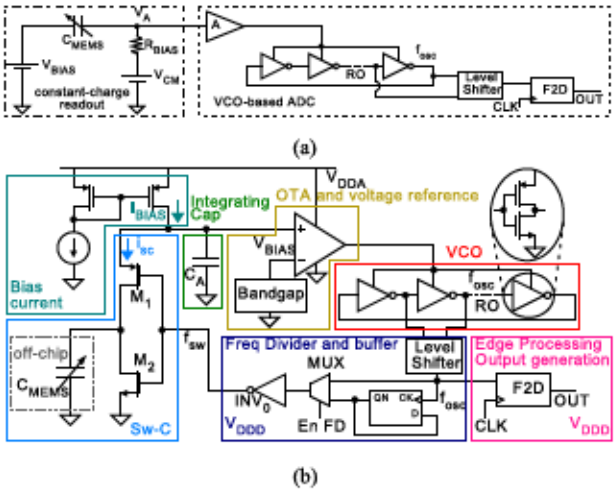

Fig. 1. (a) Conventional constant-charge readout required by VCO-ADCs. (b) Proposed readout to remove the charge pump and the high-ohmic resistance.

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Associate Editor: W. Pu.
Digital Object Identifier 10.1109/LSENS.2023.3320061

been proven to reduce RO nonlinearity and phase noise [8], [9], [10], [11]. It also permits linear sensing of the capacitance gap without requiring a constant-charge readout: The sensor functions as an SC in the feedback network. The loop reacts to any measurand variation by regulating the oscillation frequency to recover the equilibrium point. Indeed, at the equilibrium point, the product between sensor capacitance and oscillation frequency is constant and depends only on the circuit design parameters. This ensures good robustness since the oscillation frequency and sensitivity depend on controllable and stable circuit parameters that are less influenced by PVT variations than the oscillator. In this letter the proposed CDC is investigated, and the design choices and testing results of a fabricated CMOS prototype are reported.

The rest of this letter is organized as follows: In Section II, the constant-charge readout for capacitive sensors is recalled, and the main drawbacks are pointed out. In Section III, the working principle of the proposed CDC is analyzed, and the main design constraints are summarized. In Section IV, our prototype design in a 130-nm CMOS process is detailed and a method to mimic a sensor with a voltage-controlled capacitor is explained: A varactor with biasing and signal-coupling circuitry was introduced on the testing PCB. In Section V, measurement results are reported and discussed. Finally, Section VI concludes this letter.

II. BIASING CIRCUITRY AND CONSTANT-CHARGE READOUT

Several MEMS capacitive sensors (e.g., microphones, accelerometers, pressure sensors, etc.) detect gap variations due to a physical measurand $p_i(t)$ as follows [12], [13]:

$$C_{\text{MEMS}}(p_i(t)) = \frac{\varepsilon A}{d_0 + \Delta d(p_i(t))} \tag{1}$$

where ε is the dielectric permittivity, A is the area of the parallel conductive plates, d_0 is the gap in rest condition, and Δd the displacement due to measurand variations. In the case of MEMS capacitive microphones, the conventional readout is based on keeping constant the charge stored on the plates, and a change in capacitance manifests itself as a voltage variation [14]. The conventional constant-charge read-out circuitry is outlined in Fig. 1(a). The bias voltage V_{BIAS}, realized through a charge pump, stores charge on the sensor, which is kept constant by connecting the capacitor to a high-impedance node. Such a condition is realized by the high-ohmic bias resistor R_{BIAS} and the input of the subsequent buffer or amplifier. The high-impedance node is particularly sensitive to electromagnetic interference [15]. The common mode voltage V_{CM} is used to set the required dc level of voltage V_{A}, which may be expressed by the following formula:

$$V_{\text{A}}(p_i(t)) = V_{\text{CM}} - \frac{\Delta d(p_i(t))}{d_0}(V_{\text{BIAS}} - V_{\text{CM}}). \tag{2}$$

Sensitivity increases with the bias voltage, which is likely to be about one order of magnitude bigger than the supply voltage needed by the rest of the circuitry. Here comes the interest in displacement readout alternatives, which do not require such a high voltage for the sensor bias.

III. CDC WITH AN SC FEEDBACK

The CDC architecture shown in Fig. 1(b) does not require the charge pump and the high-ohmic resistance. A constant current I_{BIAS} is integrated by the capacitor C_A. When the PMOS switch M1 is ON, the larger capacitor C_A transfers a portion of its stored charge to the smaller sensitive capacitor C_{MEMS}. Alternatively, when the NMOS switch M2 is active, the capacitor C_{MEMS} is fully discharged. In the steady state, during one switching period, the charge increase on C_A due to current integration is equal to the charge that is released by the SC network; similarly, the bias current I_{BIAS} equals the average current flowing to ground through the SC network, which can be expressed as $i_{\text{SC}} = C_{\text{MEMS}} f_{\text{sw}} < V_+ >$, where $< V_+ >$ is the average voltage on the operational transconductance amplifier (OTA) positive input node during one switching period and f_{sw} is the switching frequency, which is N times smaller than the RO oscillation frequency f_{osc}. The parameter N is set by the frequency divider (FD). Negative feedback [16] forces $< V_+ >$ to be approximately equal to the voltage reference V_{BIAS} as long as the OTA and the RO ensure enough gain. Therefore, the steady-state equation can be expressed as

$$f_{\text{osc}}(t) = \frac{N I_{\text{BIAS}}}{V_{\text{BIAS}} C_{\text{MEMS}}(p_i(t))}. \tag{3}$$

The instantaneous oscillation frequency is directly proportional to the reciprocal of the sensor capacitance C_{MEMS}; this makes the architecture suitable to sense the gap between the plates. The RO output is then processed by purely digital electronics and converted to digital, as for any VCO-based $\Sigma\Delta$ ADC [17]. The switching nature introduces some ripple (whose fundamental frequency is exactly the instantaneous switching frequency) at the OTA input. The capacitor C_A should be sized to minimize the ripple amplitude and prevent the OTA saturation. Thus, the oscillation frequency at rest condition ($p_i(t) = 0$) is a periodical signal whose mean value is given by (3). The converter performance is not affected by ripple if the signal bandwidth is much smaller than the rest oscillation frequency. System stability mainly depends on two poles in the direct input–output path: One is due to the capacitor C_A and the equivalent average resistance of the SC network

$$R_{\text{avg}} = \frac{N}{f_{\text{osc}} C_{\text{MEMS}}} = \frac{V_{\text{BIAS}}}{I_{\text{BIAS}}}$$

while the other is the dominant pole of the OTA-RO set.

IV. CHIP DESIGN AND CAPACITIVE INPUT GENERATION

The proposed CDC was designed in a 130-nm CMOS node to read capacitive sensors with a rest value of a few picofarads. Switches M1 ($W_{\text{p}} = 24.8\,\mu\text{m}$) and M2 ($W_{\text{n}} = 17.3\,\mu\text{m}$) and the inverter INV_0 ($W_{\text{n}} = 5.8\,\mu\text{m}$ and $W_{\text{p}} = 8.3\,\mu\text{m}$) were sized to optimize the trade-off between power consumption and delay in the feedback path; channel length was set for all of them to the technology minimum. The sensor capacitance range affects the choice of C_{A}, which is supposed to be bigger [16]; in our design, a 15 pF capacitor was implemented. The current I_{BIAS} was chosen as 39 µA while the bias voltage V_{BIAS} is 1 V (provided by a bandgap reference). The FD ratio can be set to one or two through a programmable input and a multiplexer (MUX). The OTA and current source noise are the main limitations of the architecture. The 11-tap RO does not have any strict constraint, because its inherent nonlinearity and the noise coming from its transistors are attenuated by the OTA gain, which is about 1 mS at low frequencies. Two power supplies, one for analog blocks ($V_{\text{DDA}} = 1.8$ V) and one for digital ones ($V_{\text{DDD}} = 1.2$ V), are provided by internal low-dropout regulators (LDOs). The subsystems represented in Fig. 1(b) supplied by V_{DDD} include the aforementioned MUX, FD, and buffer, as well as a frequency-to-digital converter (F2D) and a level shifter.

The capacitive input signal was generated through the circuit shown in Fig. 2(a), which includes a varactor SMV1249-079LF by Skyworks (C_{VAR}) in series with a 2.9 pF silicon capacitor inside the chip (C_s),

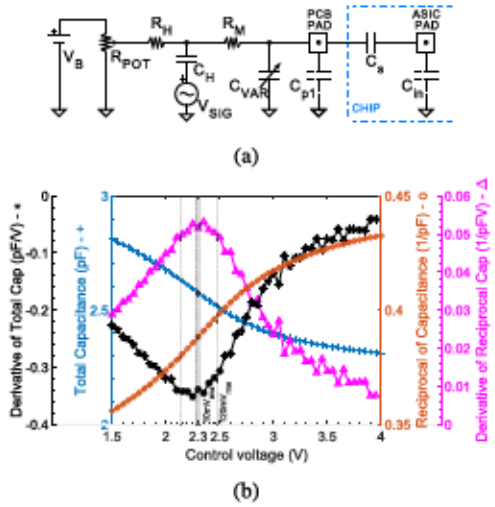

Fig. 2. (a) Implemented circuit to generate a capacitive signal; parasitic elements are represented in the circuit with a dashed line. (b) Total capacitance as well as its reciprocal value is set by a control voltage; a linear conversion is obtained in the range where the derivative may be approximated as constant, therefore around 2.3 V.

used to reduce the rest capacitance value. The capacitor C_{p1} represents the total parasitic capacitance at the PCB pad. The capacitor C_{in} represents the CDC input capacitance, seen from the node where C_{MEMS} is connected in Fig. 1(b). The potentiometer R_{pot} is used to bias the varactor at a designed dc voltage. The resistance R_H limits the current flowing in the dc bias path. The capacitor C_H is used to couple the ac control signal and to filter out the noise coming from the resistors in the dc bias path; this capacitor must be many orders of magnitude bigger than the varactor capacitance. Therefore, the resistor R_M is sized as a tradeoff: it should be big enough to prevent that, at the switching frequency, C_H shorts out the varactor, but it should be small enough such that its noise does not worsen the overall performance. Our design choices are the potentiometer ratio at 50% with $R_{pot} = 100\,k\Omega$, $R_H = 1\,M\Omega$, $R_M = 20\,k\Omega$, and $C_H = 10\,\mu F$. The parasitic parameters C_{p1} and C_{in} were obtained by laboratory measurements and data fitting; they are estimated to be 3.4 pF and 350 fF. Some tests were carried out to prove that the varactor biasing circuitry does not significantly increase the converter's noise floor. The CDC was also tested by generating the input capacitance with a trimmer capacitor instead of the varactor network. The trimmer capacitor does not require any resistor for biasing purposes. The noise power in the considered signal bandwidth may be assumed to be the same in both cases. The total input capacitance and its reciprocal were calculated for different bias conditions, as shown in Fig. 2(b), and the optimum point for linearity and sensitivity corresponds to a dc bias voltage on the varactor of 2.3 V; therefore, $V_b = 4.6$ V and $C_{MEMS} = 2.575$ pF at rest condition. Unfortunately, the linear range for the voltage-to-capacitance (or its reciprocal) conversion is quite small, as indicated in Fig. 2(b), due to the experimental setup. Here, we limited the ac signal to 120 mV_{rms}, which is equivalent to a capacitive signal with an amplitude of 56 fF. The resulting rest f_{osc} can be set to 15 MHz or 30 MHz depending on the MUX selection input.

V. MEASUREMENTS RESULTS

The prototype was fabricated in a CMOS 130-nm technology node and is shown in Fig. 3(a). The proposed CDC occupies just 0.025 mm^2 and is subdivided in the following manner: The OTA fills 44% of the

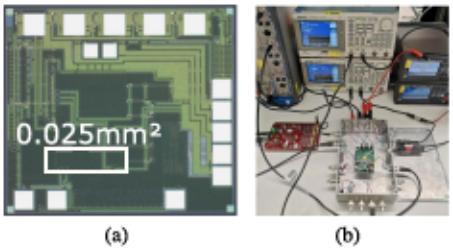

Fig. 3. (a) Micrograph of the fabricated prototype; the proposed CDC is highlighted in the white rectangle. (b) Measurement setup.

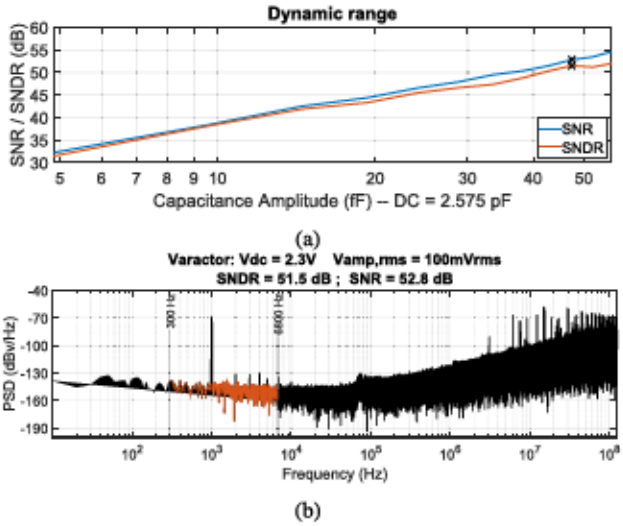

Fig. 4. (a) Measured DR of the fabricated CDC. (b) Output spectrum corresponding to the black crosses in (a); the tones highlighted in orange were used to compute the SNDR.

area, the capacitor C_A 22%, the digital blocks 18%, the current source 13%, the RO 2.5%, and the switches M1 and M2 0.5%. The rest of the chip area is used for auxiliary circuitry (LDOs, bandgap, etc.) and a noise shaper for standard 1-b pulse density modulation (PDM) compatibility. The analog power consumption is 247 µW (worst case when the FD is active and $f_{osc} = 30$ MHz) while the digital one is 96 µW, which was measured with a clock frequency of 3.072 MHz. This work's results were obtained by recording and sampling the oscillator output using an oscilloscope, as shown in Fig. 3(b), with an acquisition time of $T_{acq} = 100$ ms and a sampling frequency of $f_s = 250$ MHz; this choice is due to the focus on the capacitance-controlled oscillator performance rather than the F2D. The latter is equivalently executed in MATLAB by simulating DFFs and XOR gates, as explained in [18] to obtain a first-order ΣΔ ADC. Measured DR is shown in Fig. 4(a). The analog bandwidth for SNR and SNDR computation ranges from 300 Hz to 6.8 kHz, and the input signal frequency is 1 kHz. The input signal amplitude is reported as a capacitance value. In fact, this architecture is linear to the reciprocal of a capacitive signal, but in the reported input range (limited by the nonlinear varactor conversion), the distortion introduced by using capacitance instead of its reciprocal is negligible. The noise floor indicates an absolute resolution of $c_{res} = 130$ aF for a rest capacitance of $C_{MEMS} = 2.575$ pF, which corresponds to a relative measurement of $\log_2(\frac{C_{MEMS}}{c_{res}/\sqrt{2}}) = 14.7$ b. Peak SNDR is 51.5 dB due to the nonlinear voltage-to-capacitance conversion. The corresponding output spectrum, with a capacitive signal amplitude of 47 fF, is reported in Fig. 4(b). In-band noise is mainly due to the current source and OTA

Table 1. Comparison With the State of the Art

	[1]	[2]	[3]	[4]	This work
Architecture	SAR	CT-ΣΔ	CT-ΣΔ	Zoom	VCO-ΣΔ
Process [nm]	65	110	180	40	130
Area [mm^2]	0.08	0.033	0.42	0.06	0.025
Power [μW]	0.24	120	50.4	6.64	343
Conv. Time [ms]	0.02	1.2*	0.125*	0.0125	0.07*
Abs. Res. [aF]	6190	59	400	290	130
Rel. Res.** [bits]	10.3	14.6	13.6	14.1	14.7

* $\frac{1}{2BW}$. ** $\log_2\left(\frac{\text{Rest Capacitance}}{\text{Absolute Resolution in rms}}\right)$.

noise. The noise transfer function for the aforementioned sources (as well as the signal transfer function) is proportional to the FD parameter N; therefore, the FD is not able to improve the SNR. However, it may be used to shift upwards all the spectrum if a higher sensitivity is required regardless of the noise. A comparison with the state of the art can be found in Table I; as already explained, the SNDR of the proposed CDC is not limited by the architecture. Thus, the capacitance range information is not presented. Nevertheless, the prototype is a good proof of concept and shows results that are comparable with the state of the art. This architecture shows less energy efficiency compared to SAR-based or zoom ADCs, but it occupies a smaller area, and the relative resolution is competitive with the state of the art. Furthermore, it permits linear sensing of the capacitive sensor gap without requiring any biasing circuitry. Further improvement can be achieved by optimizing (or removing) the OTA in a future redesign.

VI. CONCLUSION

An innovative readout was proposed for capacitive sensors detecting gap variations. The architecture encloses the sensor in a loop and the sensor biasing circuitry is not required. This letter demonstrates the concept feasibility; a future redesign can improve power consumption and area occupation, reduce noise power, and introduce a differential configuration to improve the SNR performance. Therefore, the achieved resolution can be optimistically improved. A custom-made voltage-controlled capacitance based on a varactor and its biasing circuit was implemented for testing purposes; this method simplifies the input generation because the sensor is not required, but it limits the reported peak SNDR to 51.5 dB in the bandwidth from 300 Hz to 6.8 kHz.

ACKNOWLEDGMENT

The project funded from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No. 956601, involves the collaboration between Universidad Carlos III de Madrid and Infineon Technologies AG Austria. The authors would like to thank Niccolò De Milleri for the valuable contribution to this work. Funding for APC: Universidad Carlos III de Madrid (Read & Publish Agreement CRUE-CSIC 2023).

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