A current-source DC-AC converter and control strategy for grid-connected PV applications

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ABSTRACT

This paper presents a two-stage current-source DC-AC converter for grid-connected PV applications which is composed of an input step-up stage, followed by a step-down stage and an unfolding inverter. A decentralized control strategy of the DC-DC stage allows maximizing the renewable energy harvest using an Incremental Conductance MPPT algorithm and synthesizing an output current to be injected into the grid with low harmonic distortion. Double-loop PI controllers are used for the boost stage. The DC bus voltage of the buck stage is regulated using a PI controller, and an inner Proportional-Resonant (PR) controller tracks a sinusoidal reference. The PR controller proposed in this paper, includes a reduced number of resonant stages meeting the energy quality required by standards, which results in good stability margins. Finally, a SOGI-FLL algorithm synchronizes the inverter operation with the grid. Experimental results show an excellent dynamic response of the system, and the injected current complies with the IEEE Std. 1547–2018 specifications regarding harmonic content using a control law with a low computational burden.

1. Introduction

High renewable penetration on distributed energy systems, especially when integrated into a microgrid, is one of the leading research topics nowadays [1]. This situation has led to recent developments in power electronics that allow these systems to operate efficiently with a high power density and at low manufacturing costs, both in the medium [2,3] and low voltage grids [4,5] One of the most popular renewable energy resources for commercial and residential purposes, which has increased throughout the last decade, is solar power harvested through photovoltaic arrays (PV).

In the literature three approaches for power injection into the grid can be found: topologies based on an inverter operating as a voltage source (VSI), a quasi-impedance or impedance source converter [6] and current source inverters (CSI). In this article, the latter option is chosen, as it enables more accurate control of the harmonic content of the injected current despite the grid voltage harmonic distortion due to external factors. In addition, it is more resilient to short-circuits in the grid. Recently, some proposals for CSI inverters in grid-connected applications have been published. The Dual Active Bridge (DAB) converter can be used for grid-connected applications providing a galvanically

isolated DC stage from the grid [7]. It uses multiple switches and a complex control strategy. The article [8] presents a CSI consisting of an LC network on the DC side and a full-bridge inverter to interface the grid. Although DAB converter shows an adequate performance, its lack of a boosting stage limits its applications for PV systems. Then, a flyback-based converter is proposed [9], whose main advantage is that it can operate with high efficiency and reliability, but it implies a low transformer utilization and high overvoltages across the switching devices. The last issue can be solved by adding a snubber network, but the cost and complexity of the converter increase. A single-stage single-phase CSI is also presented [10], whose results show the compliance with the Standard IEEE-519. Still, the converter requires a double-tuned filter at its input and a large inductance of the output LC filter to achieve low distortion, which decreases the power density of the converter. Its dynamics also correspond to a high-order system, turning in a more complex control than other simpler topologies. Single-stage CSI has a significant drawback that requires a much larger DC inductor [11]. In addition, it does not have an additional stage capable of decoupling the instantaneous power unbalance between the grid and the PV array. This situation is depicted in [12], which presents a Model Predictive Controller (MPC) to reduce the power unbalance at twice the grid

frequency. Many power electronics topologies have been reviewed for PV applications [13]. Among them, the ones that do not need the use of a transformer are of principal interest nowadays [14,15] for their higher power density and low cost, as well as their reduced component count and higher power density.

It is well-known that DC-DC converters derived from the boost topology are of particular interest for PV systems since their constant input current feature allows the harvest of energy to be maximized [16,17]. One known issue of this topology is that it requires a proper control law design due to its non-minimum phase characteristic when controlling the output voltage.

The topology proposed in this paper belongs to the boost-buck derived topologies category, regarding a similar circuit as the Aalborg converter [18], but using a new modulation strategy that modifies the principle of operation and the electrical characteristic of the converter. This converter is adequate for these applications [19], but the THD of the injected current tends to be very high. The control strategy proposed in the present paper overcomes this drawback, which allows injecting power into the grid with a THD less than 5% and a harmonic content according to the IEEE Std. 1547–2018 [20]. A similar boost-buck converter for PV applications has been previously presented [21] using a modulation strategy that operates the converter as a boost or buck converter, which imposes different controllers to be constantly switching. On the other hand, the strategy presented in this article allows the input and output stages of the DC-DC converter to be decoupled thus independent controllers can be applied.

The DC-AC inverter is typically implemented by a full-bridge with a PWM modulation strategy. However, the need to meet power quality standards requires high-switching frequency to reduce the size of the output filters, resulting in higher switching losses. On the other hand, the output filters require that the cut-off frequency does not exceed a specific frequency to attenuate the PWM harmonics distortion and avoid their feedback to the control. These filters do not allow reducing their volume beyond a specific value. A full-bridge CSI is presented as an example [22]. A major drawback of such topology is that a complex modulation strategy is required to achieve low THD in the output current. The article [23] presents a full-bridge inverter implementing direct switching control using an MPC with an adaptive reference to circumvent the usual model parameter dependency of these controllers. This control law requires extensive and complex calculations to decide the switching sequences, whereas it is straightforward to implement the PWM modulation. A similar situation occurs using sliding mode controllers for a PV inverter [24]. However, the most relevant drawbacks of the direct switch modulation strategies are the variable switching frequency which increases the losses in the transistors and the filters due to the current ripples with varying amplitude. Furthermore, the control and filter bandwidth have enhanced complexity since the variable frequency may render them unstable or produce higher noise levels.

Another possibility is to use a line frequency-switched inverter, which works as an unfolding inverter for a premodulated current waveform, thus getting lower switching losses [25]. However, that paper presents neither an analysis of the voltage peak caused by a remanent current in the output inductor during the unfolder switching nor a proper snubber circuit design for the unfolder switches to undertake this voltage stress. In this article, a voltage unfolder is proposed to solve those issues that prevents the increased voltage stress while keeping the line frequency switched inverter operation. Moreover, it stands over their PWM and direct switch counterparts, as it has negligible conduction losses.

There are several control strategies for PV single-phase grid-connected systems proposed in the literature. Among them, some non-linear strategies like hysteresis [26] or sliding mode controllers [27,28] are found. Despite their well-behaved transient response, they require higher sampling frequencies than linear strategies to reduce the harmonic content in the injected current effectively. Other proposals include the model predictive controller strategy [29]. However, it

requires high accuracy in the mathematical model of the converter and the grid to ensure good performance, and it can also be affected by parameter uncertainties and unknown disturbances in the grid voltage. A fuzzy logic controller circumvents this parameter dependency alleviating the requirements in terms of parameter uncertainty. However, such controllers usually require the measure of the derivative of the error signal [30], which implies the addition of either a sensor or a complex estimation algorithm. The Interconnection and Damping Assignment Passivity-Based Control (IDA-PBC) is another recent strategy [31] which has low complexity and good performance. Nonetheless, it cannot control both the DC-bus voltage and the output current waveform independently. Then, the step-up stage is responsible for the control of the DC-bus voltage which is usually more difficult due to the non-minimum phase nature of the boost converter. Previous research [32] have stated the need for Resonant controllers when injecting low-distorted current into the grid. The main issue with these controllers is that their design is not straightforward since a high gain in some specific harmonic component may render the whole system unstable. One of the approaches consists of the application of Naslin polynomials [33], but this poses a significant problem when using multiple resonant stages due to the high-order equation system that tends to be inconsistent. LMI-based design is proposed to calculate the gains for the PR controllers, where model uncertainties and load disturbances are considered to ensure a robust operation [34]. However, its mathematical formulation requires a model for uncertainties and the specification of limits for disturbances, which leads to adopting approaches that are simpler to implement. A design approach that consists of the combination of a disturbance observer and a state feedback controller can be used [35]. It achieves a good transient performance in the presence of model uncertainty and disturbances, apart from the zero tracking error. However, the maximum order of the harmonic resonant stage that can be achieved is limited because obtaining a good dynamic response of the observer for higher-order harmonics is not straightforward. A scheduled gain proportional controller is added to a three-stage PR compensator to reduce the injected current THD, thus increasing the computational burden and design complexity [35]. The design already proposed [36] analyzes the expected time evolution of the sinusoidal output current and compares it to the reference, yielding the closed-loop transfer function in the frequency domain. The transfer function is then expressed as a canonical closed-loop form to extract the controller expression.

The main objective of the proposal is a topology with a control strategy for low-power and low-cost single-phase applications, which allows both the harvesting of photovoltaic solar energy efficiently and injecting the power into the grid with reduced harmonic content. It is a two-stage current-source DC-AC converter consisting of a DC-DC step-up stage cascaded with a step-down stage and an unfolding inverter for grid-connected PV applications. The former is controlled to track the maximum power of the PV array. In contrast, the latter controls the grid current to have a sinusoidal waveform by using a new modulation strategy that allows both of these stages to be controlled independently. The boost stage harvests the maximum available energy from the renewable source using an Incremental Conductance MPPT algorithm through double-loop PI controllers. The buck stage regulates the DC bus voltage using a PI compensator, and the grid current tracks a sinusoidal reference using an inner current loop which consists of a Proportional-Resonant controller. Therefore, the synthesized control law results in a very low computational cost.

In addition, this paper puts forward a novel design strategy for a Proportional-Resonant controller, including harmonic disturbance rejection, where the controller expression is obtained by comparing the desired response to the disturbances against the canonical sensitivity transfer function. The main advantage of this design technique is that only the settling time of the injected current is required. Furthermore, the resonant stages are established so that the current injected into the grid surpasses the limits imposed by international standards as a function of the operating range of the PV array. This results in minimum
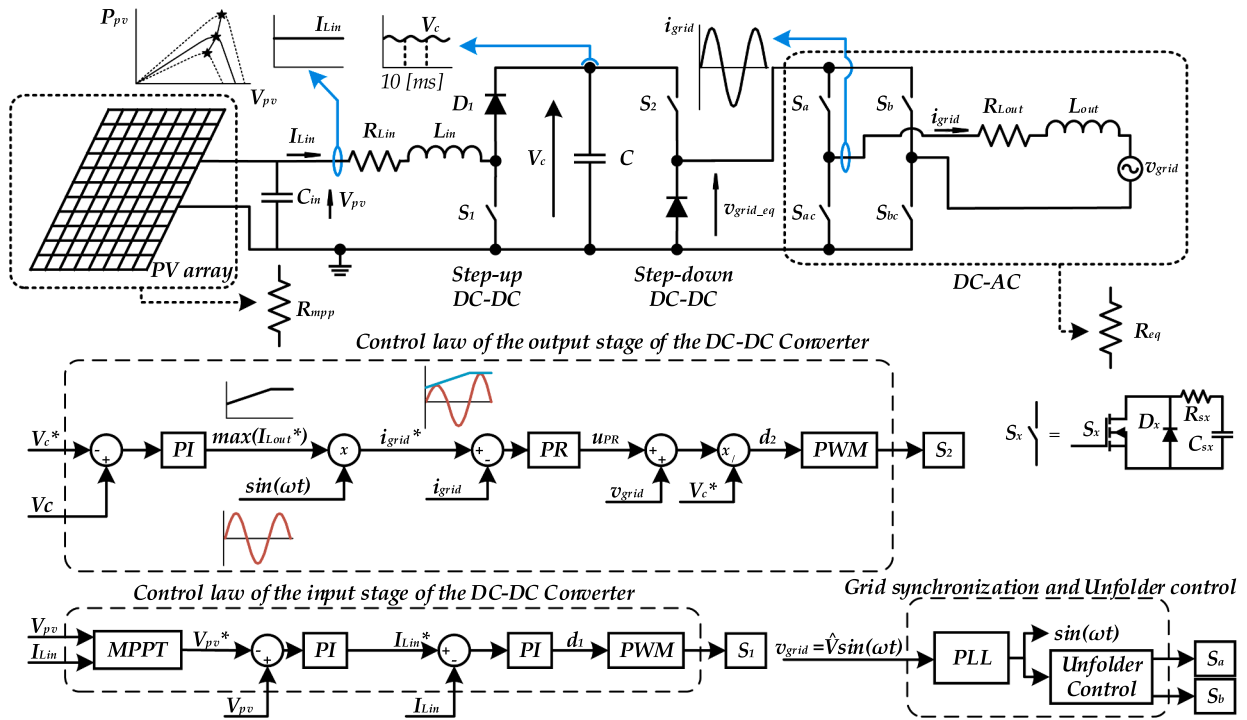
Fig. 1. Schematic circuit and control law of the proposed grid-connected PV system.

resonant stages to minimize degradation in the stability margins. Finally, the grid synchronization is accomplished using a SOGI-FLL (Second Order Generalized Integrator - Frequency Locked Loop) algorithm. Experimental testing is carried out to validate the converter design over a 500 W PV array. The results show a correct dynamic MPPT operation on the input side stage of the converter under changes in solar irradiation. Furthermore, the current injected into the grid presents a total and individual current harmonic content according to the IEEE Std. 1547–2018.

The paper's contributions correspond to a new modulation and control strategy of the current source DC-AC converter, capable of injecting the harvested power into the grid with low harmonic distortion and complying with power quality standards. In contrast to previous proposals, the proposed modulation strategy results in a new electric characteristic of the converter, which differs from the ones presented in the references, allowing the controllers from the input boost stage and the output buck stage to be decoupled, facilitating their design and tuning. In addition, the PR controller proposed in this paper includes a reduced number of resonant stages, which results in good stability margins. Another contribution of this article is the extension of the PR controllers design strategy proposed in [36 to compensate for harmonic distortion.

2. Proposed PV system

The proposed topology is shown in Fig. 1. It consists of a step-up and a step-down converter sharing a common DC bus, and an unfolding inverter at the output. The DC-DC converter makes both input and output current waveforms continuous, which allows the performance of the PV system to be improved. The step-down stage is controlled indirectly to output a sinusoidal current with the measurement of the grid current. Meanwhile, the line-frequency switched inverter, synchronized with the grid voltage zero crossings, unfolds the output voltage of the step-down stage to get the required AC voltage. In addition, the DC bus capacitor decouples the input and output currents allowing independent controllers to be implemented at both stages.
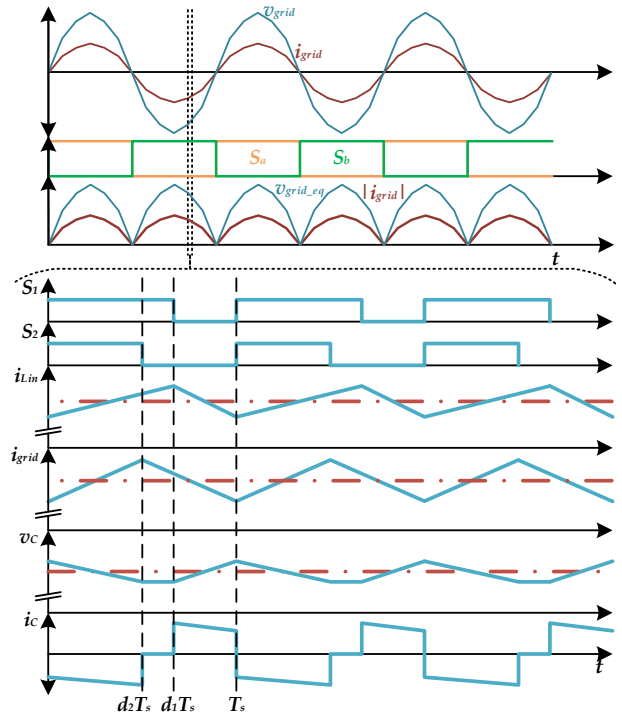

Fig. 2. Theoretical waveforms of the converter operation for power injection into a single-phase power grid and a detailed view of main waveforms of the boost and buck stages. From top to bottom: v_{grid}, i_{grid}, S_a, S_b, v_{grid_eq}, $|i_{grid}|$, S_1, S_2, i_{Lin}, i_{grid}, v_C and i_C. The average value for the input and output current and capacitor voltage is shown in red dashed lines.

2.1. Modeling of the DC-DC converter

The model of the DC-DC converter is derived by cascading a boost converter with a step-down converter [37], and fed by the PV array,

which is modelled as already suggested [38]. The equivalent circuit consists of a resistor R_{mpp} in parallel with the capacitor C_{in}. The resistance equals the ratio between voltage and current at the Maximum Power Point of the array, and despite being simple, it accurately models the dynamic response of the PV array when the operation is close to the maximum power. Furthermore, since the unfolding inverter is synchronized with the grid voltage, operation under unity power factor may be assumed, and hence the load can be modelled by an equivalent resistor R_{eq} as shown in Fig. 1.

Fig. 2 shows the unfolder switching signals S_a and S_b, the current I_{grid} and the output equivalent voltage v_{grid_eq} when power is injected into the grid with unity power factor. It also shows a particular case of the PWM signals of S_1 and S_2 switches, input and output currents (i_{Lin} and i_{Lout}), and voltage and current of the DC bus capacitor (v_c and i_c). The modulation strategy allows independent duty cycles, d_1 and d_2, for each switch. It results in three intervals during a switching period when these variables are different, $d_1 \neq d_2$.

In this paper, the small-signal analysis approach is adopted to derive the converter dynamics, where the nominal operation condition is evaluated at the maximum power point of the PV array. This approach allows the steady-state or DC terms, and dynamics or AC terms, to be obtained. The former are used to size passive components such as inductances and DC bus capacitors, and the latter are used to design the controllers. Both sets are depicted in (1)-(7).

DC Terms:

$$I_{Lin} = \frac{V_{PV} - V_C(1-d_1)}{R_{Lin}} \tag{1}$$

$$I_{grid} = I_{Lin}\frac{1-d_1}{d_2} \tag{2}$$

$$V_C = \frac{I_{grid}(R_{eq} + R_{Lout})}{d_2} \tag{3}$$

AC Terms:

$$\begin{cases} \dot{\hat{x}} = A\hat{x} + B\hat{u} \\ y = C\hat{x} + D\hat{u} \end{cases} \tag{4}$$

where:

$$\hat{x} = \begin{bmatrix} \hat{v}_{PV} \\ \hat{i}_{Lin} \\ \hat{i}_{grid} \\ \hat{v}_C \end{bmatrix}, \hat{u} = \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \end{bmatrix} \tag{5}$$

$$A = \begin{bmatrix} -\dfrac{1}{C_{in}R_{mpp}} & -\dfrac{1}{C_{in}} & 0 & 0 \\ \dfrac{1}{L_{in}} & -\dfrac{R_{Lin}}{L_{in}} & 0 & -\dfrac{1-d_1}{L_{in}} \\ 0 & 0 & -\dfrac{R_{Lout}+R_{eq}}{L_{out}} & -\dfrac{d_2}{L_{out}} \\ 0 & \dfrac{1-d_1}{C} & -\dfrac{d_2}{C} & 0 \end{bmatrix} \tag{6}$$

$$B = \begin{bmatrix} 0 & 0 \\ V_C & 0 \\ 0 & V_C \\ -I_{Lin} & -I_{grid} \end{bmatrix}, C = I_4, D = 0 \tag{7}$$

In this paper, the manipulated variables are the duty cycles of both legs of the converter. The chosen pairing is such that i_{Lin} is controlled with d_1 and i_{grid} with d_2.

From the state-space model, the following transfer functions can be obtained using the general expression $P(s) = C(sI_4 - A)^{-1}B + D$, as shown in (8), which are used in the next section to facilitate the tuning of the controllers.
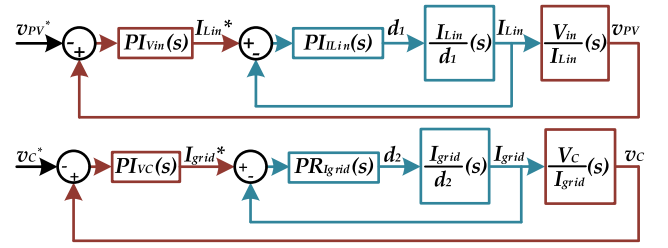

Fig. 3. Simplified block diagrams of the boost (top) and buck (bottom) stages of the converter.

$$P(s) = \begin{bmatrix} \dfrac{V_{PV}}{d_1}(s) & \dfrac{V_{PV}}{d_2}(s) \\[2mm] \dfrac{I_{Lin}}{d_1}(s) & \dfrac{I_{Lin}}{d_2}(s) \\[2mm] \dfrac{V_C}{d_1}(s) & \dfrac{V_C}{d_2}(s) \\[2mm] \dfrac{I_{grid}}{d_1}(s) & \dfrac{I_{grid}}{d_2}(s) \end{bmatrix} \tag{8}$$

3. Controller designs

This section presents the design of the proposed controllers shown in Fig. 1. The synthesis of the boost stage is performed using an inner input current control loop and an outer PV voltage control loop using PI controllers. The buck stage adopts a similar structure. An external loop regulates the DC bus voltage using a PI controller, and an inner output current loop tracks a sinusoidal current reference using a Proportional-Resonant (PR) controller.

Fig. 3 shows the block diagram of both subsystems, where the transfer functions that model each dynamic are expressed in (9)-(10), derived from the matrix transfer function given in (8). It is important to notice that the step-down stage duty cycle is calculated as the absolute value of the controller output d_2, and the voltage inversion is accomplished with the line-frequency switched unfolder circuit. It should be also noted that the outer control loops have positive feedback, where a positive increment at their input produces a decrease in their output. An equivalent system $G'(s) = -G(s)$, where $G(s)$ represents the system being controlled for each case is considered to simplify the design. The expression (11) shows the generalized closed-loop transfer function, which will be used to derive the controller expressions, $C(s)$.

$$\frac{V_{PV}}{I_{Lin}}(s) = \frac{V_{PV}}{d_1}(s)\left(\frac{I_{Lin}}{d_1}(s)\right)^{-1} \tag{9}$$

$$\frac{V_C}{I_{grid}}(s) = \frac{V_C}{d_2}(s)\left(\frac{I_{grid}}{d_2}(s)\right)^{-1} \tag{10}$$

$$T(s) = \frac{C(s)G'(s)}{1 + C(s)G'(s)} \tag{11}$$

3.1. DC-DC boost-stage controller

The reference of the PV array voltage is provided by an Incremental Conductance MPPT algorithm, which presents an adequate performance and robustness under parameter uncertainties [39]. Furthermore, it does not produce an oscillation in steady-state like the most commonly used P&O algorithms. Since the power variations of the PV array are slow compared with the dynamics of the converter, PI controllers are used in this work to meet the performance specifications in both inner and outer loops.

The design of both controllers can be performed in the frequency domain [40], applied to the experimental prototype whose main

Table 1
Parameters of the implemented converter prototype.

Parameter	Description	Value
P_{MPP}	PV Array Peak Power	500 [W]
V_{MPP}	MPP Voltage	60.6 [V]
I_{MPP}	MPP Current	8.33 [A]
f_s	Switching frequency	20 [kHz]
V_C	DC bus Voltage	150 [V]
L_{in}	Input Inductance	2.6 [mH]
L_{out}	Grid Inductance	2.7 [mH]
C	DC bus Capacitance	1.1 [mF]
R_{eq}	Grid Equivalent Resistor	9.8 [Ω]

a)

b)

Fig. 4. Bode plot of the open loop (continuous line) and the open loop with the designed controller (dashed line) transfer functions for (a) inner and (b) outer loop.

parameters are given in Table 1. The crossover frequency of the inner loop is set equal to a decade below the switching frequency to provide reasonably good switching harmonic attenuation $\omega_{c\_ILin} = 10\omega_s = 10\,2\pi\,20000 = 12566.37 rad.s^{-1}$.

The settling time is set at least at 1 [ms], which represents an adequate time response for the input current loop. The outer voltage controller is designed with a crossover frequency equal to a decade below the inner loop $\omega_{c\_Vpv} = \omega_{c_{ILin}}/10 = 1256.6 [rad.s^{-1}]$) to decouple the dynamics of both controllers. The phase margin for the voltage controller is set equal to 65° to get a damping ratio of $\zeta = 1/\sqrt{2}$ which provides both stability and a good transient response.

Because the controllers are implemented in a Digital Signal Controller (DSC), the design is completed in the discrete-time domain.

Table 2
Boost stage controller gains.

Gain	Value
K_{P_ILin}	0.191
K_{I_ILin}	409.9
K_{P_VPV}	4.310^{-5}
K_{I_VPV}	173.5

The transfer functions of the system are discretized using the zero-order hold (ZOH) method considering a unit delay and a sampling frequency of 20 kHz. The trapezoidal rule is chosen as the integration method, where a high correlation with the continuous-time domain is obtained.

Fig. 4a and Fig. 4b show the resulting open-loop Bode plots of both $I_{Lin}/d_1(z)$ and V_{PV}/I_{Lin} (z) transfer functions and with their respective discrete-time PI controllers. The gains obtained from the design procedure for both controllers are summarised in Table 2.

3.2. DC-DC buck-stage controller

Considering a 50 Hz grid frequency, the capacitor voltage presents a 100 Hz ripple produced by the instantaneous difference between the rectified sinusoidal output current and the input current delivered by the PV array. Therefore, a notch filter with a center frequency of 100 Hz is used to prevent the capacitor voltage ripple from affecting the performance of the output-current controller. Furthermore, the outer controller is tuned with a slow transient response to avoid fast changes in the output current amplitude, adopting in this study a bandwidth equal to $1/5\omega_0$, where ω_0 is the grid frequency.

The current reference is obtained by multiplying the amplitude of the reference obtained by the outer loop and a unit sinusoidal waveform whose phase reference is provided by the output of the PLL algorithm. The PLL is implemented with a SOGI-FLL scheme, consisting of a Second Order Generalized Integrator as the oscillator and a Frequency-Locked Loop that controls the SOGI output frequency to lock the output waveform in phase with the input. This algorithm is highlighted in [41] because it is as efficient as other state-of-the-art strategies, but with a lesser computational burden.

The design of the PR controller is carried out considering the output current reference to be a sinusoidal waveform as given in (12), where the frequency is equal to $\omega_0 = 2\pi 50 [rad.s^{-1}]$.

The transient response of the output current is modelled as a sinusoidal waveform whose amplitude envelope converges exponentially to the reference with a settling time of $t_c = 1/\omega_c$ as expressed in (13) [36]. Finally, expressions (14) and (15) represent the Laplace transform for both terms.

$$i^*_{grid}(t) = A\,\sin(\omega_0 t) \tag{12}$$

$$i_{grid}(t) = A(1 - e^{-\omega_c t})\sin(\omega_0 t) \tag{13}$$
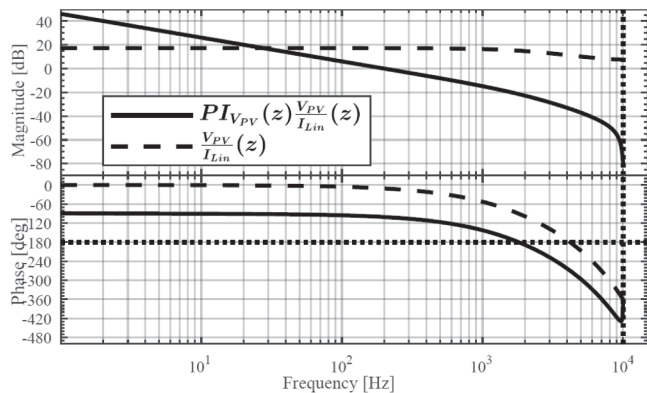
$$I^*_{grid}(s) = \frac{A\,\omega_0}{s^2 + \omega_0^2} \tag{14}$$

$$I_{grid}(s) = \left(\frac{A\omega_0}{s^2 + \omega_0^2}\right)\left(\frac{2\omega_c s + \omega_c^2}{(s + \omega_c)^2 + \omega_0^2}\right) \tag{15}$$
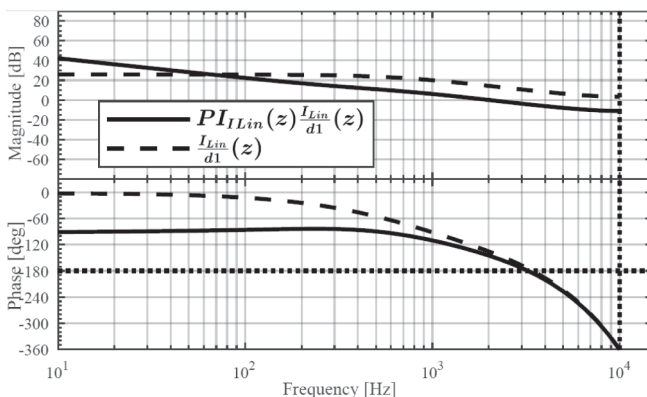
In order to obtain the controller expression, the closed-loop transfer function given in (16) is matched with the canonical equation (11), and so, the open-loop expression given in (17) can be obtained.

$$\frac{I_{grid}(s)}{I^*_{grid}(s)} = \frac{2\omega_c s + \omega_c^2}{(s + \omega_c)^2 + \omega_0^2} = \frac{\frac{2\omega_c s + \omega_c^2}{s^2 + \omega_0^2}}{1 + \frac{2\omega_c s + \omega_c^2}{s^2 + \omega_0^2}} \tag{16}$$

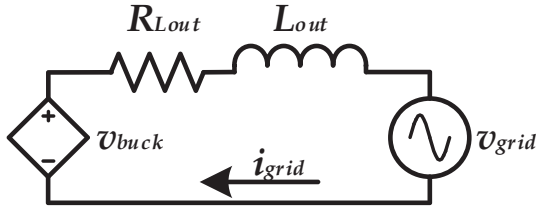$$C(s)G(s) = C(s)\frac{I_{grid}}{d_2} = \frac{2\omega_c s + \omega_c^2}{s^2 + \omega_0^2} \tag{17}$$

Fig. 5. Simplified model of the output stage of the converter.

The controller can be determined from the last expression. For that purpose, the model of the output stage of the converter connected to the grid shown in Fig. 5 is used. The output voltage of the buck stage is expressed as $v_{buck}(t) = d_2(t) v_C(t)$, resulting in the following equation:

$$L_{out} \frac{di_{grid}}{dt} = d_2(t) v_C(t) - i_{grid} R_{Lout} - v_{grid}(t) \tag{18}$$

The duty cycle d_2, and thus the output voltage v_{buck}, is composed of two terms: one to cancel out the grid voltage (v_{grid}), and another (u_{PR}) to enforce the current according to the reference signal.

$$d_2(t) = \frac{u_{PR}(t) + v_{grid}(t)}{V_C^*} \rightarrow L_{out} \frac{di_{grid}}{dt} = u_{PR}(t) - i_{grid} R \tag{19}$$

By replacing (19) in (18) and applying the Laplace transform, the following transfer function of the system can be obtained,

$$G(s) = \frac{I_{grid}(s)}{u_{PR}} = \frac{1}{L_{out} s + R_{Lout}} \tag{20}$$

Now replacing (20) in (17) and solving for $C(s)$ yields the controller expression (21) which can be rearranged as shown in (22), corresponding to a Proportional-Resonant structure.

$$C(s) = \frac{2 L_{out} \omega_c s^2 + (L_{out} \omega_c^2 + 2\omega_c R_{Lout})s + R_{Lout}\omega_c^2}{s^2 + \omega_0^2} \tag{21}$$

$$C(s) = K_P + \frac{K_{r1a}s + K_{r1b}}{s^2 + \omega_0^2} \approx K_P + \frac{K_{r1a}s + K_{r1b}}{s^2 + \omega_b s + \omega_0^2} \tag{22}$$

$K_P = 2 L_{out}\omega_c, \; K_{r1a} = L_{out}\omega_c^2 + 2\omega_c R_{Lout}$ and $K_{r1b} = R_{Lout}\omega_c^2 - 2 L_{out}\omega_c \omega_0^2$

The damping term ω_b is added to improve the stability and robustness against small frequency oscillations in the power grid.

Owing to the blanking time introduced in the switching signals of the unfolding inverter and unmodelled non-linearities such as the forward voltage of the diodes and transistors, a third-order harmonic distortion in the converter output current can be generated, which is observed as a deformation at the zero-crossings of the grid current [42]. Furthermore, the harmonic content in the grid voltage can also distort the injected current. For this reason, the control strategy must be able to reject these harmonic components to make it able to comply with the IEEE Std. 1547–2018.

For that purpose, a similar design can be carried out for the harmonic rejection using (23) as the expected harmonic currents time evolution. The difference now is that the reference for the harmonic components is equal to zero, and then it is not possible to find a closed-loop transfer function. However, analyzing the expression (24) it is clear that the first term of the summation is a sinusoidal waveform of amplitude B_k and frequency $(2k+1)\omega_0$.

This is actually the sum of the harmonic disturbances ($\sum_{k=1}^{N} P_k(s)$), and after dividing both sides of the equation by the disturbances (25), the remaining term can be compared to the canonical sensitivity expression (26) that relates the response of the system under disturbances. The process from now on is similar to the case for reference tracking; the open-loop expression (27) is obtained and the transfer functions of the controller are derived in (28).
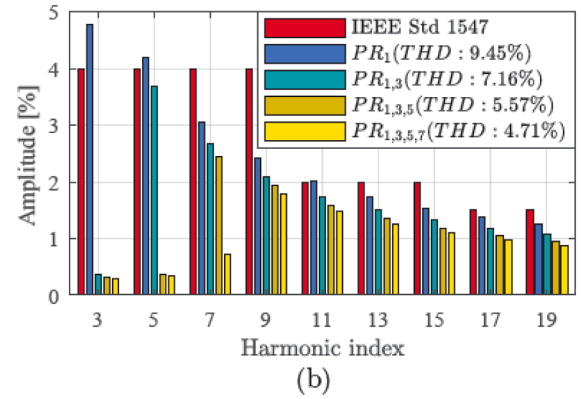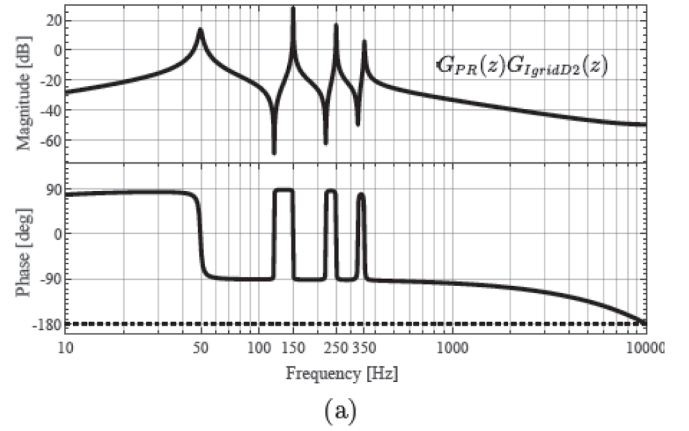

(a)

(b)

Fig. 6. (a) Bode plot of the open loop transfer function of the output stage and the PR controller. (b) Comparison between harmonic components (as a percentage of the fundamental) and THD of the output current with the proposed control strategy using a different number of resonant stages, and the IEEE Std. 1547–2018 limits for each harmonic component.

$$i_{grid}(t) = \sum_{k=1}^{N} B e^{-\omega_{ck}t} \sin((2k+1)\omega_0 t) \tag{23}$$

$$I_{grid}(s) = \sum_{k=1}^{N} \frac{B_k(2k+1)\omega_0}{s^2 + ((2k+1)\omega_0)^2} \frac{1}{1 + \frac{2\omega_c s + \omega_c^2}{s^2 + ((2k+1)\omega_0)^2}} \tag{24}$$

$$\frac{I_{grid}(s)}{\sum_{k=1}^{N} P_k(s)} = \sum_{k=1}^{N} \frac{1}{1 + \frac{2\omega_c s + \omega_c^2}{s^2 + ((2k+1)\omega_0)^2}} \tag{25}$$

$$S(s) = \frac{1}{1 + C(s)G(s)} \tag{26}$$

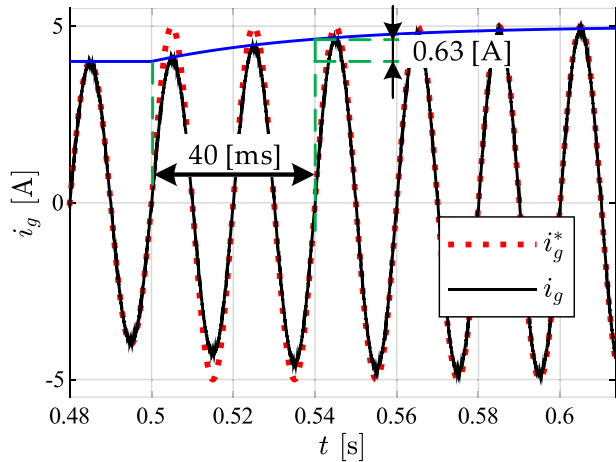$$C(s)G(s) = \frac{2\omega_c s + \omega_c^2}{s^2 + ((2k+1)\omega_0)^2} \tag{27}$$

$$C(s) = \sum_{k=2}^{N} K_{Pk} + \frac{K_{rka}s + K_{rkb}}{s^2 + \omega_{bk}s + ((2k-1)\omega_0)^2} \tag{28}$$

Fig. 6a shows the Bode plot of the open-loop transfer function of the system with the PR controller proposed in this paper. The number of resonant stages is such that the output current waveform surpasses the limits on the harmonic content imposed by the IEEE Std. 1547–2018, considering a grid voltage which consists of a fundamental component of 50 Hz with harmonic components of fifth and seventh order, whose amplitudes are 2.5 % with respect to the fundamental.
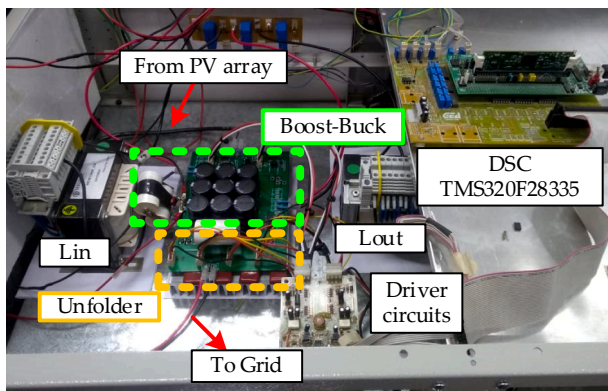
In this paper, resonant stages are applied for the 3rd, 5th, and 7th

Table 3
Step-down stage controller gains.

Gain	Value	Gain	Value
t_{c1}	$40[ms]$	t_{c3}	$70[ms]$
K_{r1a}	26.625	K_{r3a}	14.816
K_{r1b}	$-1.254 10^4$	K_{r3b}	$-6.588 10^4$
K_{P1}	0.130	K_{P3}	0.074
ω_{b1}	$6.283[s^{-1}]$	ω_{b3}	$3.142[s^{-1}]$
Gain	Value	Gain	Value
t_{c5}	$80[ms]$	t_{c7}	$80[ms]$
K_{r5a}	12.906	K_{r7a}	12.906
K_{r5b}	$-1.603 10^5$	K_{r7b}	$-3.143 10^5$
K_{P5}	0.065	K_{P7}	0.065
ω_{b5}	$3.142[s^{-1}]$	ω_{b7}	$12.566[s^{-1}]$

Table 4
Main features of the solar panel as specified by the manufacturer.

Parameter	Description	Value
$^P MPP$	PV Array Peak Power	500 [W]
$^V MPP$	MPP Voltage	60.6 [V]
$^I MPP$	MPP Current	8.33 [A]
$^V OC$	Open Circuit Voltage	38 [V]
$^I SC$	Short-Circuit Current	8.75 [A]
N_C	Cell Number	60
–	Cell Type	Polycrystalline 156x156 [mm]

Fig. 7. Time-domain simulation results of the grid current (continuous black line) when the current reference suddenly changes from 4 A to 5 A (red dashed line) at time t = 0.5 s. The envelope of the current waveform (continuous blue line) increases by 63% of the step amplitude in 40 [ms].
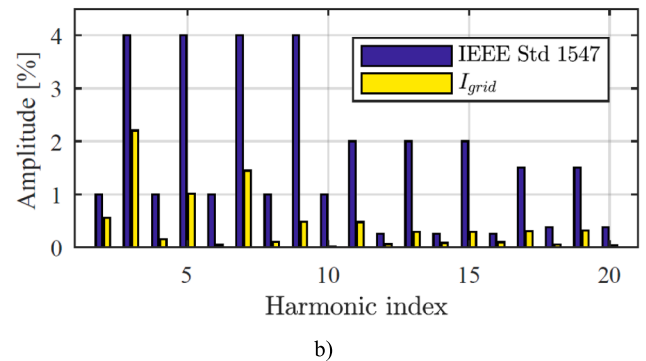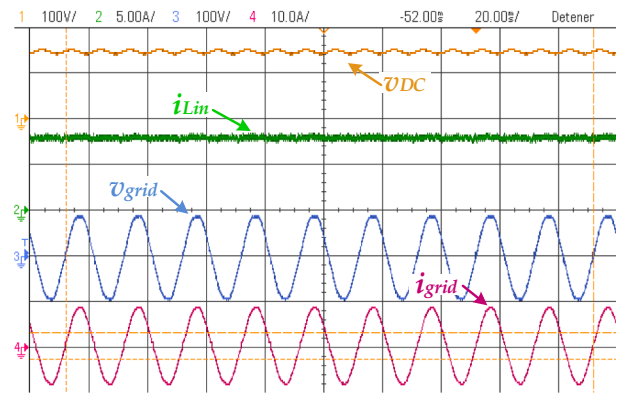

Fig. 8. Photograph of the implemented converter prototype.

a)

b)

Fig. 9. Experimental result of the converter for the rated operation condition: (a) steady-state time-domain response. (b) percentage of the grid current harmonic content compared to the IEEE Std. 1547–2018 limits.

40 *ms* which is in concordance with the design.

The controllers' equations (22) and (28) are taken to the *z* domain using the pre-warped bilinear transform to ensure the resonant peaks are mapped to the same frequencies. For this mapping, the complex variable *s* is replaced as shown in (29).

$$s = \frac{\omega_{PW}}{\tan(0.5\omega_{PW}T_s)} \frac{z-1}{z+1} \tag{29}$$

where: ω_{PW} is the pre-warping frequency and T_s the sampling period.

4. Experimental results

This section presents the experimental results using the prototype shown in Fig. 8 and whose parameters are presented in Table 1. The main features of the PV array are listed in Table 4. The input and output inductors and DC bus capacitor were designed considering 10% current ripples and 5% voltage ripple, respectively. The unfolding inverter consists of a full-bridge converter whose switching signals are synchronized with the zero-crossings of the grid voltage. Since the output current may not be exactly zero when switching occurs, the residual energy stored in L_out must be handled by the snubber circuits of the

harmonics, in addition to the fundamental frequency. The number of stages was selected based on an evaluation through simulation, adding additional resonant stages until the specifications were met. This process is depicted in Fig. 6b. It can be observed that both the THD is under 5% and every harmonic component is below the corresponding limit of the Standard fulfills when resonant stages are applied at the fundamental frequency and the 3rd, 5th, and 7th harmonics. Hence, the controller has a minimum number of resonant stages. The controller gains are calculated using the values presented in Table 1 and summarised in Table 3. Fig. 7 shows simulation results of the grid current time response after an output current reference step from 4[A] to 5[A]. It increases by 63% in
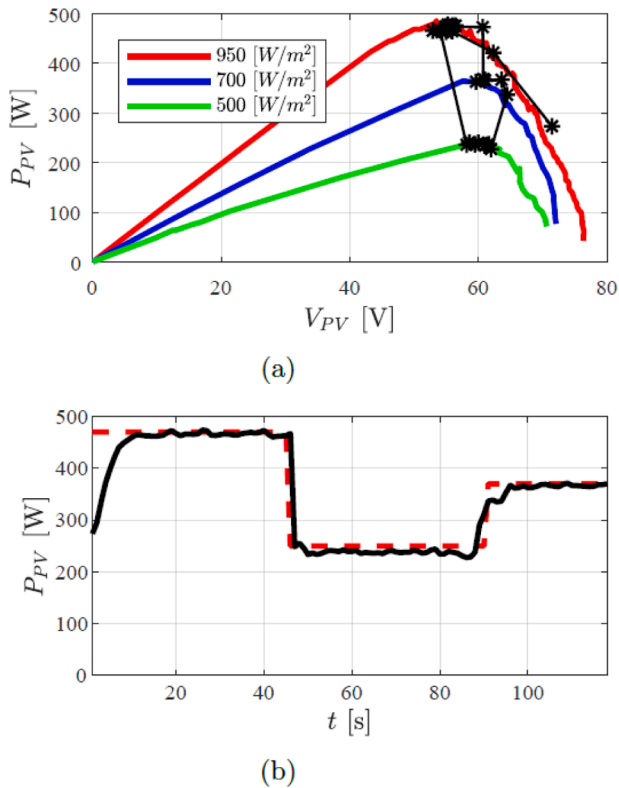
Fig. 10. MPPT performance under irradiance changes. a) Operation points sliding along P vs V curves due to MPPT operation under changes in irradiation. b) Time evolution of Solar irradiance (red dashed line) and Power extracted from the PV array (continuous black line).
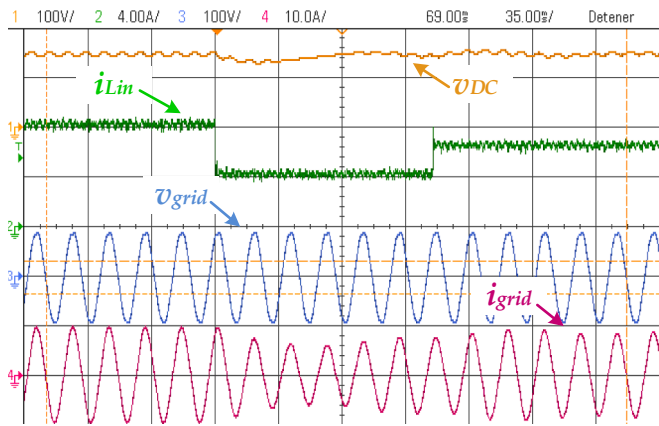

Fig. 11. Experimental test of the prototype converter with input current steps. From top to bottom: DC Bus voltage, Input current, Grid Voltage, and Grid Current. The MPPT algorithm is disabled to analyze the output current response time under sudden changes of the input current.

inverter during the blanking time of the switching signals. In this article, $R_s = 10 [\Omega]$ and $C_s = 1 [\mu F]$ (see Fig. 1) were used, for a maximum over-voltage of 10% assuming a residual current of 1 A, which is in concordance with the experimental results.

Fig. 9a shows the experimental result corresponding to the steady-state operation of the converter for the rated operation condition described in Table 1. This figure shows the DC-bus voltage, input current, and the grid voltage and current waveforms. The measured total harmonic distortion of the grid current results equal 3.37%, lower than the 5% limit imposed by the IEEE Std. 1547–2018. In addition, the
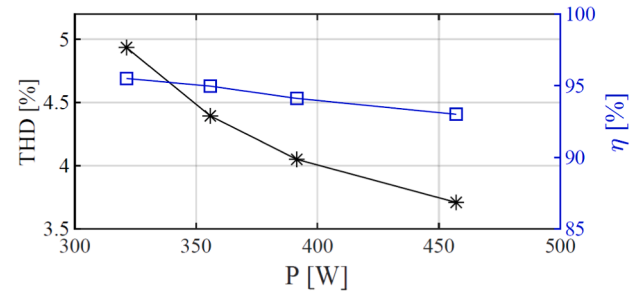

Fig. 12. THD [%] of I_{grid} (left axis) and efficiency [%] (right axis) with respect to the output power.

Table 5
THD [%] OF i_{grid} and efficiency [%] with respect to the output power.

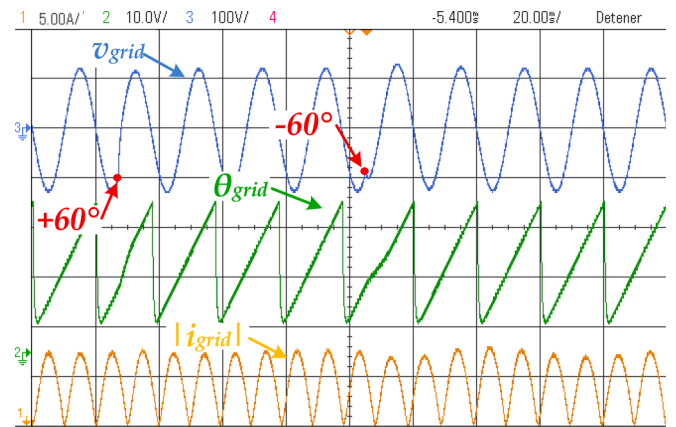| Output power [W]	THD [%]	η [%]
452.12	3.71	91.52
391.46	4.05	94.12
355.85	4.39	94.97
321.32	4.93	95.51

Fig. 13. Experimental verification of SOGI-FLL under a phase angle step variation of + 60 [°] and −60 [°]. From top to bottom: grid voltage (blue), grid phase angle (green), and $|i_{grid}|$ (yellow).

individual harmonic components' amplitudes are lower than the limits as shown in Fig. 9b.

The performance of the MPPT algorithm under varying irradiance conditions is shown in Fig. 10a, where the evolution of the PV power vs. voltage is presented. This result is obtained by covering the solar cells with sheets of material with different opacity, resulting in irradiances of 950, 700, and 500 $[W/m^2]$. The figure also shows the PV panel curves for the same irradiance conditions, previously characterized and added in the figure for comparison purposes. This result indicates that the adopted MPPT algorithm allows harvesting the maximum power available at each irradiance level. Fig. 10b shows the time evolution of the irradiance and the output power of the PV array processed from the voltage and current measurements. Again, it can be seen that the system reaches the MPP quickly.

With the aim to verify the operation of the controller under an extreme scenario in terms of stability, the MPPT algorithm was disabled and sudden input current reference changes were set. Fig. 11 shows the experimental transient response, where each input current reference was established according to the previous MPPT test. The result shows that both the outer and inner control loops of the output stage of the boost-buck converter work adequately, and the DC-bus voltage controller rejects the perturbation of the input current increasing or

Table 6
Comparison of the proposed converter with other single-phase CSI.

Reference	[18]	[8]	[10]	[22]	[44]	nnn	**Proposed**
High frequency switches	2	4	4	4	7	2	2
Low frequency switches	4	0	0	0	0	2	4
Additional diode	4	4	4	10	3	4	2
No. of C	3	3	3	5	5	1	2
No. of L	3	3	4	3	5	4	2
Rated power	2[kW]	250[W]	500[W]	900[W]	300[W]	1[kW]	500[w]
Reported THD	N/A	4.78%	2.73%	1.8%	N/A	3.2%	3.37%
Maximum reported efficiency	97%	89%	95%	94%	94%	99%	95.5%

decreasing the output current amplitude. The output current controller remains stable in all cases and with an overshoot of less than 20%.

Finally, the harmonic content of the output current and the converter efficiency were obtained for different power transfers using the designed controller, whose results are presented in Fig. 12 and tabulated in Table 5 for further clarification. It can be observed that the THD decreases while the power increases, and it remains lower than the limits of 5% in the range of interest, using minimum resonant stages in the output current controller. Although it shows a decreasing efficiency with respect to the power transfer, it remains above 90% for all the tested cases, and it is important to note that the usage of lower resistance inductors may enhance the overall efficiency of the converter.

The experimental results shown in Fig. 13 corresponds to a phase step increase of $+60$ [°] and another one of -60 [°] after 3 grid voltage cycles, approximately. It can be seen that the algorithm can follow the output signal after a transient period lasting about 100 [ms], which matches the designed settling time of the algorithm. This result proves the robustness of this strategy since the disturbances simulated are more significant than expected in a power grid.

5. Conclusions

This paper presented a low-cost and low-power single-phase power DC-AC converter for grid-connected PV arrays and its control strategy. The topology is based on a boost-buck converter and an unfolding inverter interfaced with the power grid, allowing high power density. The proposed modulation strategy allowed the controllers from the input step-up stage and the output step-down stage to be decoupled, facilitating their design and tuning. This also allows the non-minimum phase issue of the boost stage to be avoided, controlling only the input current through a double-loop PI controller. The PR controller for harmonic compensation was based on the envelope settling time to design the resonant stages according to the standard specifications of individual harmonic contents. Finally, the topology and the proposed controller were experimentally tested using a prototype of 500 W.

The results show total concordance with the standard IEEE Std. 1547–2018 specifications regarding power quality for grid current injection. In addition, the controller was tested under several simulated irradiance conditions to verify the operation of the converter under the worst-case scenario. The results showed a fast and stable dynamic response. Finally, the input stage controller showed good performance in MPP tracking of the PV array, even under significant changes in solar irradiation. Table 6 shows a comparison between the proposed converter and other CSI topologies. It shows that the proposal of this article stands out using fewer switches and passive filters while maintaining a reduced THD in the grid current to meet power quality standards. Similar current distortions have been also achieved with more complex PR controllers like those previously proposed in [35] or [43], achieving good harmonic rejection and tracking performance with a simple PR controller.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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